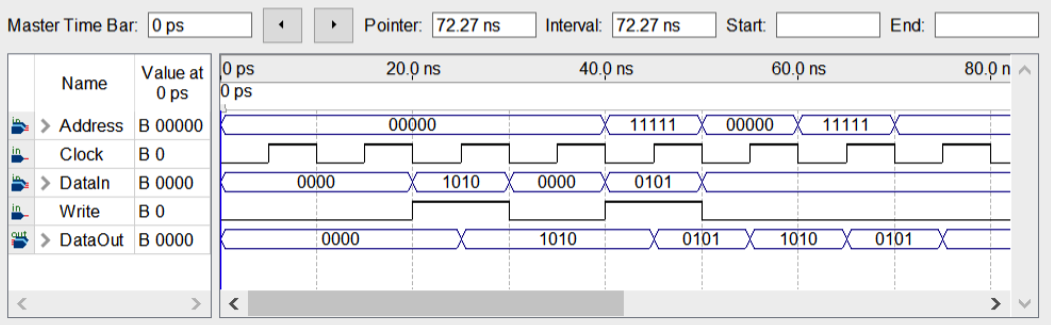
**Lab 7**

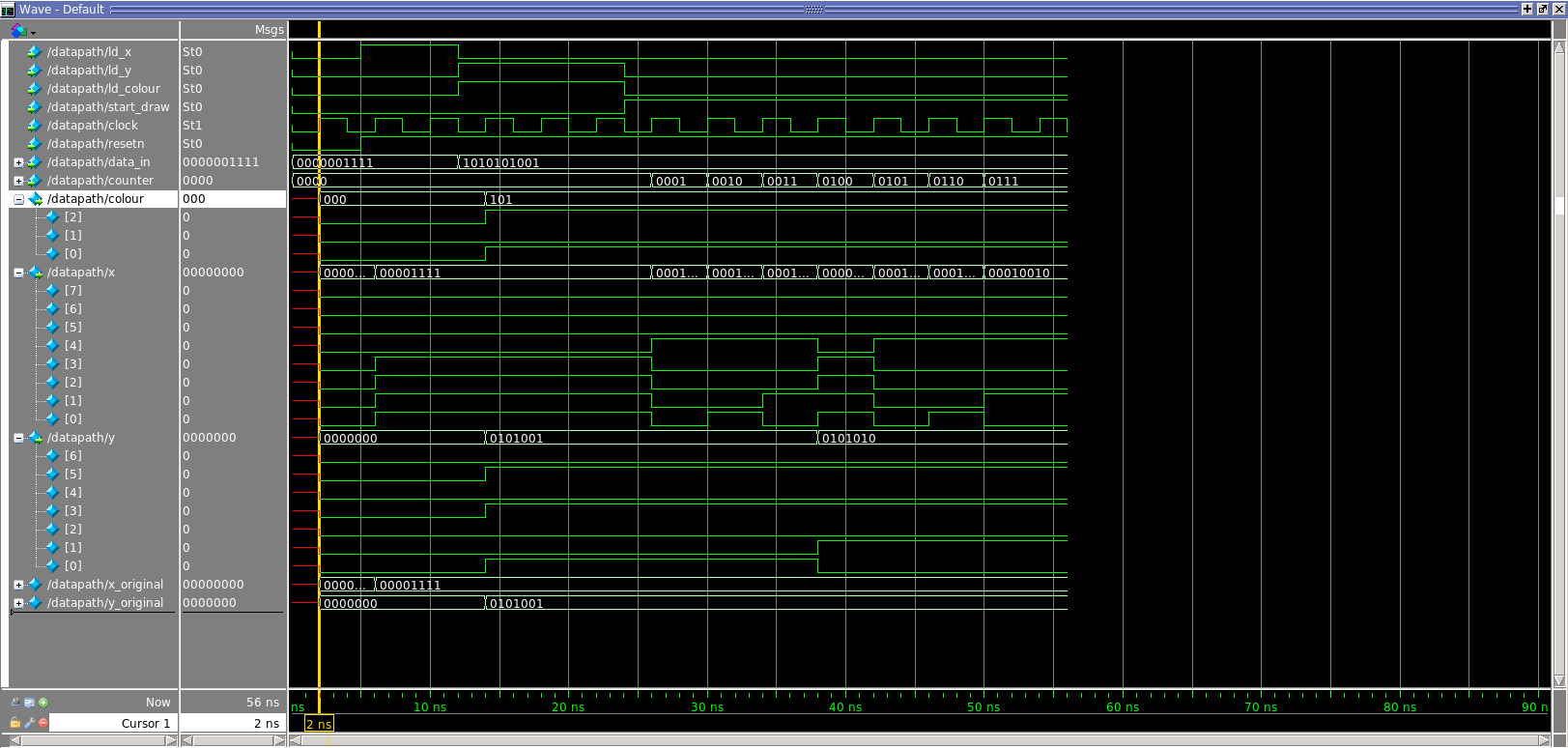
**Part 1.**



“include "ram32x4.v”  
  
module lab7p1 (input [[9:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B9%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) SW, input [[1:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B1%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) KEY, output [[6:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B6%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) HEX0, output [[6:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B6%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) HEX2, output [[6:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B6%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) HEX4, output [[6:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B6%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) HEX5);  
wire [[3:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B3%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) data;  
assign data[[3:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B3%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) = SW[[3:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B3%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank);  
wire [[4:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B4%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) address;  
assign address[[4:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B4%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) = SW[[8:4]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B8%3A4%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank);  
wire wren;  
wire clock;  
assign wren = SW[9];  
assign clock = KEY[0];  
  
wire out\_value;  
  
ram32x4 ram\_ist(  
.address(address),  
.clock(clock),  
.data(data),  
.wren(wren),  
.q(out\_value)  
);  
  
// === Display the output  
  
// the data output of the memory  
hex\_decoder H0(   
.hex\_digit(out\_value),  
.segments(HEX0)  
);  
  
// the data input of the memory   
hex\_decoder H2(  
.hex\_digit(data),  
.segments(HEX2)  
);  
  
// Display the address   
hex\_decoder H4(   
.hex\_digit(address[[3:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B3%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank)),  
.segments(HEX0)  
);  
  
// Display the remaining bit of the address.   
hex\_decoder H5(  
.hex\_digit(address[4]),  
.segments(HEX1)  
);  
  
endmodule  
  
module hex\_decoder(input [[3:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B3%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) hex\_digit, output reg [[6:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B6%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank)segments);  
always @(\*)  
case (hex\_digit)  
4'h0: segments = 7'b100\_0000;  
4'h1: segments = 7'b111\_1001;  
4'h2: segments = 7'b010\_0100;  
4'h3: segments = 7'b011\_0000;  
4'h4: segments = 7'b001\_1001;  
4'h5: segments = 7'b001\_0010;  
4'h6: segments = 7'b000\_0010;  
4'h7: segments = 7'b111\_1000;  
4'h8: segments = 7'b000\_0000;  
4'h9: segments = 7'b001\_1000;  
4'hA: segments = 7'b000\_1000;  
4'hB: segments = 7'b000\_0011;  
4'hC: segments = 7'b100\_0110;  
4'hD: segments = 7'b010\_0001;  
4'hE: segments = 7'b000\_0110;  
4'hF: segments = 7'b000\_1110;  
default: segments = 7'h7f;  
endcase  
endmodule

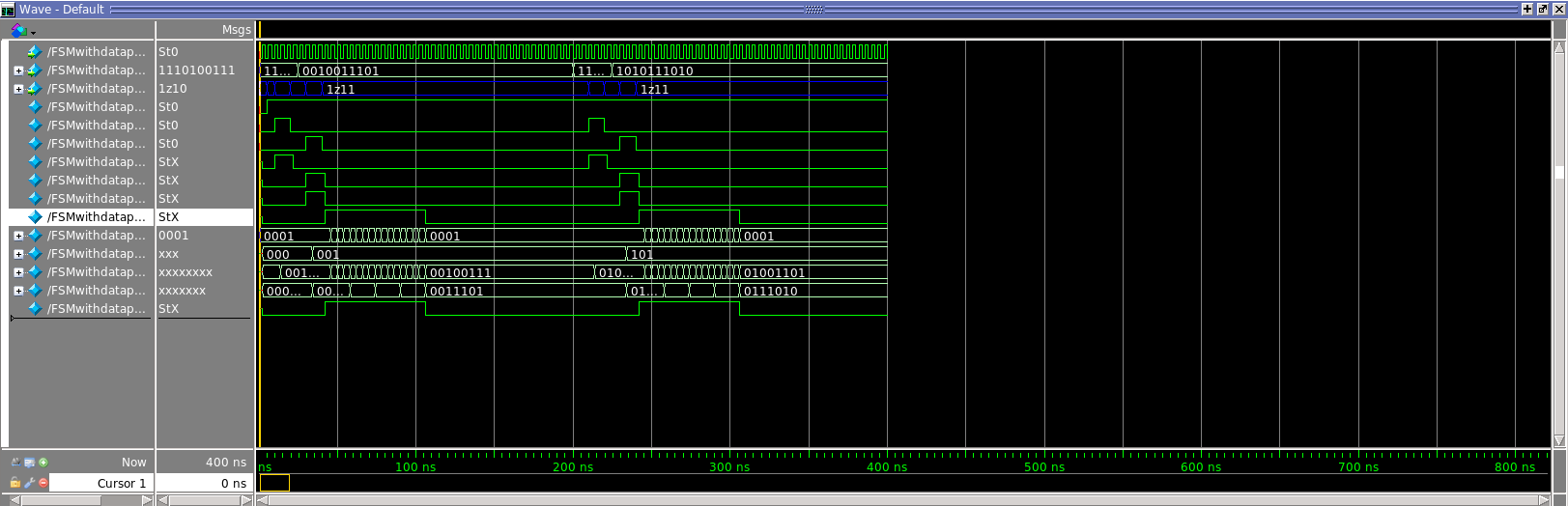
**Part 2.**

1. Datapath



module datapath(  
input ld\_x, ld\_y, ld\_colour,  
input start\_draw,  
input clock,  
input resetn,  
input [[9:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B9%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) data\_in,  
input [[3:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B3%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) counter,  
output reg [[2:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B2%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) colour,  
output reg [[7:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B7%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) x,  
output reg [[6:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B6%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) y  
);  
reg [[7:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B7%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank)x\_original;  
reg [[6:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B6%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank)y\_original;  
always @ (posedge clock) begin  
if (!resetn) begin  
x <= 8'b00000000;   
y <= 7'b0000000;   
colour <= 3'b000;  
x\_original <= 8'b00000000;  
y\_original <= 7'b0000000;  
end  
else begin  
if (ld\_x)begin  
x\_original <= {1'b0, data\_in[[6:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B6%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank)};  
x <= {1'b0, data\_in[[6:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B6%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank)};  
end  
if (ld\_y && ld\_colour) begin  
y <= data\_in[[6:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B6%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank);   
y\_original <= data\_in[[6:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B6%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank);   
colour <= data\_in[[9:7]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B9%3A7%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank);  
end  
if (start\_draw) begin  
x <= x\_original + counter[[1:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B1%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank);  
y <= y\_original + counter[[3:2]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B3%3A2%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank);  
end  
end  
end  
endmodule

2. FSM



module FSMwithdatapath  
(  
CLOCK\_50,  
KEY,  
SW  
);  
  
input CLOCK\_50; // 50 MHz  
input [[9:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B9%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) SW;  
input [[3:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B3%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) KEY;  
  
// Declare your inputs and outputs here  
// Do not change the following outputs  
wire resetn;  
assign resetn = KEY[0];  
wire load\_x;  
assign load\_x = ~KEY[3];  
wire load\_y;  
assign load\_y = ~KEY[1];  
wire ld\_x,ld\_y,ld\_colour,start\_draw;  
wire [[3:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B3%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) counter;  
// Create the colour, x, y and writeEn wires that are inputs to the controller.  
wire [[2:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B2%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) colour;  
wire [[7:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B7%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) x;  
wire [[6:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B6%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) y;  
wire writeEn;  
  
// Create an Instance of a VGA controller - there can be only one!  
// Define the number of colours as well as the initial background  
// image file (.MIF) for the controller.  
// Put your code here. Your code should produce signals x,y,colour and writeEn/plot  
// for the VGA controller, in addition to any other functionality your design may require.  
  
// Instansiate datapath  
datapath d0(  
.ld\_x(ld\_x),  
.ld\_y(ld\_y),  
.ld\_colour(ld\_colour),  
.start\_draw(start\_draw),  
.resetn(resetn),  
.clock(CLOCK\_50),  
.data\_in(SW[[9:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B9%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank)),  
.counter(counter),  
.colour(colour),  
.x(x),  
.y(y)  
);  
  
// Instansiate FSM control  
control c0(  
.resetn(resetn),  
.clock(CLOCK\_50),  
.load\_x(load\_x),  
.load\_y(load\_y),  
.ld\_x(ld\_x),  
.ld\_y(ld\_y),  
.ld\_colour(ld\_colour),  
.start\_draw(start\_draw),  
.plot(writeEn),  
.counter(counter)  
);  
  
endmodule  
  
module control(  
input resetn,  
input clock,  
input load\_x,  
input load\_y,  
output reg ld\_x, ld\_y, ld\_colour,  
output reg start\_draw,  
output reg plot,  
output reg [[3:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B3%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) counter = 4'b0001  
);  
reg [[3:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B3%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) current\_state, next\_state;  
reg done;  
  
localparam LOAD\_X\_WAIT = 4'd0,  
LOAD\_X = 4'd1,  
LOAD\_Y\_WAIT = 4'd2,  
LOAD\_Y\_COLOUR = 4'd3,  
DRAW = 4'd4;  
always @(\*)  
begin: state\_table   
case (current\_state)  
LOAD\_X\_WAIT: next\_state = load\_x ? LOAD\_X : LOAD\_X\_WAIT; // waiting for the load\_x to become high  
LOAD\_X: next\_state = load\_x ? LOAD\_X : LOAD\_Y\_WAIT; // load the x value into datapath until load\_x become low  
LOAD\_Y\_WAIT: next\_state = load\_y ? LOAD\_Y\_COLOUR : LOAD\_Y\_WAIT; // waiting for the load\_y to become high  
LOAD\_Y\_COLOUR: next\_state = load\_y ? LOAD\_Y\_COLOUR : DRAW; // load y and colour into datapath, start drawing when load\_y become low  
DRAW: next\_state = done ? LOAD\_X\_WAIT : DRAW; // we had told the datapath it can start drawing and we are now waiting for the new X input.  
default: next\_state = LOAD\_X\_WAIT;  
endcase  
end   
  
always @(\*)  
begin: enable\_signals  
ld\_x = 1'b0;  
ld\_y = 1'b0;  
ld\_colour = 1'b0;  
start\_draw = 1'b0;  
plot = 1'b0;  
  
case (current\_state)  
LOAD\_X: begin  
ld\_x = 1'b1;  
end  
LOAD\_Y\_COLOUR: begin  
ld\_y = 1'b1;  
ld\_colour = 1'b1;  
end  
DRAW: begin  
start\_draw = 1'b1;  
plot = 1'b1;  
end  
endcase  
end   
  
always@(posedge clock)  
begin  
if(!resetn) begin  
counter <= 4'b0001;  
done <= 1'b0;  
end  
else   
if (current\_state == DRAW) begin  
if (counter == 4'b1111)   
done <= 1'b1;  
counter <= counter + 1'b1;  
end   
else  
done <= 1'b0;  
end   
  
always@(posedge clock)  
begin: state\_FFs  
if(!resetn)  
current\_state <= LOAD\_X\_WAIT;  
else  
current\_state <= next\_state;  
end // state\_FFS  
endmodule  
  
module datapath(  
input ld\_x, ld\_y, ld\_colour,  
input start\_draw,  
input clock,  
input resetn,  
input [[9:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B9%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) data\_in,  
input [[3:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B3%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) counter,  
output reg [[2:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B2%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) colour,  
output reg [[7:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B7%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) x,  
output reg [[6:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B6%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) y  
);  
reg [[7:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B7%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank)x\_original;  
reg [[6:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B6%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank)y\_original;  
always @ (posedge clock) begin  
if (!resetn) begin  
x <= 8'b00000000;   
y <= 7'b0000000;   
colour <= 3'b000;  
x\_original <= 8'b00000000;  
y\_original <= 7'b0000000;  
end  
else begin  
if (ld\_x)begin  
x\_original <= {1'b0, data\_in[[6:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B6%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank)};  
x <= {1'b0, data\_in[[6:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B6%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank)};  
end  
if (ld\_y && ld\_colour) begin  
y <= data\_in[[6:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B6%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank);   
y\_original <= data\_in[[6:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B6%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank);   
colour <= data\_in[[9:7]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B9%3A7%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank);  
end  
if (start\_draw) begin  
x <= x\_original + counter[[1:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B1%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank);  
y <= y\_original + counter[[3:2]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B3%3A2%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank);  
end  
end  
end  
endmodule

1. FSM

module FSM(resetn, clock, load\_x, load\_y, ld\_x, ld\_y, ld\_colour, start\_draw, plot, counter);  
input resetn;  
input clock;  
input load\_x;  
input load\_y;  
output reg ld\_x, ld\_y, ld\_colour;  
output reg start\_draw;  
output reg plot;  
output reg [[3:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B3%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) counter = 4'b0001;  
  
reg [[3:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B3%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) current\_state, next\_state;  
reg done;  
  
localparam LOAD\_X\_WAIT = 4'd0,  
LOAD\_X = 4'd1,  
LOAD\_Y\_WAIT = 4'd2,  
LOAD\_Y\_COLOUR = 4'd3,  
DRAW = 4'd4;  
always @(\*)  
begin: state\_table   
case (current\_state)  
LOAD\_X\_WAIT: next\_state = load\_x ? LOAD\_X : LOAD\_X\_WAIT; // waiting for the load\_x to become high  
LOAD\_X: next\_state = load\_x ? LOAD\_X : LOAD\_Y\_WAIT; // load the x value into datapath until load\_x become low  
LOAD\_Y\_WAIT: next\_state = load\_y ? LOAD\_Y\_COLOUR : LOAD\_Y\_WAIT; // waiting for the load\_y to become high  
LOAD\_Y\_COLOUR: next\_state = load\_y ? LOAD\_Y\_COLOUR : DRAW; // load y and colour into datapath, start drawing when load\_y become low  
DRAW: next\_state = done ? LOAD\_X\_WAIT : DRAW; // we had told the datapath it can start drawing and we are now waiting for the new X input.  
default: next\_state = LOAD\_X\_WAIT;  
endcase  
end   
  
always @(\*)  
begin: enable\_signals  
ld\_x = 1'b0;  
ld\_y = 1'b0;  
ld\_colour = 1'b0;  
start\_draw = 1'b0;  
plot = 1'b0;  
  
case (current\_state)  
LOAD\_X: begin  
ld\_x = 1'b1;  
end  
LOAD\_Y\_COLOUR: begin  
ld\_y = 1'b1;  
ld\_colour = 1'b1;  
end  
DRAW: begin  
start\_draw = 1'b1;  
plot = 1'b1;  
end  
endcase  
end   
  
always@(posedge clock)  
begin  
if(!resetn) begin  
counter <= 4'b0001;  
done <= 1'b0;  
end  
else   
if (current\_state == DRAW) begin  
if (counter == 4'b1111)   
done <= 1'b1;  
counter <= counter + 1'b1;  
end   
else  
done <= 1'b0;  
end   
  
always@(posedge clock)  
begin: state\_FFs  
if(!resetn)  
current\_state <= LOAD\_X\_WAIT;  
else  
current\_state <= next\_state;  
end // state\_FFS  
endmodule

3.

module part2  
(  
CLOCK\_50, // On Board 50 MHz  
// Your inputs and outputs here  
KEY,  
SW,  
// The ports below are for the VGA output. Do not change.  
VGA\_CLK, // VGA Clock  
VGA\_HS, // VGA H\_SYNC  
VGA\_VS, // VGA V\_SYNC  
VGA\_BLANK\_N, // VGA BLANK  
VGA\_SYNC\_N, // VGA SYNC  
VGA\_R, // VGA Red[[9:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B9%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank)  
VGA\_G, // VGA Green[[9:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B9%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank)  
VGA\_B // VGA Blue[[9:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B9%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank)  
);  
  
input CLOCK\_50; // 50 MHz  
input [[9:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B9%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) SW;  
input [[3:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B3%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) KEY;  
  
// Declare your inputs and outputs here  
// Do not change the following outputs  
output VGA\_CLK; // VGA Clock  
output VGA\_HS; // VGA H\_SYNC  
output VGA\_VS; // VGA V\_SYNC  
output VGA\_BLANK\_N; // VGA BLANK  
output VGA\_SYNC\_N; // VGA SYNC  
output [[9:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B9%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) VGA\_R; // VGA Red[[9:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B9%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank)  
output [[9:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B9%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) VGA\_G; // VGA Green[[9:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B9%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank)  
output [[9:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B9%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) VGA\_B; // VGA Blue[[9:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B9%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank)  
  
wire resetn;  
assign resetn = KEY[0];  
wire load\_x;  
assign load\_x = ~KEY[3];  
wire load\_y;  
assign load\_y = ~KEY[1];  
wire ld\_x,ld\_y,ld\_colour,start\_draw;  
wire [[3:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B3%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) counter;  
// Create the colour, x, y and writeEn wires that are inputs to the controller.  
wire [[2:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B2%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) colour;  
wire [[7:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B7%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) x;  
wire [[6:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B6%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) y;  
wire writeEn;  
  
// Create an Instance of a VGA controller - there can be only one!  
// Define the number of colours as well as the initial background  
// image file (.MIF) for the controller.  
vga\_adapter VGA(  
.resetn(resetn),  
.clock(CLOCK\_50),  
.colour(colour),  
.x(x),  
.y(y),  
.plot(writeEn),  
/\* Signals for the DAC to drive the monitor. \*/  
.VGA\_R(VGA\_R),  
.VGA\_G(VGA\_G),  
.VGA\_B(VGA\_B),  
.VGA\_HS(VGA\_HS),  
.VGA\_VS(VGA\_VS),  
.VGA\_BLANK(VGA\_BLANK\_N),  
.VGA\_SYNC(VGA\_SYNC\_N),  
.VGA\_CLK(VGA\_CLK));  
defparam VGA.RESOLUTION = "160x120";  
defparam VGA.MONOCHROME = "FALSE";  
defparam VGA.BITS\_PER\_COLOUR\_CHANNEL = 1;  
defparam VGA.BACKGROUND\_IMAGE = "black.mif";  
  
// Put your code here. Your code should produce signals x,y,colour and writeEn/plot  
// for the VGA controller, in addition to any other functionality your design may require.  
  
// Instansiate datapath  
datapath d0(  
.ld\_x(ld\_x),  
.ld\_y(ld\_y),  
.ld\_colour(ld\_colour),  
.start\_draw(start\_draw),  
.resetn(resetn),  
.clock(CLOCK\_50),  
.data\_in(SW[[9:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B9%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank)),  
.counter(counter),  
.colour(colour),  
.x(x),  
.y(y)  
);  
  
// Instansiate FSM control  
control c0(  
.resetn(resetn),  
.clock(CLOCK\_50),  
.load\_x(load\_x),  
.load\_y(load\_y),  
.ld\_x(ld\_x),  
.ld\_y(ld\_y),  
.ld\_colour(ld\_colour),  
.start\_draw(start\_draw),  
.plot(writeEn),  
.counter(counter)  
);  
  
endmodule  
  
module control(  
input resetn,  
input clock,  
input load\_x,  
input load\_y,  
output reg ld\_x, ld\_y, ld\_colour,  
output reg start\_draw,  
output reg plot,  
output reg [[3:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B3%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) counter = 4'b0001  
);  
reg [[3:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B3%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) current\_state, next\_state;  
reg done;  
  
localparam LOAD\_X\_WAIT = 4'd0,  
LOAD\_X = 4'd1,  
LOAD\_Y\_WAIT = 4'd2,  
LOAD\_Y\_COLOUR = 4'd3,  
DRAW = 4'd4;  
always @(\*)  
begin: state\_table   
case (current\_state)  
LOAD\_X\_WAIT: next\_state = load\_x ? LOAD\_X : LOAD\_X\_WAIT; // waiting for the load\_x to become high  
LOAD\_X: next\_state = load\_x ? LOAD\_X : LOAD\_Y\_WAIT; // load the x value into datapath until load\_x become low  
LOAD\_Y\_WAIT: next\_state = load\_y ? LOAD\_Y\_COLOUR : LOAD\_Y\_WAIT; // waiting for the load\_y to become high  
LOAD\_Y\_COLOUR: next\_state = load\_y ? LOAD\_Y\_COLOUR : DRAW; // load y and colour into datapath, start drawing when load\_y become low  
DRAW: next\_state = done ? LOAD\_X\_WAIT : DRAW; // we had told the datapath it can start drawing and we are now waiting for the new X input.  
default: next\_state = LOAD\_X\_WAIT;  
endcase  
end   
  
always @(\*)  
begin: enable\_signals  
ld\_x = 1'b0;  
ld\_y = 1'b0;  
ld\_colour = 1'b0;  
start\_draw = 1'b0;  
plot = 1'b0;  
  
case (current\_state)  
LOAD\_X: begin  
ld\_x = 1'b1;  
end  
LOAD\_Y\_COLOUR: begin  
ld\_y = 1'b1;  
ld\_colour = 1'b1;  
end  
DRAW: begin  
start\_draw = 1'b1;  
plot = 1'b1;  
end  
endcase  
end   
  
always@(posedge clock)  
begin  
if(!resetn) begin  
counter <= 4'b0001;  
done <= 1'b0;  
end  
else   
if (current\_state == DRAW) begin  
if (counter == 4'b1111)   
done <= 1'b1;  
counter <= counter + 1'b1;  
end   
else  
done <= 1'b0;  
end   
  
always@(posedge clock)  
begin: state\_FFs  
if(!resetn)  
current\_state <= LOAD\_X\_WAIT;  
else  
current\_state <= next\_state;  
end // state\_FFS  
endmodule  
  
module datapath(  
input ld\_x, ld\_y, ld\_colour,  
input start\_draw,  
input clock,  
input resetn,  
input [[9:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B9%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) data\_in,  
input [[3:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B3%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) counter,  
output reg [[2:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B2%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) colour,  
output reg [[7:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B7%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) x,  
output reg [[6:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B6%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank) y  
);  
reg [[7:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B7%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank)x\_original;  
reg [[6:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B6%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank)y\_original;  
always @ (posedge clock) begin  
if (!resetn) begin  
x <= 8'b00000000;   
y <= 7'b0000000;   
colour <= 3'b000;  
x\_original <= 8'b00000000;  
y\_original <= 7'b0000000;  
end  
else begin  
if (ld\_x)begin  
x\_original <= {1'b0, data\_in[[6:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B6%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank)};  
x <= {1'b0, data\_in[[6:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B6%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank)};  
end  
if (ld\_y && ld\_colour) begin  
y <= data\_in[[6:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B6%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank);   
y\_original <= data\_in[[6:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B6%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank);   
colour <= data\_in[[9:7]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B9%3A7%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank);  
end  
if (start\_draw) begin  
x <= x\_original + counter[[1:0]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B1%3A0%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank);  
y <= y\_original + counter[[3:2]](https://l.facebook.com/l.php?u=http%3A%2F%2F%5B3%3A2%5D%2F&h=ATNbhm07K1-C6YgS8tqqg6LSgbgT3SqpF9Ceu601LAtbnJ369YN6hlRxHOv42ZxGbB-Nm1hS98_a6NG4iizf7oq5IWFjQWDXmrMqE4RwtsPsNmJ2O-iFll0rm6LrT4mv9S0b5ns7smHHsA" \t "_blank);  
end  
end  
end  
endmodule

