112 Autumn

EEIE30076

系統晶片設計 SOC Design

Lab. #3

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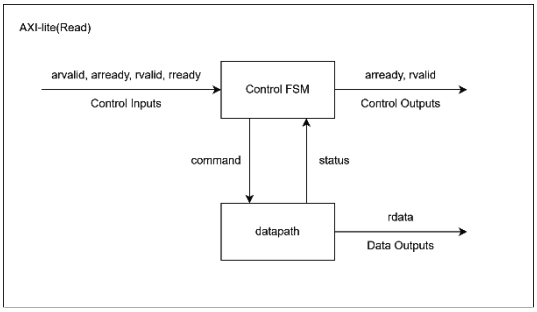
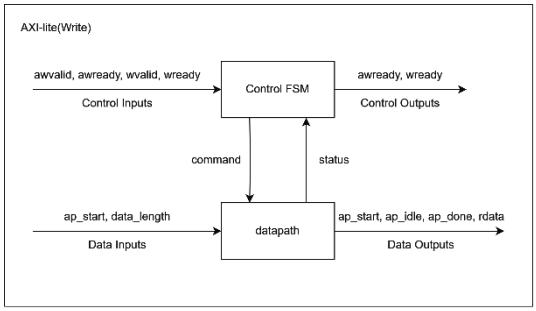
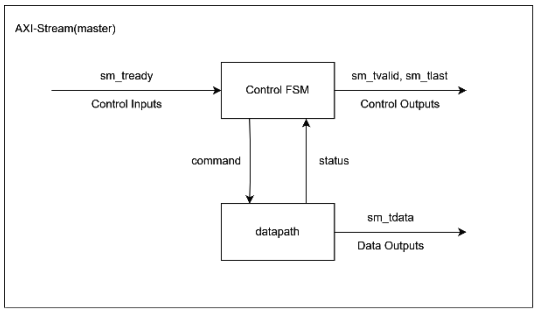
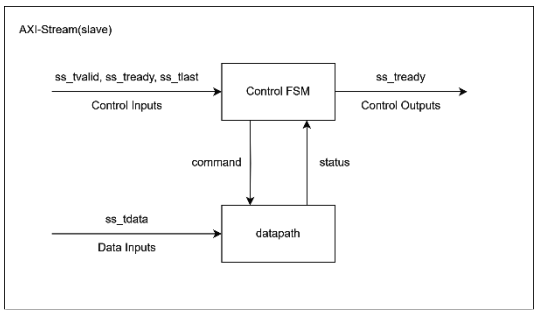
系級：機械所碩一

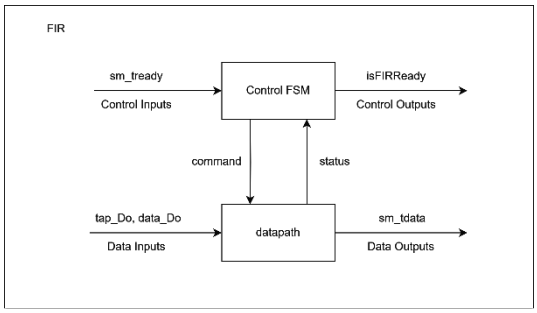
1. Block Diagram

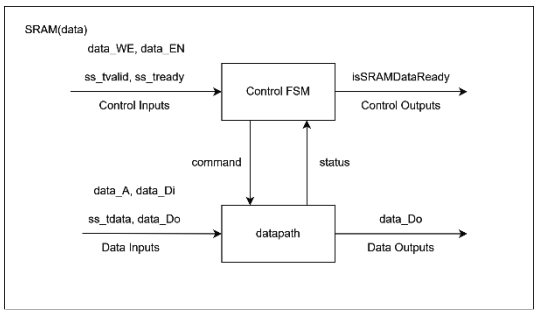


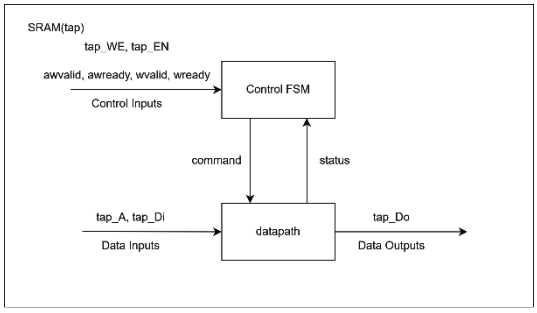








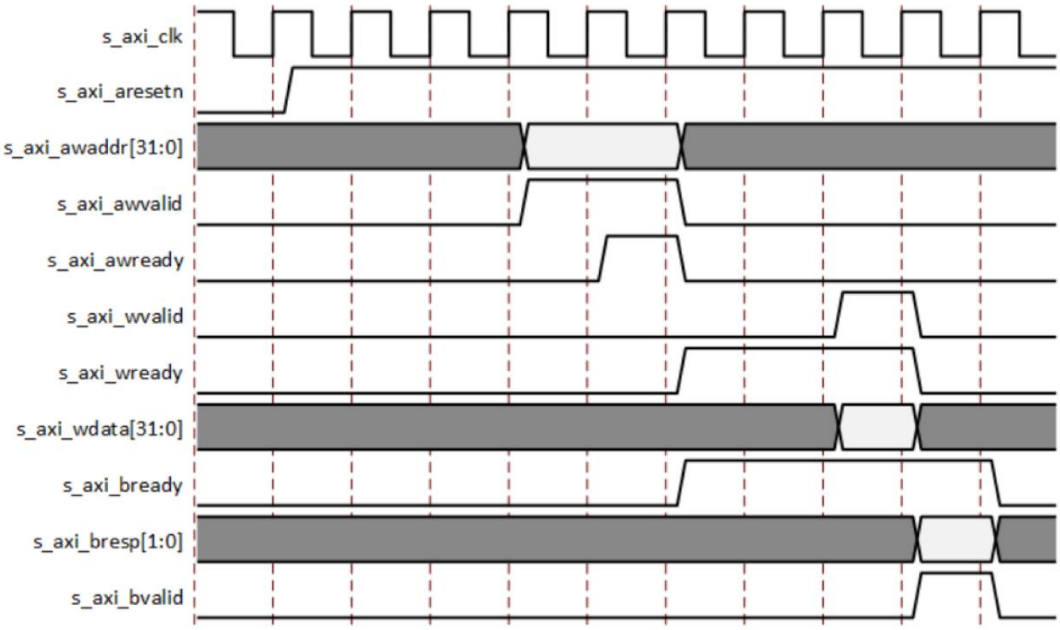




2. Describe operation

- How to receive data-in and tap parameters and place into SRAM

Data-in 是透過 AXI-Stream 從 testbench 傳至 source，當 tvalid 由 testbench 設定成 1 且 source 的 tready 設定為 1 時，source 開始接收資料。

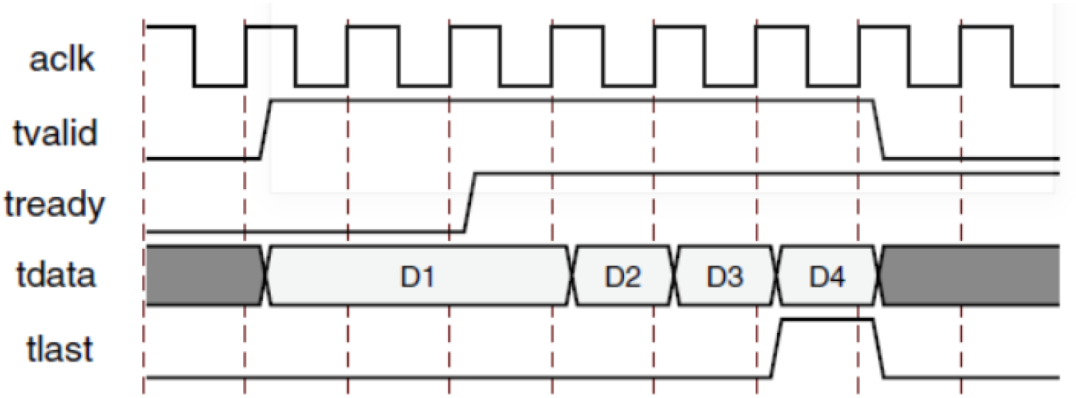


下列 n 為時序，n=2 為第 1 個 clk、n=3 為第 4 個 clk、n=4 為第 7 個 clk，以此類推

For n = 2:11
  1. read SRAM_data[n-1]
  2. wait for data
  3. write SRAM_data[n] = SRAM_data[n-1]
SRAM_data[0]=data_in

Tap parameters 是透過 AXI-lite(Write)從 testbench 傳至 source，當 awvalid 由 testbench 設定成 1 且 source 的 awready 設定成 1 時，awaddr 從 testbench 傳送的地址會被 source 收下。當 wvalid 由 testbench 設定成 1 且 source 的

wready 設定成 1 時，wdata 從 testbench 傳送的資料會被 source 收下。



For n = 1:11
1. Read awaddr
2. Read wdata
3. Write SRAM_tap[n]

- How to access shiftRAM and tapRAM to do computation

  SRAM 的獲取方式皆相同，EN=1, WE=0, ADDR=xxx，兩個上升緣之後，會取得 ADDR=xxx 的資料。

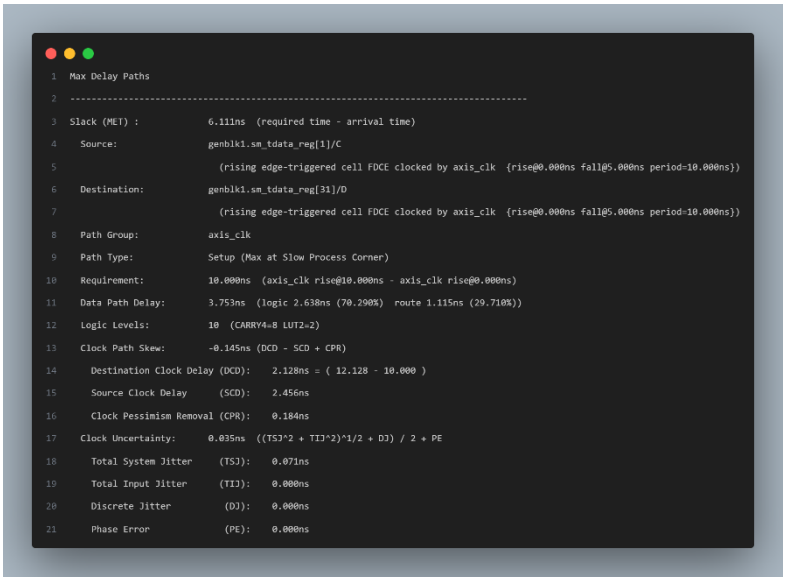
- How ap_done is generated
  when engine complete s last data processing

3. Resource usage: including FF, LUT, BRAM

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	210	0	0	53200	0.39
LUT as Logic	210	0	0	53200	0.39
LUT as Memory	0	0	0	17400	0.00
Slice Registers	190	0	0	106400	0.18
Register as Flip Flop	190	0	0	106400	0.18
Register as Latch	0	0	0	106400	0.00
F7 Muxes	0	0	0	26600	0.00
F8 Muxes	0	0	0	13300	0.00

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	0	0	140	0.00
RAMB36/FIFO*	0	0	0	140	0.00
RAMB18	0	0	0	280	0.00

4. Time Report
   - Report timing on longest path, slack



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Max Delay Paths
--------------------------------------------------------------------------------
Slack (MET) :             6.111ns  (required time - arrival time)
  Source:                 genblk1.sm_tdata_reg[1]/C
                            (rising edge-triggered cell FDCE clocked by axis_clk  {rise@0.000ns fall@5.000ns period=10.000ns})
  Destination:            genblk1.sm_tdata_reg[31]/D
                            (rising edge-triggered cell FDCE clocked by axis_clk  {rise@0.000ns fall@5.000ns period=10.000ns})
  Path Group:             axis_clk
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            10.000ns  (axis_clk rise@10.000ns - axis_clk rise@0.000ns)
  Data Path Delay:        3.753ns  (logic 2.638ns (70.290%)  route 1.115ns (29.710%))
  Logic Levels:           10  (CARRY4=8 LUT2=2)
  Clock Path Skew:        -0.145ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    2.128ns = ( 12.128 - 10.000 )
    Source Clock Delay      (SCD):    2.456ns
    Clock Pessimism Removal (CPR):    0.184ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter          (DJ):    0.000ns
    Phase Error              (PE):    0.000ns
```

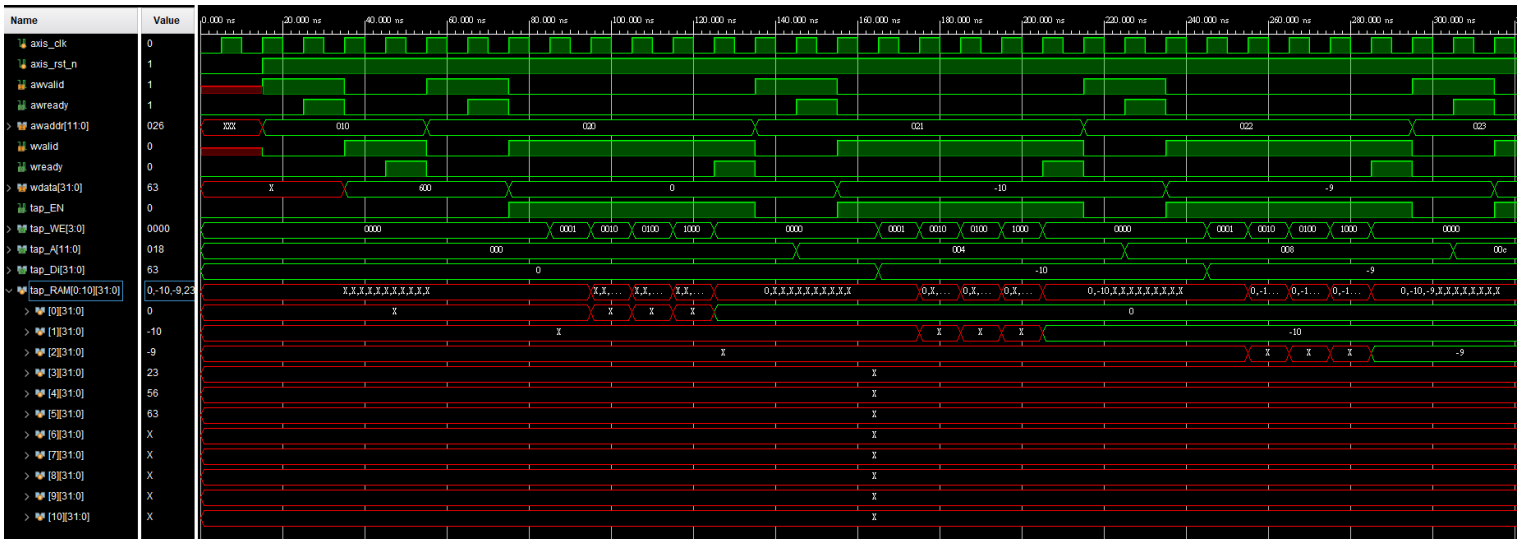
   - Try to synthesize the design with maximum frequency

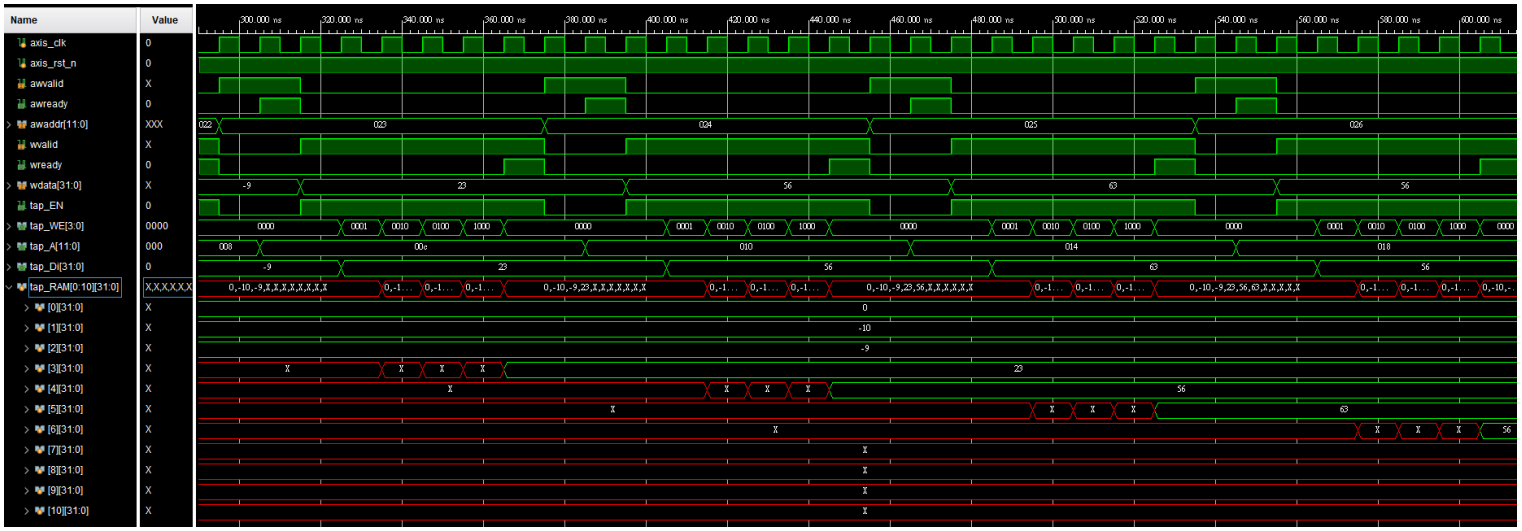
     Slack = required time – arrival time

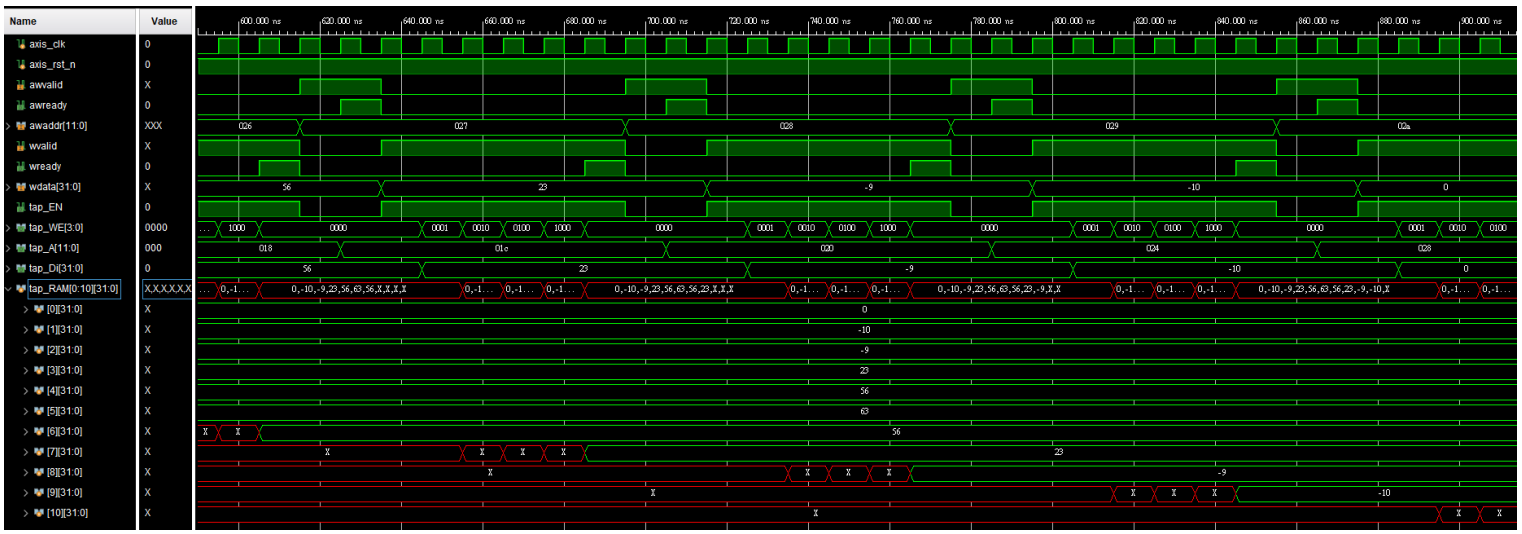
     Slack = 6.111 [ns], clock = 10 [ns]

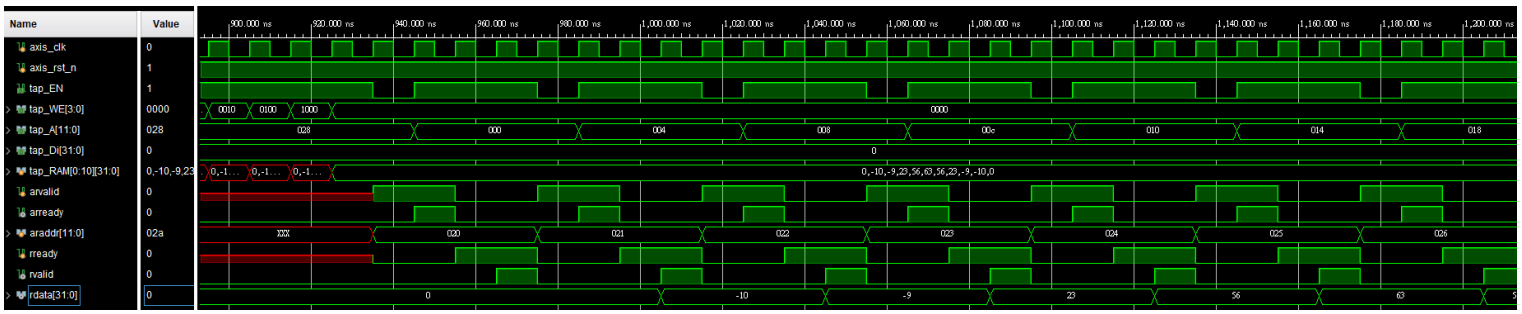
     Maximum frequency = $\frac{1}{10-6.111[ns]} = 257.14MHz$

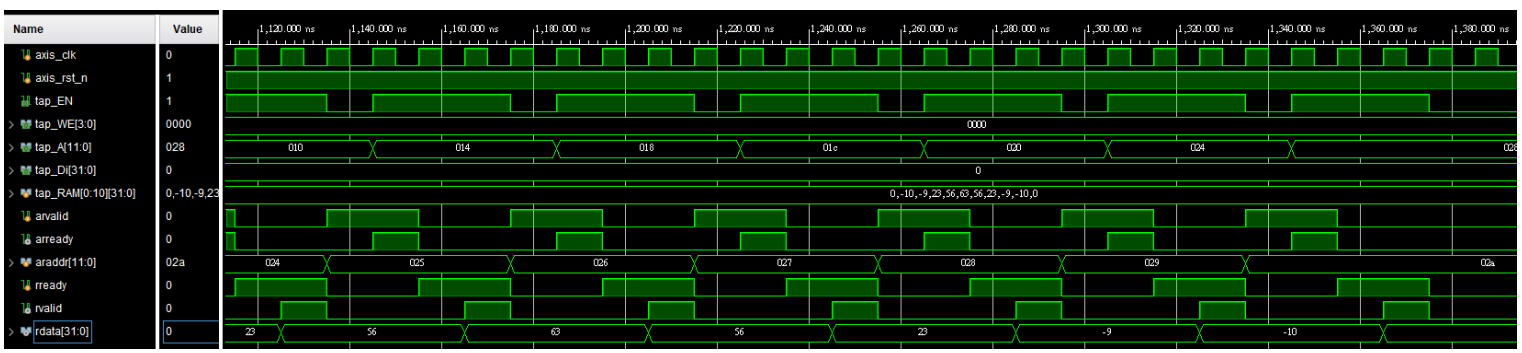
5. Simulaton Waveform
   - Coefficient program, and read back



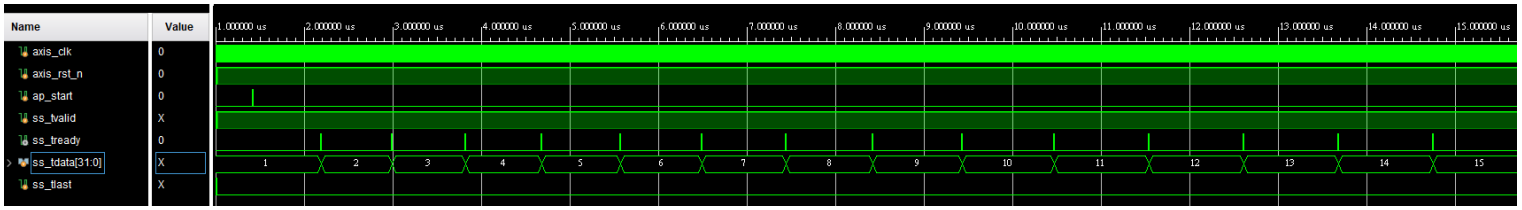

Name
Value
axis_clk
axis_rst_n
awvalid
awready
awaddr[11:0]
wvalid
wready
wdata[31:0]
tap_EN
tap_WE[3:0]
tap_A[11:0]
tap_Di[31:0]
tap_RAM[0:10][31:0]
[0][31:0]
[1][31:0]
[2][31:0]
[3][31:0]
[4][31:0]
[5][31:0]
[6][31:0]
[7][31:0]
[8][31:0]
[9][31:0]
[10][31:0]

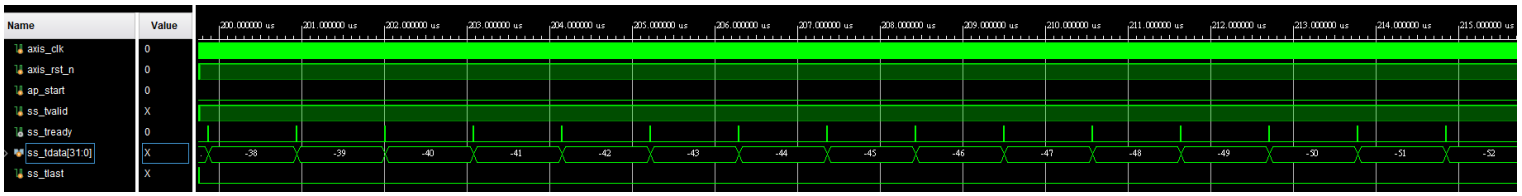

Name
Value
axis_clk
axis_rst_n
awvalid
awready
awaddr[11:0]
wvalid
wready
wdata[31:0]
tap_EN
tap_WE[3:0]
tap_A[11:0]
tap_Di[31:0]
tap_RAM[0:10][31:0]
[0][31:0]
[1][31:0]
[2][31:0]
[3][31:0]
[4][31:0]
[5][31:0]
[6][31:0]
[7][31:0]
[8][31:0]
[9][31:0]
[10][31:0]

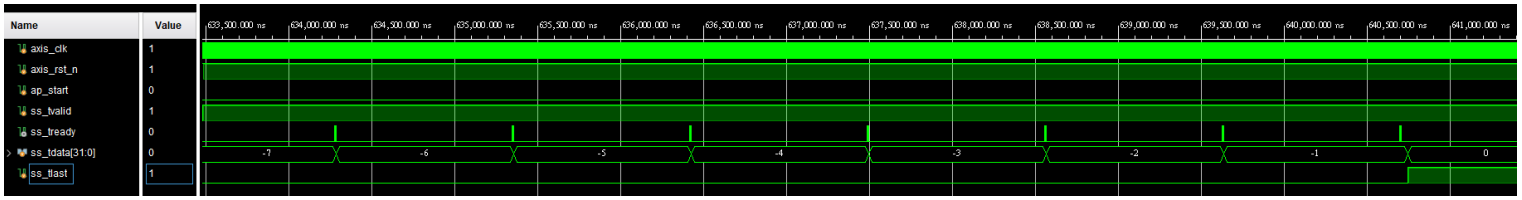

Name
Value
axis_clk
axis_rst_n
tap_EN
tap_WE[3:0]
tap_A[11:0]
tap_Di[31:0]
tap_RAM[0:10][31:0]
arvalid
arready
araddr[11:0]
rready
rvalid
rdata[31:0]


Name
Value
axis_clk
axis_rst_n
tap_EN
tap_WE[3:0]
tap_A[11:0]
tap_Di[31:0]
tap_RAM[0:10][31:0]
arvalid
arready
araddr[11:0]
rready
rvalid
rdata[31:0]

- Data-in stream-in

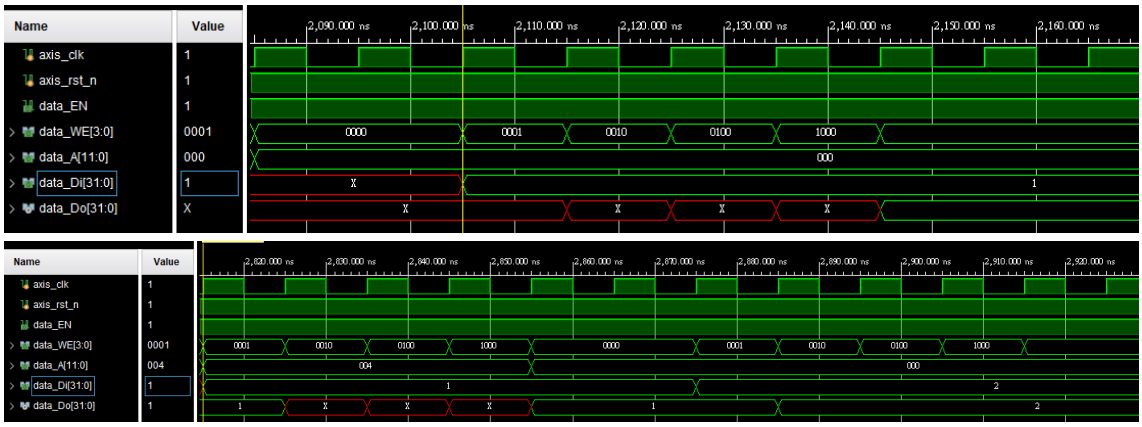




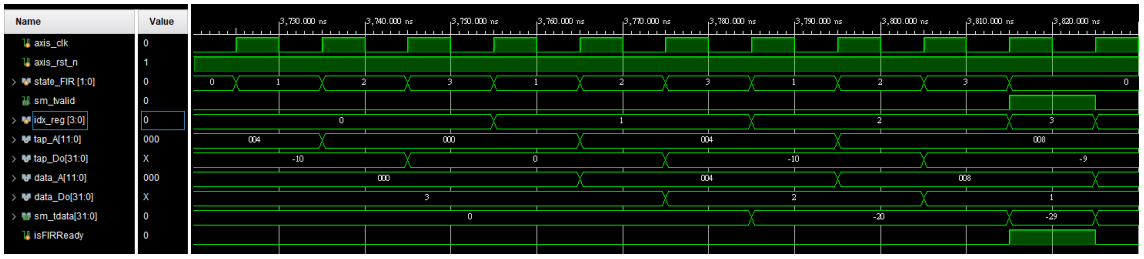


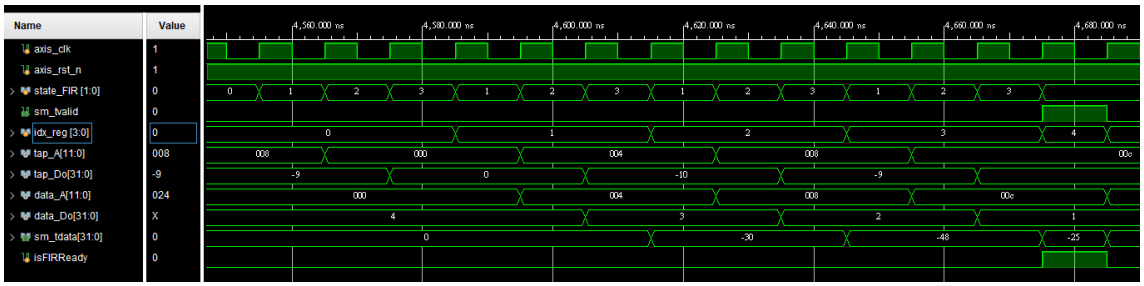
- Data-out stream-out

- RAM access control



- FSM


Name
Value
axis_clk
axis_rst_n
state_FIR [1:0]
sm_tvalid
idx_reg [3:0]
tap_A[11:0]
tap_Do[31:0]
data_A[11:0]
data_Do[31:0]
sm_tdata[31:0]
isFIRReady


Name
Value
axis_clk
axis_rst_n
state_FIR [1:0]
sm_tvalid
idx_reg [3:0]
tap_A[11:0]
tap_Do[31:0]
data_A[11:0]
data_Do[31:0]
sm_tdata[31:0]
isFIRReady