SOC LAB 4-1

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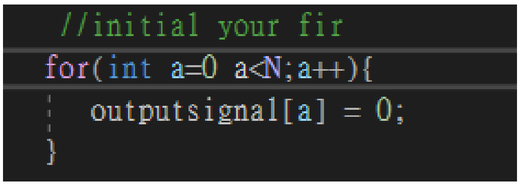
1. Explanation of your firmware code

- **How does it execute a multiplication in assembly code**

  在 FIR.C 檔案中分兩個部分:

1. Initial fir

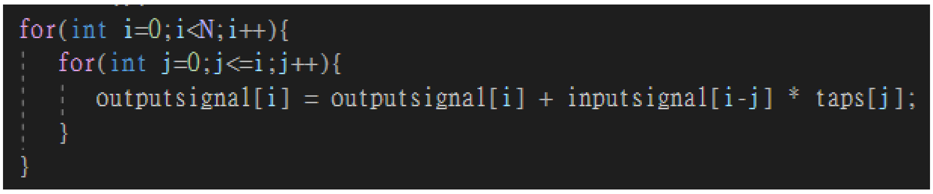
   Outputsignal 預先歸 0



```
//initial your fir
for(int a=0 a<N;a++){
    outputsignal[a] = 0;
}
```

2. Main fir.c

   累加 inputsignal 和 taps 的乘積，計算 outputsignal 的值

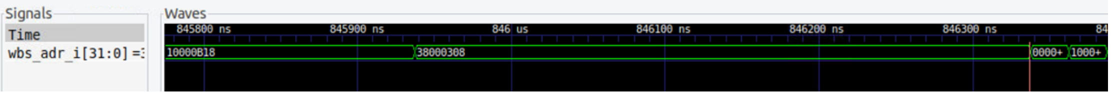


```
for(int i=0;i<N;i++){
    for(int j=0;j<=i;j++){
        outputsignal[i] = outputsignal[i] + inputsignal[i-j] * taps[j];
    }
}
```

- **What address allocate for user project and how many space is required to allocate to firmware code**

From 0x3800_0000 to 0x3800_0308 (actually is 0x3800_030A)

780*8bits = 780 Bytes

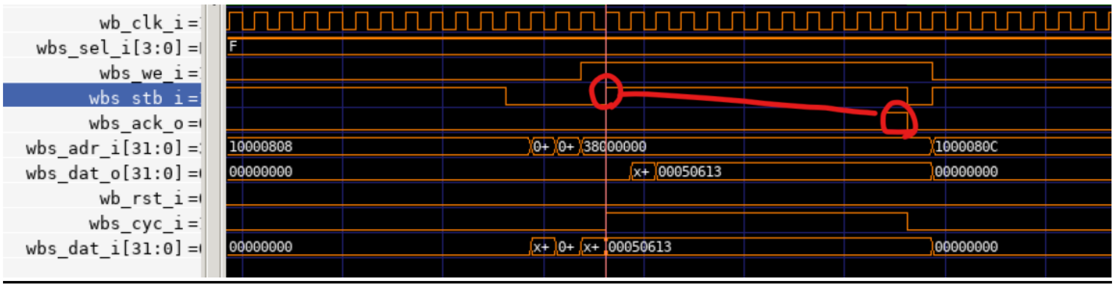


2. Interface between BRAM and wishbone

➢ Waveform from xsim

1. Wishbond:

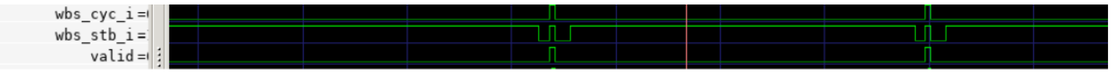
Cyc_i & ack_o 差 10cycle

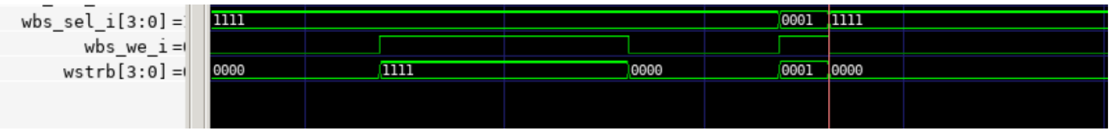


Input:

Valid = wbs_cyc_i && wbs_stb_i;

wstrb= wbs_sel_i & {4{wbs_we_i}};

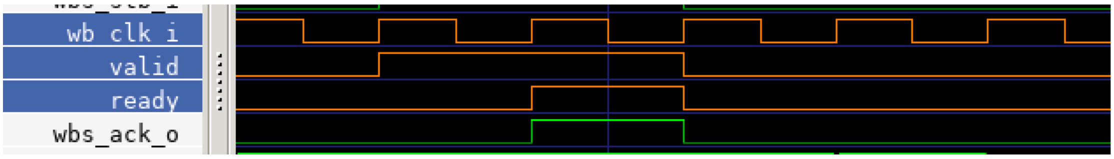




Output:

wbs_dat_o = ready ;

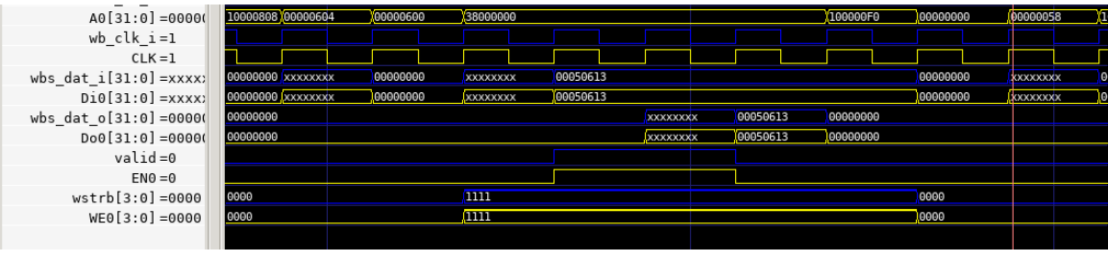
if(vaild && !ready) => ready 下一個 clk 輸入 1



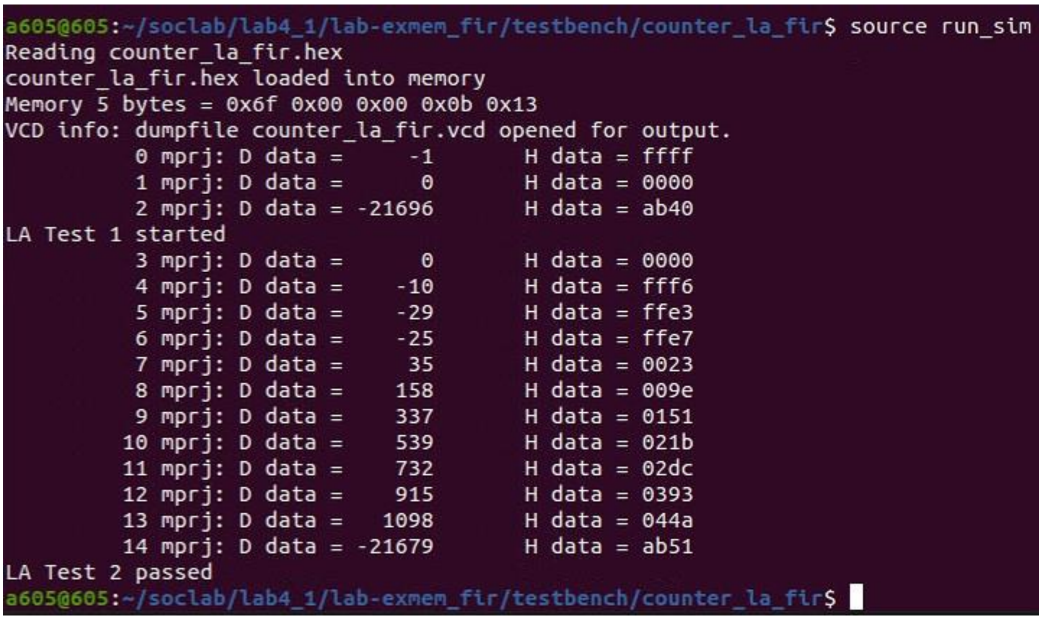
2. Bram:

藍色: 表示 wishbond input signal

黃色: 表示 Bram get signal

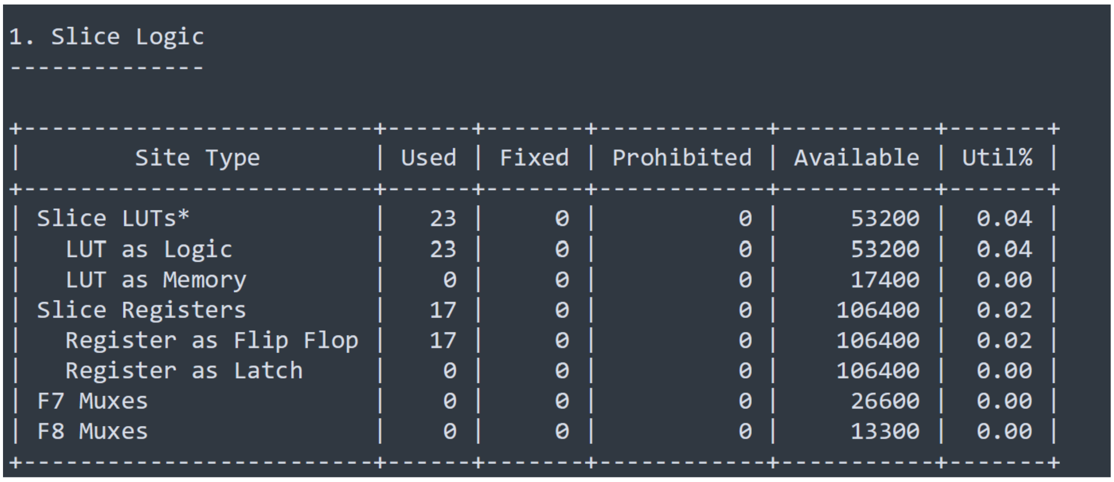


3. Simulation result

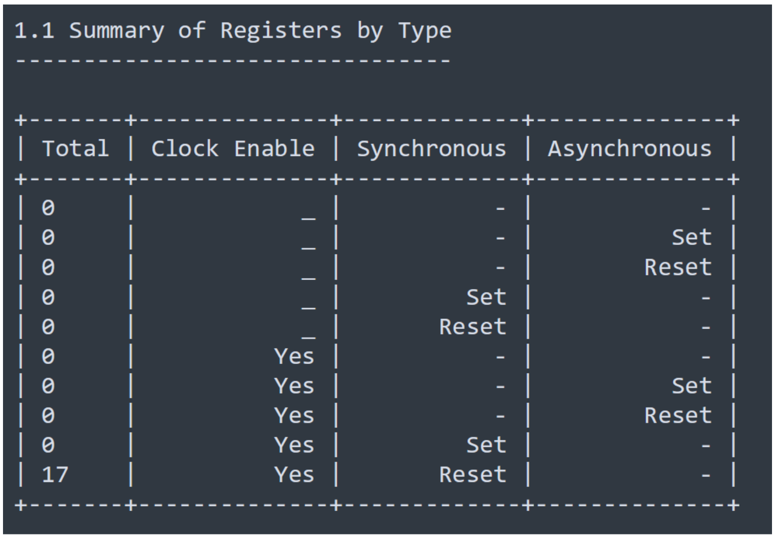


```
a605@605:~/soclab/lab4_1/lab-exmem_fir/testbench/counter_la_fir$ source run_sim
Reading counter_la_fir.hex
counter_la_fir.hex loaded into memory
Memory 5 bytes = 0x6f 0x00 0x00 0x0b 0x13
VCD info: dumpfile counter_la_fir.vcd opened for output.
          0 mprj: D data =     -1       H data = ffff
          1 mprj: D data =      0       H data = 0000
          2 mprj: D data = -21696       H data = ab40
LA Test 1 started
          3 mprj: D data =      0       H data = 0000
          4 mprj: D data =    -10       H data = fff6
          5 mprj: D data =    -29       H data = ffe3
          6 mprj: D data =    -25       H data = ffe7
          7 mprj: D data =     35       H data = 0023
          8 mprj: D data =    158       H data = 009e
          9 mprj: D data =    337       H data = 0151
         10 mprj: D data =    539       H data = 021b
         11 mprj: D data =    732       H data = 02dc
         12 mprj: D data =    915       H data = 0393
         13 mprj: D data =   1098       H data = 044a
         14 mprj: D data = -21679       H data = ab51
LA Test 2 passed
a605@605:~/soclab/lab4_1/lab-exmem_fir/testbench/counter_la_fir$
```

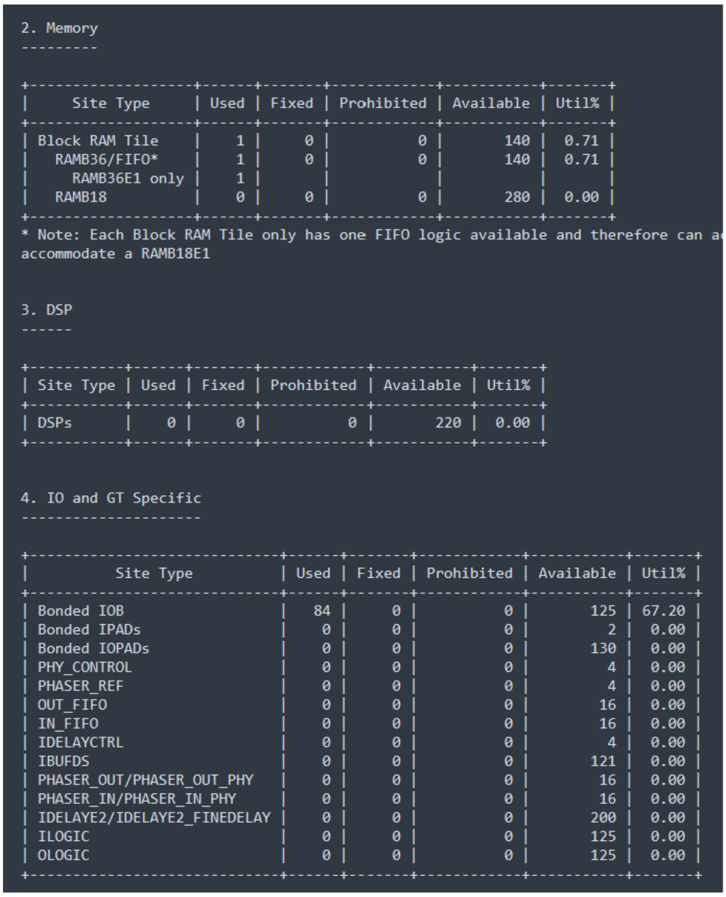
4. Synthesis report



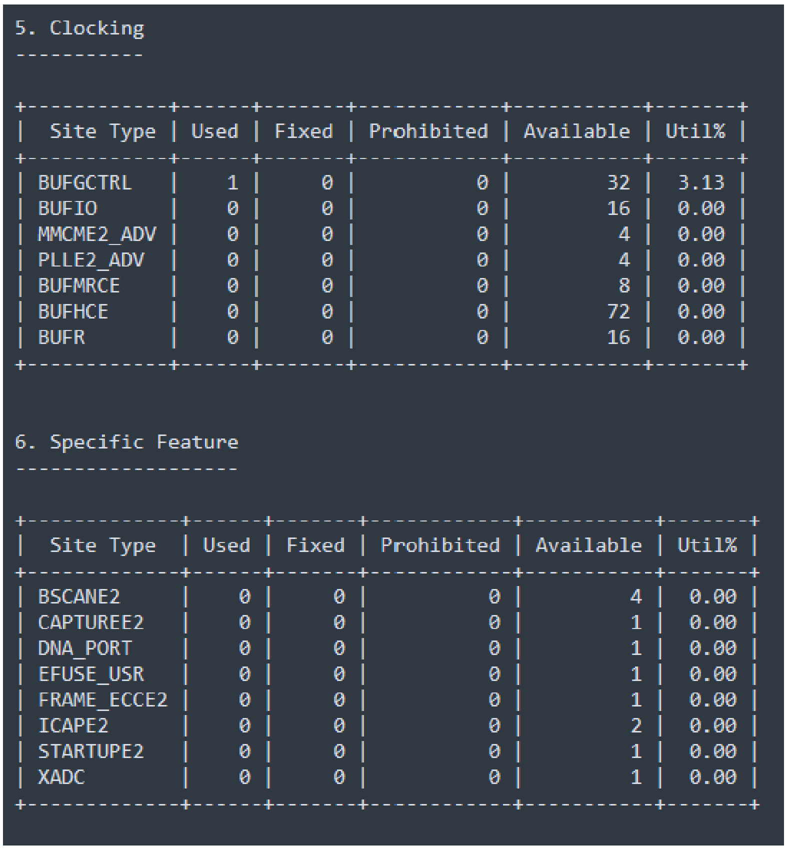
```
1. Slice Logic
--------------

+-------------------------+------+-------+------------+-----------+-------+
|        Site Type        | Used | Fixed | Prohibited | Available | Util% |
+-------------------------+------+-------+------------+-----------+-------+
| Slice LUTs*             |   23 |     0 |          0 |     53200 |  0.04 |
|   LUT as Logic          |   23 |     0 |          0 |     53200 |  0.04 |
|   LUT as Memory         |    0 |     0 |          0 |     17400 |  0.00 |
| Slice Registers         |   17 |     0 |          0 |    106400 |  0.02 |
|   Register as Flip Flop |   17 |     0 |          0 |    106400 |  0.02 |
|   Register as Latch     |    0 |     0 |          0 |    106400 |  0.00 |
| F7 Muxes                |    0 |     0 |          0 |     26600 |  0.00 |
| F8 Muxes                |    0 |     0 |          0 |     13300 |  0.00 |
+-------------------------+------+-------+------------+-----------+-------+
```



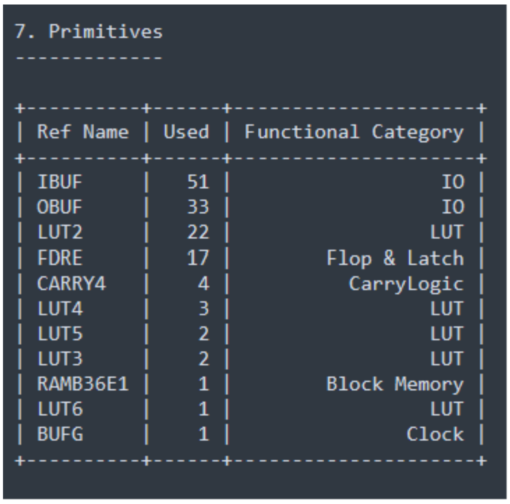
```
1.1 Summary of Registers by Type
--------------------------------

+-------+--------------+-------------+--------------+
| Total | Clock Enable | Synchronous | Asynchronous |
+-------+--------------+-------------+--------------+
| 0     |            _ |           - |            - |
| 0     |            _ |           - |          Set |
| 0     |            _ |           - |        Reset |
| 0     |            _ |         Set |            - |
| 0     |            _ |       Reset |            - |
| 0     |          Yes |           - |            - |
| 0     |          Yes |           - |          Set |
| 0     |          Yes |           - |        Reset |
| 0     |          Yes |         Set |            - |
| 17    |          Yes |       Reset |            - |
+-------+--------------+-------------+--------------+
```



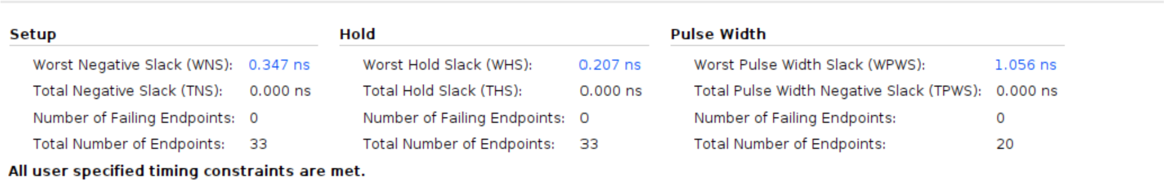
```
2. Memory
---------

+-------------------+------+-------+------------+-----------+-------+
|     Site Type     | Used | Fixed | Prohibited | Available | Util% |
+-------------------+------+-------+------------+-----------+-------+
| Block RAM Tile    |    1 |     0 |          0 |       140 |  0.71 |
|   RAMB36/FIFO*    |    1 |     0 |          0 |       140 |  0.71 |
|     RAMB36E1 only |    1 |       |            |           |       |
|   RAMB18          |    0 |     0 |          0 |       280 |  0.00 |
+-------------------+------+-------+------------+-----------+-------+
* Note: Each Block RAM Tile only has one FIFO logic available and therefore can a
accommodate a RAMB18E1


3. DSP
------

+-----------+------+-------+------------+-----------+-------+
| Site Type | Used | Fixed | Prohibited | Available | Util% |
+-----------+------+-------+------------+-----------+-------+
| DSPs      |    0 |     0 |          0 |       220 |  0.00 |
+-----------+------+-------+------------+-----------+-------+


4. IO and GT Specific
--------------------

+-----------------------------+------+-------+------------+-----------+-------+
|          Site Type          | Used | Fixed | Prohibited | Available | Util% |
+-----------------------------+------+-------+------------+-----------+-------+
| Bonded IOB                  |   84 |     0 |          0 |       125 | 67.20 |
| Bonded IPADs                |    0 |     0 |          0 |         2 |  0.00 |
| Bonded IOPADs               |    0 |     0 |          0 |       130 |  0.00 |
| PHY_CONTROL                 |    0 |     0 |          0 |         4 |  0.00 |
| PHASER_REF                  |    0 |     0 |          0 |         4 |  0.00 |
| OUT_FIFO                    |    0 |     0 |          0 |        16 |  0.00 |
| IN_FIFO                     |    0 |     0 |          0 |        16 |  0.00 |
| IDELAYCTRL                  |    0 |     0 |          0 |         4 |  0.00 |
| IBUFDS                      |    0 |     0 |          0 |       121 |  0.00 |
| PHASER_OUT/PHASER_OUT_PHY   |    0 |     0 |          0 |        16 |  0.00 |
| PHASER_IN/PHASER_IN_PHY     |    0 |     0 |          0 |        16 |  0.00 |
| IDELAYE2/IDELAYE2_FINEDELAY |    0 |     0 |          0 |       200 |  0.00 |
| ILOGIC                      |    0 |     0 |          0 |       125 |  0.00 |
| OLOGIC                      |    0 |     0 |          0 |       125 |  0.00 |
+-----------------------------+------+-------+------------+-----------+-------+
```



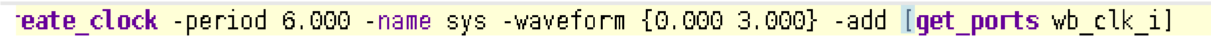
```
5. Clocking
-----------

+------------+------+-------+------------+-----------+-------+
|  Site Type | Used | Fixed | Prohibited | Available | Util% |
+------------+------+-------+------------+-----------+-------+
| BUFGCTRL   |    1 |     0 |          0 |        32 |  3.13 |
| BUFIO      |    0 |     0 |          0 |        16 |  0.00 |
| MMCME2_ADV |    0 |     0 |          0 |         4 |  0.00 |
| PLLE2_ADV  |    0 |     0 |          0 |         4 |  0.00 |
| BUFMRCE    |    0 |     0 |          0 |         8 |  0.00 |
| BUFHCE     |    0 |     0 |          0 |        72 |  0.00 |
| BUFR       |    0 |     0 |          0 |        16 |  0.00 |
+------------+------+-------+------------+-----------+-------+


6. Specific Feature
-------------------

+-------------+------+-------+------------+-----------+-------+
|  Site Type  | Used | Fixed | Prohibited | Available | Util% |
+-------------+------+-------+------------+-----------+-------+
| BSCANE2     |    0 |     0 |          0 |         4 |  0.00 |
| CAPTUREE2   |    0 |     0 |          0 |         1 |  0.00 |
| DNA_PORT    |    0 |     0 |          0 |         1 |  0.00 |
| EFUSE_USR   |    0 |     0 |          0 |         1 |  0.00 |
| FRAME_ECCE2 |    0 |     0 |          0 |         1 |  0.00 |
| ICAPE2      |    0 |     0 |          0 |         2 |  0.00 |
| STARTUPE2   |    0 |     0 |          0 |         1 |  0.00 |
| XADC        |    0 |     0 |          0 |         1 |  0.00 |
+-------------+------+-------+------------+-----------+-------+
```



```
7. Primitives
-------------

+----------+------+---------------------+
| Ref Name | Used | Functional Category |
+----------+------+---------------------+
| IBUF     |   51 |                  IO |
| OBUF     |   33 |                  IO |
| LUT2     |   22 |                 LUT |
| FDRE     |   17 |        Flop & Latch |
| CARRY4   |    4 |          CarryLogic |
| LUT4     |    3 |                 LUT |
| LUT5     |    2 |                 LUT |
| LUT3     |    2 |                 LUT |
| RAMB36E1 |    1 |        Block Memory |
| LUT6     |    1 |                 LUT |
| BUFG     |    1 |               Clock |
+----------+------+---------------------+
```



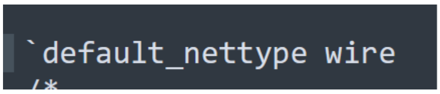
```
Setup                                      Hold                                       Pulse Width
   Worst Negative Slack (WNS):   0.347 ns     Worst Hold Slack (WHS):       0.207 ns     Worst Pulse Width Slack (WPWS):             1.056 ns
   Total Negative Slack (TNS):   0.000 ns     Total Hold Slack (THS):       0.000 ns     Total Pulse Width Negative Slack (TPWS):    0.000 ns
   Number of Failing Endpoints:  0            Number of Failing Endpoints:  0            Number of Failing Endpoints:                0
   Total Number of Endpoints:    33           Total Number of Endpoints:    33           Total Number of Endpoints:                  20
All user specified timing constraints are met.
```



```
eate_clock -period 6.000 -name sys -waveform {0.000 3.000} -add [get_ports wb_clk_i]
```

5. Other discoveries

在做 syn 時因為只有針對 counter.v & bram.v syn 因此 default_nettype 需要改成 wire (原本定義在 define 的檔案)



```
`default_nettype wire
/*
```

valid 功能：

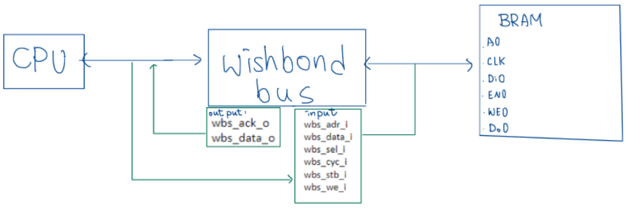
slave only " strab 88 cycle " = = 1 → logic output

slave would drive "read-data"

wstrb 功能:

decoder 概念

wbs-sel-i 8 wbs-we-i ⇒ output 4 bit for BRAM Decoder


CPU
wishbond bus
BRAM
AO
CLK
DiO
ENO
WEO
DoO
out put :
wbs_ack_o
wbs_data_o
input
wbs_adr_i
wbs_data_i
wbs_sel_i
wbs_cyc_i
wbs_stb_i
wbs_we_i