Digital System Design and Implementation

Homework #2

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a. Verilog codes

```verilog
`timescale 1ns / 1ps
module main(SerialIn, CLK, Reset, Test, SO);
input SerialIn, CLK, Reset, Test;
output [4:0]SO;

wire [4:0]mux_out;
wire [2:0]gate_xor_out;
wire [3:0]gate_not_out;

// Instance
MUX2x1
mux2x1_1(.In0(SO[0]),.In1(SerialIn),.Out(mux_out[4]),.sel(Test));
FlipFlop
FP_1(.CLK(CLK), .data(mux_out[4]), .Reset(Reset), .Q(SO[4]));

xor(gate_xor_out[2],SO[4],SO[0]);
not(gate_not_out[3],SO[4]);
MUX2x1
mux2x1_2(.In0(gate_xor_out[2]),.In1(gate_not_out[3]),.Out(mux_out[3])
,.sel(Test));
FlipFlop
FP_2(.CLK(CLK), .data(mux_out[3]), .Reset(Reset), .Q(SO[3]));

not(gate_not_out[2],SO[3]);
MUX2x1
mux2x1_3(.In0(SO[3]),.In1(gate_not_out[2]),.Out(mux_out[2]),.sel(Test)
);
```

```verilog
FlipFlop
FP_3(.CLK(CLK), .data(mux_out[2]), .Reset(Reset), .Q(SO[2]));

xor(gate_xor_out[1],SO[2],SO[0]);
not(gate_not_out[1],SO[2]);
MUX2x1
mux2x1_4(.In0(gate_xor_out[1]),.In1(gate_not_out[1]),.Out(mux_out[1])
,.sel(Test));
FlipFlop
FP_4(.CLK(CLK), .data(mux_out[1]), .Reset(Reset), .Q(SO[1]));

xor(gate_xor_out[0],SO[1],SO[0]);
not(gate_not_out[0],SO[1]);
MUX2x1
mux2x1_5(.In0(gate_xor_out[0]),.In1(gate_not_out[0]),.Out(mux_out[0])
,.sel(Test));
FlipFlop
FP_5(.CLK(CLK), .data(mux_out[0]), .Reset(Reset), .Q(SO[0]));
endmodule

module FlipFlop(CLK, data, Reset, Q);
input CLK, data, Reset;
output Q;
reg Q;
always @(posedge CLK or posedge Reset)
    if(Reset)
        Q<=1'b0;
    else
        Q<=data;
endmodule

module MUX2x1(In0,In1,Out,sel);
input In0,In1,sel;
output Out;
reg tmp;
always @(In0,In1,sel)
begin
    case(sel)
```

```verilog
        1'b0:
            tmp=In0;
        1'b1:
            tmp=In1;
    endcase
end
assign Out=tmp;
endmodule
```

b. Test bench

```verilog
`timescale 1ns / 1ps


module main_tb;
reg [7:0]ID=13;
reg SerialIn, CLK, Reset, Test;
wire [4:0]SO;

// Instance
main
m(.SerialIn(SerialIn), .CLK(CLK), .Reset(Reset), .Test(Test), .SO(SO));
initial
begin
    Test=0; Reset=0; CLK=1; SerialIn=0; #100;
    #05; Reset=1; #10;
    Reset=0; Test=1; SerialIn=ID[0]; #10;
    Test=1; SerialIn=ID[1]; #10;
    SerialIn=ID[2]; #10;
    SerialIn=ID[3]; #10;
    SerialIn=ID[4]; #10;
    SerialIn=1; #10;
    SerialIn=0; #10;
    SerialIn=ID[5]; #10;
    Test=0; SerialIn=ID[6]; #10;
    #(350-15);
    $finish;
end
```
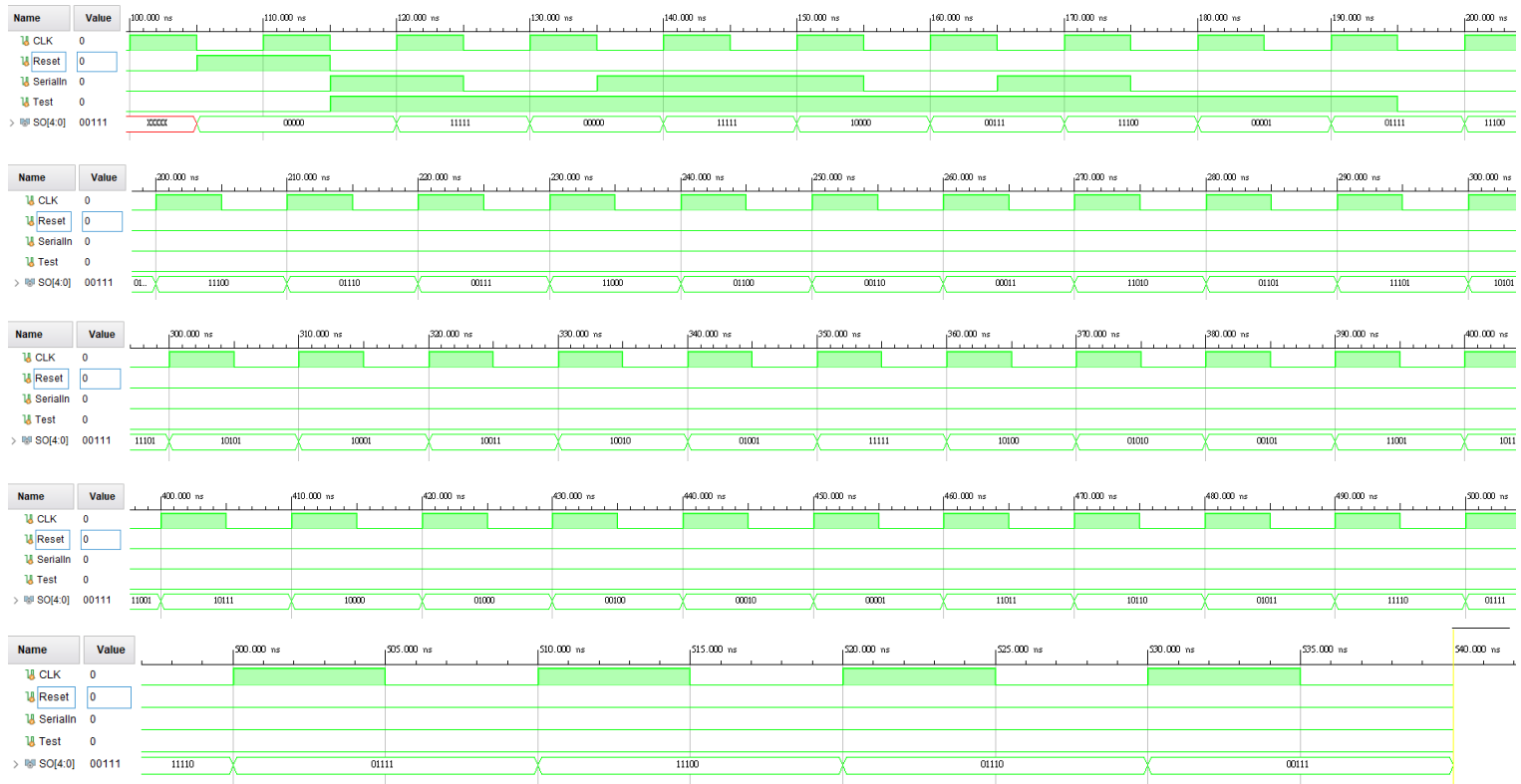
```verilog
always begin
    #5; CLK=~CLK;
end

initial
    $monitor("SO = %2d, SerialIn = %2d, Test = %d, CLK = %d, Reset
= %d, Time = %4d",SO,SerialIn,Test,CLK,Reset,$time);
endmodule;
```

c. Behavior simulation (text output and waveforms)
   Waveforms

text output

SO = x, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   0
SO = x, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   5
SO = x, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   10
SO = x, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   15
SO = x, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   20
SO = x, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   25

SO = x, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   30
SO = x, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   35
SO = x, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   40
SO = x, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   45
SO = x, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   50
SO = x, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   55
SO = x, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   60
SO = x, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   65
SO = x, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   70
SO = x, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   75
SO = x, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   80
SO = x, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   85
SO = x, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   90
SO = x, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   95
SO = x, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   100
SO =   0, SerialIn =   0, Test = 0, CLK = 0, Reset = 1, Time =   105
SO =   0, SerialIn =   0, Test = 0, CLK = 1, Reset = 1, Time =   110
SO =   0, SerialIn =   1, Test = 1, CLK = 0, Reset = 0, Time =   115
SO = 31, SerialIn =   1, Test = 1, CLK = 1, Reset = 0, Time =   120
SO = 31, SerialIn =   0, Test = 1, CLK = 0, Reset = 0, Time =   125
SO =   0, SerialIn =   0, Test = 1, CLK = 1, Reset = 0, Time =   130
SO =   0, SerialIn =   1, Test = 1, CLK = 0, Reset = 0, Time =   135
SO = 31, SerialIn =   1, Test = 1, CLK = 1, Reset = 0, Time =   140
SO = 31, SerialIn =   1, Test = 1, CLK = 0, Reset = 0, Time =   145
SO = 16, SerialIn =   1, Test = 1, CLK = 1, Reset = 0, Time =   150
SO = 16, SerialIn =   0, Test = 1, CLK = 0, Reset = 0, Time =   155
SO =   7, SerialIn =   0, Test = 1, CLK = 1, Reset = 0, Time =   160
SO =   7, SerialIn =   1, Test = 1, CLK = 0, Reset = 0, Time =   165
SO = 28, SerialIn =   1, Test = 1, CLK = 1, Reset = 0, Time =   170
SO = 28, SerialIn =   0, Test = 1, CLK = 0, Reset = 0, Time =   175
SO =   1, SerialIn =   0, Test = 1, CLK = 1, Reset = 0, Time =   180
SO =   1, SerialIn =   0, Test = 1, CLK = 0, Reset = 0, Time =   185
SO = 15, SerialIn =   0, Test = 1, CLK = 1, Reset = 0, Time =   190
SO = 15, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   195
SO = 28, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   200
SO = 28, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   205
SO = 14, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   210
SO = 14, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   215

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SO =   7, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   220
SO =   7, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   225
SO = 24, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   230
SO = 24, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   235
SO = 12, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   240
SO = 12, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   245
SO =   6, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   250
SO =   6, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   255
SO =   3, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   260
SO =   3, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   265
SO = 26, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   270
SO = 26, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   275
SO = 13, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   280
SO = 13, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   285
SO = 29, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   290
SO = 29, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   295
SO = 21, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   300
SO = 21, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   305
SO = 17, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   310
SO = 17, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   315
SO = 19, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   320
SO = 19, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   325
SO = 18, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   330
SO = 18, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   335
SO =   9, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   340
SO =   9, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   345
SO = 31, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   350
SO = 31, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   355
SO = 20, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   360
SO = 20, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   365
SO = 10, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   370
SO = 10, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   375
SO =   5, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   380
SO =   5, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   385
SO = 25, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   390
SO = 25, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   395
SO = 23, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   400
SO = 23, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   405
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SO = 16, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   410
SO = 16, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   415
SO =   8, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   420
SO =   8, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   425
SO =   4, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   430
SO =   4, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   435
SO =   2, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   440
SO =   2, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   445
SO =   1, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   450
SO =   1, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   455
SO = 27, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   460
SO = 27, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   465
SO = 22, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   470
SO = 22, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   475
SO = 11, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   480
SO = 11, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   485
SO = 30, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   490
SO = 30, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   495
SO = 15, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   500
SO = 15, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   505
SO = 28, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   510
SO = 28, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   515
SO = 14, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   520
SO = 14, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   525
SO =   7, SerialIn =   0, Test = 0, CLK = 1, Reset = 0, Time =   530
SO =   7, SerialIn =   0, Test = 0, CLK = 0, Reset = 0, Time =   535

d. Synthesis timing report

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	8.574 ns	Worst Hold Slack (WHS):	0.139 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	5	Total Number of Endpoints:	5	Total Number of Endpoints:	6
All user specified timing constraints are met.					

e. Post-route simulation