Digital System Design and Implementation

Homework #1

姓名:黃鉦淳 學號:108303013

a. Verilog codes:

```
1  `timescale 1ns / 1ps
2
3  module Parity(A, P1);
4  input [3:0]A;
5  output P1;
6
7  wire tmp1, tmp2;
8  xnor U0(tmp1, A[0], A[1]);
9  xor  U1(tmp2,  tmp1, A[2]);
10 xor  U2(P1,   tmp2, A[3]);
11 endmodule
12
13 module MUX(A, O1, Mask, Sel);
14 input [3:0]A;
15 input Mask;
16 input [1:0]Sel;
17 output O1;
18 reg tmp;
19 always@(Sel)
20 begin
21     case(Sel)
22         2'b00: tmp = Mask&A[0];
23         2'b01: tmp = Mask&A[1];
24         2'b10: tmp = ~(Mask&A[2]);
25         2'b11: tmp = ~(Mask&A[3]);
26     endcase
27 end
28 assign O1 = tmp;
29 endmodule
```

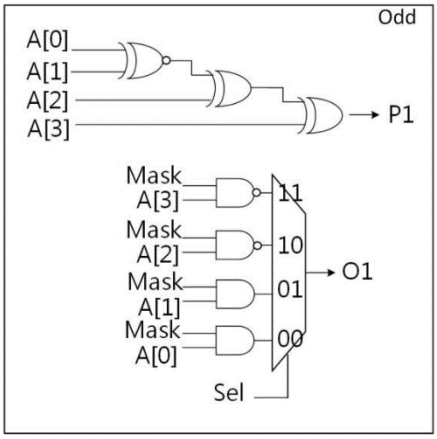

Fig. 1 Block diagram for odd-numbered students

b. Test bench:

```
1  `timescale 1ns / 1ps
2
3  module EX1_tb;
4  // Input
5  reg [3:0]A;
6  reg Mask;
7  reg [1:0]Sel;
8
9  // Output
10 wire P1;
11 wire O1;
12
13 // Instance
14 Parity parity(.A(A),.P1(P1));
15 MUX mux(.A(A),.O1(O1),.Mask(Mask),.Sel(Sel));
16
17 // Initial
18 initial begin
19     A=4'b0001; Mask=1; Sel=2'b10;
20     #80; A=4'b0001; Mask=1; Sel=2'b11;
21     #80; A=4'b1100; Mask=0; Sel=2'b00;
22     #80; A=4'b1110; Mask=0; Sel=2'b01;
23     #80; A=4'b0011; Mask=0; Sel=2'b00;
24     #80; A=4'b1010; Mask=1; Sel=2'b10;
25     #80; A=4'b0001; Mask=1; Sel=2'b01;
26     #80; A=4'b0110; Mask=1; Sel=2'b11;
27     #80; A=4'b1101; Mask=0; Sel=2'b01;
28     #80; A=4'b1100; Mask=0; Sel=2'b11;
29 end
30 endmodule
```

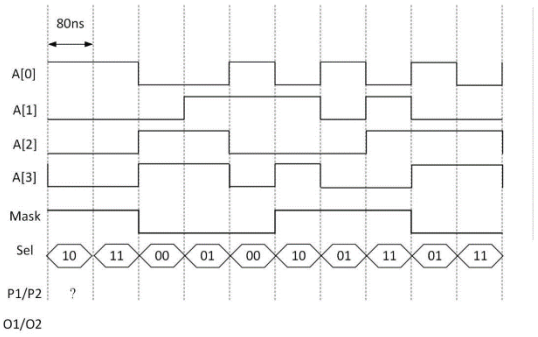

Fig. 2 Test pattern for students with Lab. time on Friday

c. Input/Output waveforms