

SMD Version  
V1 - Initial design

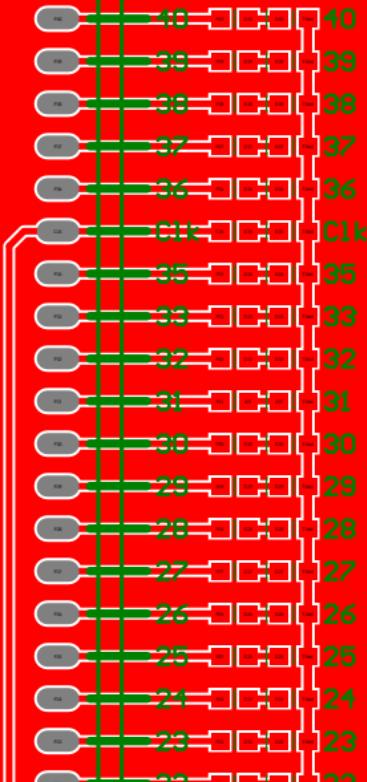
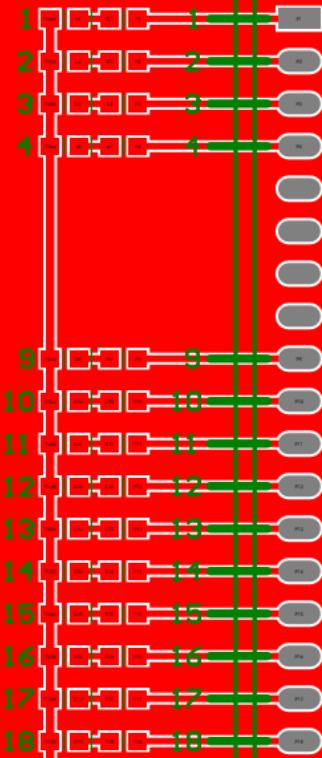
Tester

CP

CP

1

S1



TUdd

Vdd

Gnd

Vdd

TUdd

Clock

Power

J1

C5

F2

F1

R39

P29

C3

U2

C2

U1

C1

U6

C4

R3

D5

C8

R40

D6

C9

R41

D7

C10

R42

D8

C11

R43

D9

C12

R44

D10

C13

R45

D11

R2

P1

R1

R3

R4

R5

R6

R7

R8

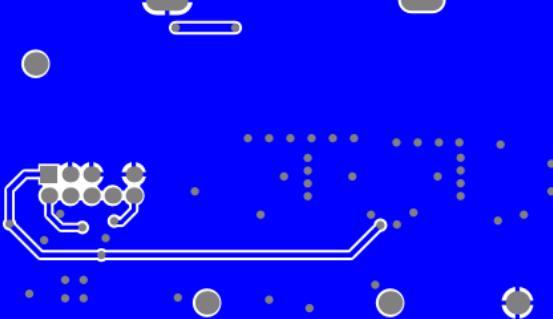
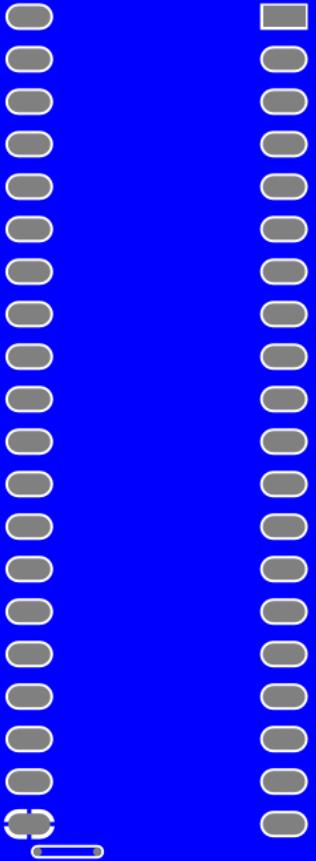
R9

R10

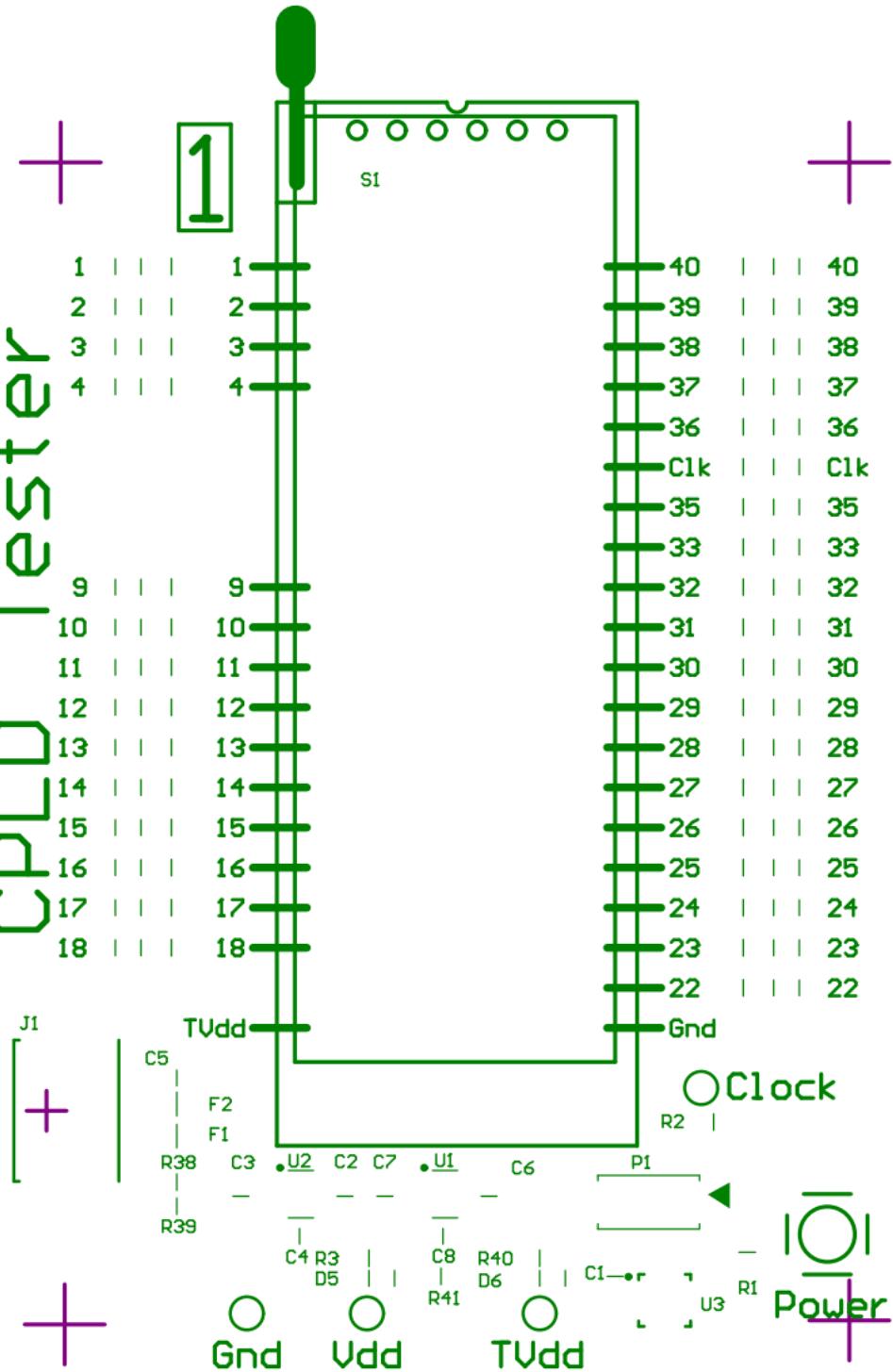
R11

R12

CPLD Tester SMT Version  
Version = V1



# CPU Tester



# CPU Tester

