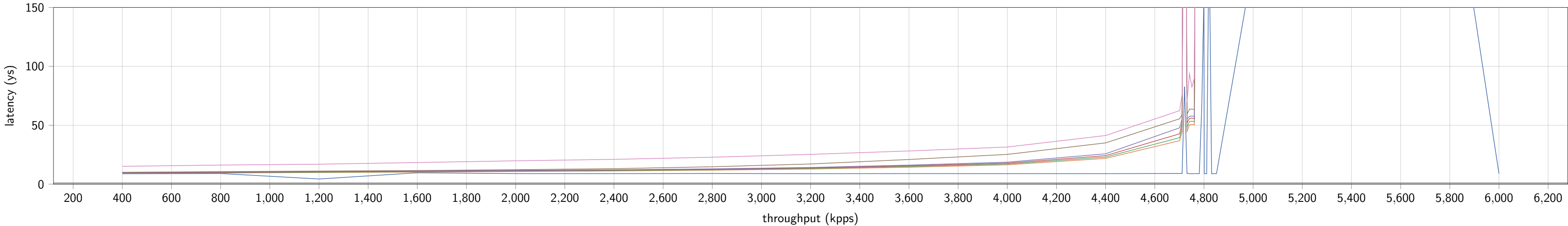
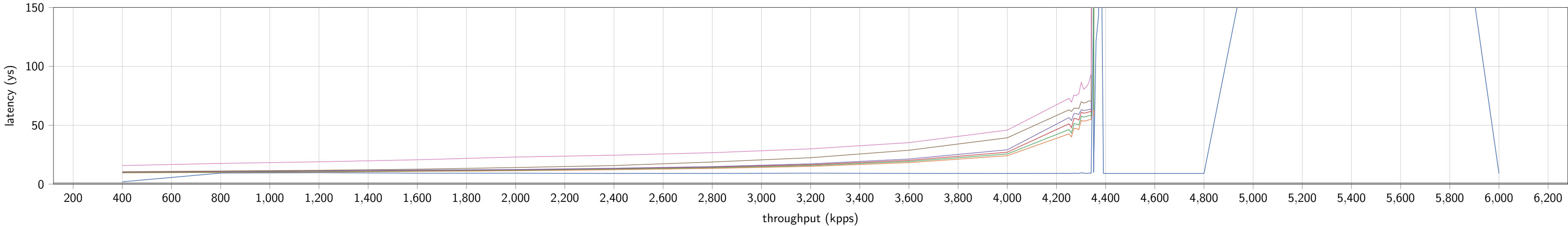


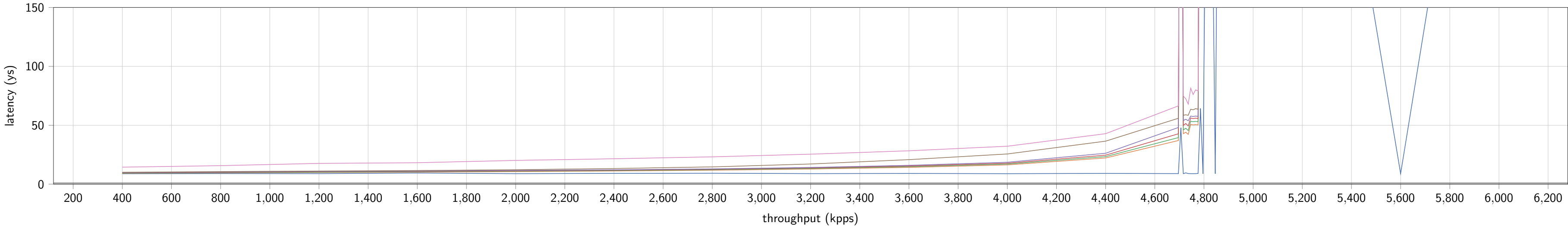
l2\_bridging\_cnf0\_mbit\*



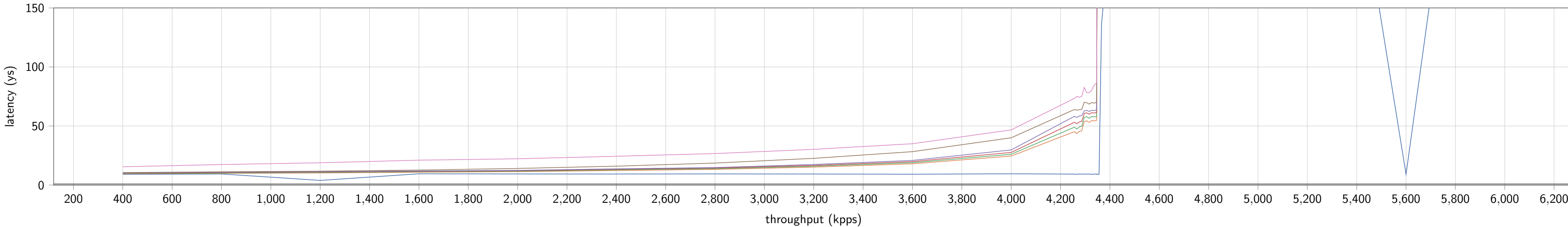
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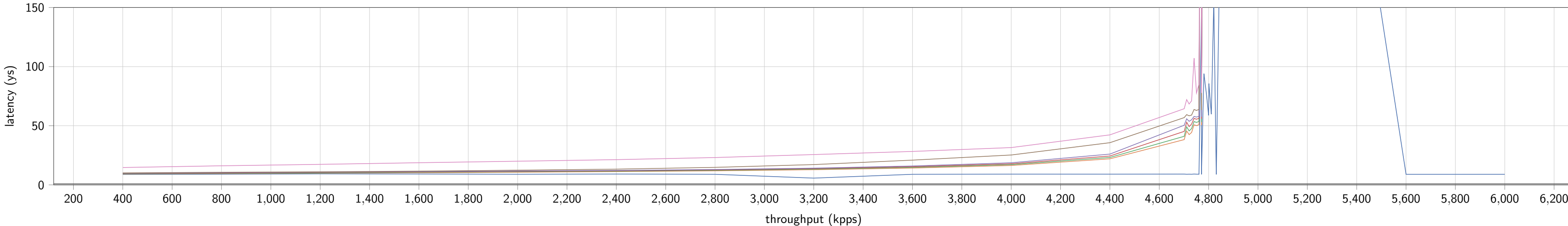
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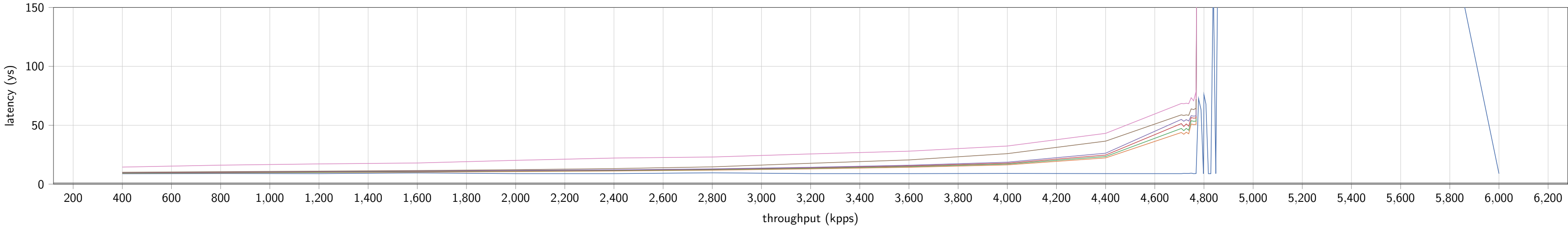
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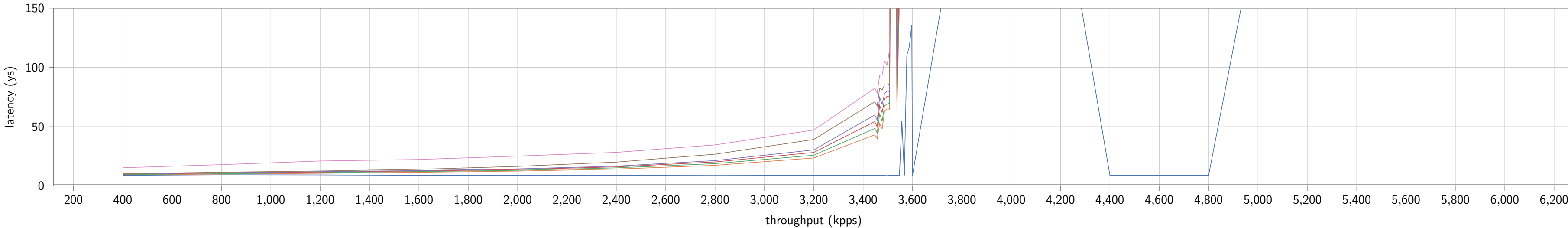
l2\_bridging\_cnf4\_mbit\*



l2\_bridging\_cnf5\_mbit\*

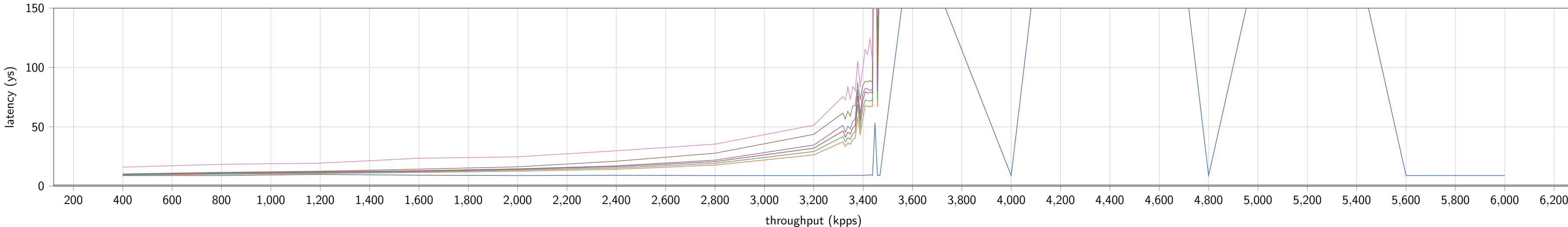


l2\_multimac\_00000100\_mbit\*

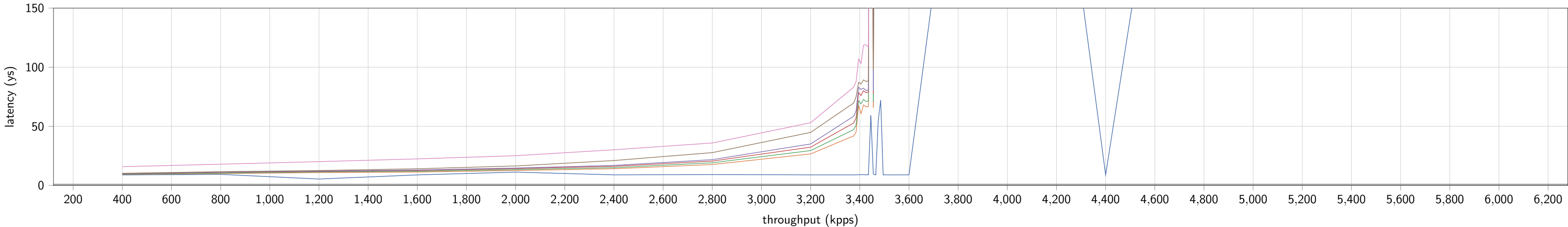




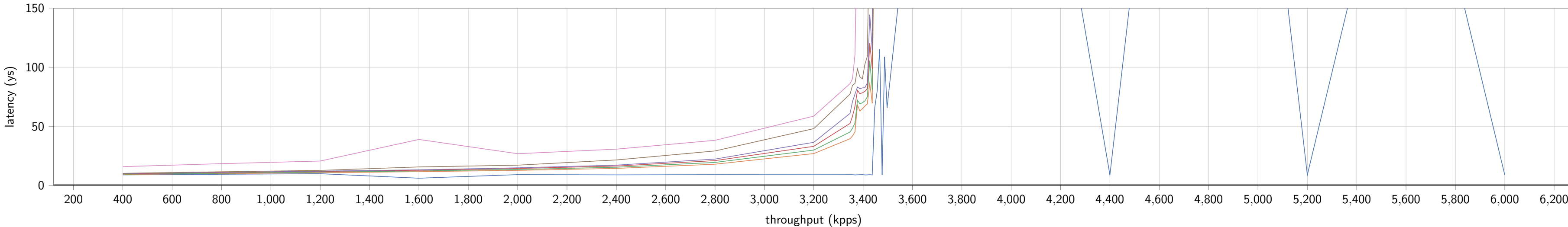
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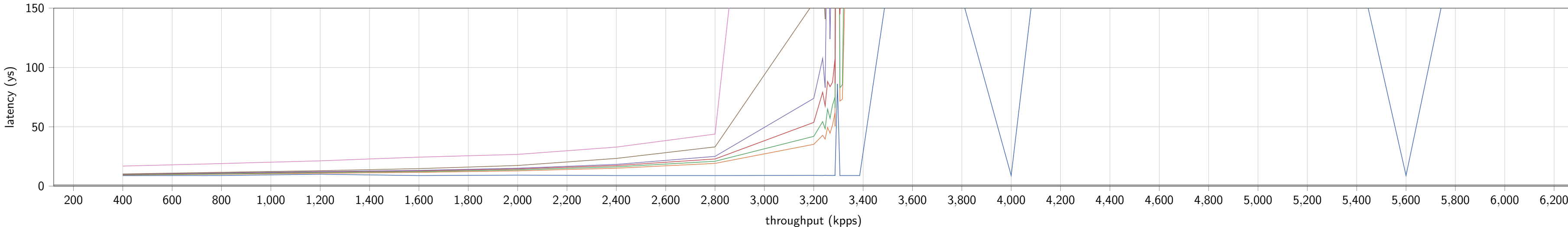
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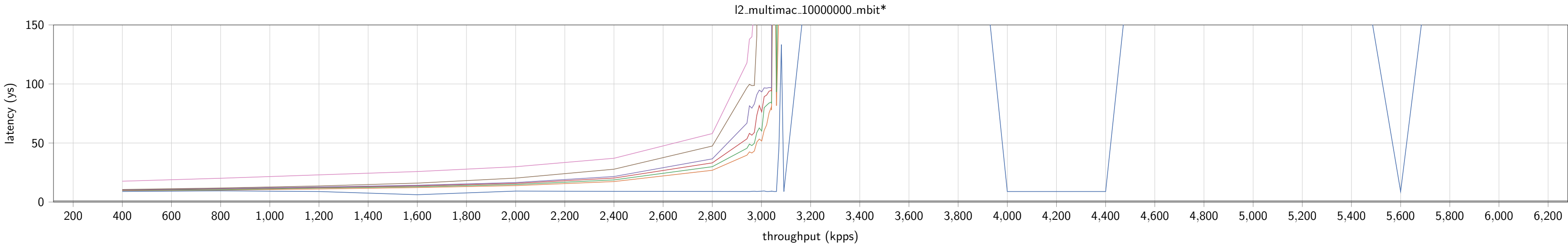


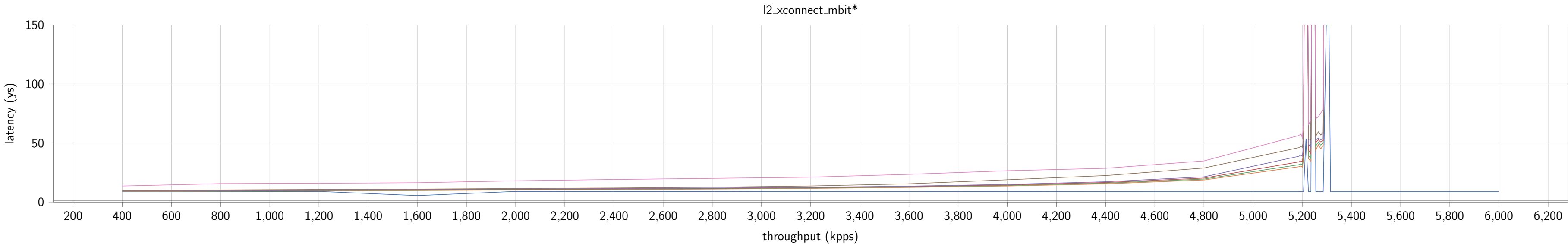
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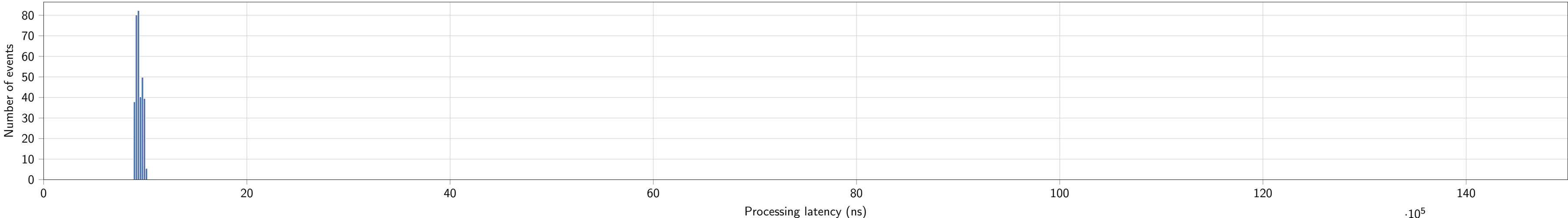
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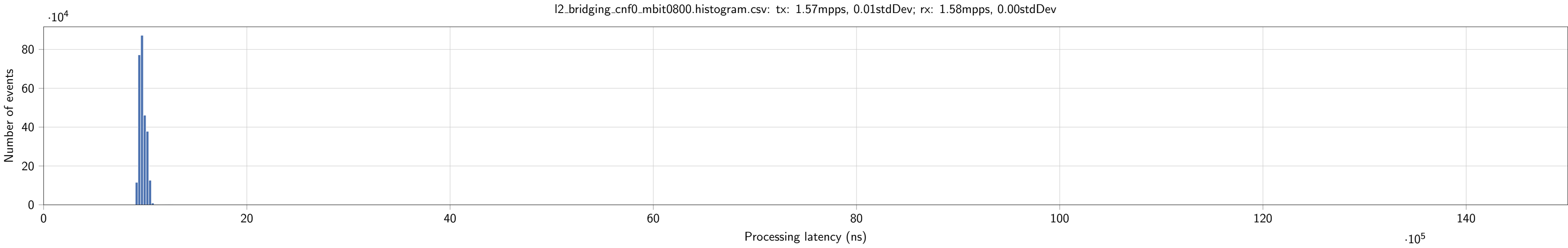




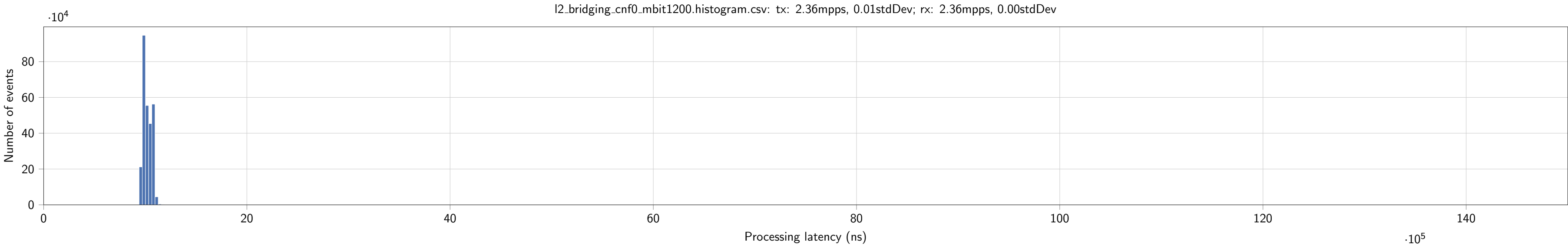


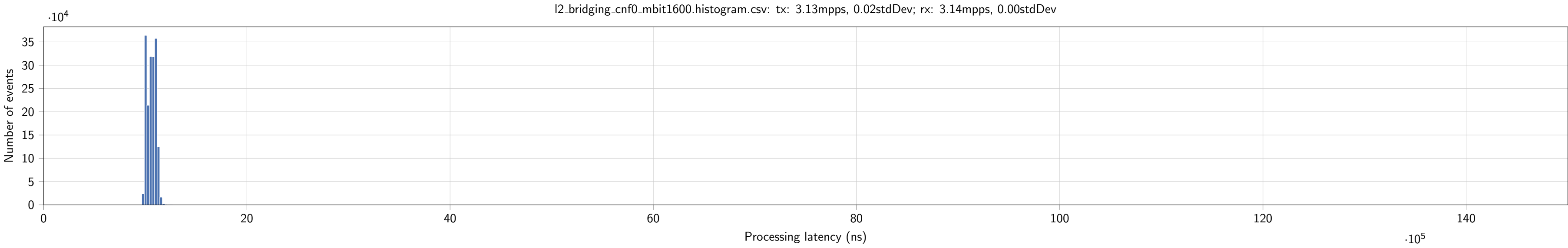
l2\_bridging\_cnf0\_mbit0400.histogram.csv: tx: 0.80mpps, 0.00stdDev; rx: 0.80mpps, 0.00stdDev



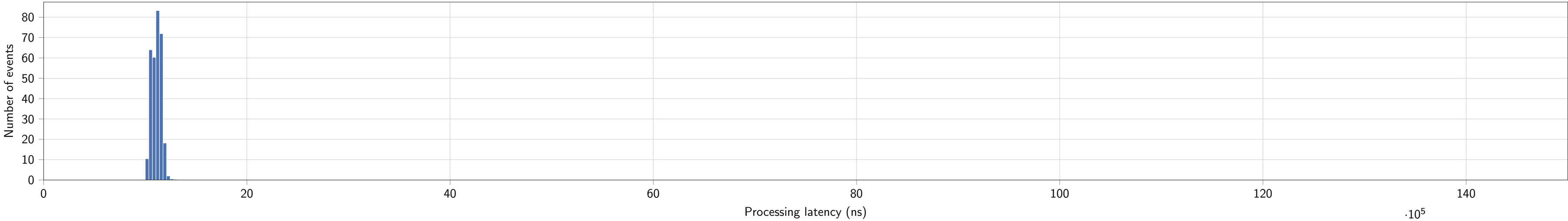


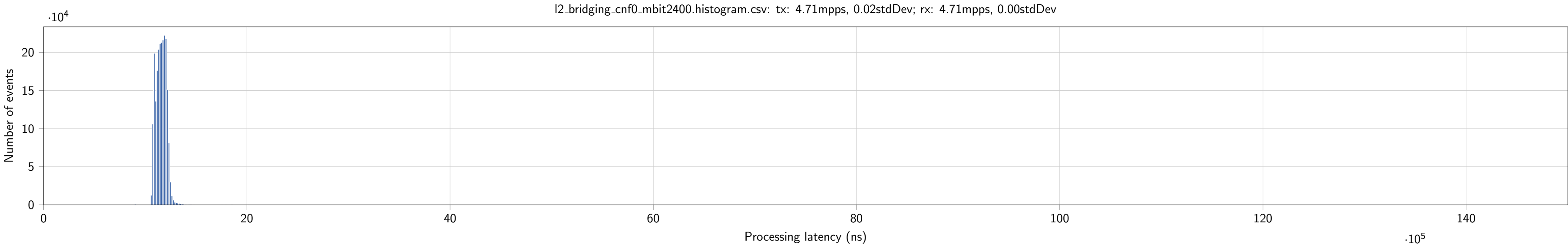




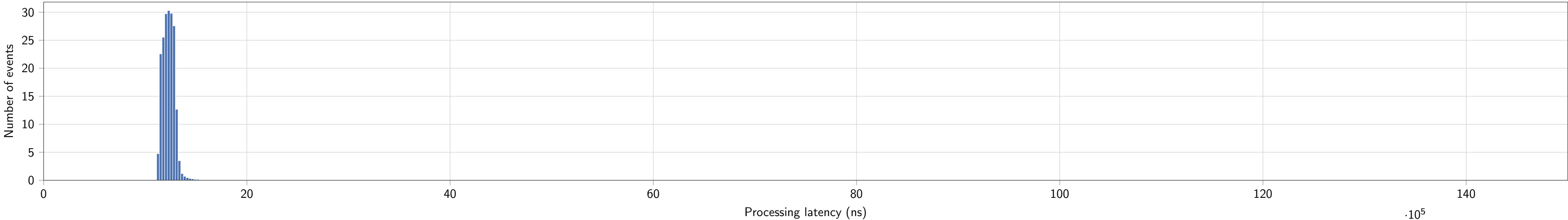


l2\_bridging\_cnf0\_mbit2000.histogram.csv: tx: 3.92mpps, 0.02stdDev; rx: 3.92mpps, 0.00stdDev

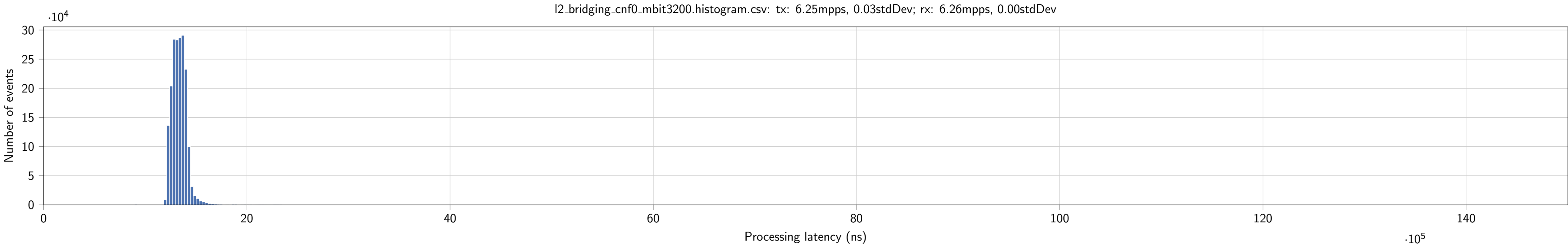




l2\_bridging\_cnf0\_mbit2800.histogram.csv: tx: 5.49mpps, 0.03stdDev; rx: 5.49mpps, 0.00stdDev



l2\_bridging\_cnf0\_mbit3200.histogram.csv: tx: 6.25mpps, 0.03stdDev; rx: 6.26mpps, 0.00stdDev



l2\_bridging\_cnf0\_mbit3600.histogram.csv: tx: 7.06mpps, 0.04stdDev; rx: 7.07mpps, 0.00stdDev

Number of events

20.0  
17.5  
15.0  
12.5  
10.0  
7.5  
5.0  
2.5  
0.0

0

20

40

60

80

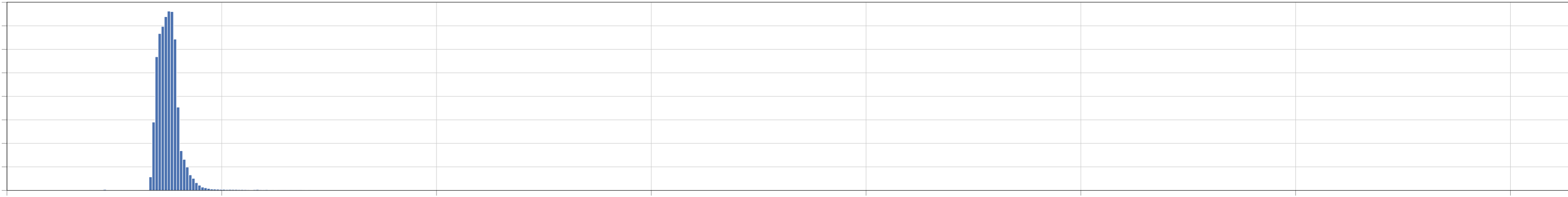
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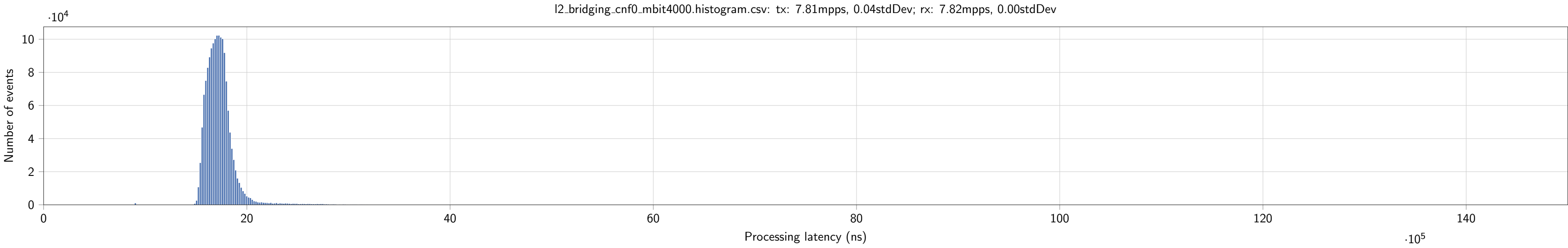
120

140

Processing latency (ns)

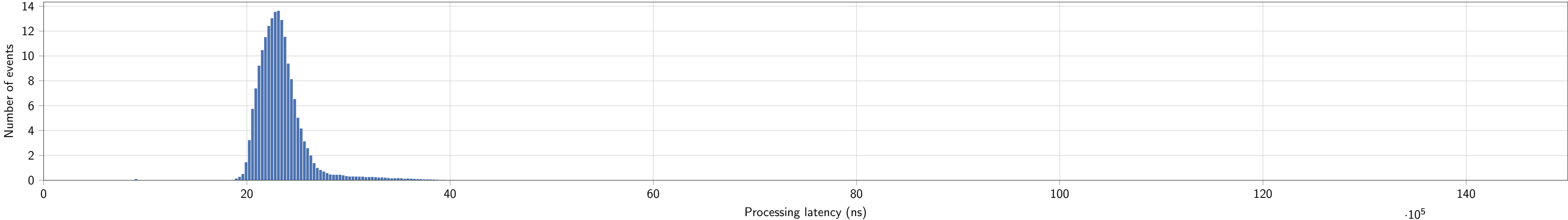
$\cdot 10^5$



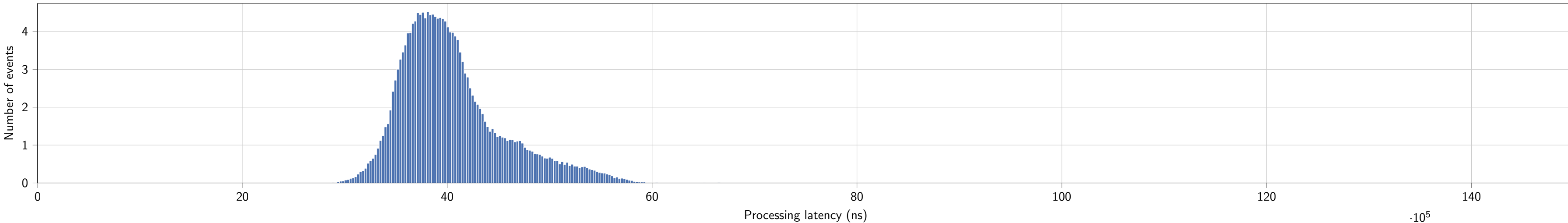




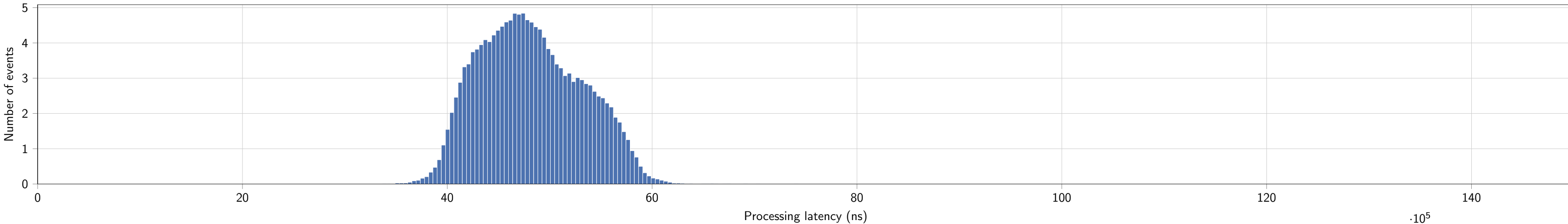
l2\_bridging\_cnf0\_mbit4400.histogram.csv: tx: 8.62mpps, 0.04stdDev; rx: 8.63mpps, 0.00stdDev

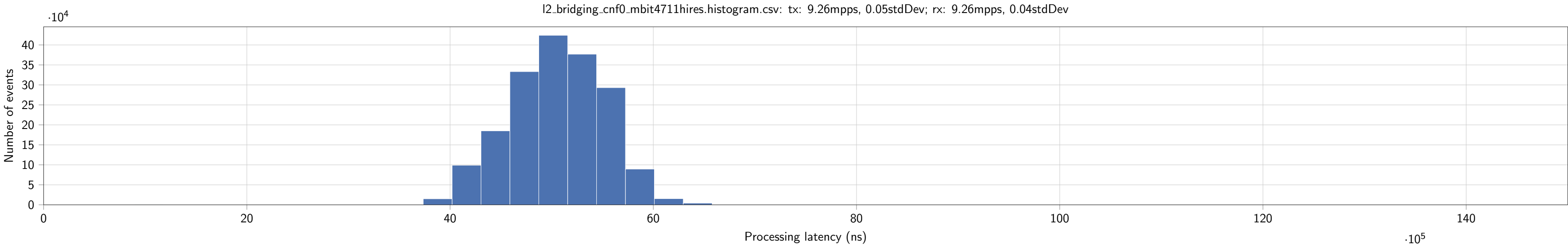


l2\_bridging\_cnf0\_mbit4701hires.histogram.csv: tx: 9.19mpps, 0.04stdDev; rx: 9.20mpps, 0.00stdDev

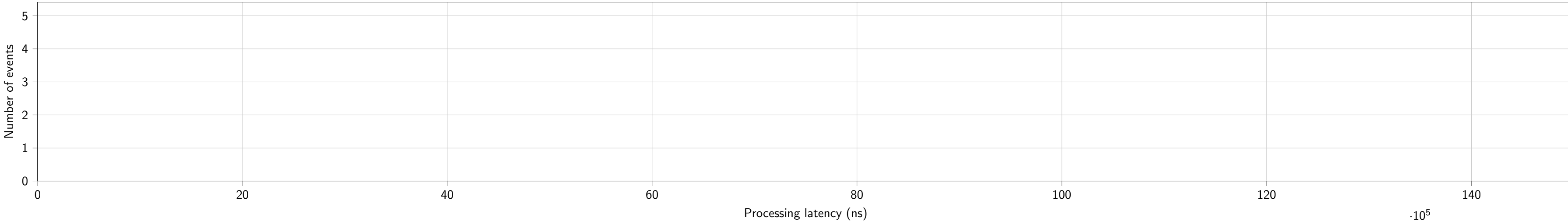


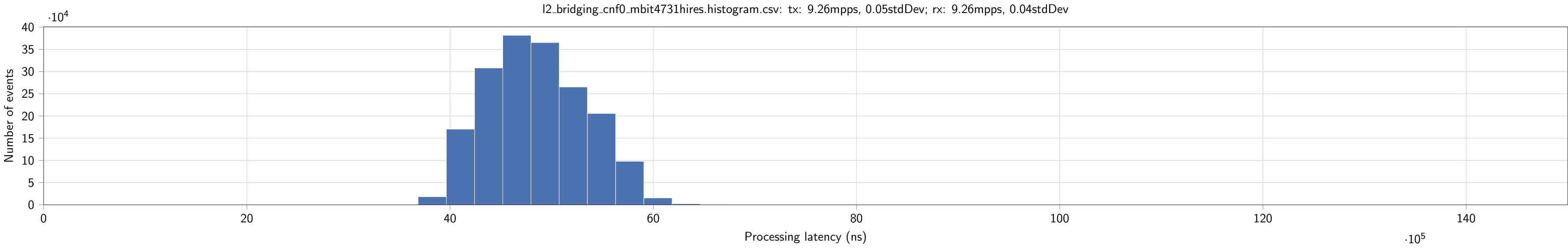
l2\_bridging\_cnf0\_mbit4711\_final.histogram.csv: tx: 9.26mpps, 0.05stdDev; rx: 9.27mpps, 0.00stdDev

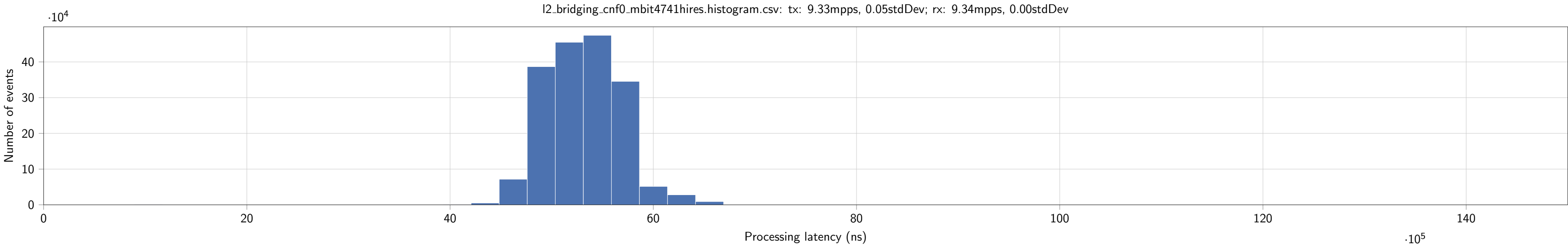




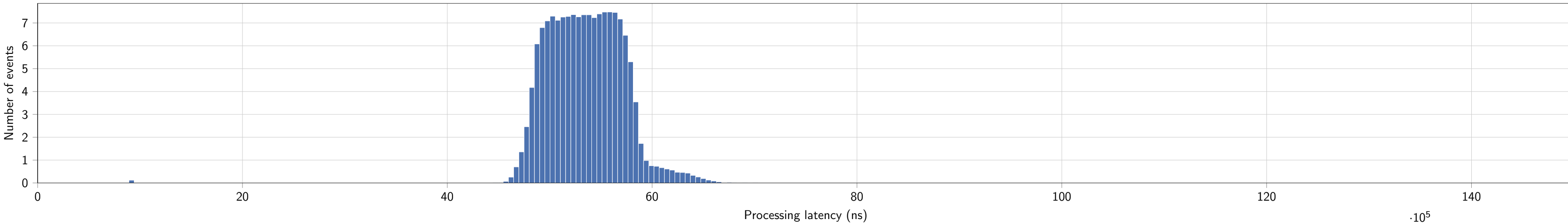
l2\_bridging\_cnf0\_mbit4721hires.histogram.csv: tx: 9.25mpps, 0.04stdDev; rx: 9.23mpps, 0.00stdDev



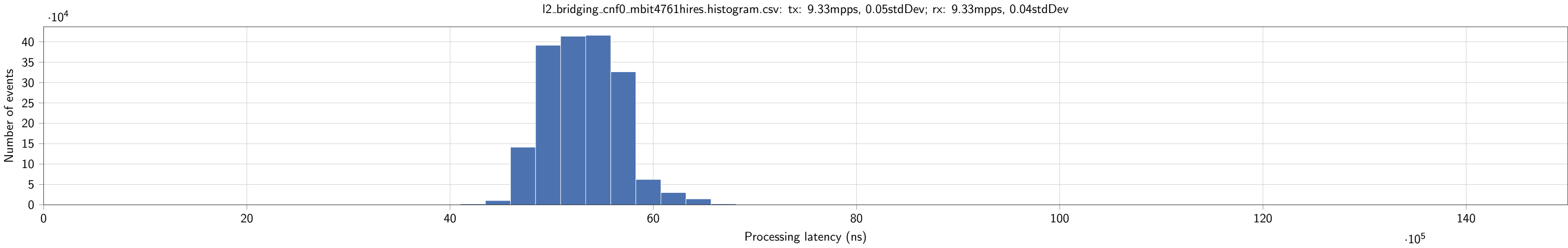




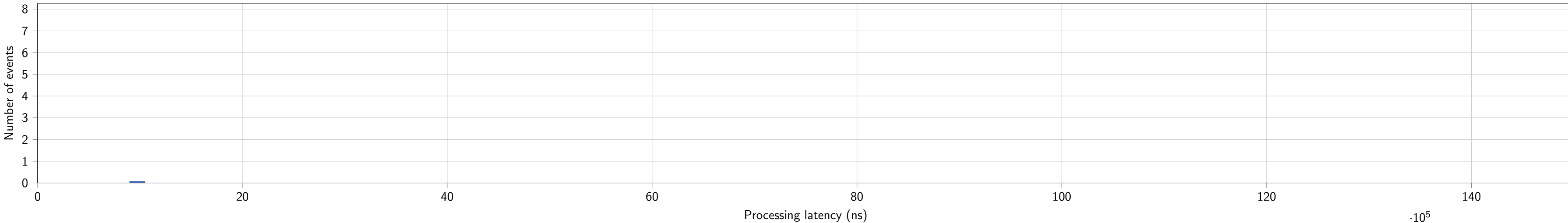
l2\_bridging\_cnf0\_mbit4751hires.histogram.csv: tx: 9.32mpps, 0.05stdDev; rx: 9.34mpps, 0.00stdDev



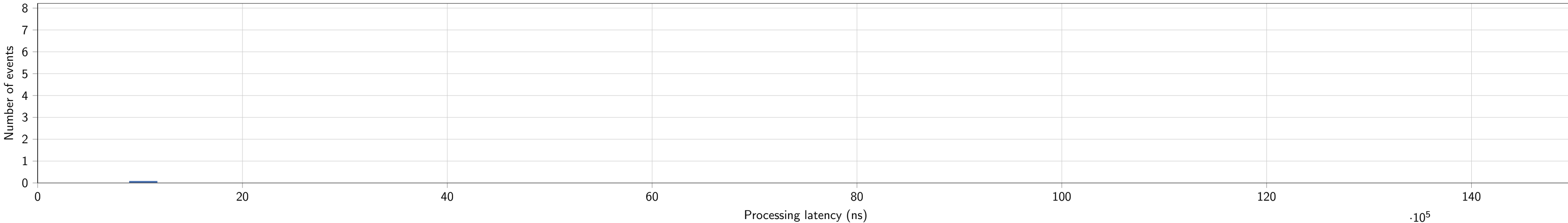




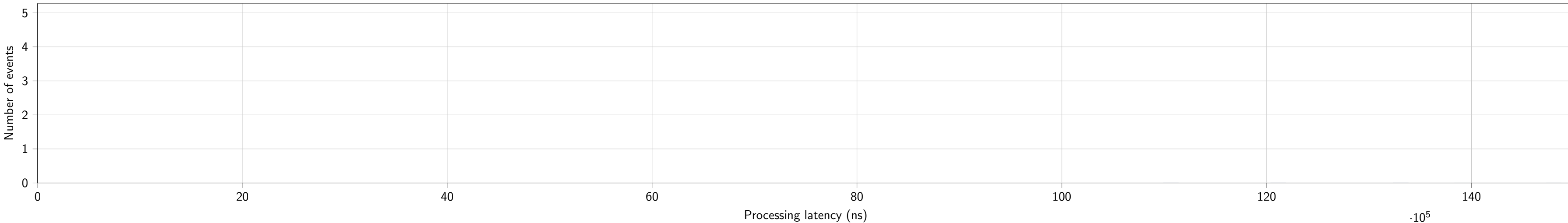
l2\_bridging\_cnf0\_mbit4771hires.histogram.csv: tx: 9.32mpps, 0.05stdDev; rx: 9.28mpps, 0.00stdDev



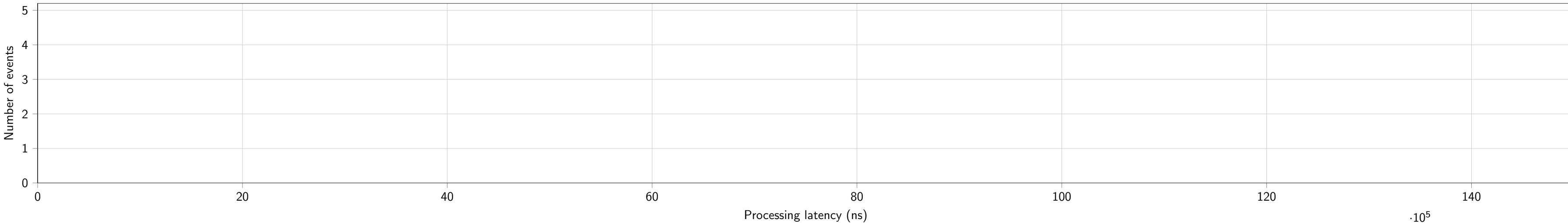
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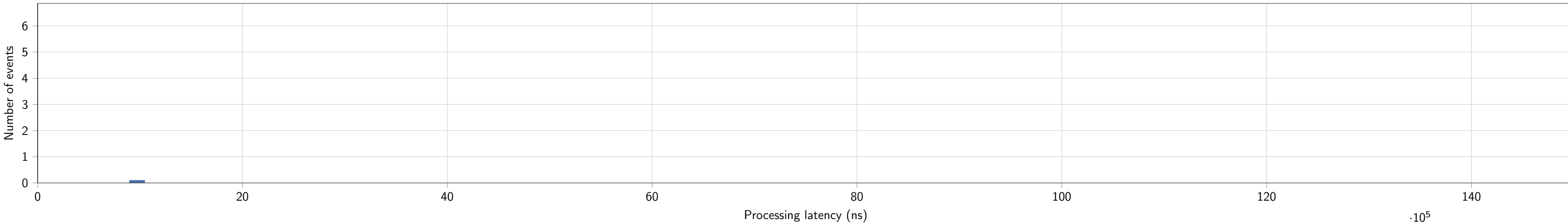
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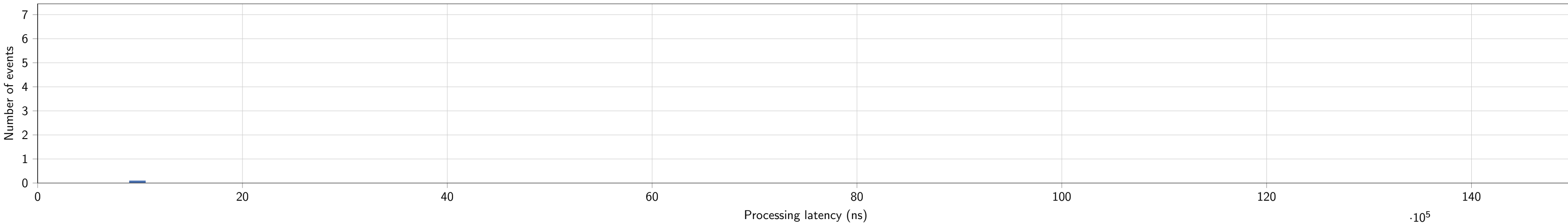
l2\_bridging\_cnf0\_mbit4800.histogram.csv: tx: 9.39mpps, 0.05stdDev; rx: 9.34mpps, 0.00stdDev



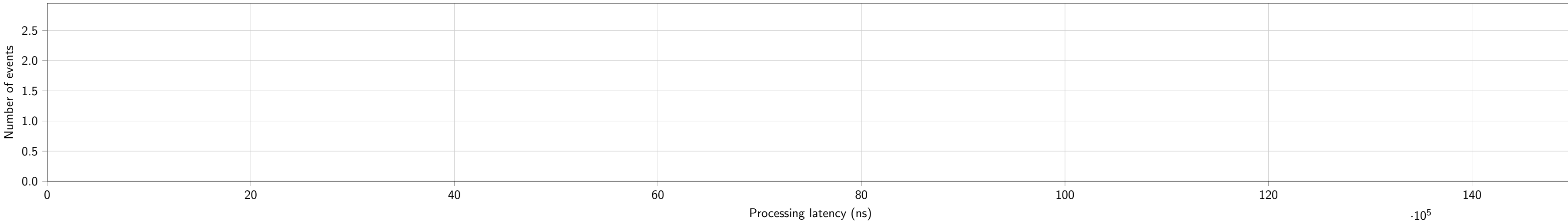
l2\_bridging\_cnf0\_mbit4801hires.histogram.csv: tx: 9.39mpps, 0.05stdDev; rx: 9.37mpps, 0.00stdDev



l2\_bridging\_cnf0\_mbit4811hires.histogram.csv: tx: 9.39mpps, 0.05stdDev; rx: 9.36mpps, 0.00stdDev

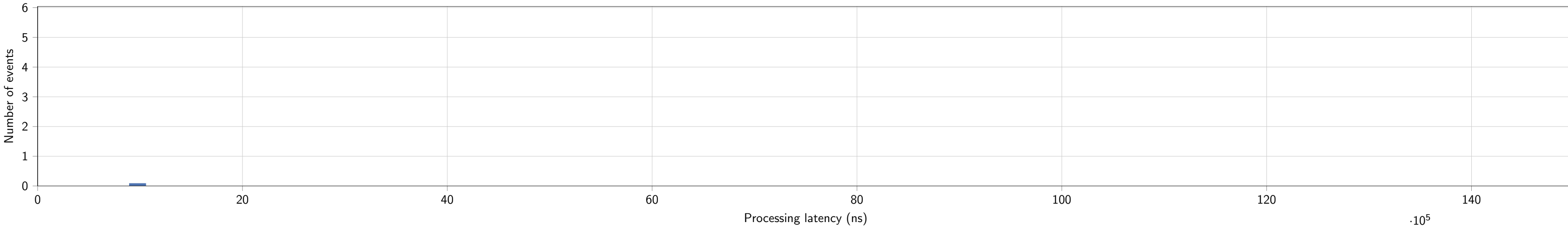


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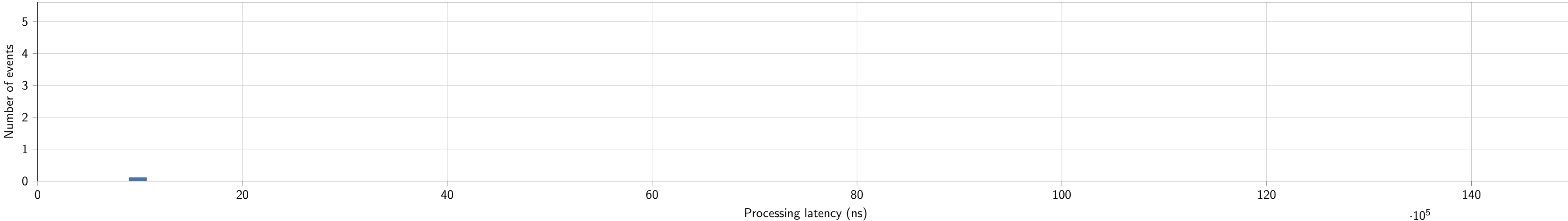




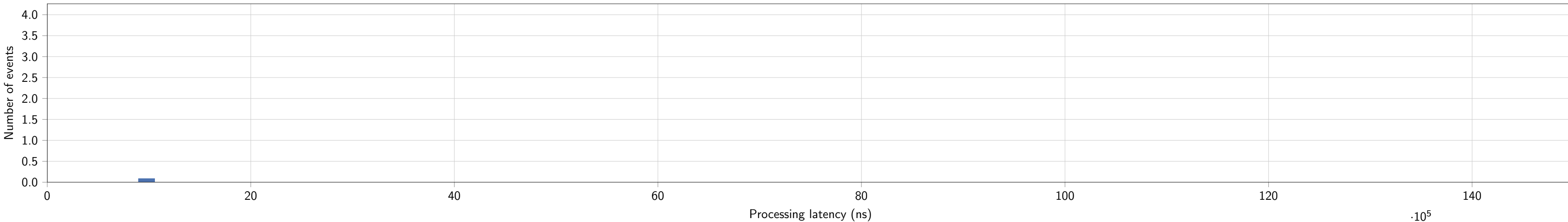
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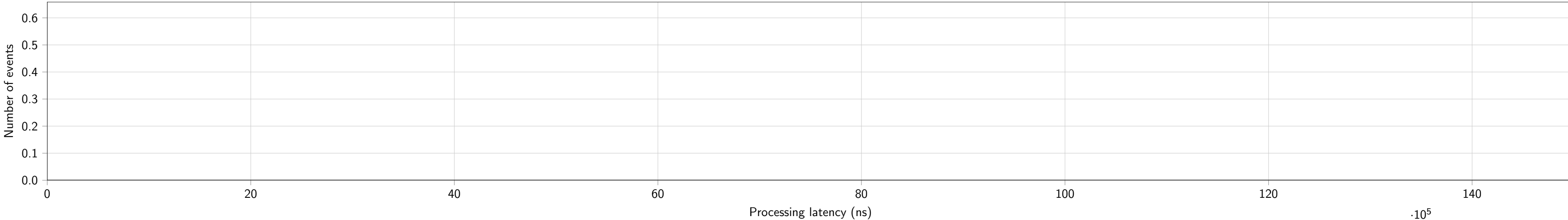
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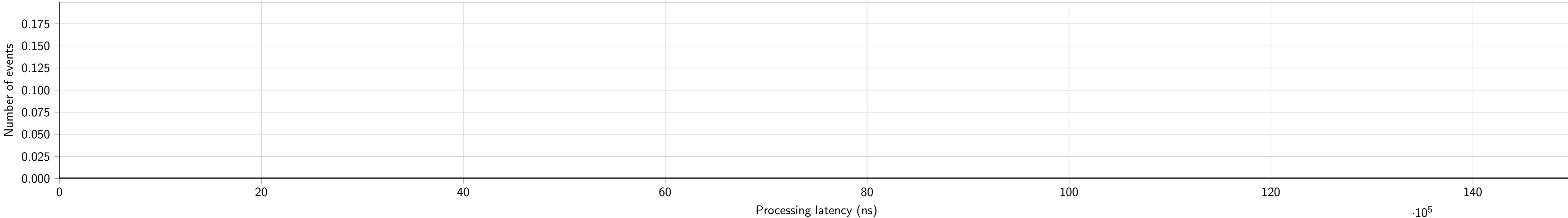
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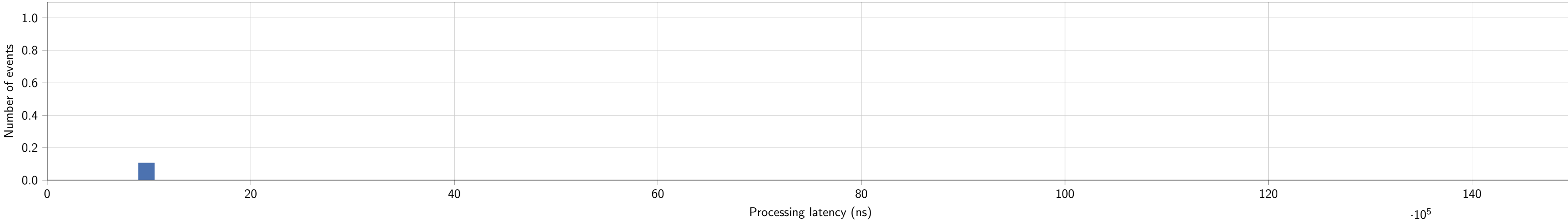
l2\_bridging\_cnf0\_mbit5200.histogram.csv: tx: 10.15mpps, 0.05stdDev; rx: 9.40mpps, 0.00stdDev



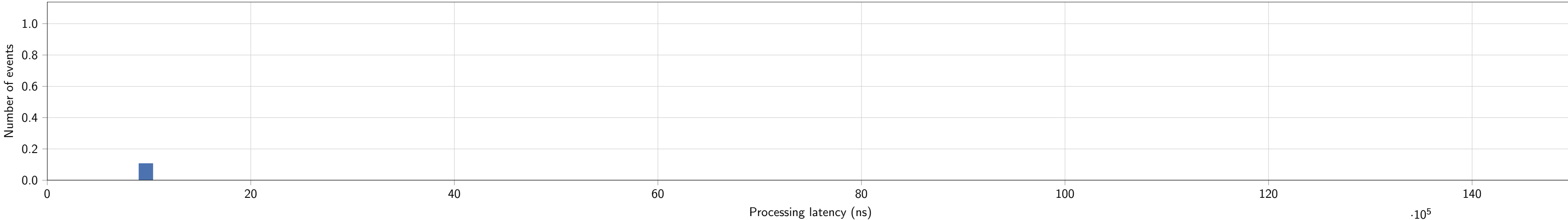
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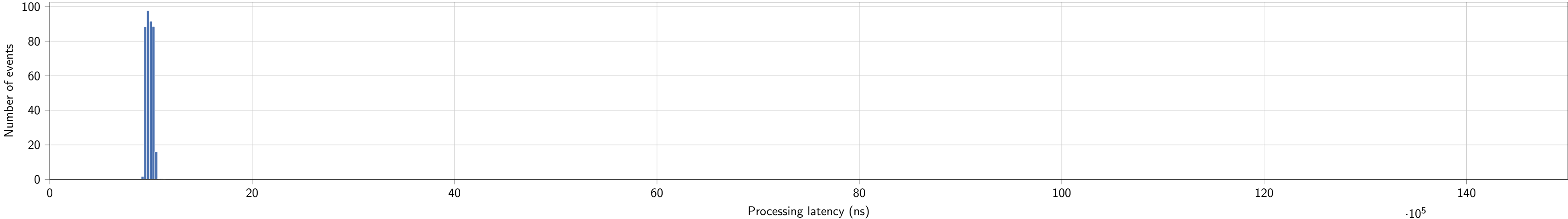
l2\_bridging\_cnf0\_mbit6000.histogram.csv: tx: 11.78mpps, 0.06stdDev; rx: 9.37mpps, 0.00stdDev



l2\_bridging\_cnf0\_mbit9000.histogram.csv: tx: 14.86mpps, 0.08stdDev; rx: 9.38mpps, 0.00stdDev

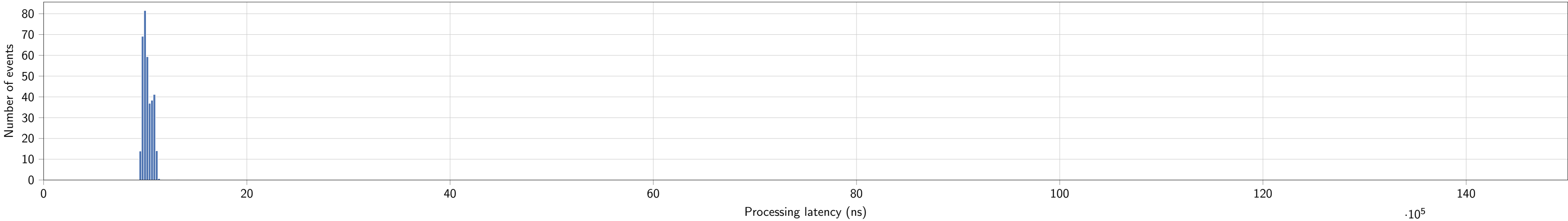


l2\_bridging\_cnf1\_mbit0400.histogram.csv: tx: 0.80mpps, 0.00stdDev; rx: 0.80mpps, 0.00stdDev

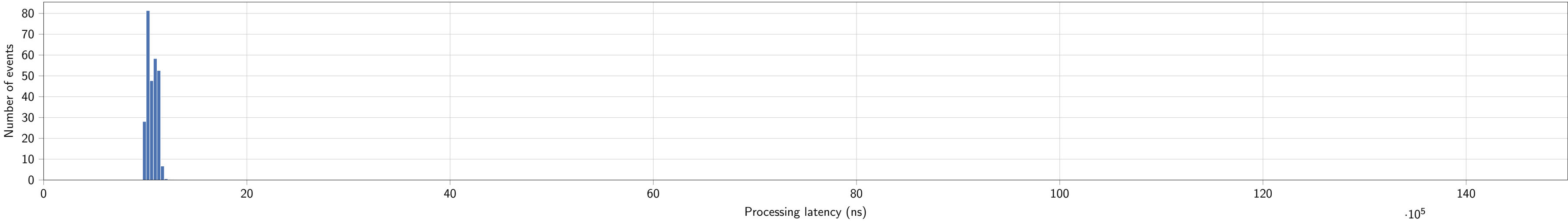




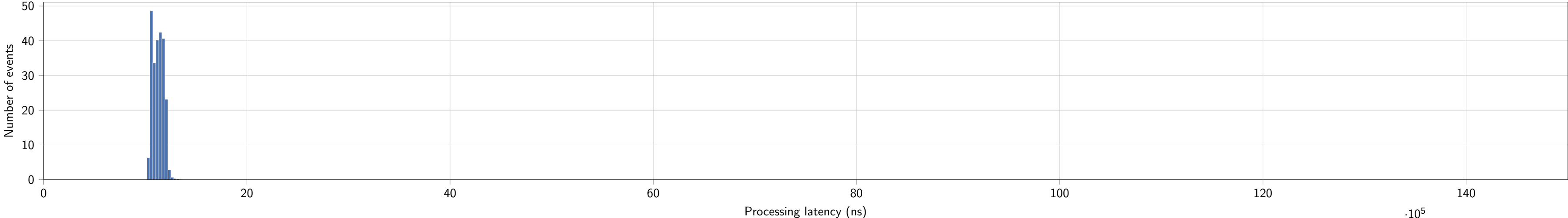
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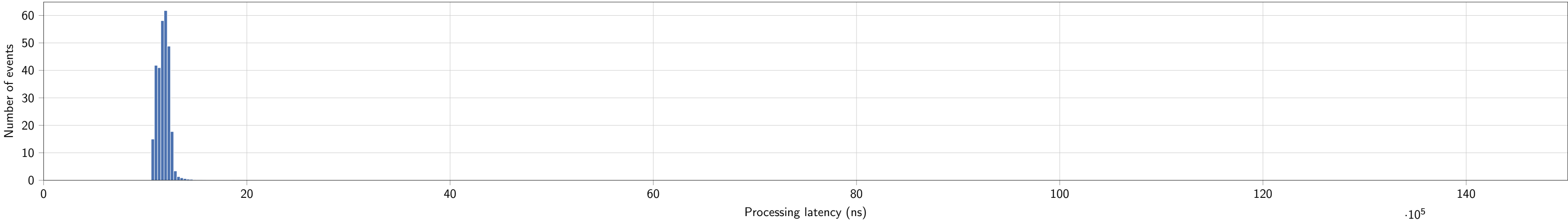
l2\_bridging\_cnf1\_mbit1200.histogram.csv: tx: 2.36mpps, 0.01stdDev; rx: 2.36mpps, 0.00stdDev



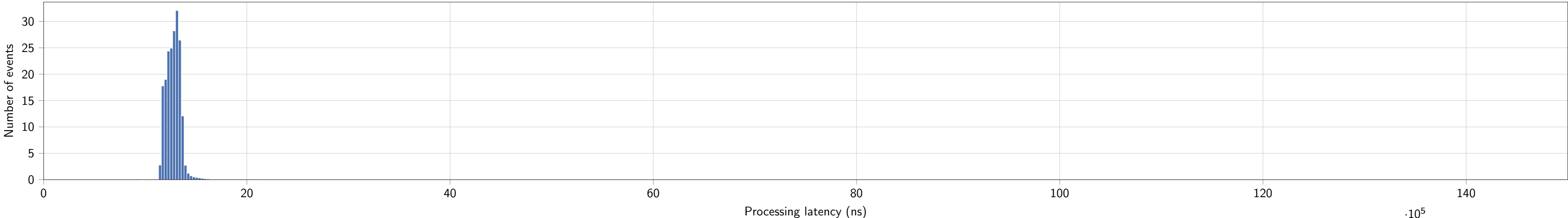
l2\_bridging\_cnf1\_mbit1600.histogram.csv: tx: 3.13mpps, 0.01stdDev; rx: 3.14mpps, 0.00stdDev



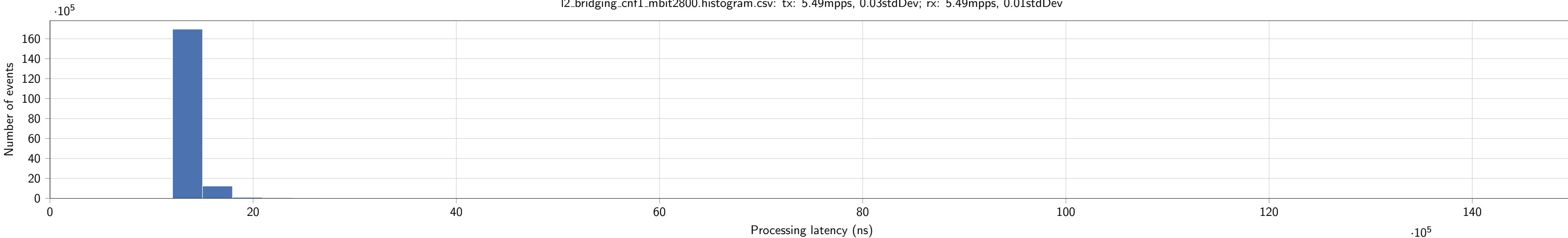
l2\_bridging\_cnf1\_mbit2000.histogram.csv: tx: 3.92mpps, 0.02stdDev; rx: 3.92mpps, 0.00stdDev



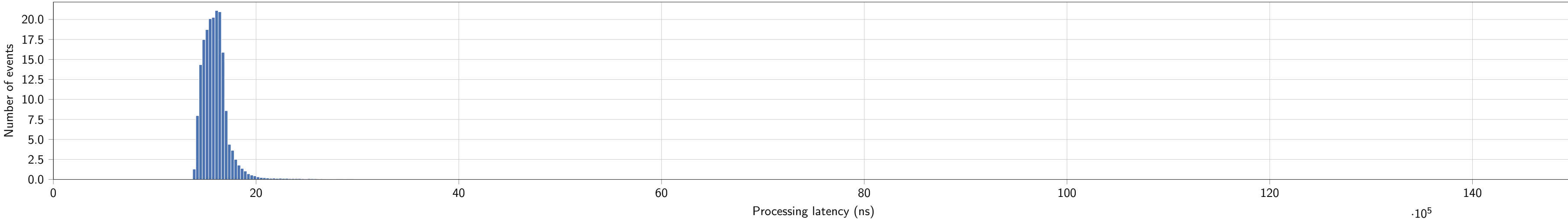
l2\_bridging\_cnf1\_mbit2400.histogram.csv: tx: 4.70mpps, 0.02stdDev; rx: 4.71mpps, 0.00stdDev



l2\_bridging\_cnf1\_mbit2800.histogram.csv: tx: 5.49mpps, 0.03stdDev; rx: 5.49mpps, 0.01stdDev



l2\_bridging\_cnf1\_mbit3200.histogram.csv: tx: 6.25mpps, 0.03stdDev; rx: 6.26mpps, 0.00stdDev



l2\_bridging\_cnf1\_mbit3600.histogram.csv: tx: 7.06mpps, 0.03stdDev; rx: 7.07mpps, 0.00stdDev

Number of events

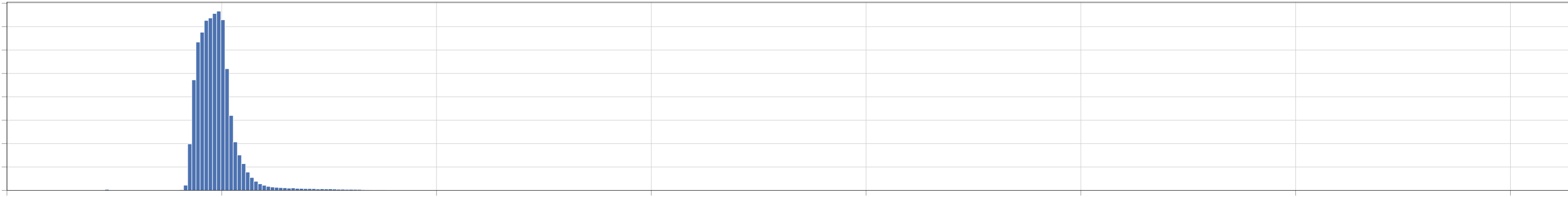
20.0  
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15.0  
12.5  
10.0  
7.5  
5.0  
2.5  
0.0

0 20 40 60 80 100 120 140

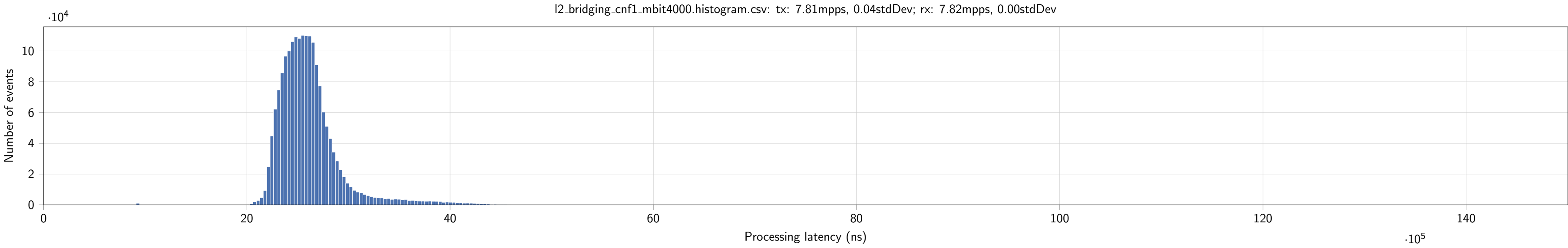
Processing latency (ns)

$\cdot 10^5$

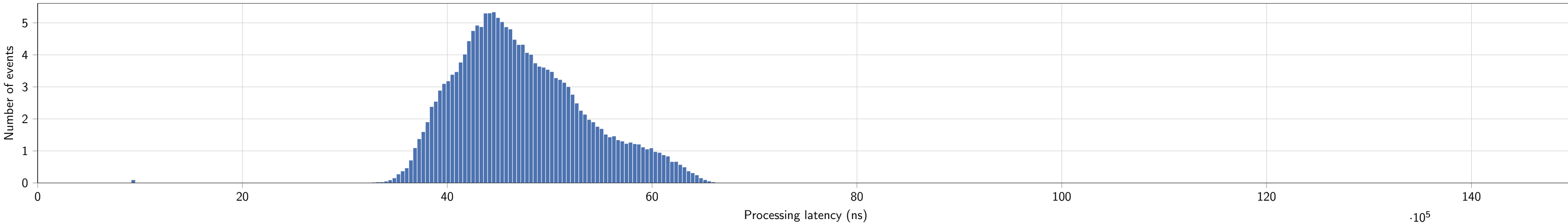
$\cdot 10^4$



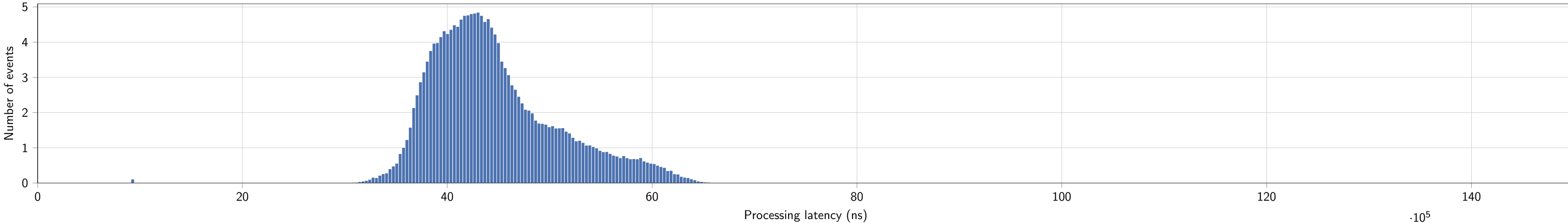




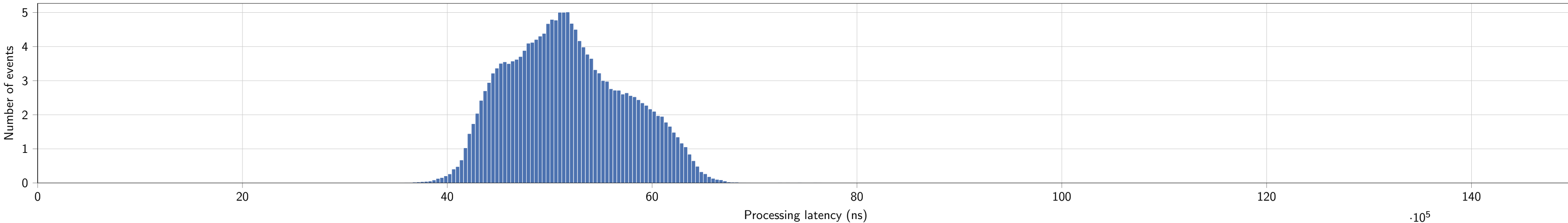
l2\_bridging\_cnf1\_mbit4251hires.histogram.csv: tx: 8.33mpps, 0.04stdDev; rx: 8.34mpps, 0.00stdDev



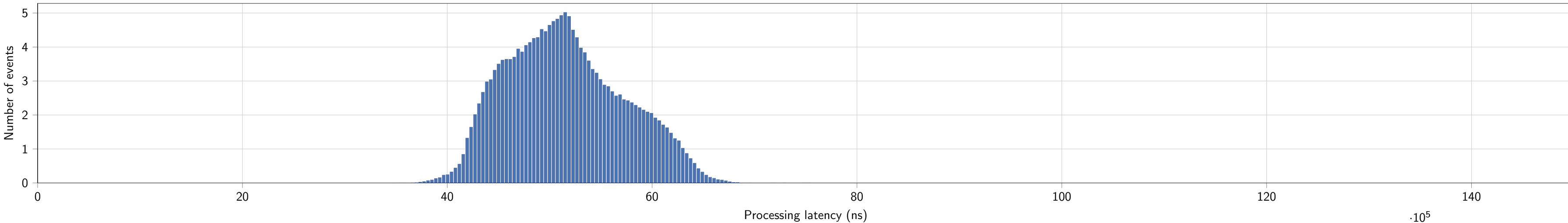
l2\_bridging\_cnf1\_mbit4261hires.histogram.csv: tx: 8.33mpps, 0.04stdDev; rx: 8.34mpps, 0.00stdDev



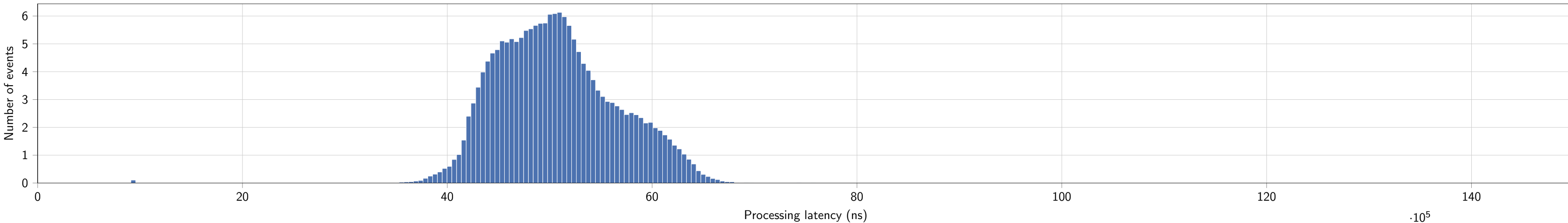
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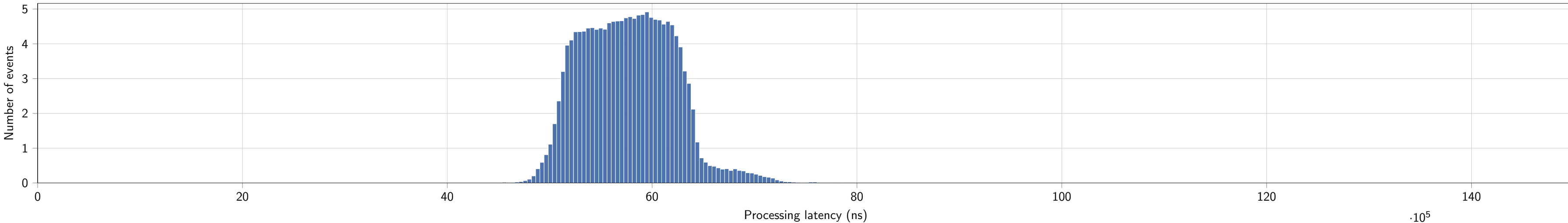
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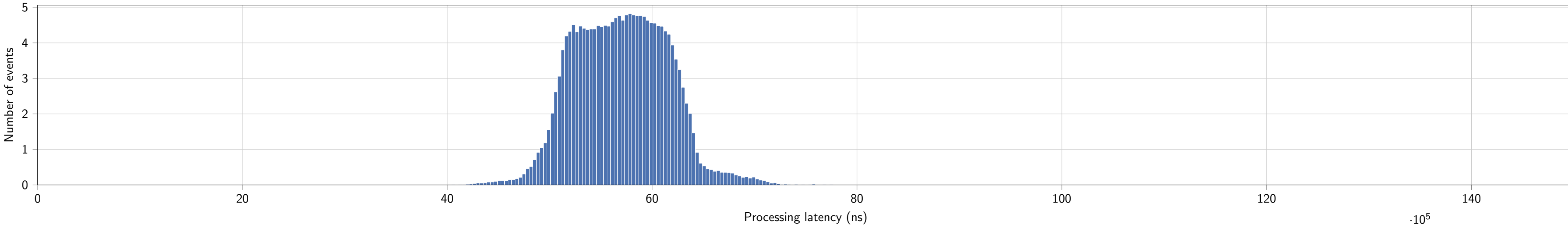
l2\_bridging\_cnf1\_mbit4291hires.histogram.csv: tx: 8.39mpps, 0.04stdDev; rx: 8.40mpps, 0.00stdDev



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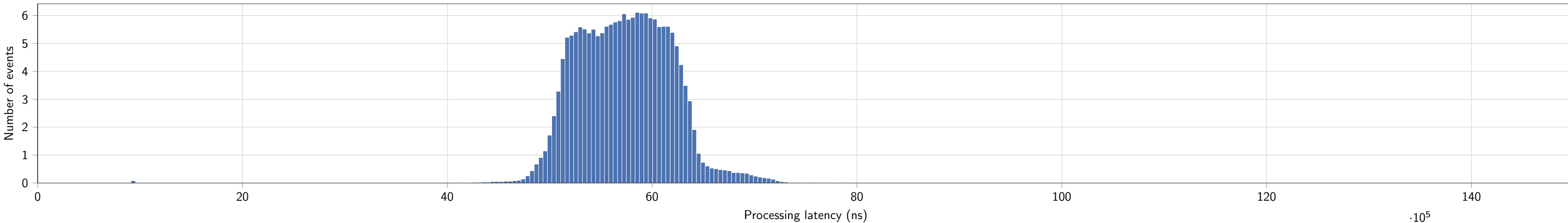


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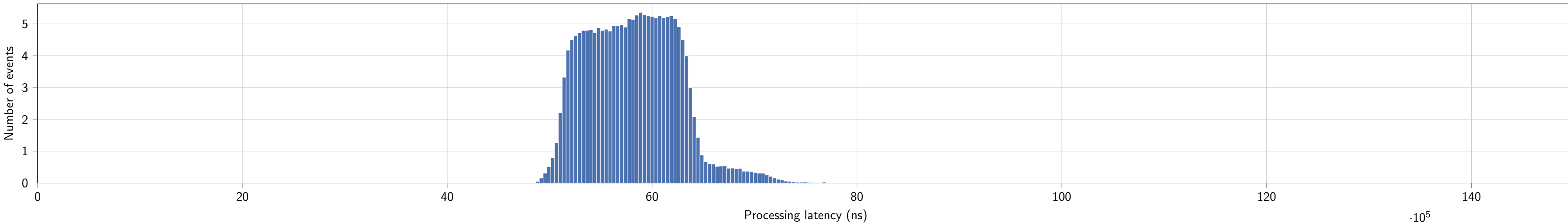




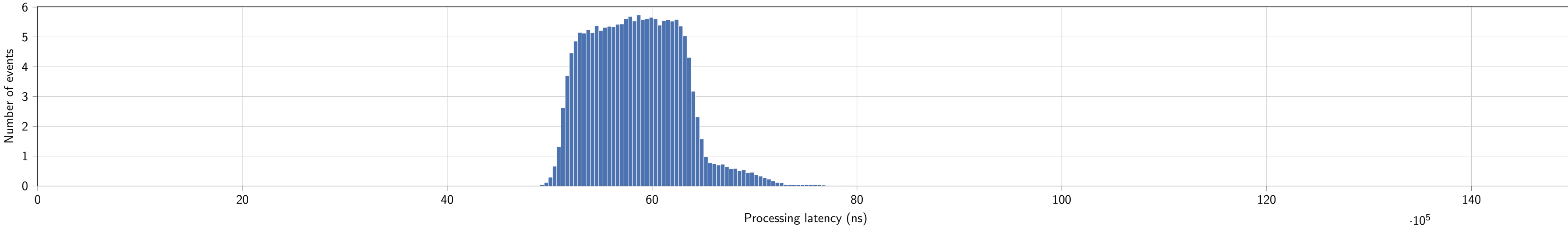
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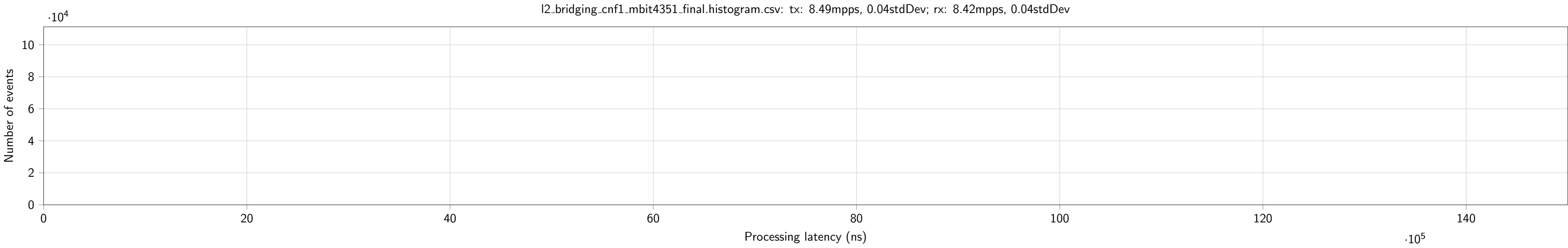


l2\_bridging\_cnf1\_mbit4331hires.histogram.csv: tx: 8.50mpps, 0.04stdDev; rx: 8.51mpps, 0.00stdDev

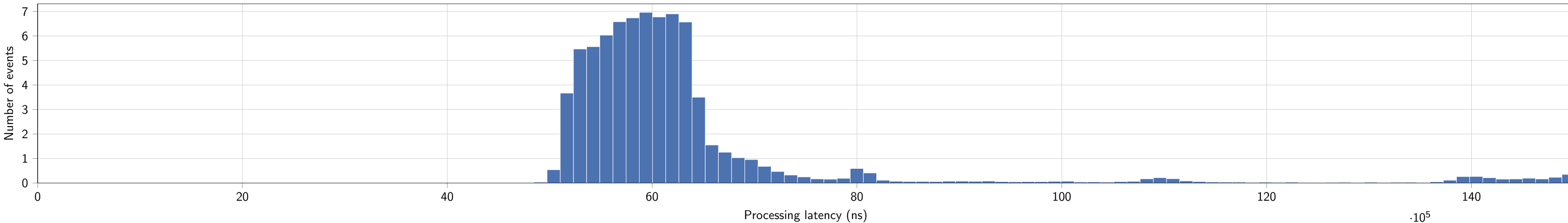


l2\_bridging\_cnf1\_mbit4341hires.histogram.csv: tx: 8.50mpps, 0.04stdDev; rx: 8.51mpps, 0.00stdDev

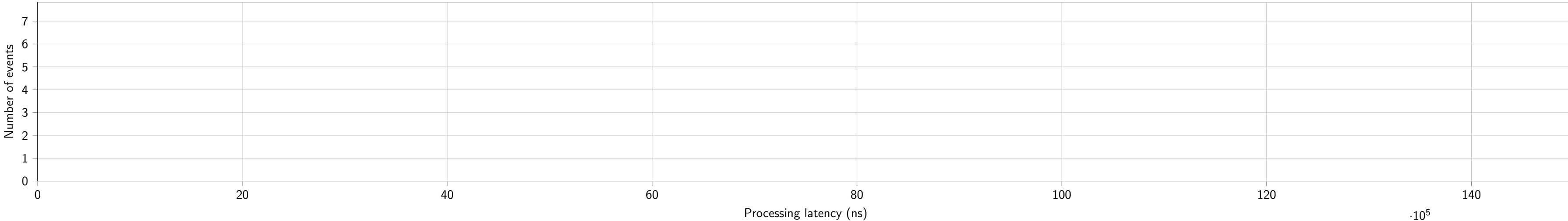




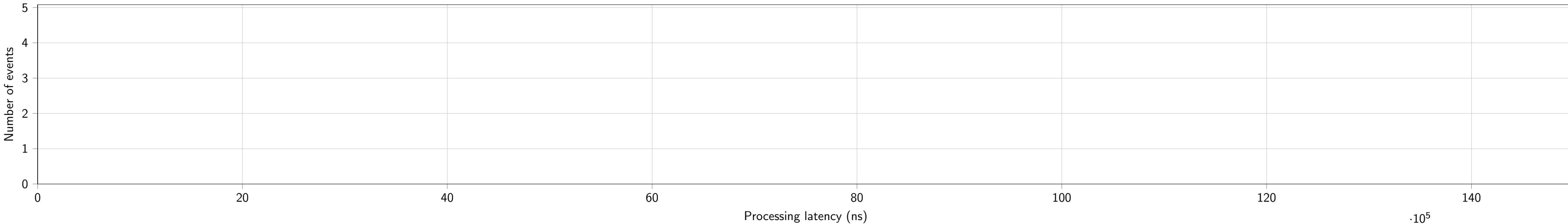
l2\_bridging\_cnf1\_mbit4351hires.histogram.csv: tx: 8.50mpps, 0.04stdDev; rx: 8.51mpps, 0.00stdDev



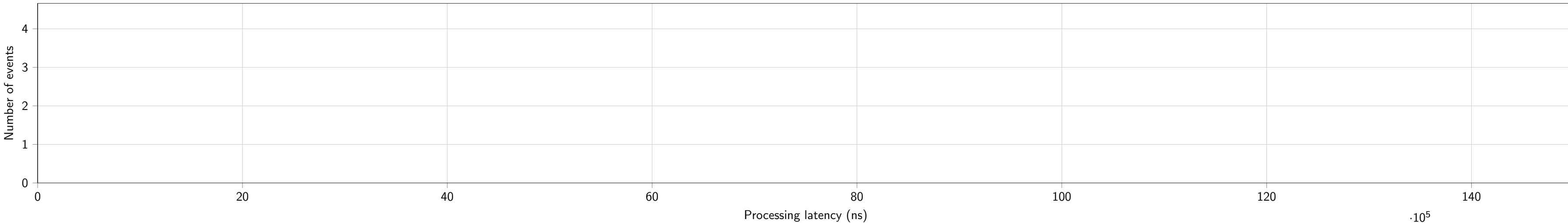
l2\_bridging\_cnf1\_mbit4361hires.histogram.csv: tx: 8.55mpps, 0.04stdDev; rx: 8.52mpps, 0.00stdDev



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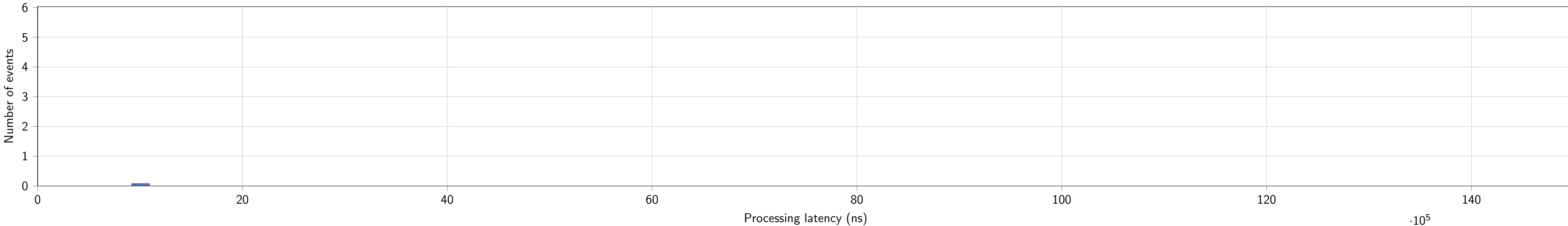


l2\_bridging\_cnf1\_mbit4381hires.histogram.csv: tx: 8.55mpps, 0.04stdDev; rx: 8.44mpps, 0.00stdDev

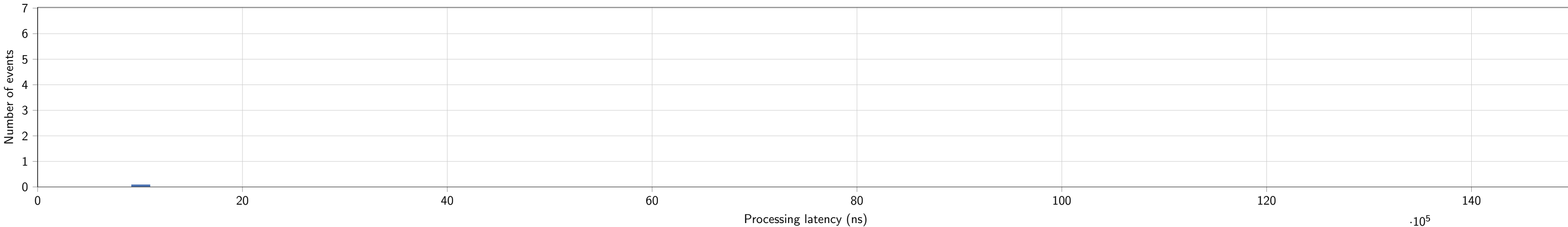




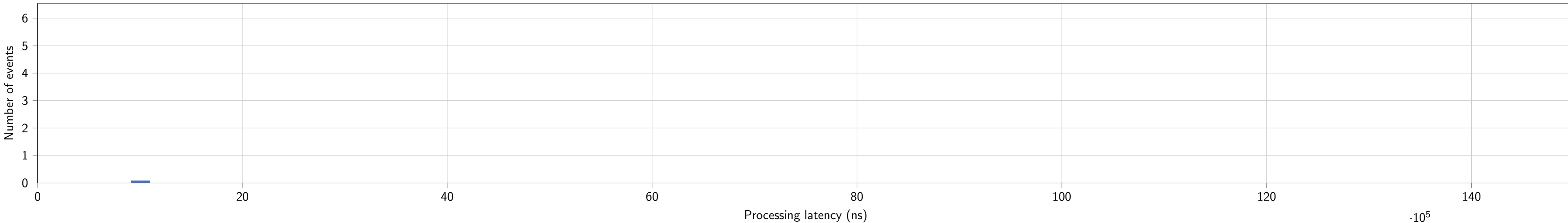
l2\_bridging\_cnf1\_mbit4391hires.histogram.csv: tx: 8.61mpps, 0.04stdDev; rx: 8.50mpps, 0.00stdDev



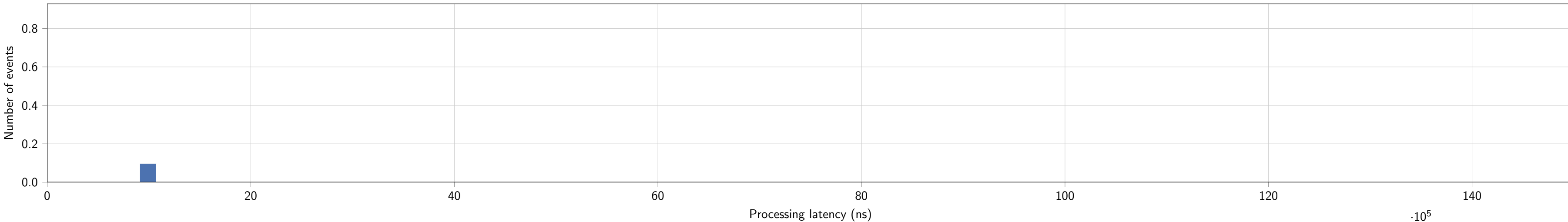
l2\_bridging\_cnf1\_mbit4400.histogram.csv: tx: 8.61mpps, 0.05stdDev; rx: 8.53mpps, 0.00stdDev



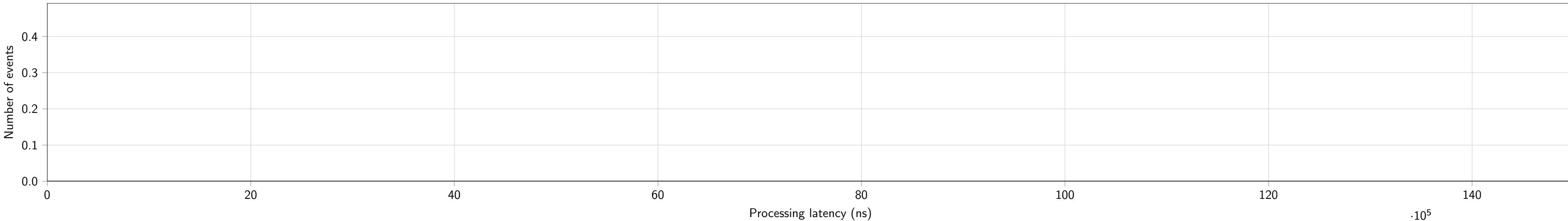
l2\_bridging\_cnf1\_mbit4401hires.histogram.csv: tx: 8.61mpps, 0.04stdDev; rx: 8.52mpps, 0.00stdDev



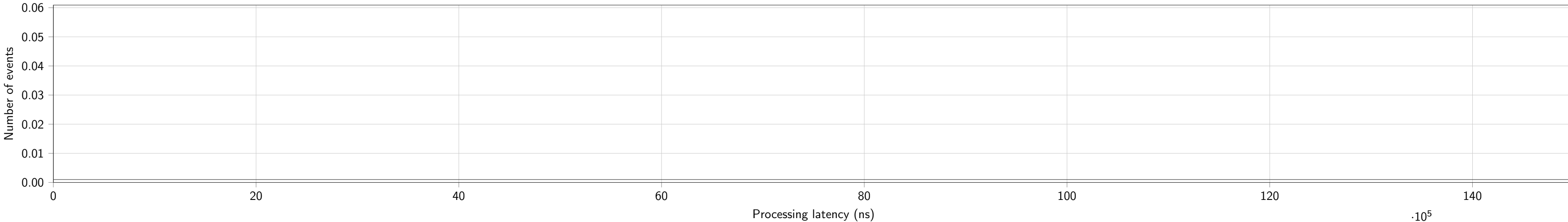
l2\_bridging\_cnf1\_mbit4800.histogram.csv: tx: 9.39mpps, 0.05stdDev; rx: 8.51mpps, 0.00stdDev



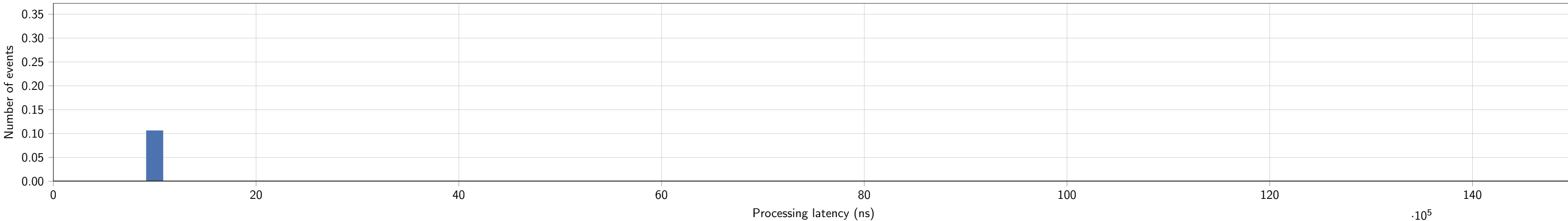
l2\_bridging\_cnf1\_mbit5200.histogram.csv: tx: 10.15mpps, 0.05stdDev; rx: 8.50mpps, 0.04stdDev



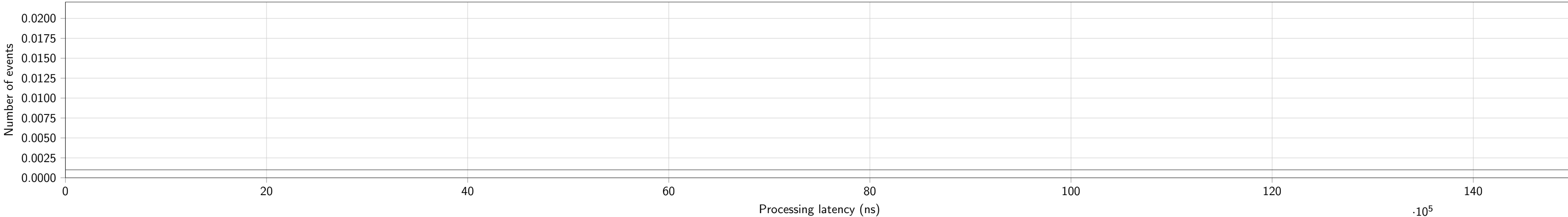
l2\_bridging\_cnf1\_mbit5600.histogram.csv: tx: 10.95mpps, 0.05stdDev; rx: 8.50mpps, 0.00stdDev



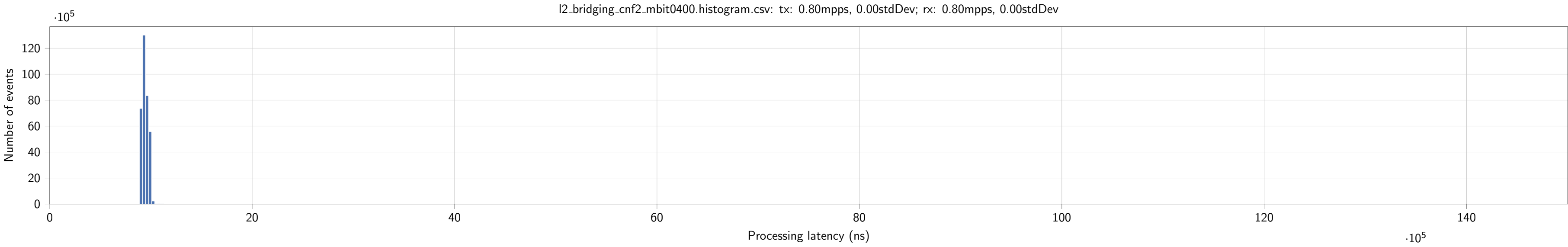
l2\_bridging\_cnf1\_mbit6000.histogram.csv: tx: 11.78mpps, 0.06stdDev; rx: 8.48mpps, 0.00stdDev

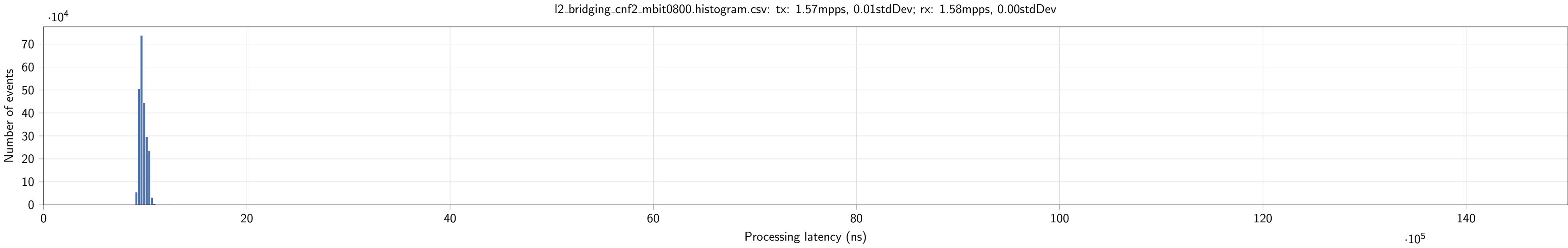


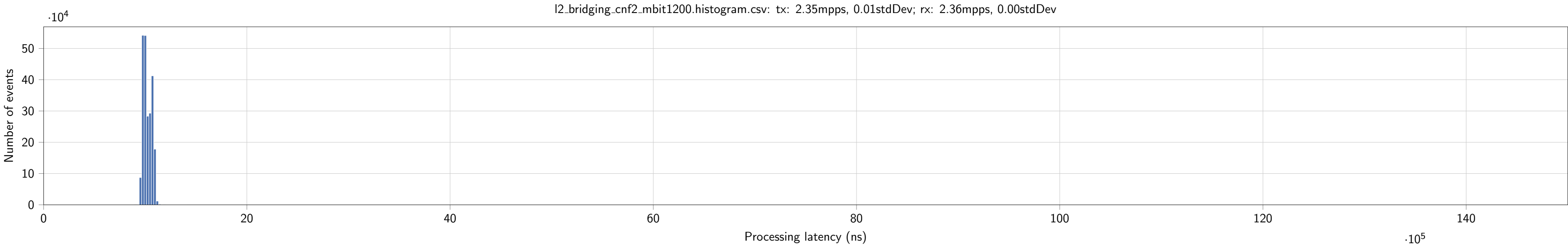
l2\_bridging\_cnf1\_mbit9000.histogram.csv: tx: 14.86mpps, 0.07stdDev; rx: 8.50mpps, 0.00stdDev

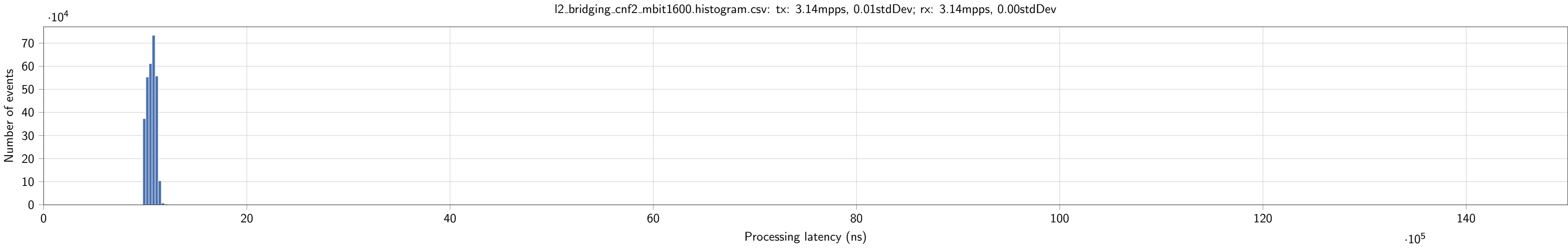




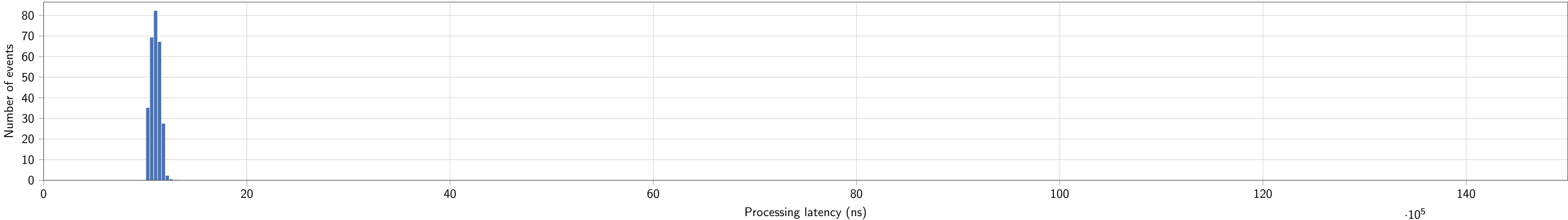


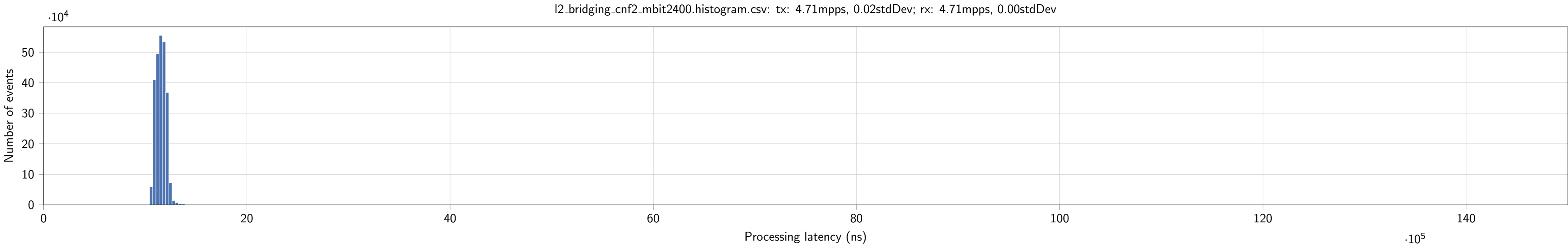




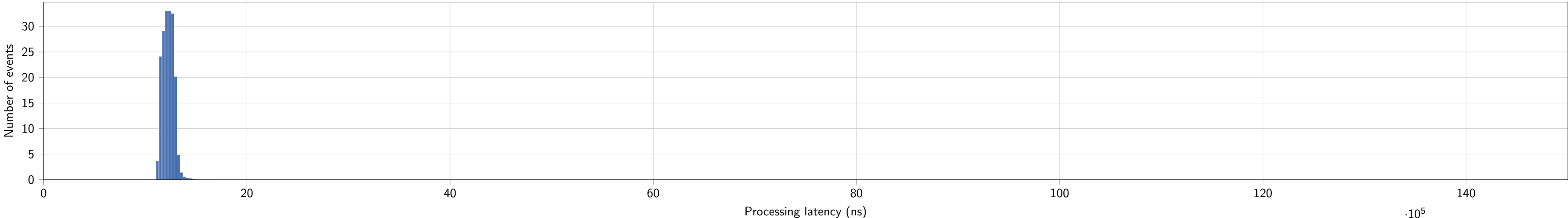


l2\_bridging\_cnf2\_mbit2000.histogram.csv: tx: 3.92mpps, 0.02stdDev; rx: 3.92mpps, 0.00stdDev

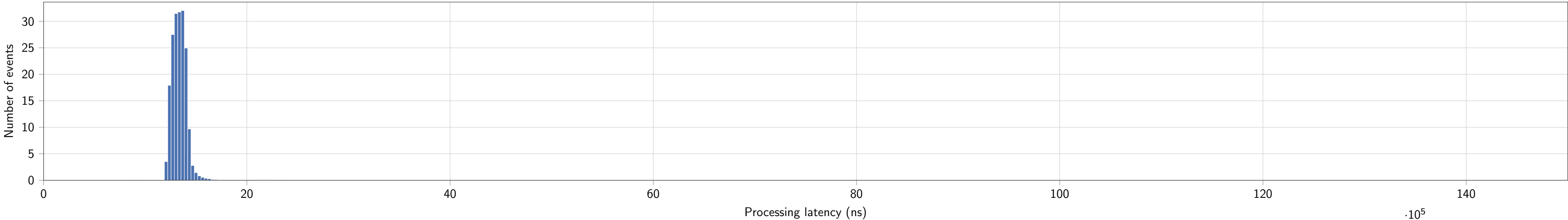




l2\_bridging\_cnf2\_mbit2800.histogram.csv: tx: 5.49mpps, 0.03stdDev; rx: 5.49mpps, 0.00stdDev



l2\_bridging\_cnf2\_mbit3200.histogram.csv: tx: 6.25mpps, 0.03stdDev; rx: 6.26mpps, 0.00stdDev





l2\_bridging\_cnf2\_mbit3600.histogram.csv: tx: 7.06mpps, 0.04stdDev; rx: 7.07mpps, 0.00stdDev

Number of events

30  
25  
20  
15  
10  
5  
0

$\cdot 10^4$

20

40

60

80

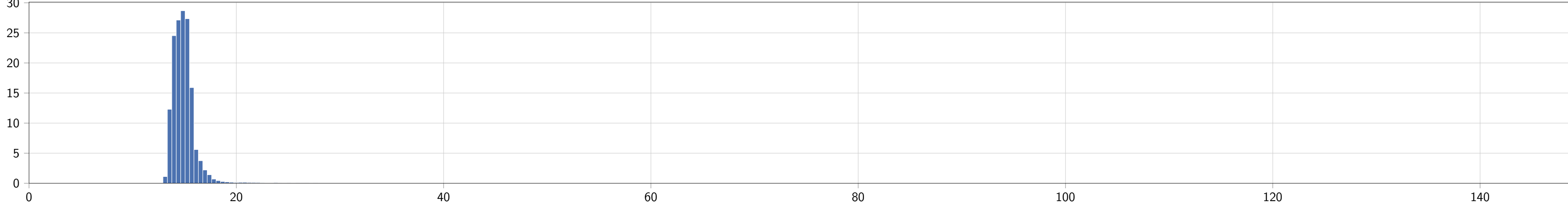
100

120

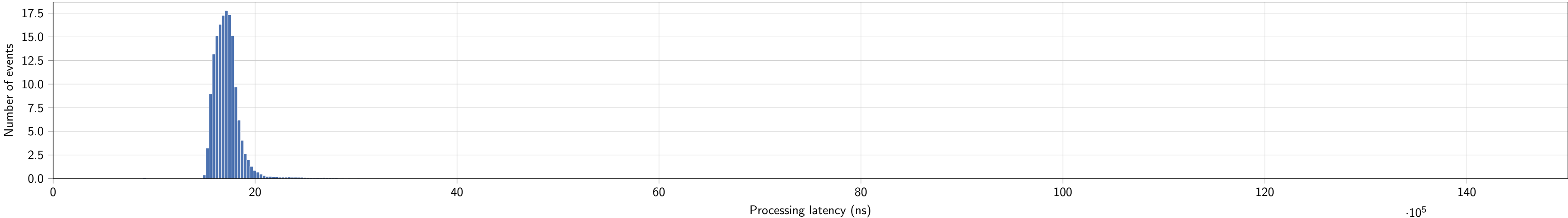
140

Processing latency (ns)

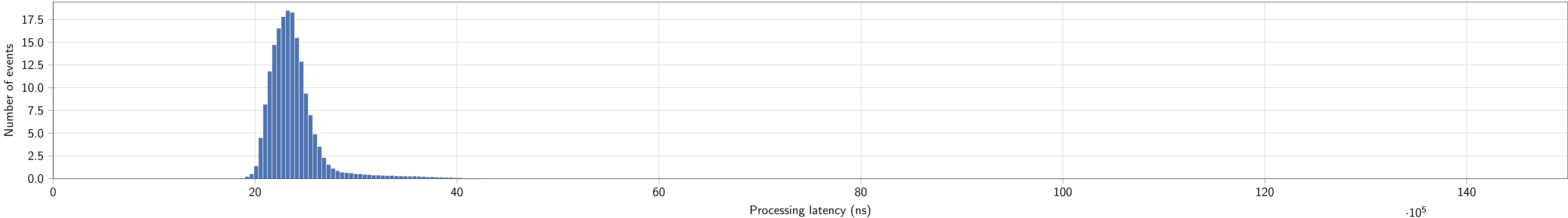
$\cdot 10^5$



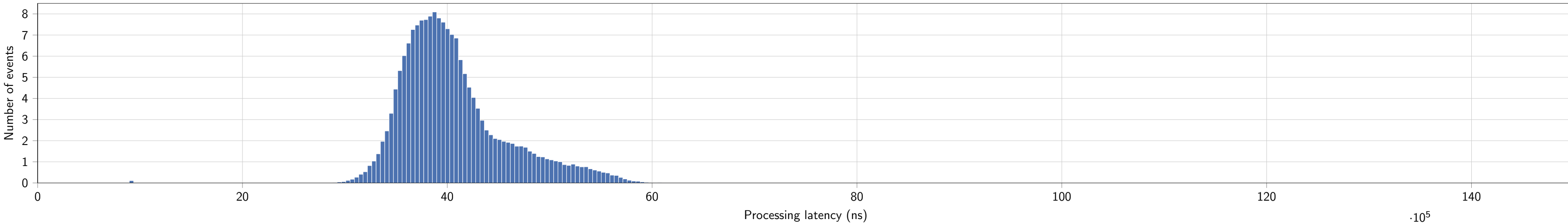
l2\_bridging\_cnf2\_mbit4000.histogram.csv: tx: 7.81mpps, 0.04stdDev; rx: 7.82mpps, 0.00stdDev



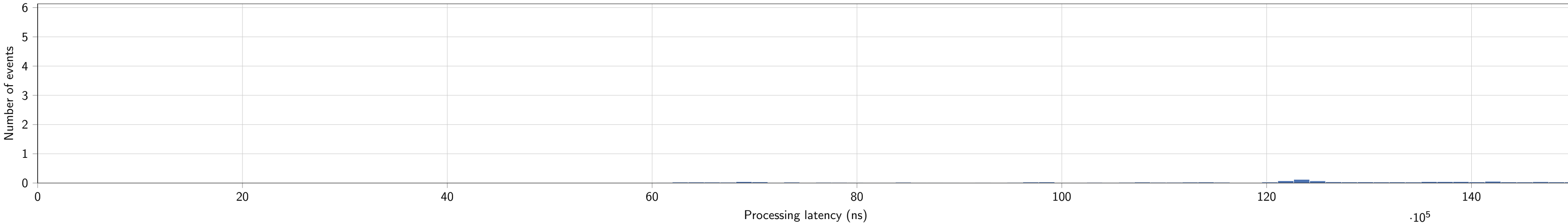
l2\_bridging\_cnf2\_mbit4400.histogram.csv: tx: 8.62mpps, 0.04stdDev; rx: 8.63mpps, 0.00stdDev

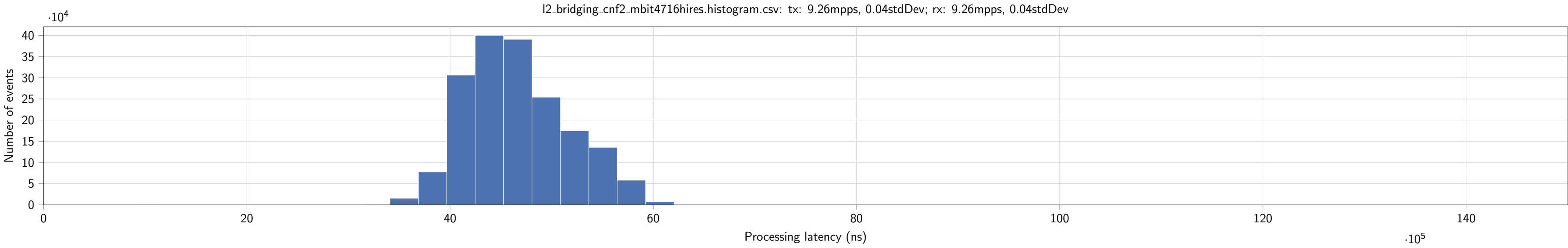


l2\_bridging\_cnf2\_mbit4696\_final.histogram.csv: tx: 9.19mpps, 0.04stdDev; rx: 9.20mpps, 0.00stdDev

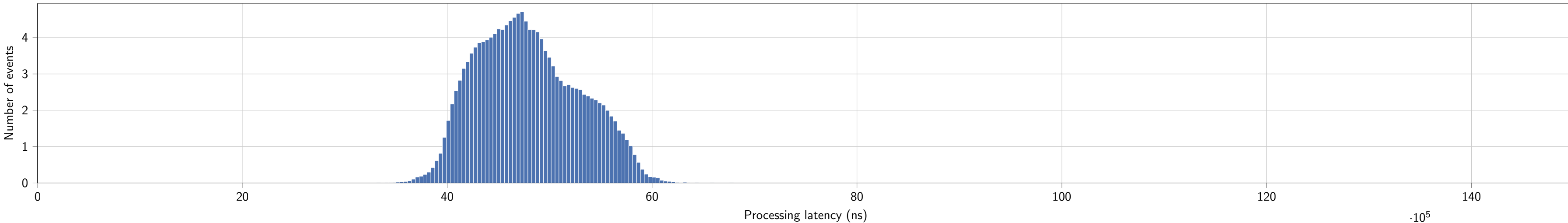


l2\_bridging\_cnf2\_mbit4706hires.histogram.csv: tx: 9.25mpps, 0.04stdDev; rx: 9.25mpps, 0.00stdDev

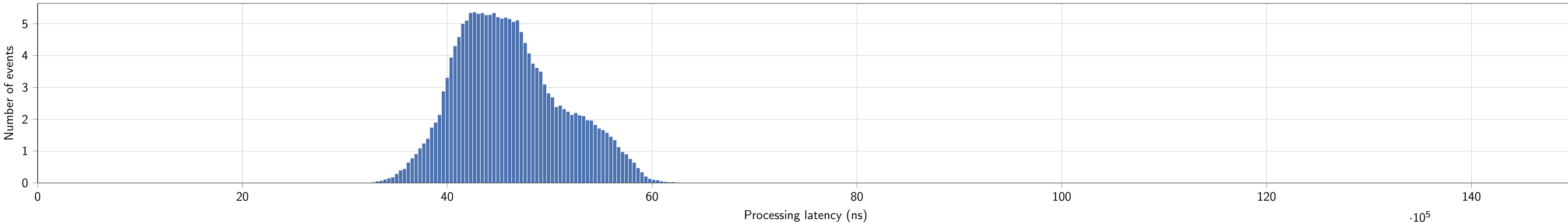




l2\_bridging\_cnf2\_mbit4726hires.histogram.csv: tx: 9.26mpps, 0.05stdDev; rx: 9.27mpps, 0.00stdDev

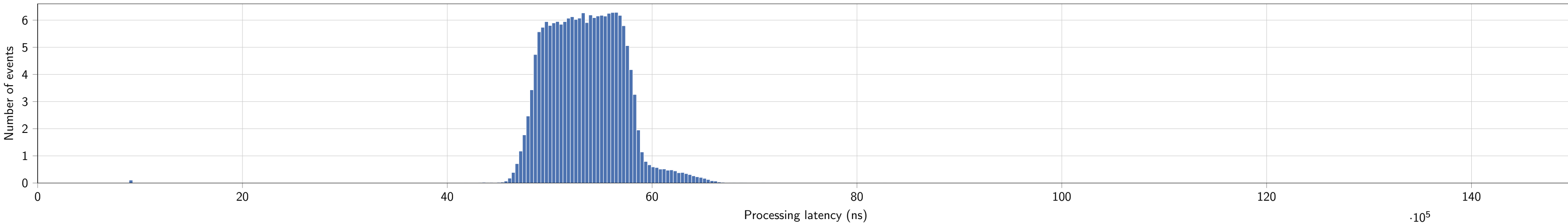


l2\_bridging\_cnf2\_mbit4736hires.histogram.csv: tx: 9.26mpps, 0.04stdDev; rx: 9.27mpps, 0.00stdDev

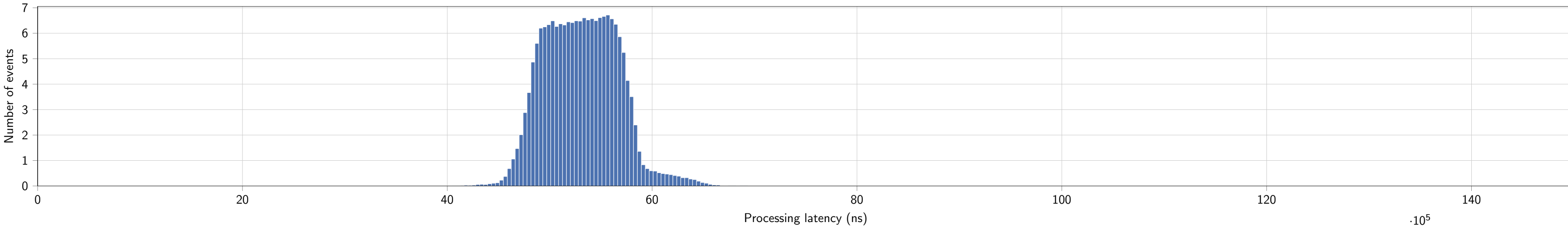




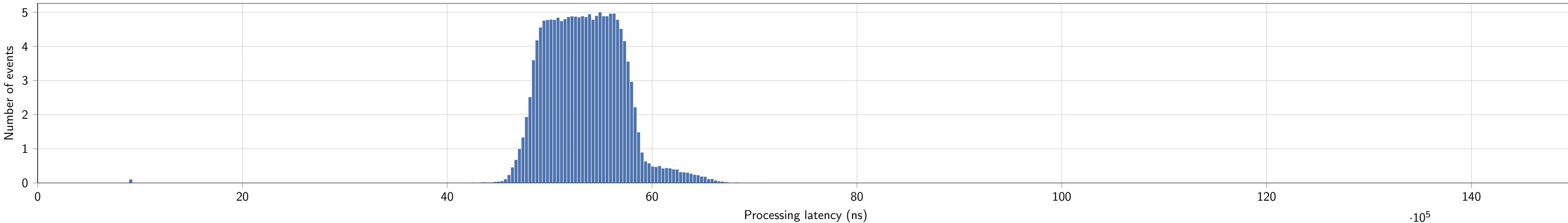
l2\_bridging\_cnf2\_mbit4746hires.histogram.csv: tx: 9.33mpps, 0.04stdDev; rx: 9.34mpps, 0.00stdDev



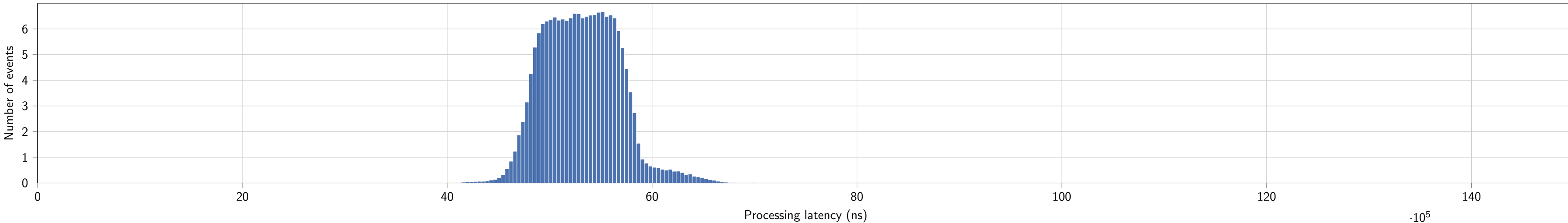
l2\_bridging\_cnf2\_mbit4756hires.histogram.csv: tx: 9.33mpps, 0.04stdDev; rx: 9.34mpps, 0.00stdDev



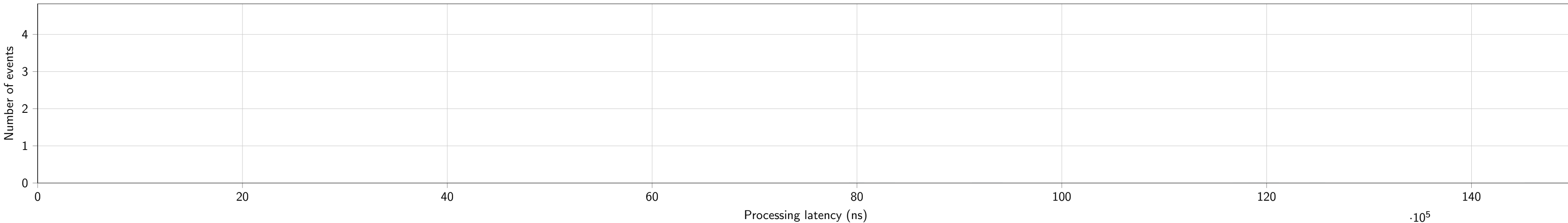
l2\_bridging\_cnf2\_mbit4766hires.histogram.csv: tx: 9.32mpps, 0.05stdDev; rx: 9.34mpps, 0.00stdDev



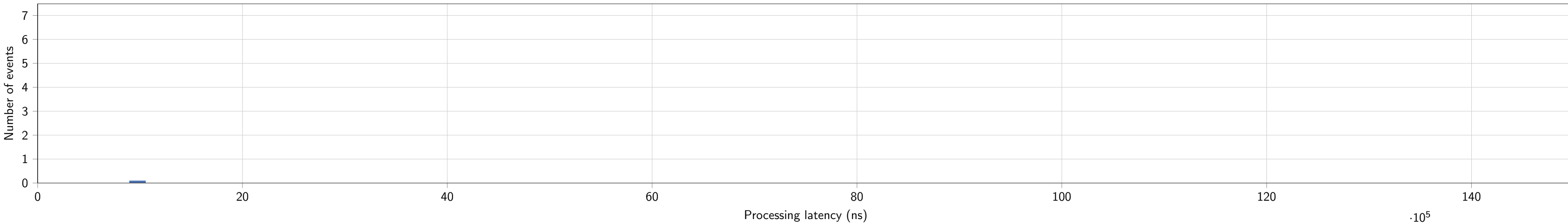
l2\_bridging\_cnf2\_mbit4776hires.histogram.csv: tx: 9.33mpps, 0.04stdDev; rx: 9.34mpps, 0.00stdDev



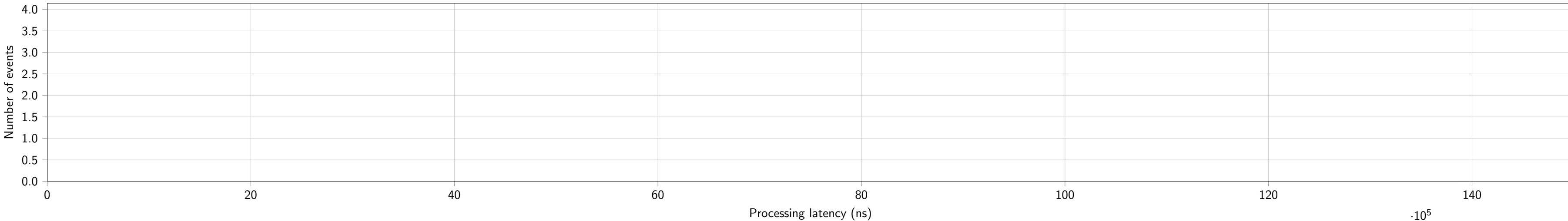
l2\_bridging\_cnf2\_mbit4786hires.histogram.csv: tx: 9.39mpps, 0.04stdDev; rx: 9.39mpps, 0.00stdDev



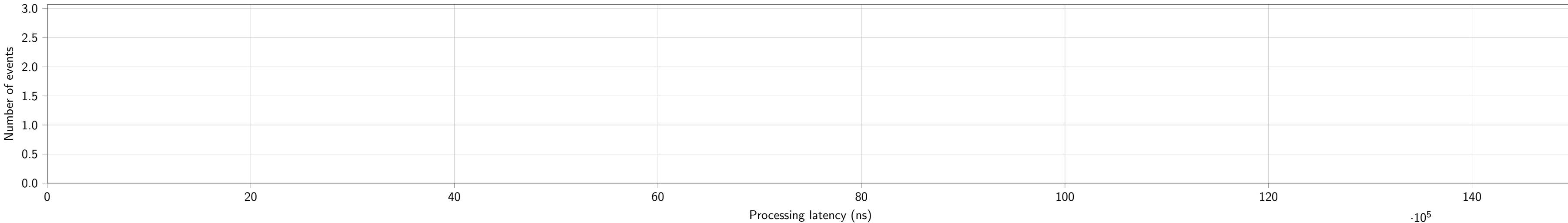
l2\_bridging\_cnf2\_mbit4796hires.histogram.csv: tx: 9.39mpps, 0.05stdDev; rx: 9.35mpps, 0.00stdDev



l2\_bridging\_cnf2\_mbit4800.histogram.csv: tx: 9.39mpps, 0.05stdDev; rx: 9.37mpps, 0.00stdDev

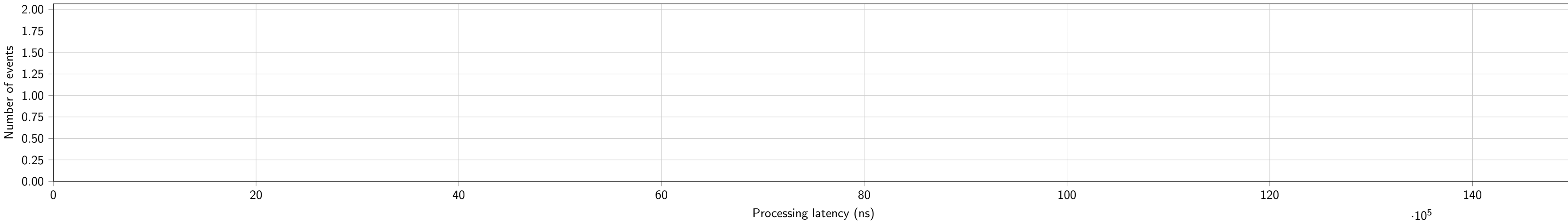


l2\_bridging\_cnf2\_mbit4806hires.histogram.csv: tx: 9.39mpps, 0.05stdDev; rx: 9.27mpps, 0.00stdDev

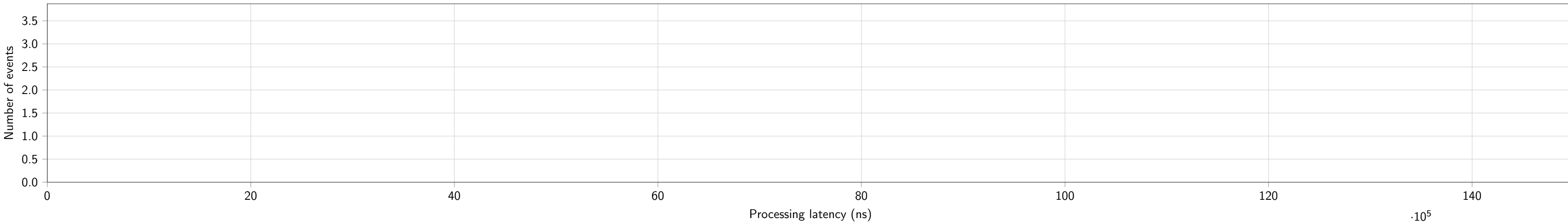




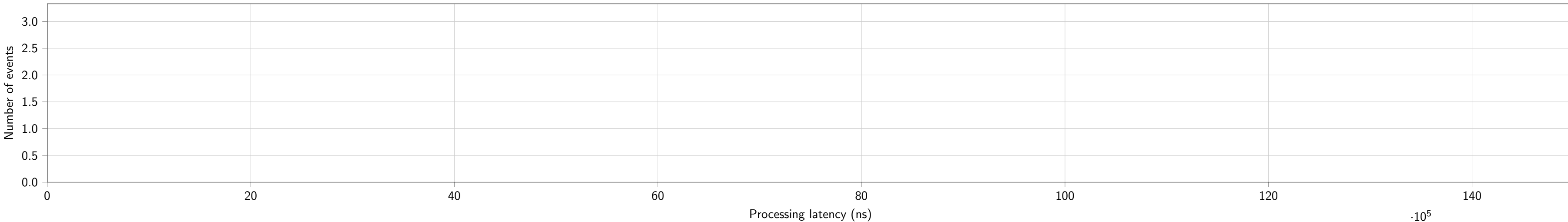
l2\_bridging\_cnf2\_mbit4816hires.histogram.csv: tx: 9.46mpps, 0.05stdDev; rx: 9.27mpps, 0.00stdDev



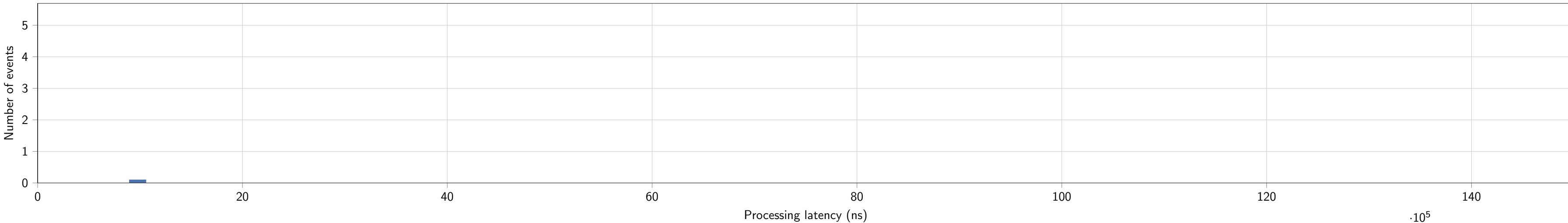
l2\_bridging\_cnf2\_mbit4826hires.histogram.csv: tx: 9.46mpps, 0.05stdDev; rx: 9.36mpps, 0.00stdDev



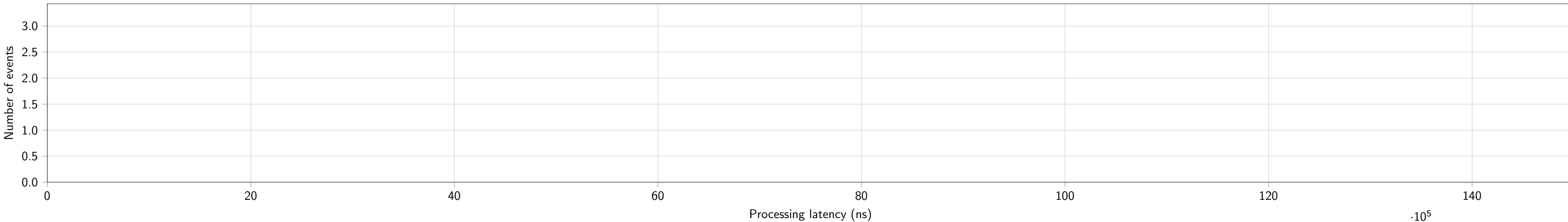
l2\_bridging\_cnf2\_mbit4836hires.histogram.csv: tx: 9.46mpps, 0.05stdDev; rx: 9.37mpps, 0.00stdDev



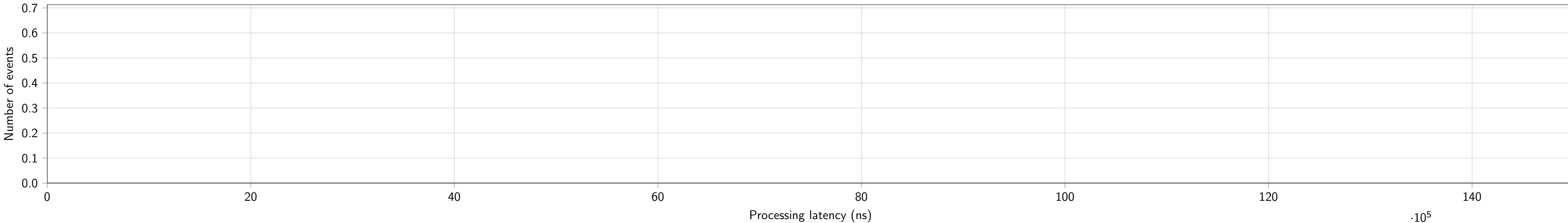
l2\_bridging\_cnf2\_mbit4846hires.histogram.csv: tx: 9.46mpps, 0.05stdDev; rx: 9.35mpps, 0.00stdDev



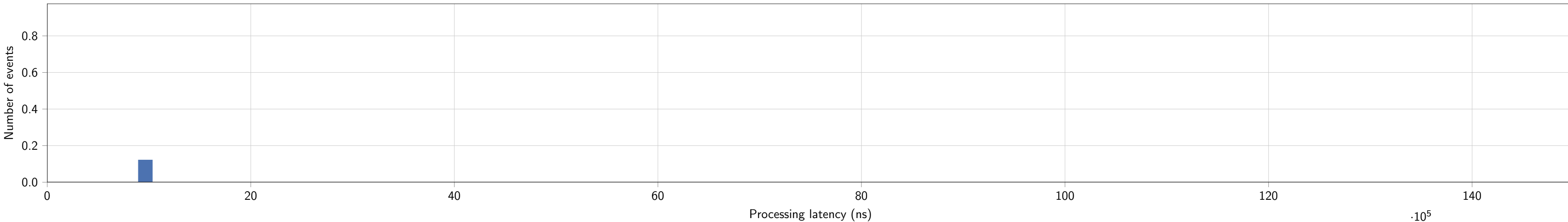
l2\_bridging\_cnf2\_mbit4856hires.histogram.csv: tx: 9.53mpps, 0.05stdDev; rx: 9.37mpps, 0.00stdDev



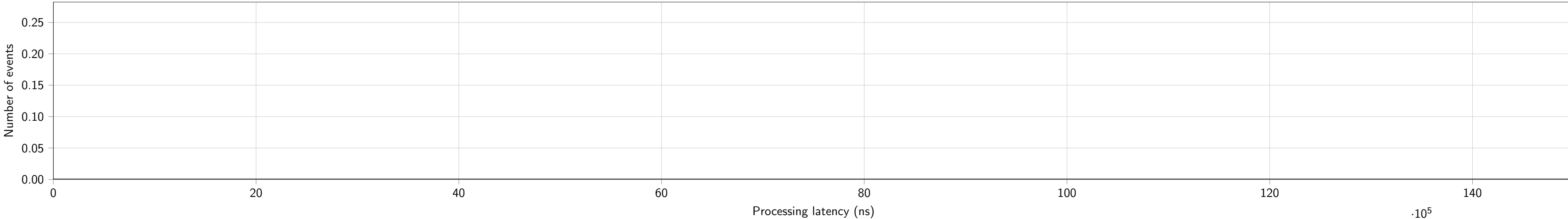
l2\_bridging\_cnf2\_mbit5200.histogram.csv: tx: 10.15mpps, 0.05stdDev; rx: 9.24mpps, 0.00stdDev



l2\_bridging\_cnf2\_mbit5600.histogram.csv: tx: 10.95mpps, 0.05stdDev; rx: 9.38mpps, 0.00stdDev

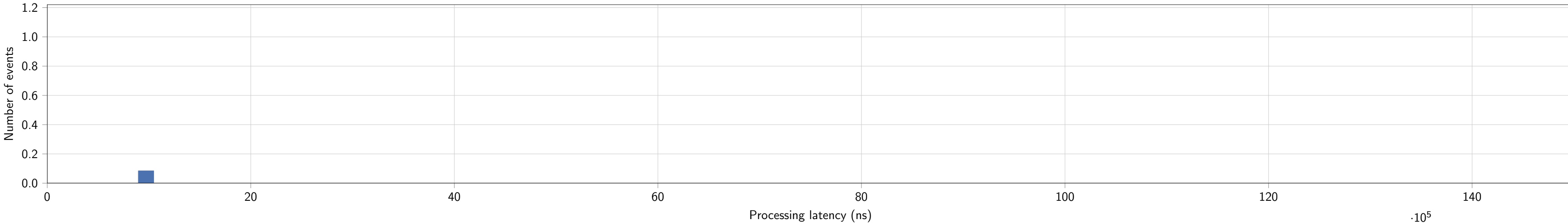


l2\_bridging\_cnf2\_mbit6000.histogram.csv: tx: 11.78mpps, 0.06stdDev; rx: 9.32mpps, 0.00stdDev

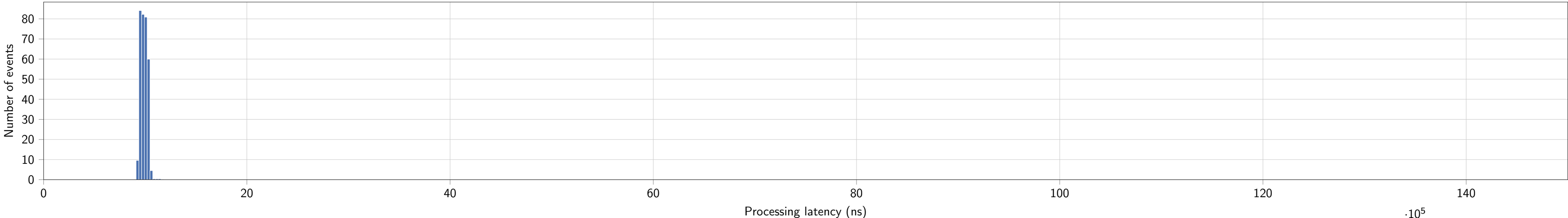




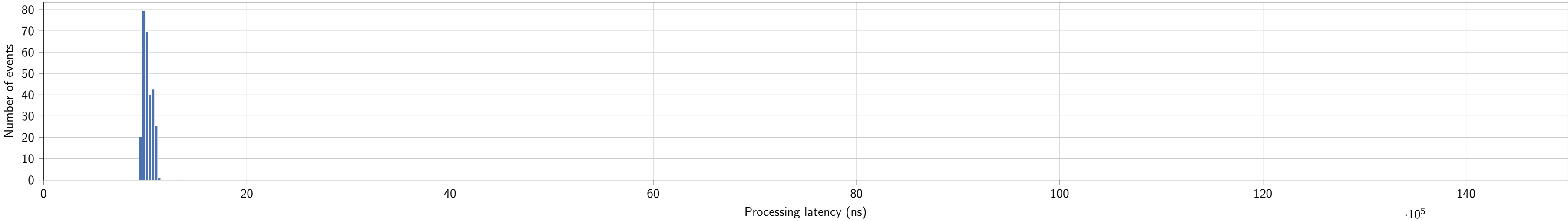
l2\_bridging\_cnf2\_mbit9000.histogram.csv: tx: 14.86mpps, 0.07stdDev; rx: 9.39mpps, 0.00stdDev

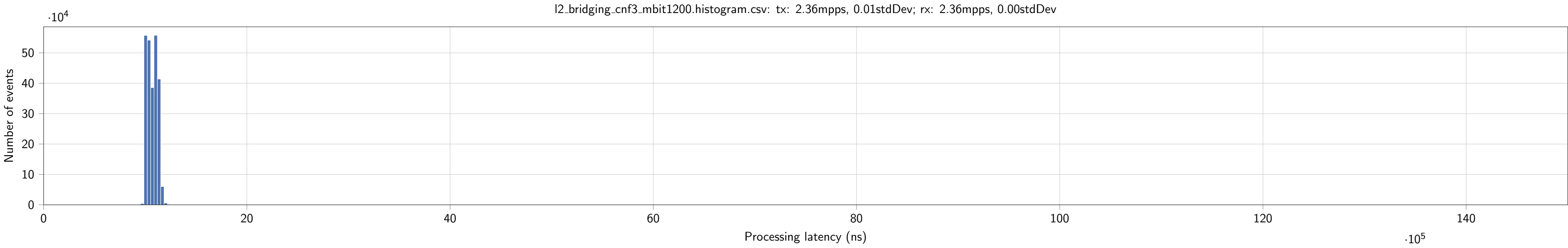


l2\_bridging\_cnf3\_mbit0400.histogram.csv: tx: 0.80mpps, 0.00stdDev; rx: 0.80mpps, 0.00stdDev

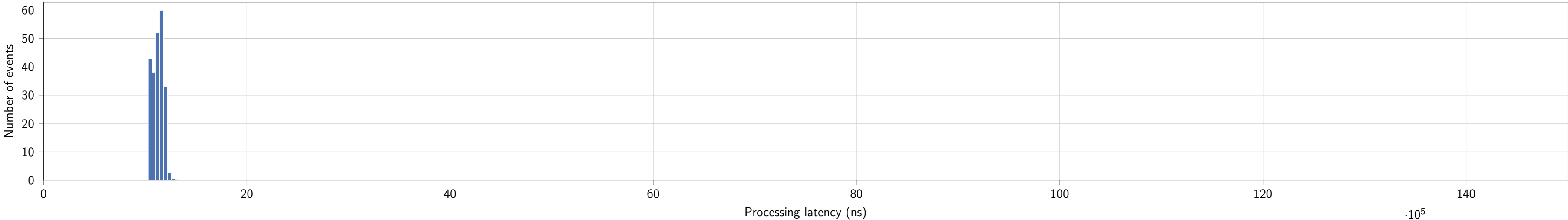


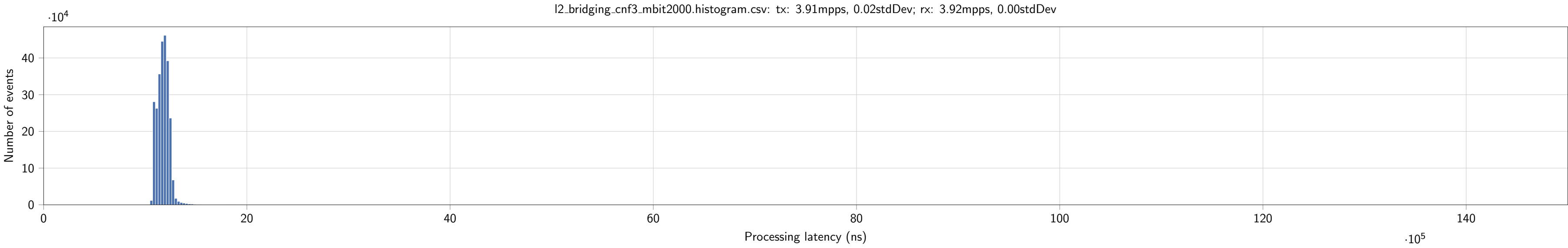
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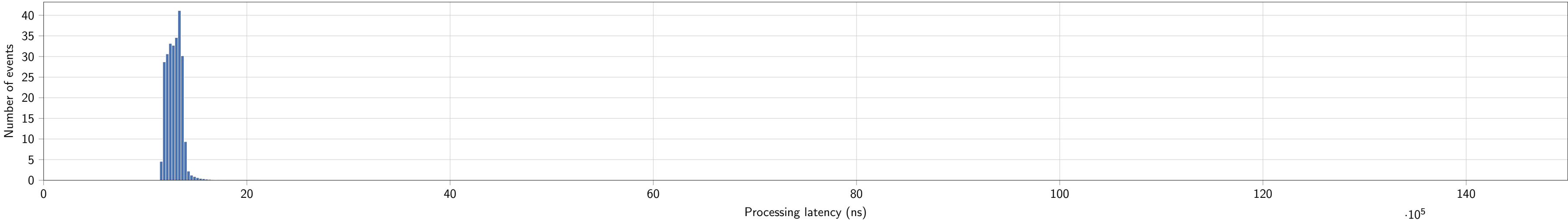


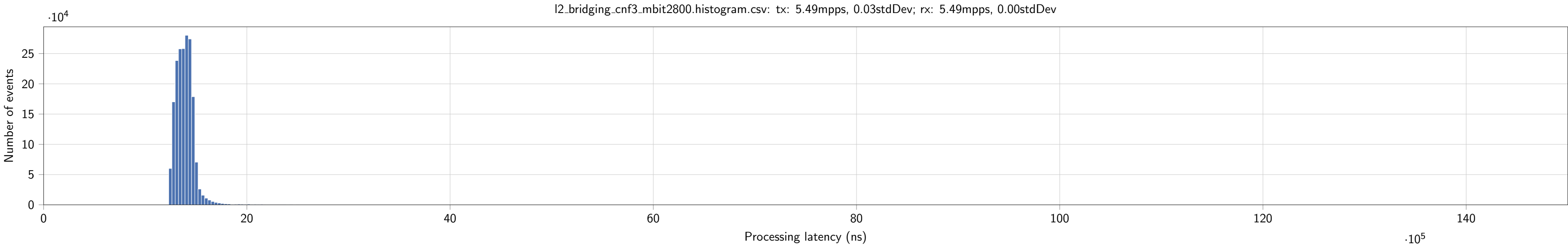
l2\_bridging\_cnf3\_mbit1600.histogram.csv: tx: 3.13mpps, 0.01stdDev; rx: 3.14mpps, 0.00stdDev



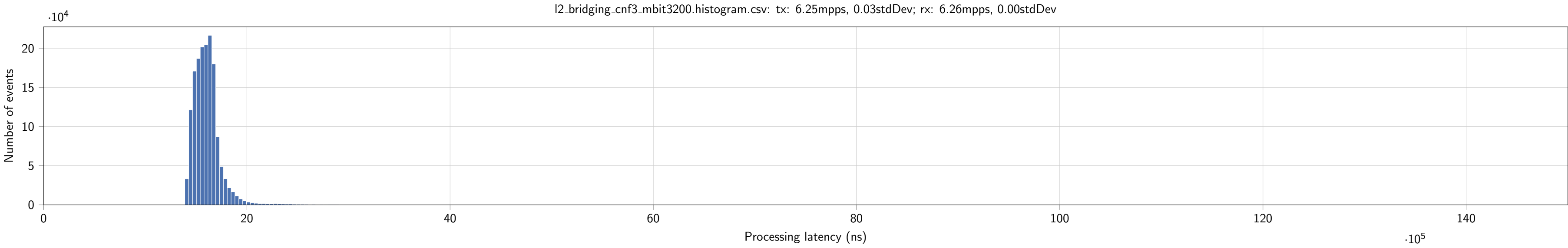


l2\_bridging\_cnf3\_mbit2400.histogram.csv: tx: 4.71mpps, 0.02stdDev; rx: 4.71mpps, 0.00stdDev

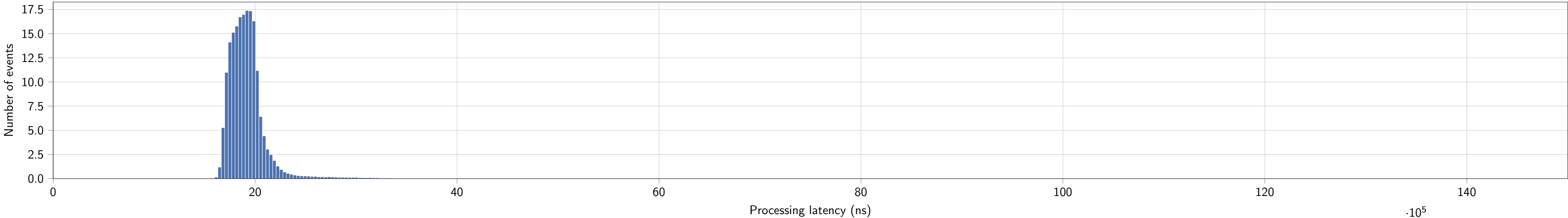




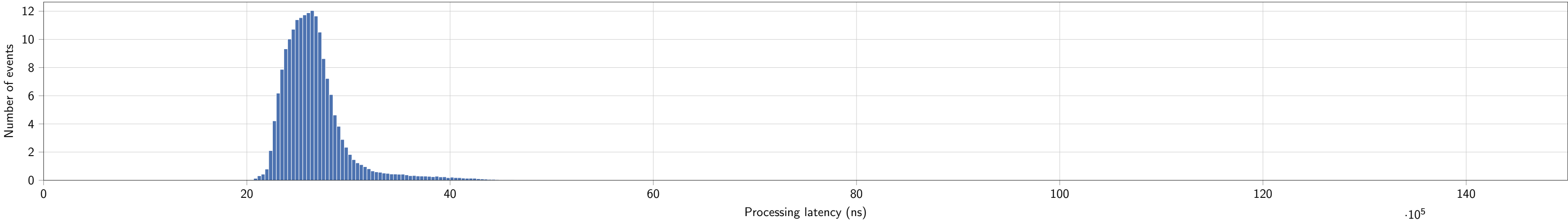




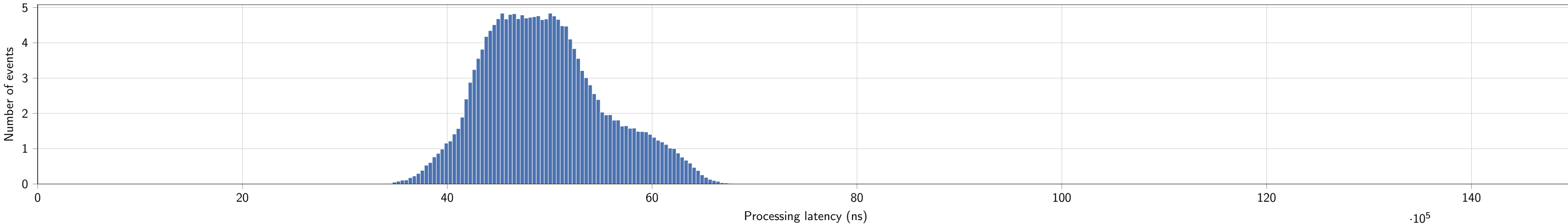
l2\_bridging\_cnf3\_mbit3600.histogram.csv: tx: 7.06mpps, 0.03stdDev; rx: 7.07mpps, 0.00stdDev



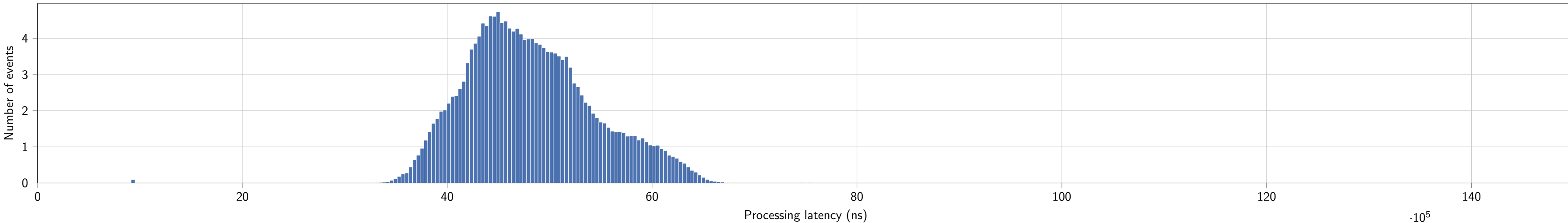
l2\_bridging\_cnf3\_mbit4000.histogram.csv: tx: 7.81mpps, 0.04stdDev; rx: 7.82mpps, 0.00stdDev



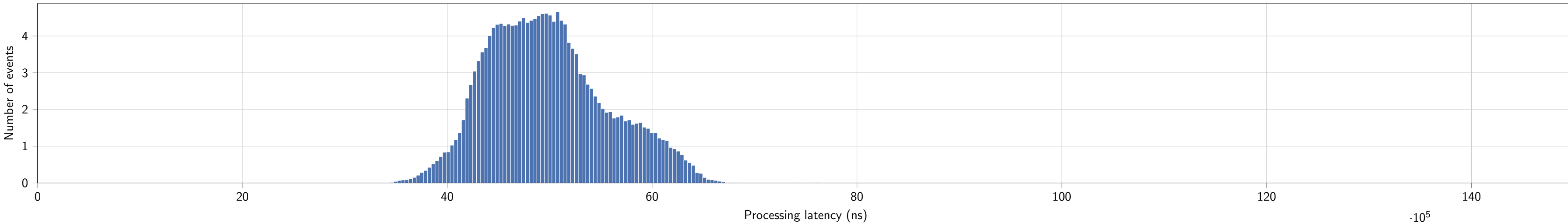
l2\_bridging\_cnf3\_mbit4256hires.histogram.csv: tx: 8.33mpps, 0.04stdDev; rx: 8.34mpps, 0.00stdDev



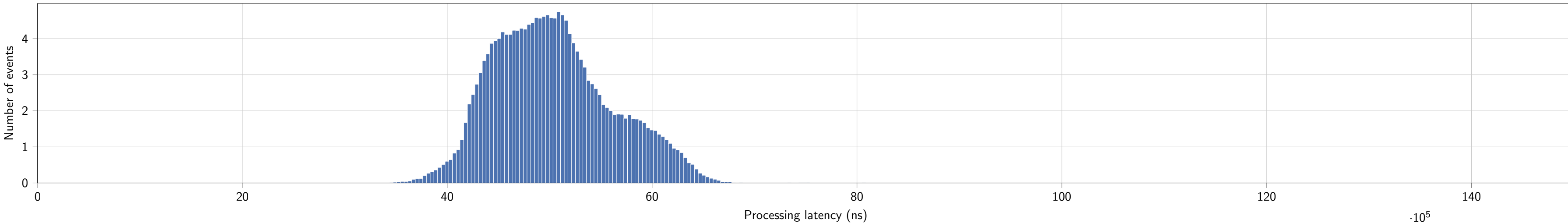
l2\_bridging\_cnf3\_mbit4266hires.histogram.csv: tx: 8.33mpps, 0.04stdDev; rx: 8.34mpps, 0.00stdDev



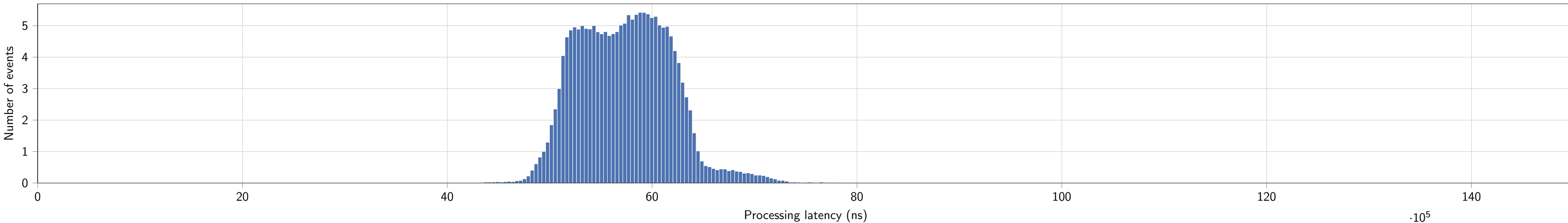
l2\_bridging\_cnf3\_mbit4276hires.histogram.csv: tx: 8.39mpps, 0.04stdDev; rx: 8.40mpps, 0.00stdDev



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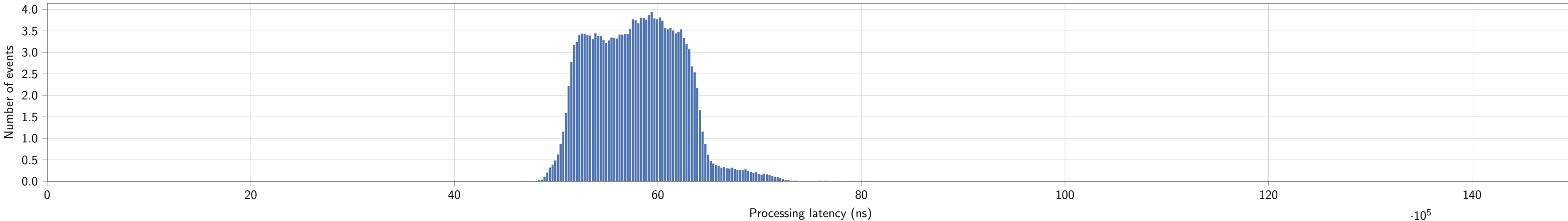


l2\_bridging\_cnf3\_mbit4296hires.histogram.csv: tx: 8.45mpps, 0.04stdDev; rx: 8.46mpps, 0.00stdDev

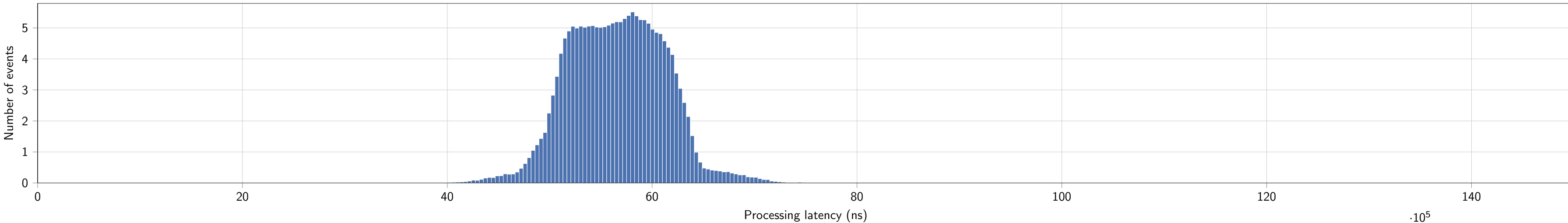




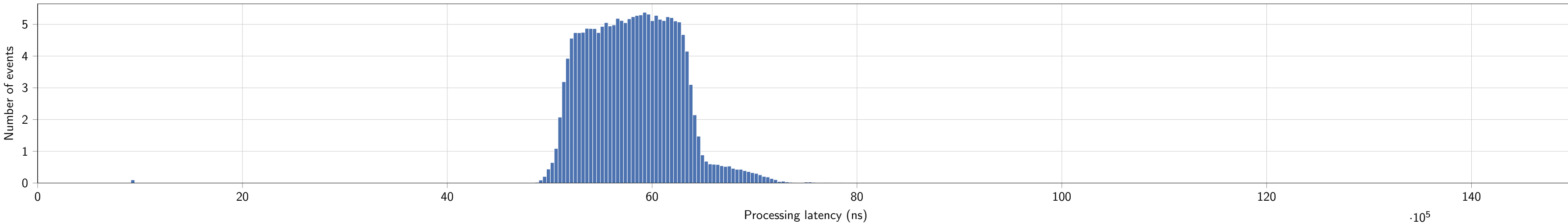
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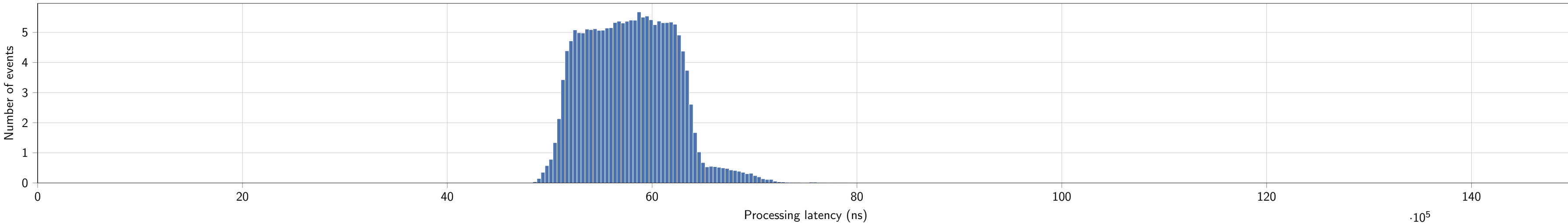
l2\_bridging\_cnf3\_mbit4316hires.histogram.csv: tx: 8.45mpps, 0.04stdDev; rx: 8.46mpps, 0.00stdDev



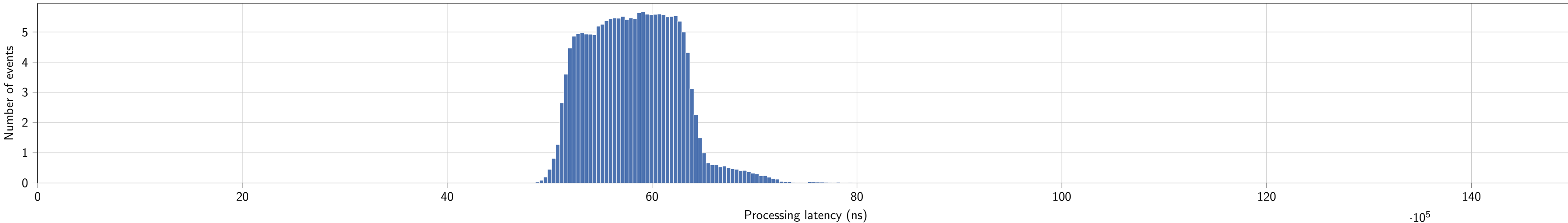
l2\_bridging\_cnf3\_mbit4326hires.histogram.csv: tx: 8.50mpps, 0.04stdDev; rx: 8.51mpps, 0.00stdDev



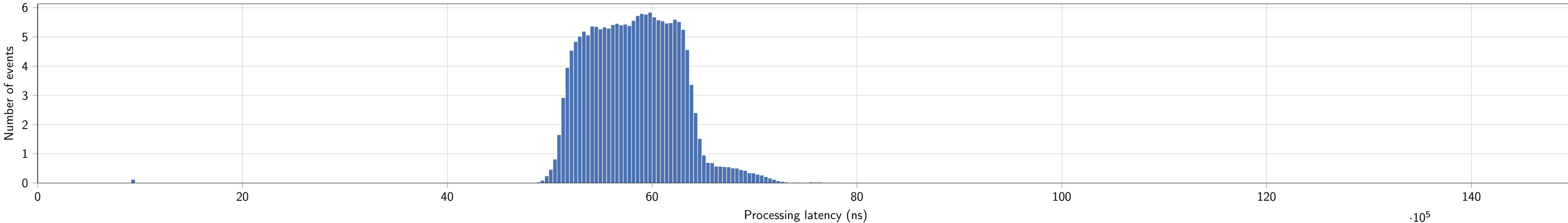
l2\_bridging\_cnf3\_mbit4336hires.histogram.csv: tx: 8.50mpps, 0.04stdDev; rx: 8.51mpps, 0.00stdDev



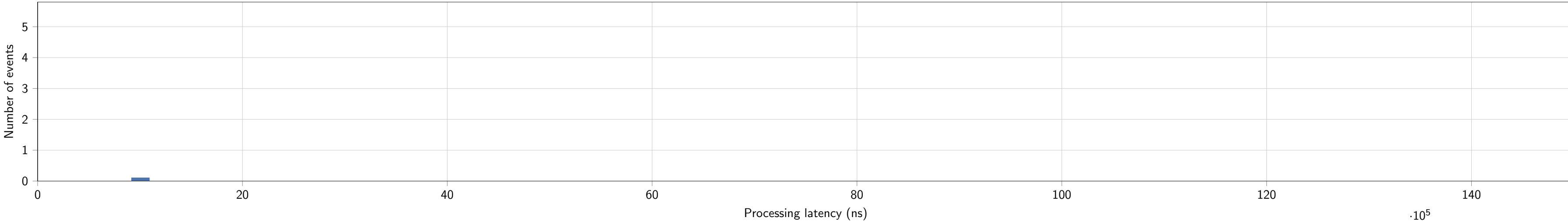
l2\_bridging\_cnf3\_mbit4346\_final.histogram.csv: tx: 8.50mpps, 0.04stdDev; rx: 8.51mpps, 0.00stdDev



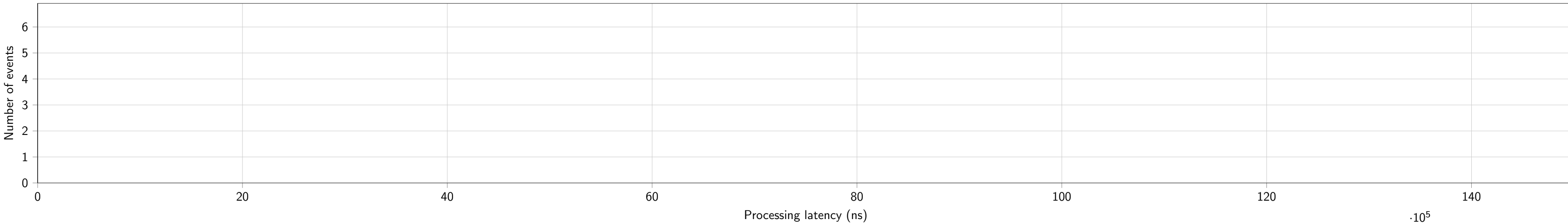
l2\_bridging\_cnf3\_mbit4346hires.histogram.csv: tx: 8.50mpps, 0.04stdDev; rx: 8.51mpps, 0.00stdDev



l2\_bridging\_cnf3\_mbit4356hires.histogram.csv: tx: 8.55mpps, 0.04stdDev; rx: 7.80mpps, 0.00stdDev

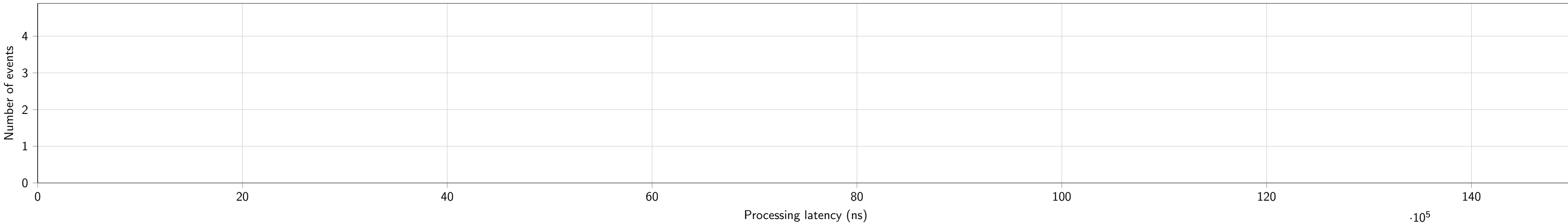


l2\_bridging\_cnf3\_mbit4366hires.histogram.csv: tx: 8.55mpps, 0.04stdDev; rx: 8.52mpps, 0.00stdDev

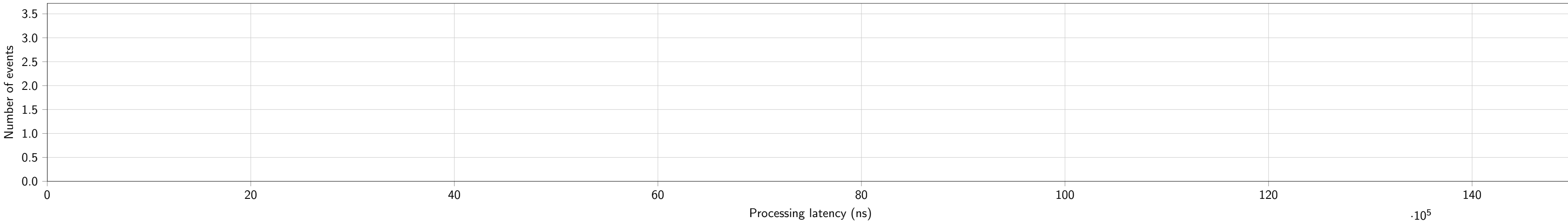




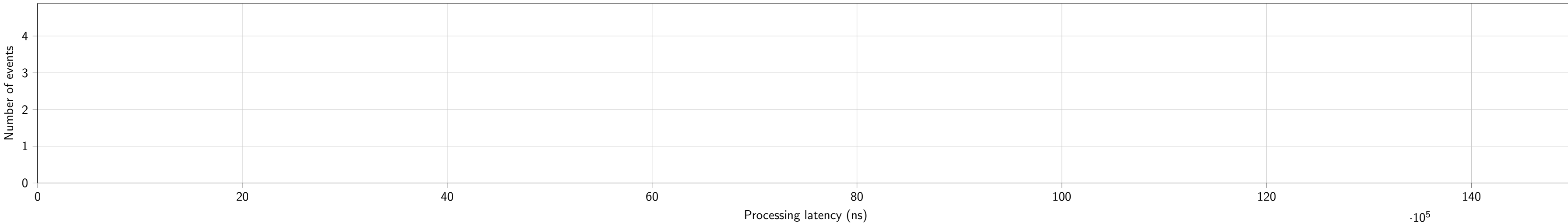
l2\_bridging\_cnf3\_mbit4376hires.histogram.csv: tx: 8.55mpps, 0.04stdDev; rx: 8.49mpps, 0.00stdDev



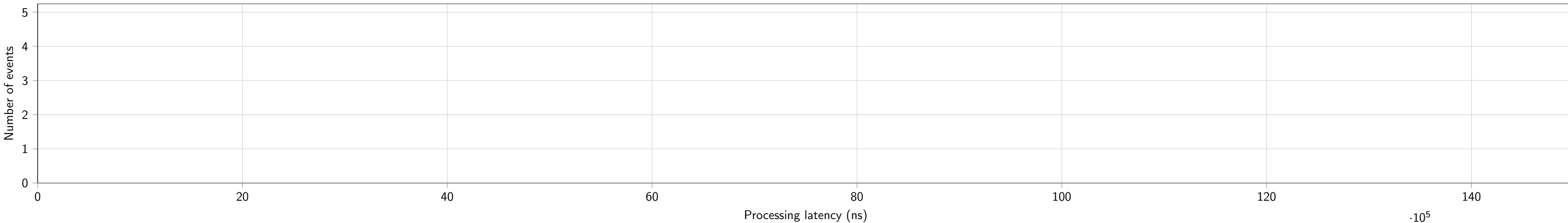
l2\_bridging\_cnf3\_mbit4386hires.histogram.csv: tx: 8.61mpps, 0.04stdDev; rx: 8.49mpps, 0.00stdDev



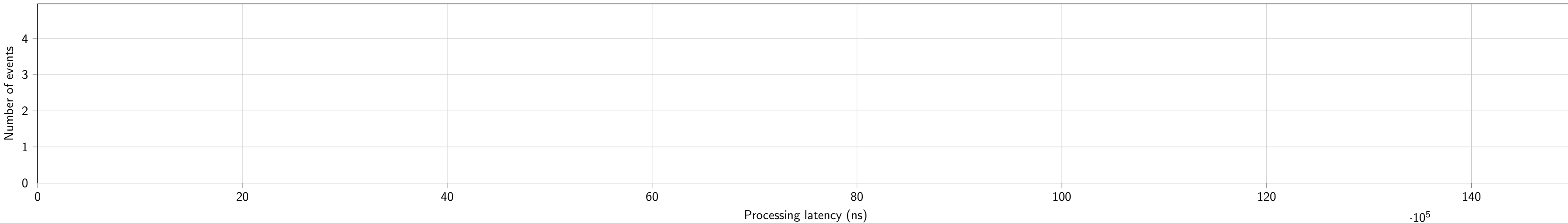
l2\_bridging\_cnf3\_mbit4396hires.histogram.csv: tx: 8.61mpps, 0.04stdDev; rx: 8.49mpps, 0.04stdDev



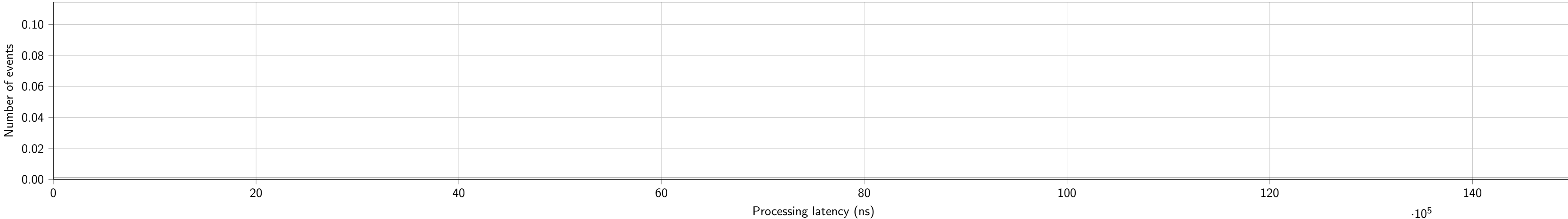
l2\_bridging\_cnf3\_mbit4400.histogram.csv: tx: 8.61mpps, 0.04stdDev; rx: 8.53mpps, 0.00stdDev



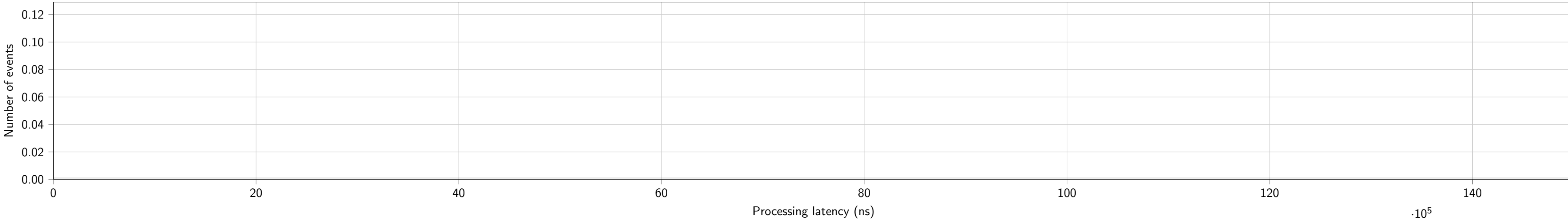
l2\_bridging\_cnf3\_mbit4406hires.histogram.csv: tx: 8.61mpps, 0.04stdDev; rx: 8.49mpps, 0.00stdDev



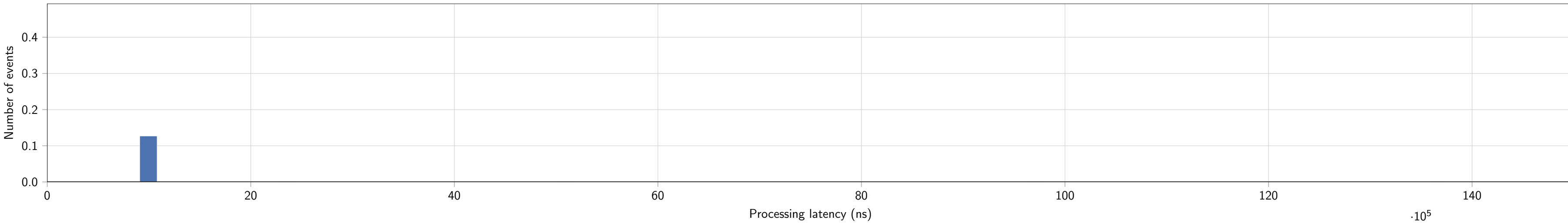
l2\_bridging\_cnf3\_mbit4800.histogram.csv: tx: 9.39mpps, 0.05stdDev; rx: 8.51mpps, 0.00stdDev



l2\_bridging\_cnf3\_mbit5200.histogram.csv: tx: 10.15mpps, 0.05stdDev; rx: 8.51mpps, 0.00stdDev

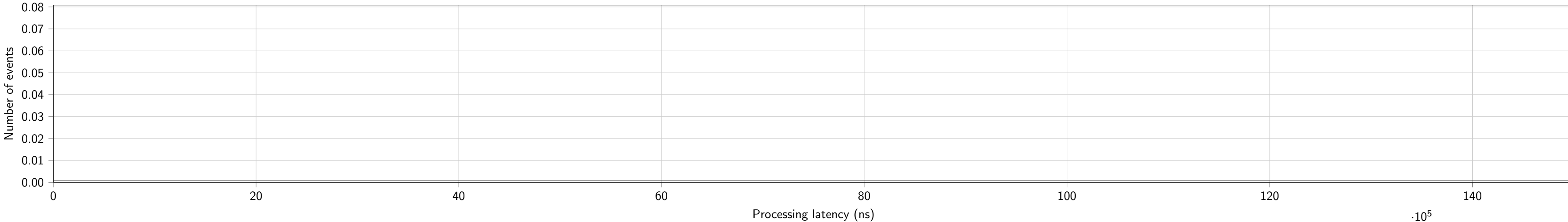


l2\_bridging\_cnf3\_mbit5600.histogram.csv: tx: 10.95mpps, 0.05stdDev; rx: 8.53mpps, 0.00stdDev

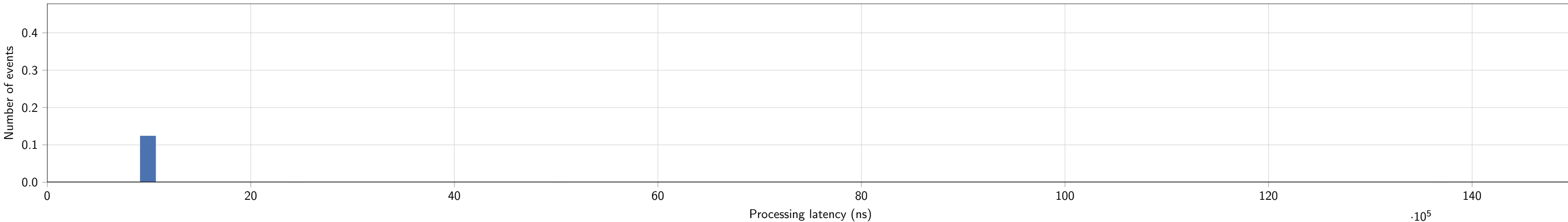


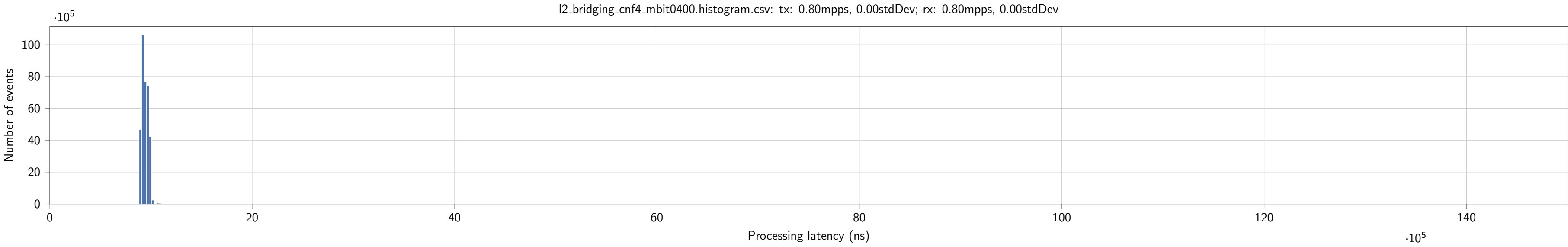


l2\_bridging\_cnf3\_mbit6000.histogram.csv: tx: 11.78mpps, 0.06stdDev; rx: 8.53mpps, 0.00stdDev

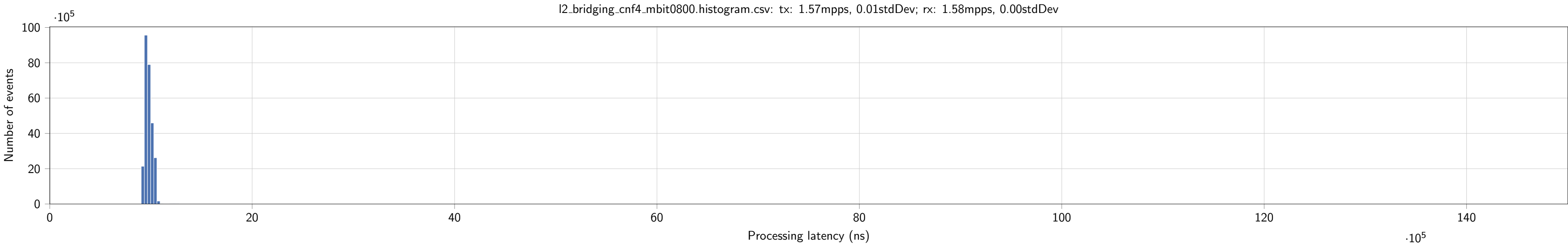


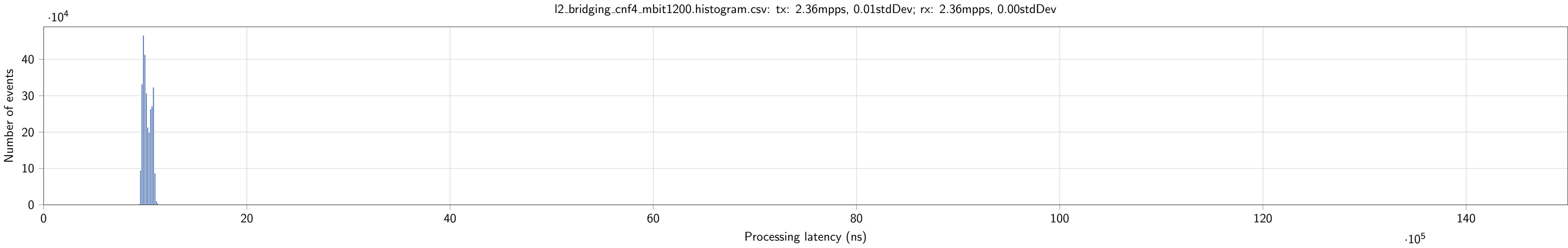
l2\_bridging\_cnf3\_mbit9000.histogram.csv: tx: 14.86mpps, 0.07stdDev; rx: 8.51mpps, 0.00stdDev



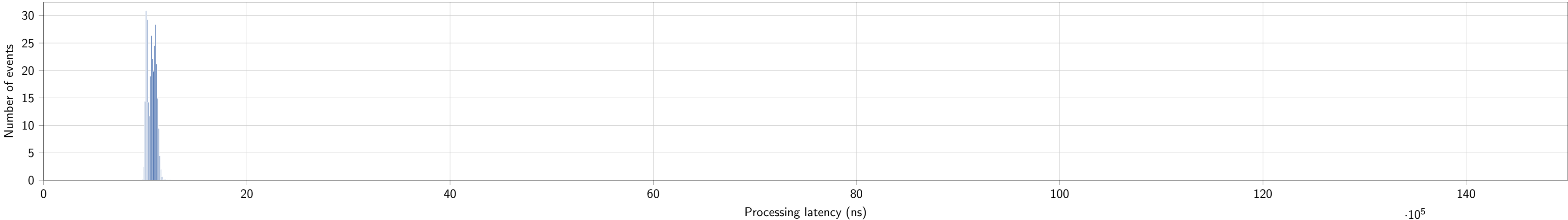


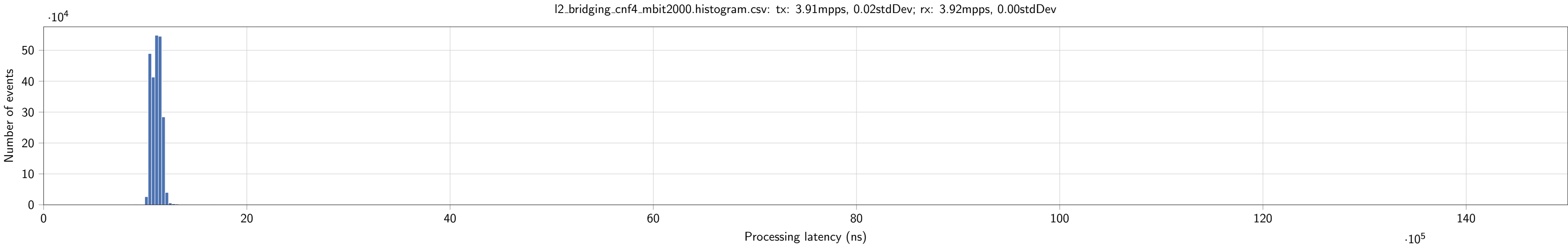
l2\_bridging\_cnf4\_mbit0800.histogram.csv: tx: 1.57mpps, 0.01stdDev; rx: 1.58mpps, 0.00stdDev

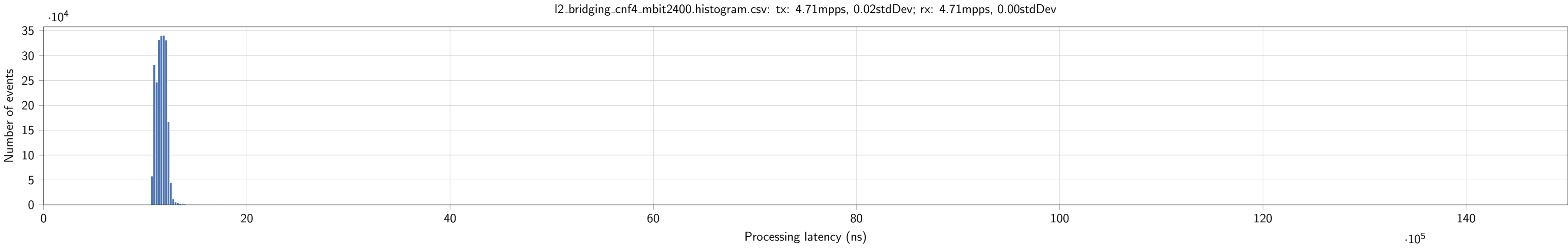




l2\_bridging\_cnf4\_mbit1600.histogram.csv: tx: 3.14mpps, 0.01stdDev; rx: 3.14mpps, 0.00stdDev

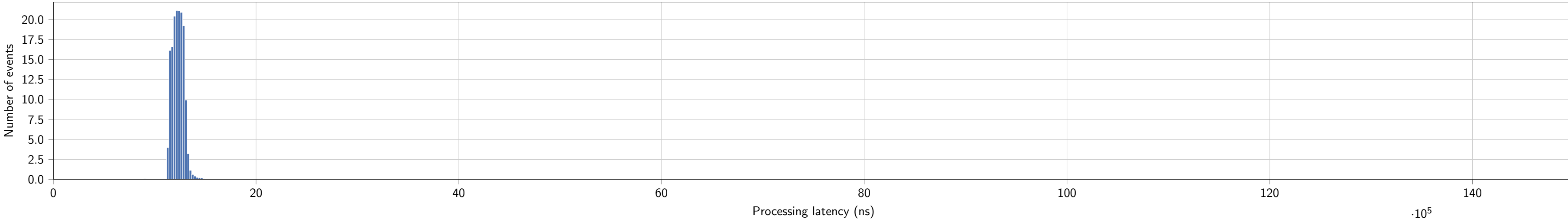




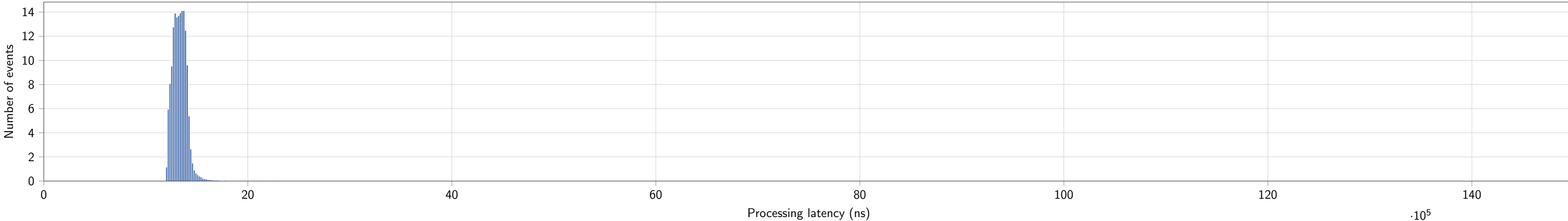




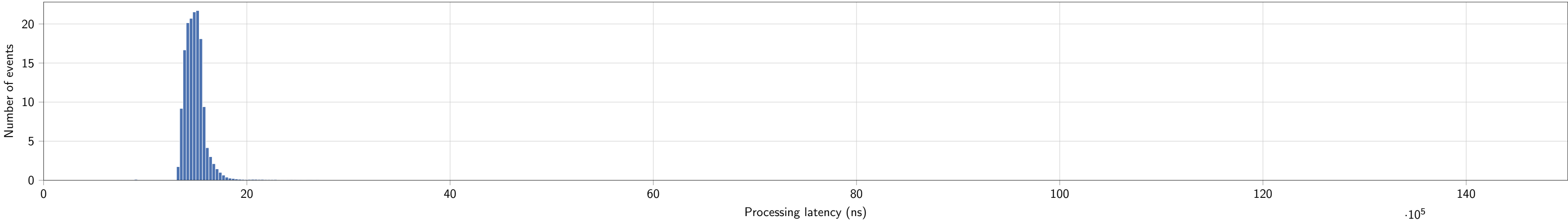
l2\_bridging\_cnf4\_mbit2800.histogram.csv: tx: 5.48mpps, 0.03stdDev; rx: 5.49mpps, 0.00stdDev



l2\_bridging\_cnf4\_mbit3200.histogram.csv: tx: 6.25mpps, 0.03stdDev; rx: 6.26mpps, 0.00stdDev



l2\_bridging\_cnf4\_mbit3600.histogram.csv: tx: 7.06mpps, 0.04stdDev; rx: 7.07mpps, 0.00stdDev



l2\_bridging\_cnf4\_mbit4000.histogram.csv: tx: 7.81mpps, 0.04stdDev; rx: 7.82mpps, 0.00stdDev

Number of events

$\cdot 10^4$

20.0

17.5

15.0

12.5

10.0

7.5

5.0

2.5

0.0

20

40

60

80

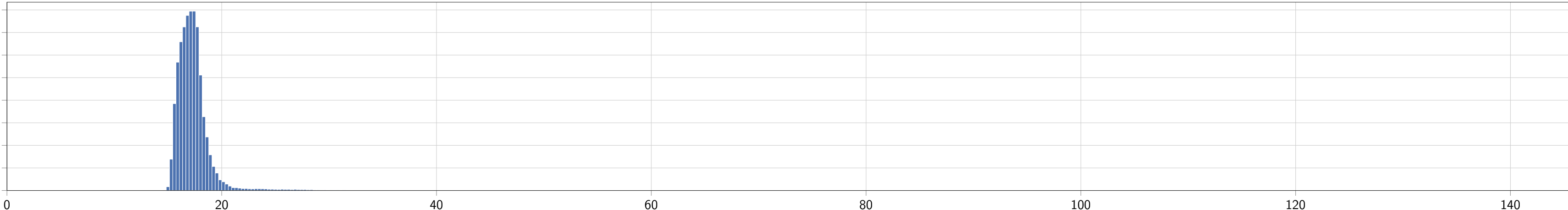
100

120

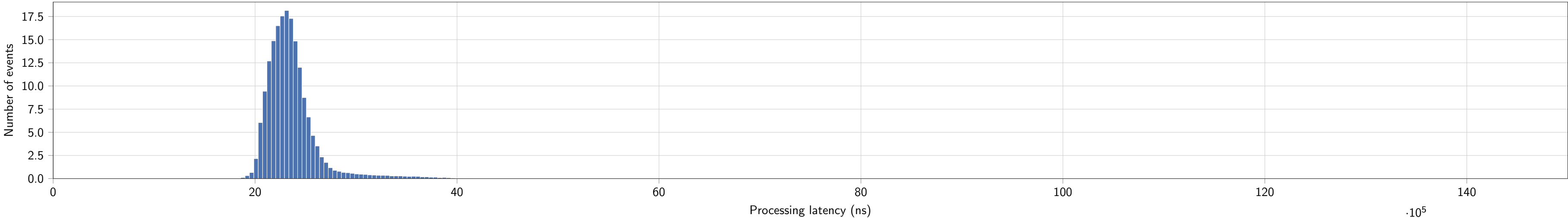
140

Processing latency (ns)

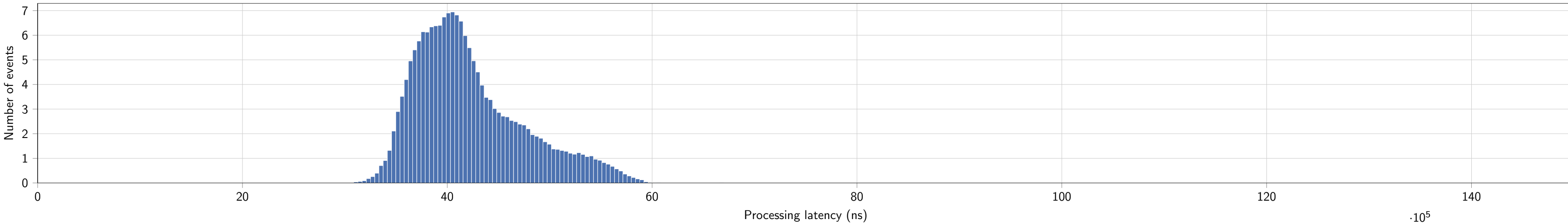
$\cdot 10^5$



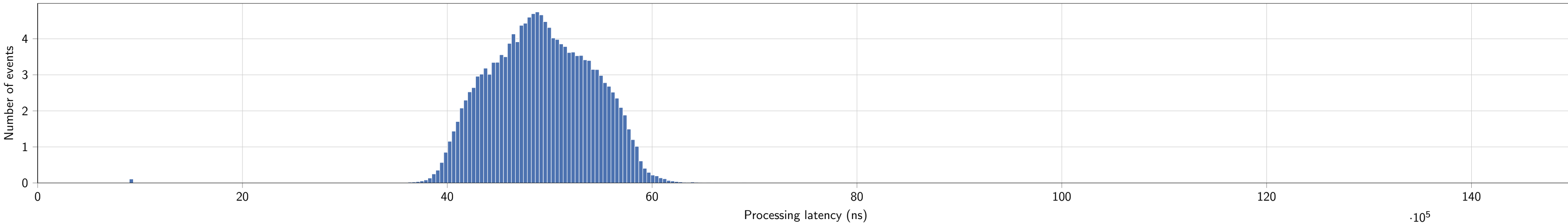
l2\_bridging\_cnf4\_mbit4400.histogram.csv: tx: 8.62mpps, 0.04stdDev; rx: 8.63mpps, 0.00stdDev



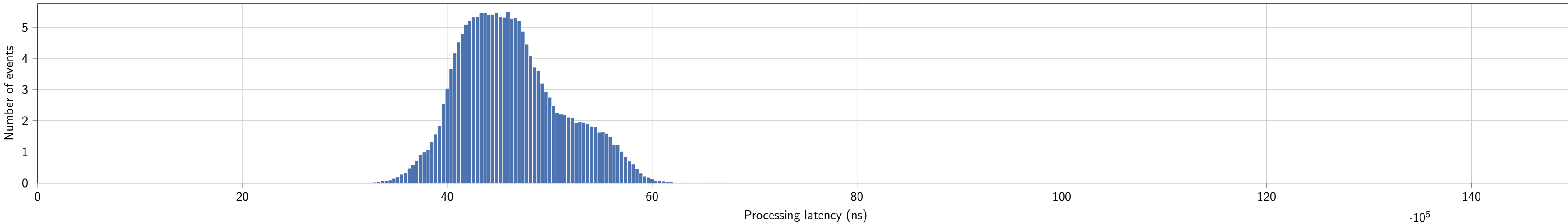
l2\_bridging\_cnf4\_mbit4701hires.histogram.csv: tx: 9.19mpps, 0.04stdDev; rx: 9.20mpps, 0.00stdDev



l2\_bridging\_cnf4\_mbit4711hires.histogram.csv: tx: 9.26mpps, 0.05stdDev; rx: 9.27mpps, 0.00stdDev

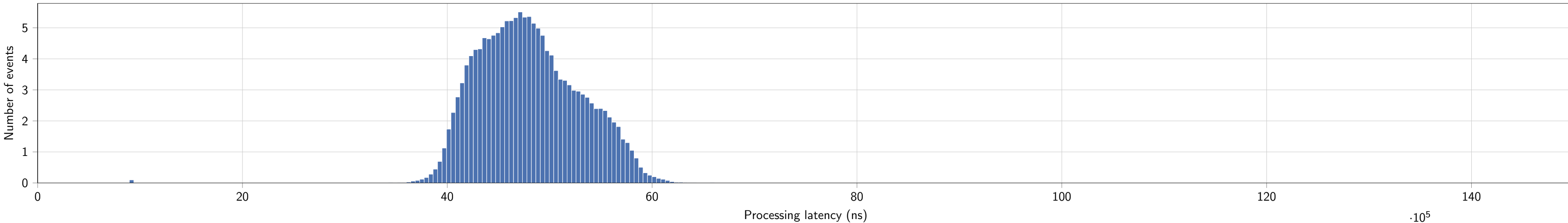


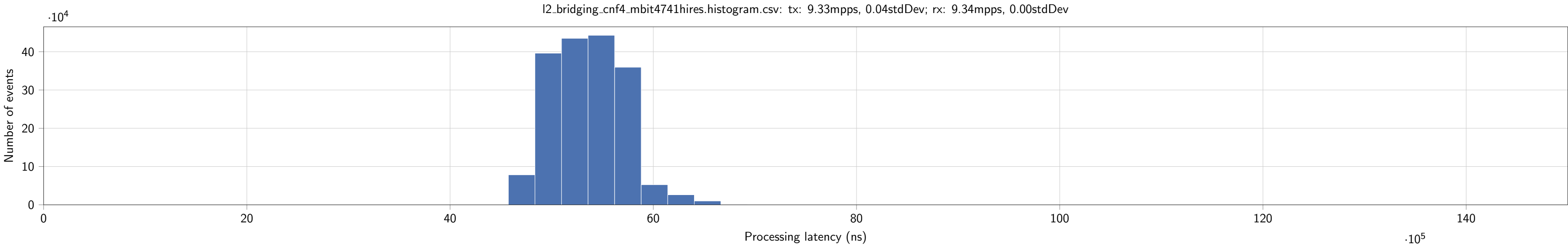
l2\_bridging\_cnf4\_mbit4721hires.histogram.csv: tx: 9.26mpps, 0.05stdDev; rx: 9.27mpps, 0.00stdDev



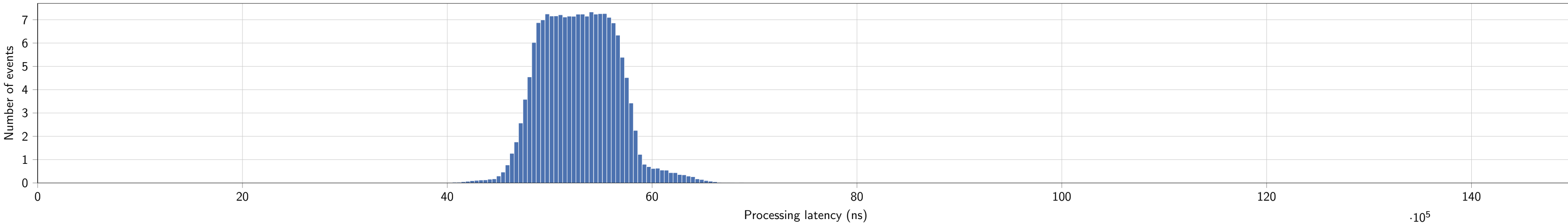


l2\_bridging\_cnf4\_mbit4731hires.histogram.csv: tx: 9.26mpps, 0.05stdDev; rx: 9.27mpps, 0.00stdDev

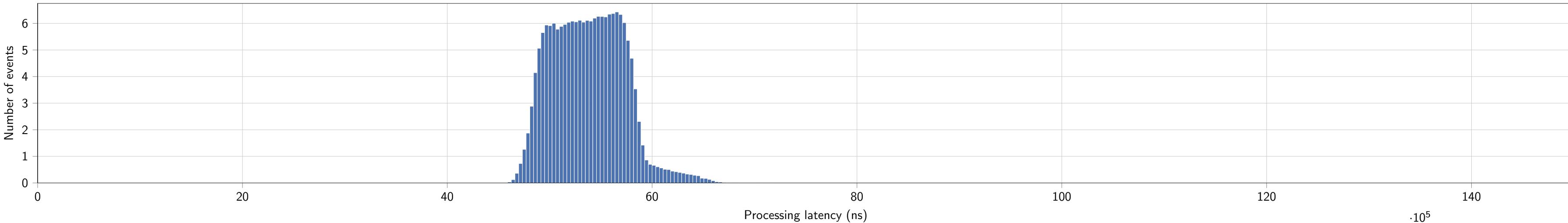




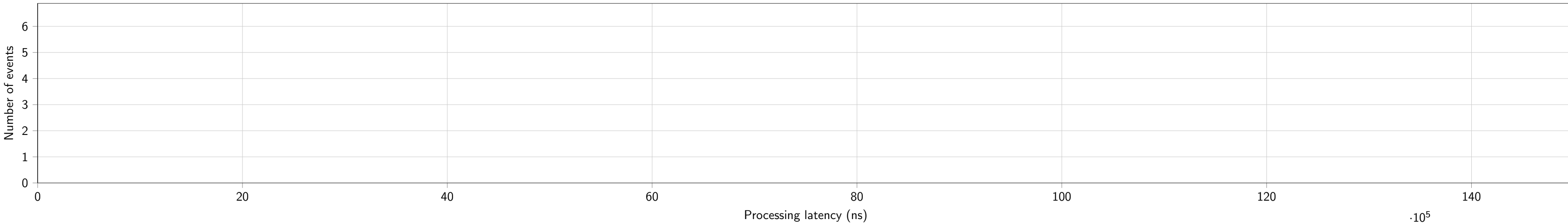
l2\_bridging\_cnf4\_mbit4751hires.histogram.csv: tx: 9.33mpps, 0.05stdDev; rx: 9.34mpps, 0.00stdDev



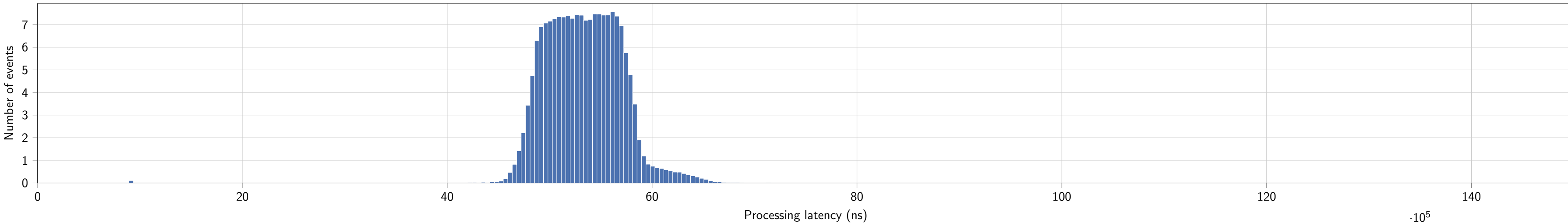
l2\_bridging\_cnf4\_mbit4761hires.histogram.csv: tx: 9.33mpps, 0.05stdDev; rx: 9.34mpps, 0.00stdDev



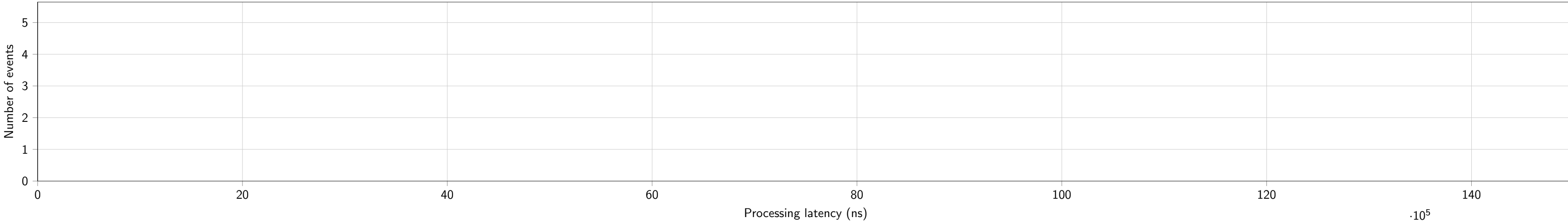
l2\_bridging\_cnf4\_mbit4771\_final.histogram.csv: tx: 9.32mpps, 0.04stdDev; rx: 9.28mpps, 0.00stdDev



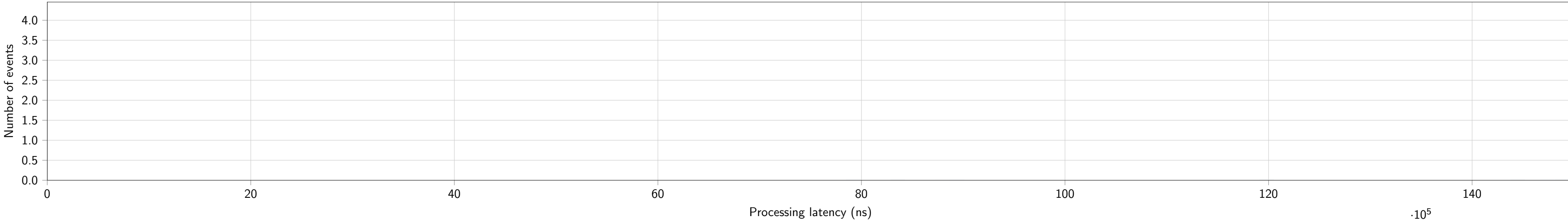
l2\_bridging\_cnf4\_mbit4771hires.histogram.csv: tx: 9.33mpps, 0.05stdDev; rx: 9.34mpps, 0.00stdDev



l2\_bridging\_cnf4\_mbit4781hires.histogram.csv: tx: 9.39mpps, 0.05stdDev; rx: 9.36mpps, 0.00stdDev

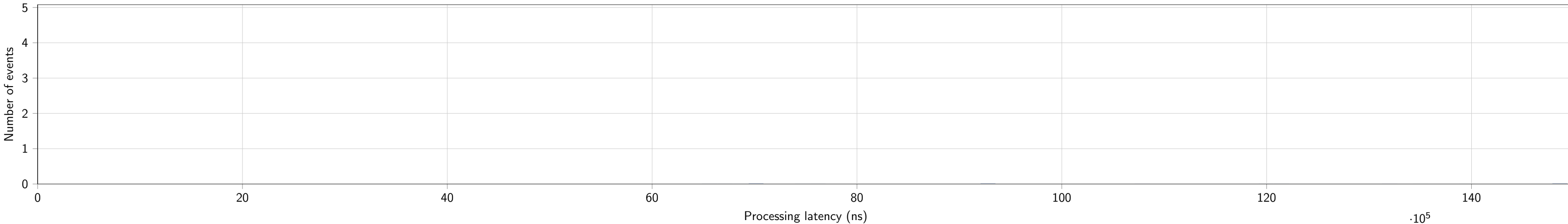


l2\_bridging\_cnf4\_mbit4791hires.histogram.csv: tx: 9.39mpps, 0.05stdDev; rx: 9.38mpps, 0.00stdDev

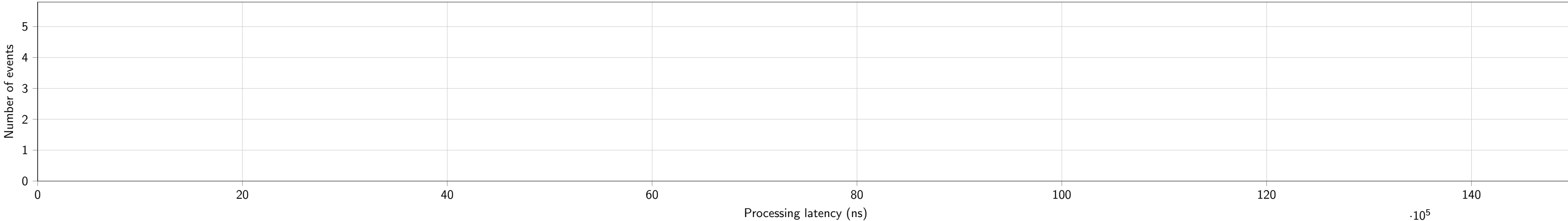




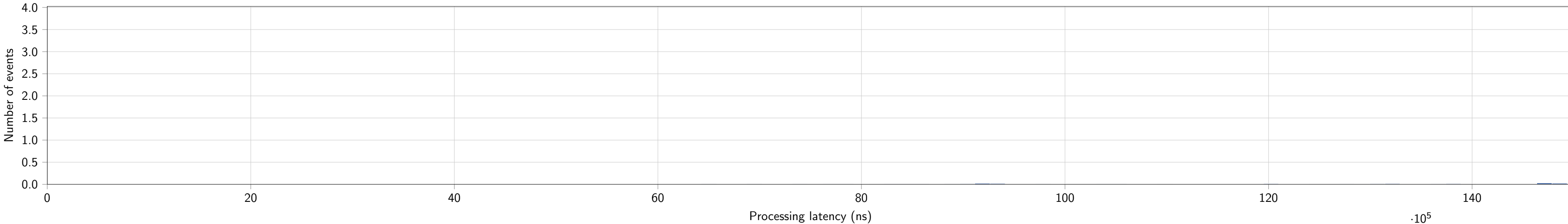
l2\_bridging\_cnf4\_mbit4800.histogram.csv: tx: 9.39mpps, 0.04stdDev; rx: 9.39mpps, 0.00stdDev



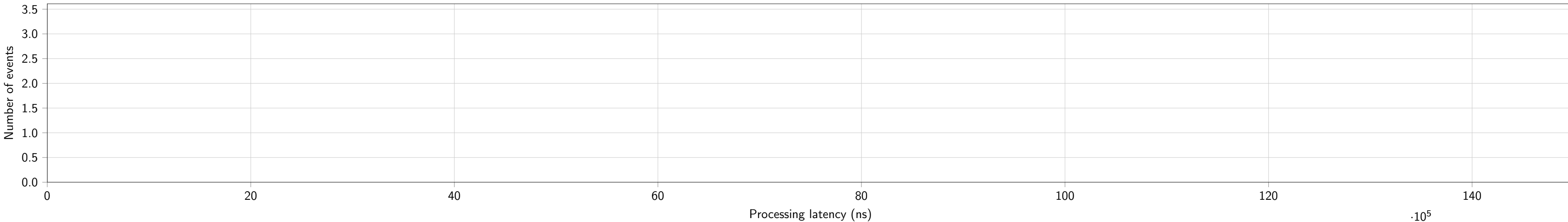
l2\_bridging\_cnf4\_mbit4801hires.histogram.csv: tx: 9.39mpps, 0.04stdDev; rx: 9.37mpps, 0.00stdDev



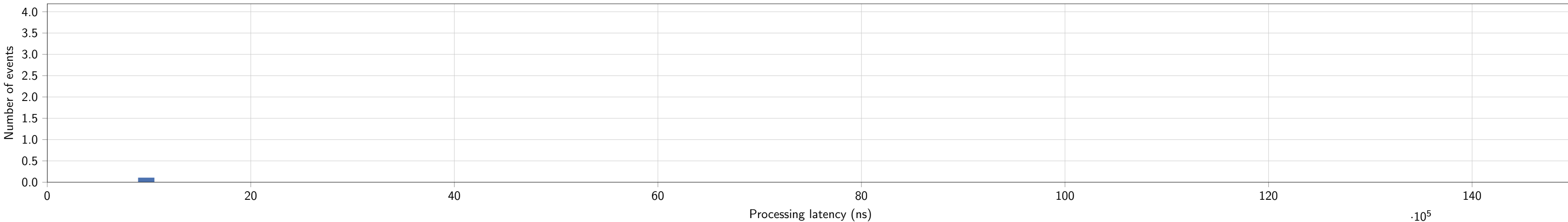
l2\_bridging\_cnf4\_mbit4811hires.histogram.csv: tx: 9.39mpps, 0.05stdDev; rx: 9.40mpps, 0.00stdDev



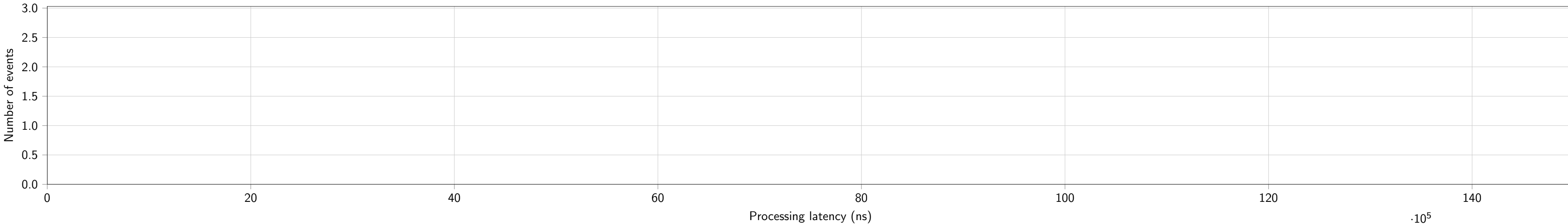
l2\_bridging\_cnf4\_mbit4821hires.histogram.csv: tx: 9.46mpps, 0.04stdDev; rx: 9.39mpps, 0.00stdDev



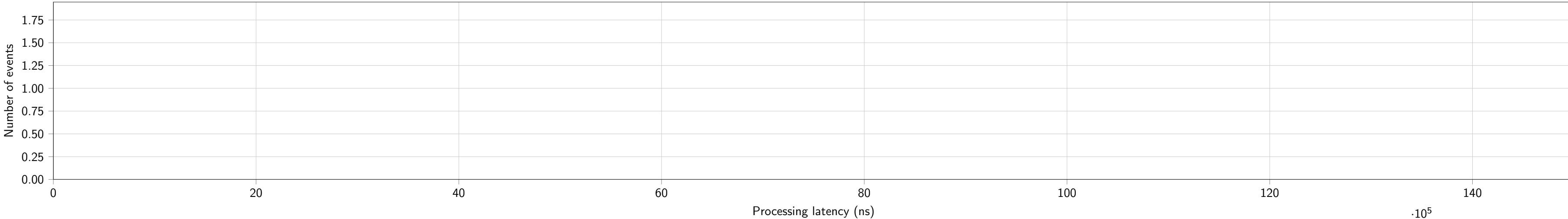
l2\_bridging\_cnf4\_mbit4831hires.histogram.csv: tx: 9.46mpps, 0.05stdDev; rx: 9.35mpps, 0.00stdDev



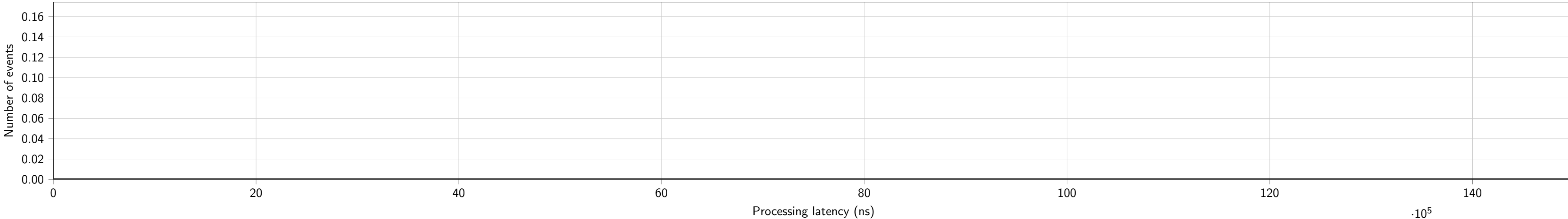
l2\_bridging\_cnf4\_mbit4841hires.histogram.csv: tx: 9.46mpps, 0.05stdDev; rx: 9.38mpps, 0.00stdDev



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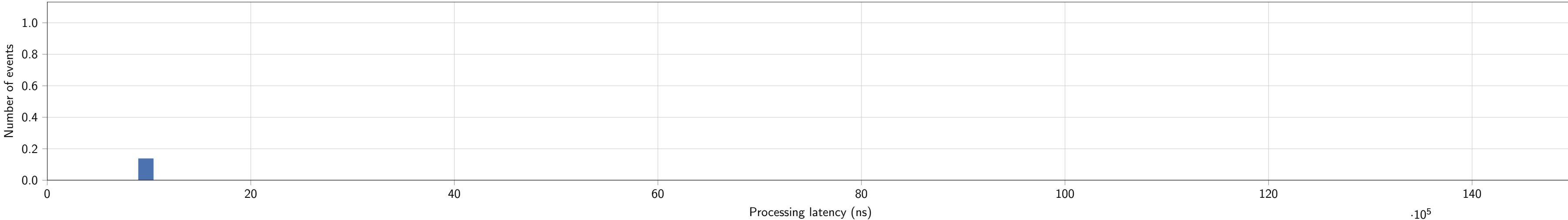


l2\_bridging\_cnf4\_mbit5200.histogram.csv: tx: 10.15mpps, 0.05stdDev; rx: 9.38mpps, 0.00stdDev

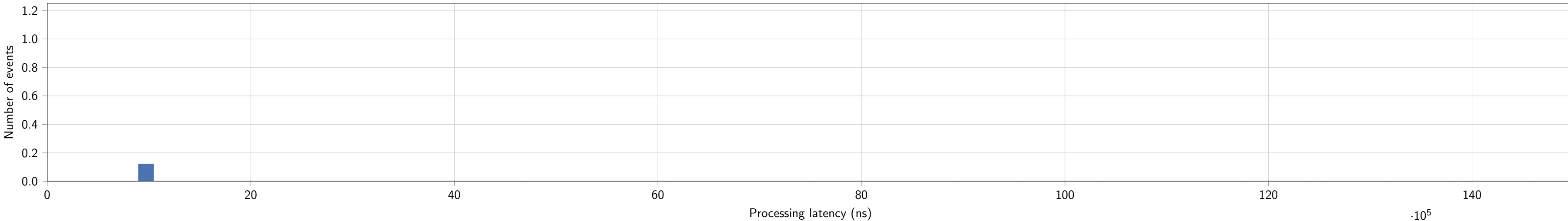




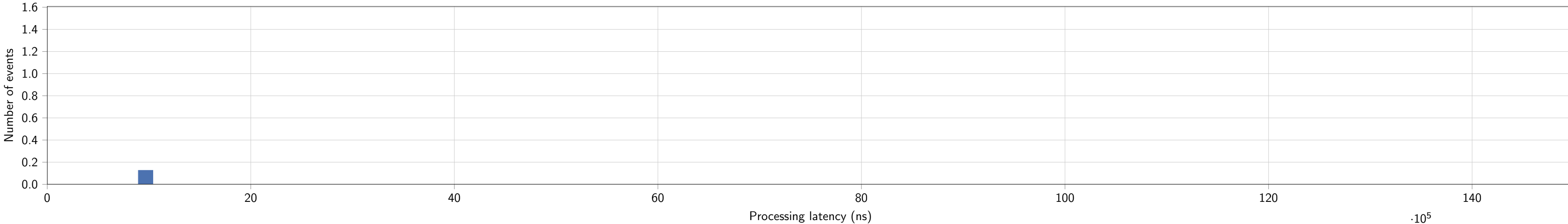
l2\_bridging\_cnf4\_mbit5600.histogram.csv: tx: 10.95mpps, 0.05stdDev; rx: 9.27mpps, 0.00stdDev

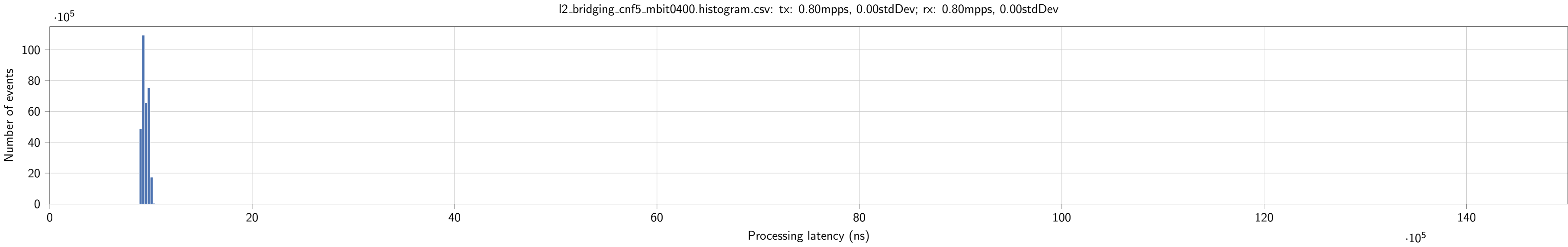


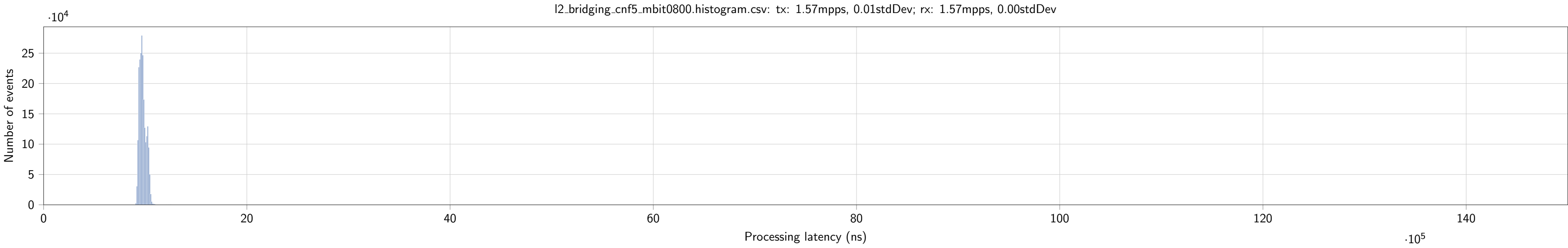
l2\_bridging\_cnf4\_mbit6000.histogram.csv: tx: 11.78mpps, 0.06stdDev; rx: 9.39mpps, 0.00stdDev



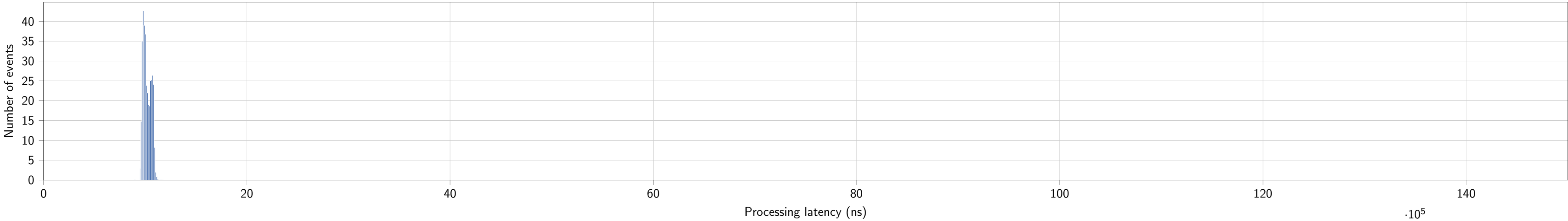
l2\_bridging\_cnf4\_mbit9000.histogram.csv: tx: 14.86mpps, 0.07stdDev; rx: 9.38mpps, 0.00stdDev

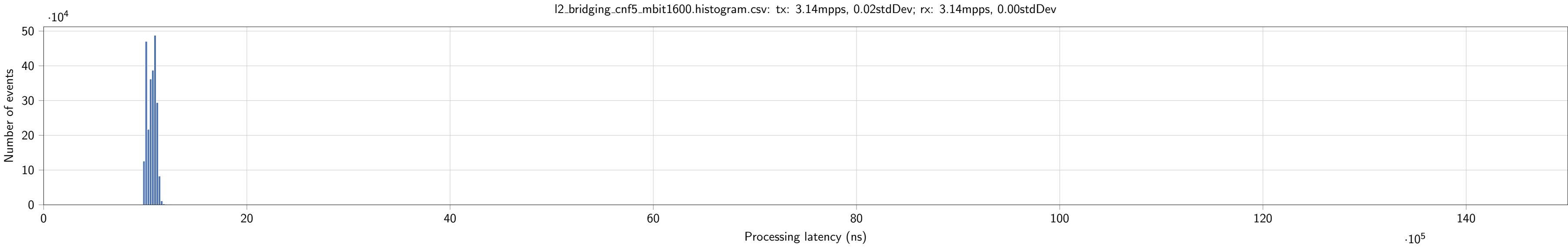


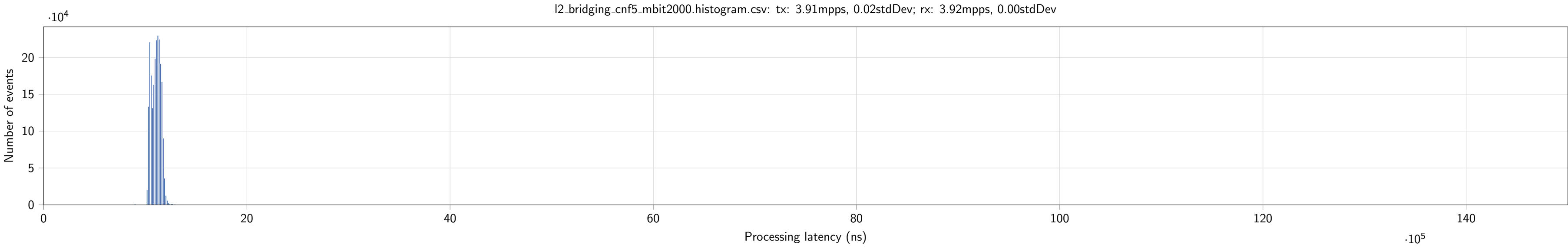




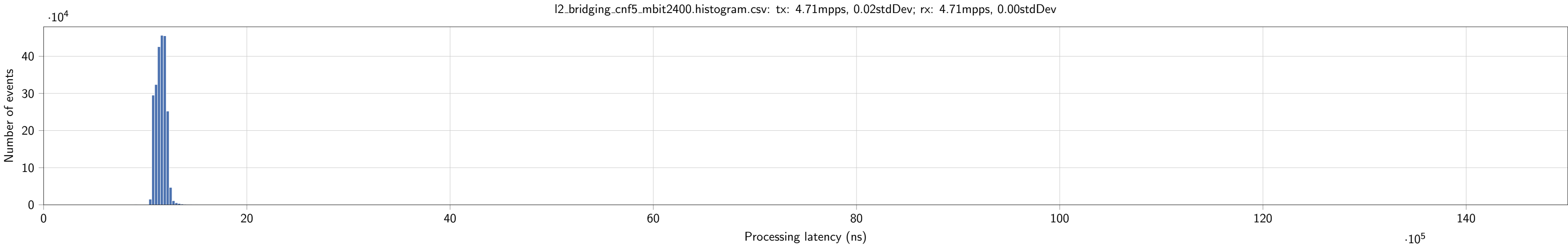
l2\_bridging\_cnf5\_mbit1200.histogram.csv: tx: 2.36mpps, 0.01stdDev; rx: 2.36mpps, 0.00stdDev



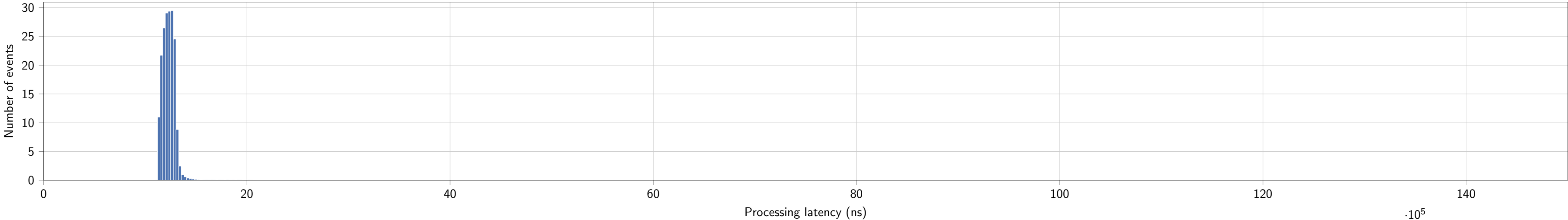


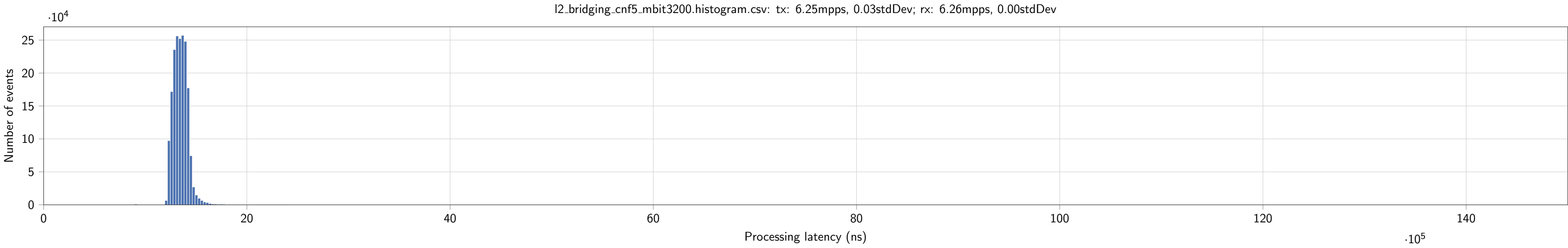




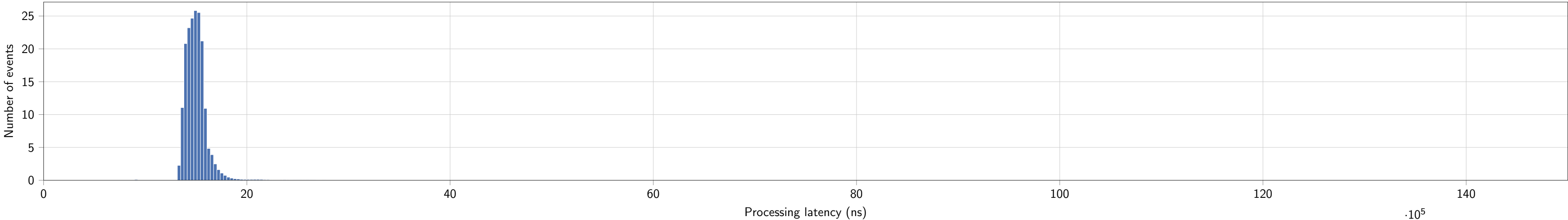


l2\_bridging\_cnf5\_mbit2800.histogram.csv: tx: 5.49mpps, 0.03stdDev; rx: 5.49mpps, 0.00stdDev





l2\_bridging\_cnf5\_mbit3600.histogram.csv: tx: 7.06mpps, 0.03stdDev; rx: 7.07mpps, 0.00stdDev



l2\_bridging\_cnf5\_mbit4000.histogram.csv: tx: 7.81mpps, 0.04stdDev; rx: 7.82mpps, 0.00stdDev

Number of events

20.0  
17.5  
15.0  
12.5  
10.0  
7.5  
5.0  
2.5  
0.0

0

20

40

60

80

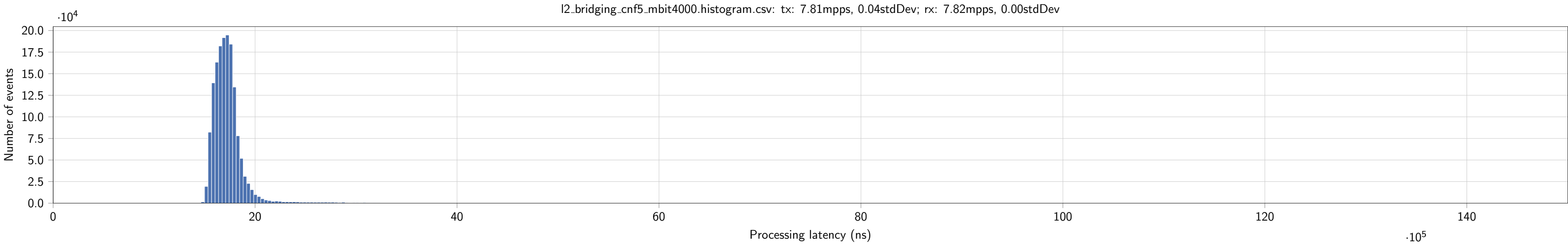
100

120

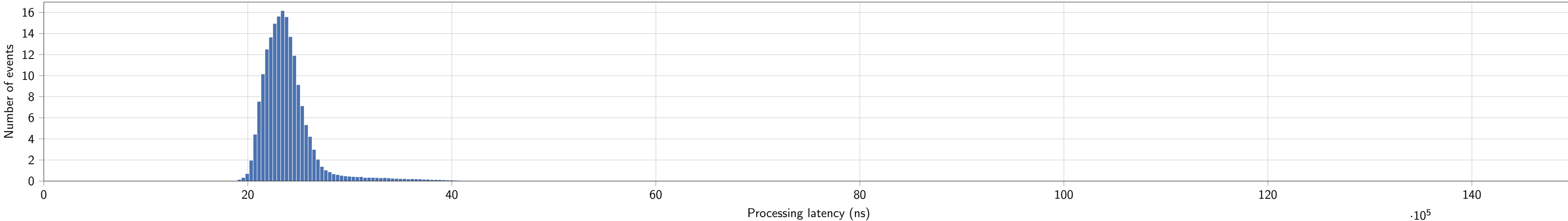
140

Processing latency (ns)

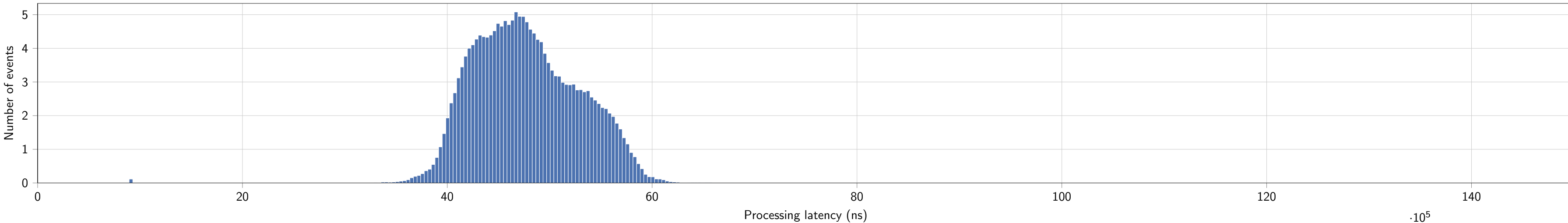
$\cdot 10^5$



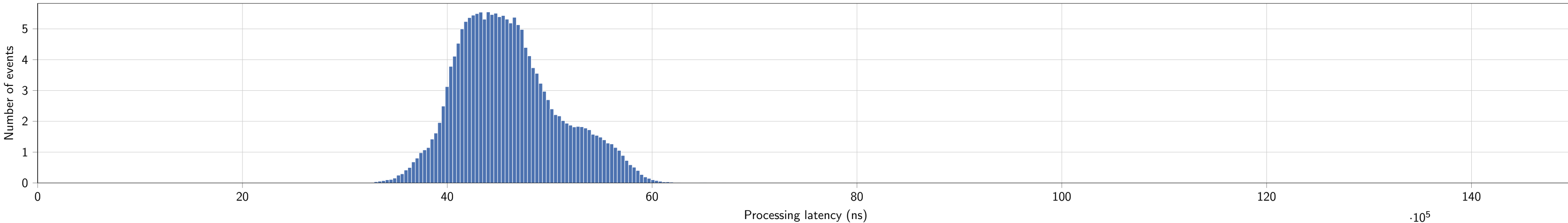
l2\_bridging\_cnf5\_mbit4400.histogram.csv: tx: 8.62mpps, 0.04stdDev; rx: 8.63mpps, 0.00stdDev



l2\_bridging\_cnf5\_mbit4708hires.histogram.csv: tx: 9.26mpps, 0.05stdDev; rx: 9.27mpps, 0.00stdDev

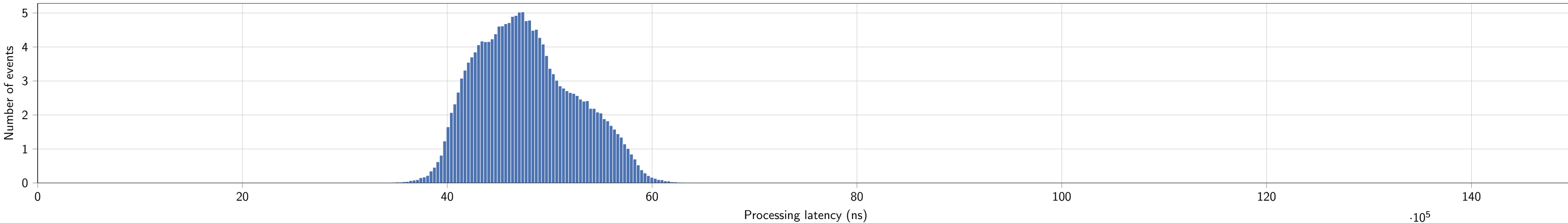


l2\_bridging\_cnf5\_mbit4718hires.histogram.csv: tx: 9.26mpps, 0.05stdDev; rx: 9.27mpps, 0.00stdDev

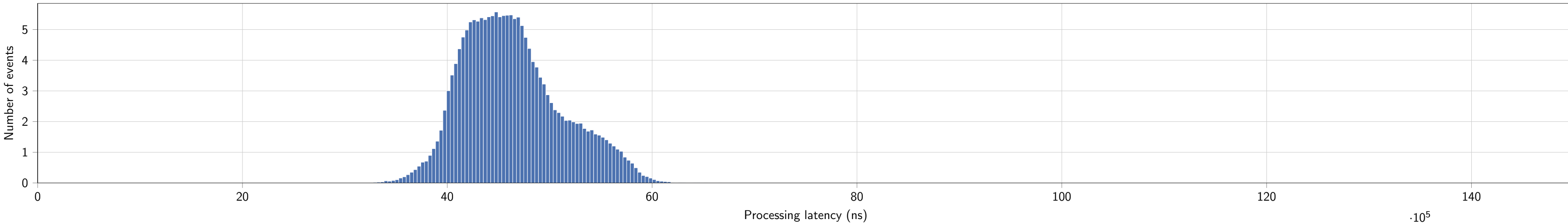




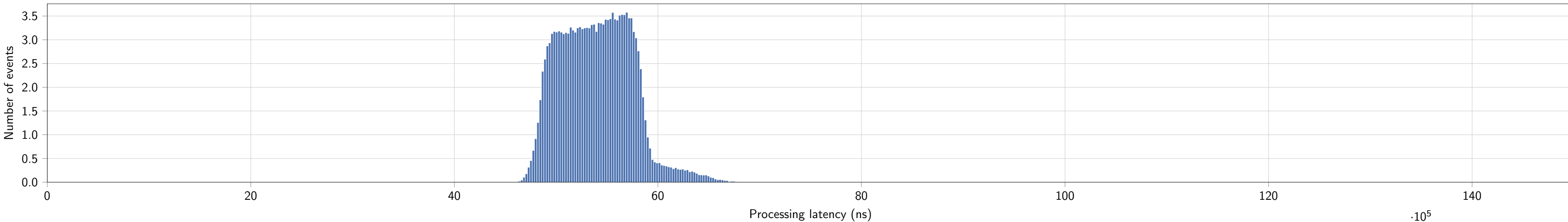
l2\_bridging\_cnf5\_mbit4728hires.histogram.csv: tx: 9.26mpps, 0.05stdDev; rx: 9.27mpps, 0.00stdDev



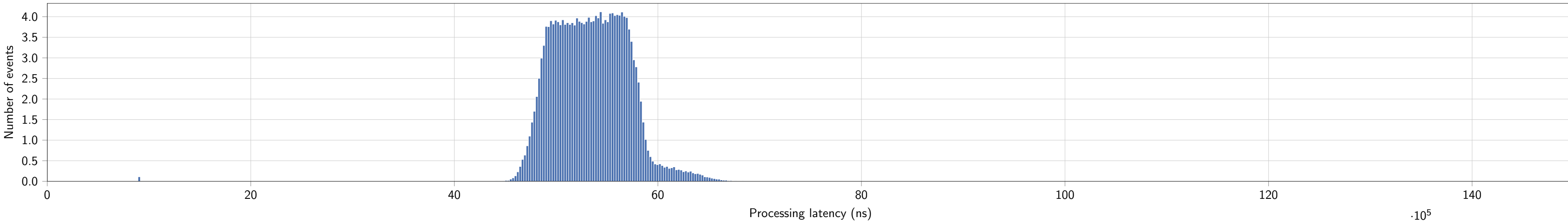
l2\_bridging\_cnf5\_mbit4738hires.histogram.csv: tx: 9.26mpps, 0.05stdDev; rx: 9.27mpps, 0.00stdDev



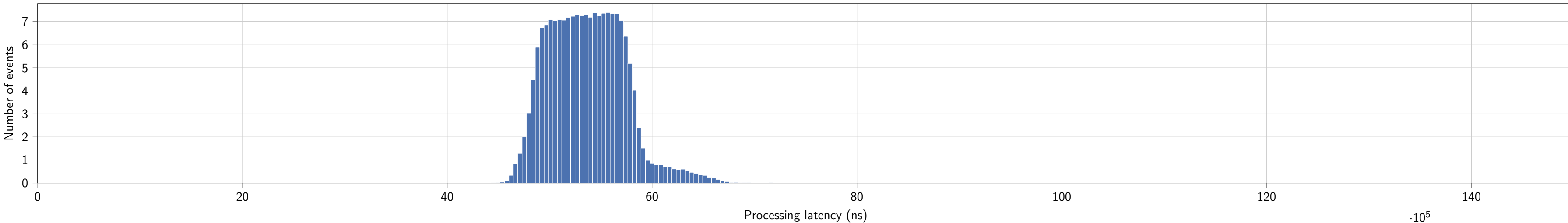
l2\_bridging\_cnf5\_mbit4748hires.histogram.csv: tx: 9.33mpps, 0.05stdDev; rx: 9.34mpps, 0.00stdDev



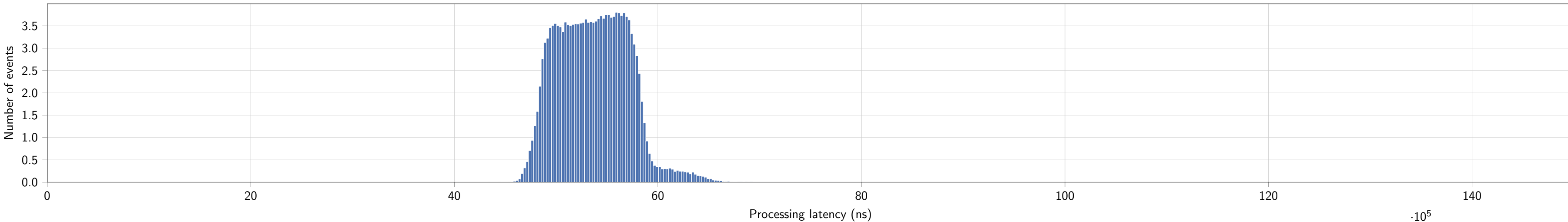
l2\_bridging\_cnf5\_mbit4758hires.histogram.csv: tx: 9.33mpps, 0.05stdDev; rx: 9.34mpps, 0.00stdDev



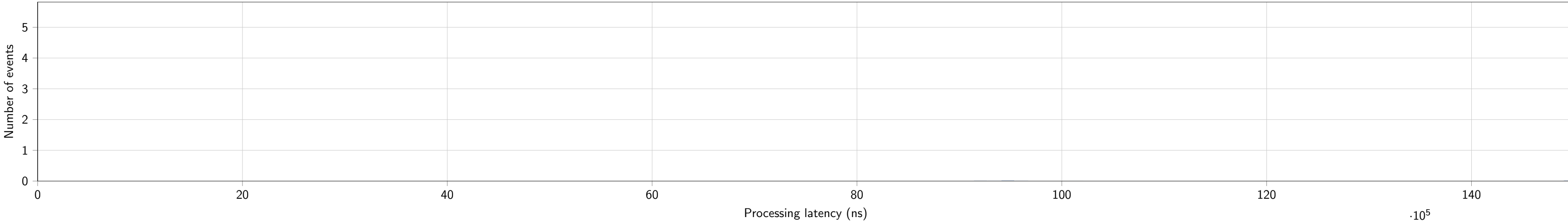
l2\_bridging\_cnf5\_mbit4768\_final.histogram.csv: tx: 9.33mpps, 0.05stdDev; rx: 9.34mpps, 0.00stdDev



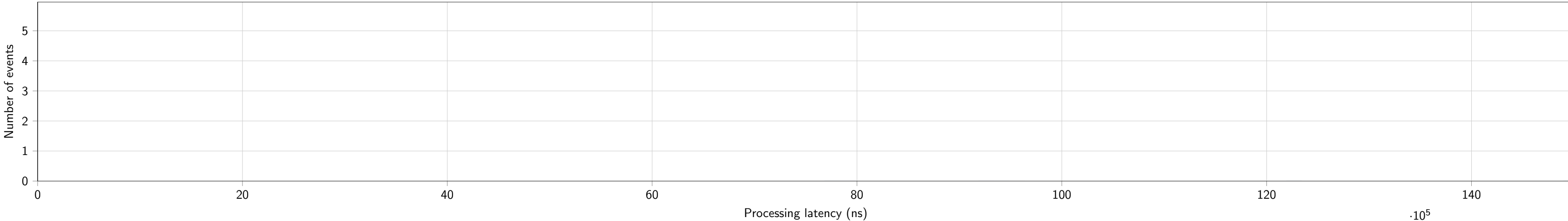
l2\_bridging\_cnf5\_mbit4768hires.histogram.csv: tx: 9.33mpps, 0.05stdDev; rx: 9.34mpps, 0.00stdDev



l2\_bridging\_cnf5\_mbit4778hires.histogram.csv: tx: 9.39mpps, 0.04stdDev; rx: 9.39mpps, 0.00stdDev

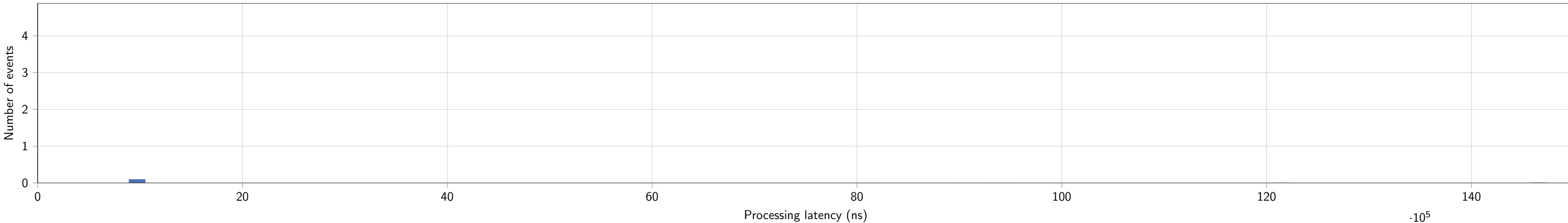


l2\_bridging\_cnf5\_mbit4788hires.histogram.csv: tx: 9.39mpps, 0.05stdDev; rx: 9.39mpps, 0.00stdDev

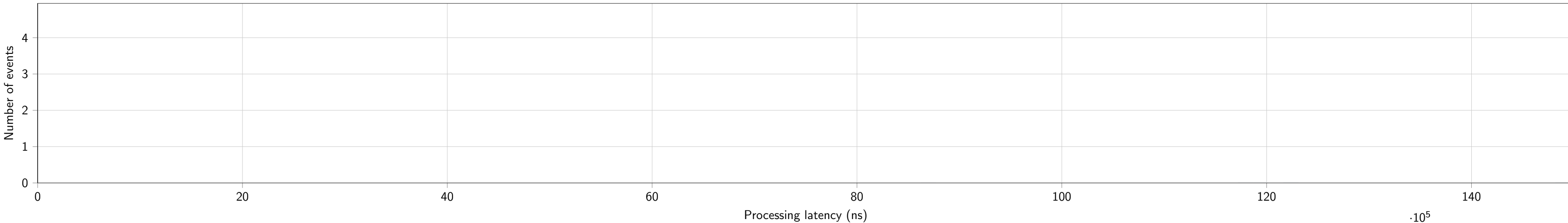




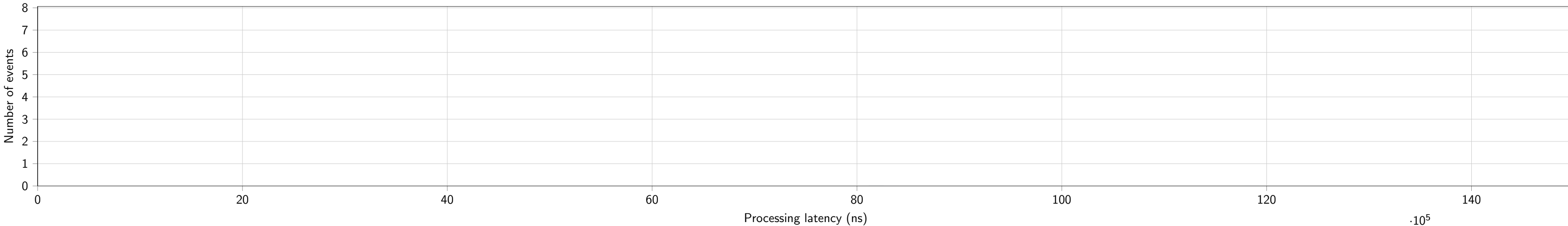
l2\_bridging\_cnf5\_mbit4798hires.histogram.csv: tx: 9.39mpps, 0.05stdDev; rx: 9.38mpps, 0.00stdDev



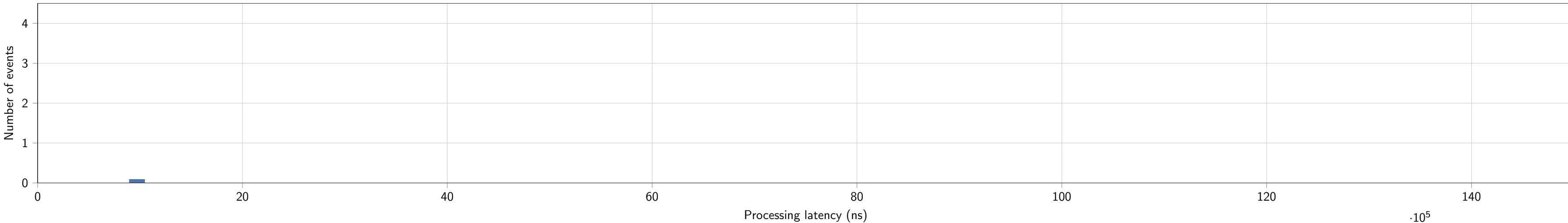
l2\_bridging\_cnf5\_mbit4800.histogram.csv: tx: 9.39mpps, 0.05stdDev; rx: 9.38mpps, 0.00stdDev



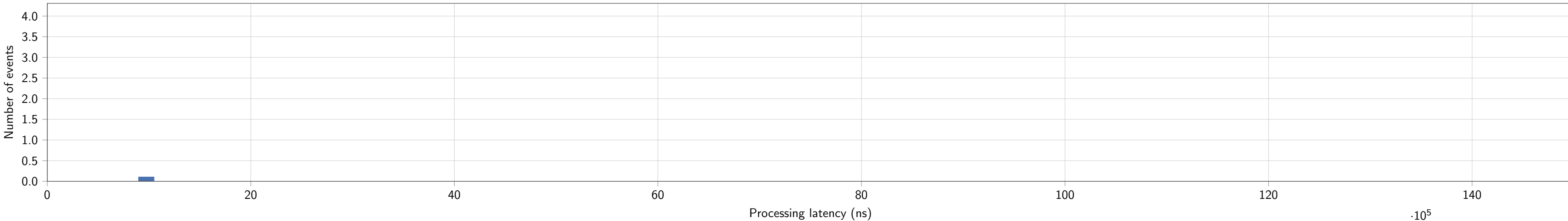
l2\_bridging\_cnf5\_mbit4808hires.histogram.csv: tx: 9.39mpps, 0.05stdDev; rx: 9.38mpps, 0.00stdDev



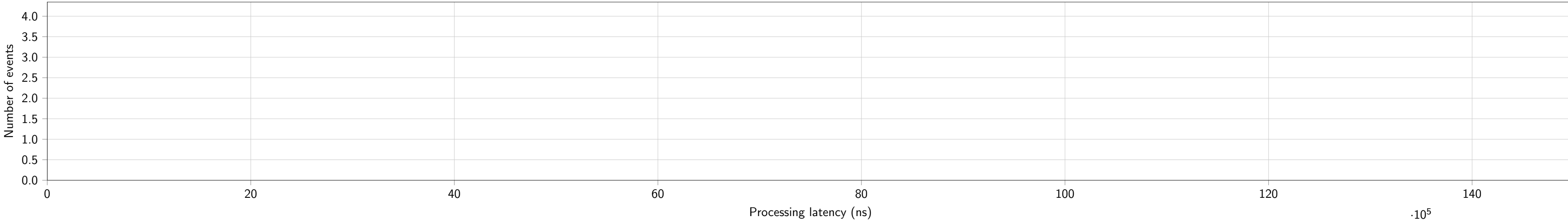
l2\_bridging\_cnf5\_mbit4818hires.histogram.csv: tx: 9.46mpps, 0.05stdDev; rx: 9.35mpps, 0.00stdDev



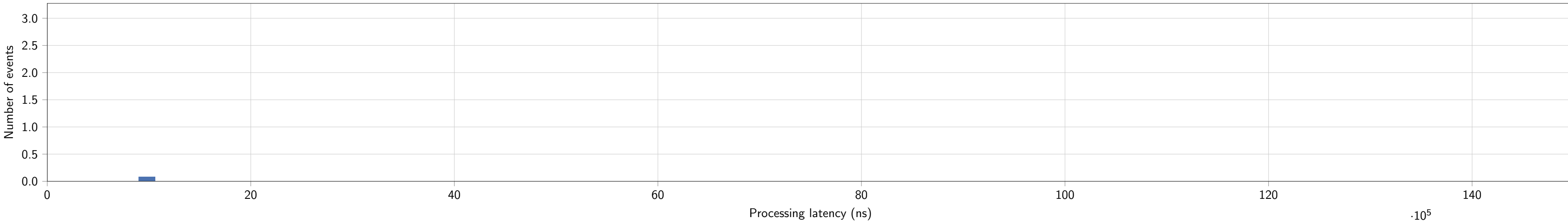
l2\_bridging\_cnf5\_mbit4828hires.histogram.csv: tx: 9.46mpps, 0.05stdDev; rx: 9.26mpps, 0.00stdDev



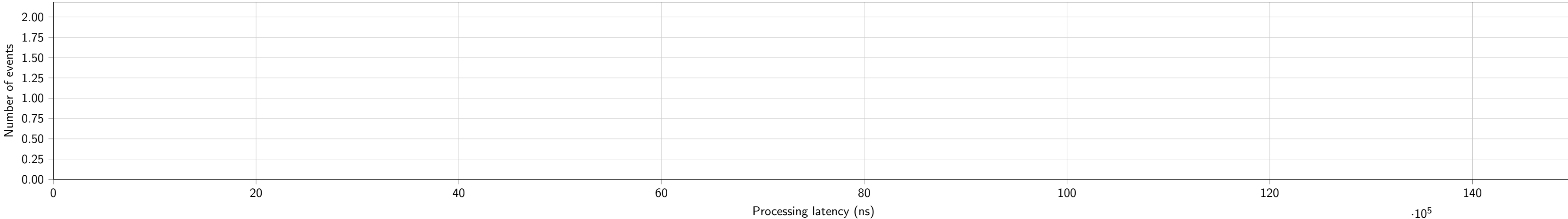
l2\_bridging\_cnf5\_mbit4838hires.histogram.csv: tx: 9.46mpps, 0.05stdDev; rx: 9.37mpps, 0.00stdDev



l2\_bridging\_cnf5\_mbit4848hires.histogram.csv: tx: 9.46mpps, 0.05stdDev; rx: 9.37mpps, 0.00stdDev

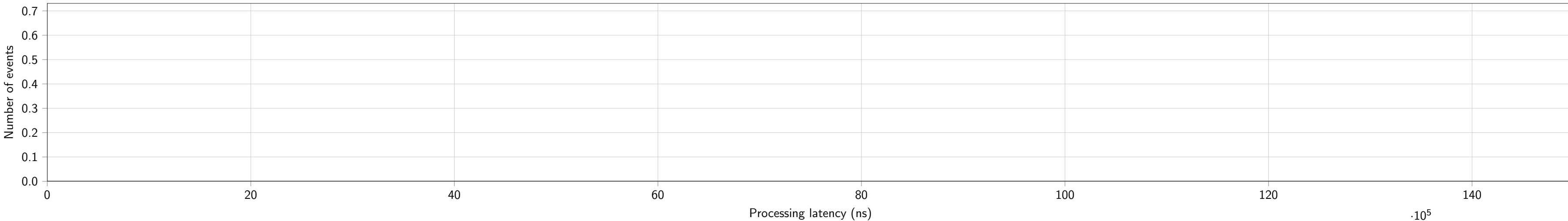


l2\_bridging\_cnf5\_mbit4858hires.histogram.csv: tx: 9.53mpps, 0.05stdDev; rx: 9.38mpps, 0.00stdDev

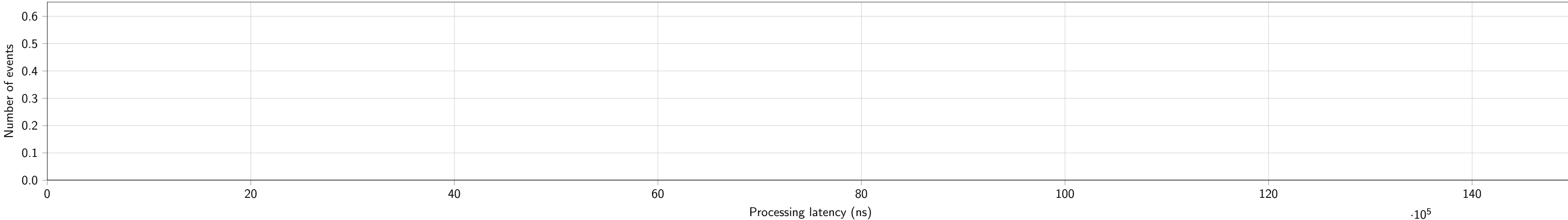




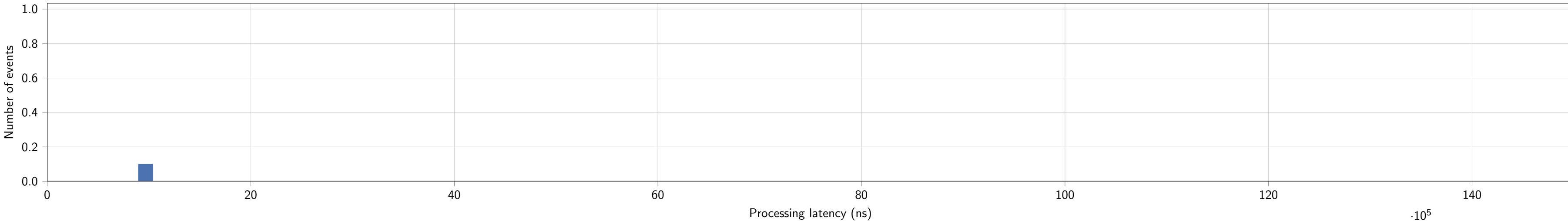
l2\_bridging\_cnf5\_mbit5200.histogram.csv: tx: 10.15mpps, 0.05stdDev; rx: 9.33mpps, 0.00stdDev



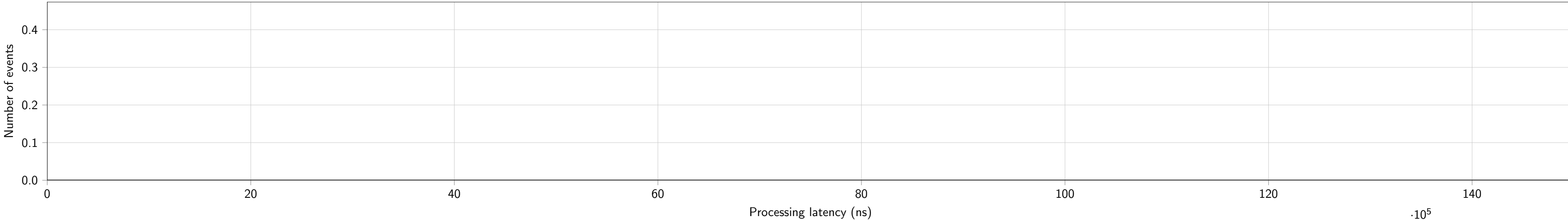
l2\_bridging\_cnf5\_mbit5600.histogram.csv: tx: 10.95mpps, 0.05stdDev; rx: 9.26mpps, 0.00stdDev

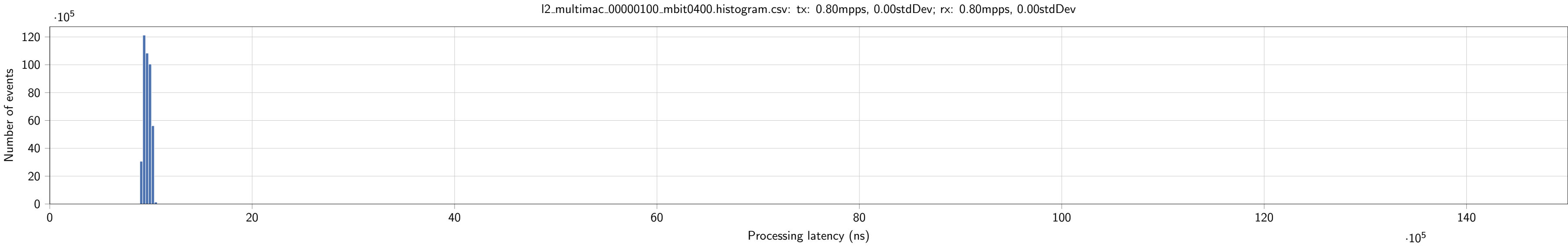


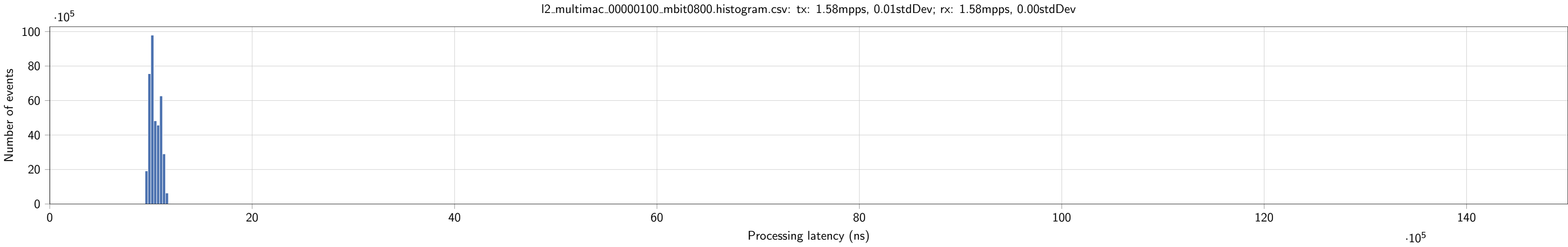
l2\_bridging\_cnf5\_mbit6000.histogram.csv: tx: 11.78mpps, 0.06stdDev; rx: 9.35mpps, 0.00stdDev



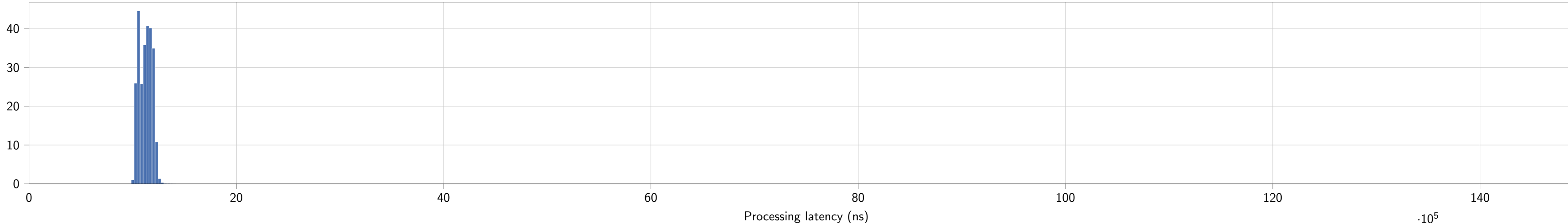
l2\_bridging\_cnf5\_mbit9000.histogram.csv: tx: 14.86mpps, 0.07stdDev; rx: 9.39mpps, 0.00stdDev





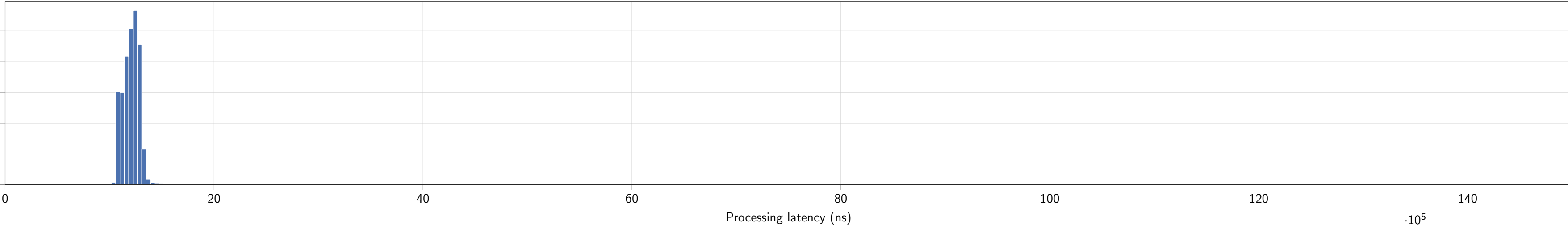


Number of events

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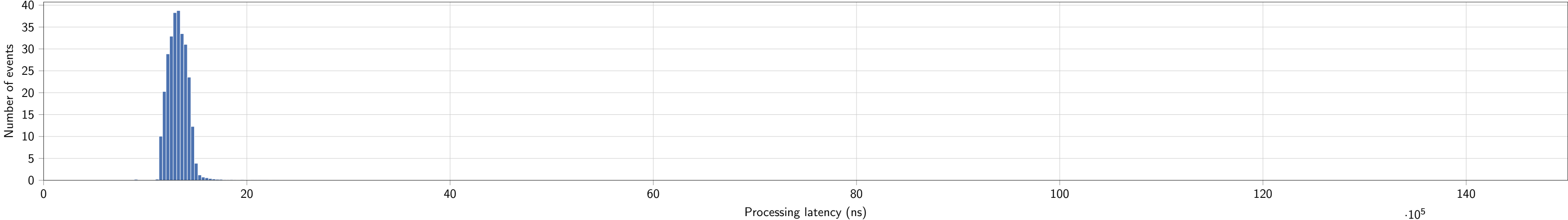
l2\_multimac\_00000100\_mbit1600.histogram.csv: tx: 3.14mpps, 0.02stdDev; rx: 3.14mpps, 0.00stdDev

Number of events

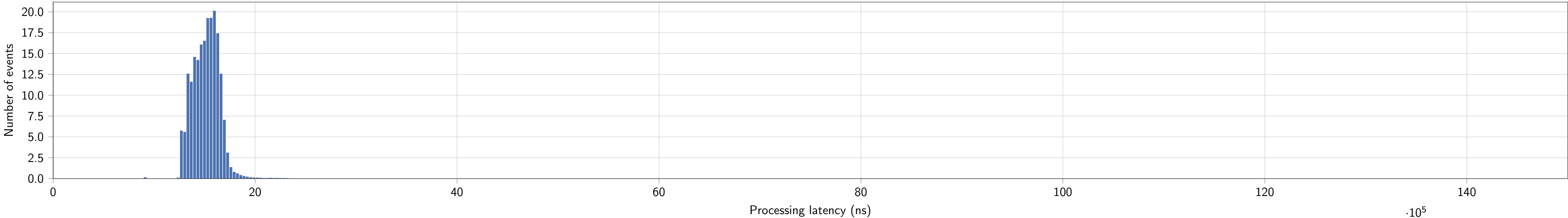




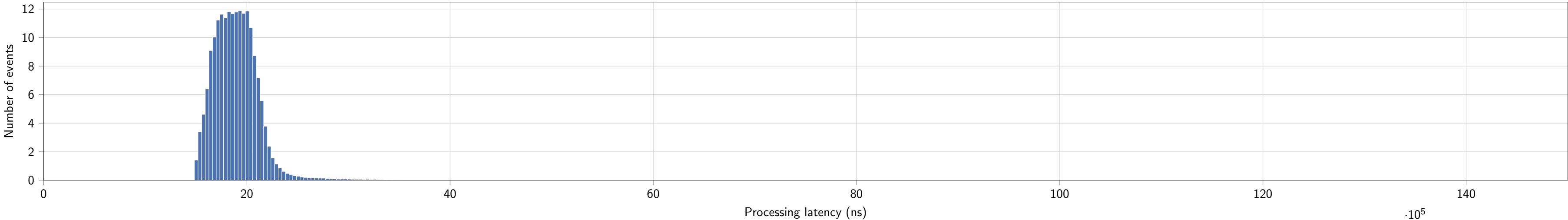
l2\_multimac\_00000100\_mbit2000.histogram.csv: tx: 3.92mpps, 0.02stdDev; rx: 3.92mpps, 0.00stdDev



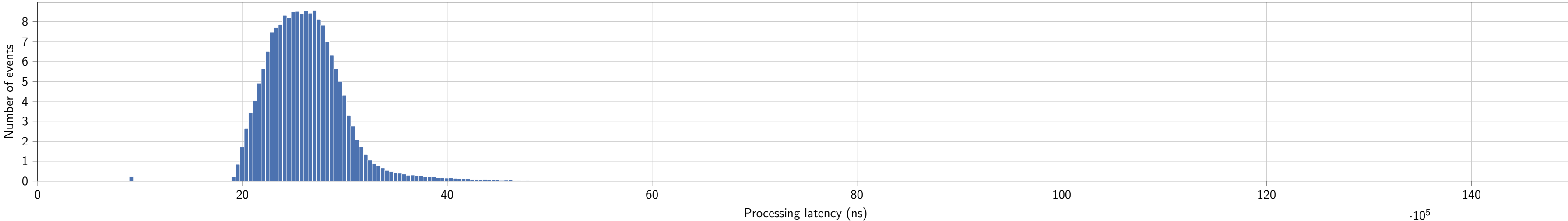
l2\_multimac\_00000100\_mbit2400.histogram.csv: tx: 4.70mpps, 0.03stdDev; rx: 4.71mpps, 0.00stdDev



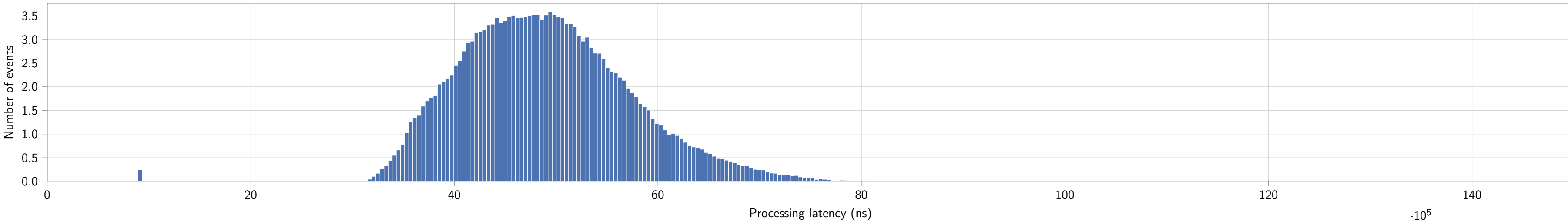
l2\_multimac\_00000100\_mbit2800.histogram.csv: tx: 5.48mpps, 0.04stdDev; rx: 5.49mpps, 0.00stdDev



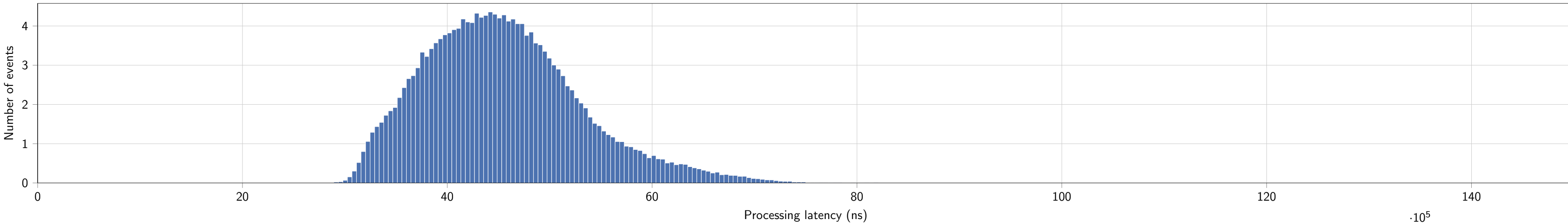
l2\_multimac\_00000100\_mbit3200.histogram.csv: tx: 6.25mpps, 0.04stdDev; rx: 6.26mpps, 0.00stdDev



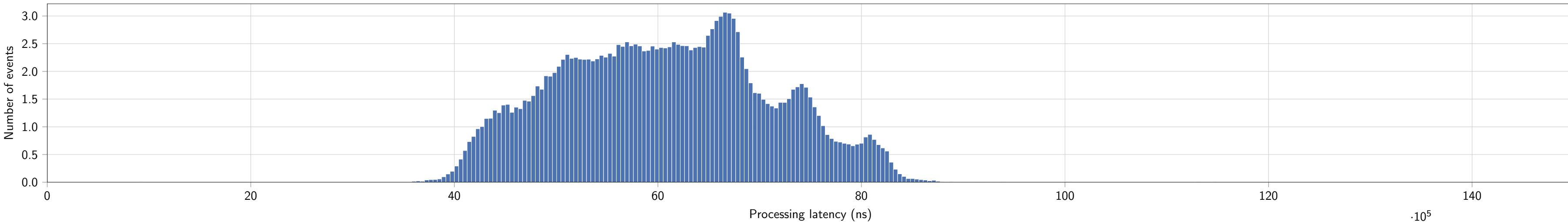
l2\_multimac\_00000100\_mbit3447hires.histogram.csv: tx: 6.76mpps, 0.04stdDev; rx: 6.77mpps, 0.00stdDev



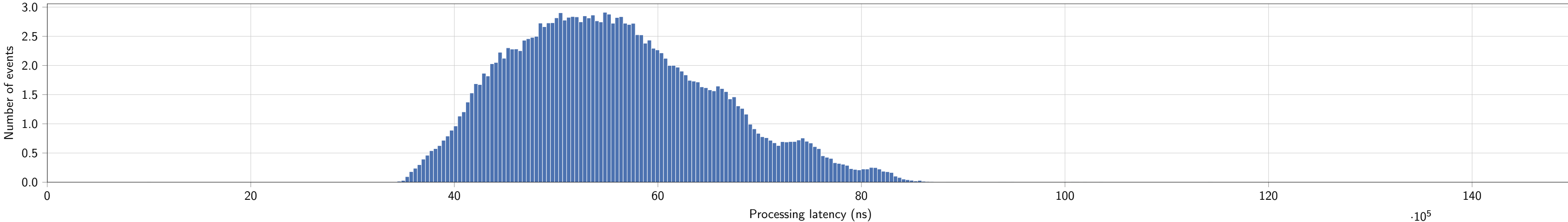
l2\_multimac\_00000100\_mbit3457hires.histogram.csv: tx: 6.76mpps, 0.04stdDev; rx: 6.77mpps, 0.00stdDev



l2\_multimac\_00000100\_mbit3467hires.histogram.csv: tx: 6.79mpps, 0.04stdDev; rx: 6.80mpps, 0.00stdDev

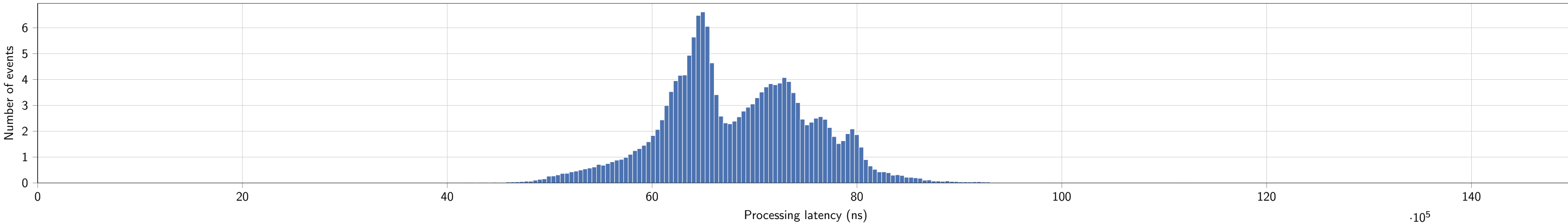


l2\_multimac\_00000100\_mbit3477hires.histogram.csv: tx: 6.79mpps, 0.04stdDev; rx: 6.80mpps, 0.00stdDev

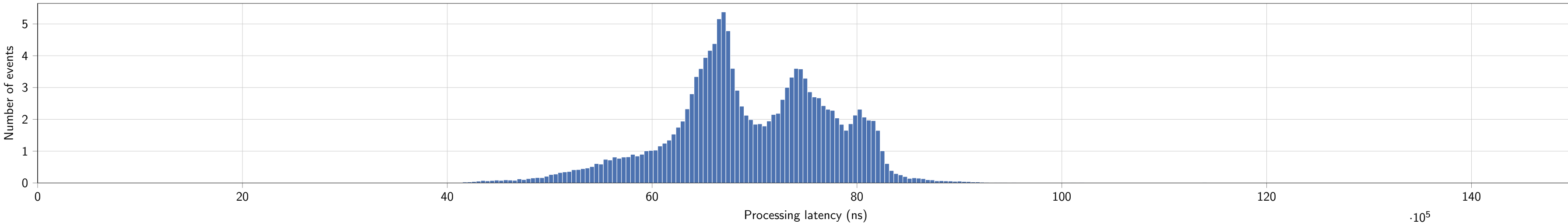




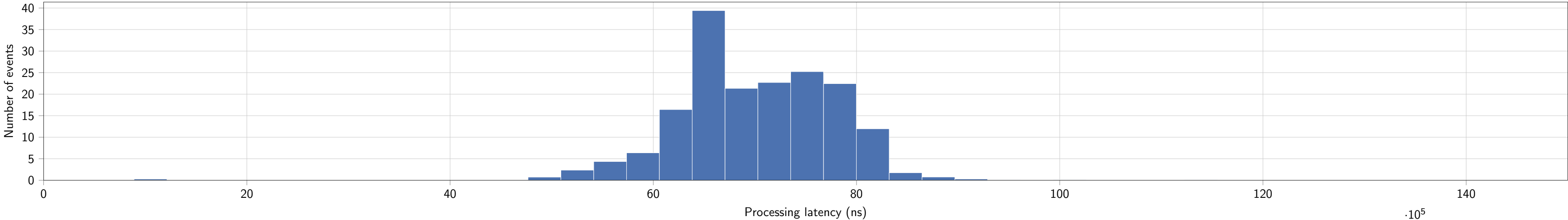
l2\_multimac\_00000100\_mbit3487hires.histogram.csv: tx: 6.83mpps, 0.04stdDev; rx: 6.84mpps, 0.00stdDev



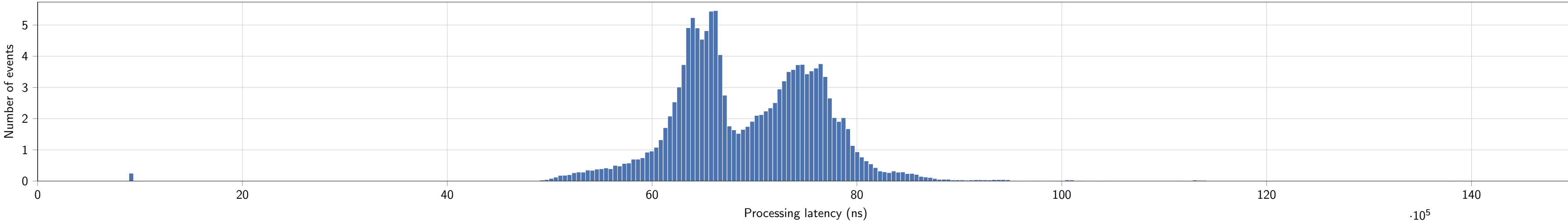
l2\_multimac\_00000100\_mbit3497hires.histogram.csv: tx: 6.83mpps, 0.05stdDev; rx: 6.84mpps, 0.00stdDev



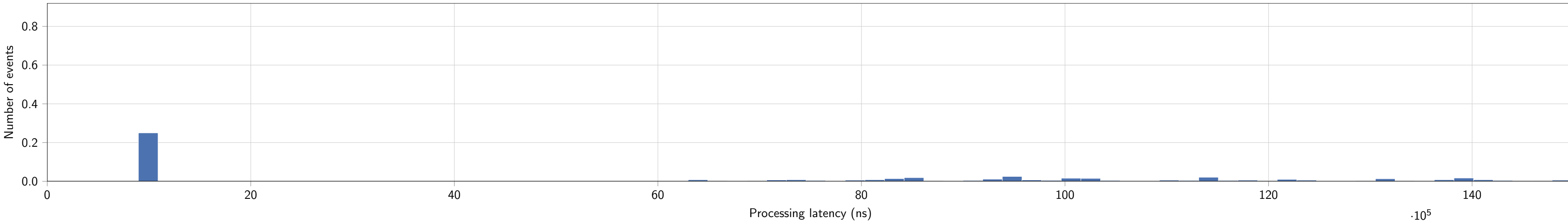
l2\_multimac\_00000100\_mbit3507\_final.histogram.csv: tx: 6.87mpps, 0.04stdDev; rx: 6.87mpps, 0.02stdDev



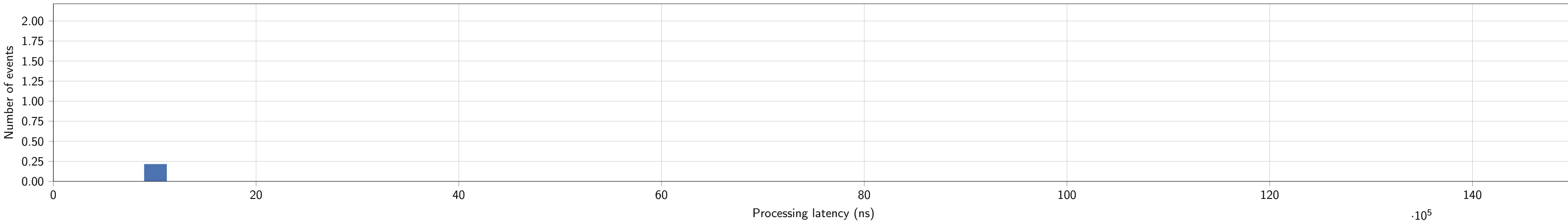
l2\_multimac\_00000100\_mbit3507hires.histogram.csv: tx: 6.87mpps, 0.05stdDev; rx: 6.88mpps, 0.00stdDev



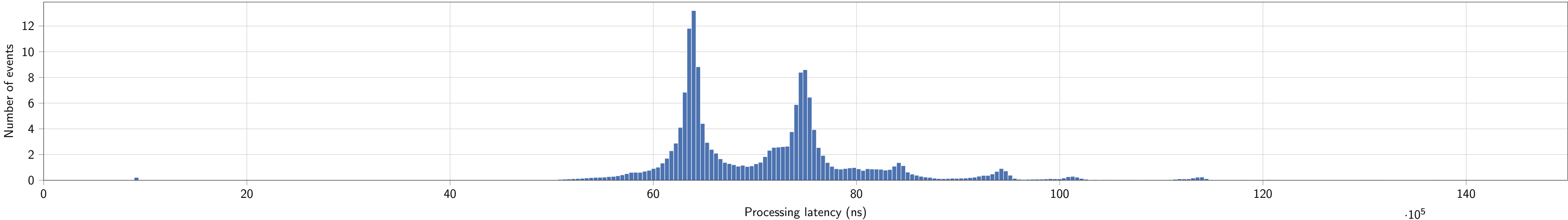
l2\_multimac\_00000100\_mbit3517hires.histogram.csv: tx: 6.90mpps, 0.04stdDev; rx: 6.91mpps, 0.00stdDev



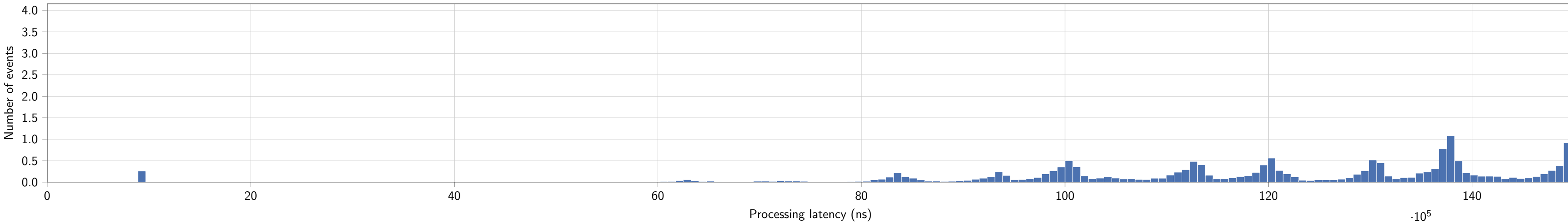
l2\_multimac\_00000100\_mbit3527hires.histogram.csv: tx: 6.90mpps, 0.04stdDev; rx: 6.53mpps, 0.00stdDev



Number of events

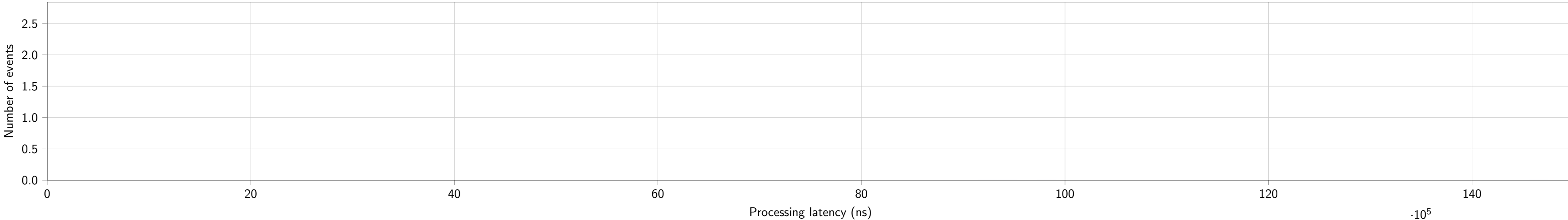
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l2\_multimac\_00000100\_mbit3547hires.histogram.csv: tx: 6.94mpps, 0.05stdDev; rx: 6.95mpps, 0.00stdDev

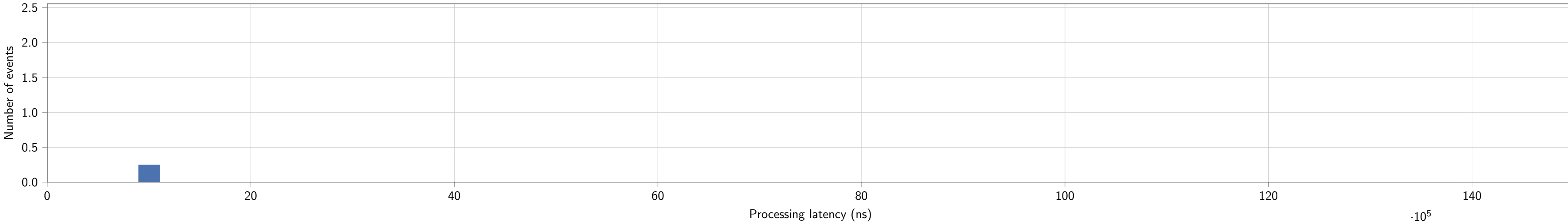




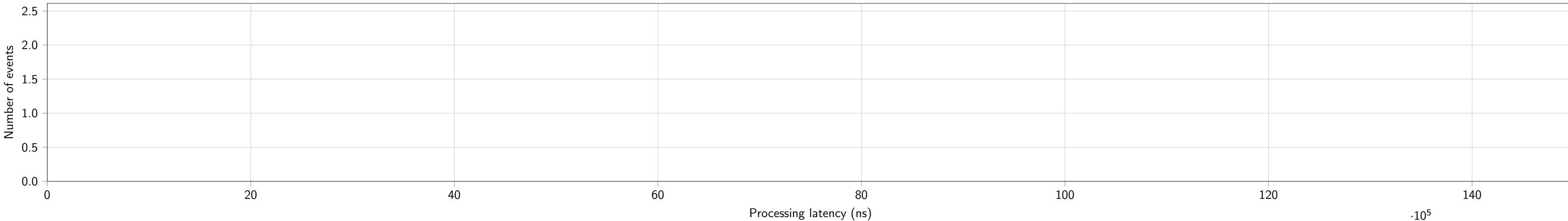
l2\_multimac\_00000100\_mbit3557hires.histogram.csv: tx: 6.97mpps, 0.04stdDev; rx: 6.97mpps, 0.00stdDev



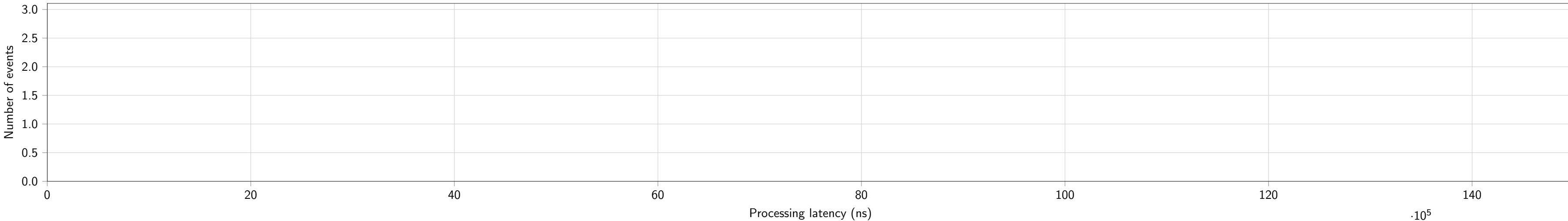
l2\_multimac\_00000100\_mbit3567hires.histogram.csv: tx: 6.97mpps, 0.04stdDev; rx: 6.88mpps, 0.00stdDev



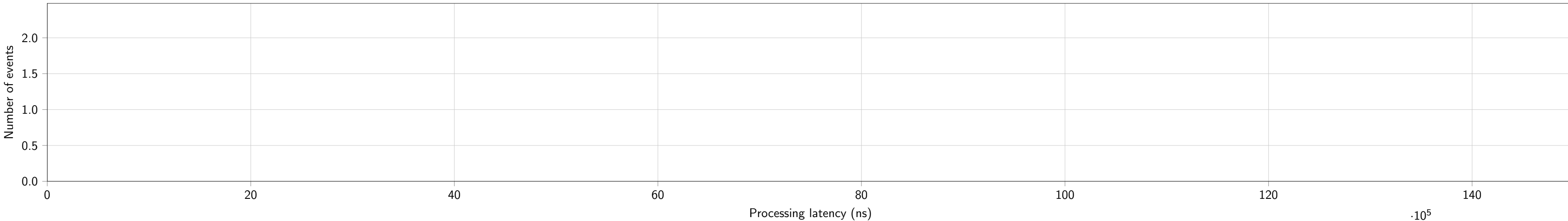
l2\_multimac\_00000100\_mbit3577hires.histogram.csv: tx: 7.01mpps, 0.04stdDev; rx: 6.96mpps, 0.00stdDev



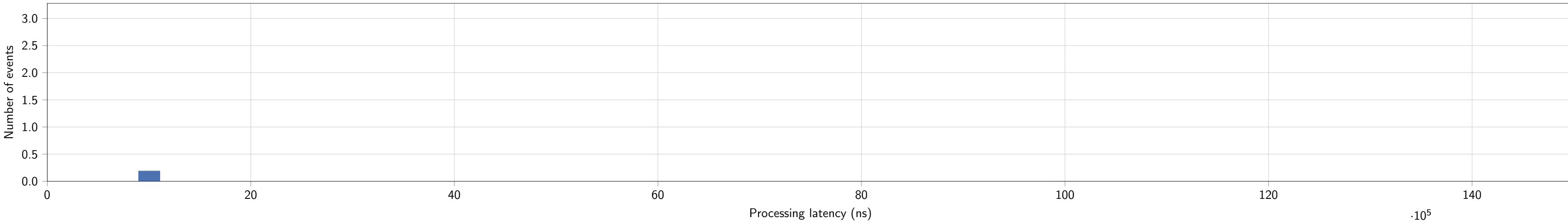
l2\_multimac\_00000100\_mbit3587hires.histogram.csv: tx: 7.01mpps, 0.04stdDev; rx: 6.94mpps, 0.00stdDev



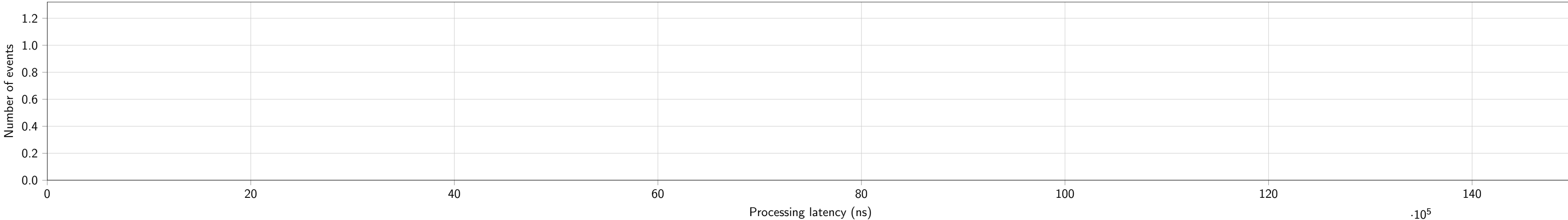
l2\_multimac\_00000100\_mbit3597hires.histogram.csv: tx: 7.05mpps, 0.04stdDev; rx: 6.92mpps, 0.00stdDev



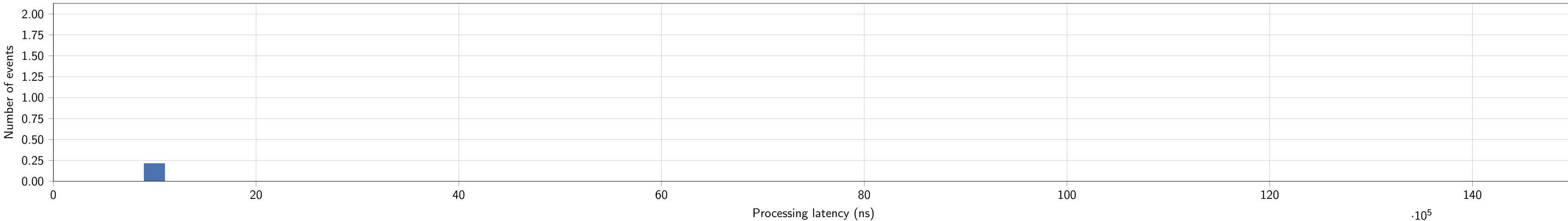
l2\_multimac\_00000100\_mbit3600.histogram.csv: tx: 7.05mpps, 0.04stdDev; rx: 6.97mpps, 0.00stdDev



l2\_multimac\_00000100\_mbit4000.histogram.csv: tx: 7.80mpps, 0.05stdDev; rx: 6.93mpps, 0.00stdDev

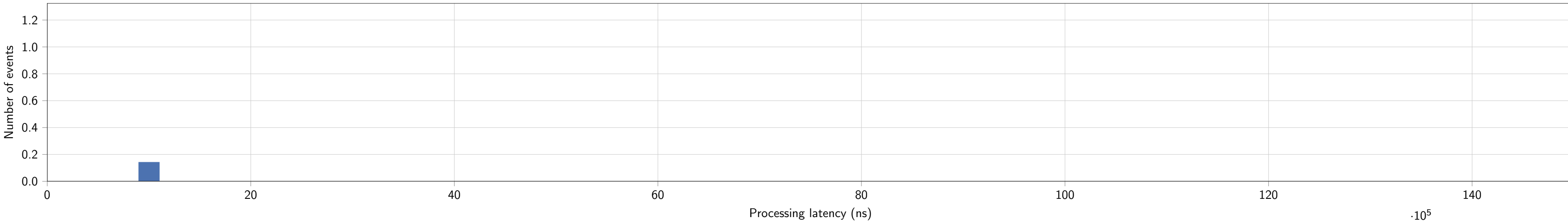


l2\_multimac\_00000100\_mbit4400.histogram.csv: tx: 8.61mpps, 0.05stdDev; rx: 6.97mpps, 0.00stdDev

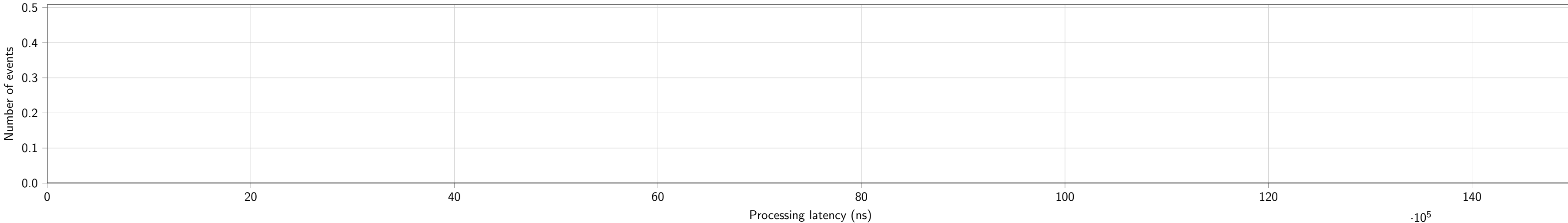




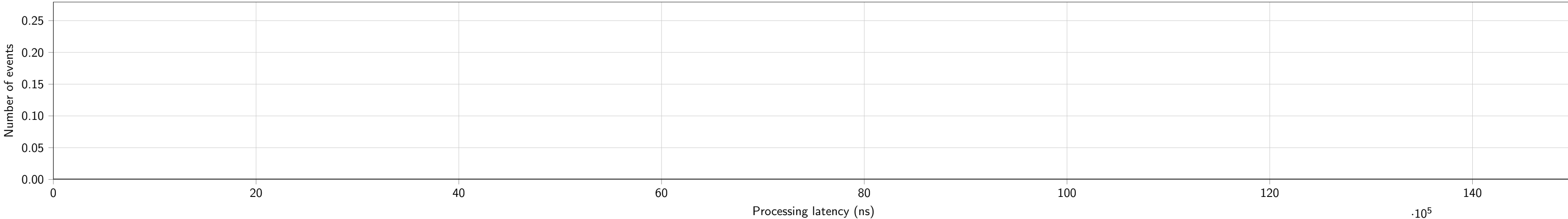
l2\_multimac\_00000100\_mbit4800.histogram.csv: tx: 9.39mpps, 0.05stdDev; rx: 6.94mpps, 0.00stdDev



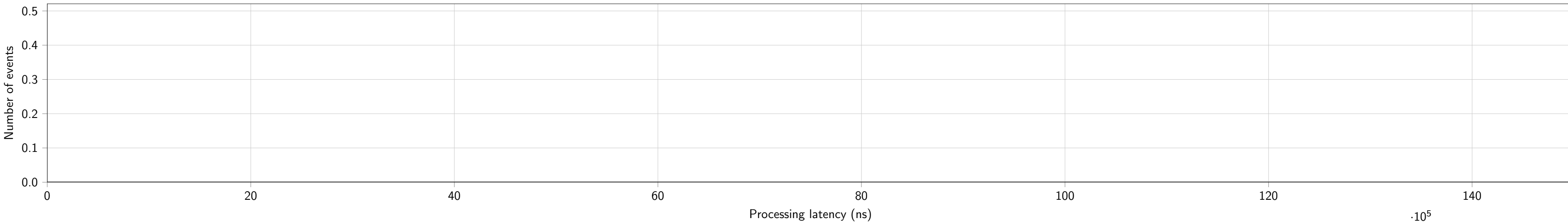
l2\_multimac\_00000100\_mbit5200.histogram.csv: tx: 9.97mpps, 0.05stdDev; rx: 6.95mpps, 0.00stdDev



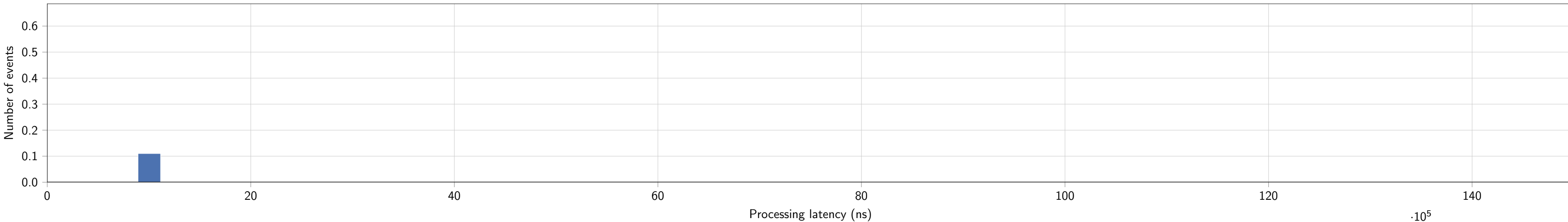
l2\_multimac\_00000100\_mbit5600.histogram.csv: tx: 10.19mpps, 0.05stdDev; rx: 6.95mpps, 0.00stdDev

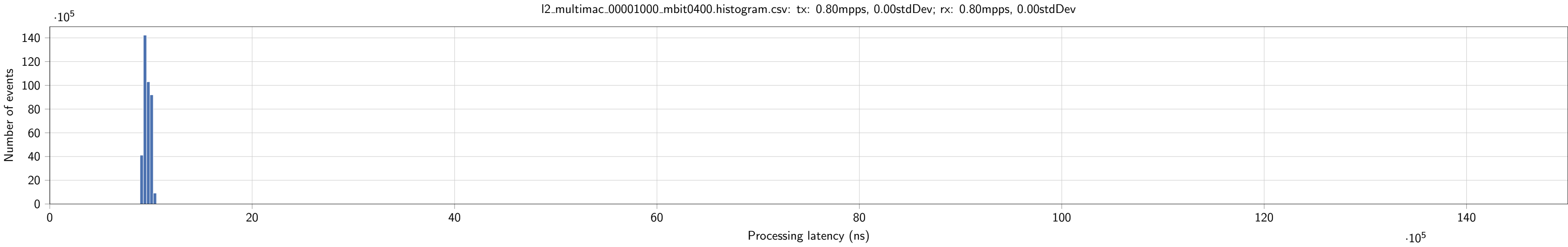


l2\_multimac\_00000100\_mbit6000.histogram.csv: tx: 10.16mpps, 0.05stdDev; rx: 6.97mpps, 0.00stdDev



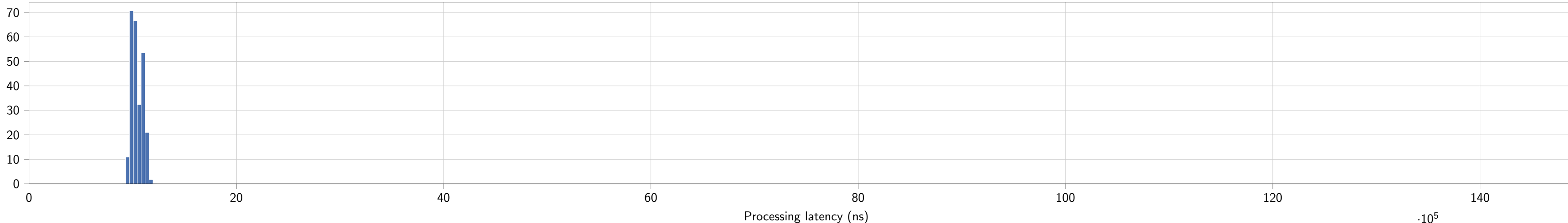
l2\_multimac\_00000100\_mbit9000.histogram.csv: tx: 10.16mpps, 0.05stdDev; rx: 6.93mpps, 0.00stdDev



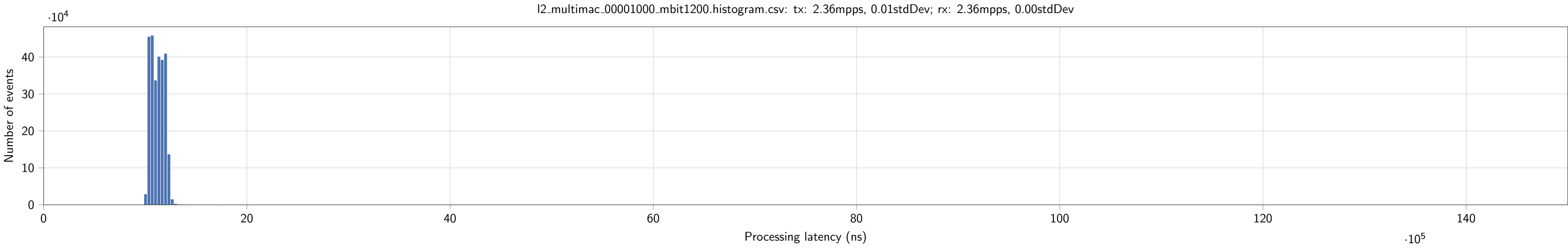


l2\_multimac\_00001000\_mbit0800.histogram.csv: tx: 1.57mpps, 0.01stdDev; rx: 1.58mpps, 0.00stdDev

Number of events

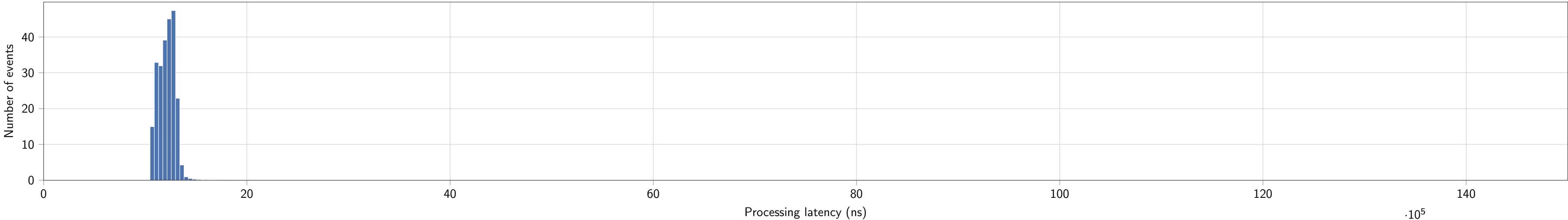


Number of events

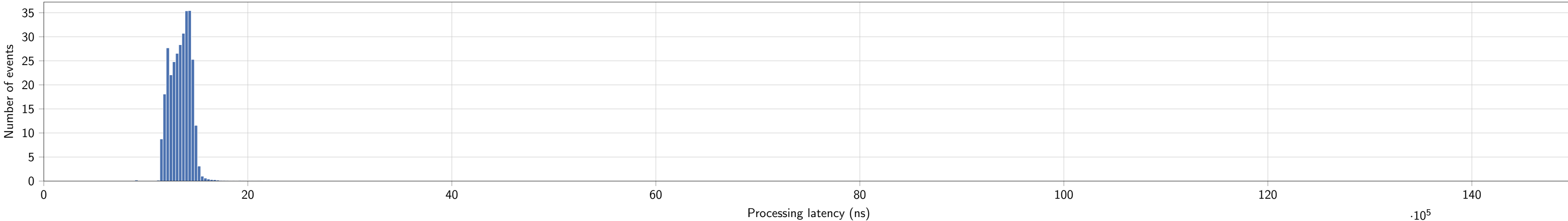


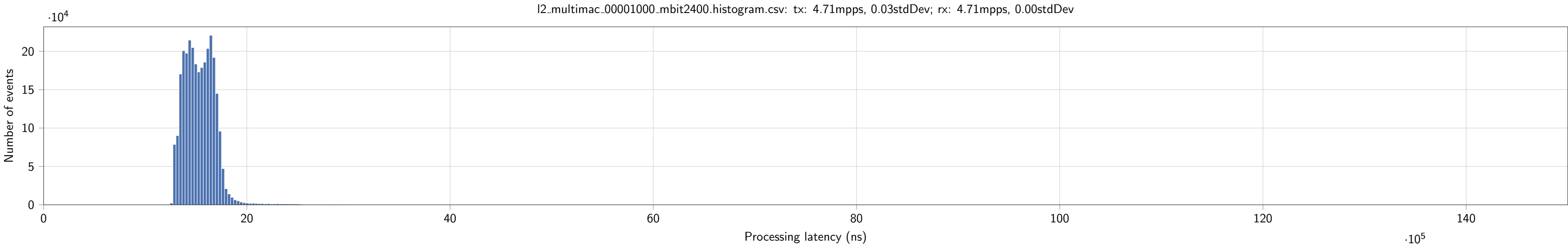


l2\_multimac\_00001000\_mbit1600.histogram.csv: tx: 3.13mpps, 0.02stdDev; rx: 3.14mpps, 0.00stdDev

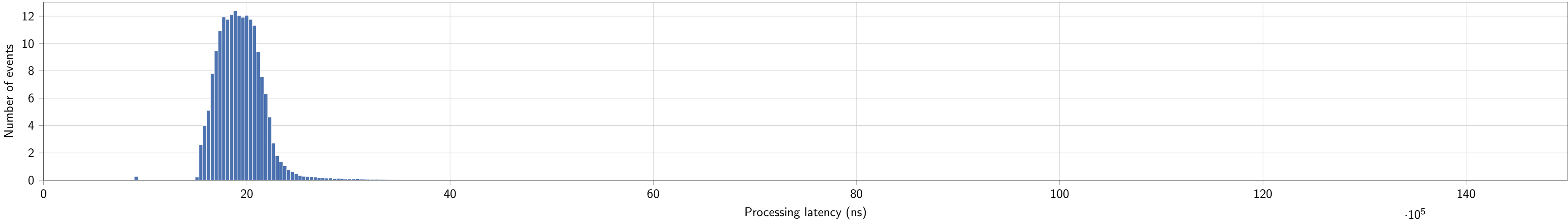


l2\_multimac\_00001000\_mbit2000.histogram.csv: tx: 3.92mpps, 0.02stdDev; rx: 3.92mpps, 0.00stdDev

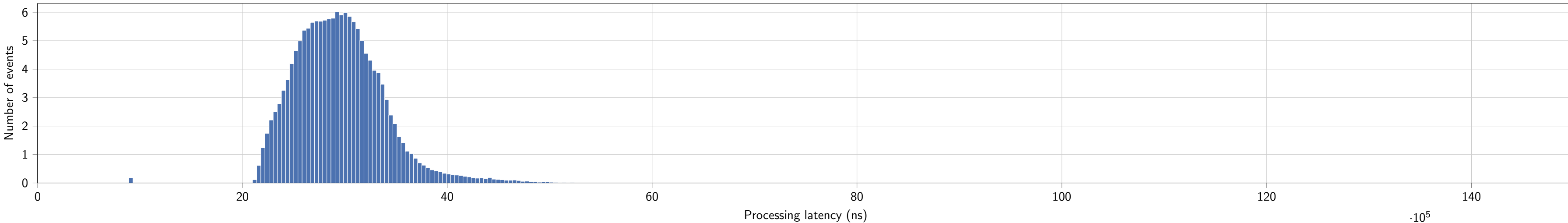




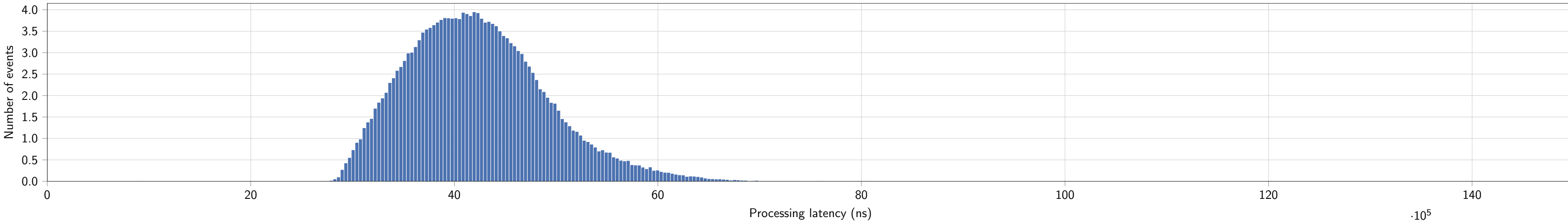
l2\_multimac\_00001000\_mbit2800.histogram.csv: tx: 5.48mpps, 0.04stdDev; rx: 5.49mpps, 0.00stdDev



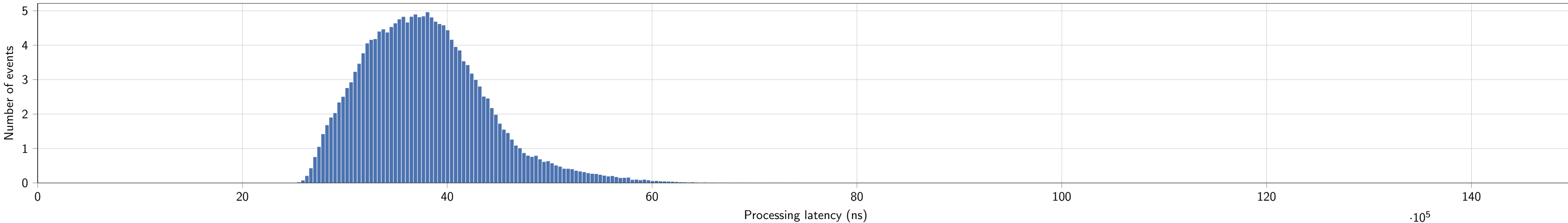
l2\_multimac\_00001000\_mbit3200.histogram.csv: tx: 6.25mpps, 0.04stdDev; rx: 6.26mpps, 0.00stdDev



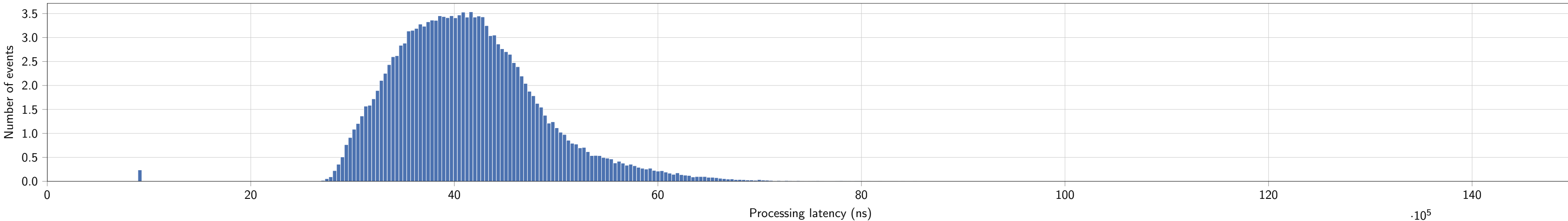
l2\_multimac\_00001000\_mbit3318hires.histogram.csv: tx: 6.51mpps, 0.04stdDev; rx: 6.52mpps, 0.00stdDev



l2\_multimac\_00001000\_mbit3328hires.histogram.csv: tx: 6.51mpps, 0.04stdDev; rx: 6.52mpps, 0.00stdDev

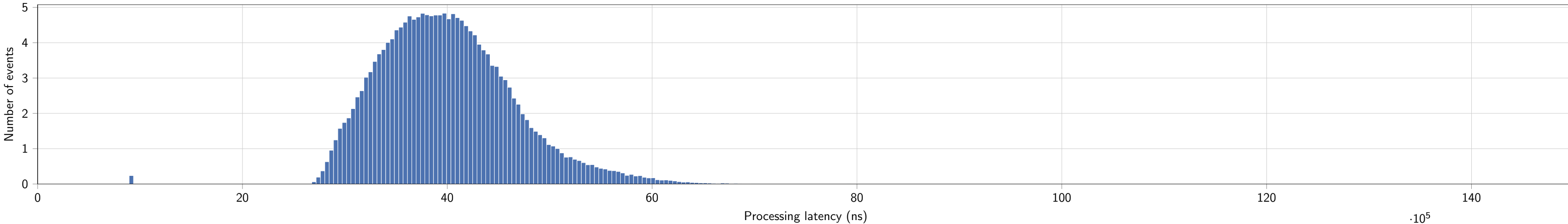


l2\_multimac\_00001000\_mbit3338hires.histogram.csv: tx: 6.54mpps, 0.05stdDev; rx: 6.55mpps, 0.00stdDev

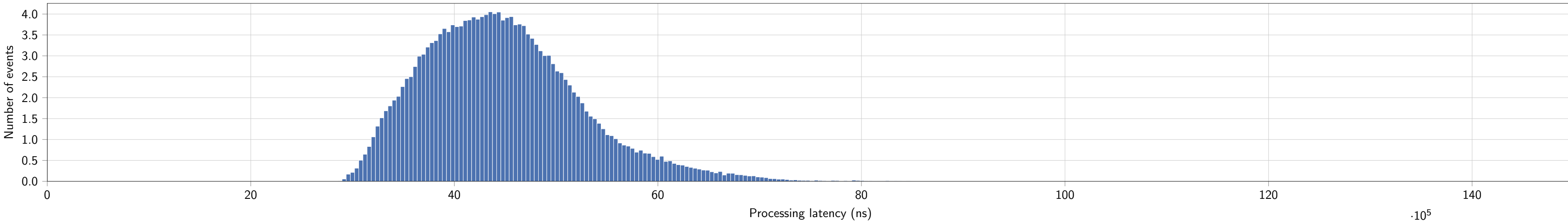




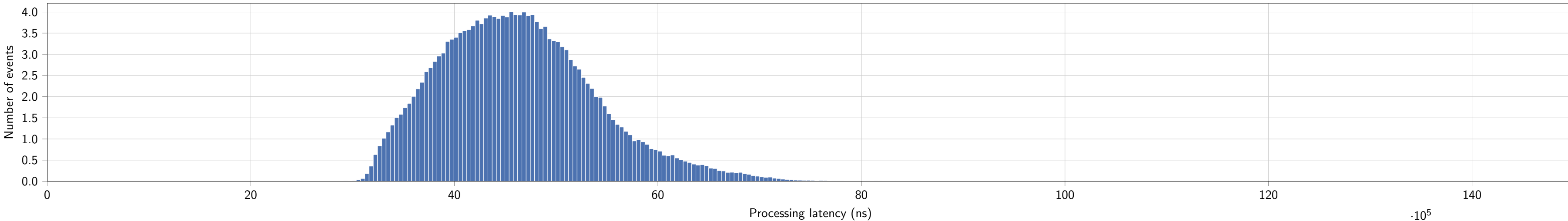
l2\_multimac\_00001000\_mbit3348hires.histogram.csv: tx: 6.54mpps, 0.04stdDev; rx: 6.55mpps, 0.00stdDev



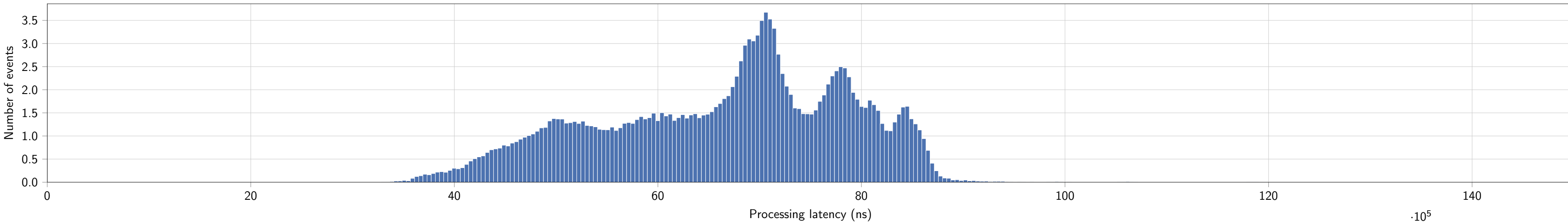
l2\_multimac\_00001000\_mbit3358hires.histogram.csv: tx: 6.58mpps, 0.04stdDev; rx: 6.59mpps, 0.00stdDev



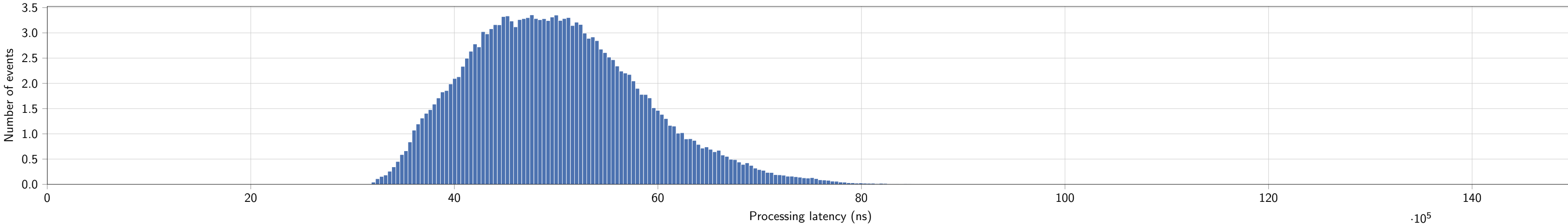
l2\_multimac\_00001000\_mbit3368hires.histogram.csv: tx: 6.58mpps, 0.04stdDev; rx: 6.59mpps, 0.00stdDev



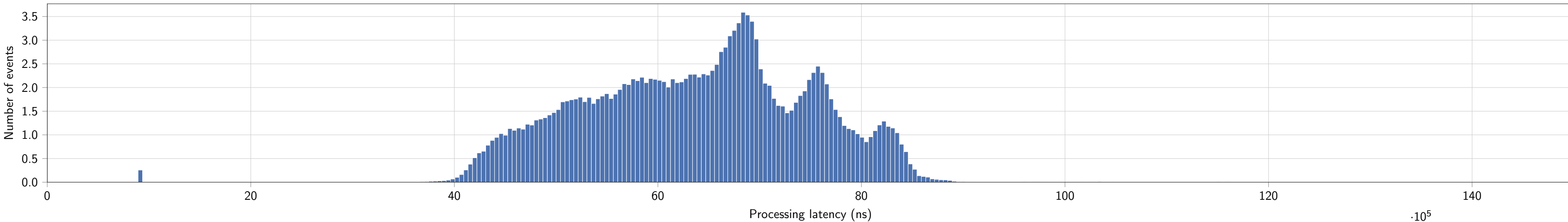
l2\_multimac\_00001000\_mbit3378hires.histogram.csv: tx: 6.61mpps, 0.04stdDev; rx: 6.62mpps, 0.00stdDev



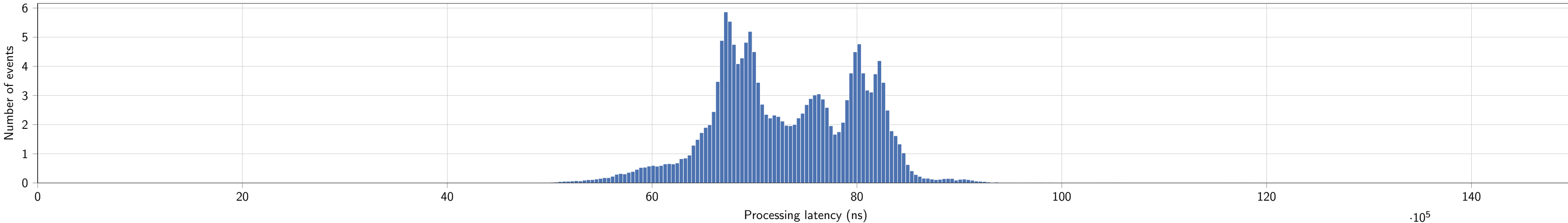
l2\_multimac\_00001000\_mbit3388hires.histogram.csv: tx: 6.65mpps, 0.04stdDev; rx: 6.66mpps, 0.00stdDev



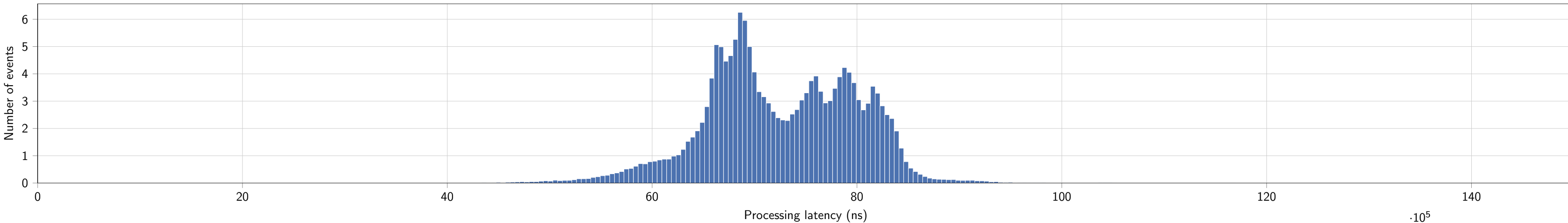
l2\_multimac\_00001000\_mbit3398hires.histogram.csv: tx: 6.65mpps, 0.04stdDev; rx: 6.66mpps, 0.00stdDev



l2\_multimac\_00001000\_mbit3408hires.histogram.csv: tx: 6.68mpps, 0.04stdDev; rx: 6.69mpps, 0.00stdDev

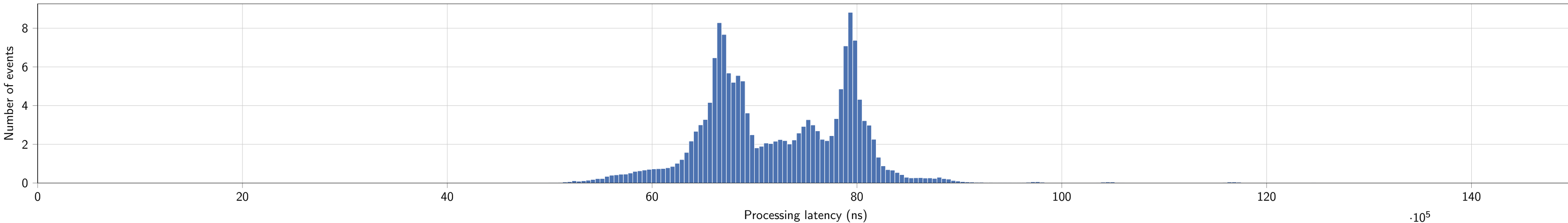


l2\_multimac\_00001000\_mbit3418hires.histogram.csv: tx: 6.68mpps, 0.04stdDev; rx: 6.69mpps, 0.00stdDev

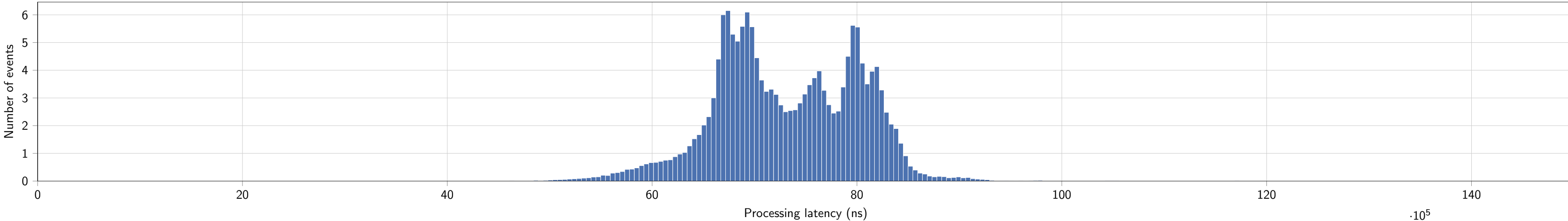




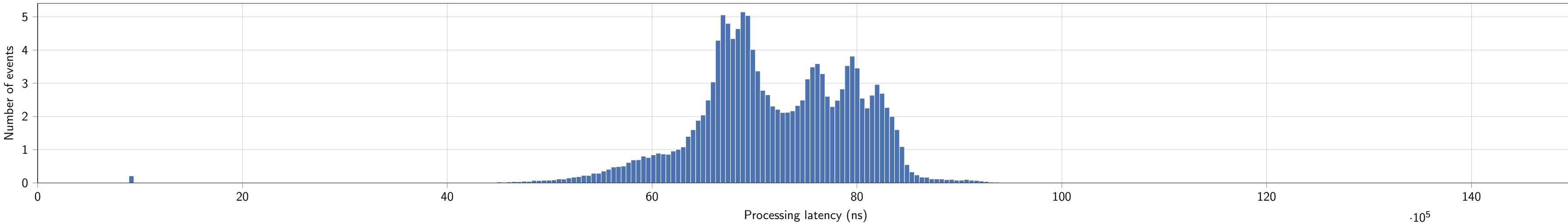
l2\_multimac\_00001000\_mbit3428hires.histogram.csv: tx: 6.72mpps, 0.04stdDev; rx: 6.73mpps, 0.00stdDev



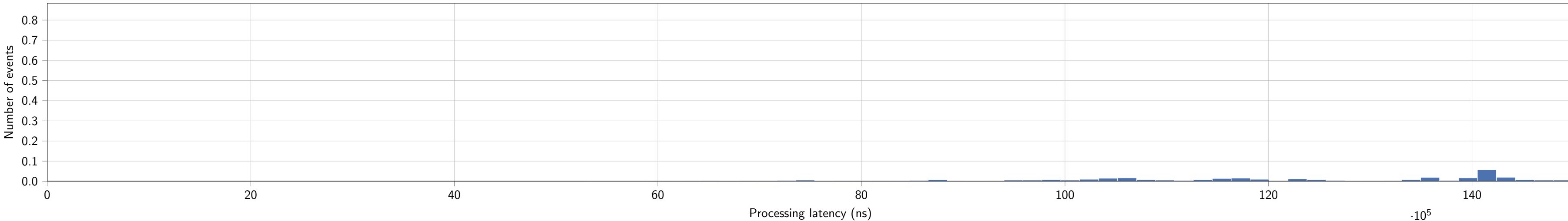
l2\_multimac\_00001000\_mbit3438\_final.histogram.csv: tx: 6.72mpps, 0.04stdDev; rx: 6.73mpps, 0.00stdDev



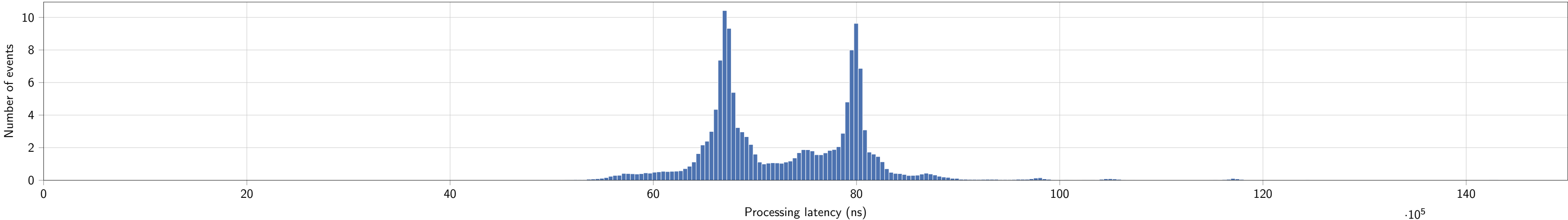
l2\_multimac\_00001000\_mbit3438hires.histogram.csv: tx: 6.72mpps, 0.05stdDev; rx: 6.73mpps, 0.00stdDev



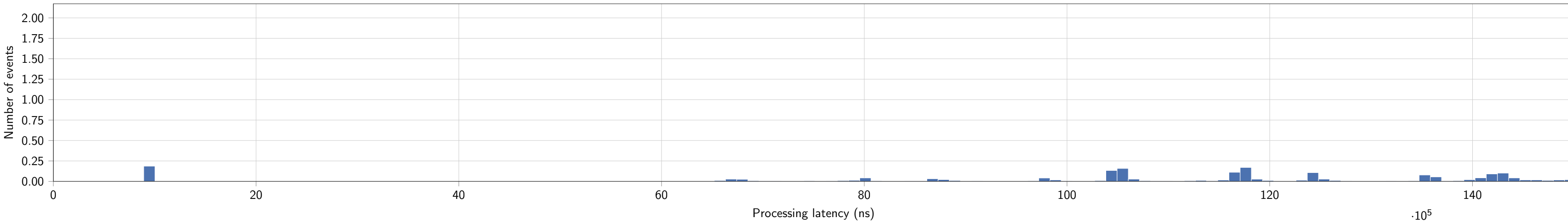
l2\_multimac\_00001000\_mbit3448hires.histogram.csv: tx: 6.75mpps, 0.04stdDev; rx: 6.76mpps, 0.00stdDev



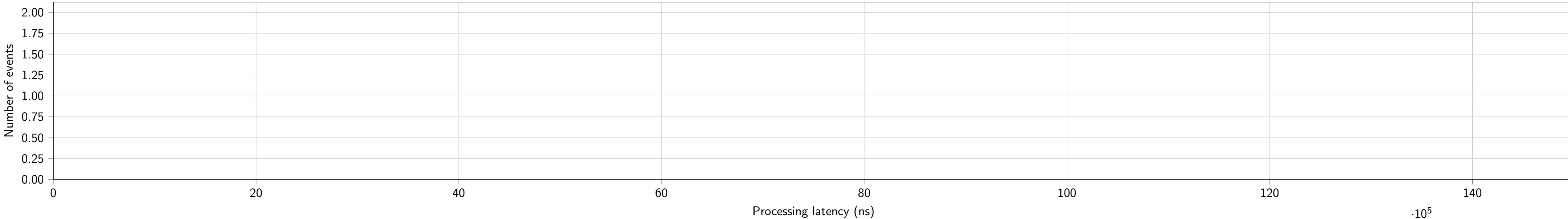
l2\_multimac\_00001000\_mbit3458hires.histogram.csv: tx: 6.75mpps, 0.05stdDev; rx: 6.77mpps, 0.00stdDev



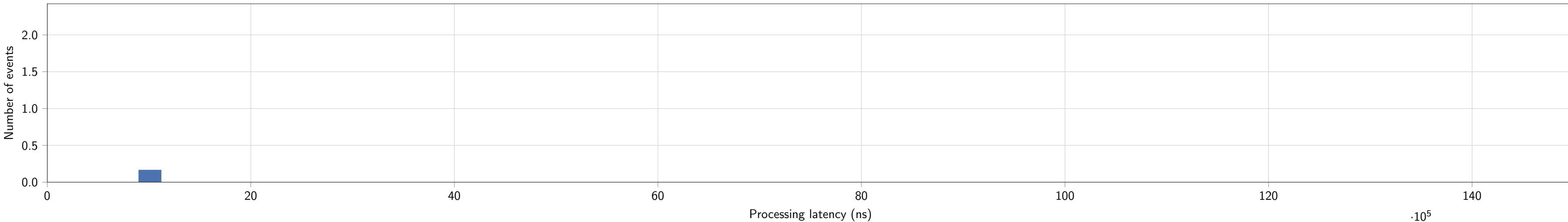
l2\_multimac\_00001000\_mbit3468hires.histogram.csv: tx: 6.79mpps, 0.04stdDev; rx: 6.80mpps, 0.00stdDev



l2\_multimac\_00001000\_mbit3600.histogram.csv: tx: 7.05mpps, 0.04stdDev; rx: 6.73mpps, 0.00stdDev

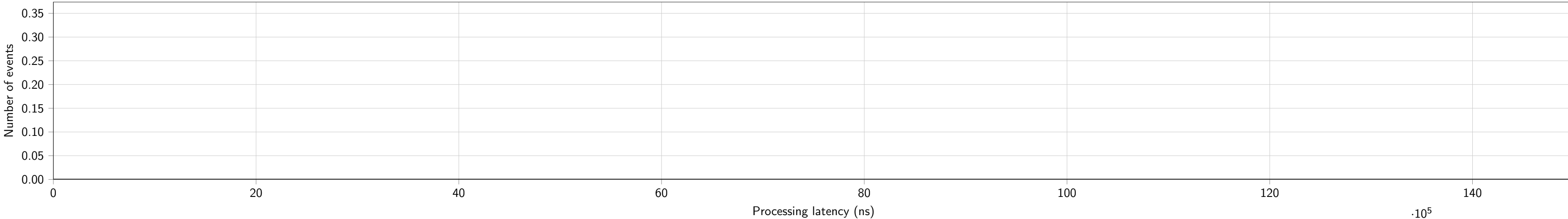


l2\_multimac\_00001000\_mbit4000.histogram.csv: tx: 7.80mpps, 0.05stdDev; rx: 6.78mpps, 0.00stdDev

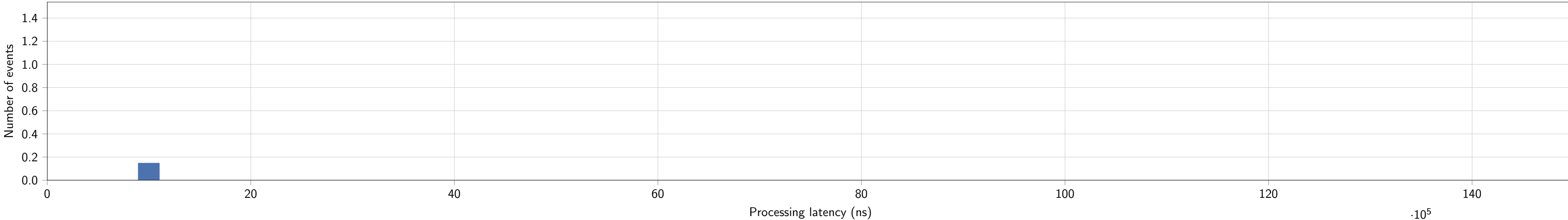




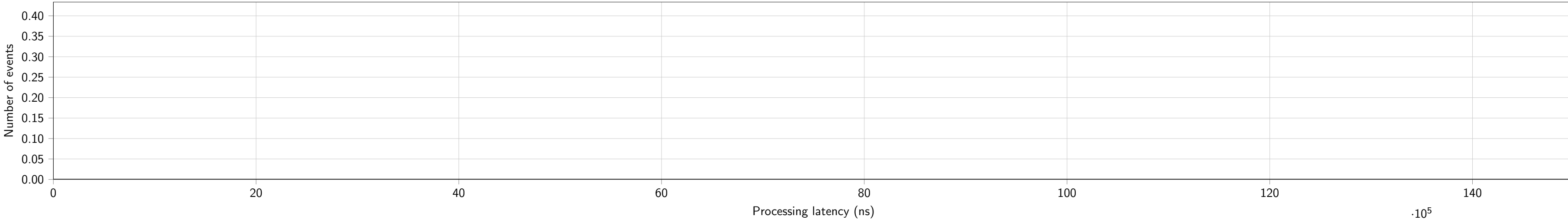
l2\_multimac\_00001000\_mbit4400.histogram.csv: tx: 8.61mpps, 0.05stdDev; rx: 6.77mpps, 0.00stdDev



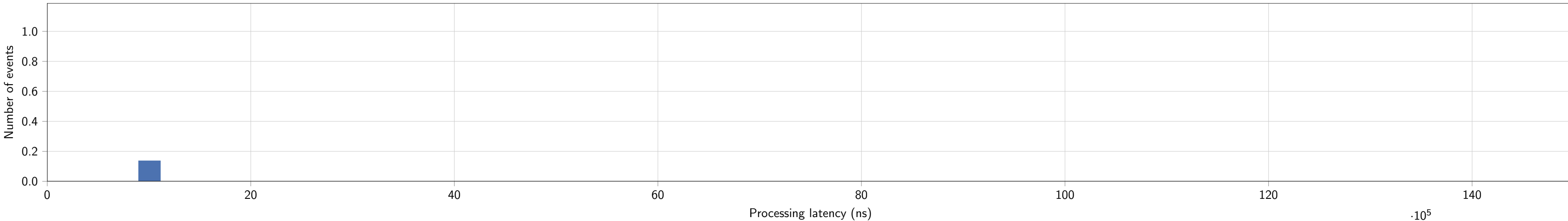
l2\_multimac\_00001000\_mbit4800.histogram.csv: tx: 9.39mpps, 0.05stdDev; rx: 6.78mpps, 0.00stdDev



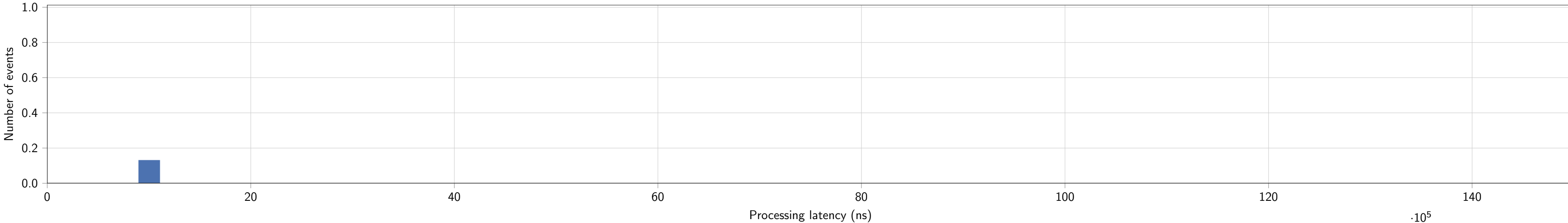
l2\_multimac\_00001000\_mbit5200.histogram.csv: tx: 10.11mpps, 0.06stdDev; rx: 6.78mpps, 0.00stdDev



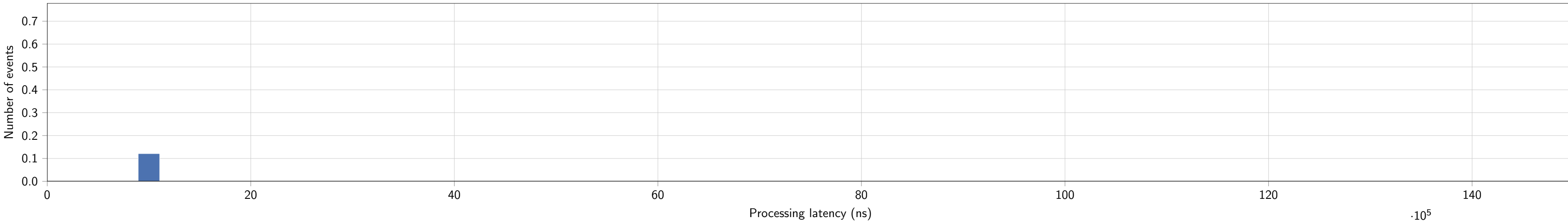
l2\_multimac\_00001000\_mbit5600.histogram.csv: tx: 10.18mpps, 0.05stdDev; rx: 6.76mpps, 0.00stdDev

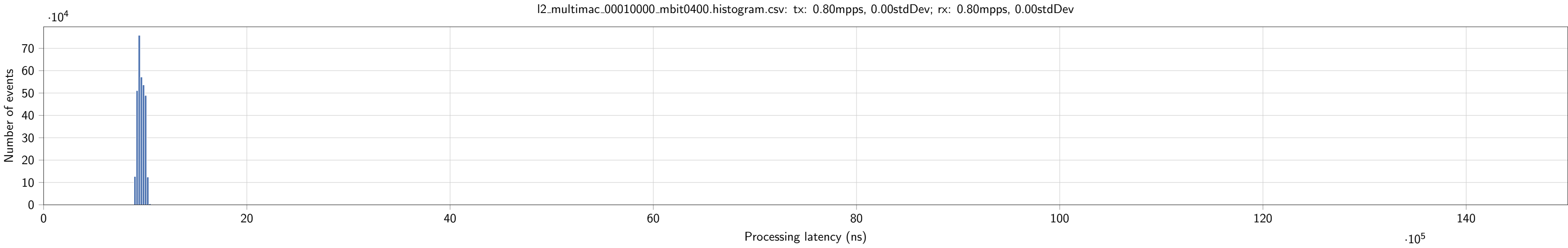


l2\_multimac\_00001000\_mbit6000.histogram.csv: tx: 9.98mpps, 0.05stdDev; rx: 6.76mpps, 0.00stdDev



l2\_multimac\_00001000\_mbit9000.histogram.csv: tx: 10.13mpps, 0.05stdDev; rx: 6.68mpps, 0.00stdDev





l2\_multimac\_00010000\_mbit0800.histogram.csv: tx: 1.58mpps, 0.01stdDev; rx: 1.58mpps, 0.00stdDev

Number of events

30  
25  
20  
15  
10  
5  
0

$\cdot 10^4$

0

20

40

60

80

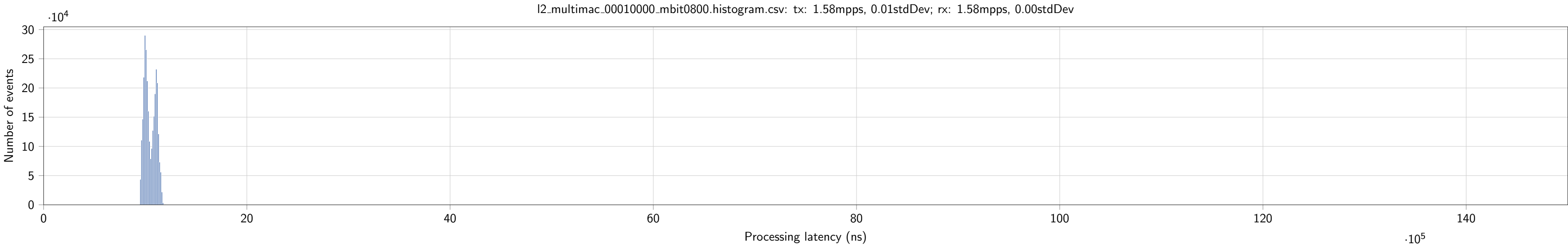
100

120

140

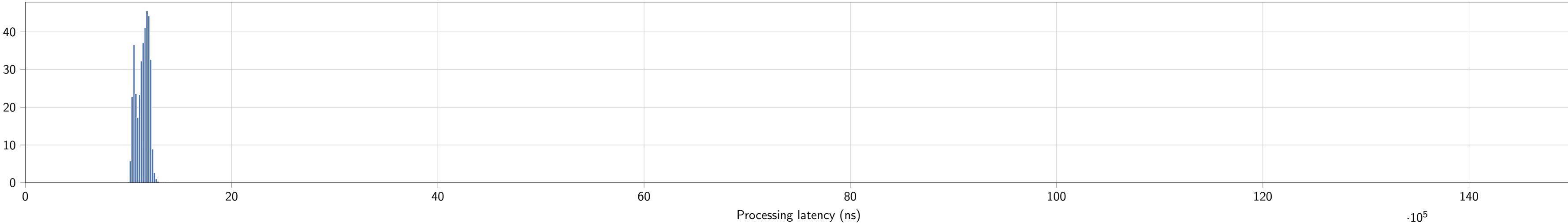
Processing latency (ns)

$\cdot 10^5$

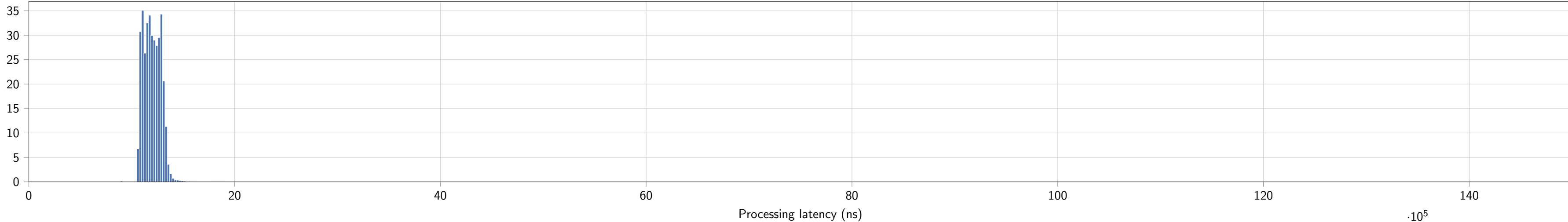


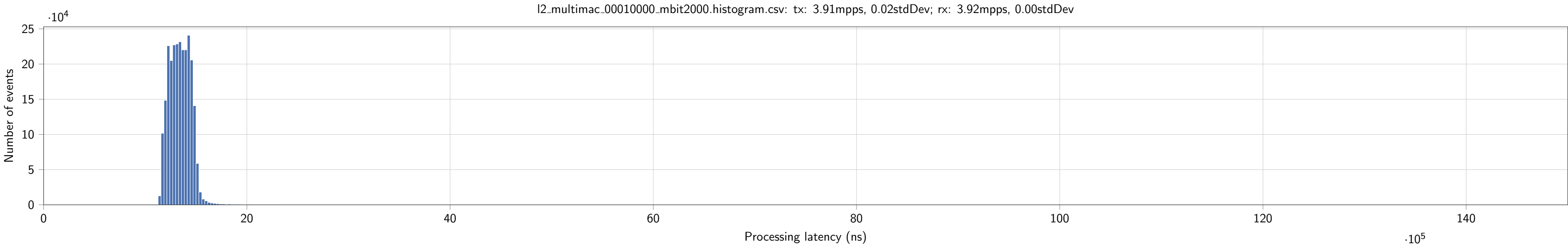


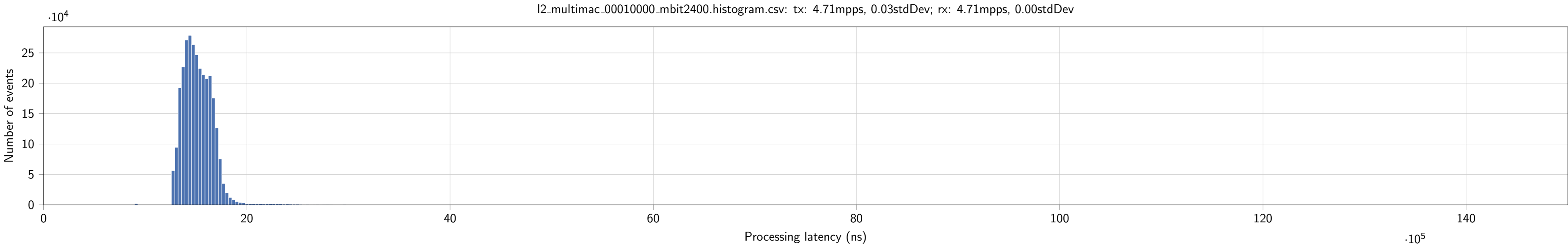
Number of events

 $\cdot 10^4$ 

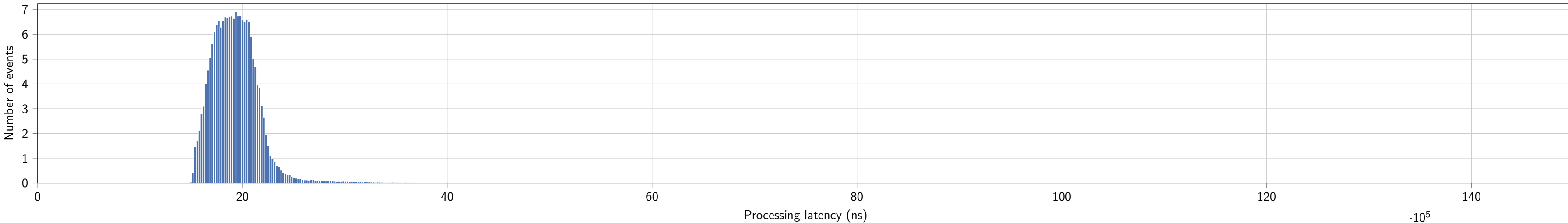
Number of events

 $\cdot 10^4$ 

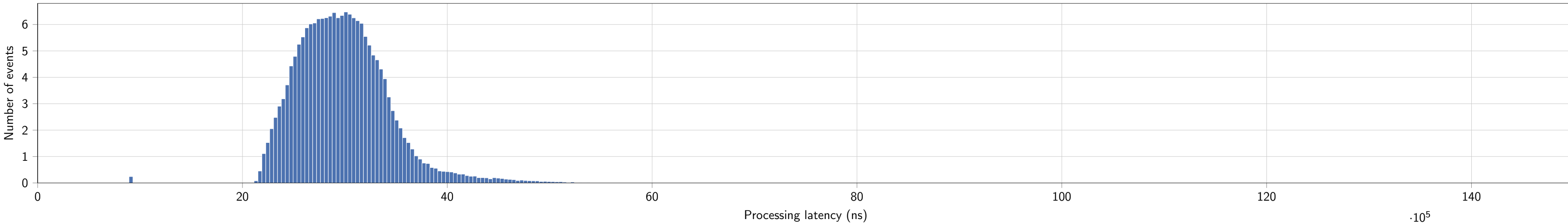




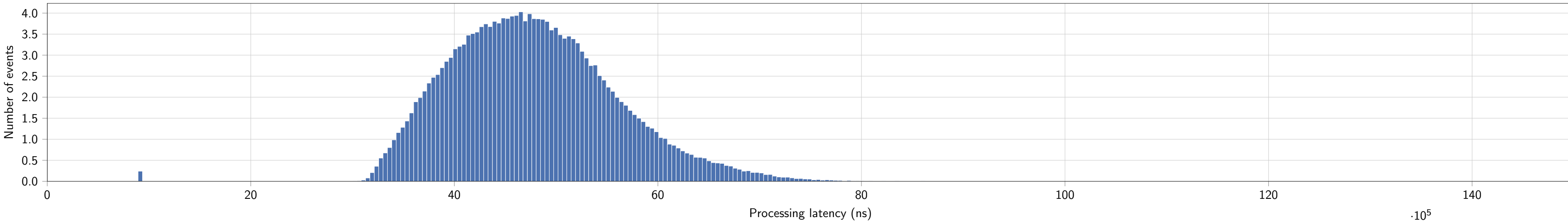
l2\_multimac\_00010000\_mbit2800.histogram.csv: tx: 5.48mpps, 0.03stdDev; rx: 5.49mpps, 0.00stdDev



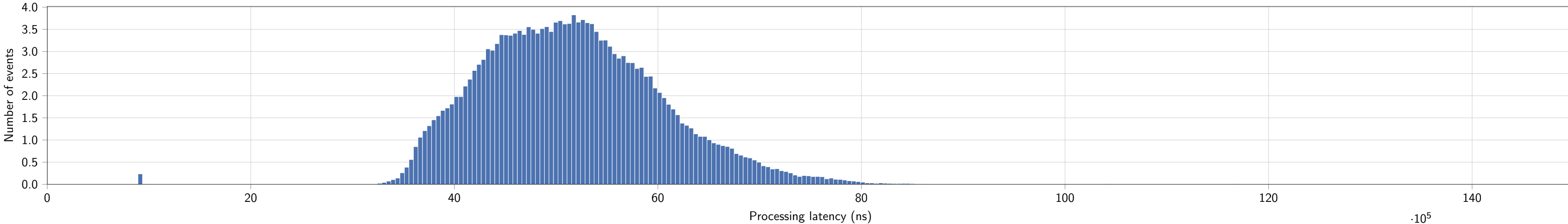
l2\_multimac\_00010000\_mbit3200.histogram.csv: tx: 6.25mpps, 0.04stdDev; rx: 6.26mpps, 0.00stdDev



l2\_multimac\_00010000\_mbit3375hires.histogram.csv: tx: 6.61mpps, 0.04stdDev; rx: 6.62mpps, 0.00stdDev

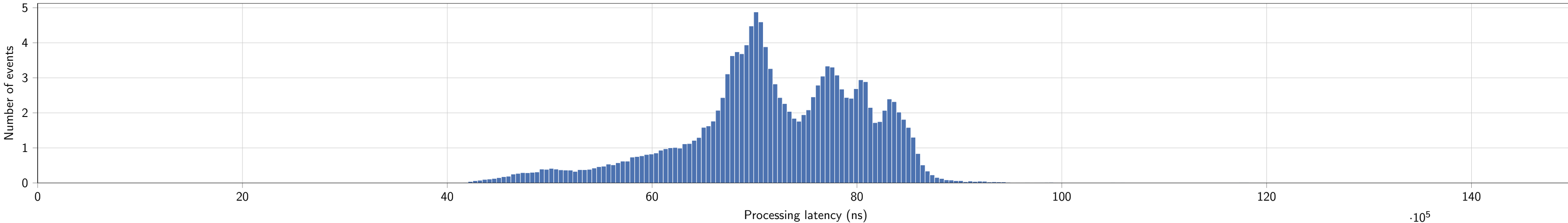


l2\_multimac\_00010000\_mbit3385hires.histogram.csv: tx: 6.61mpps, 0.04stdDev; rx: 6.62mpps, 0.00stdDev

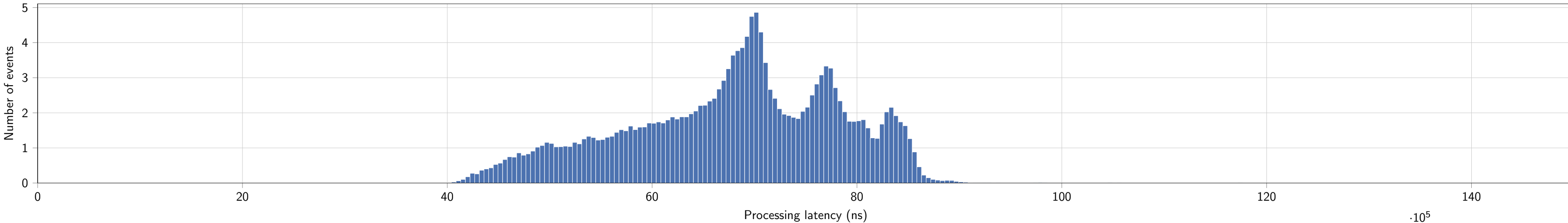




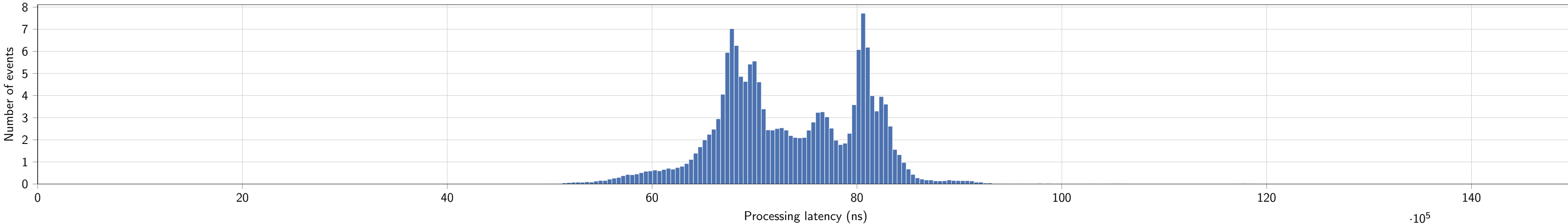
l2\_multimac\_00010000\_mbit3395hires.histogram.csv: tx: 6.65mpps, 0.05stdDev; rx: 6.66mpps, 0.00stdDev



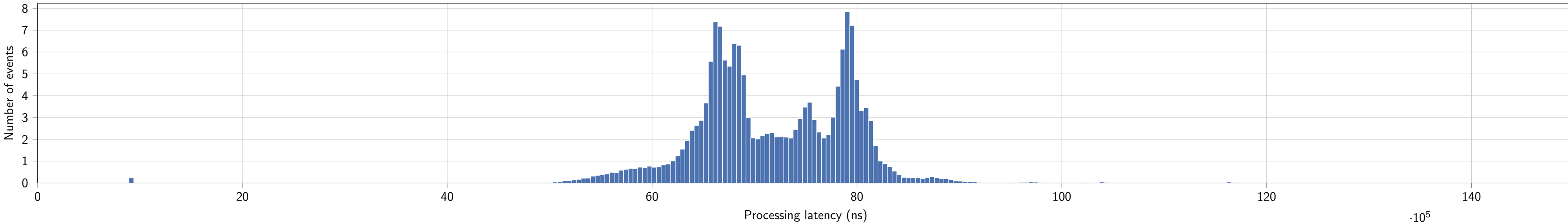
l2\_multimac\_00010000\_mbit3405hires.histogram.csv: tx: 6.68mpps, 0.04stdDev; rx: 6.69mpps, 0.00stdDev



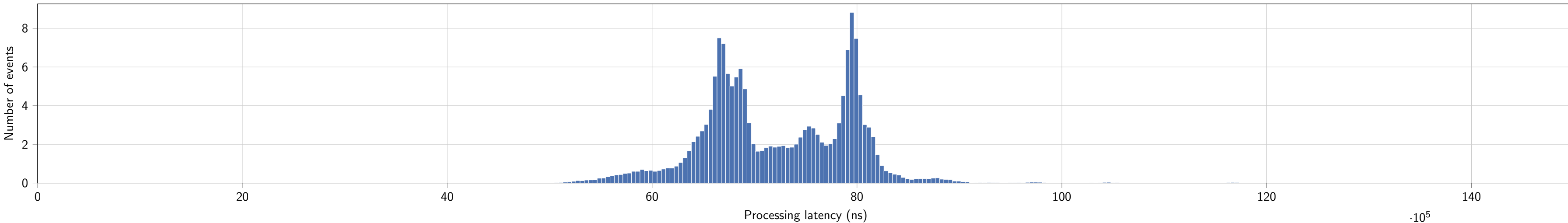
l2\_multimac\_00010000\_mbit3415hires.histogram.csv: tx: 6.68mpps, 0.04stdDev; rx: 6.69mpps, 0.00stdDev



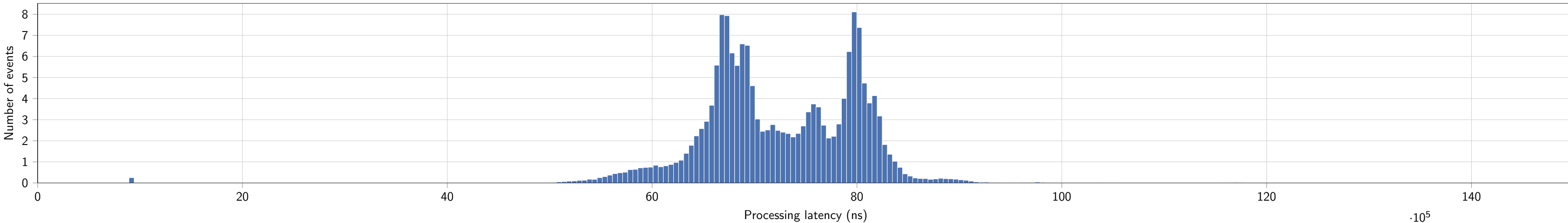
l2\_multimac\_00010000\_mbit3425hires.histogram.csv: tx: 6.72mpps, 0.04stdDev; rx: 6.73mpps, 0.00stdDev



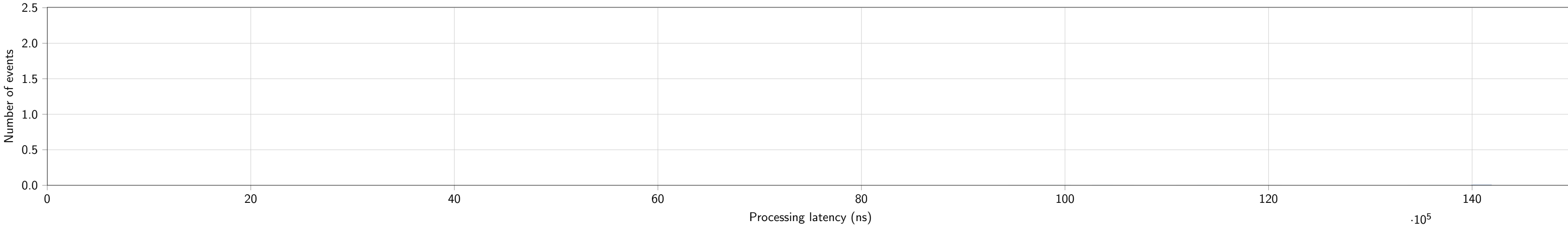
l2\_multimac\_00010000\_mbit3435\_final.histogram.csv: tx: 6.72mpps, 0.04stdDev; rx: 6.73mpps, 0.00stdDev



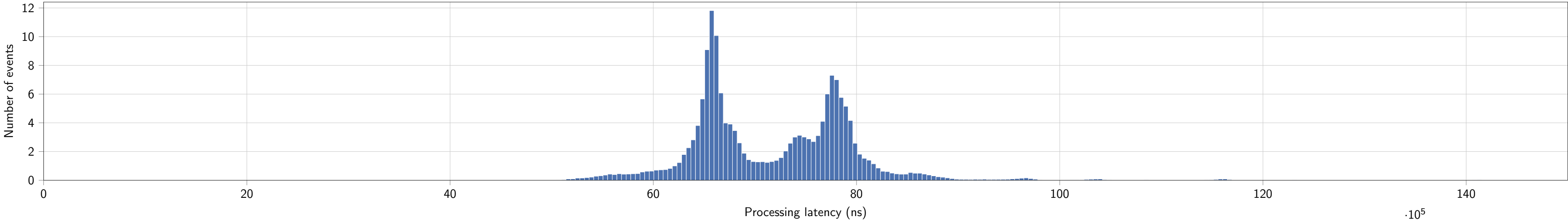
l2\_multimac\_00010000\_mbit3435hires.histogram.csv: tx: 6.72mpps, 0.04stdDev; rx: 6.73mpps, 0.00stdDev



l2\_multimac\_00010000\_mbit3445hires.histogram.csv: tx: 6.75mpps, 0.04stdDev; rx: 6.73mpps, 0.00stdDev

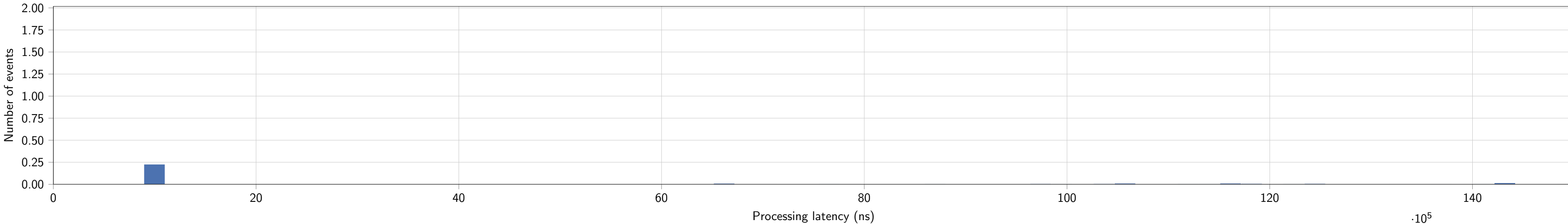


l2\_multimac\_00010000\_mbit3455hires.histogram.csv: tx: 6.76mpps, 0.04stdDev; rx: 6.77mpps, 0.00stdDev

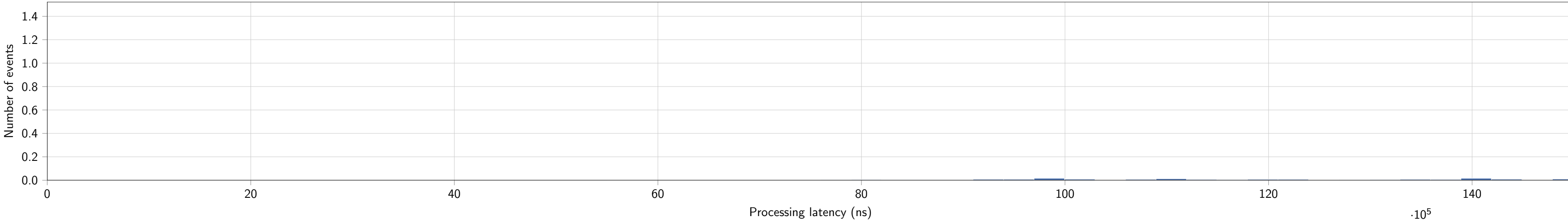




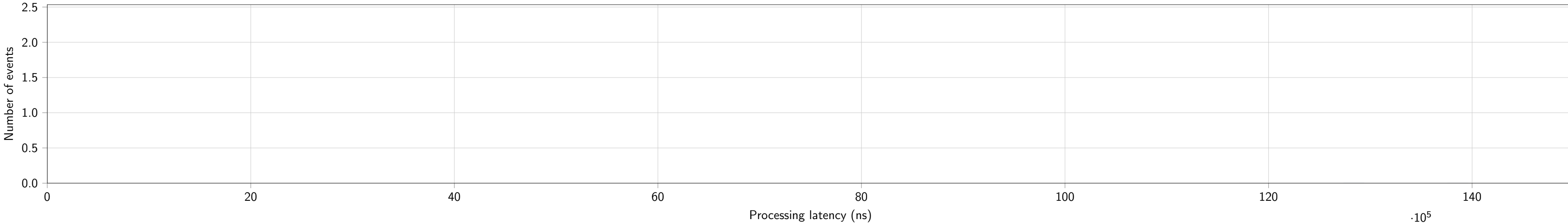
l2\_multimac\_00010000\_mbit3465hires.histogram.csv: tx: 6.78mpps, 0.04stdDev; rx: 6.79mpps, 0.00stdDev



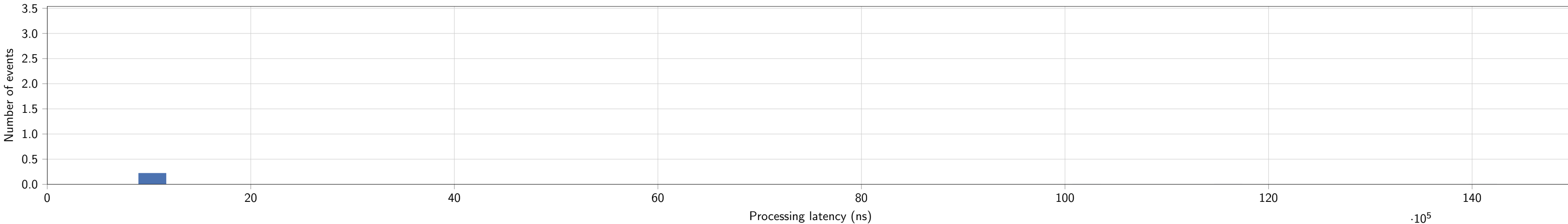
l2\_multimac\_00010000\_mbit3475hires.histogram.csv: tx: 6.78mpps, 0.05stdDev; rx: 6.79mpps, 0.00stdDev



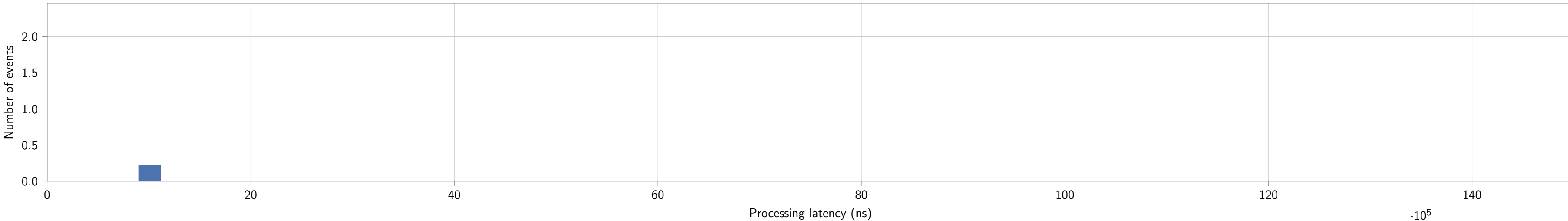
l2\_multimac\_00010000\_mbit3485hires.histogram.csv: tx: 6.82mpps, 0.04stdDev; rx: 6.79mpps, 0.00stdDev



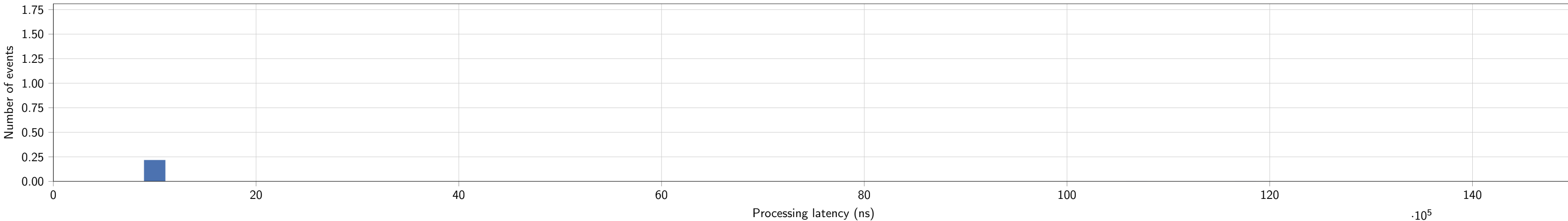
l2\_multimac\_00010000\_mbit3495hires.histogram.csv: tx: 6.82mpps, 0.04stdDev; rx: 6.79mpps, 0.00stdDev



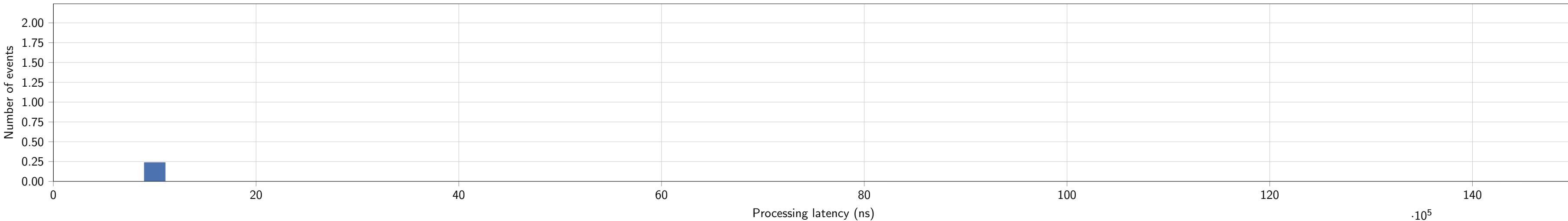
l2\_multimac\_00010000\_mbit3505hires.histogram.csv: tx: 6.86mpps, 0.04stdDev; rx: 6.71mpps, 0.00stdDev



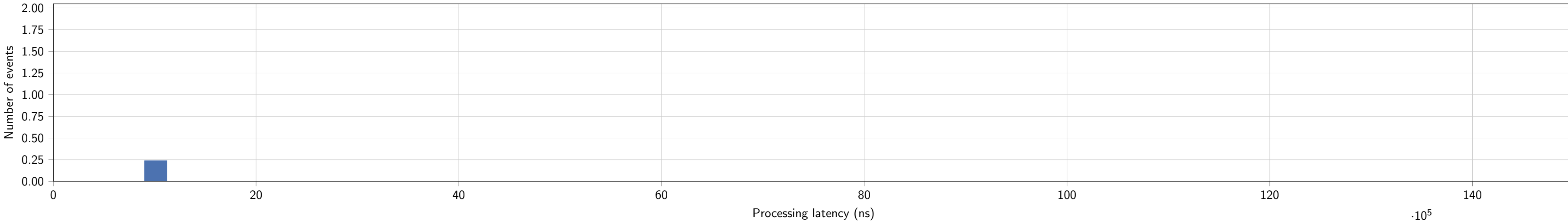
l2\_multimac\_00010000\_mbit3515hires.histogram.csv: tx: 6.86mpps, 0.05stdDev; rx: 6.72mpps, 0.00stdDev



l2\_multimac\_00010000\_mbit3525hires.histogram.csv: tx: 6.90mpps, 0.04stdDev; rx: 6.80mpps, 0.00stdDev

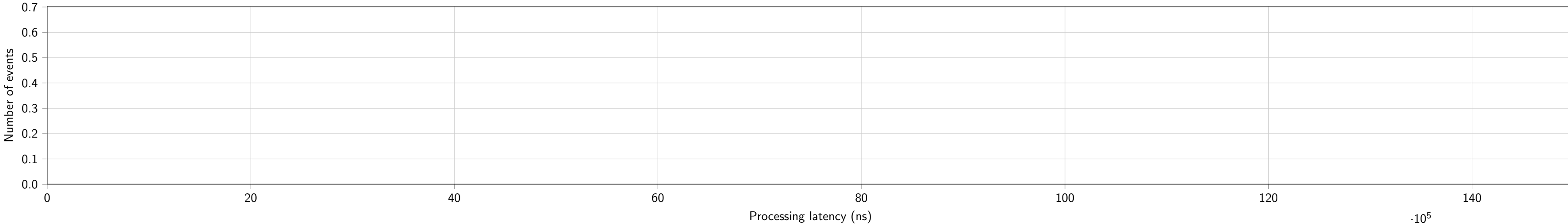


l2\_multimac\_00010000\_mbit3600.histogram.csv: tx: 7.05mpps, 0.04stdDev; rx: 6.61mpps, 0.00stdDev

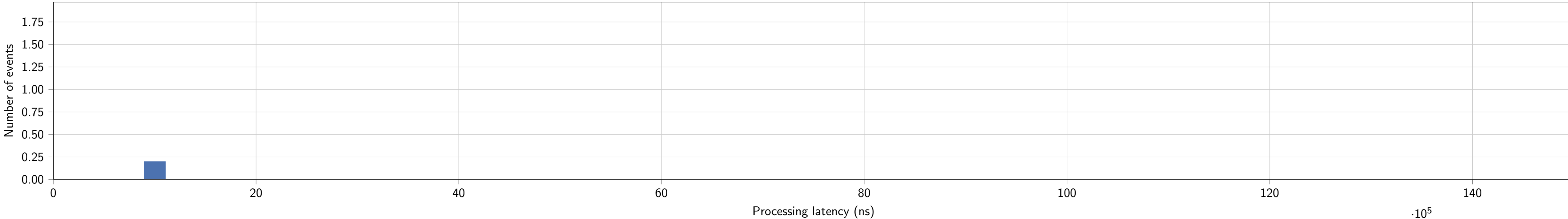




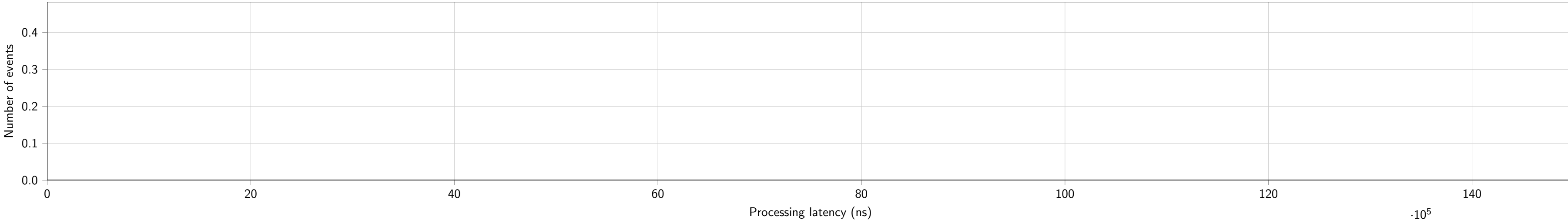
l2\_multimac\_00010000\_mbit4000.histogram.csv: tx: 7.80mpps, 0.05stdDev; rx: 6.78mpps, 0.00stdDev



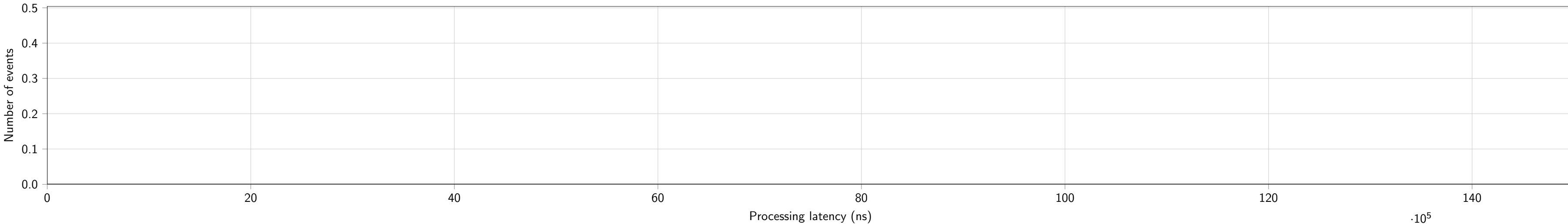
l2\_multimac\_00010000\_mbit4400.histogram.csv: tx: 8.61mpps, 0.05stdDev; rx: 6.72mpps, 0.00stdDev



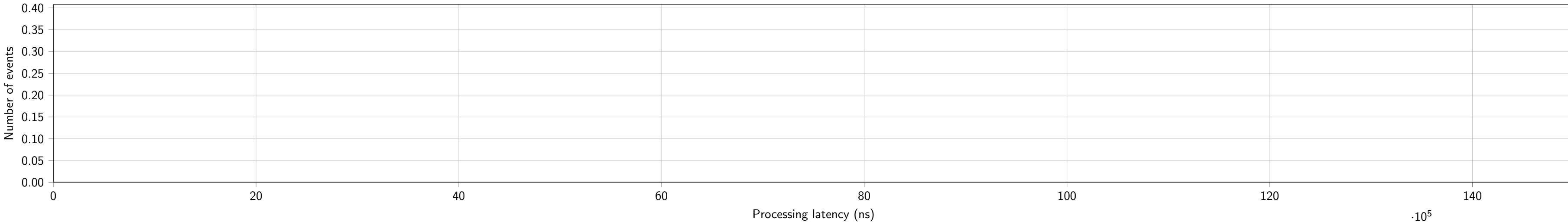
l2\_multimac\_00010000\_mbit4800.histogram.csv: tx: 9.39mpps, 0.05stdDev; rx: 6.74mpps, 0.00stdDev



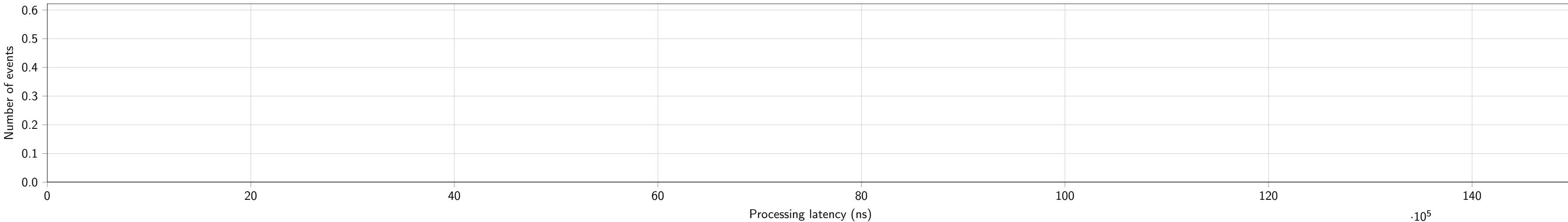
l2\_multimac\_00010000\_mbit5200.histogram.csv: tx: 10.10mpps, 0.05stdDev; rx: 6.78mpps, 0.00stdDev



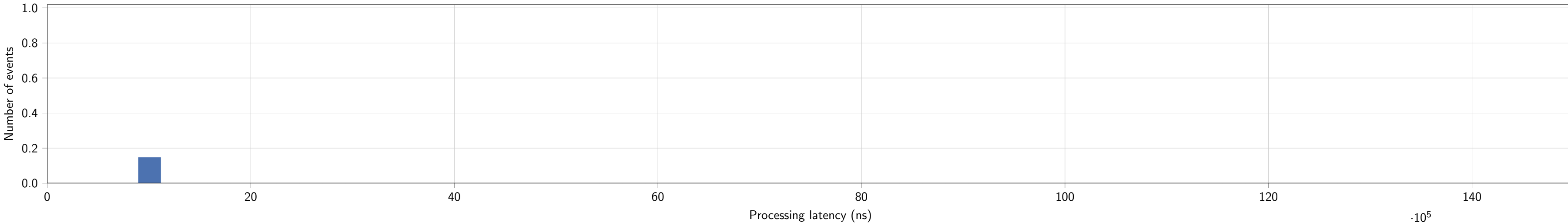
l2\_multimac\_00010000\_mbit5600.histogram.csv: tx: 10.14mpps, 0.05stdDev; rx: 6.77mpps, 0.00stdDev

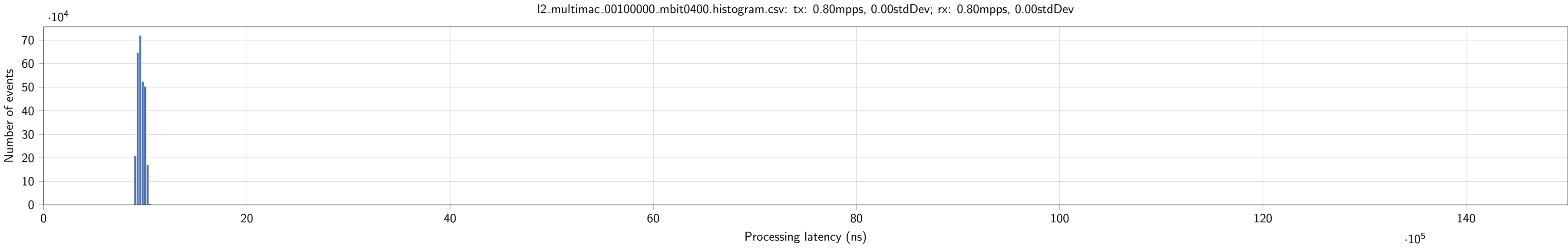


l2\_multimac\_00010000\_mbit6000.histogram.csv: tx: 10.15mpps, 0.05stdDev; rx: 6.74mpps, 0.00stdDev

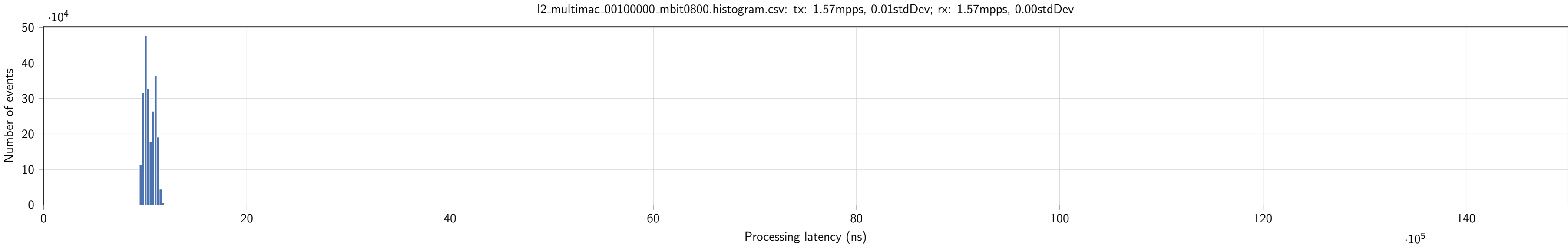


l2\_multimac\_00010000\_mbit9000.histogram.csv: tx: 10.18mpps, 0.05stdDev; rx: 6.79mpps, 0.00stdDev



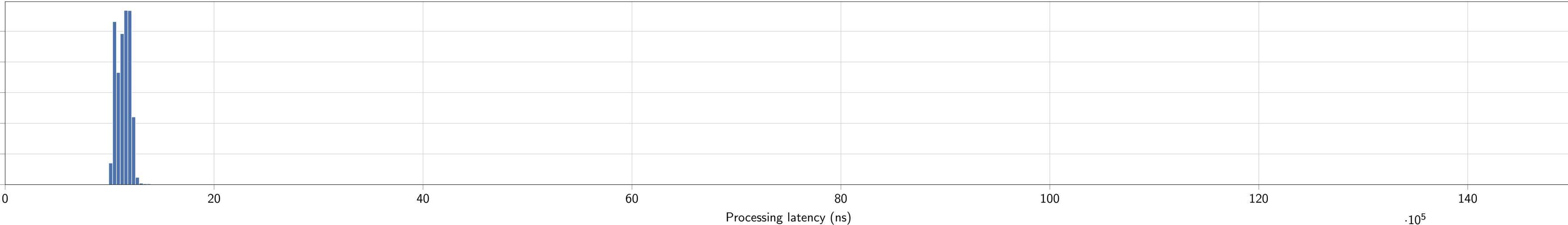






l2\_multimac\_00100000\_mbit1200.histogram.csv: tx: 2.36mpps, 0.01stdDev; rx: 2.36mpps, 0.00stdDev

Number of events



l2\_multimac\_00100000\_mbit1600.histogram.csv: tx: 3.14mpps, 0.02stdDev; rx: 3.14mpps, 0.00stdDev

Number of events

50  
40  
30  
20  
10  
0

$\cdot 10^4$

20

40

60

80

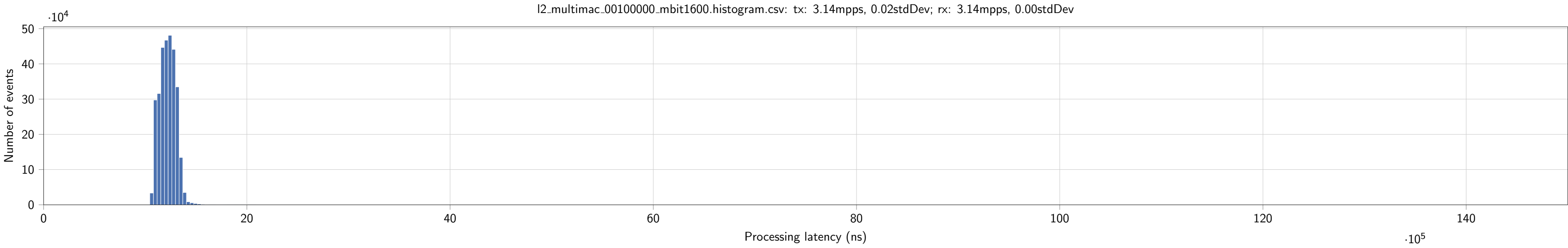
100

120

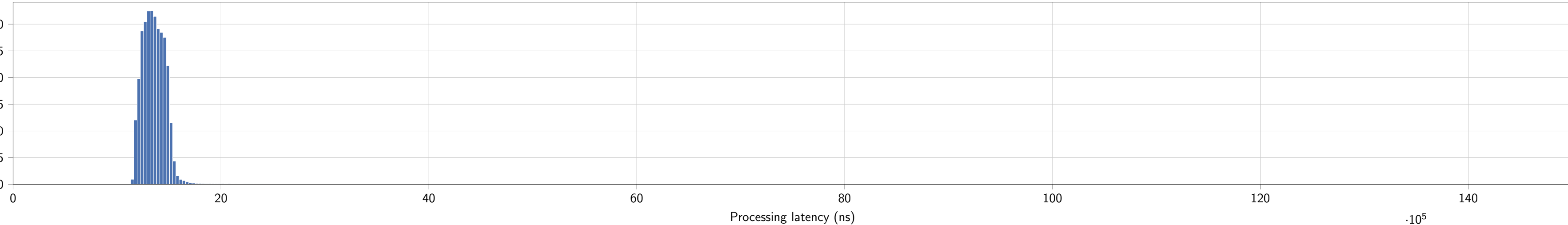
140

Processing latency (ns)

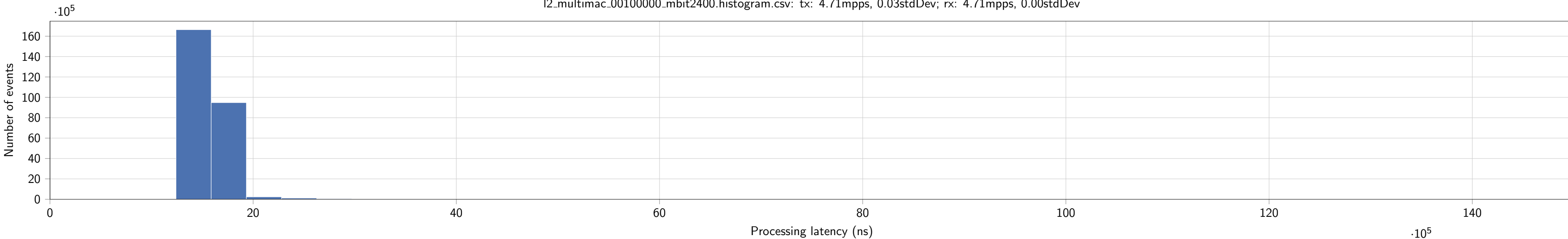
$\cdot 10^5$

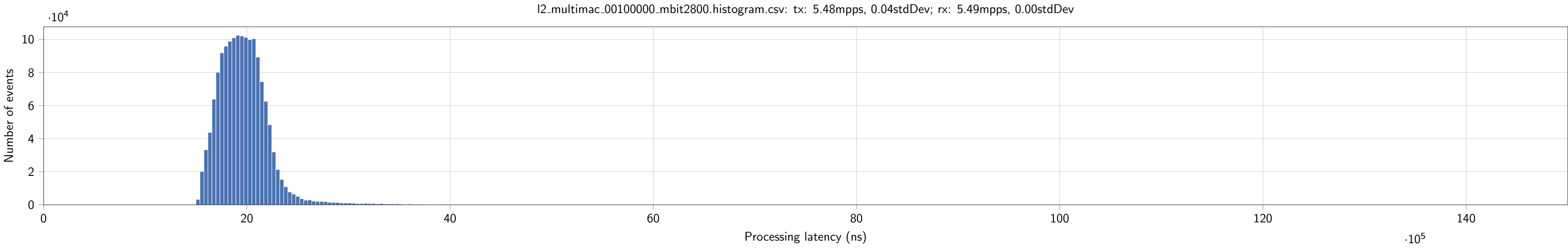


Number of events

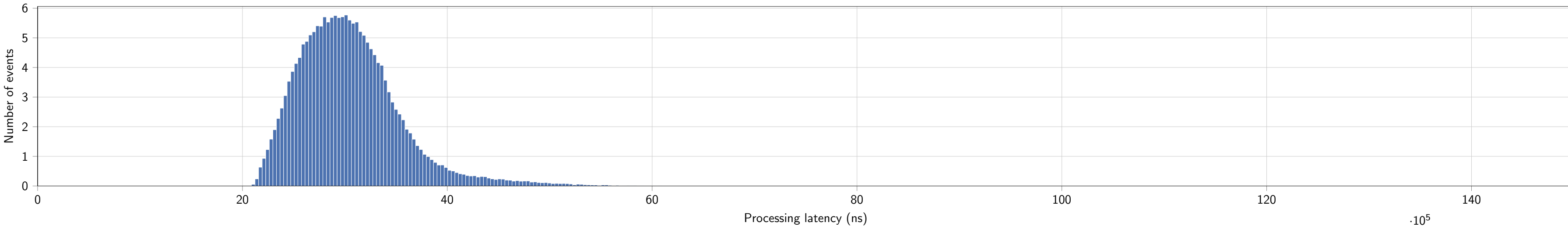
 $\cdot 10^4$ 

l2\_multimac\_00100000\_mbit2400.histogram.csv: tx: 4.71mpps, 0.03stdDev; rx: 4.71mpps, 0.00stdDev

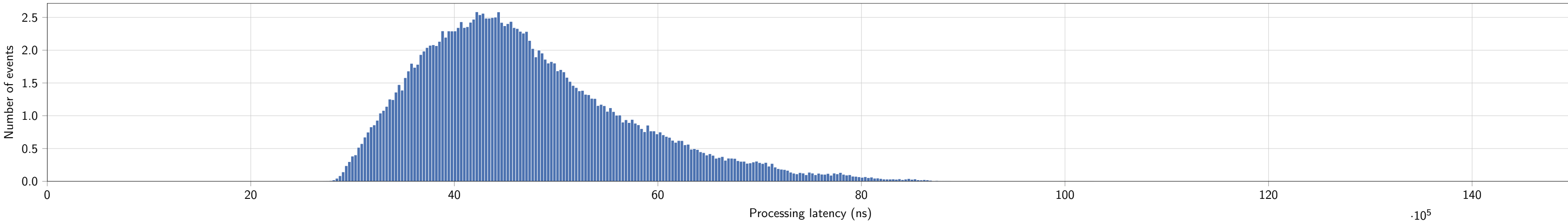




l2\_multimac\_00100000\_mbit3200.histogram.csv: tx: 6.25mpps, 0.04stdDev; rx: 6.26mpps, 0.00stdDev

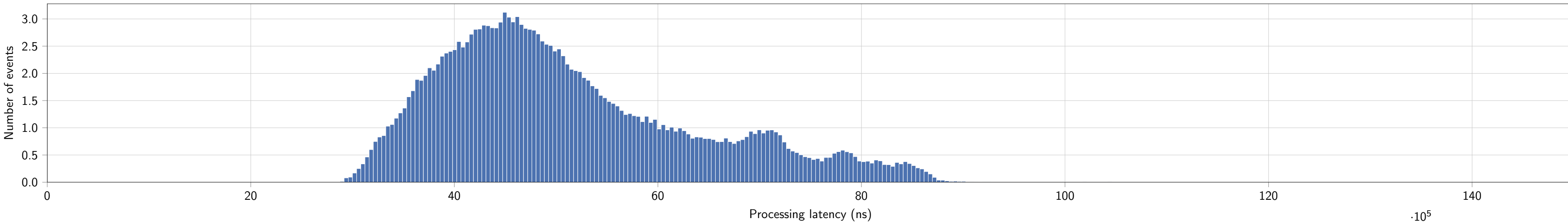


l2\_multimac\_00100000\_mbit3347hires.histogram.csv: tx: 6.54mpps, 0.04stdDev; rx: 6.55mpps, 0.00stdDev

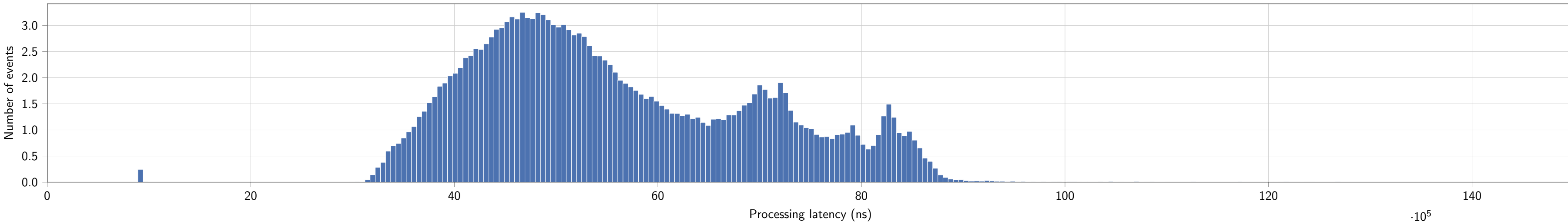




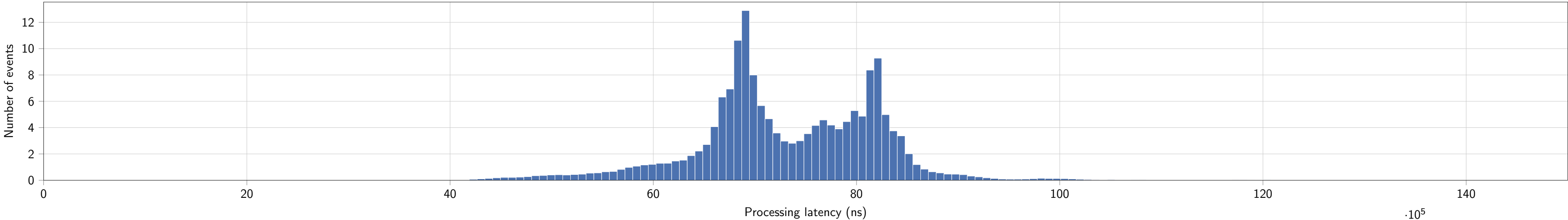
l2\_multimac\_00100000\_mbit3357hires.histogram.csv: tx: 6.58mpps, 0.04stdDev; rx: 6.59mpps, 0.00stdDev



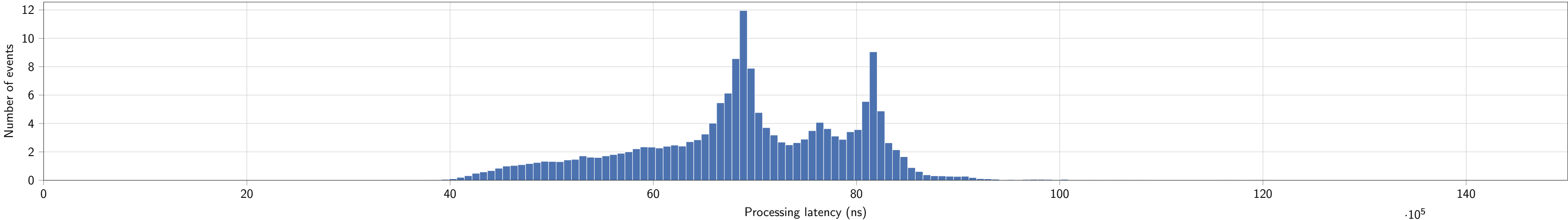
l2\_multimac\_00100000\_mbit3367hires.histogram.csv: tx: 6.58mpps, 0.04stdDev; rx: 6.59mpps, 0.00stdDev



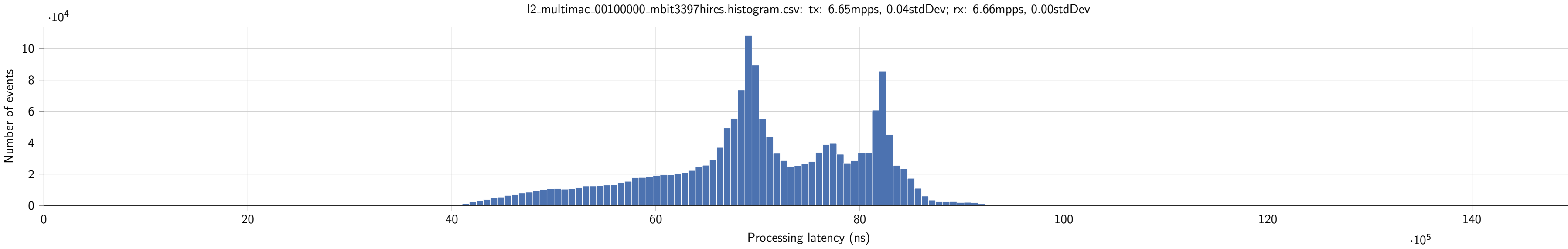
l2\_multimac\_00100000\_mbit3377hires.histogram.csv: tx: 6.61mpps, 0.04stdDev; rx: 6.62mpps, 0.00stdDev



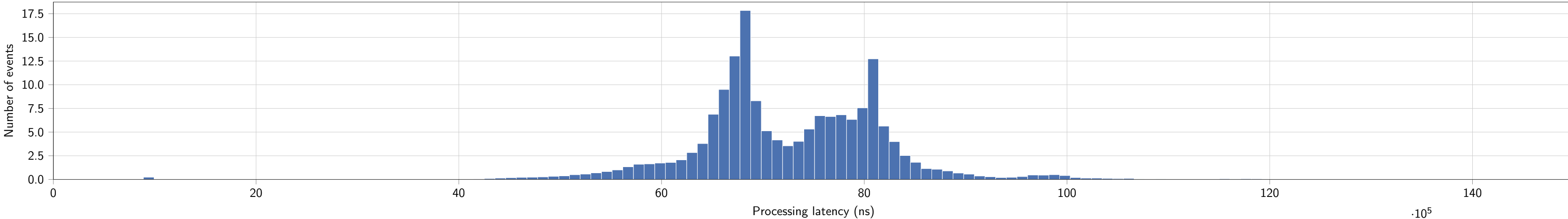
l2\_multimac\_00100000\_mbit3387hires.histogram.csv: tx: 6.65mpps, 0.04stdDev; rx: 6.66mpps, 0.00stdDev

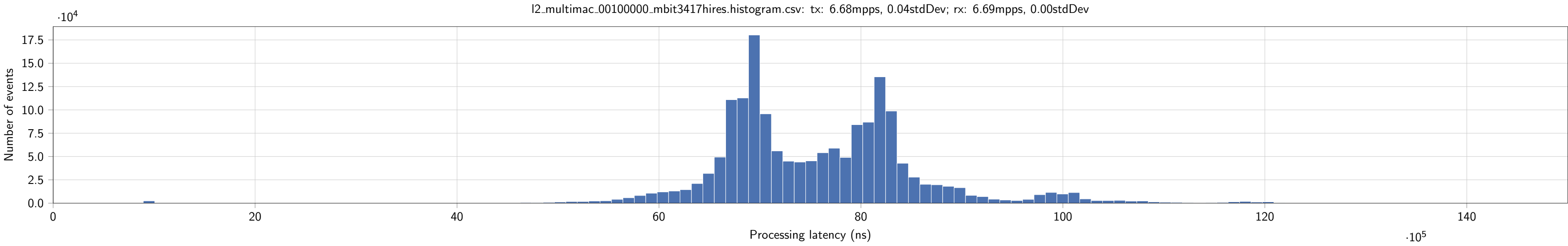


Number of events

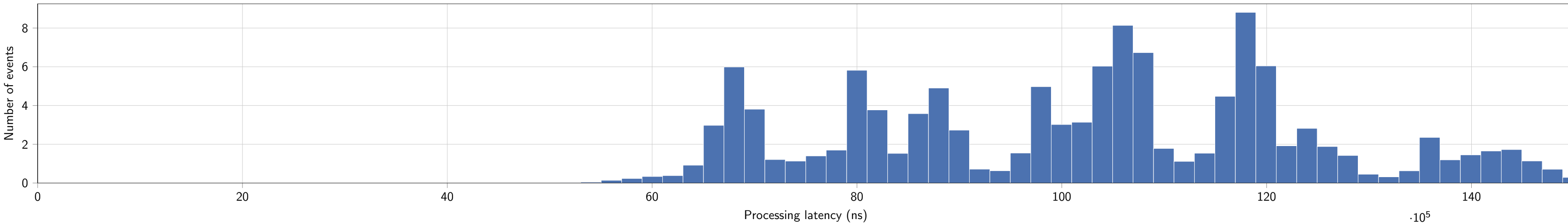


l2\_multimac\_00100000\_mbit3407hires.histogram.csv: tx: 6.68mpps, 0.04stdDev; rx: 6.69mpps, 0.00stdDev



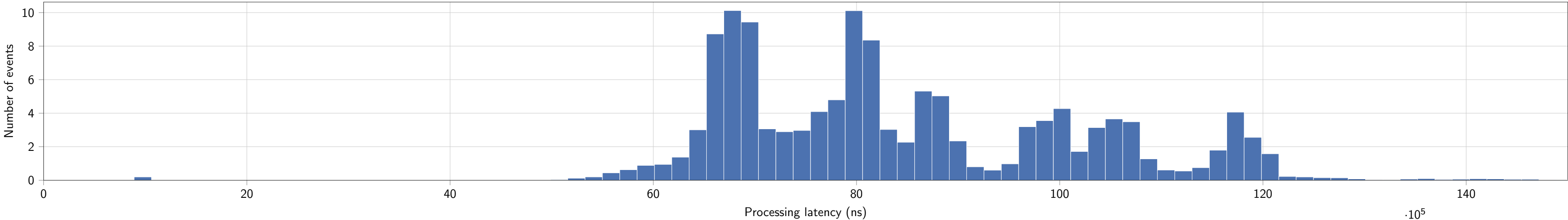


l2\_multimac\_00100000\_mbit3427hires.histogram.csv: tx: 6.72mpps, 0.04stdDev; rx: 6.73mpps, 0.00stdDev

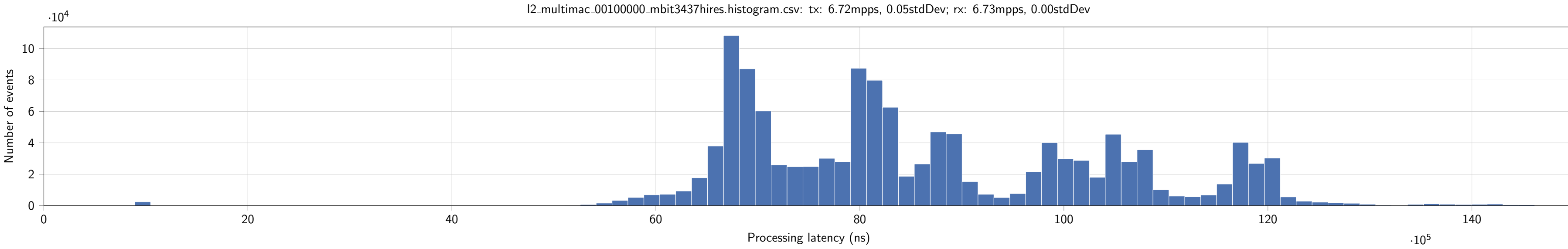




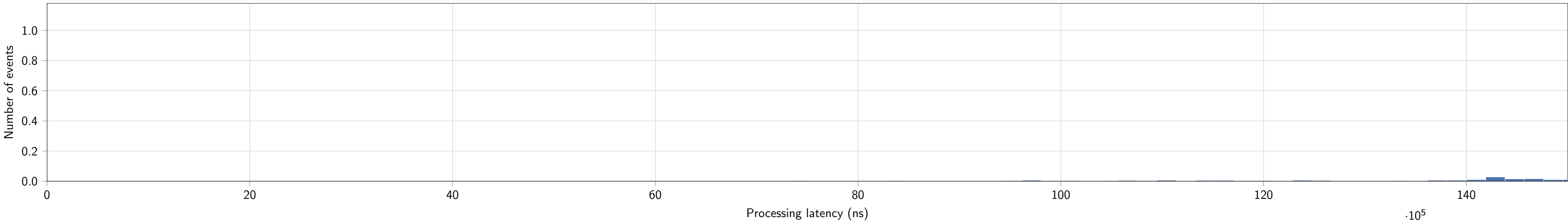
l2\_multimac\_00100000\_mbit3437\_final.histogram.csv: tx: 6.72mpps, 0.05stdDev; rx: 6.73mpps, 0.00stdDev



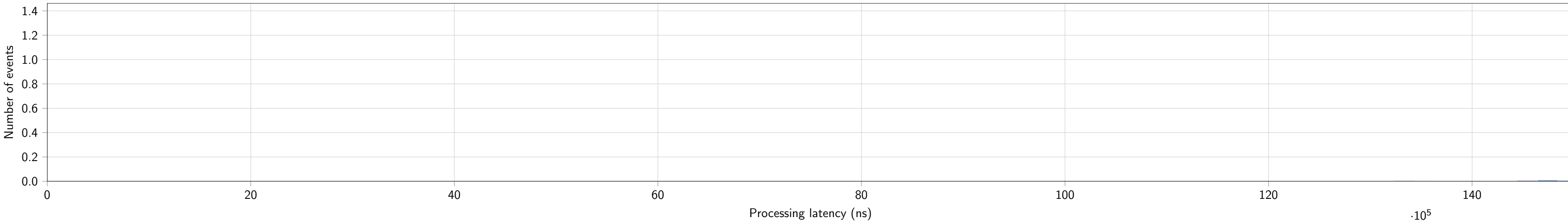
Number of events



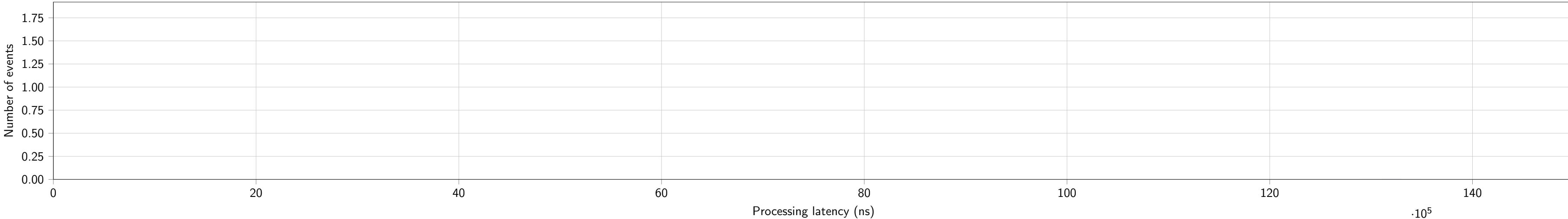
l2\_multimac\_00100000\_mbit3447hires.histogram.csv: tx: 6.75mpps, 0.04stdDev; rx: 6.76mpps, 0.00stdDev



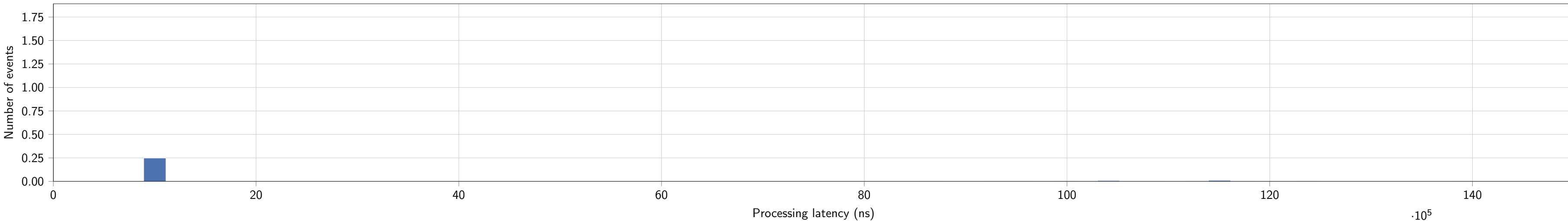
l2\_multimac\_00100000\_mbit3457hires.histogram.csv: tx: 6.75mpps, 0.04stdDev; rx: 6.73mpps, 0.00stdDev



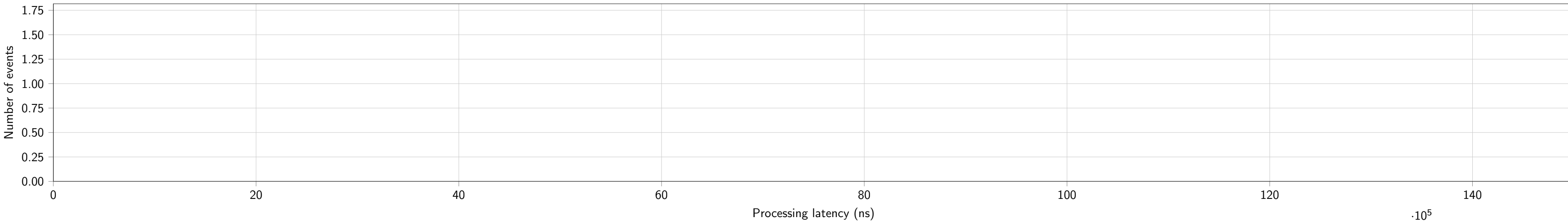
l2\_multimac\_00100000\_mbit3467hires.histogram.csv: tx: 6.78mpps, 0.04stdDev; rx: 6.73mpps, 0.00stdDev



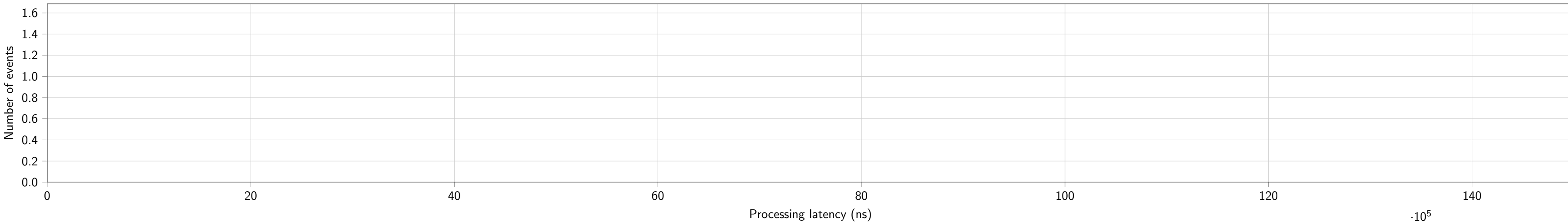
l2\_multimac\_00100000\_mbit3477hires.histogram.csv: tx: 6.78mpps, 0.04stdDev; rx: 6.75mpps, 0.00stdDev



l2\_multimac\_00100000\_mbit3487hires.histogram.csv: tx: 6.82mpps, 0.04stdDev; rx: 6.70mpps, 0.00stdDev

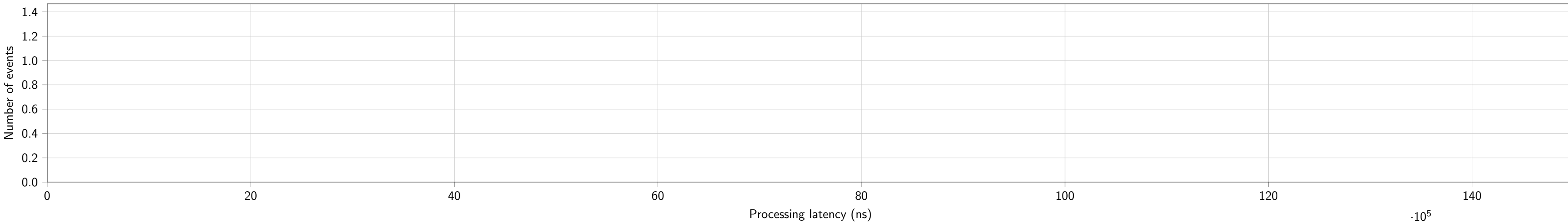


l2\_multimac\_00100000\_mbit3497hires.histogram.csv: tx: 6.82mpps, 0.04stdDev; rx: 6.75mpps, 0.00stdDev

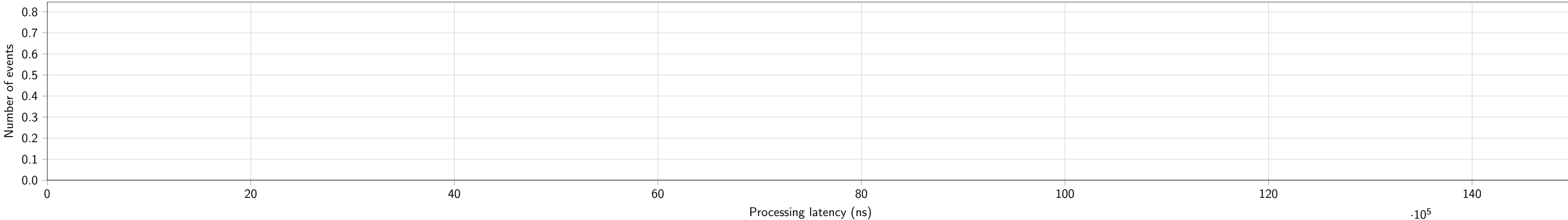




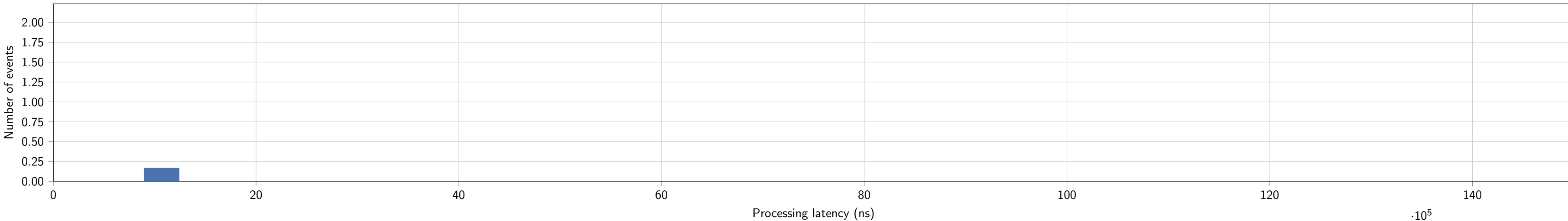
l2\_multimac\_00100000\_mbit3600.histogram.csv: tx: 7.05mpps, 0.04stdDev; rx: 6.72mpps, 0.00stdDev



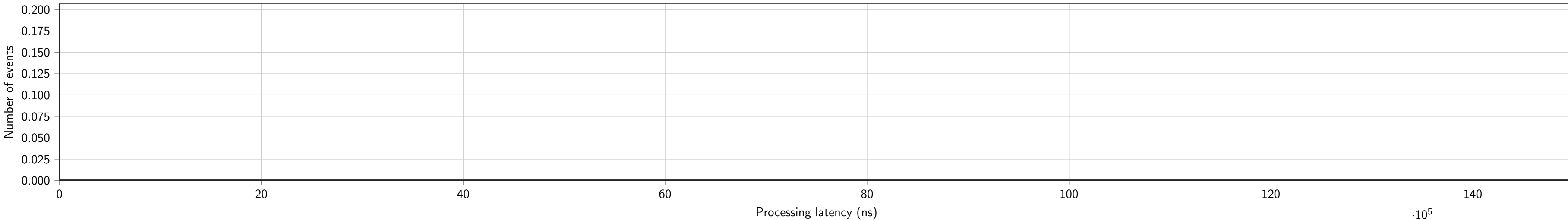
l2\_multimac\_00100000\_mbit4000.histogram.csv: tx: 7.80mpps, 0.05stdDev; rx: 6.75mpps, 0.00stdDev



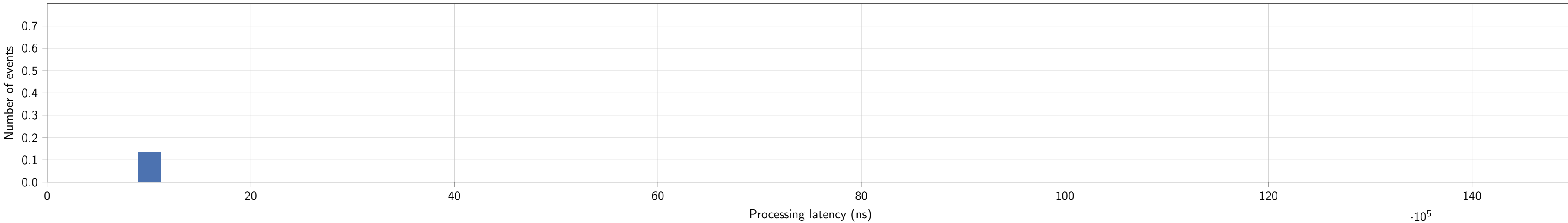
l2\_multimac\_00100000\_mbit4400.histogram.csv: tx: 8.61mpps, 0.05stdDev; rx: 6.74mpps, 0.03stdDev



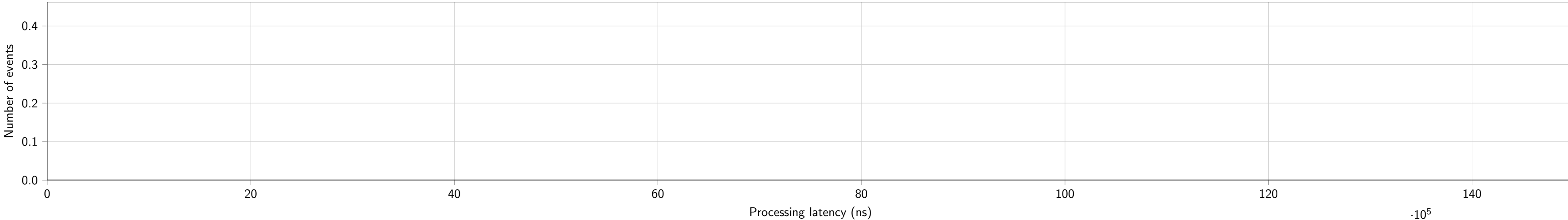
l2\_multimac\_00100000\_mbit4800.histogram.csv: tx: 9.39mpps, 0.05stdDev; rx: 6.75mpps, 0.00stdDev



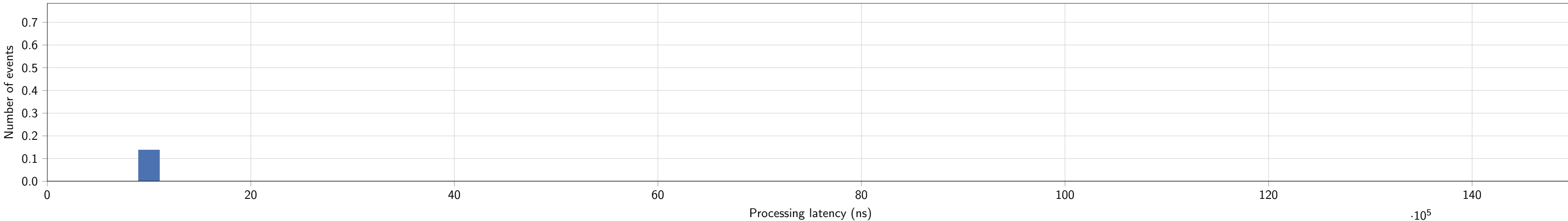
l2\_multimac\_00100000\_mbit5200.histogram.csv: tx: 10.10mpps, 0.05stdDev; rx: 6.74mpps, 0.00stdDev



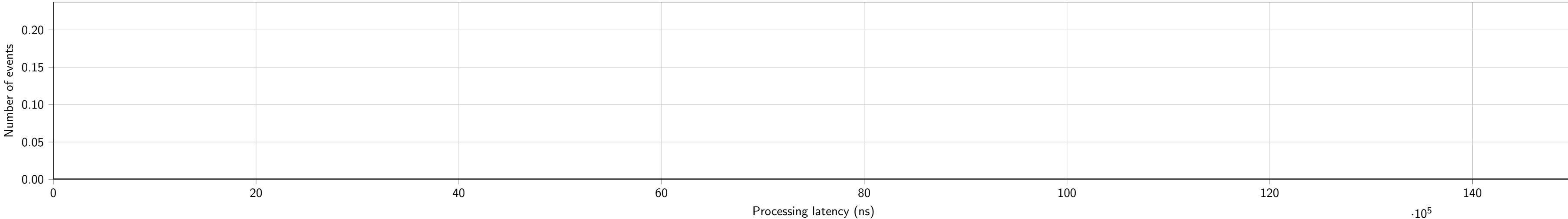
l2\_multimac\_00100000\_mbit5600.histogram.csv: tx: 9.98mpps, 0.05stdDev; rx: 6.71mpps, 0.00stdDev



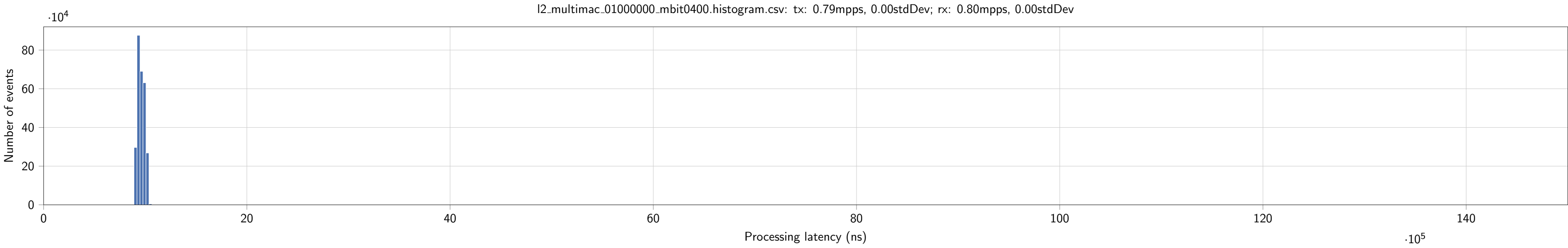
l2\_multimac\_00100000\_mbit6000.histogram.csv: tx: 10.17mpps, 0.05stdDev; rx: 6.74mpps, 0.00stdDev



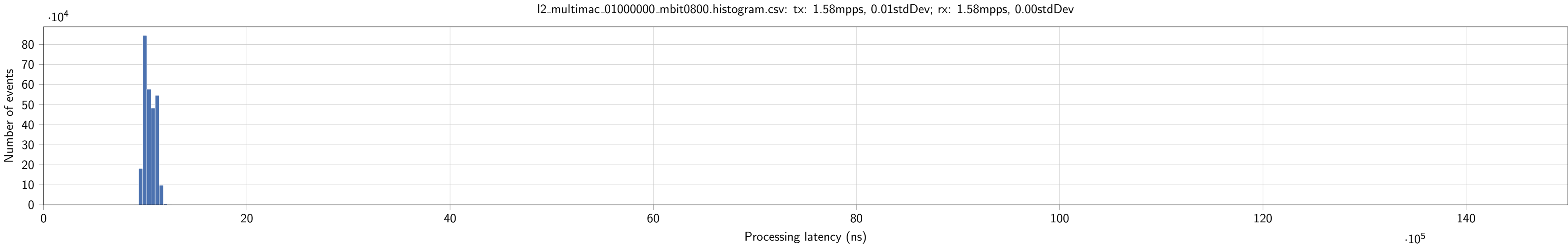
l2\_multimac\_00100000\_mbit9000.histogram.csv: tx: 10.11mpps, 0.05stdDev; rx: 6.73mpps, 0.00stdDev



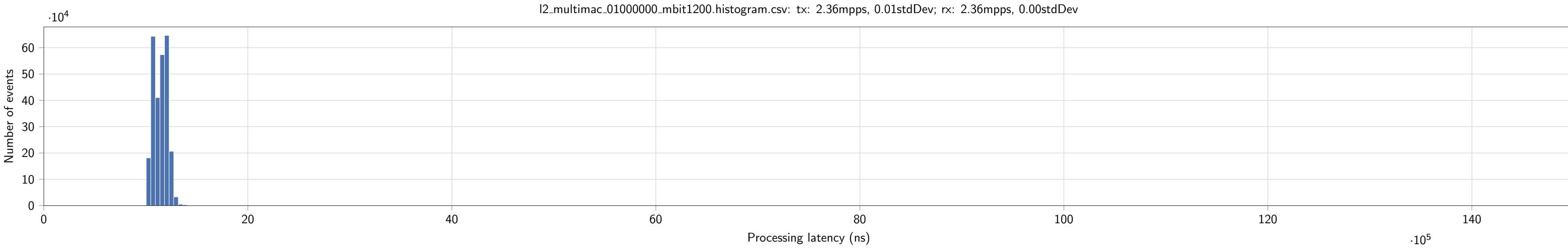




Number of events



Number of events



l2\_multimac\_01000000\_mbit1600.histogram.csv: tx: 3.14mpps, 0.02stdDev; rx: 3.14mpps, 0.00stdDev

Number of events

70  
60  
50  
40  
30  
20  
10  
0

$\cdot 10^4$

20

40

60

80

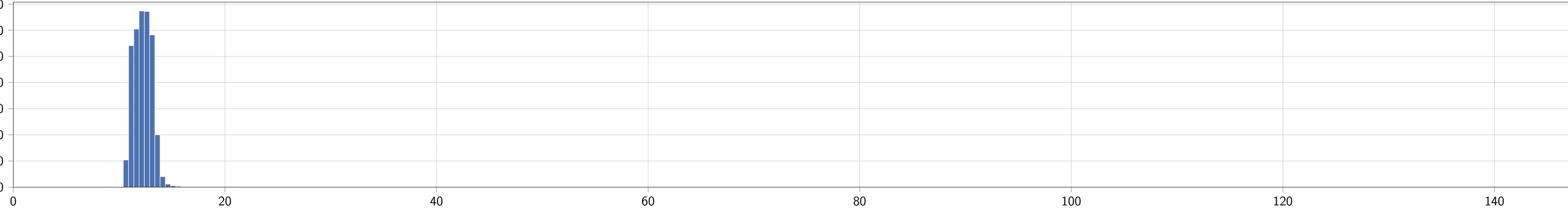
100

120

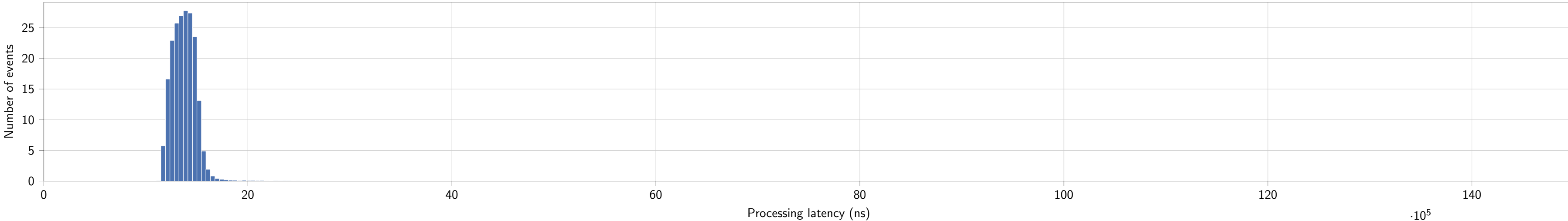
140

Processing latency (ns)

$\cdot 10^5$



l2\_multimac\_01000000\_mbit2000.histogram.csv: tx: 3.91mpps, 0.02stdDev; rx: 3.92mpps, 0.00stdDev



l2\_multimac\_01000000\_mbit2400.histogram.csv: tx: 4.70mpps, 0.03stdDev; rx: 4.71mpps, 0.00stdDev

Number of events

25  
20  
15  
10  
5  
0

0

20

40

60

80

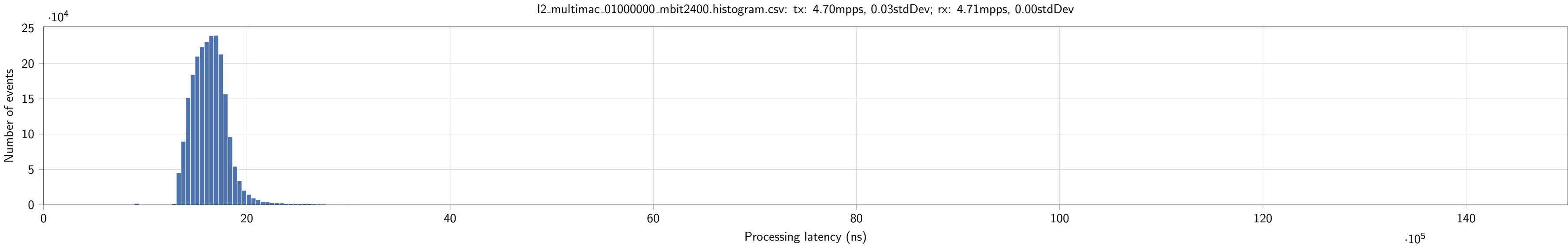
100

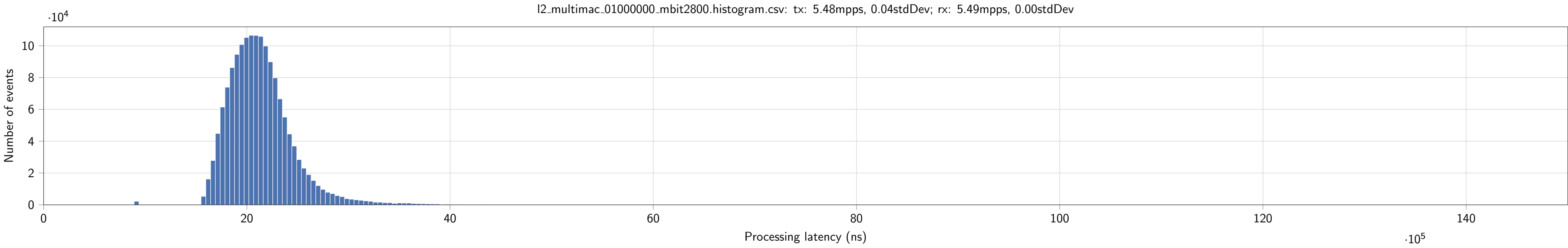
120

140

Processing latency (ns)

$\cdot 10^5$





l2\_multimac\_01000000\_mbit3200.histogram.csv: tx: 6.25mpps, 0.04stdDev; rx: 6.26mpps, 0.00stdDev

Number of events

$\cdot 10^4$

14

12

10

8

6

4

2

0

0

20

40

60

80

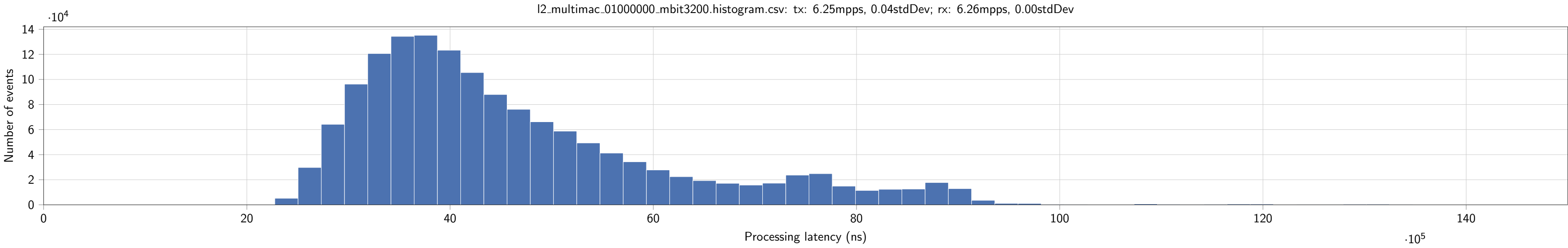
100

120

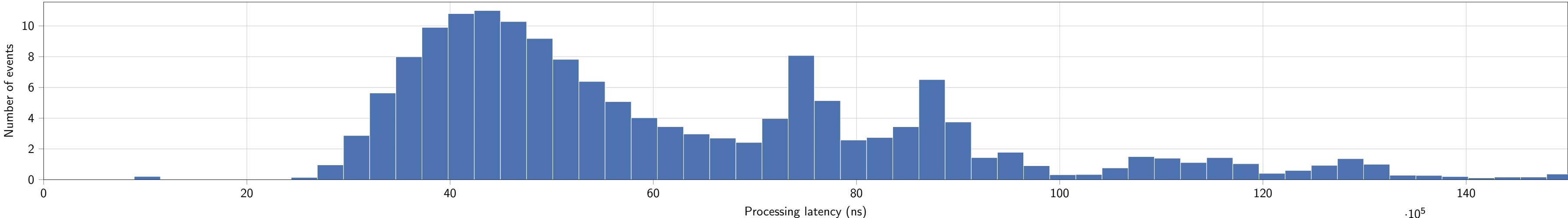
140

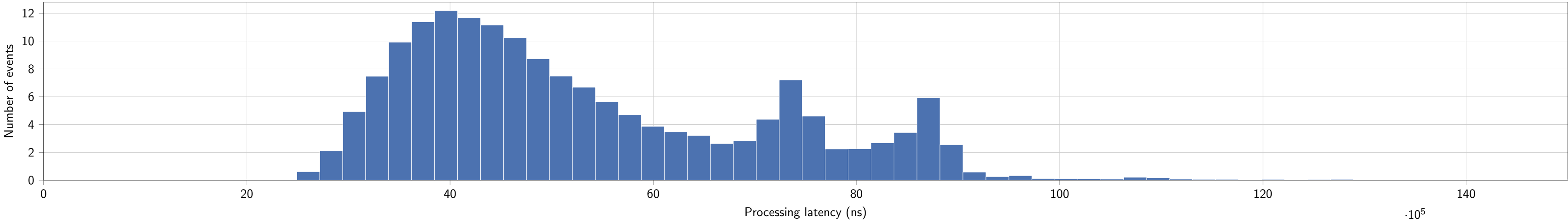
Processing latency (ns)

$\cdot 10^5$

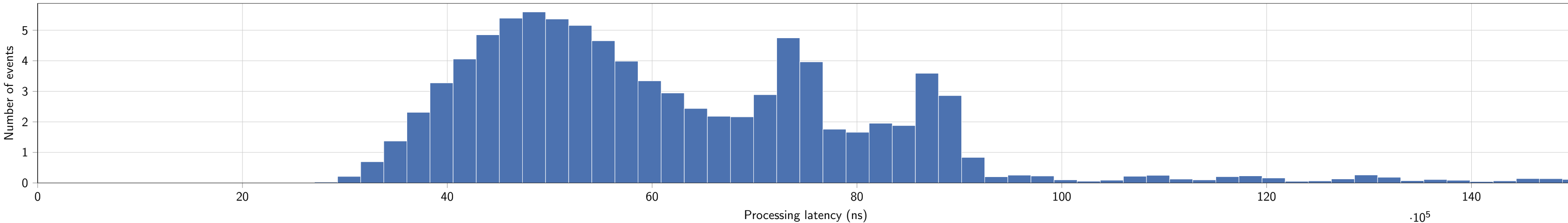




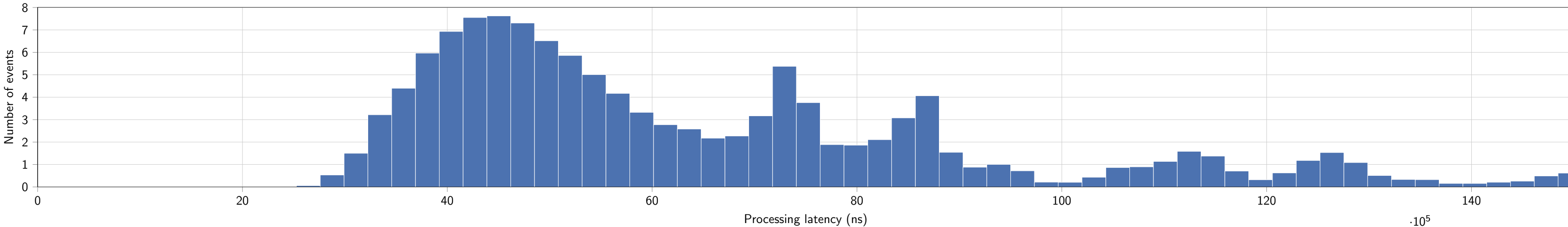




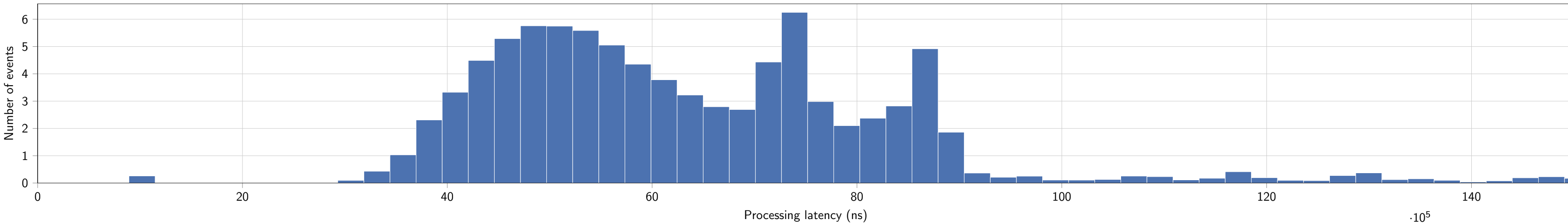
l2\_multimac\_01000000\_mbit3256hires.histogram.csv: tx: 6.37mpps, 0.04stdDev; rx: 6.38mpps, 0.01stdDev



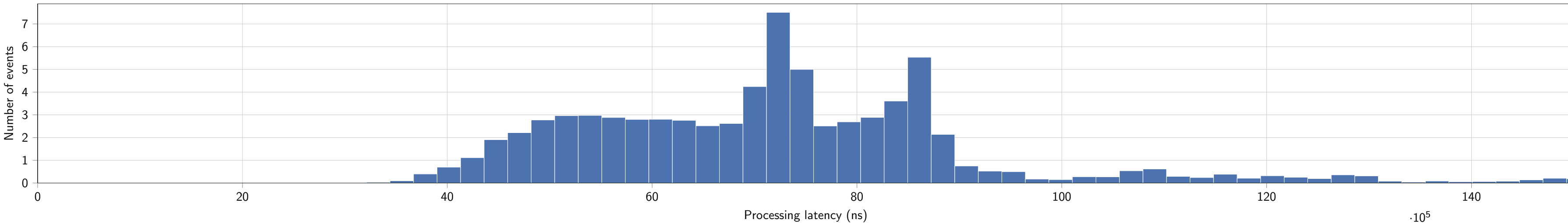
l2\_multimac\_01000000\_mbit3266hires.histogram.csv: tx: 6.41mpps, 0.04stdDev; rx: 6.42mpps, 0.01stdDev

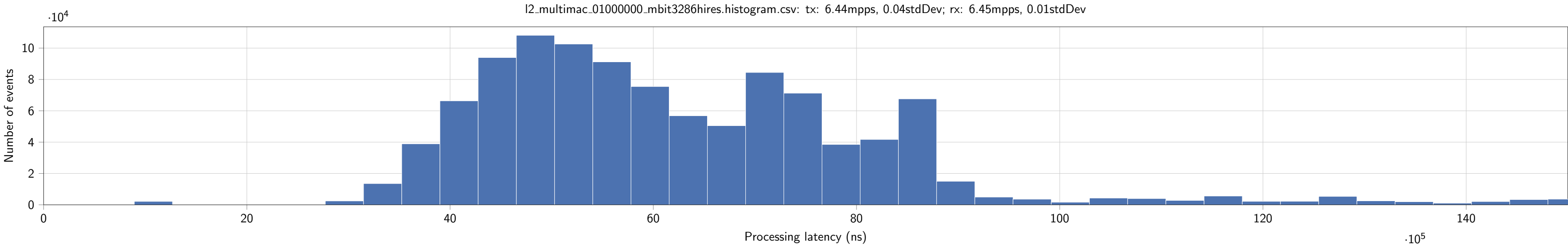


l2\_multimac\_01000000\_mbit3276hires.histogram.csv: tx: 6.41mpps, 0.04stdDev; rx: 6.41mpps, 0.01stdDev

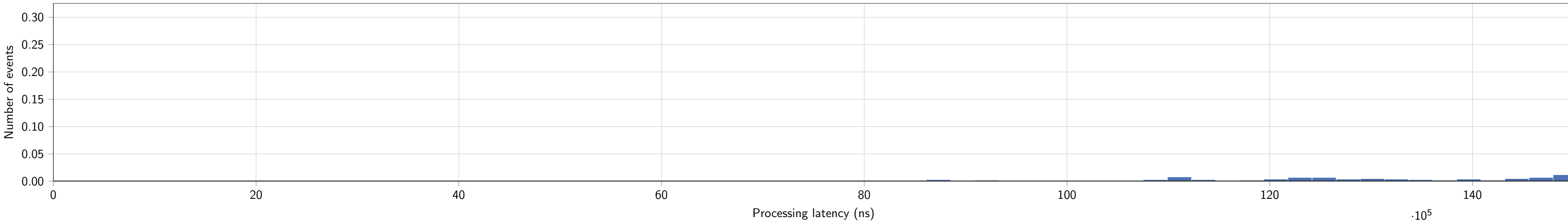


l2\_multimac\_01000000\_mbit3286\_final.histogram.csv: tx: 6.44mpps, 0.04stdDev; rx: 6.45mpps, 0.01stdDev



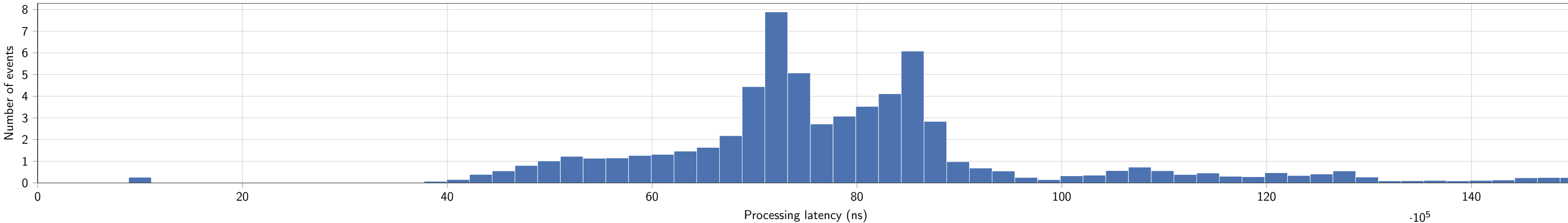


l2\_multimac\_01000000\_mbit3296hires.histogram.csv: tx: 6.43mpps, 0.04stdDev; rx: 6.40mpps, 0.01stdDev

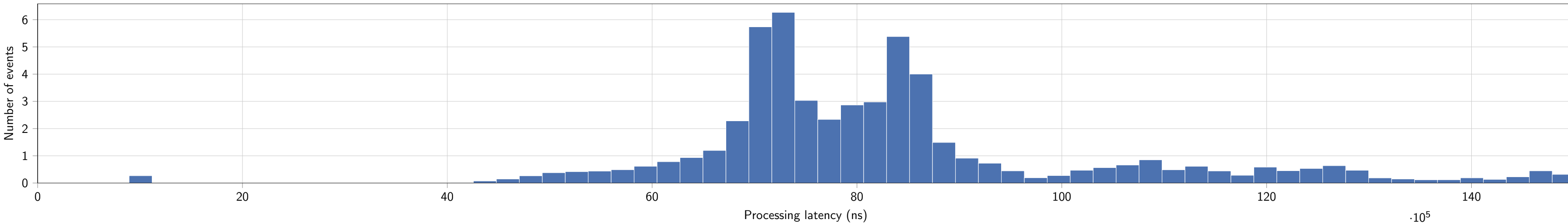


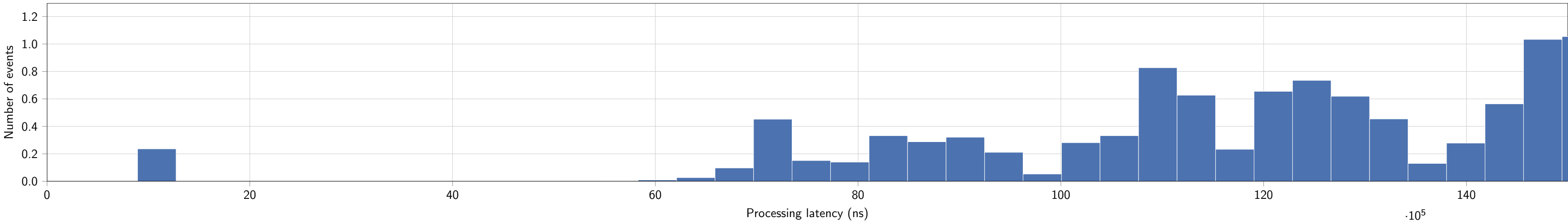


l2\_multimac\_01000000\_mbit3306hires.histogram.csv: tx: 6.47mpps, 0.05stdDev; rx: 6.48mpps, 0.01stdDev

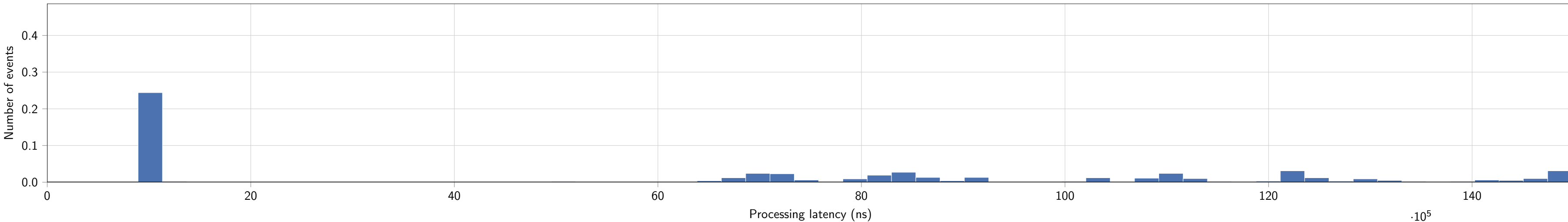


l2\_multimac\_01000000\_mbit3316hires.histogram.csv: tx: 6.47mpps, 0.05stdDev; rx: 6.48mpps, 0.01stdDev

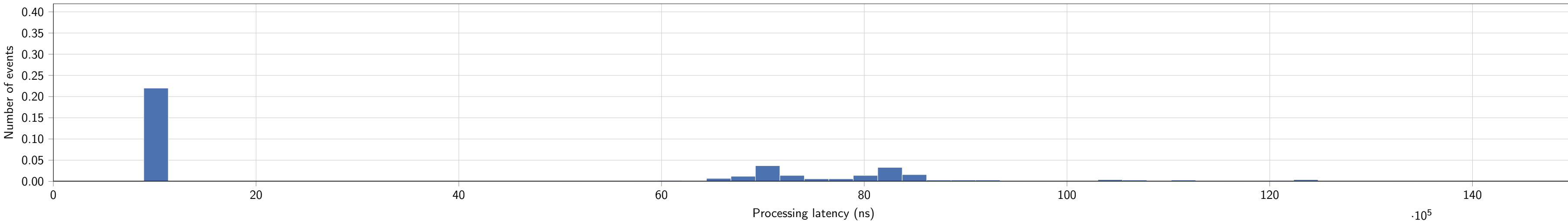




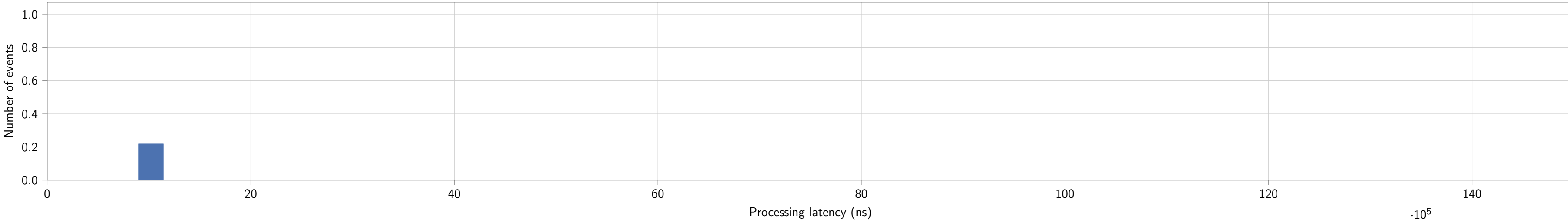
l2\_multimac\_01000000\_mbit3336hires.histogram.csv: tx: 6.53mpps, 0.05stdDev; rx: 6.52mpps, 0.01stdDev

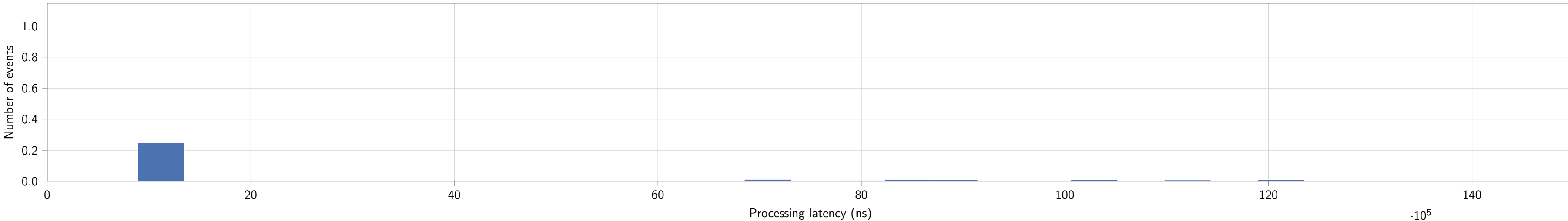


l2\_multimac\_01000000\_mbit3346hires.histogram.csv: tx: 6.53mpps, 0.05stdDev; rx: 6.51mpps, 0.01stdDev

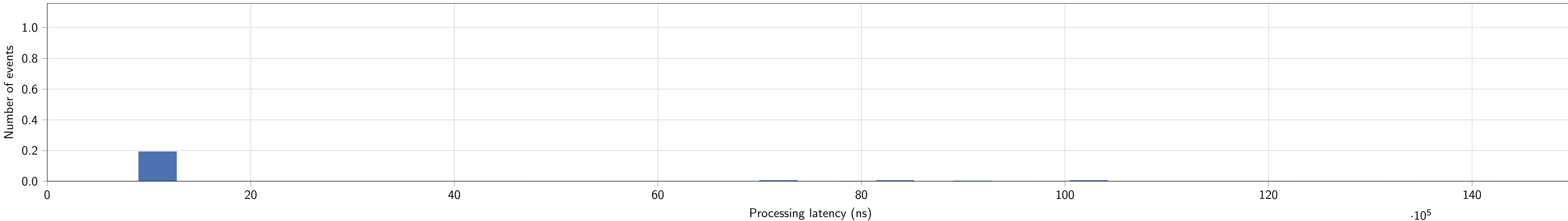


l2\_multimac\_01000000\_mbit3356hires.histogram.csv: tx: 6.57mpps, 0.04stdDev; rx: 6.43mpps, 0.04stdDev



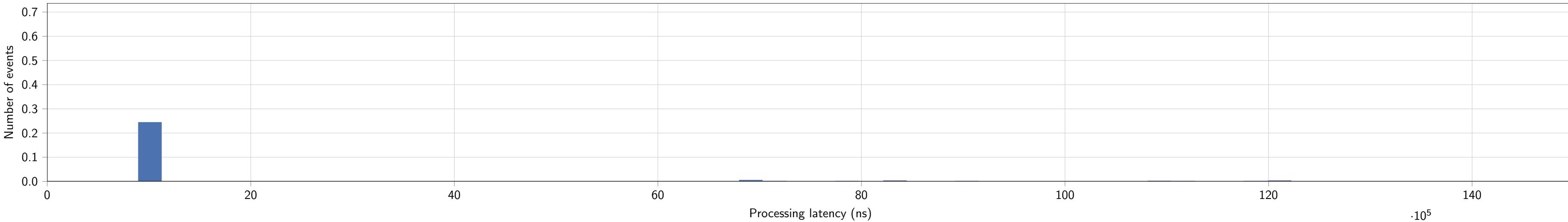


l2\_multimac\_01000000\_mbit3376hires.histogram.csv: tx: 6.61mpps, 0.04stdDev; rx: 6.53mpps, 0.01stdDev

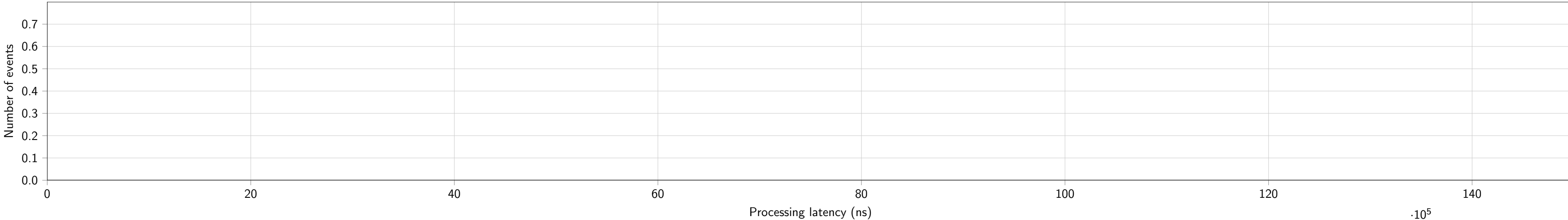




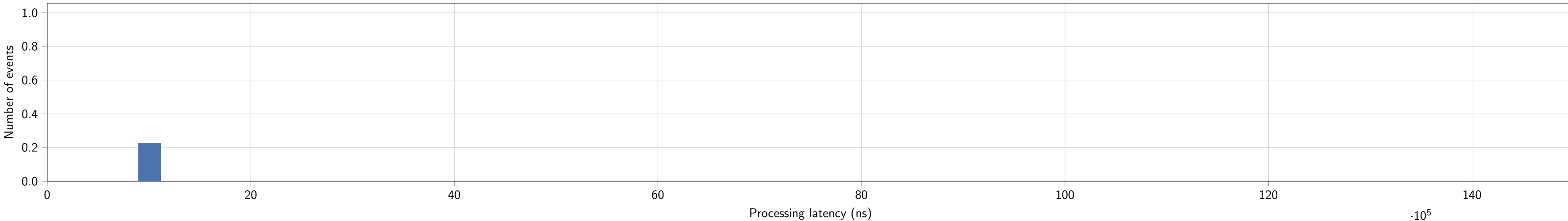
l2\_multimac\_01000000\_mbit3386hires.histogram.csv: tx: 6.60mpps, 0.05stdDev; rx: 6.52mpps, 0.01stdDev



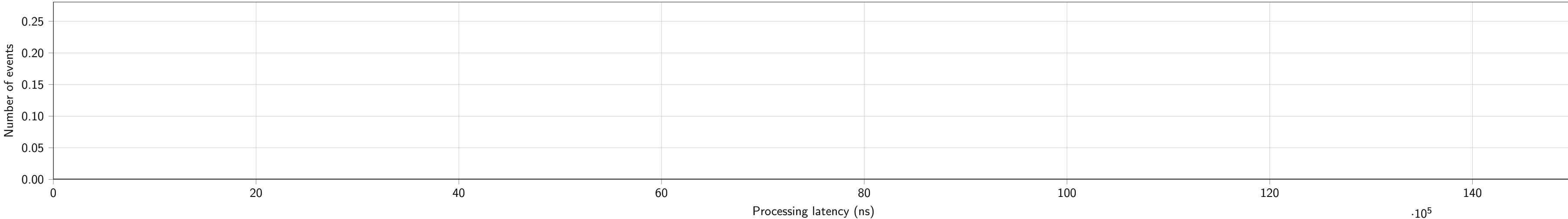
l2\_multimac\_01000000\_mbit3600.histogram.csv: tx: 7.05mpps, 0.05stdDev; rx: 6.46mpps, 0.04stdDev



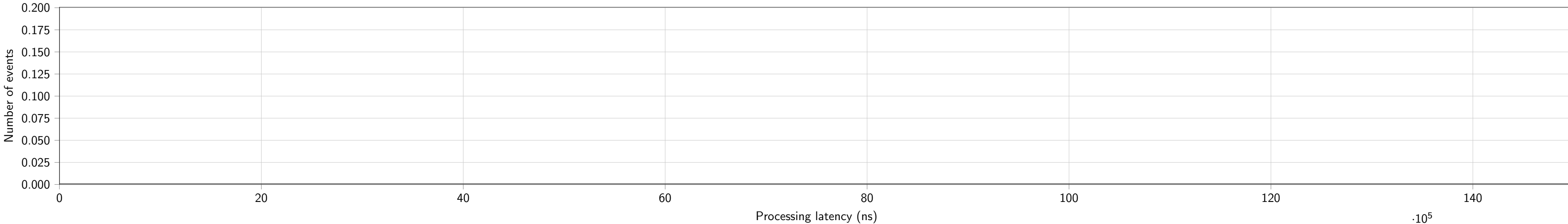
l2\_multimac\_01000000\_mbit4000.histogram.csv: tx: 7.80mpps, 0.05stdDev; rx: 6.50mpps, 0.01stdDev



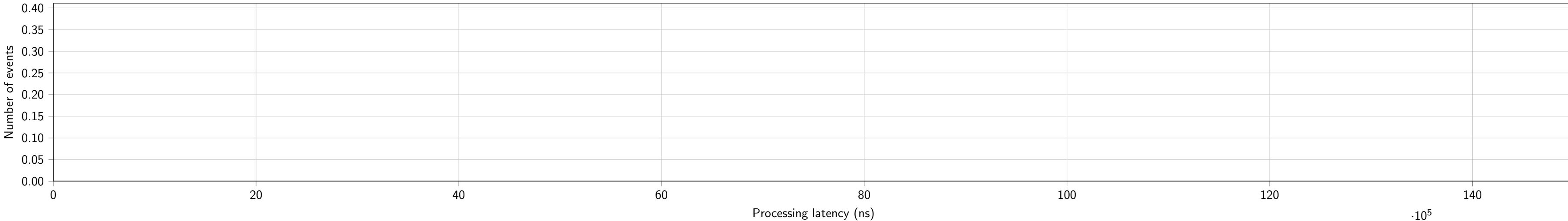
l2\_multimac\_01000000\_mbit4400.histogram.csv: tx: 8.61mpps, 0.05stdDev; rx: 6.47mpps, 0.01stdDev



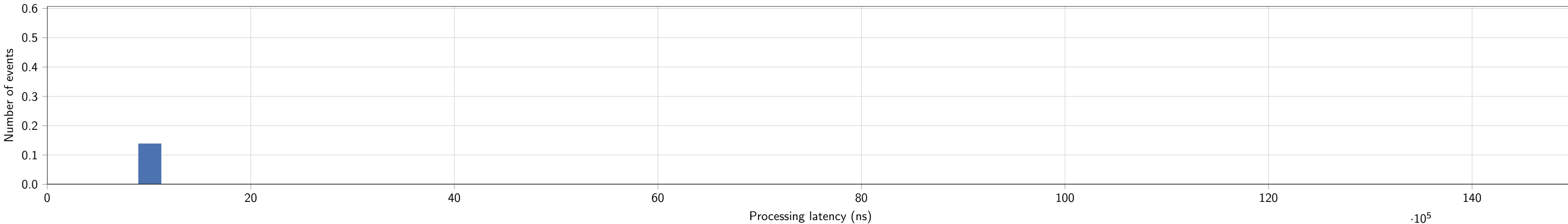
l2\_multimac\_01000000\_mbit4800.histogram.csv: tx: 9.38mpps, 0.05stdDev; rx: 6.40mpps, 0.01stdDev



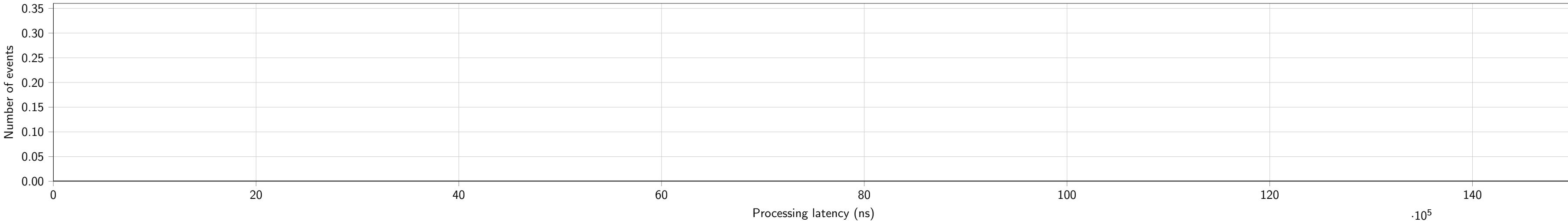
l2\_multimac\_01000000\_mbit5200.histogram.csv: tx: 10.09mpps, 0.05stdDev; rx: 6.48mpps, 0.01stdDev



l2\_multimac\_01000000\_mbit5600.histogram.csv: tx: 10.13mpps, 0.05stdDev; rx: 6.42mpps, 0.01stdDev

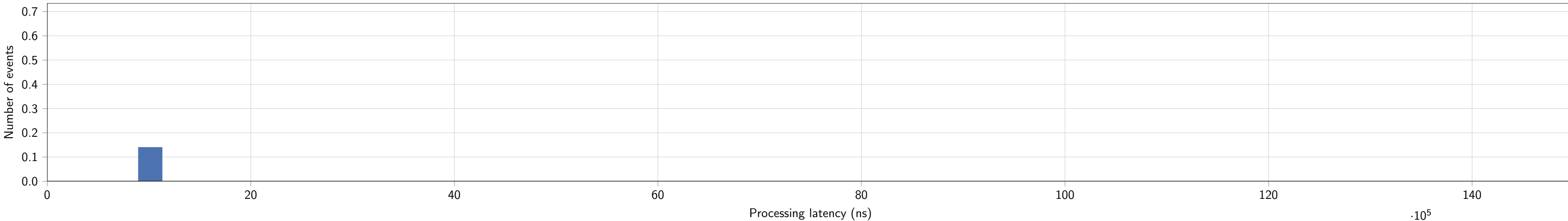


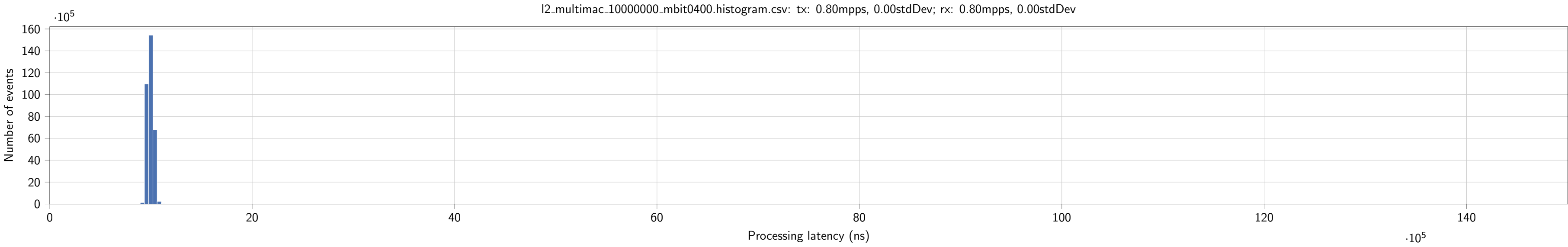
l2\_multimac\_01000000\_mbit6000.histogram.csv: tx: 10.11mpps, 0.05stdDev; rx: 6.52mpps, 0.01stdDev

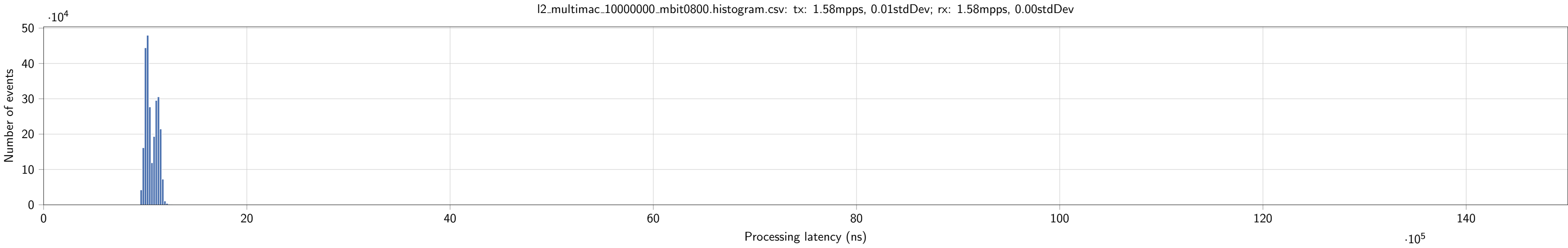




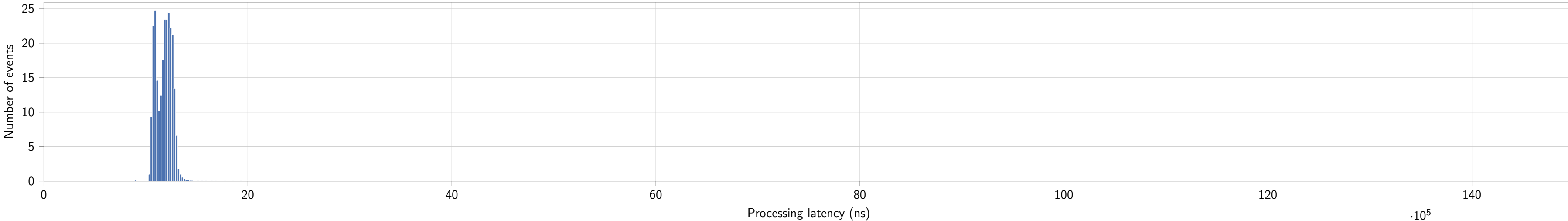
l2\_multimac\_01000000\_mbit9000.histogram.csv: tx: 10.16mpps, 0.05stdDev; rx: 6.52mpps, 0.01stdDev







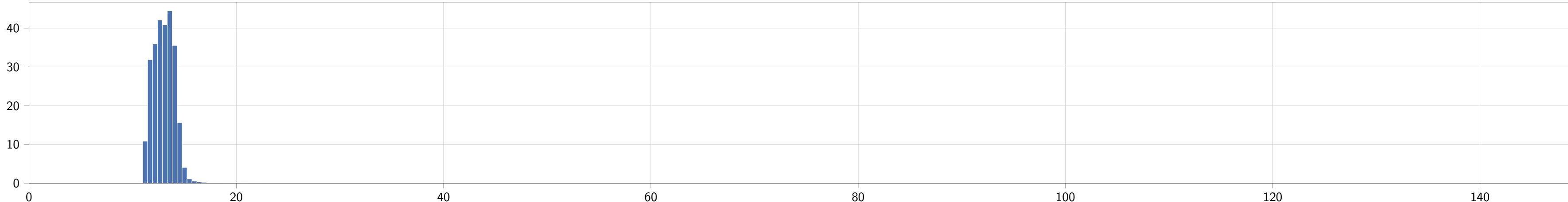
l2\_multimac\_10000000\_mbit1200.histogram.csv: tx: 2.36mpps, 0.01stdDev; rx: 2.36mpps, 0.00stdDev



l2\_multimac\_10000000\_mbit1600.histogram.csv: tx: 3.14mpps, 0.02stdDev; rx: 3.14mpps, 0.00stdDev

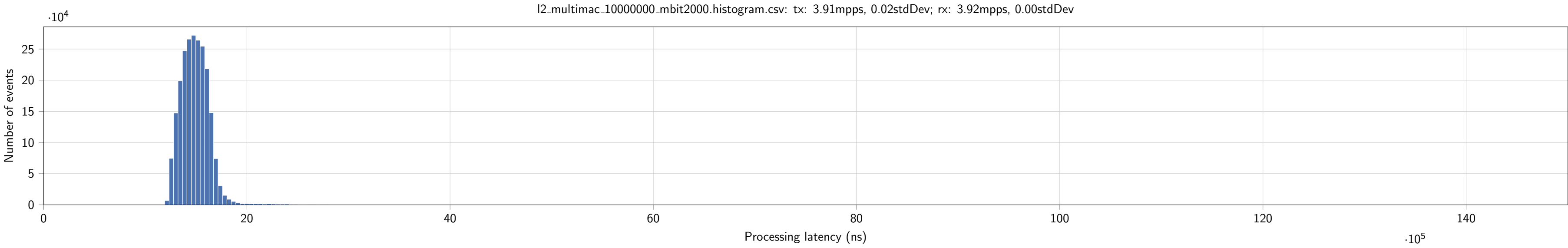
Number of events

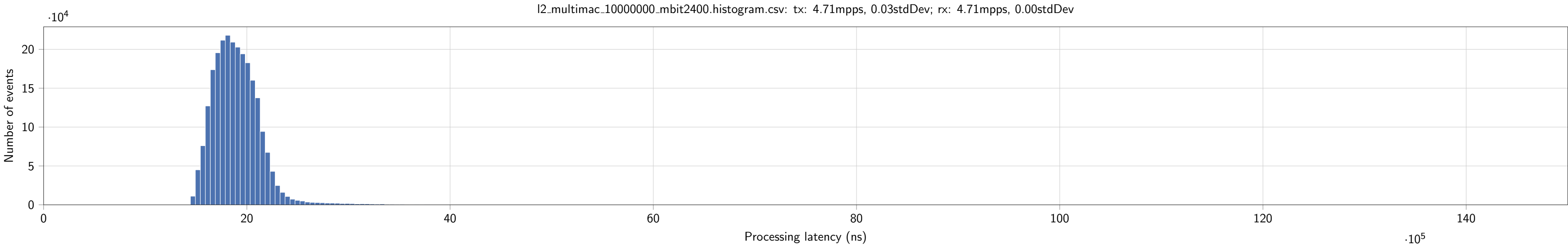
$\cdot 10^4$



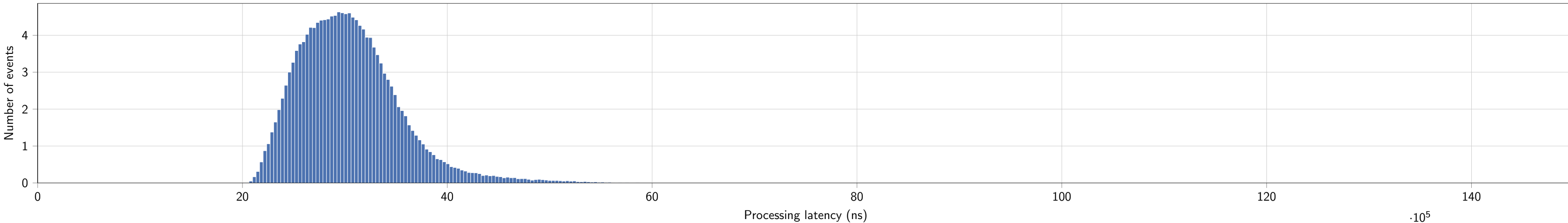
Processing latency (ns)

$\cdot 10^5$



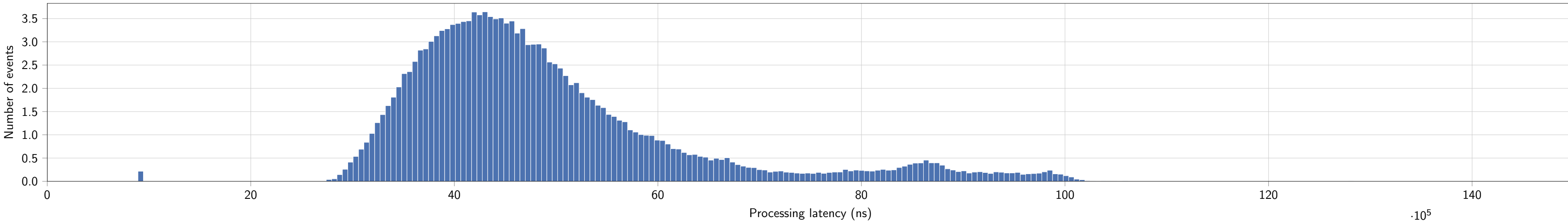


l2\_multimac\_10000000\_mbit2800.histogram.csv: tx: 5.48mpps, 0.04stdDev; rx: 5.49mpps, 0.00stdDev

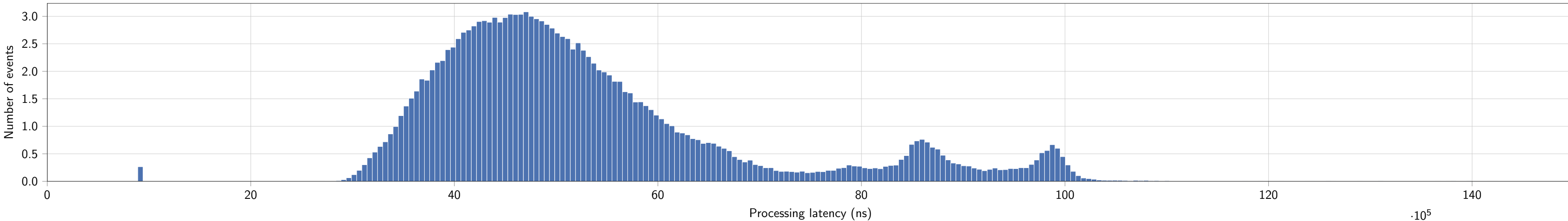




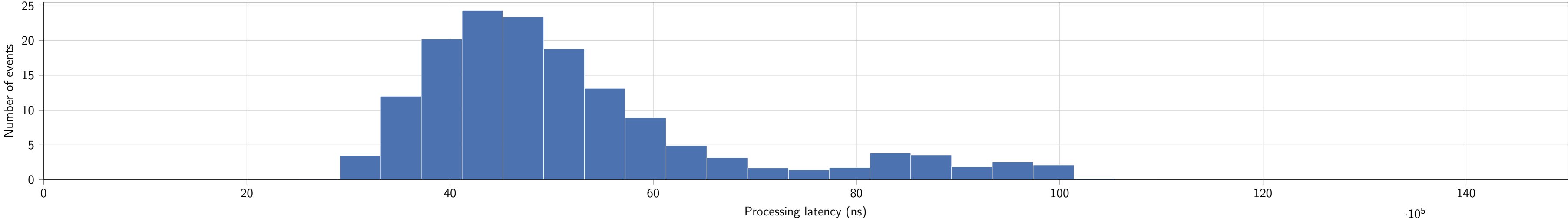
l2\_multimac\_10000000\_mbit2941hires.histogram.csv: tx: 5.76mpps, 0.04stdDev; rx: 5.77mpps, 0.00stdDev



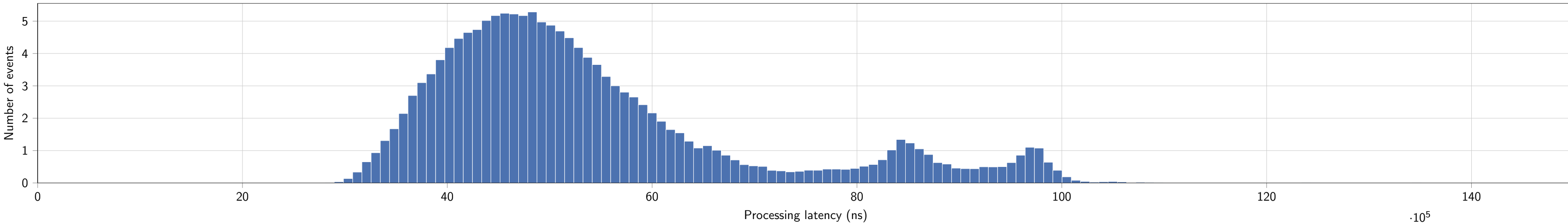
l2\_multimac\_10000000\_mbit2951hires.histogram.csv: tx: 5.79mpps, 0.04stdDev; rx: 5.80mpps, 0.00stdDev



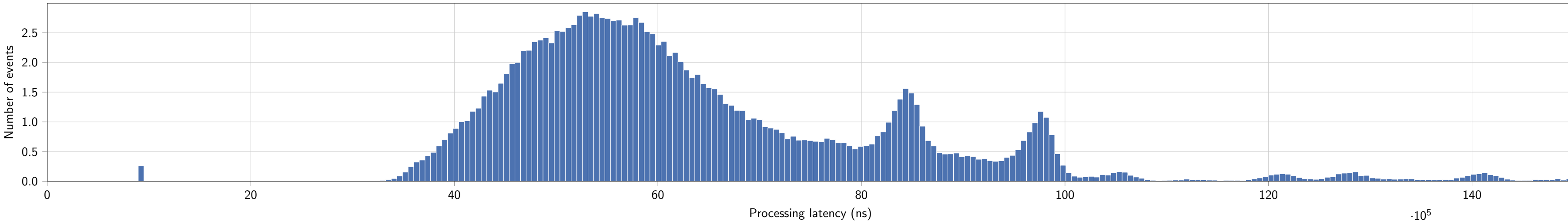
l2\_multimac\_10000000\_mbit2961hires.histogram.csv: tx: 5.79mpps, 0.04stdDev; rx: 5.80mpps, 0.00stdDev



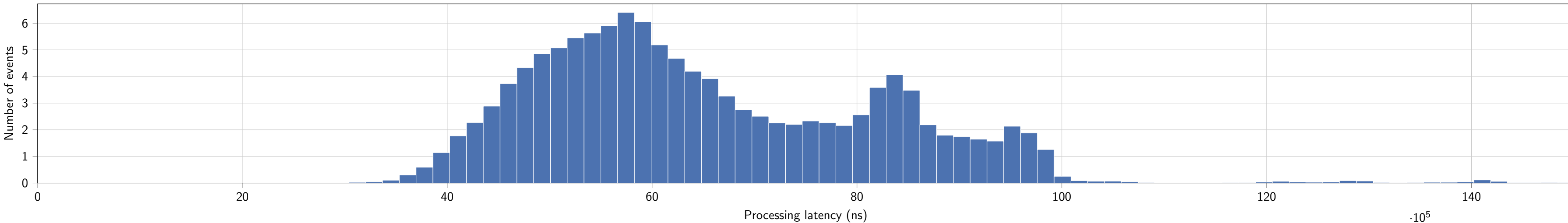
l2\_multimac\_10000000\_mbit2971hires.histogram.csv: tx: 5.81mpps, 0.04stdDev; rx: 5.82mpps, 0.00stdDev



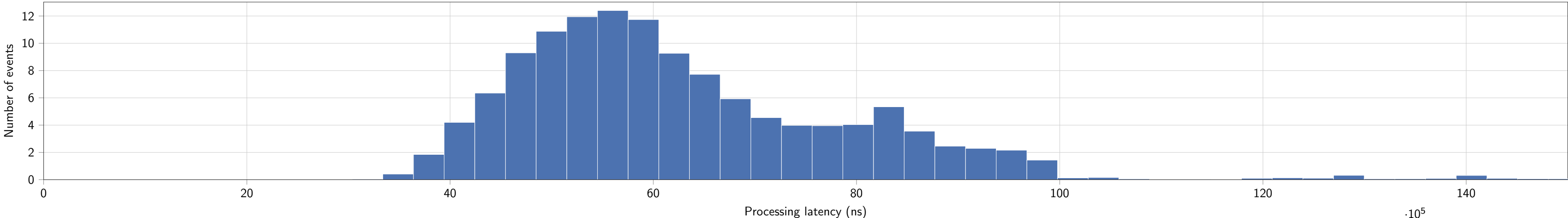
l2\_multimac\_10000000\_mbit2981hires.histogram.csv: tx: 5.84mpps, 0.04stdDev; rx: 5.85mpps, 0.00stdDev



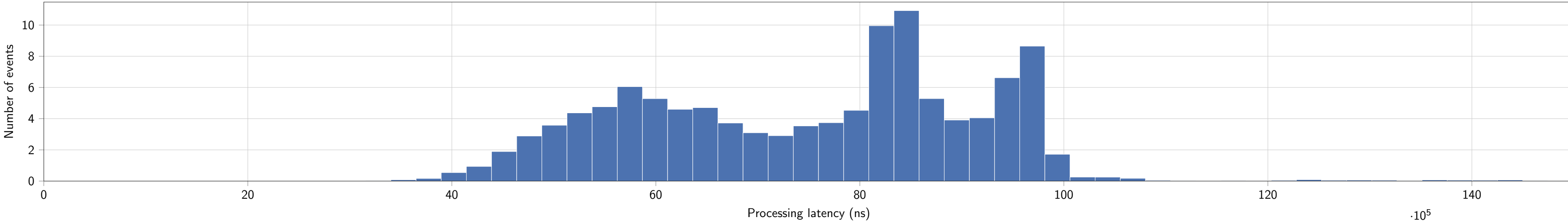
l2\_multimac\_10000000\_mbit2991hires.histogram.csv: tx: 5.87mpps, 0.04stdDev; rx: 5.88mpps, 0.00stdDev



l2\_multimac\_10000000\_mbit3001hires.histogram.csv: tx: 5.87mpps, 0.04stdDev; rx: 5.87mpps, 0.02stdDev

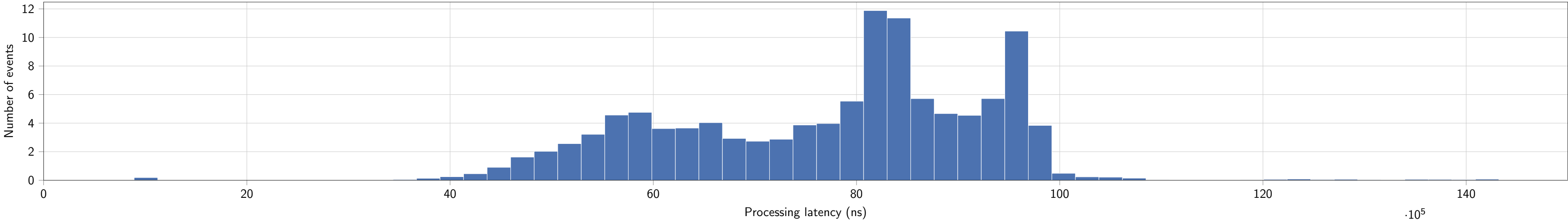


l2\_multimac\_10000000\_mbit3011hires.histogram.csv: tx: 5.89mpps, 0.04stdDev; rx: 5.90mpps, 0.01stdDev

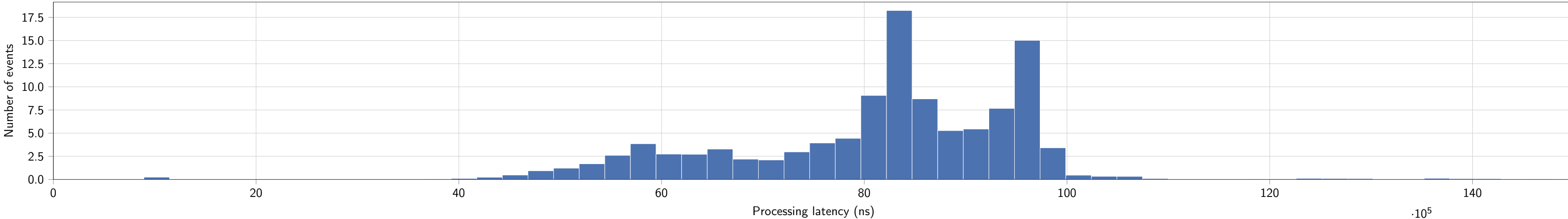




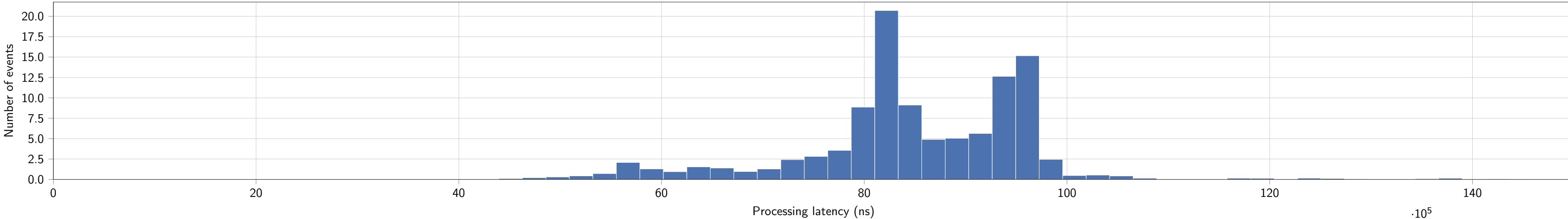
l2\_multimac\_10000000\_mbit3021hires.histogram.csv: tx: 5.92mpps, 0.04stdDev; rx: 5.93mpps, 0.01stdDev



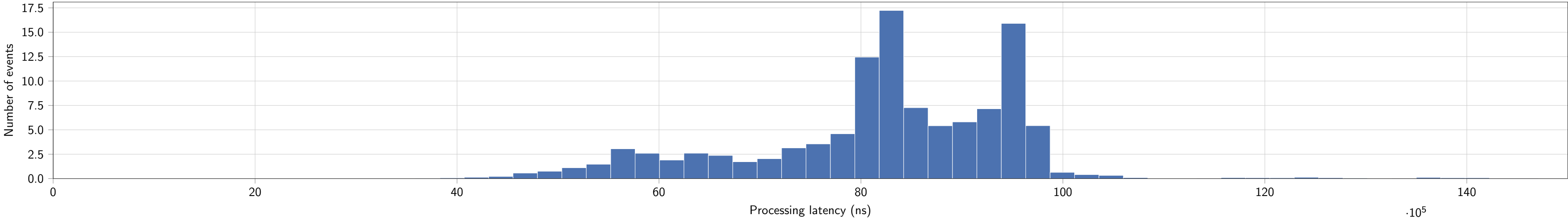
l2\_multimac\_10000000\_mbit3031hires.histogram.csv: tx: 5.92mpps, 0.04stdDev; rx: 5.92mpps, 0.01stdDev



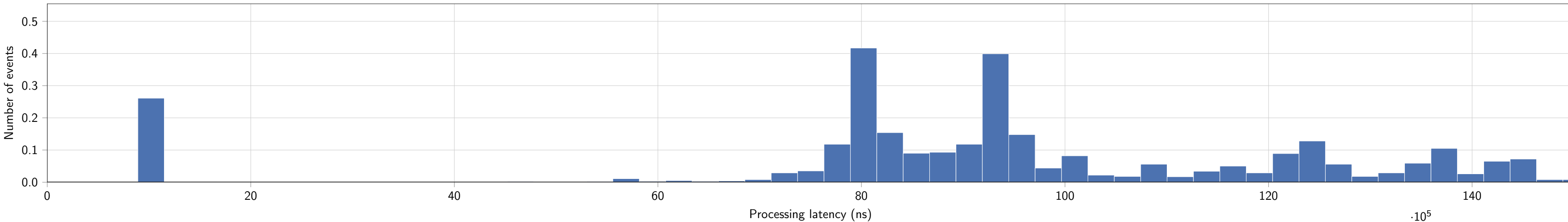
l2\_multimac\_10000000\_mbit3041\_final.histogram.csv: tx: 5.95mpps, 0.04stdDev; rx: 5.95mpps, 0.01stdDev



l2\_multimac\_10000000\_mbit3041hires.histogram.csv: tx: 5.95mpps, 0.04stdDev; rx: 5.95mpps, 0.01stdDev

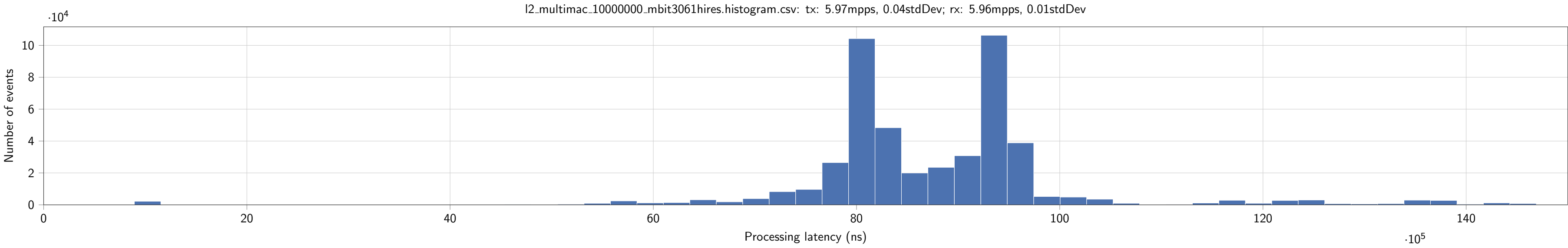


l2\_multimac\_10000000\_mbit3051hires.histogram.csv: tx: 5.97mpps, 0.04stdDev; rx: 5.94mpps, 0.02stdDev

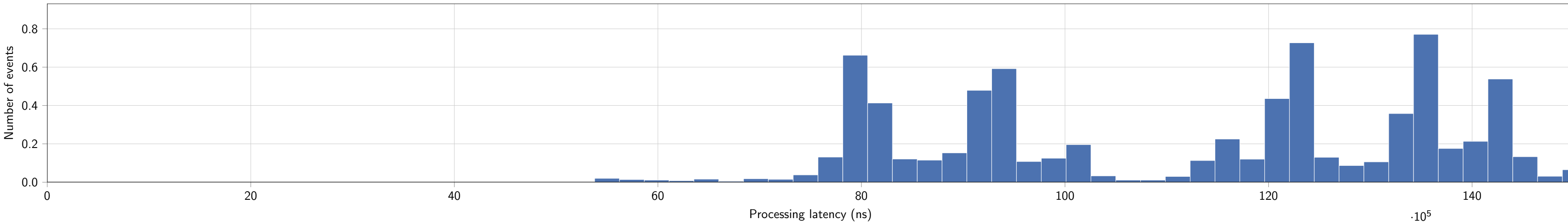


l2\_multimac\_10000000\_mbit3061hires.histogram.csv: tx: 5.97mpps, 0.04stdDev; rx: 5.96mpps, 0.01stdDev

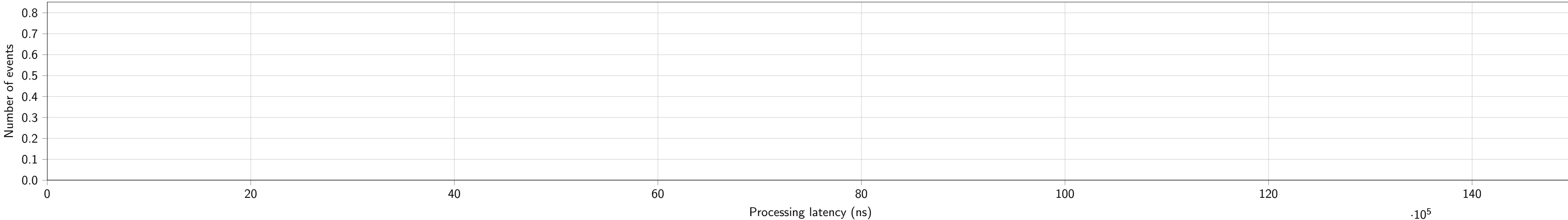
Number of events



l2\_multimac\_10000000\_mbit3071hires.histogram.csv: tx: 6.00mpps, 0.04stdDev; rx: 5.97mpps, 0.02stdDev

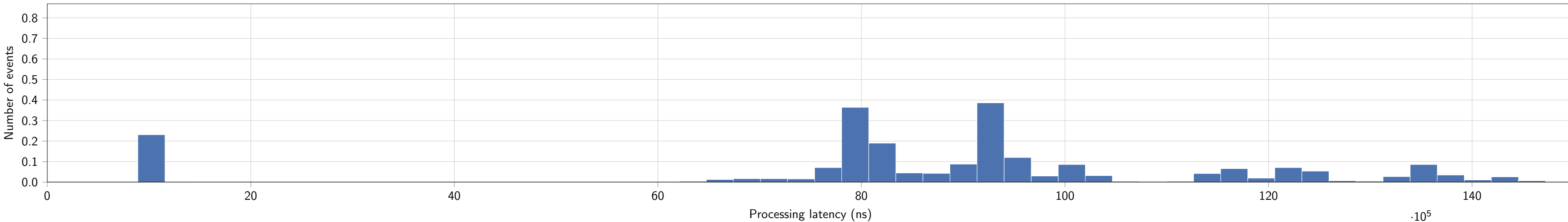


l2\_multimac\_10000000\_mbit3081hires.histogram.csv: tx: 6.03mpps, 0.04stdDev; rx: 5.91mpps, 0.02stdDev

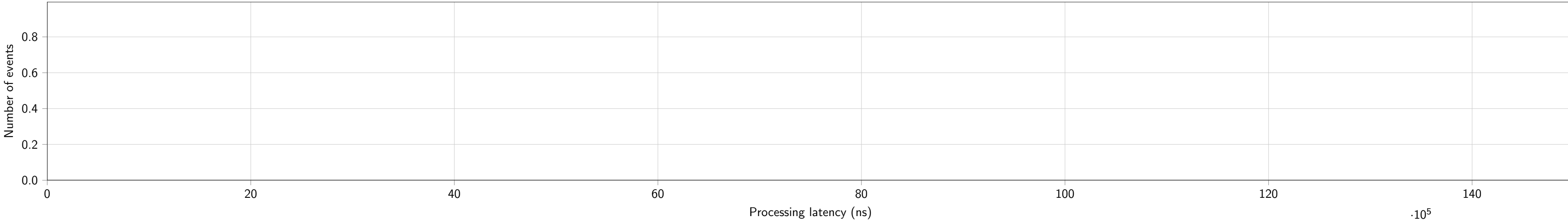




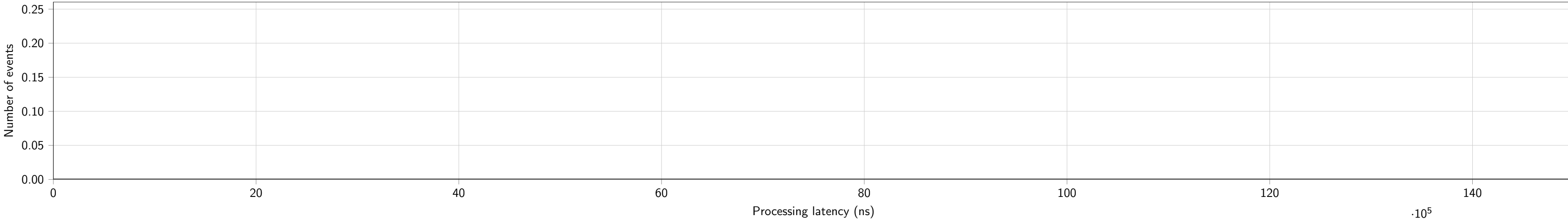
l2\_multimac\_10000000\_mbit3091hires.histogram.csv: tx: 6.03mpps, 0.04stdDev; rx: 5.98mpps, 0.02stdDev



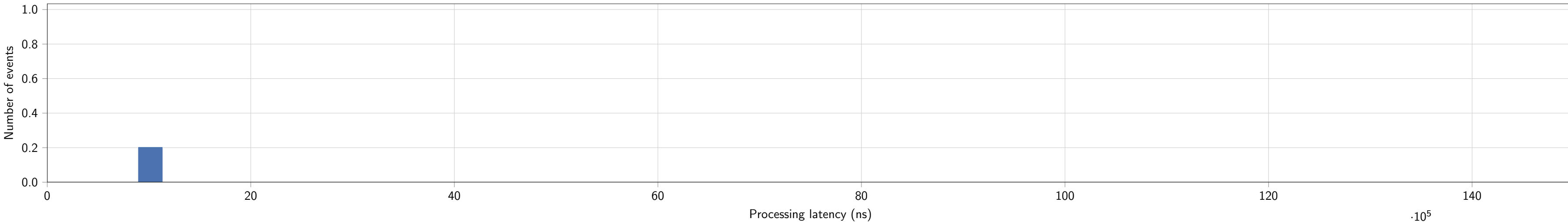
l2\_multimac\_10000000\_mbit3200.histogram.csv: tx: 6.24mpps, 0.04stdDev; rx: 5.96mpps, 0.02stdDev



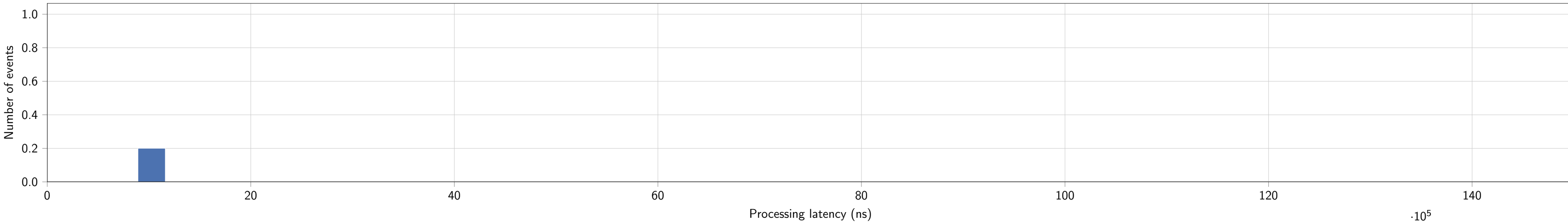
l2\_multimac\_10000000\_mbit3600.histogram.csv: tx: 7.05mpps, 0.05stdDev; rx: 5.98mpps, 0.01stdDev



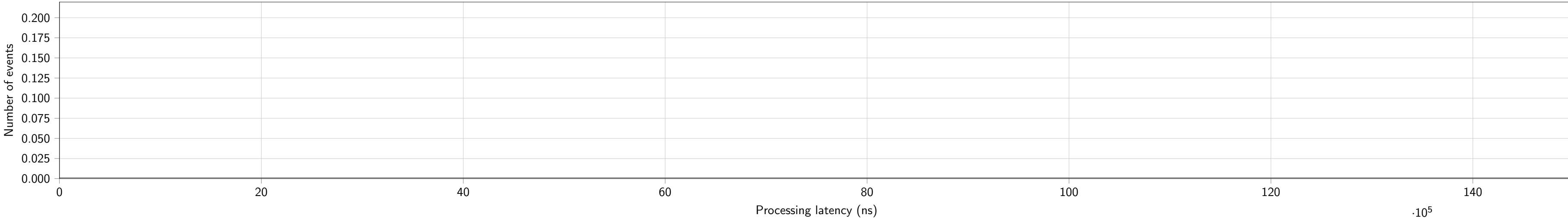
l2\_multimac\_10000000\_mbit4000.histogram.csv: tx: 7.80mpps, 0.05stdDev; rx: 5.89mpps, 0.01stdDev



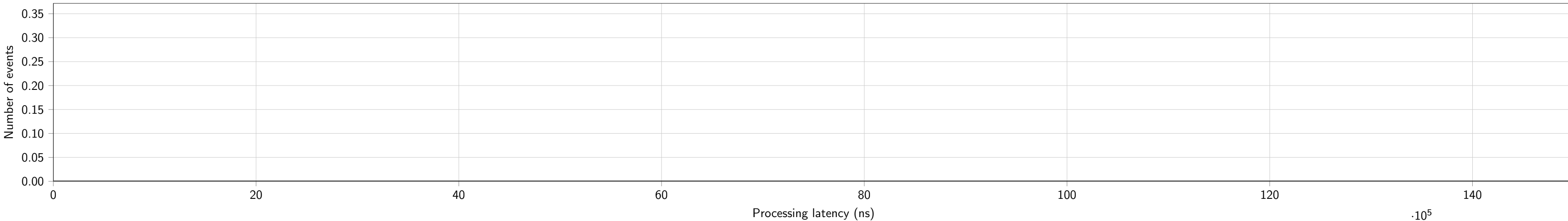
l2\_multimac\_10000000\_mbit4400.histogram.csv: tx: 8.61mpps, 0.05stdDev; rx: 5.96mpps, 0.01stdDev



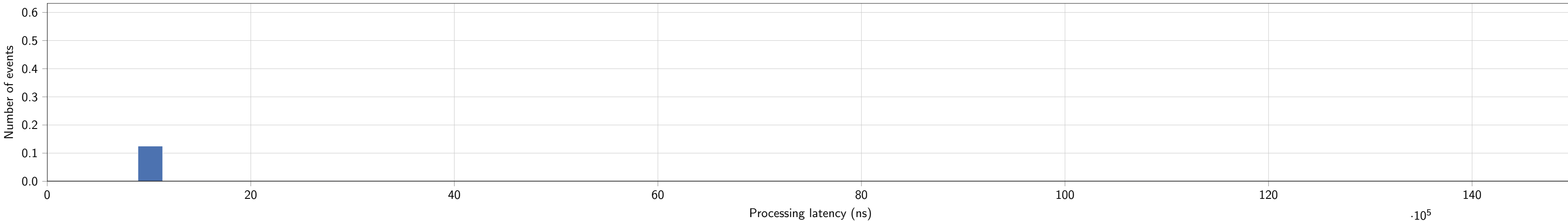
l2\_multimac\_10000000\_mbit4800.histogram.csv: tx: 9.39mpps, 0.05stdDev; rx: 5.95mpps, 0.00stdDev



l2\_multimac\_10000000\_mbit5200.histogram.csv: tx: 10.12mpps, 0.06stdDev; rx: 5.98mpps, 0.00stdDev

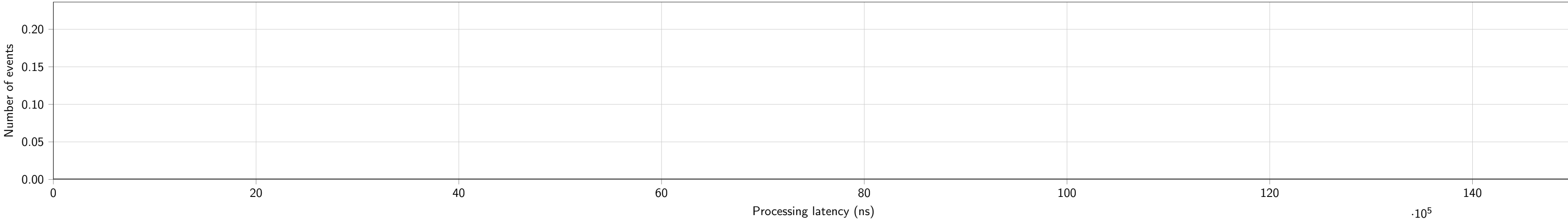


l2\_multimac\_10000000\_mbit5600.histogram.csv: tx: 10.15mpps, 0.05stdDev; rx: 5.95mpps, 0.00stdDev

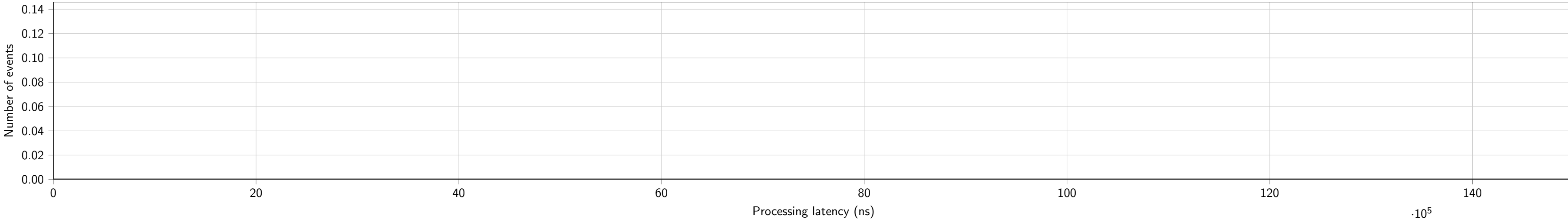


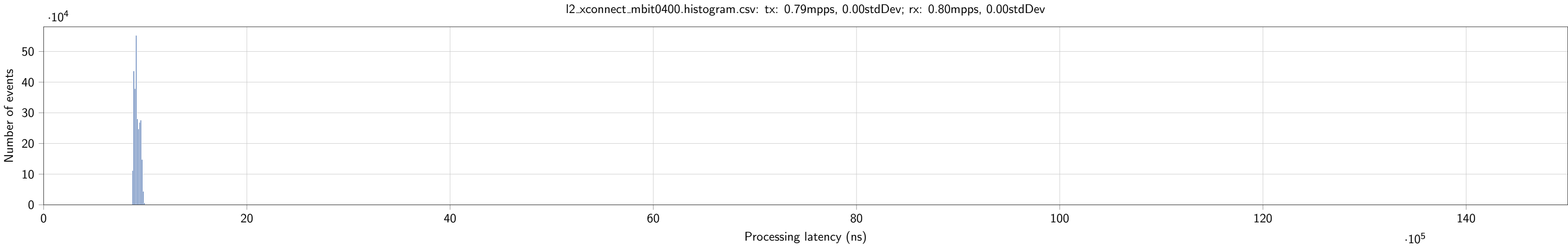


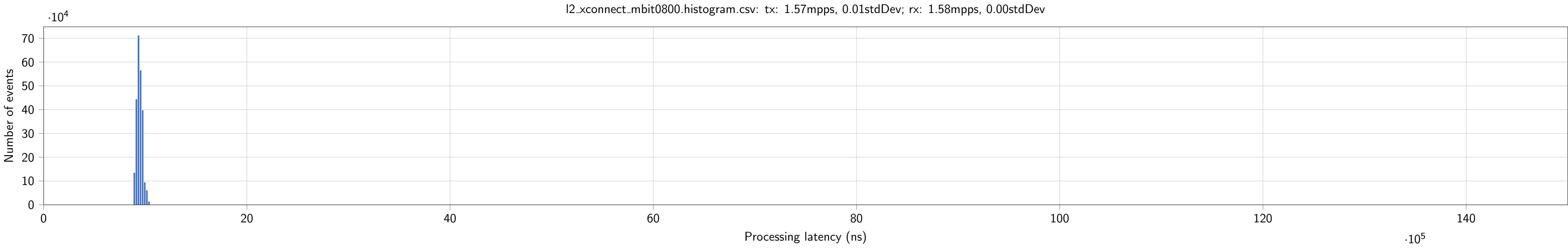
l2\_multimac\_10000000\_mbit6000.histogram.csv: tx: 10.13mpps, 0.05stdDev; rx: 5.96mpps, 0.00stdDev

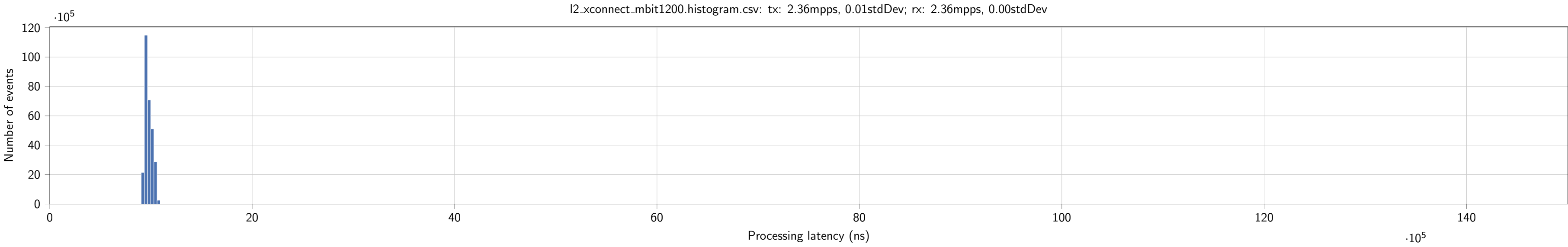


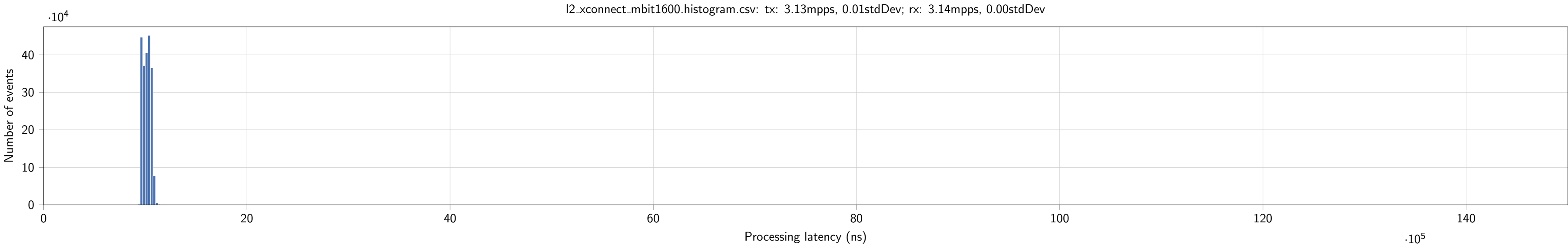
l2\_multimac\_10000000\_mbit9000.histogram.csv: tx: 10.15mpps, 0.05stdDev; rx: 5.94mpps, 0.00stdDev



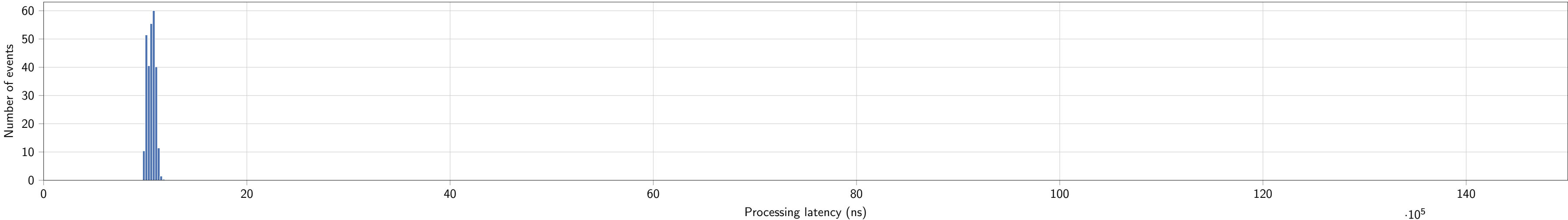






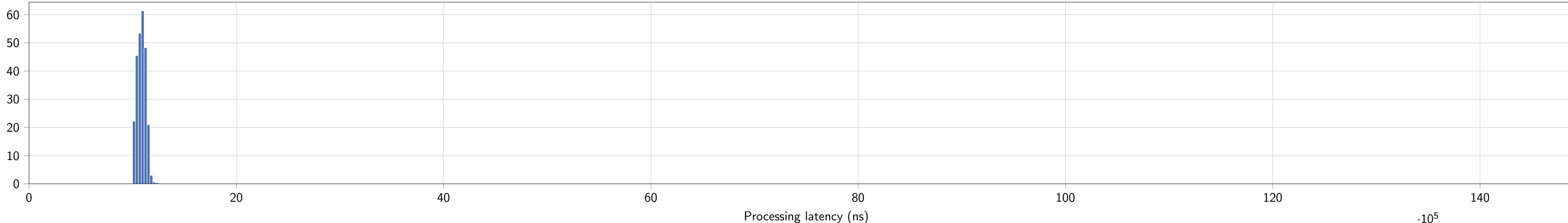


l2\_xconnect\_mbit2000.histogram.csv: tx: 3.92mpps, 0.02stdDev; rx: 3.92mpps, 0.00stdDev



l2\_xconnect\_mbit2400.histogram.csv: tx: 4.71mpps, 0.02stdDev; rx: 4.71mpps, 0.00stdDev

Number of events





l2\_xconnect\_mbit2800.histogram.csv: tx: 5.49mpps, 0.03stdDev; rx: 5.49mpps, 0.00stdDev

Number of events

$\cdot 10^4$

20

15

10

5

0

0

20

40

60

80

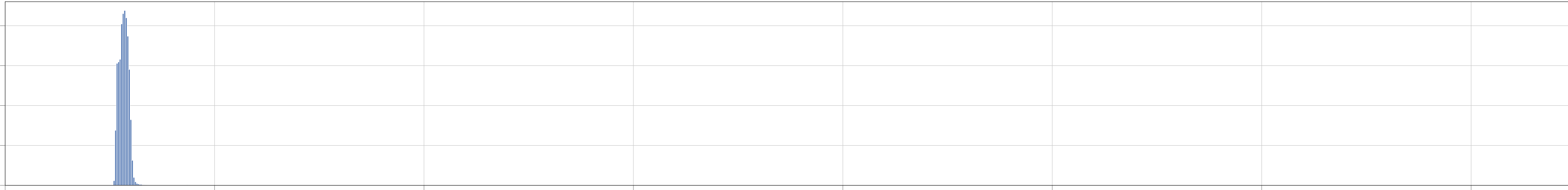
100

120

140

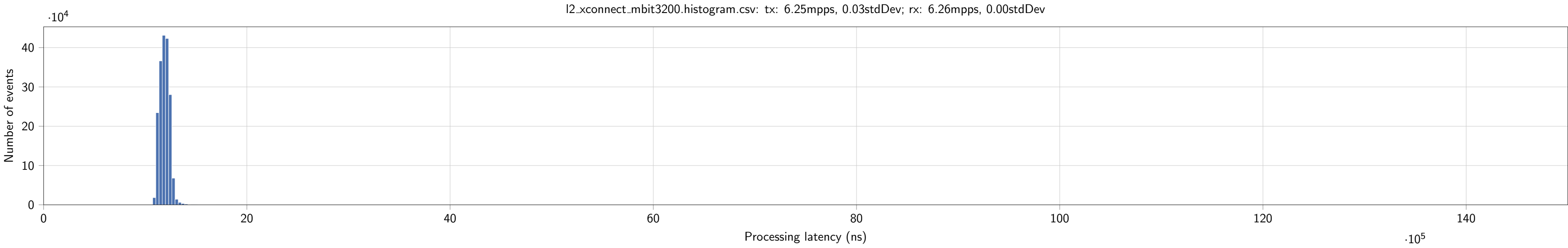
Processing latency (ns)

$\cdot 10^5$

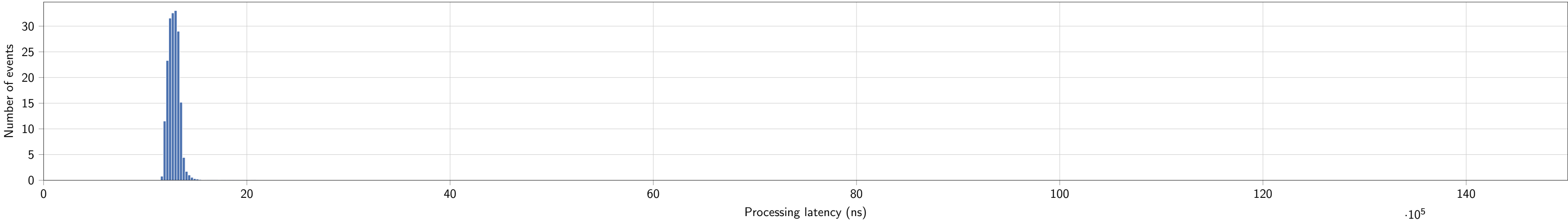


l2\_xconnect\_mbit3200.histogram.csv: tx: 6.25mpps, 0.03stdDev; rx: 6.26mpps, 0.00stdDev

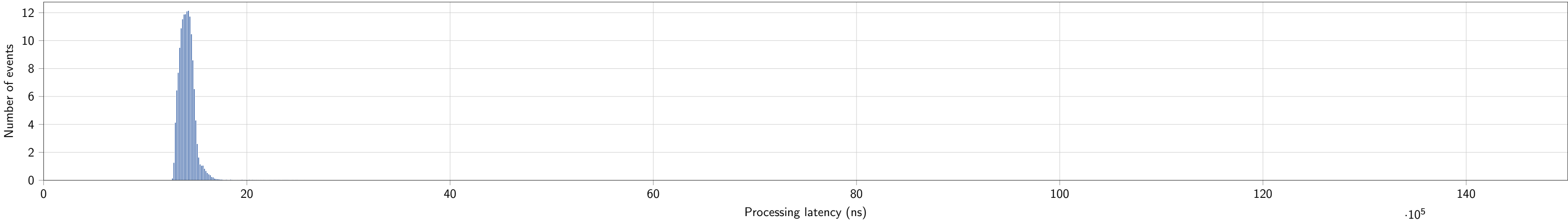
Number of events



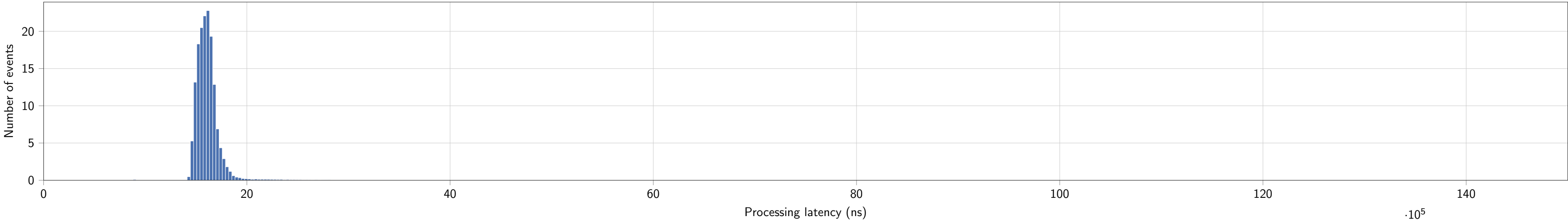
l2\_xconnect\_mbit3600.histogram.csv: tx: 7.06mpps, 0.03stdDev; rx: 7.07mpps, 0.00stdDev

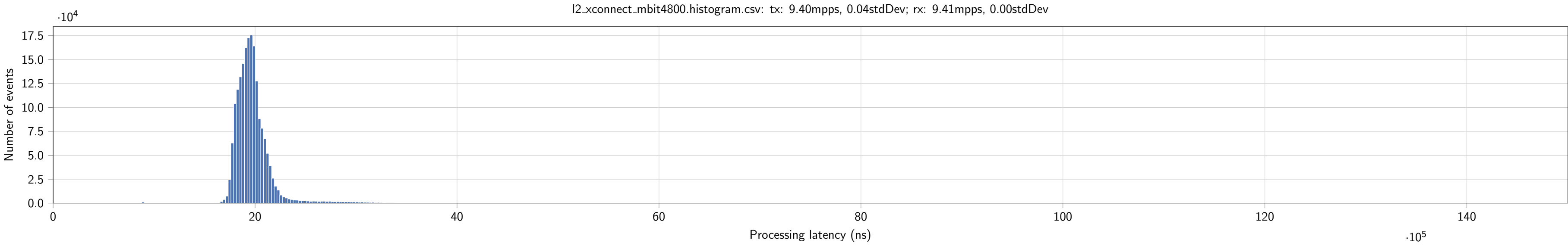


l2\_xconnect\_mbit4000.histogram.csv: tx: 7.81mpps, 0.04stdDev; rx: 7.82mpps, 0.00stdDev

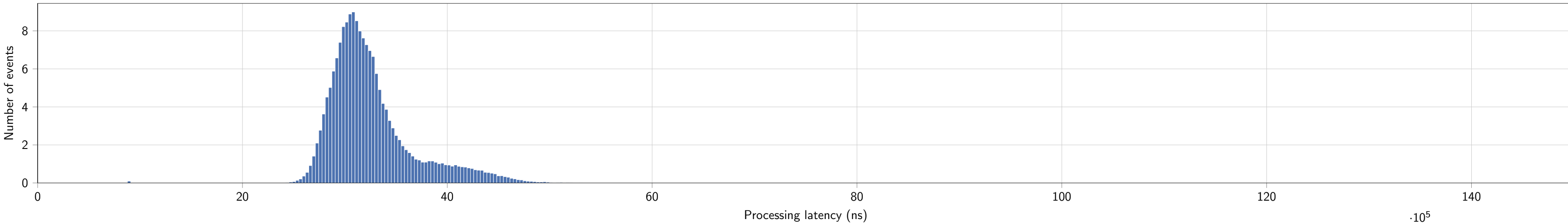


l2\_xconnect\_mbit4400.histogram.csv: tx: 8.62mpps, 0.05stdDev; rx: 8.63mpps, 0.00stdDev

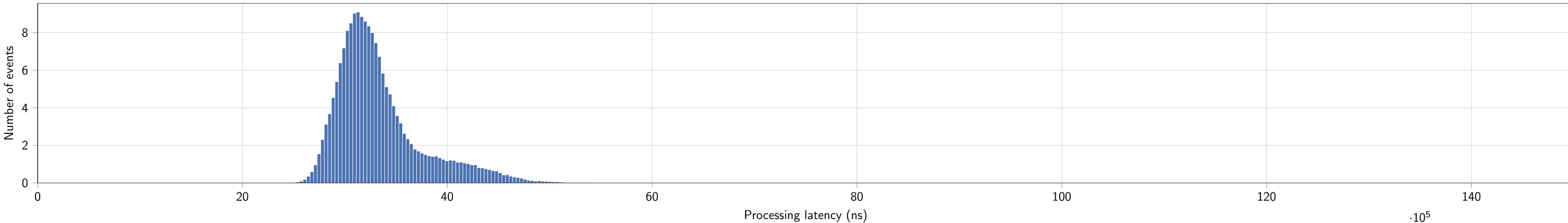




l2\_xconnect\_mbit5185hires.histogram.csv: tx: 10.16mpps, 0.05stdDev; rx: 10.17mpps, 0.00stdDev

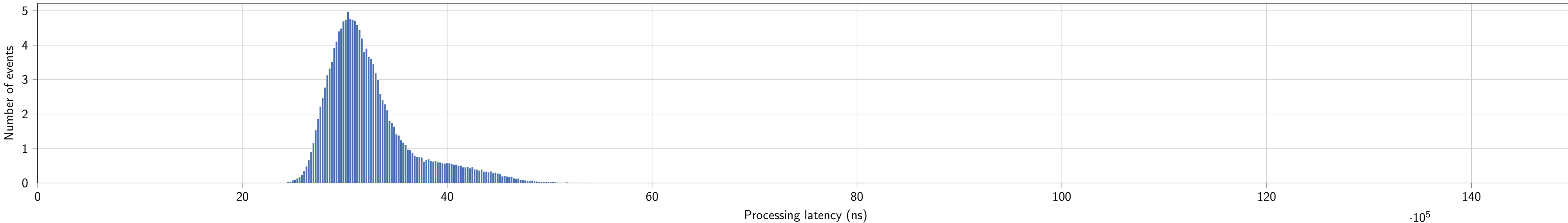


l2\_xconnect\_mbit5195hires.histogram.csv: tx: 10.16mpps, 0.05stdDev; rx: 10.17mpps, 0.00stdDev

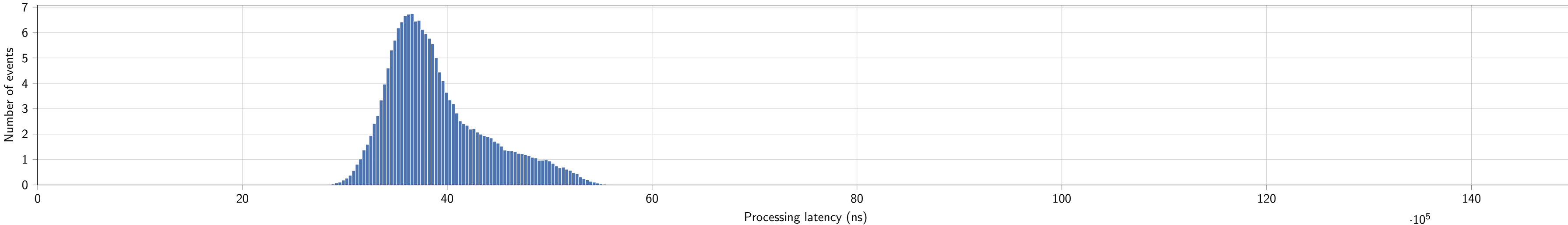




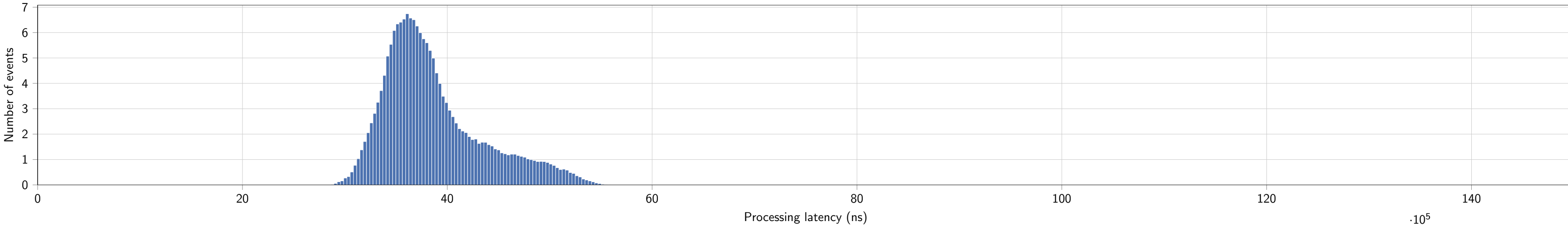
l2\_xconnect\_mbit5200.histogram.csv: tx: 10.16mpps, 0.05stdDev; rx: 10.17mpps, 0.00stdDev



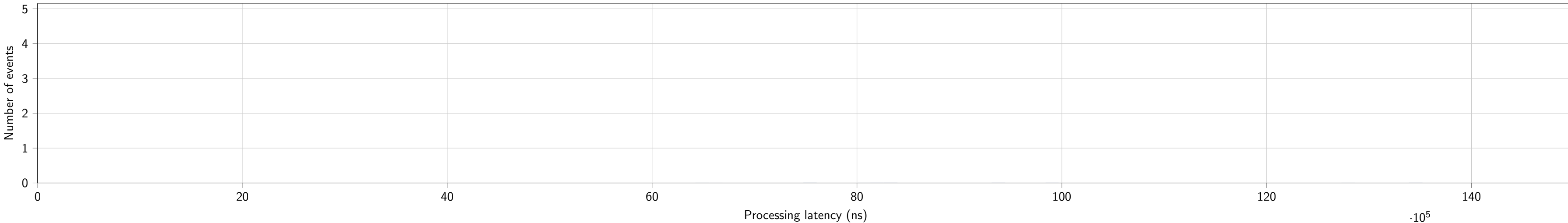
l2\_xconnect\_mbit5205\_final.histogram.csv: tx: 10.24mpps, 0.05stdDev; rx: 10.25mpps, 0.00stdDev



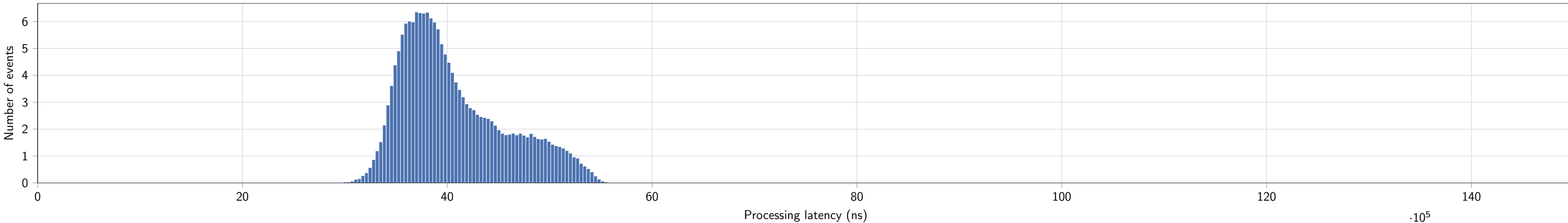
l2\_xconnect\_mbit5205hires.histogram.csv: tx: 10.24mpps, 0.05stdDev; rx: 10.25mpps, 0.00stdDev



l2\_xconnect\_mbit5215hires.histogram.csv: tx: 10.24mpps, 0.05stdDev; rx: 10.23mpps, 0.00stdDev

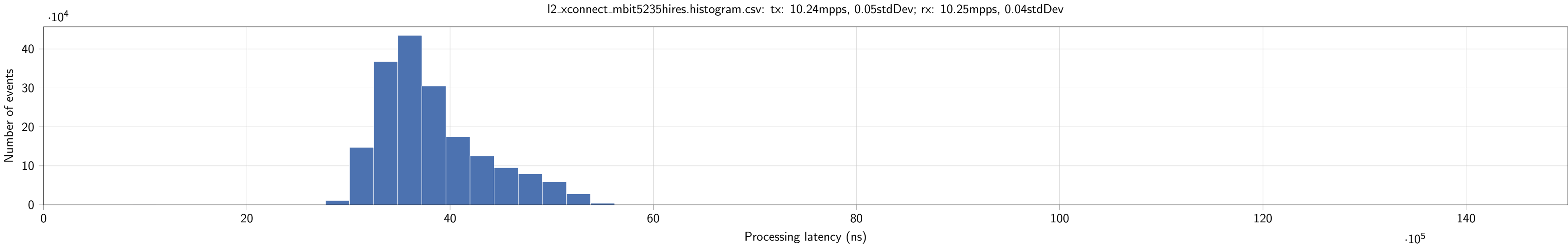


l2\_xconnect\_mbit5225hires.histogram.csv: tx: 10.24mpps, 0.05stdDev; rx: 10.25mpps, 0.00stdDev

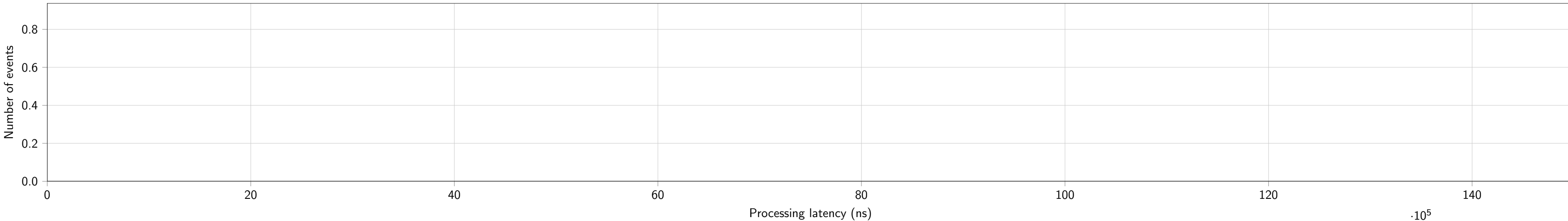


l2\_xconnect\_mbit5235hires.histogram.csv: tx: 10.24mpps, 0.05stdDev; rx: 10.25mpps, 0.04stdDev

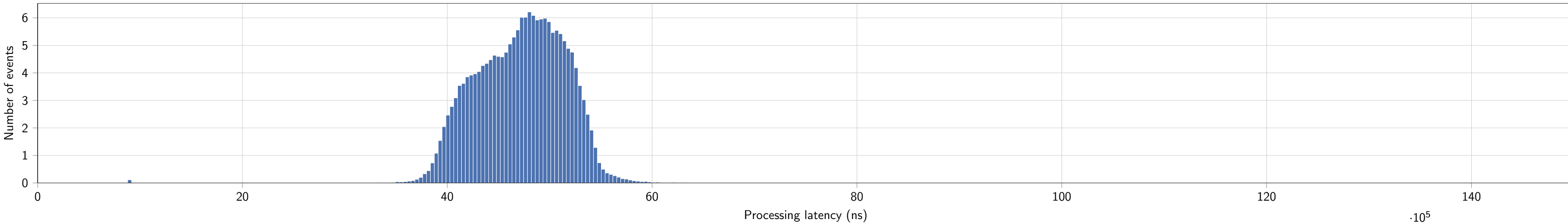
Number of events



l2\_xconnect\_mbit5245hires.histogram.csv: tx: 10.23mpps, 0.05stdDev; rx: 9.46mpps, 0.00stdDev

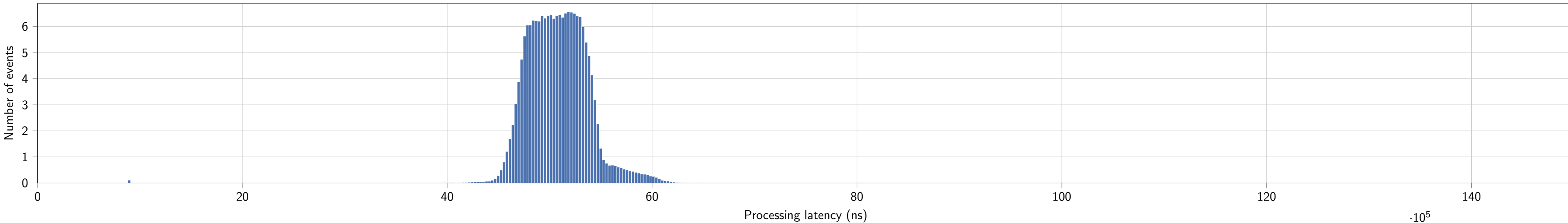


l2\_xconnect\_mbit5255hires.histogram.csv: tx: 10.33mpps, 0.05stdDev; rx: 10.34mpps, 0.00stdDev

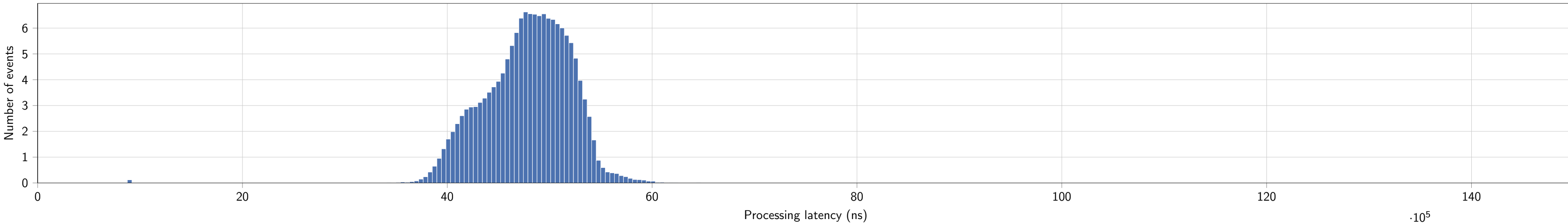




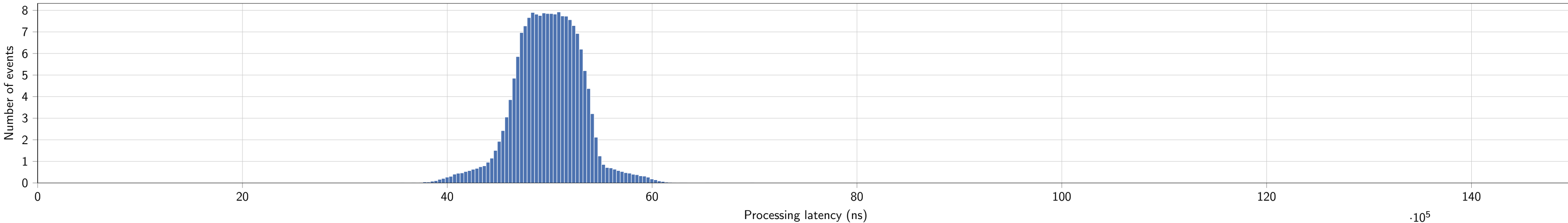
l2\_xconnect\_mbit5265hires.histogram.csv: tx: 10.33mpps, 0.05stdDev; rx: 10.34mpps, 0.00stdDev



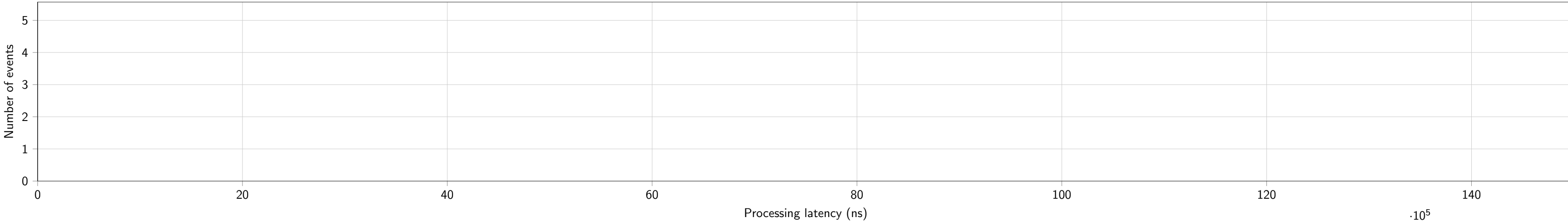
l2\_xconnect\_mbit5275hires.histogram.csv: tx: 10.33mpps, 0.06stdDev; rx: 10.34mpps, 0.00stdDev



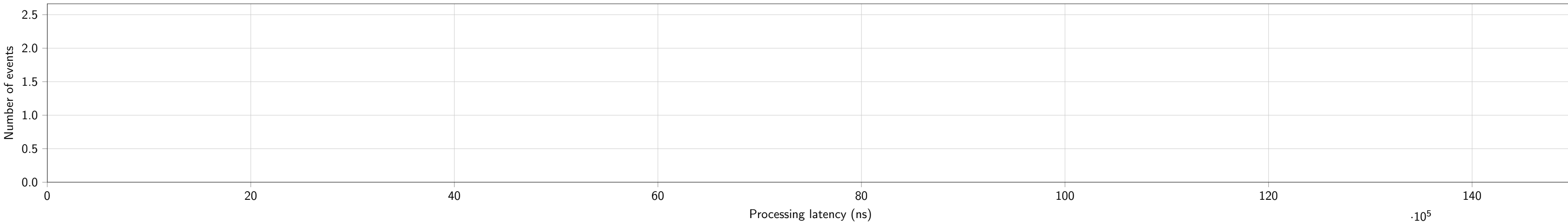
l2\_xconnect\_mbit5285hires.histogram.csv: tx: 10.33mpps, 0.05stdDev; rx: 10.34mpps, 0.00stdDev



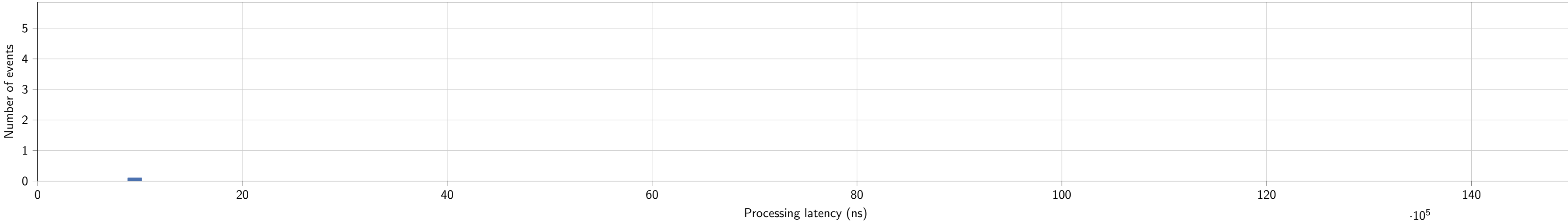
l2\_xconnect\_mbit5295hires.histogram.csv: tx: 10.41mpps, 0.05stdDev; rx: 10.34mpps, 0.00stdDev



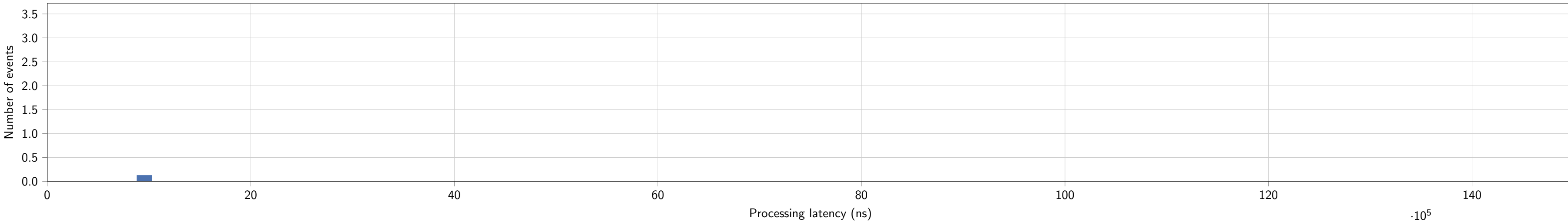
l2\_xconnect\_mbit5305hires.histogram.csv: tx: 10.41mpps, 0.05stdDev; rx: 10.22mpps, 0.00stdDev



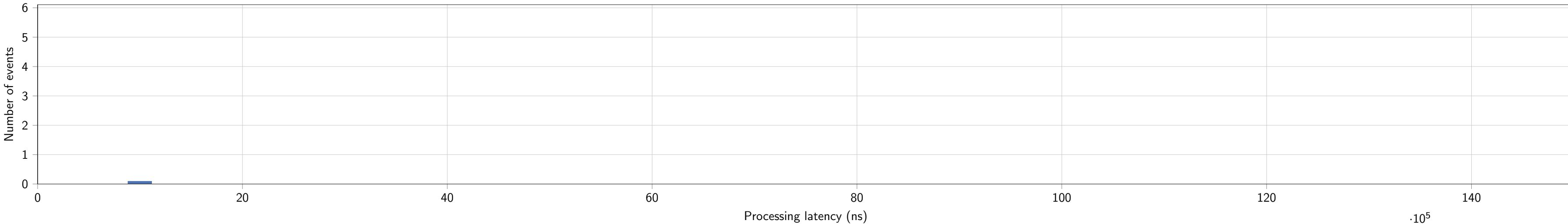
l2\_xconnect\_mbit5315hires.histogram.csv: tx: 10.41mpps, 0.05stdDev; rx: 10.34mpps, 0.00stdDev



l2\_xconnect\_mbit5325hires.histogram.csv: tx: 10.41mpps, 0.05stdDev; rx: 10.20mpps, 0.00stdDev

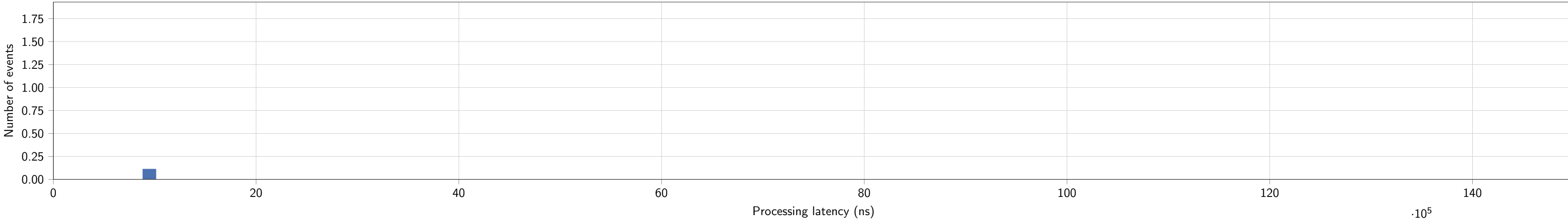


l2\_xconnect\_mbit5335hires.histogram.csv: tx: 10.49mpps, 0.05stdDev; rx: 10.37mpps, 0.04stdDev

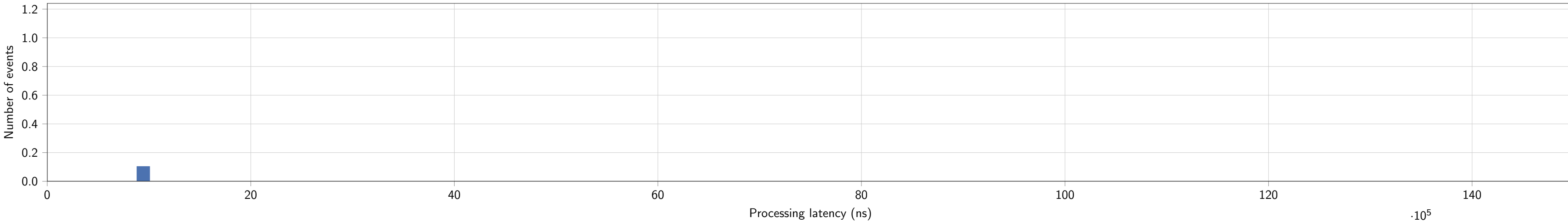




l2\_xconnect\_mbit5600.histogram.csv: tx: 10.95mpps, 0.05stdDev; rx: 10.33mpps, 0.00stdDev



l2\_xconnect\_mbit6000.histogram.csv: tx: 11.78mpps, 0.06stdDev; rx: 10.33mpps, 0.00stdDev



l2\_xconnect\_mbit9000.histogram.csv: tx: 14.86mpps, 0.07stdDev; rx: 10.32mpps, 0.00stdDev

