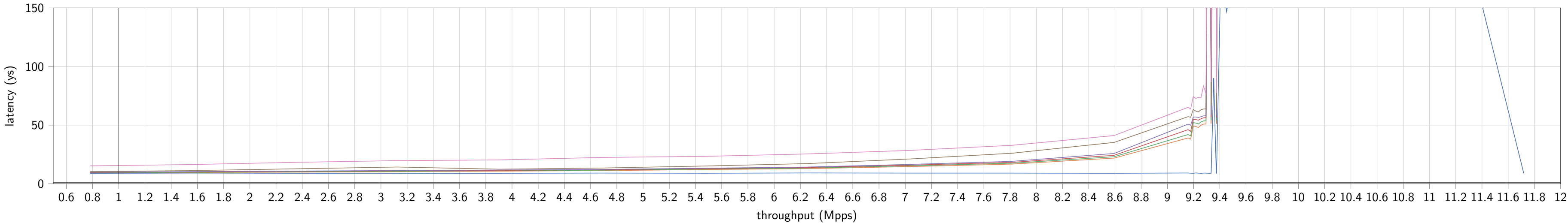
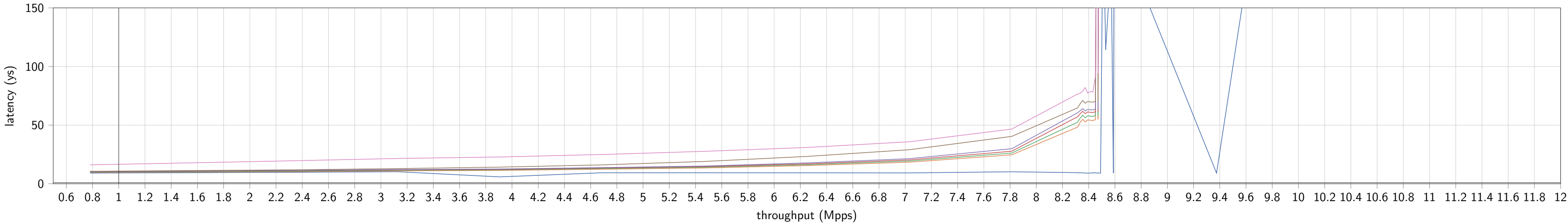


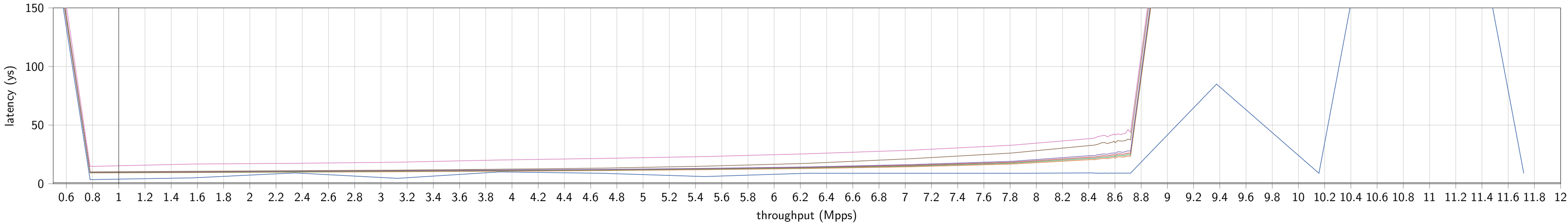
l2_bridging_cnf0_mbit*



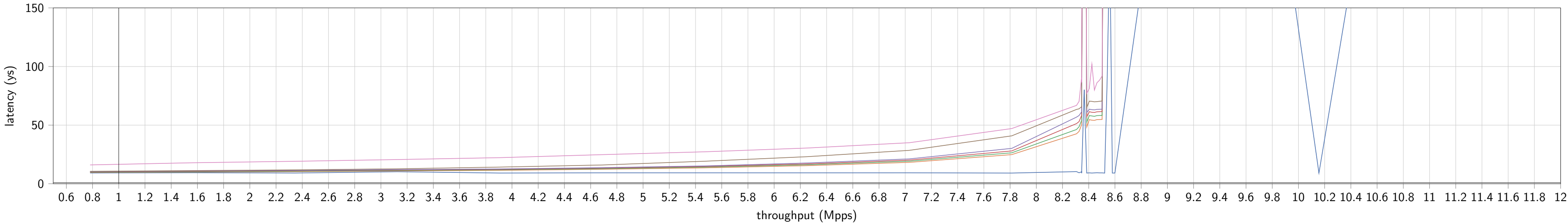
l2_bridging_cnf1_mbit*



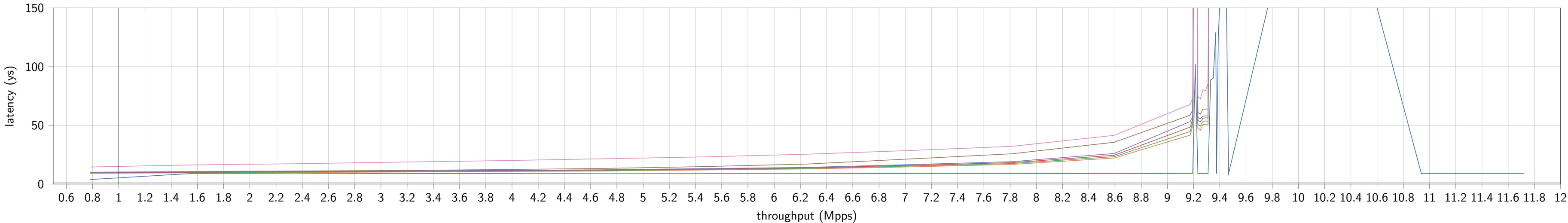
l2_bridging_cnf2_mbit*



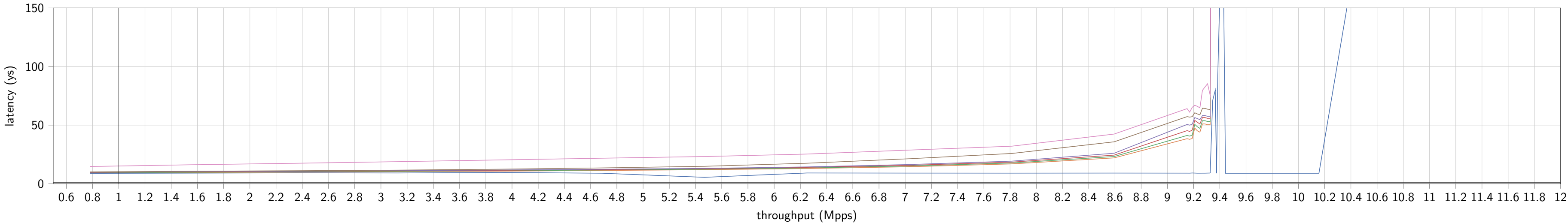
l2_bridging_cnf3_mbit*



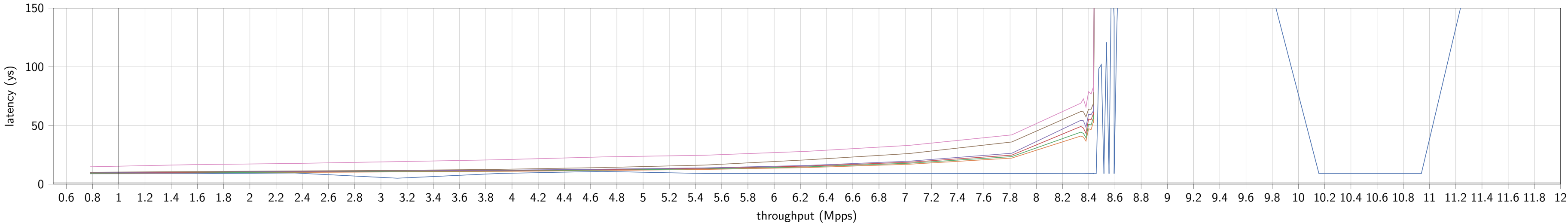
l2_bridging_cnf4_mbit*



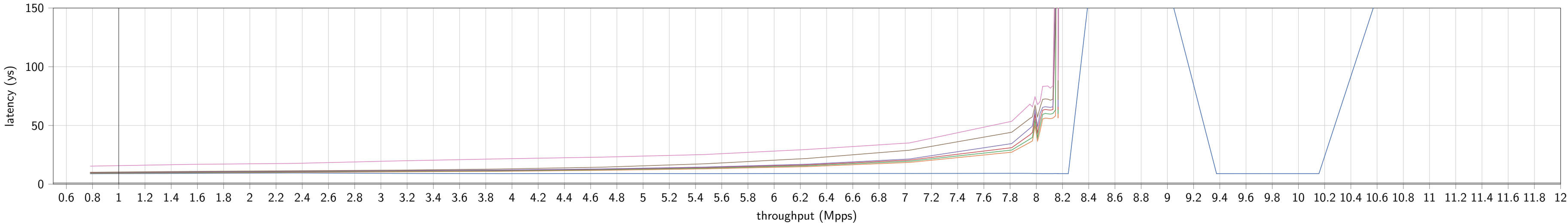
l2_bridging_cnf5_mbit*



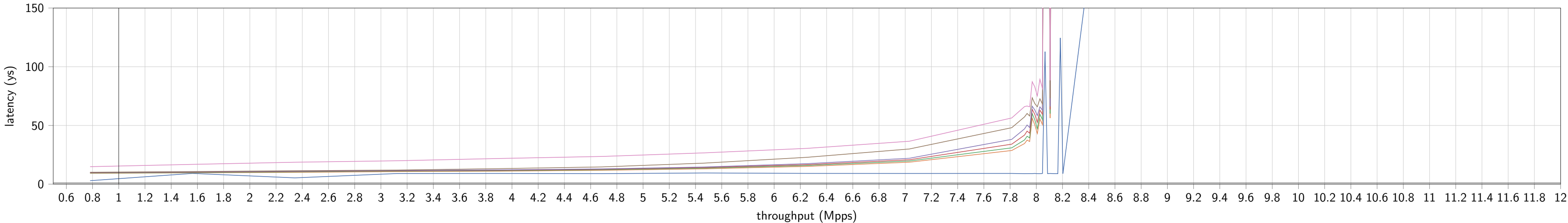
l2_multimac_00000100_mbit*



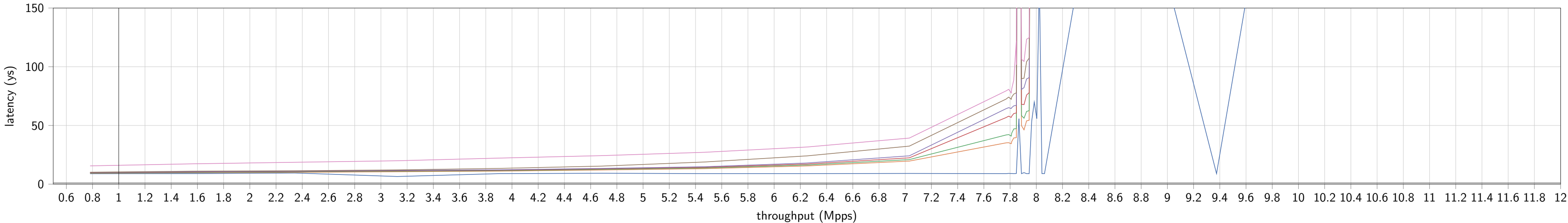
l2_multimac_00001000_mbit*



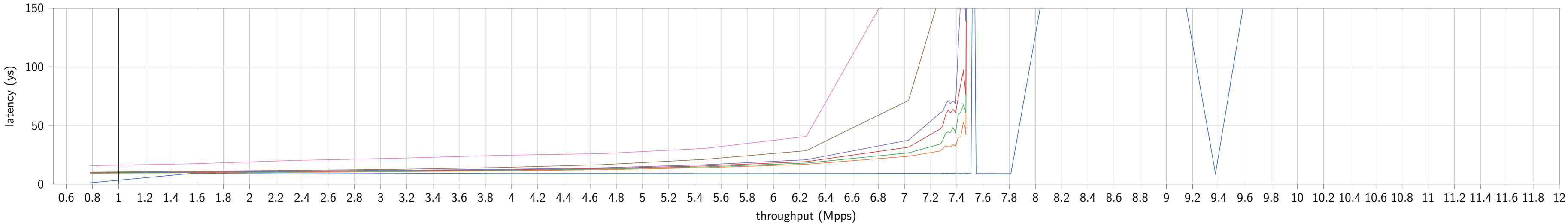
l2_multimac_00010000_mbit*



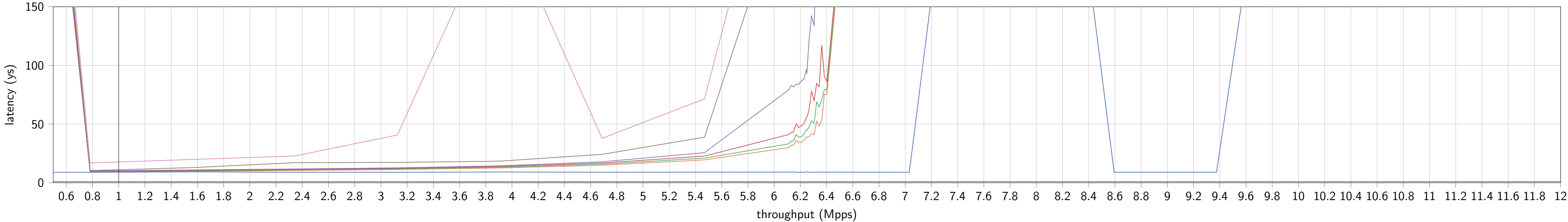
l2_multimac_00100000_mbit*

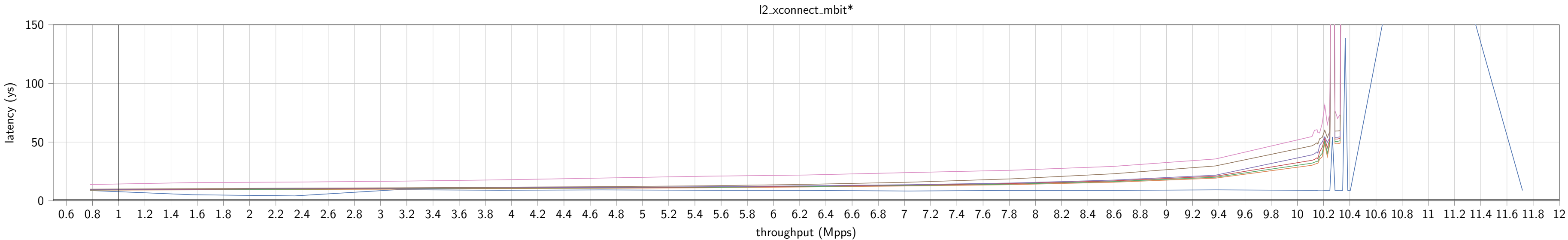


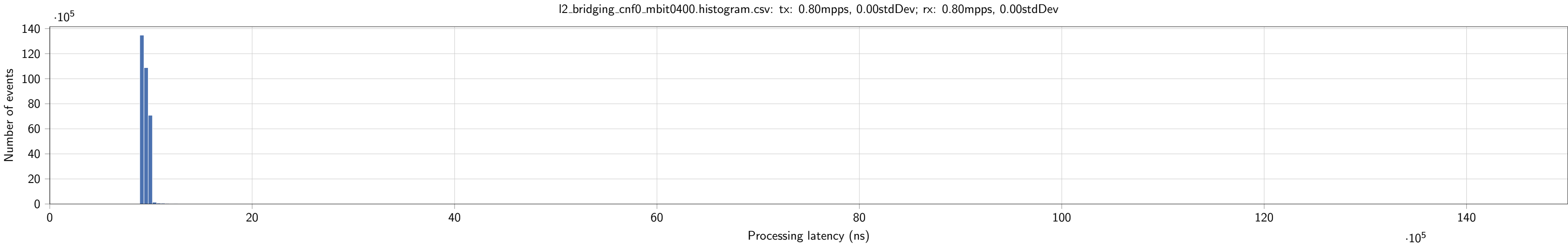
l2_multimac_01000000_mbit*



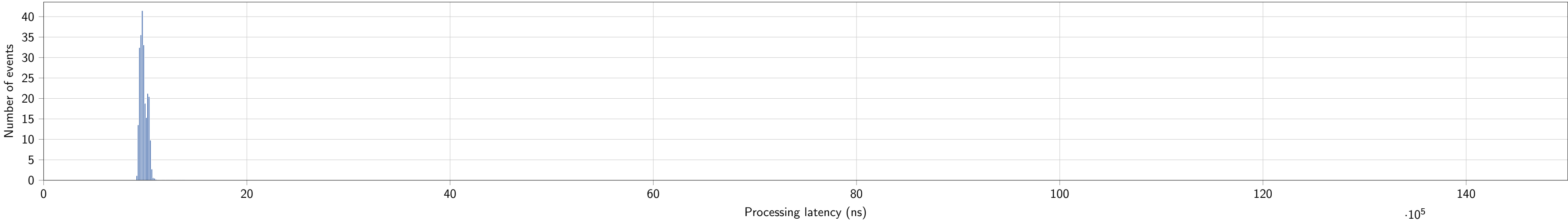
l2_multimac_10000000_mbit*

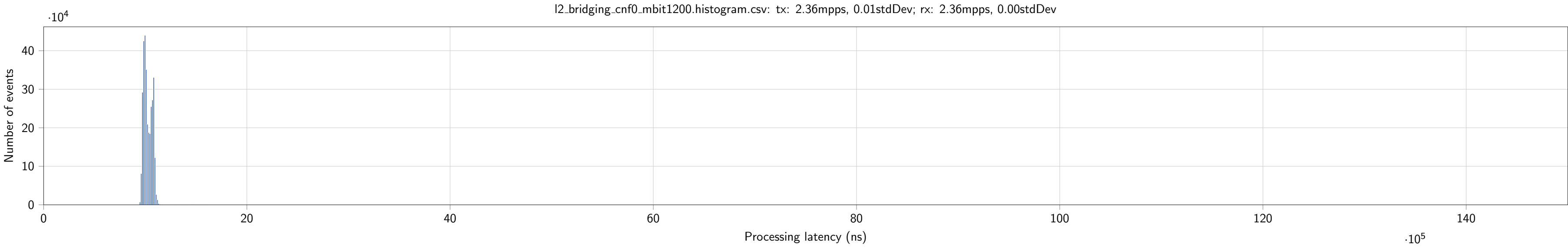


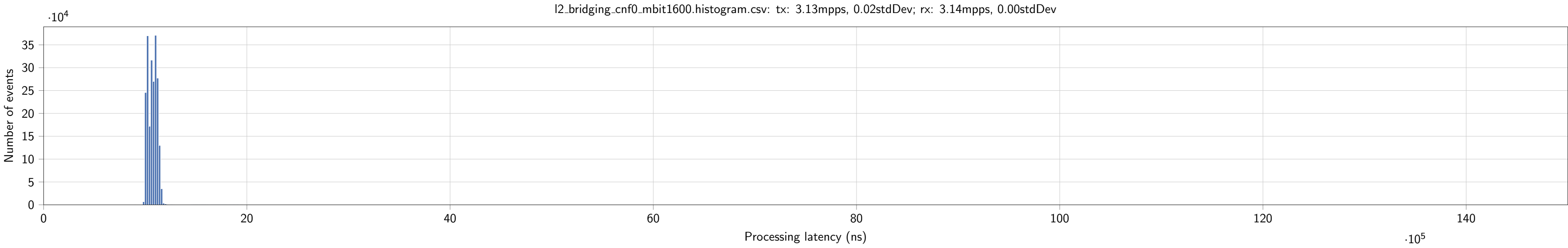




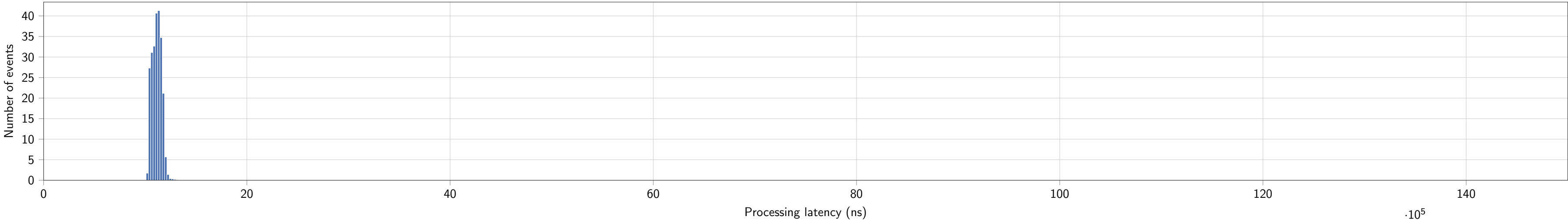
l2_bridging_cnf0_mbit0800.histogram.csv: tx: 1.57mpps, 0.01stdDev; rx: 1.58mpps, 0.00stdDev



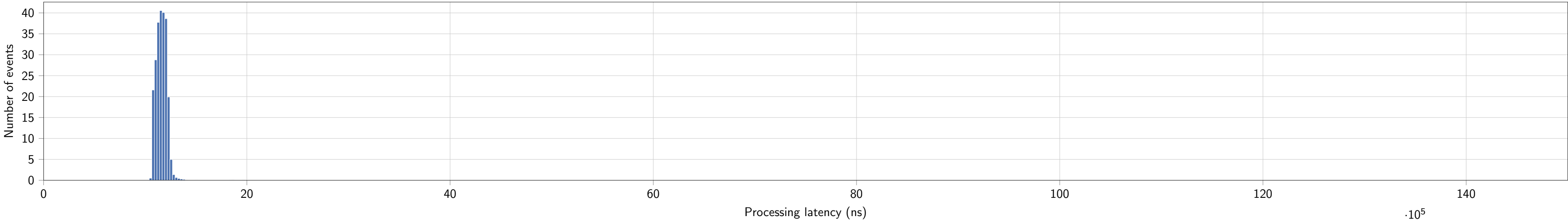


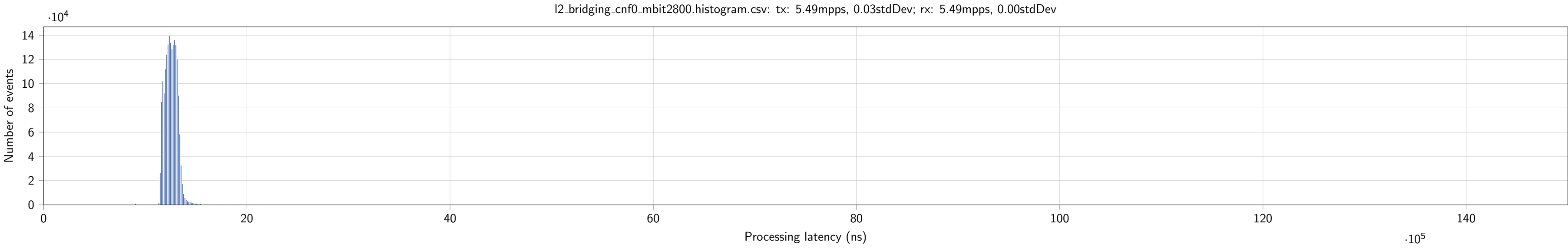


l2_bridging_cnf0_mbit2000.histogram.csv: tx: 3.91mpps, 0.02stdDev; rx: 3.92mpps, 0.00stdDev



l2_bridging_cnf0_mbit2400.histogram.csv: tx: 4.71mpps, 0.02stdDev; rx: 4.71mpps, 0.00stdDev





l2_bridging_cnf0_mbit3200.histogram.csv: tx: 6.25mpps, 0.03stdDev; rx: 6.26mpps, 0.00stdDev

Number of events

25
20
15
10
5
0

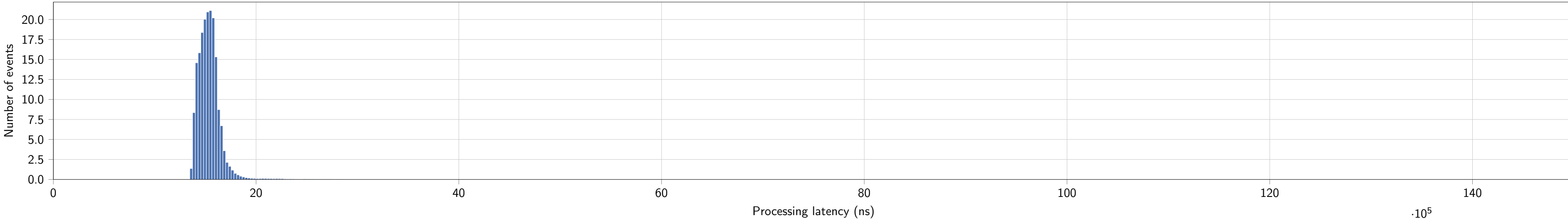
0 20 40 60 80 100 120 140

Processing latency (ns)

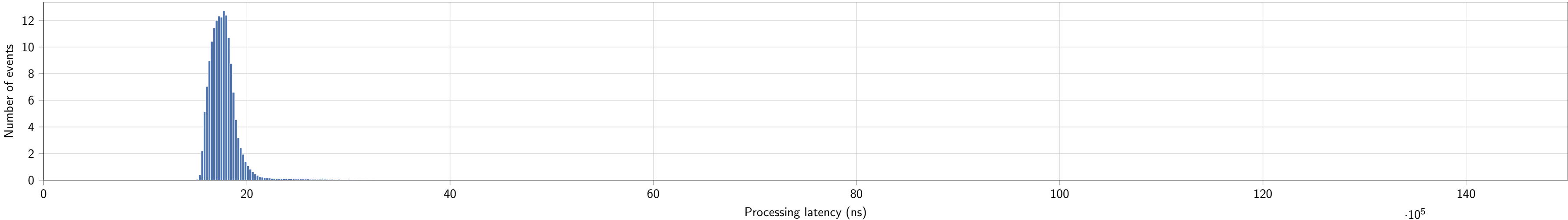
$\cdot 10^5$



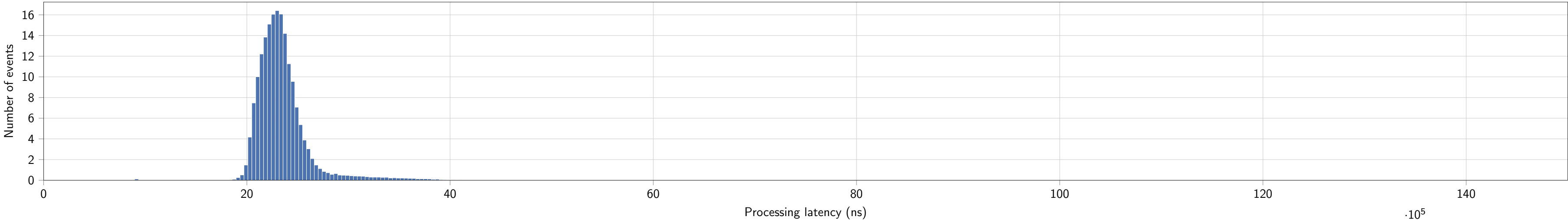
l2_bridging_cnf0_mbit3600.histogram.csv: tx: 7.06mpps, 0.03stdDev; rx: 7.07mpps, 0.00stdDev



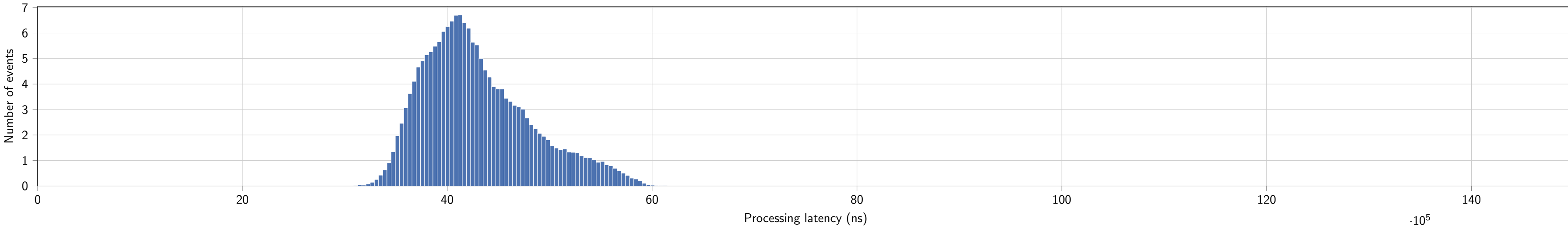
l2_bridging_cnf0_mbit4000.histogram.csv: tx: 7.81mpps, 0.04stdDev; rx: 7.82mpps, 0.00stdDev



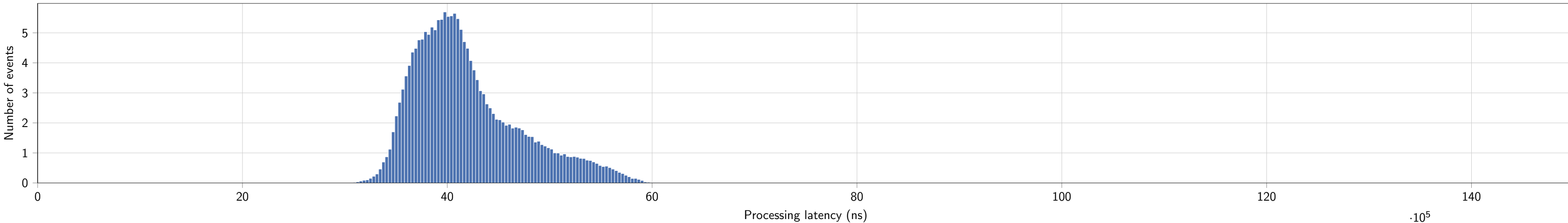
l2_bridging_cnf0_mbit4400.histogram.csv: tx: 8.62mpps, 0.04stdDev; rx: 8.63mpps, 0.00stdDev



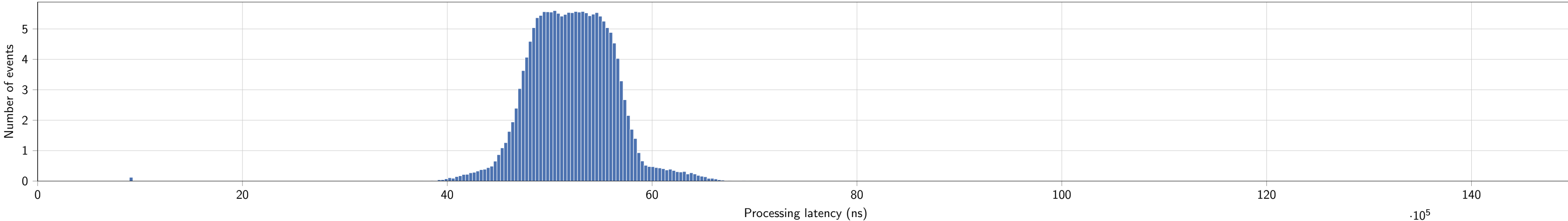
l2_bridging_cnf0_mbit4689hires.histogram.csv: tx: 9.19mpps, 0.04stdDev; rx: 9.20mpps, 0.00stdDev



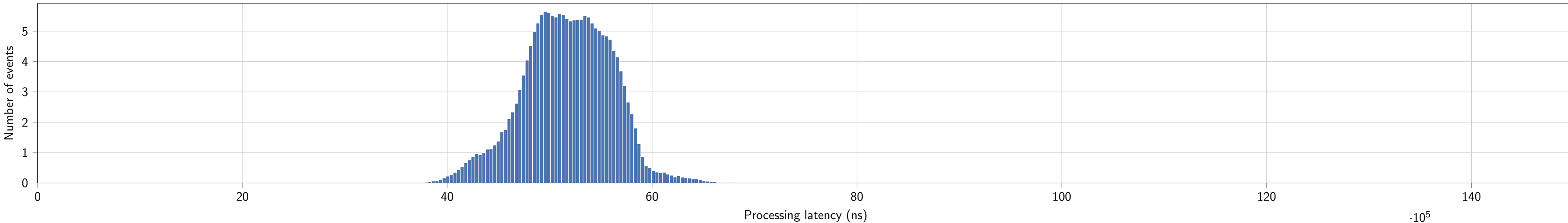
l2_bridging_cnf0_mbit4699hires.histogram.csv: tx: 9.19mpps, 0.04stdDev; rx: 9.20mpps, 0.00stdDev



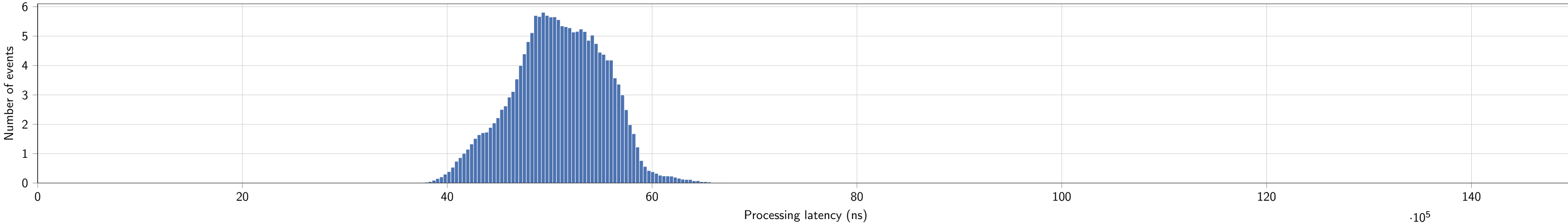
l2_bridging_cnf0_mbit4709hires.histogram.csv: tx: 9.26mpps, 0.04stdDev; rx: 9.27mpps, 0.00stdDev



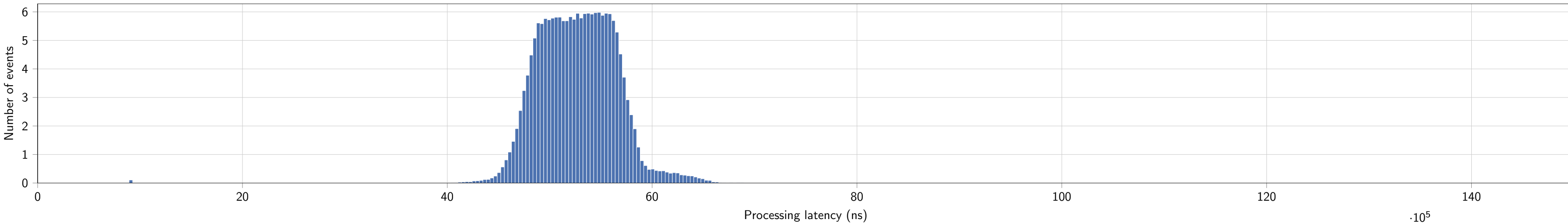
l2_bridging_cnf0_mbit4719hires.histogram.csv: tx: 9.26mpps, 0.04stdDev; rx: 9.27mpps, 0.00stdDev



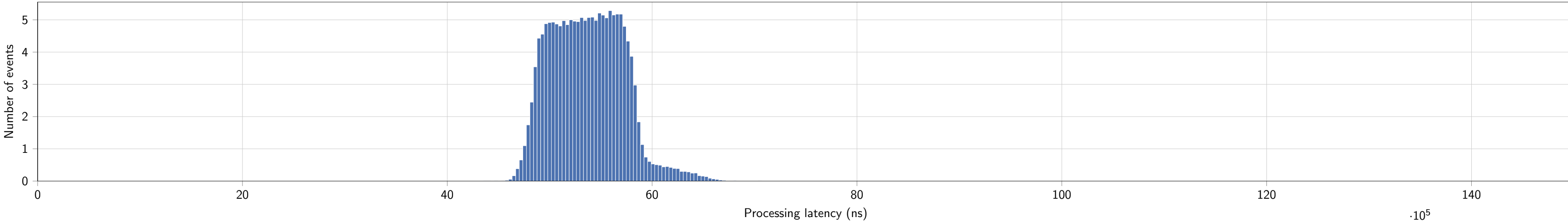
l2_bridging_cnf0_mbit4729hires.histogram.csv: tx: 9.26mpps, 0.04stdDev; rx: 9.27mpps, 0.00stdDev



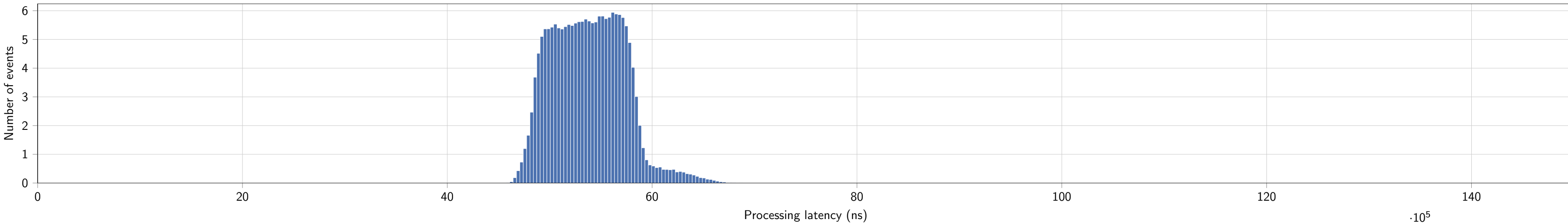
l2_bridging_cnf0_mbit4739hires.histogram.csv: tx: 9.26mpps, 0.05stdDev; rx: 9.27mpps, 0.00stdDev



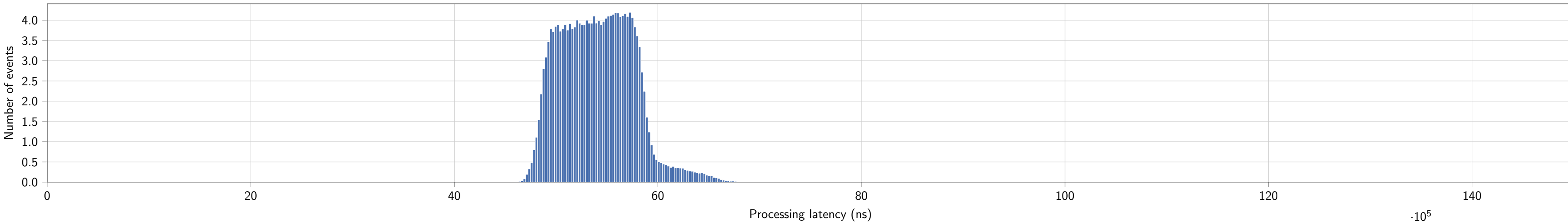
l2_bridging_cnf0_mbit4749hires.histogram.csv: tx: 9.33mpps, 0.05stdDev; rx: 9.34mpps, 0.00stdDev



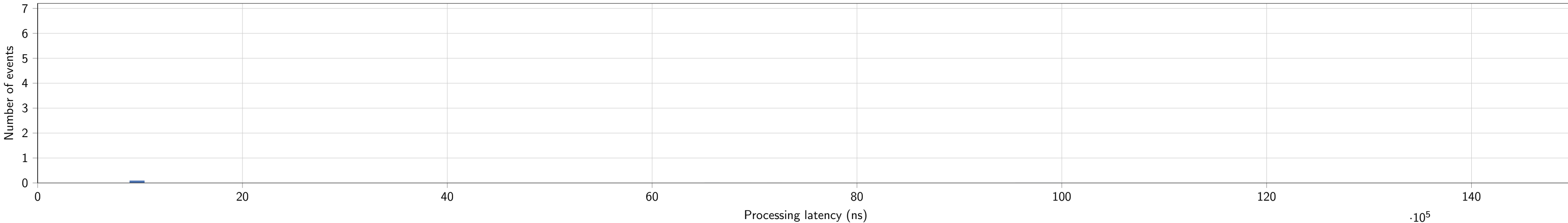
l2_bridging_cnf0_mbit4759_final.histogram.csv: tx: 9.33mpps, 0.05stdDev; rx: 9.34mpps, 0.00stdDev



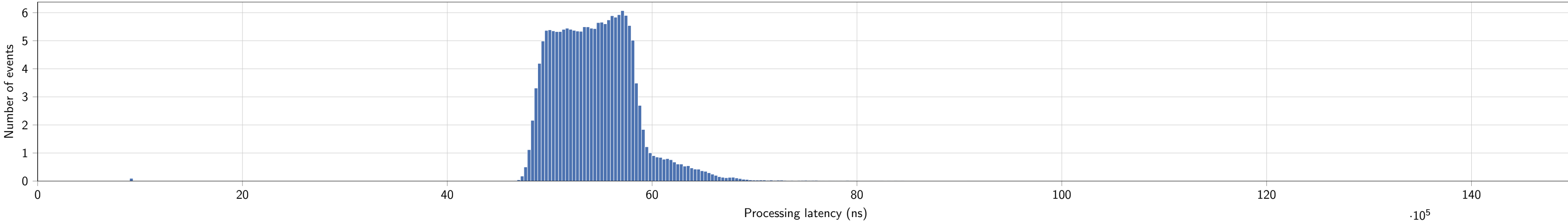
l2_bridging_cnf0_mbit4759hires.histogram.csv: tx: 9.33mpps, 0.04stdDev; rx: 9.34mpps, 0.00stdDev



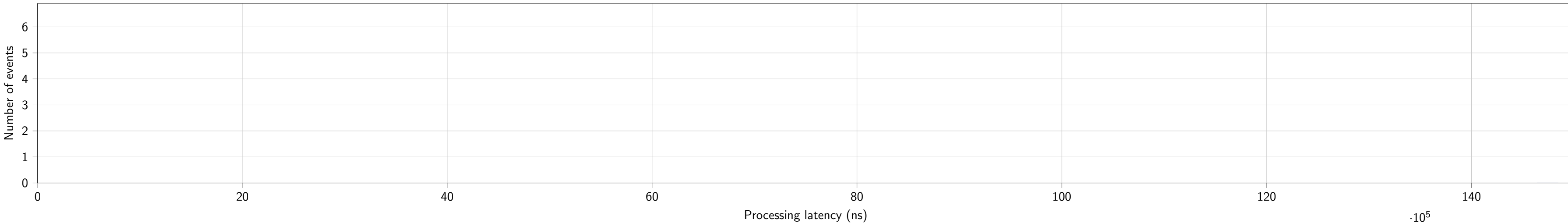
l2_bridging_cnf0_mbit4769hires.histogram.csv: tx: 9.32mpps, 0.04stdDev; rx: 9.32mpps, 0.00stdDev



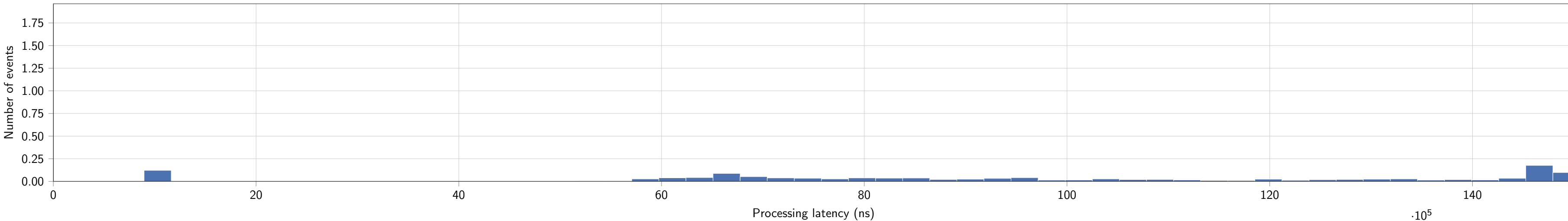
l2_bridging_cnf0_mbit4779hires.histogram.csv: tx: 9.40mpps, 0.05stdDev; rx: 9.41mpps, 0.00stdDev



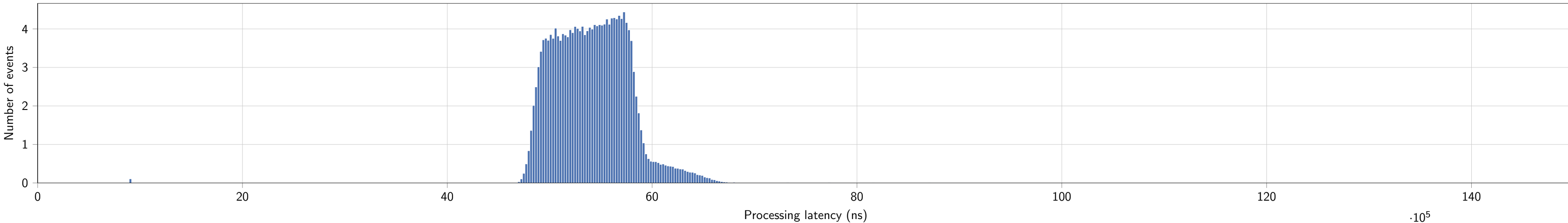
l2_bridging_cnf0_mbit4789hires.histogram.csv: tx: 9.39mpps, 0.05stdDev; rx: 9.37mpps, 0.00stdDev



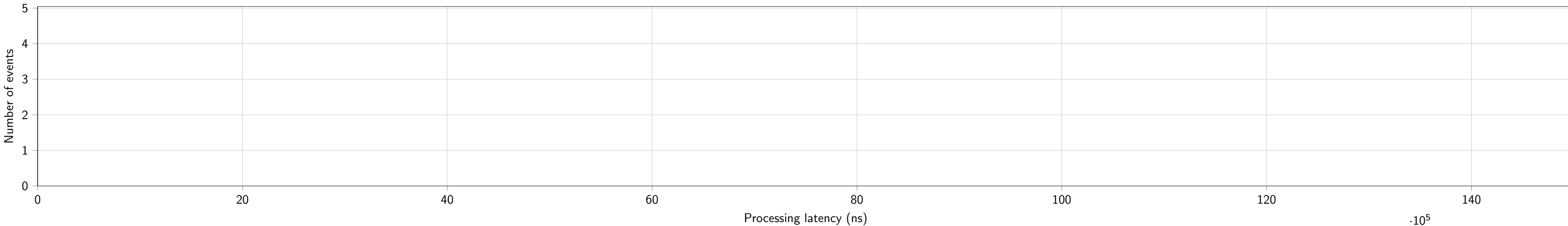
l2_bridging_cnf0_mbit4799hires.histogram.csv: tx: 9.39mpps, 0.04stdDev; rx: 9.39mpps, 0.04stdDev



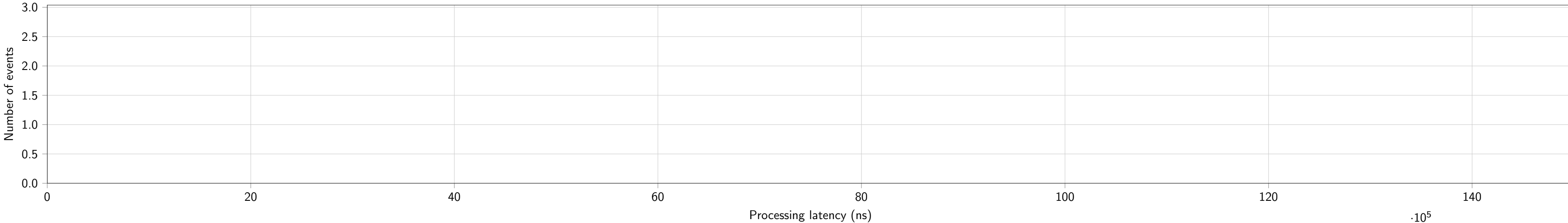
l2_bridging_cnf0_mbit4800.histogram.csv: tx: 9.40mpps, 0.05stdDev; rx: 9.41mpps, 0.00stdDev



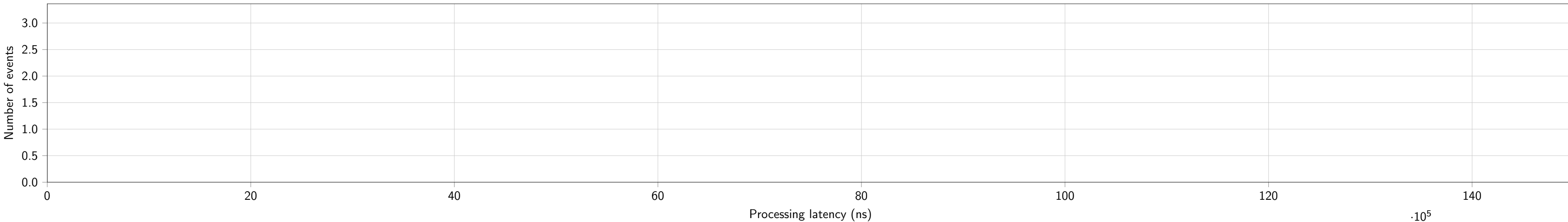
l2_bridging_cnf0_mbit4809hires.histogram.csv: tx: 9.39mpps, 0.05stdDev; rx: 9.36mpps, 0.00stdDev



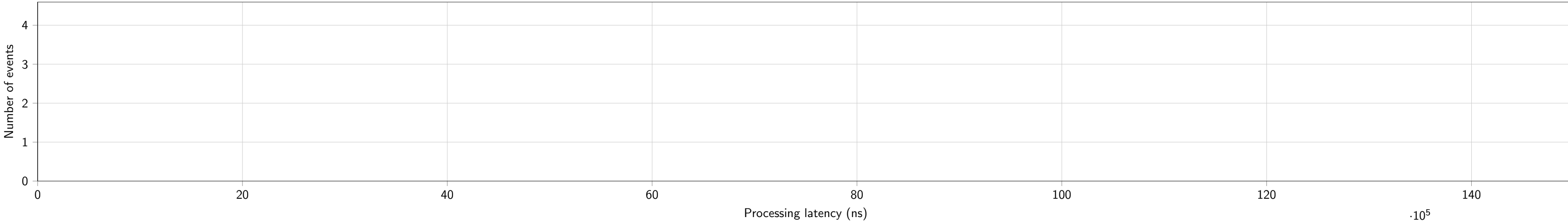
l2_bridging_cnf0_mbit4819hires.histogram.csv: tx: 9.46mpps, 0.05stdDev; rx: 9.35mpps, 0.00stdDev



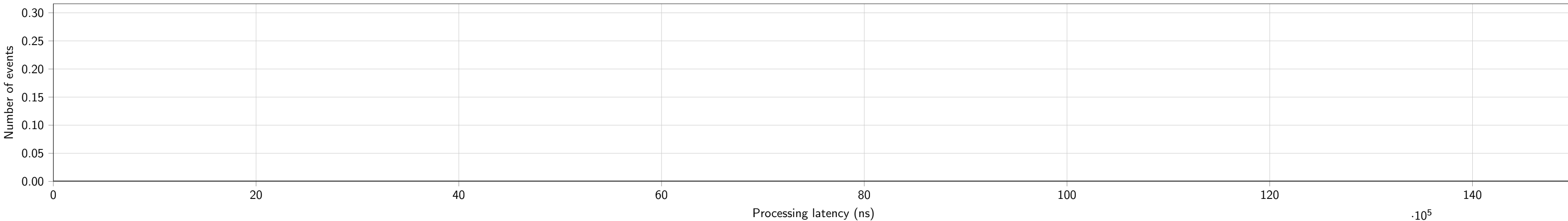
l2_bridging_cnf0_mbit4829hires.histogram.csv: tx: 9.46mpps, 0.04stdDev; rx: 9.37mpps, 0.00stdDev



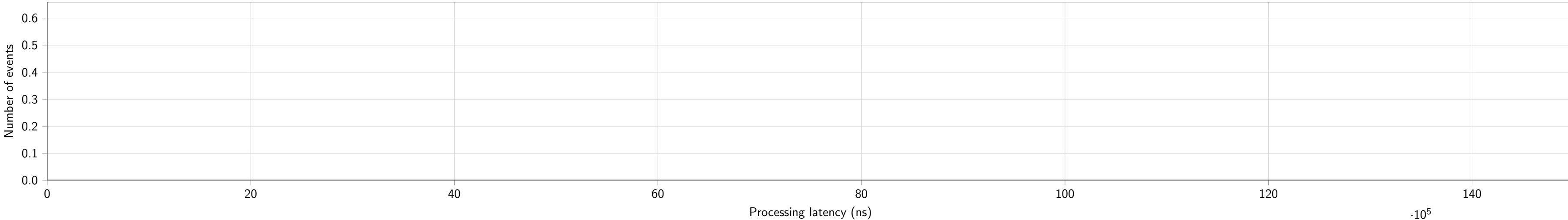
l2_bridging_cnf0_mbit4839hires.histogram.csv: tx: 9.46mpps, 0.05stdDev; rx: 9.40mpps, 0.00stdDev



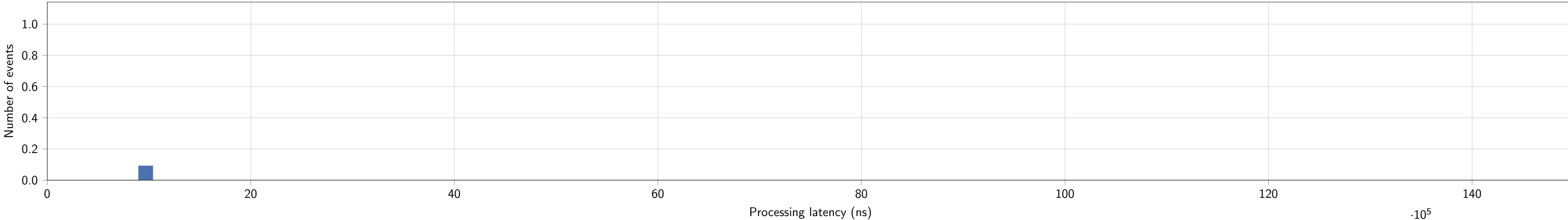
l2_bridging_cnf0_mbit5200.histogram.csv: tx: 10.15mpps, 0.05stdDev; rx: 9.22mpps, 0.00stdDev



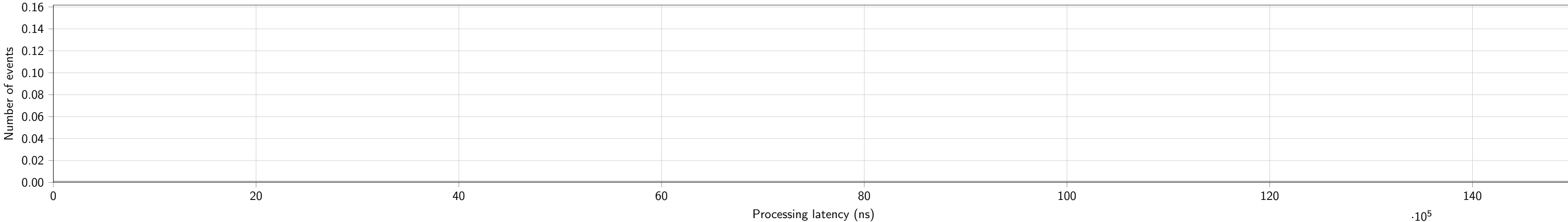
l2_bridging_cnf0_mbit5600.histogram.csv: tx: 10.95mpps, 0.05stdDev; rx: 9.36mpps, 0.00stdDev

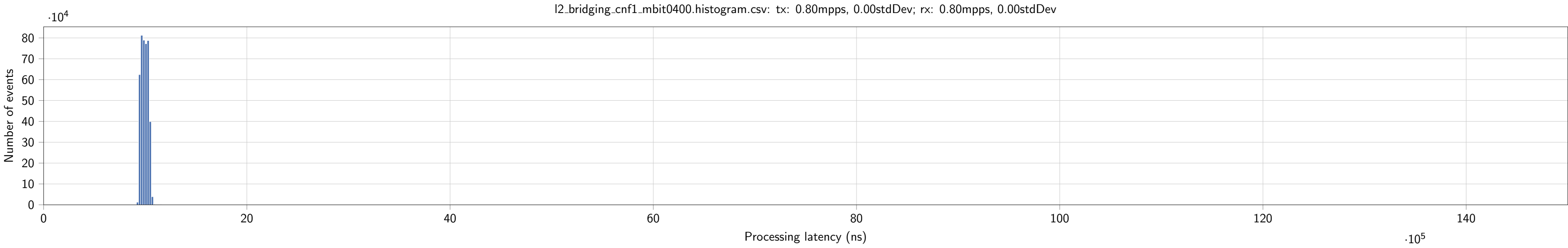


l2_bridging_cnf0_mbit6000.histogram.csv: tx: 11.78mpps, 0.06stdDev; rx: 9.35mpps, 0.00stdDev



l2_bridging_cnf0_mbit9000.histogram.csv: tx: 14.86mpps, 0.07stdDev; rx: 9.35mpps, 0.00stdDev





l2_bridging_cnf1_mbit0800.histogram.csv: tx: 1.58mpps, 0.01stdDev; rx: 1.58mpps, 0.00stdDev

Number of events

80
70
60
50
40
30
20
10
0

$\cdot 10^4$

0

20

40

60

80

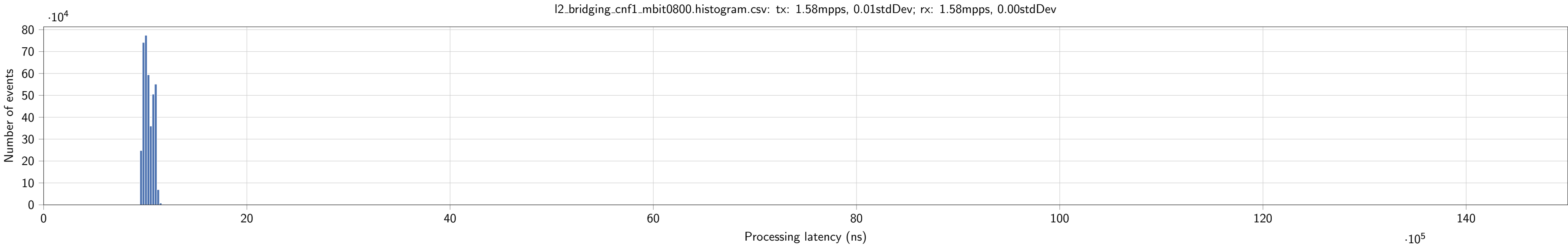
100

120

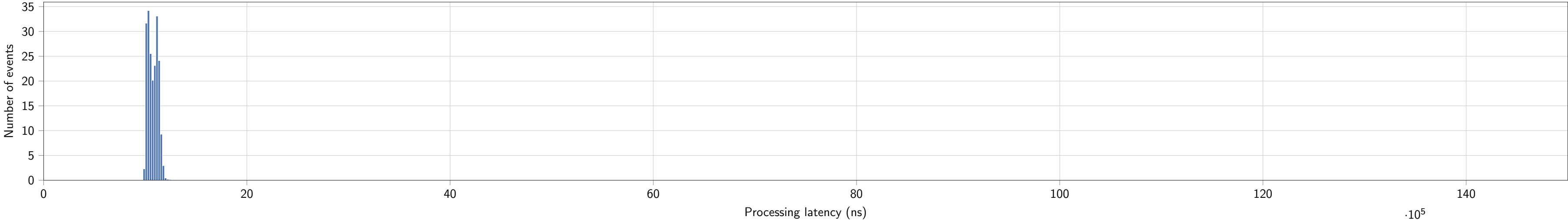
140

Processing latency (ns)

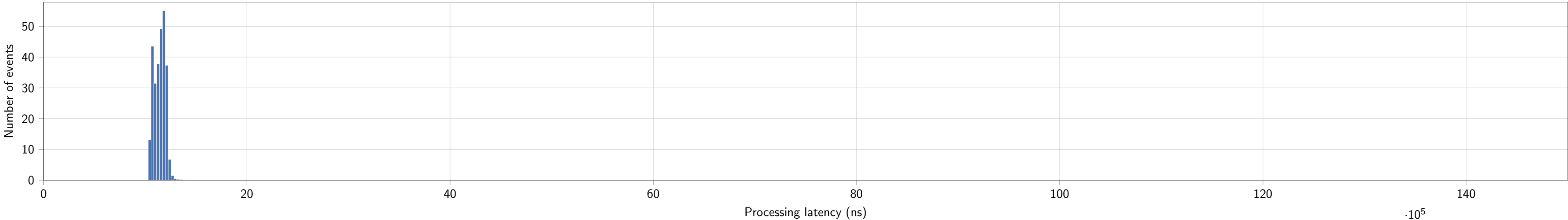
$\cdot 10^5$

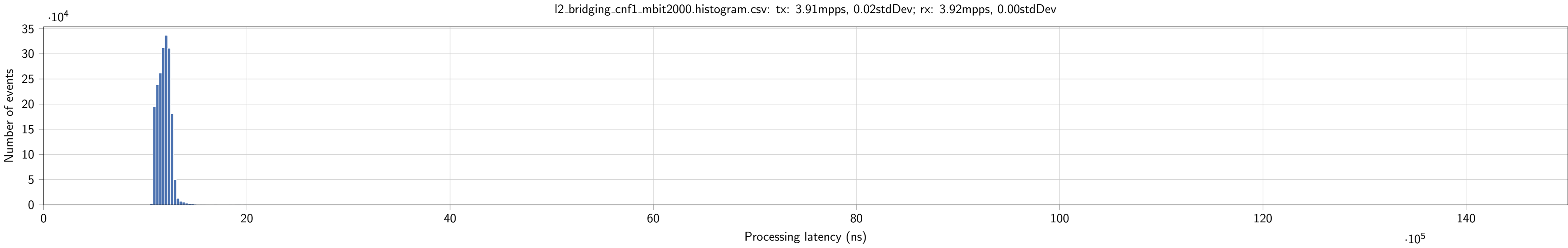


l2_bridging_cnf1_mbit1200.histogram.csv: tx: 2.35mpps, 0.01stdDev; rx: 2.36mpps, 0.00stdDev

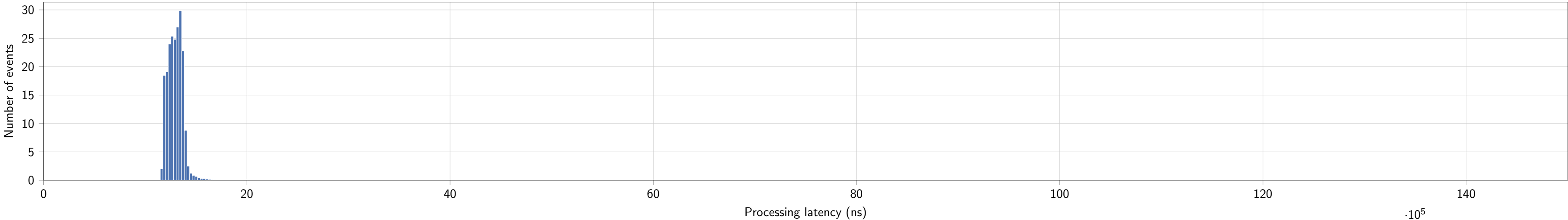


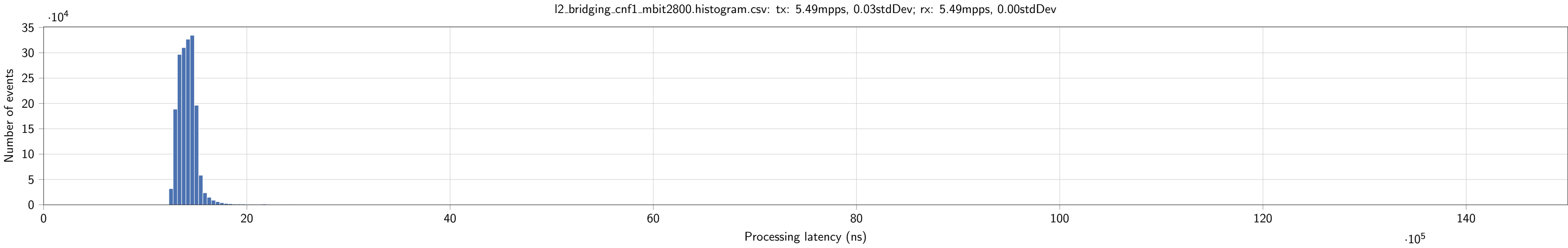
l2_bridging_cnf1_mbit1600.histogram.csv: tx: 3.14mpps, 0.01stdDev; rx: 3.14mpps, 0.00stdDev



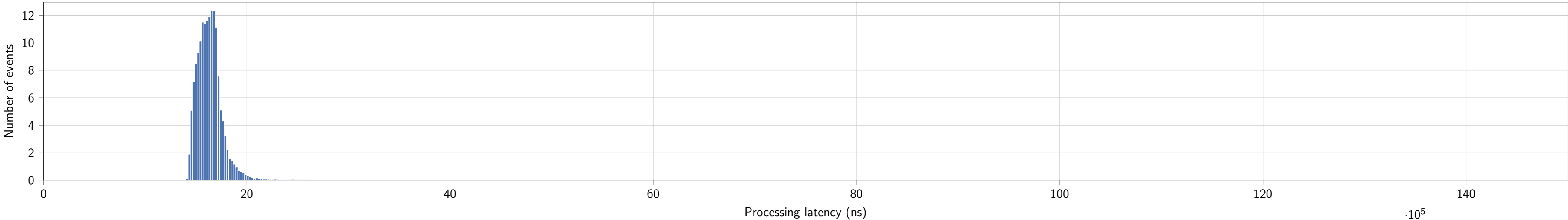


l2_bridging_cnf1_mbit2400.histogram.csv: tx: 4.70mpps, 0.02stdDev; rx: 4.71mpps, 0.00stdDev

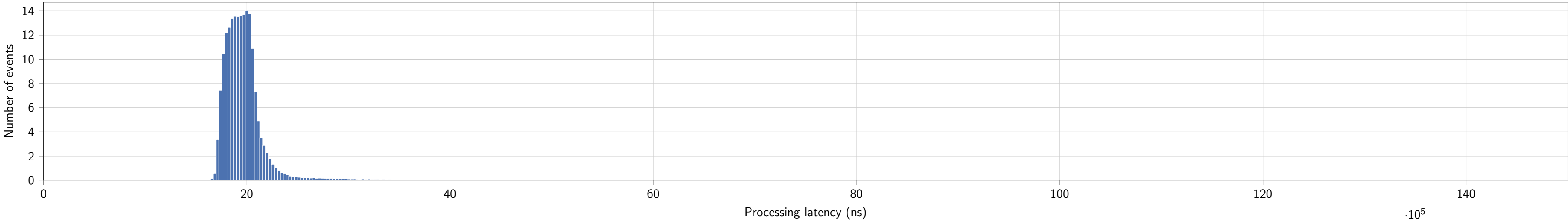


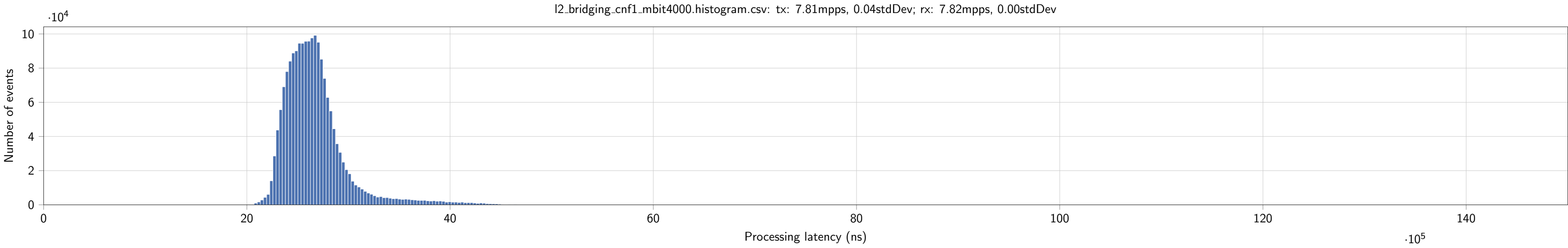


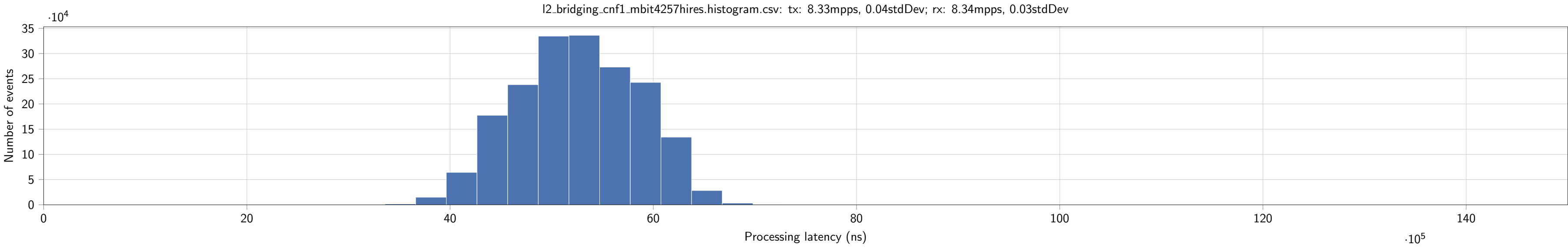
l2_bridging_cnf1_mbit3200.histogram.csv: tx: 6.25mpps, 0.03stdDev; rx: 6.26mpps, 0.00stdDev



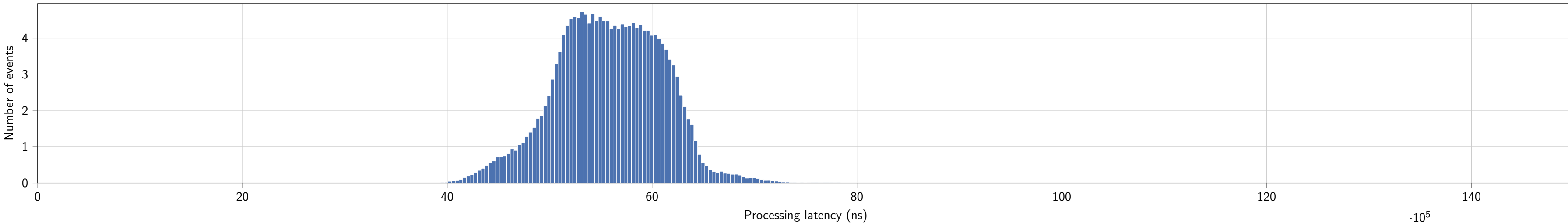
l2_bridging_cnf1_mbit3600.histogram.csv: tx: 7.06mpps, 0.03stdDev; rx: 7.07mpps, 0.00stdDev



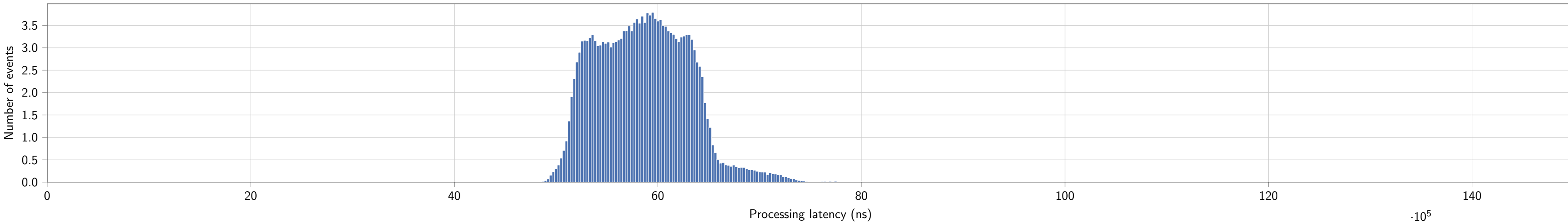


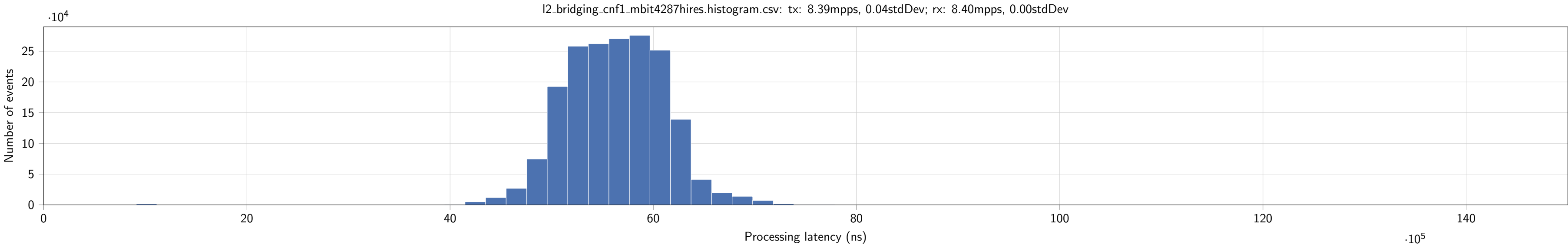


l2_bridging_cnf1_mbit4267hires.histogram.csv: tx: 8.39mpps, 0.04stdDev; rx: 8.40mpps, 0.00stdDev

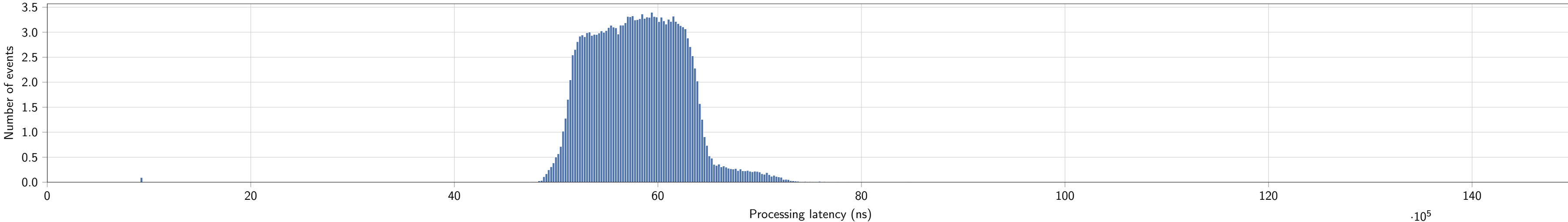


l2_bridging_cnf1_mbit4277hires.histogram.csv: tx: 8.39mpps, 0.04stdDev; rx: 8.40mpps, 0.00stdDev

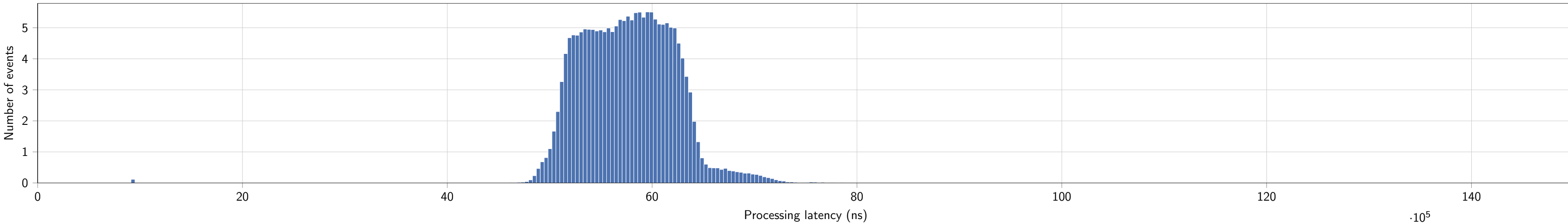




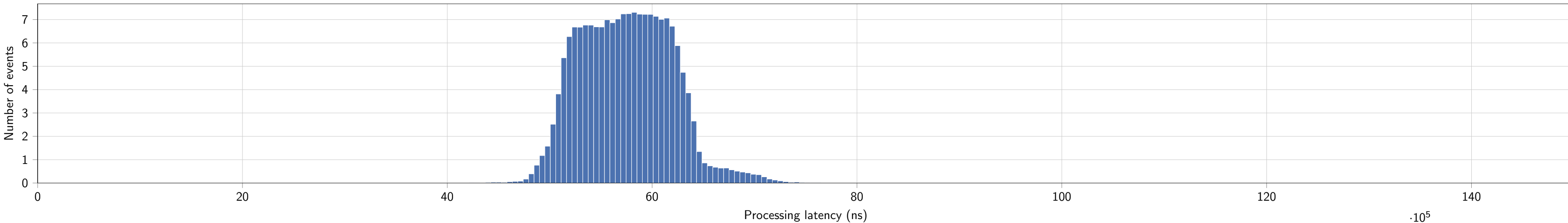
l2_bridging_cnf1_mbit4297hires.histogram.csv: tx: 8.45mpps, 0.04stdDev; rx: 8.46mpps, 0.00stdDev



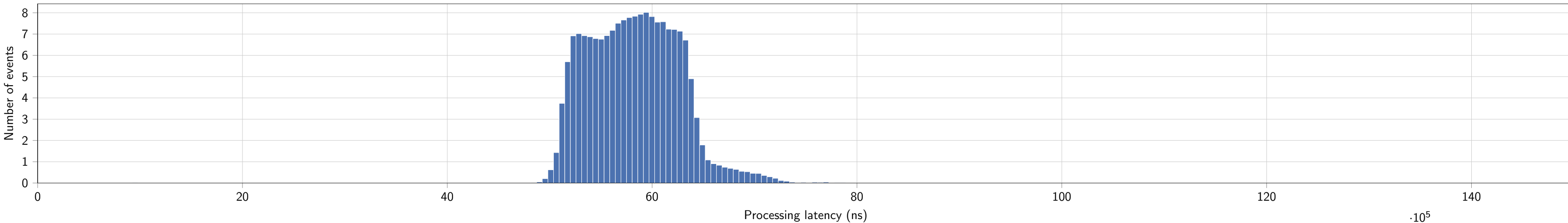
l2_bridging_cnf1_mbit4307hires.histogram.csv: tx: 8.45mpps, 0.04stdDev; rx: 8.46mpps, 0.00stdDev



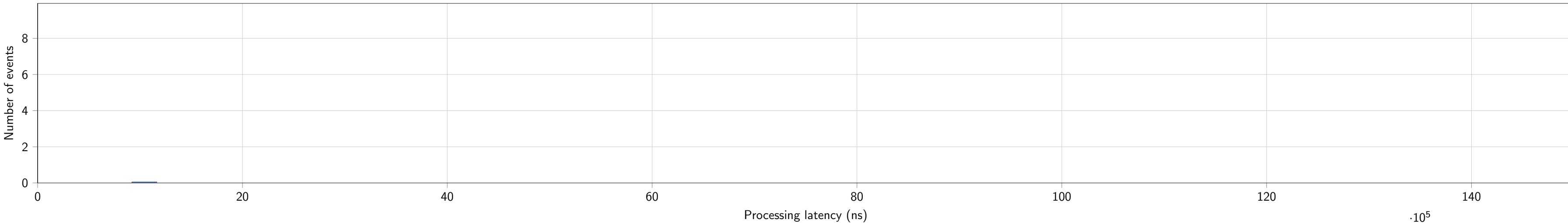
l2_bridging_cnf1_mbit4317hires.histogram.csv: tx: 8.45mpps, 0.04stdDev; rx: 8.45mpps, 0.00stdDev



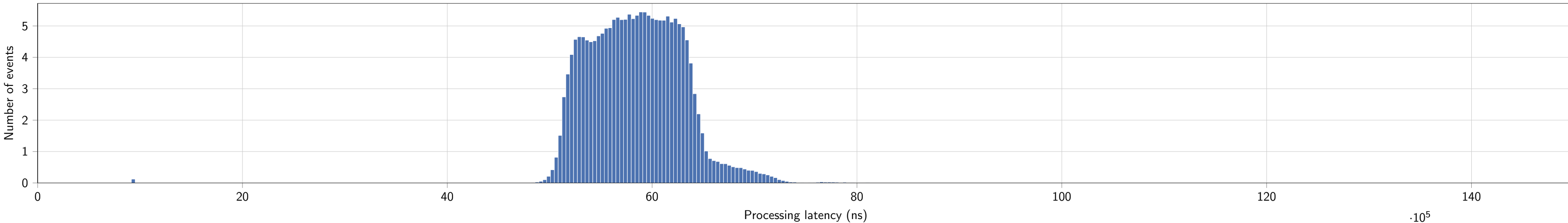
l2_bridging_cnf1_mbit4327hires.histogram.csv: tx: 8.50mpps, 0.04stdDev; rx: 8.51mpps, 0.00stdDev



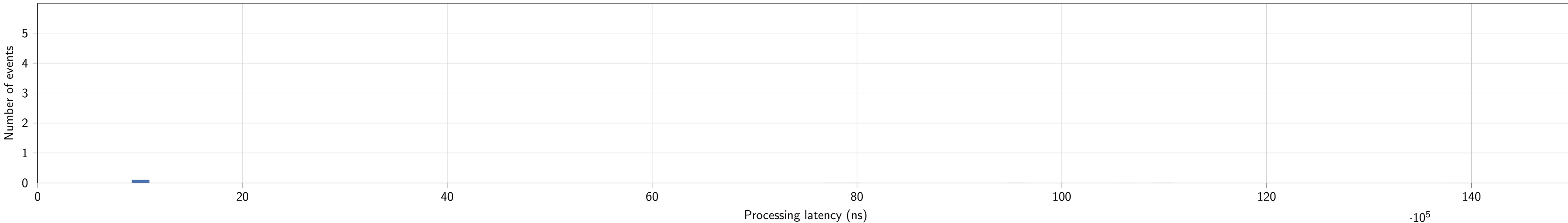
l2_bridging_cnf1_mbit4337_final.histogram.csv: tx: 8.50mpps, 0.04stdDev; rx: 8.45mpps, 0.00stdDev



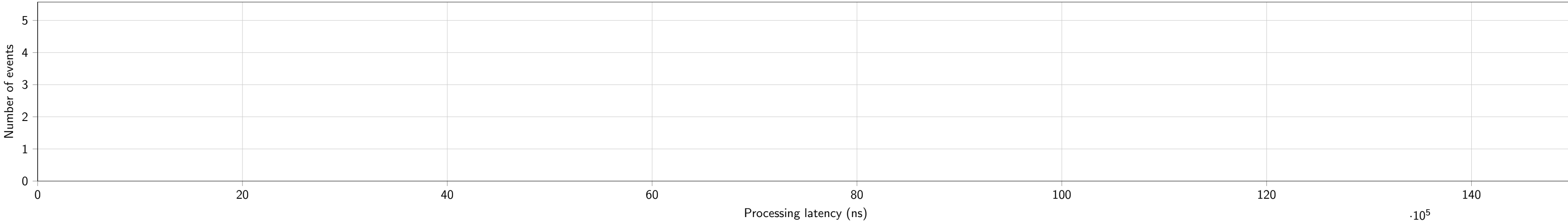
l2_bridging_cnf1_mbit4337hires.histogram.csv: tx: 8.50mpps, 0.04stdDev; rx: 8.51mpps, 0.00stdDev



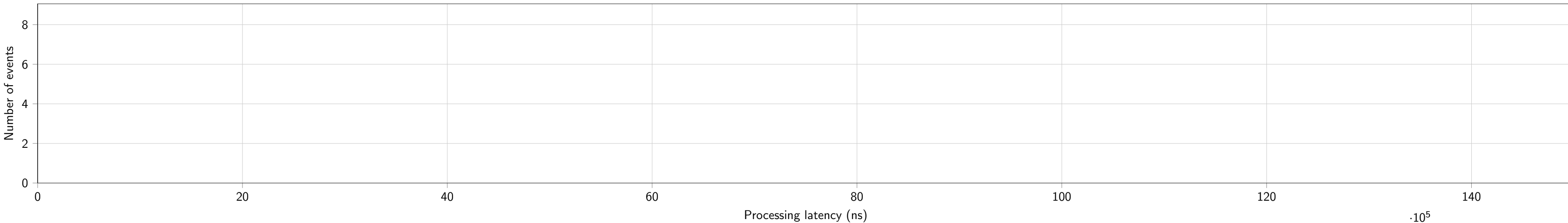
l2_bridging_cnf1_mbit4347hires.histogram.csv: tx: 8.50mpps, 0.04stdDev; rx: 8.49mpps, 0.00stdDev



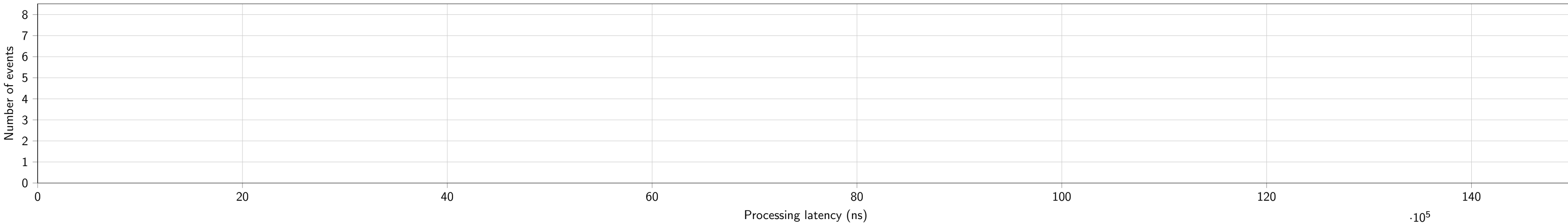
l2_bridging_cnf1_mbit4357hires.histogram.csv: tx: 8.55mpps, 0.04stdDev; rx: 8.46mpps, 0.00stdDev



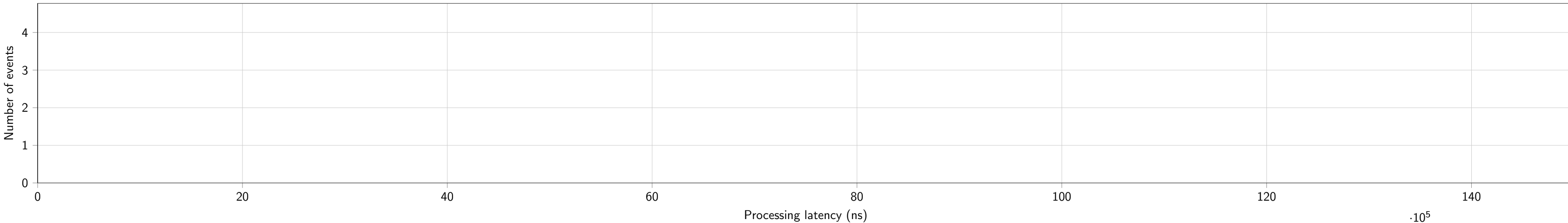
l2_bridging_cnf1_mbit4367hires.histogram.csv: tx: 8.55mpps, 0.04stdDev; rx: 8.54mpps, 0.00stdDev



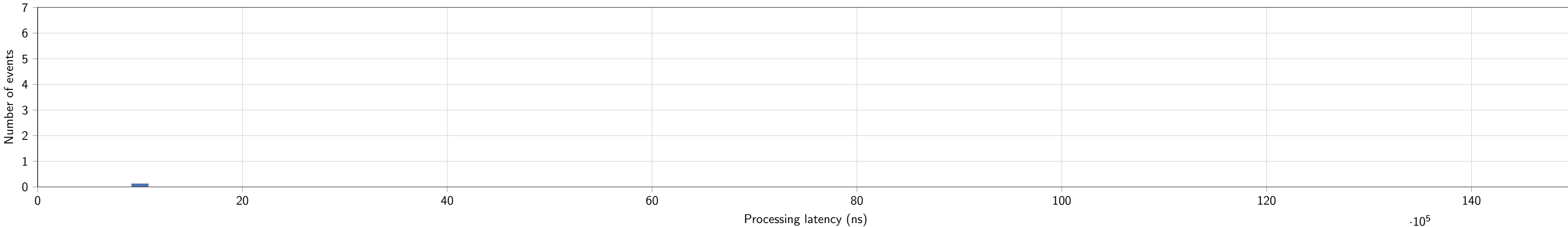
l2_bridging_cnf1_mbit4377hires.histogram.csv: tx: 8.55mpps, 0.04stdDev; rx: 8.52mpps, 0.00stdDev



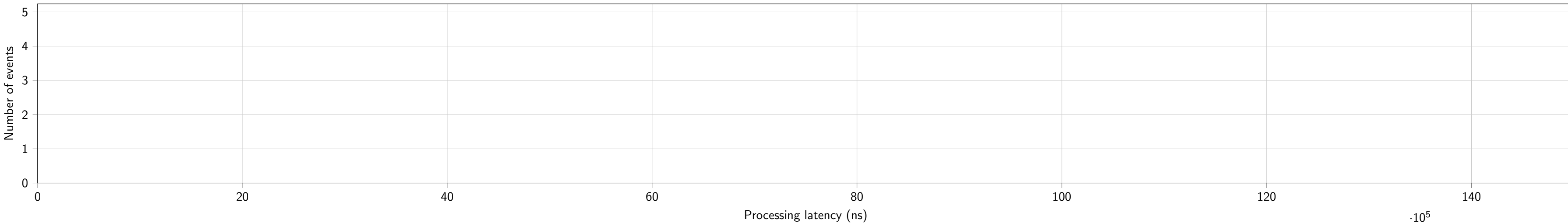
l2_bridging_cnf1_mbit4387hires.histogram.csv: tx: 8.61mpps, 0.04stdDev; rx: 8.50mpps, 0.00stdDev



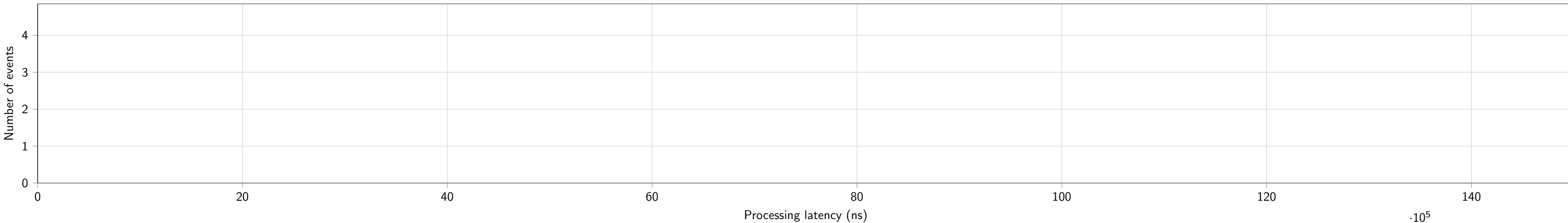
l2_bridging_cnf1_mbit4397hires.histogram.csv: tx: 8.61mpps, 0.04stdDev; rx: 8.53mpps, 0.00stdDev



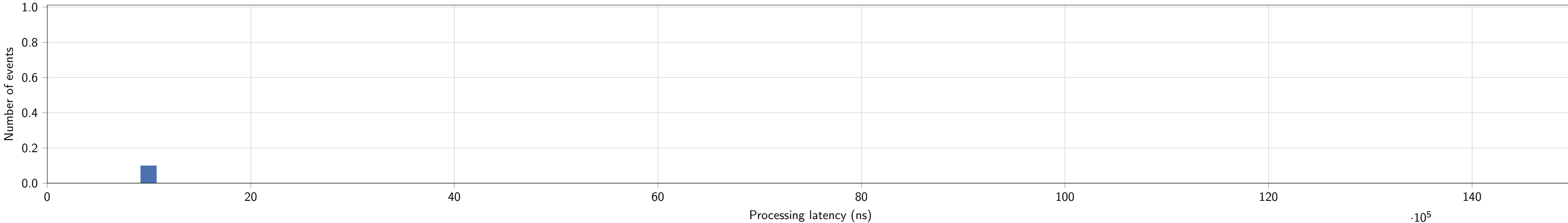
l2_bridging_cnf1_mbit4400.histogram.csv: tx: 8.61mpps, 0.04stdDev; rx: 8.49mpps, 0.00stdDev



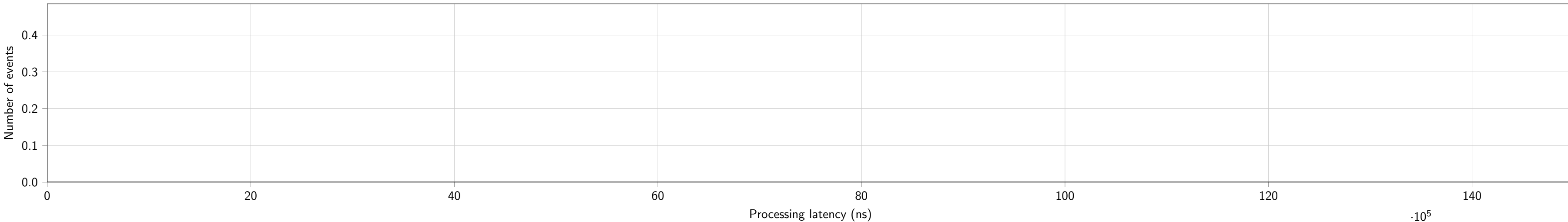
l2_bridging_cnf1_mbit4407hires.histogram.csv: tx: 8.61mpps, 0.04stdDev; rx: 8.50mpps, 0.00stdDev



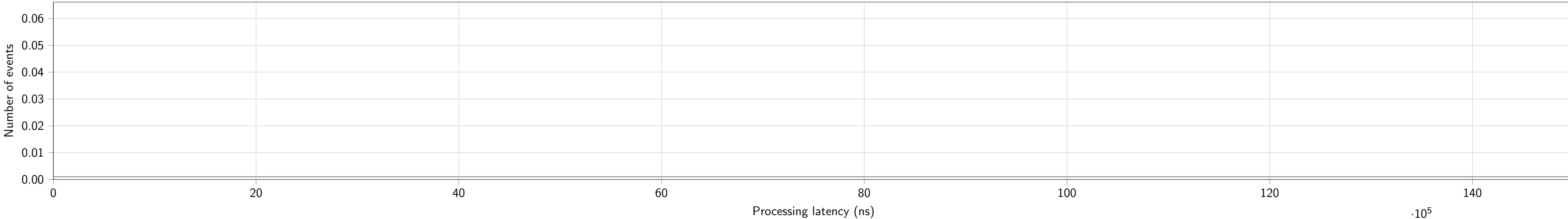
l2_bridging_cnf1_mbit4800.histogram.csv: tx: 9.39mpps, 0.05stdDev; rx: 8.52mpps, 0.00stdDev



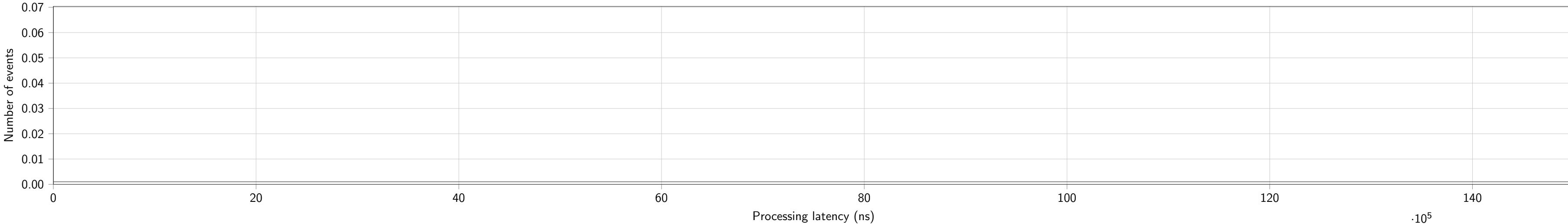
l2_bridging_cnf1_mbit5200.histogram.csv: tx: 10.15mpps, 0.05stdDev; rx: 8.50mpps, 0.04stdDev



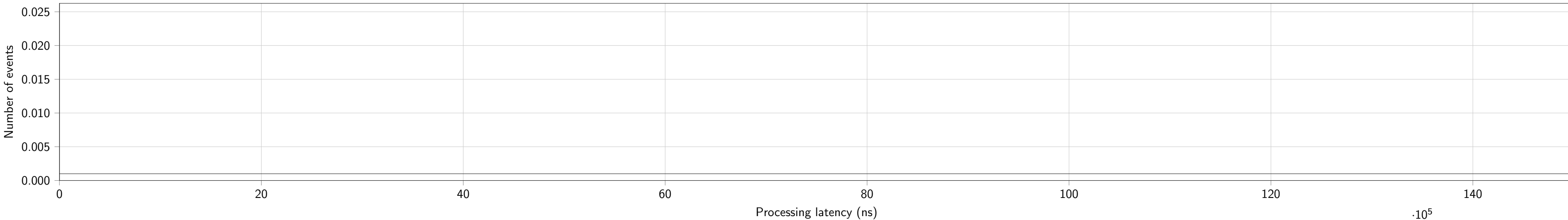
l2_bridging_cnf1_mbit5600.histogram.csv: tx: 10.95mpps, 0.05stdDev; rx: 8.51mpps, 0.00stdDev



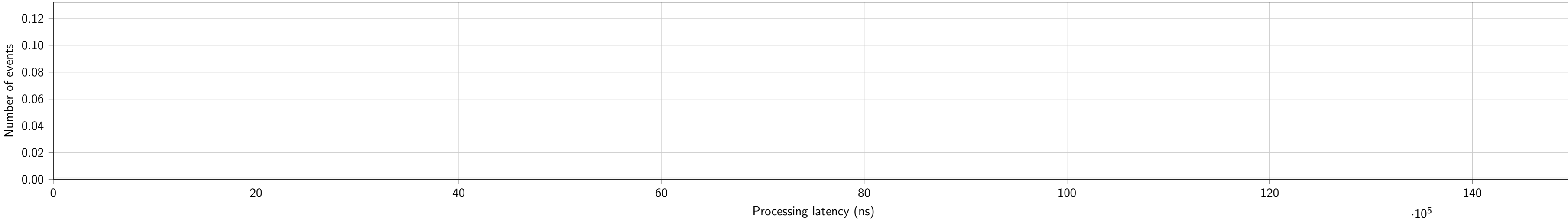
l2_bridging_cnf1_mbit6000.histogram.csv: tx: 11.78mpps, 0.06stdDev; rx: 8.44mpps, 0.00stdDev

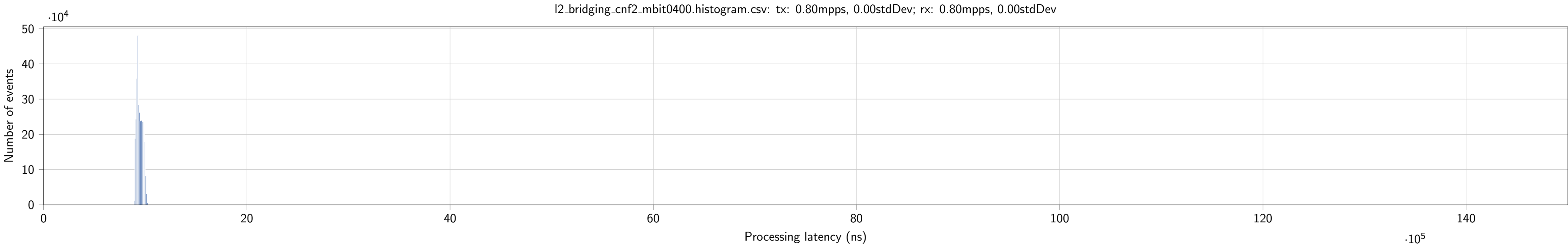


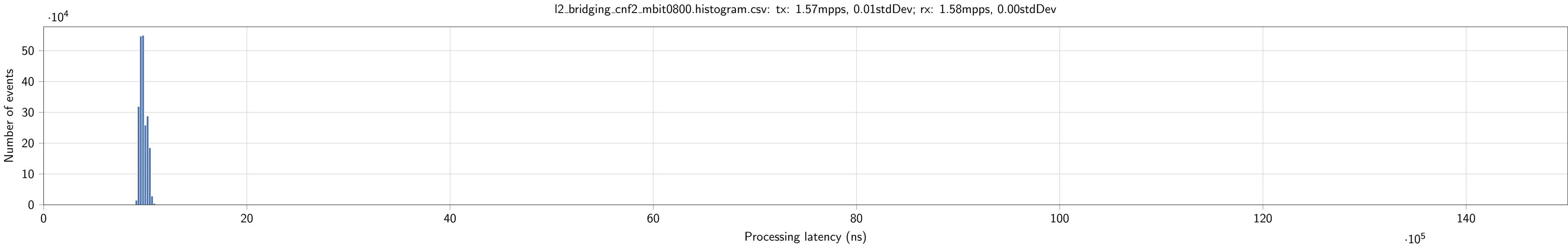
l2_bridging_cnf1_mbit9000.histogram.csv: tx: 14.86mpps, 0.07stdDev; rx: 8.51mpps, 0.00stdDev

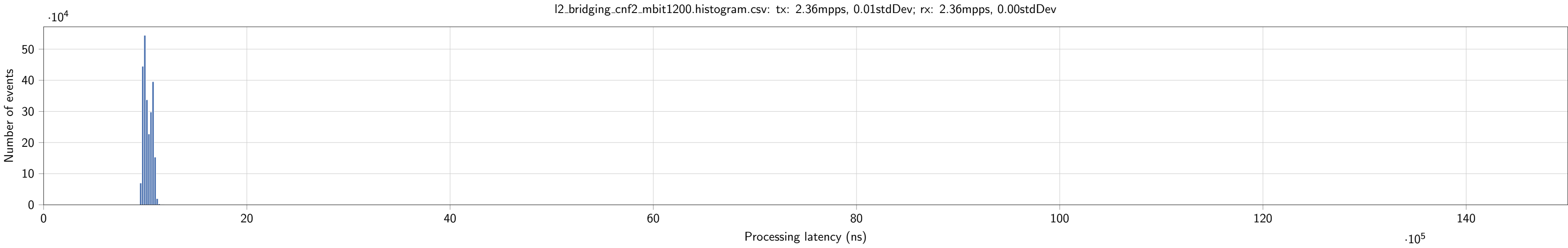


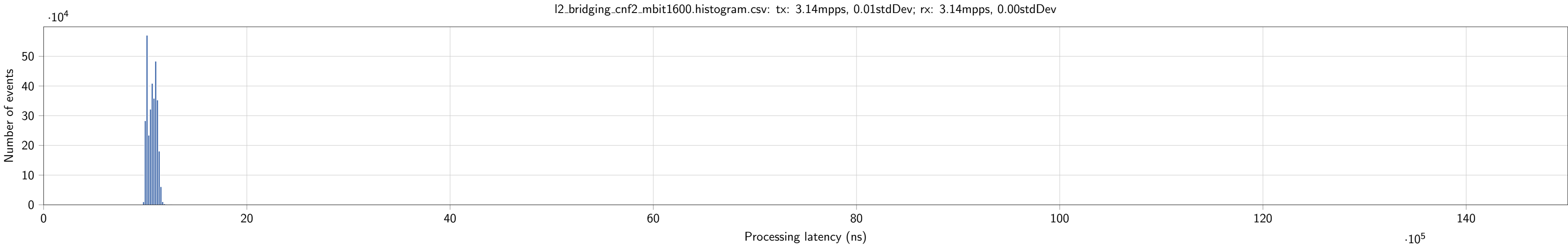
l2_bridging_cnf2_mbit0000_final.histogram.csv: tx: 14.86mpps, 0.08stdDev; rx: 9.34mpps, 0.00stdDev

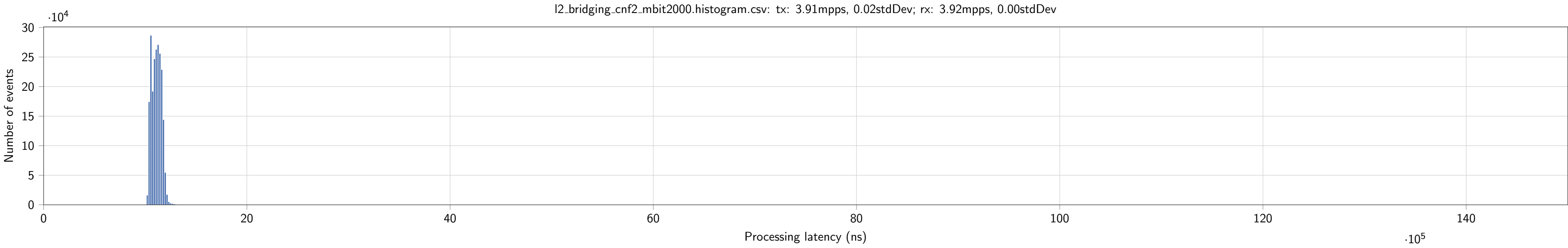


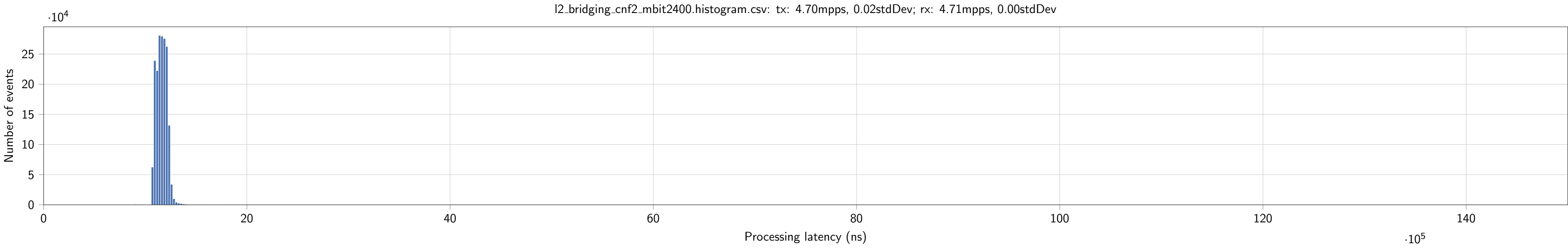


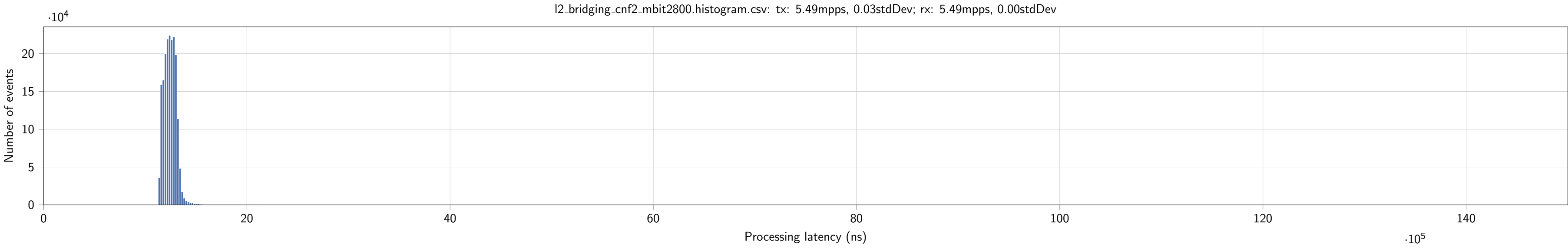


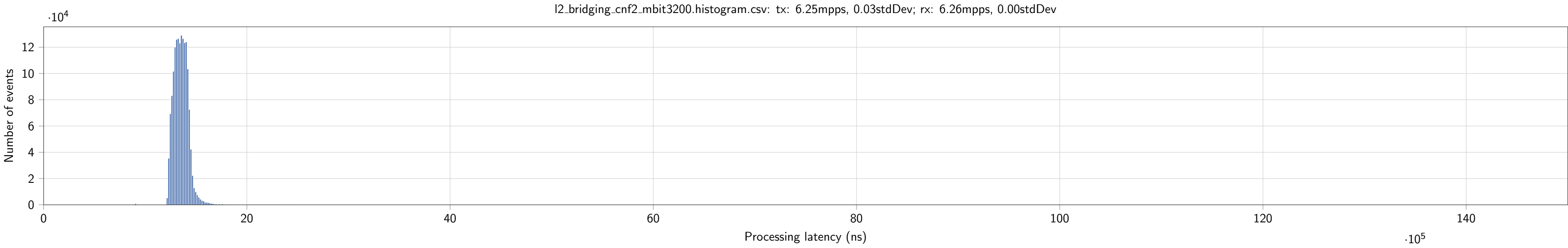












l2_bridging_cnf2_mbit3600.histogram.csv: tx: 7.06mpps, 0.03stdDev; rx: 7.07mpps, 0.00stdDev

Number of events

20.0
17.5
15.0
12.5
10.0
7.5
5.0
2.5
0.0

$\cdot 10^4$

20

40

60

80

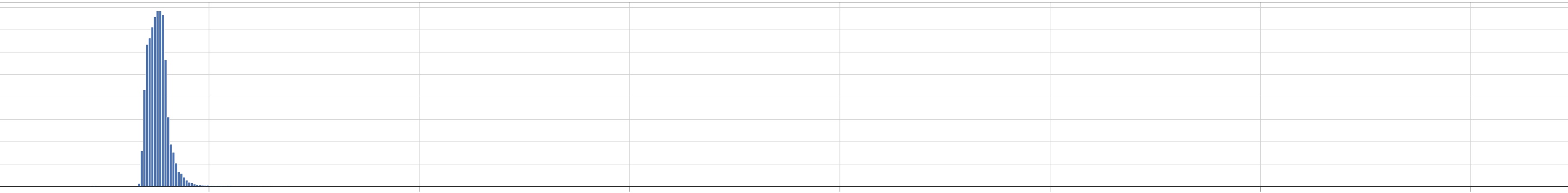
100

120

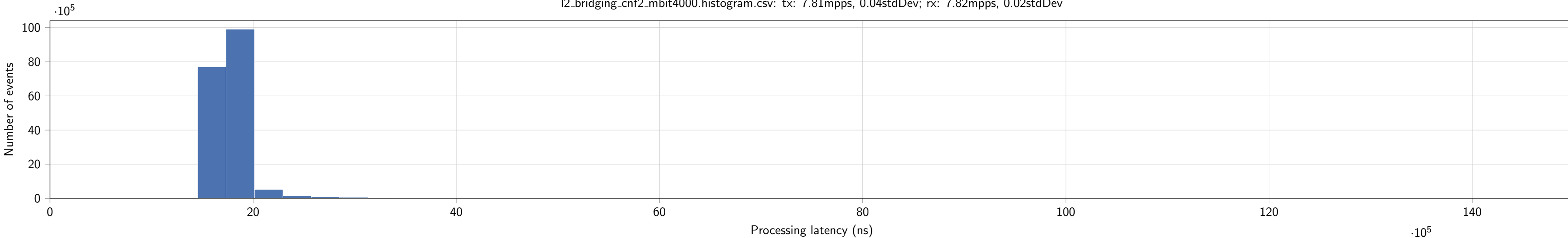
140

Processing latency (ns)

$\cdot 10^5$



l2_bridging_cnf2_mbit4000.histogram.csv: tx: 7.81mpps, 0.04stdDev; rx: 7.82mpps, 0.02stdDev



l2_bridging_cnf2_mbit4314hires.histogram.csv: tx: 8.44mpps, 0.04stdDev; rx: 8.46mpps, 0.00stdDev

Number of events

10
8
6
4
2
0

$\cdot 10^4$

20

40

60

80

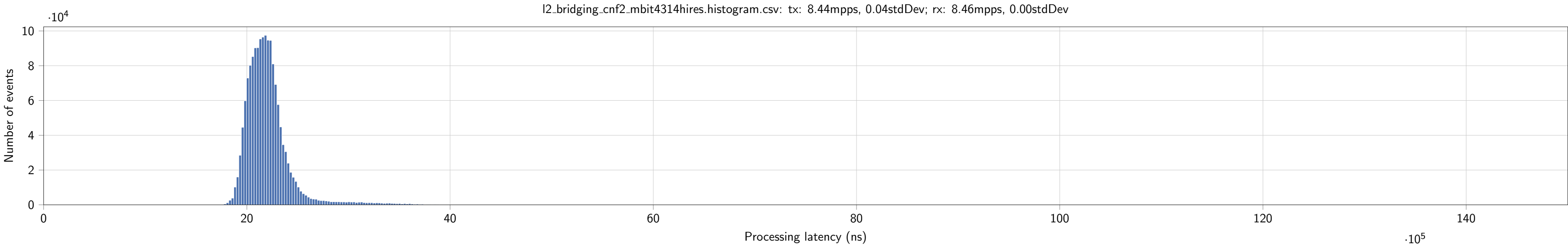
100

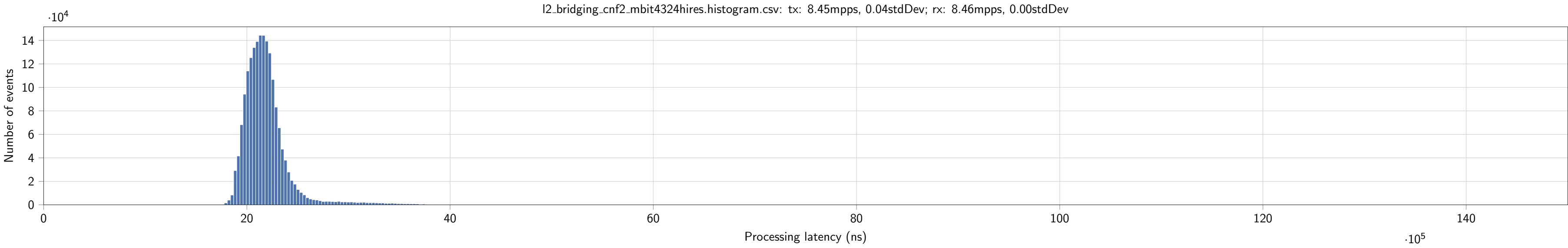
120

140

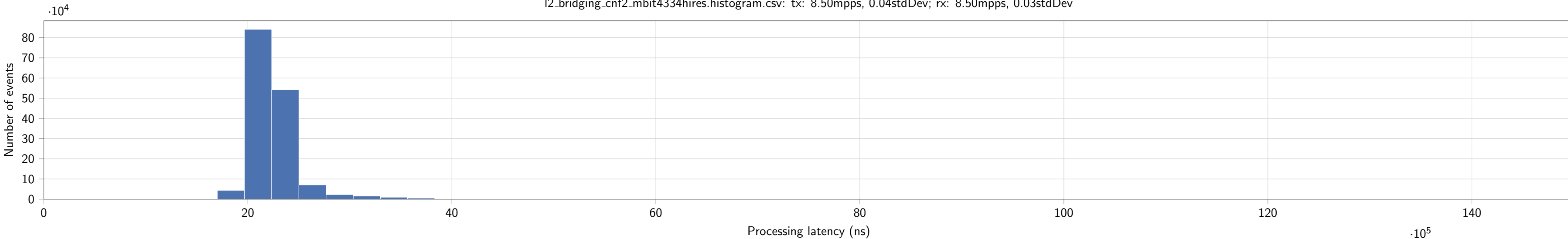
Processing latency (ns)

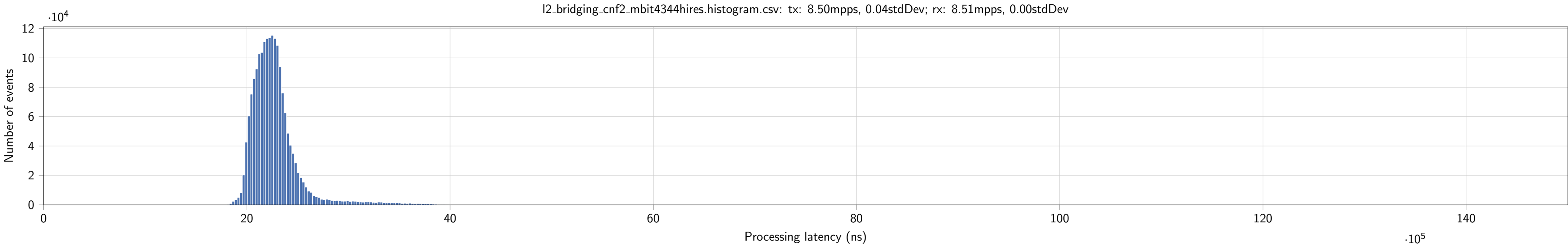
$\cdot 10^5$

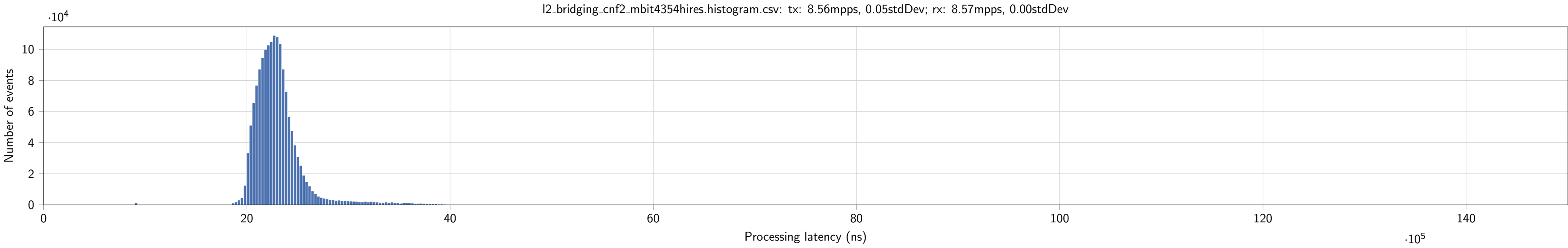




l2_bridging_cnf2_mbit4334hires.histogram.csv: tx: 8.50mpps, 0.04stdDev; rx: 8.50mpps, 0.03stdDev

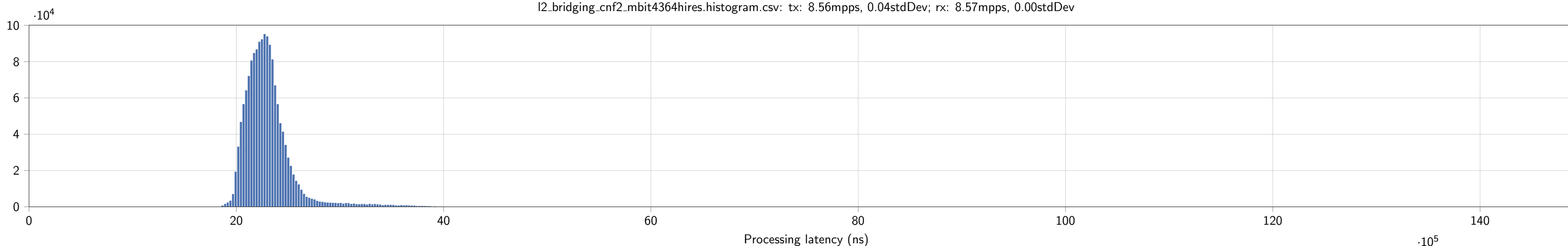




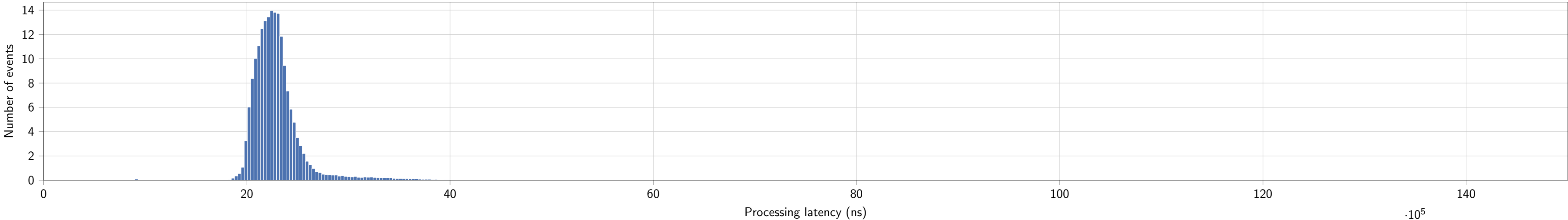


l2_bridging_cnf2_mbit4364hires.histogram.csv: tx: 8.56mpps, 0.04stdDev; rx: 8.57mpps, 0.00stdDev

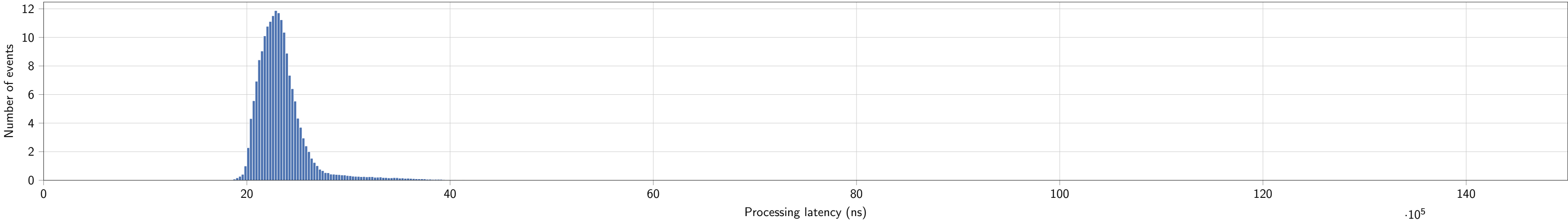
Number of events



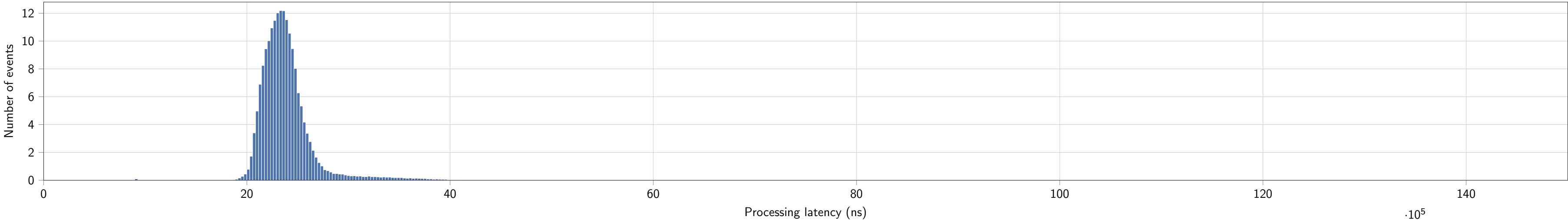
l2_bridging_cnf2_mbit4374hires.histogram.csv: tx: 8.56mpps, 0.04stdDev; rx: 8.57mpps, 0.00stdDev



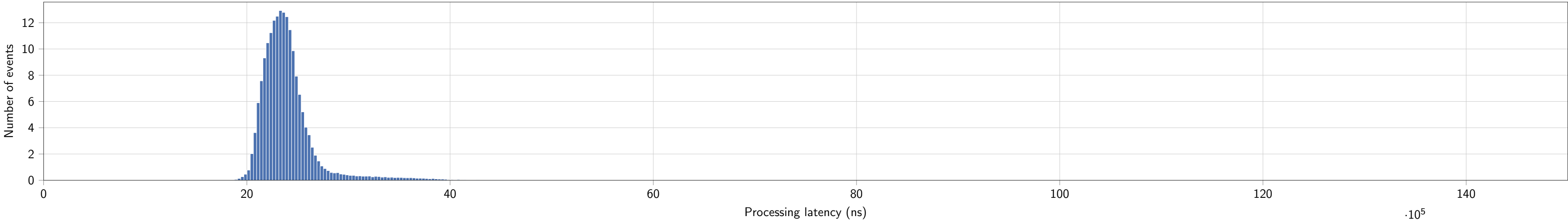
l2_bridging_cnf2_mbit4384hires.histogram.csv: tx: 8.62mpps, 0.04stdDev; rx: 8.63mpps, 0.00stdDev

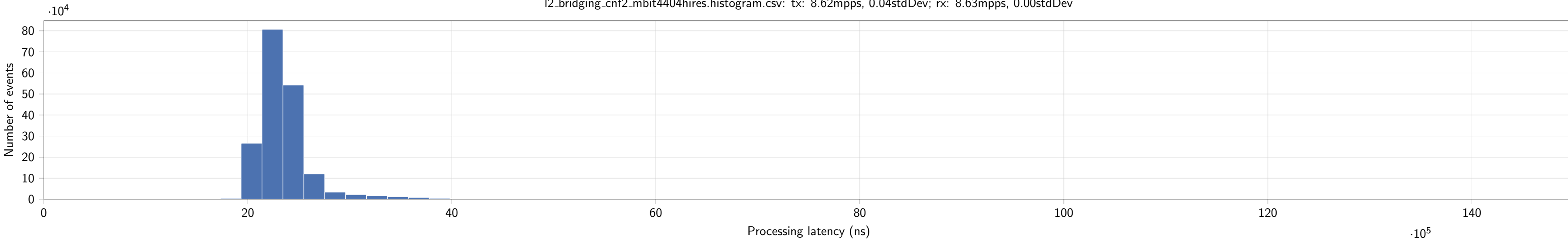


l2_bridging_cnf2_mbit4394hires.histogram.csv: tx: 8.62mpps, 0.04stdDev; rx: 8.63mpps, 0.00stdDev

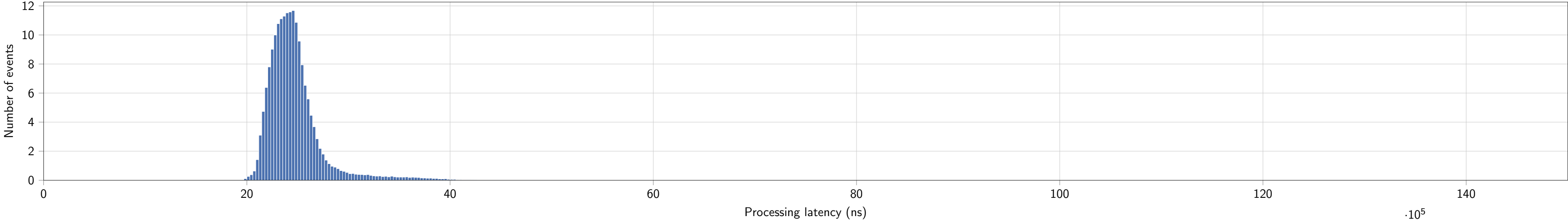


l2_bridging_cnf2_mbit4400.histogram.csv: tx: 8.62mpps, 0.04stdDev; rx: 8.63mpps, 0.00stdDev

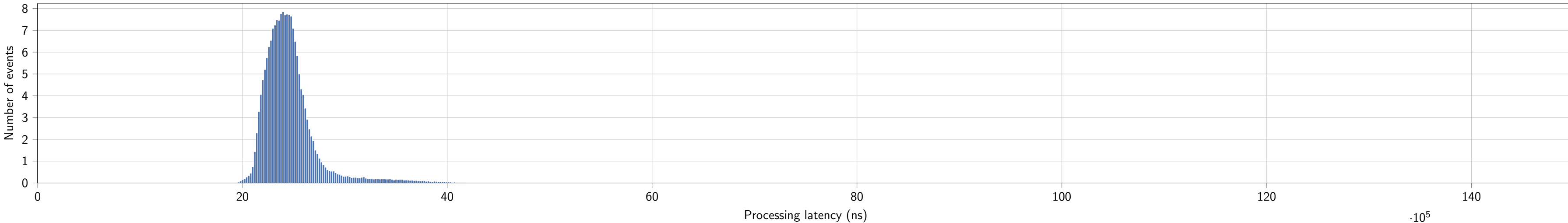




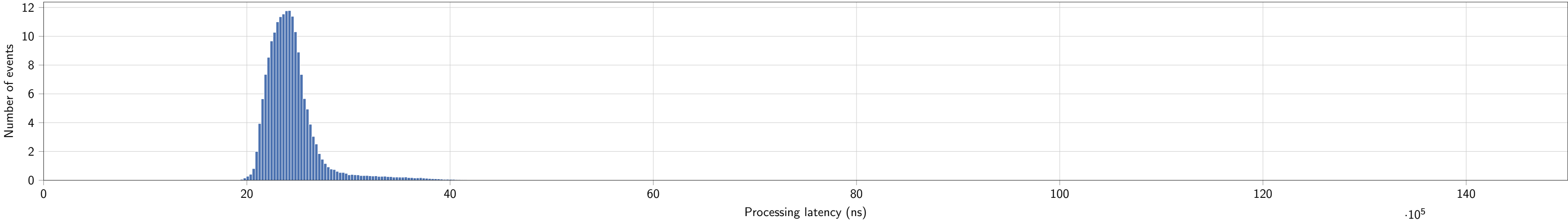
l2_bridging_cnf2_mbit4414hires.histogram.csv: tx: 8.68mpps, 0.04stdDev; rx: 8.69mpps, 0.00stdDev

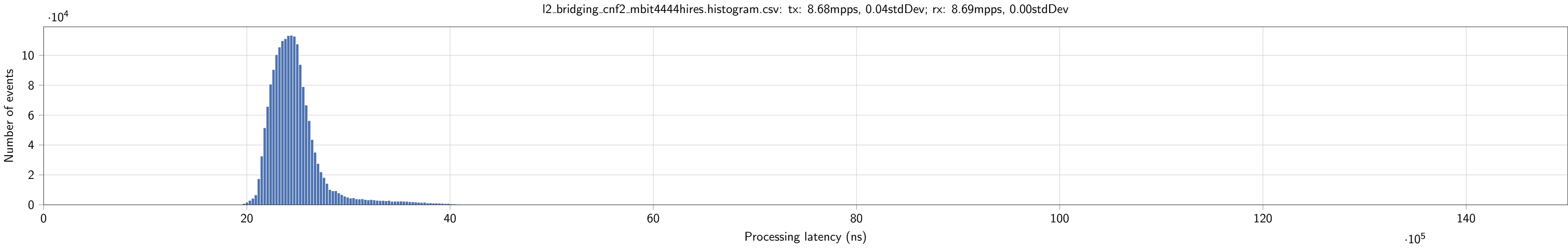


l2_bridging_cnf2_mbit4424hires.histogram.csv: tx: 8.68mpps, 0.04stdDev; rx: 8.69mpps, 0.00stdDev

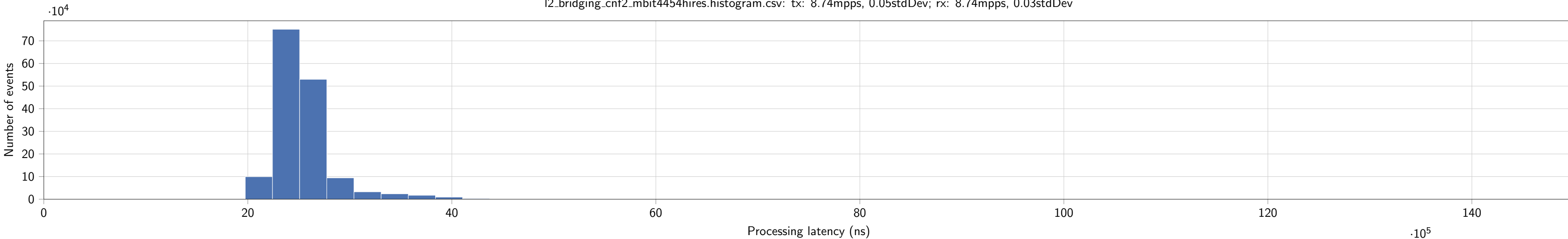


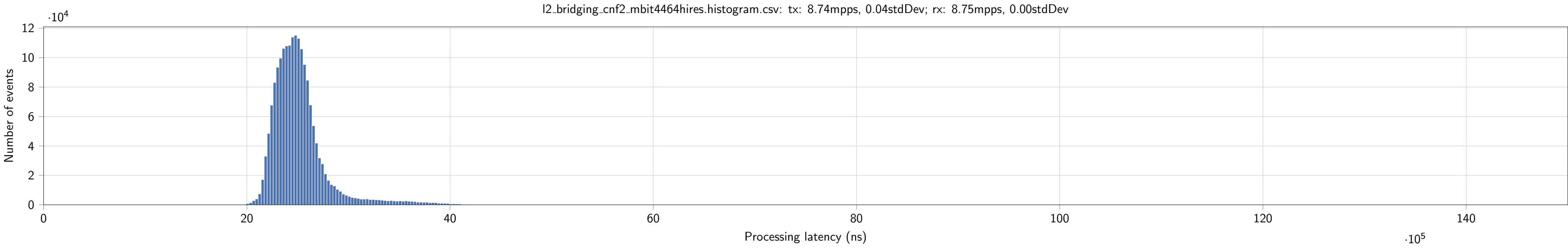
l2_bridging_cnf2_mbit4434hires.histogram.csv: tx: 8.68mpps, 0.04stdDev; rx: 8.69mpps, 0.00stdDev



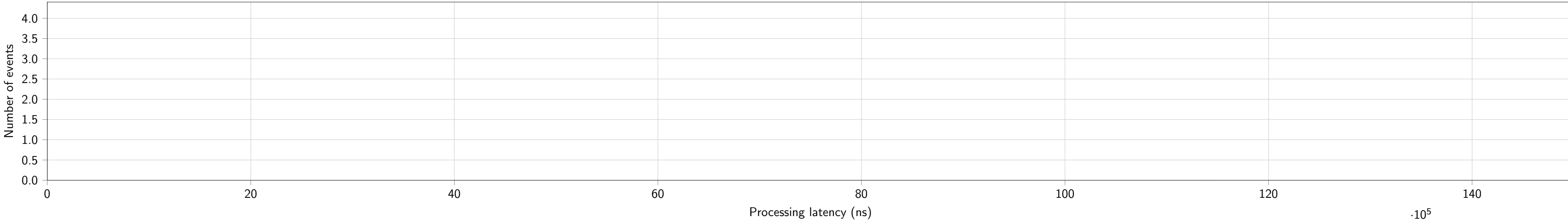


l2_bridging_cnf2_mbit4454hires.histogram.csv: tx: 8.74mpps, 0.05stdDev; rx: 8.74mpps, 0.03stdDev

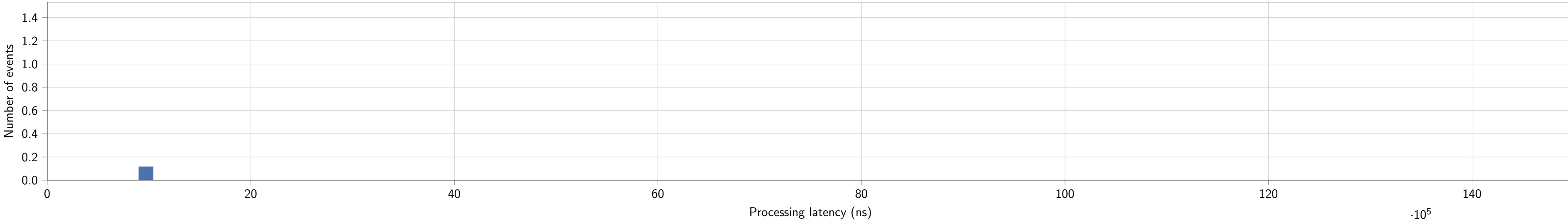




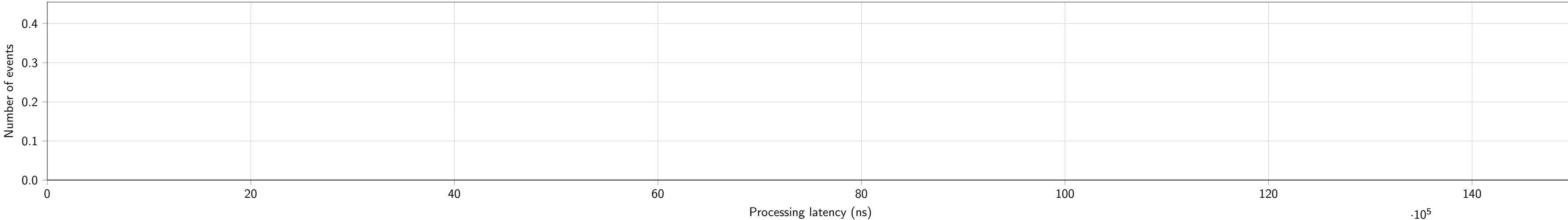
l2_bridging_cnf2_mbit4800.histogram.csv: tx: 9.39mpps, 0.05stdDev; rx: 9.37mpps, 0.00stdDev



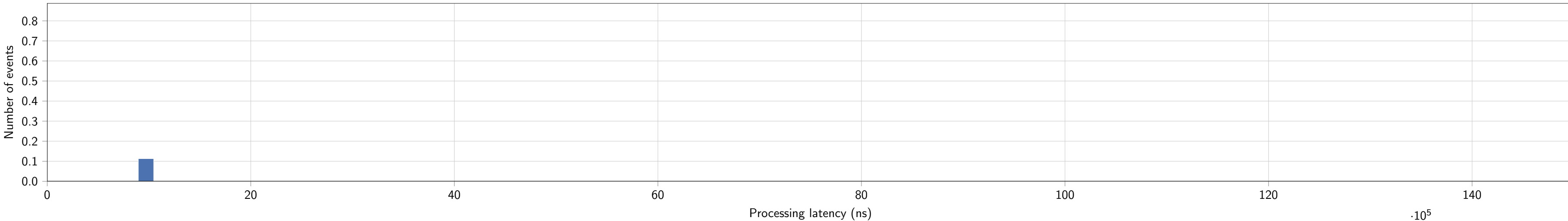
l2_bridging_cnf2_mbit5200.histogram.csv: tx: 10.15mpps, 0.05stdDev; rx: 9.35mpps, 0.00stdDev



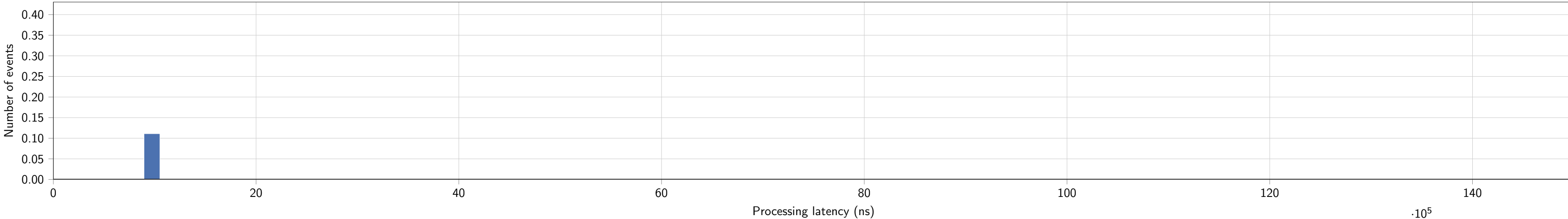
l2_bridging_cnf2_mbit5600.histogram.csv: tx: 10.95mpps, 0.05stdDev; rx: 9.37mpps, 0.00stdDev

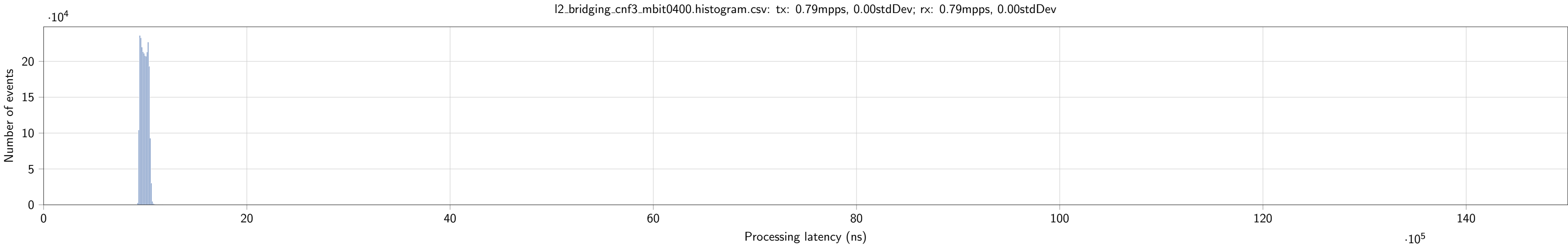


l2_bridging_cnf2_mbit6000.histogram.csv: tx: 11.78mpps, 0.06stdDev; rx: 9.31mpps, 0.00stdDev

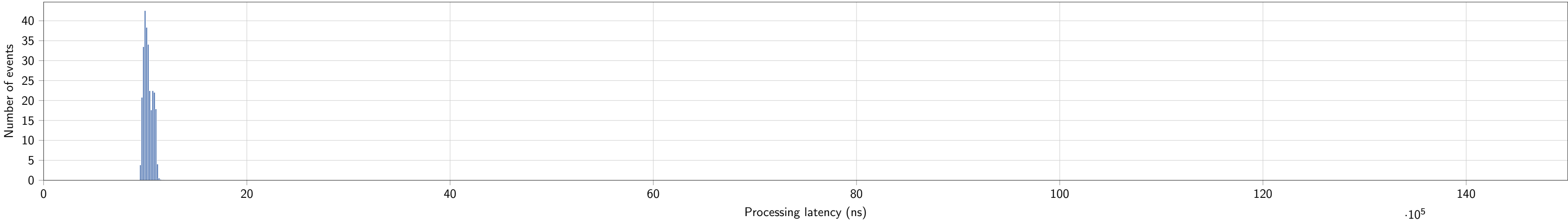


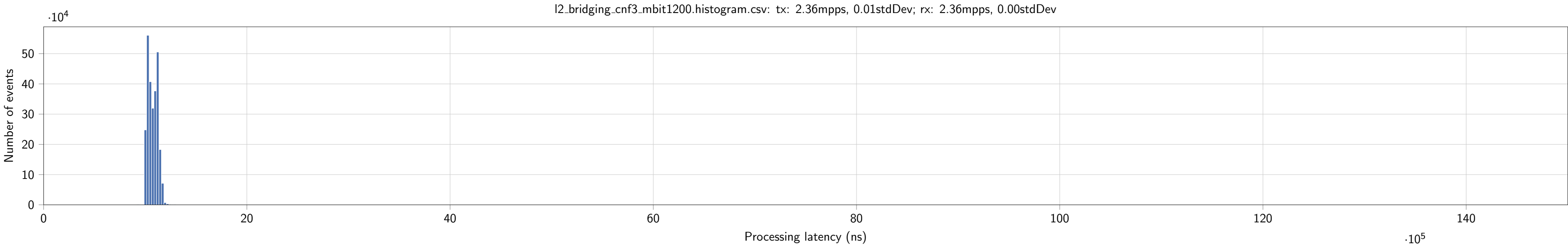
l2_bridging_cnf2_mbit9000.histogram.csv: tx: 14.86mpps, 0.07stdDev; rx: 8.62mpps, 0.00stdDev

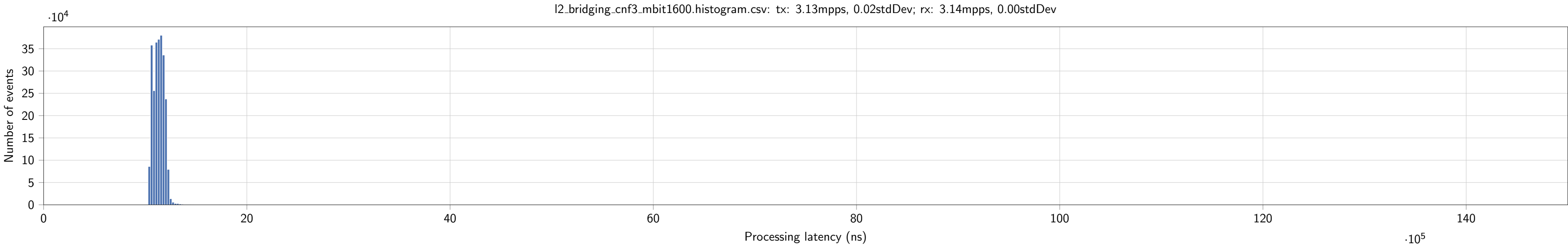




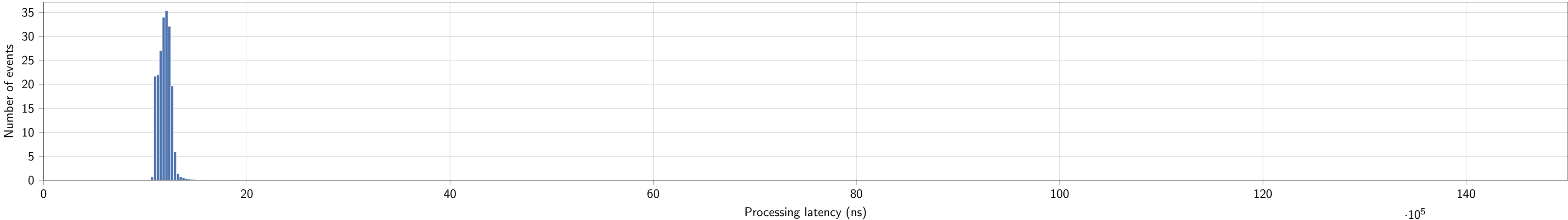
l2_bridging_cnf3_mbit0800.histogram.csv: tx: 1.58mpps, 0.01stdDev; rx: 1.58mpps, 0.00stdDev

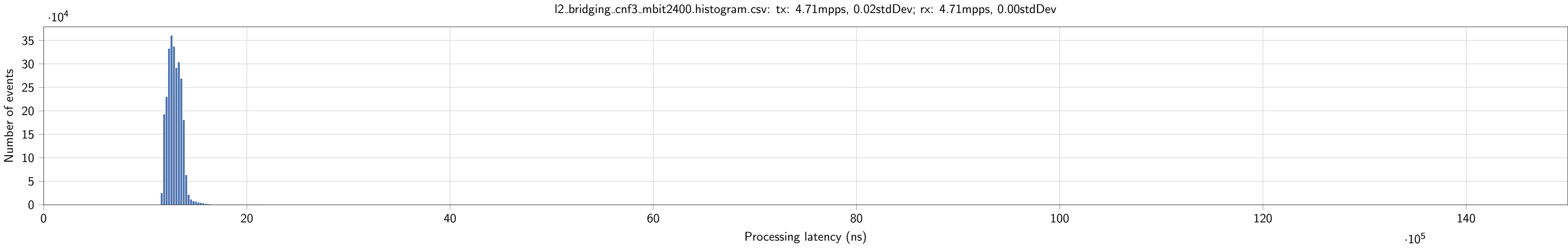


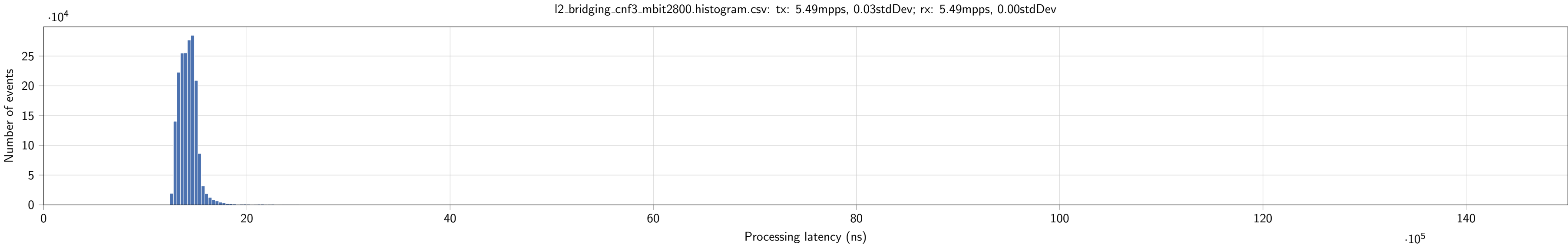




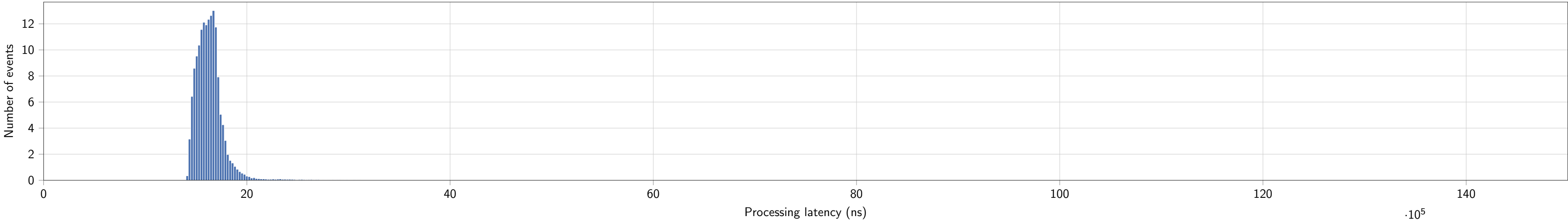
l2_bridging_cnf3_mbit2000.histogram.csv: tx: 3.91mpps, 0.02stdDev; rx: 3.92mpps, 0.00stdDev



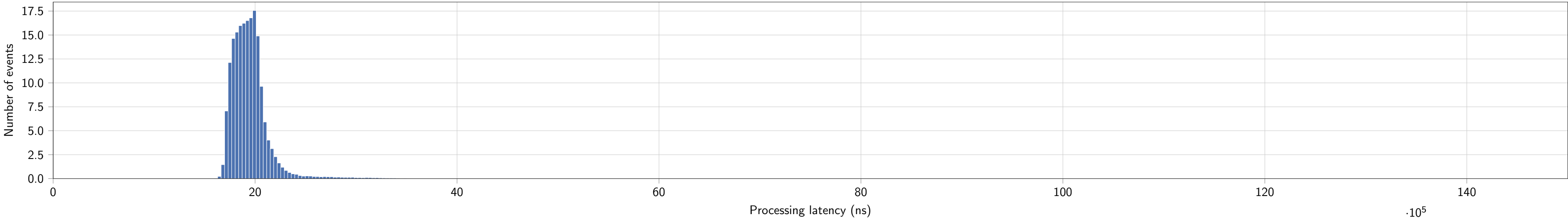




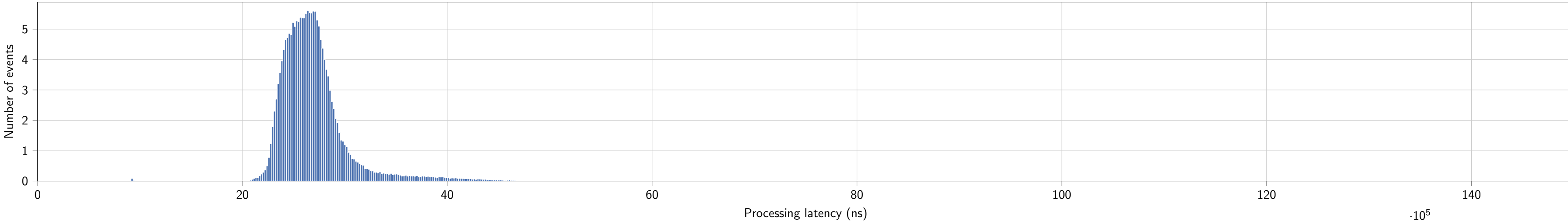
l2_bridging_cnf3_mbit3200.histogram.csv: tx: 6.25mpps, 0.03stdDev; rx: 6.26mpps, 0.00stdDev



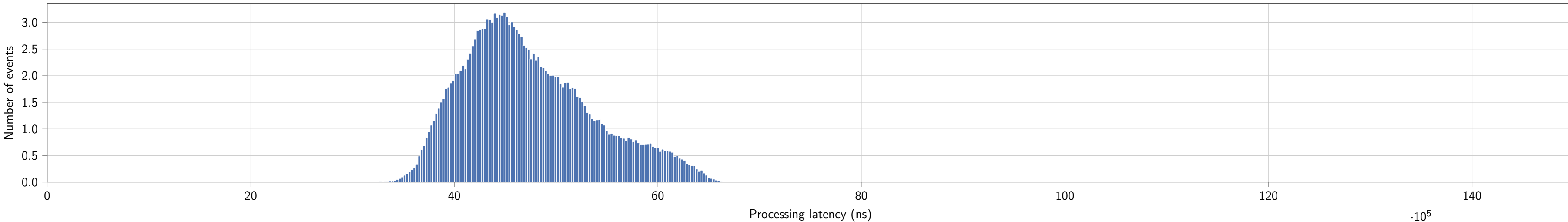
l2_bridging_cnf3_mbit3600.histogram.csv: tx: 7.06mpps, 0.03stdDev; rx: 7.07mpps, 0.00stdDev



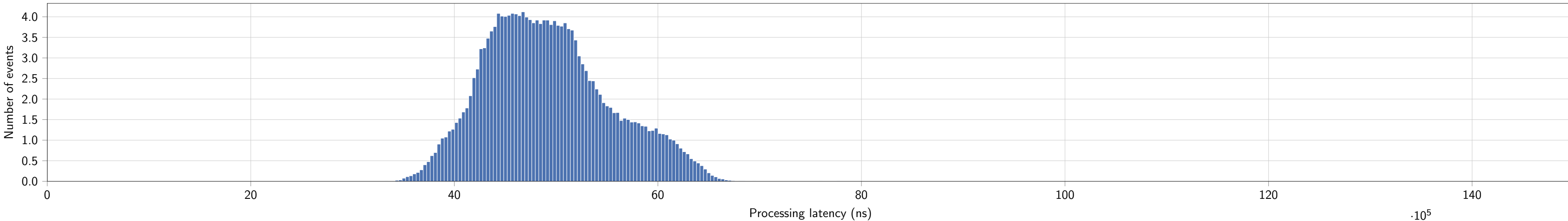
l2_bridging_cnf3_mbit4000.histogram.csv: tx: 7.81mpps, 0.04stdDev; rx: 7.82mpps, 0.00stdDev



l2_bridging_cnf3_mbit4253hires.histogram.csv: tx: 8.33mpps, 0.04stdDev; rx: 8.34mpps, 0.00stdDev

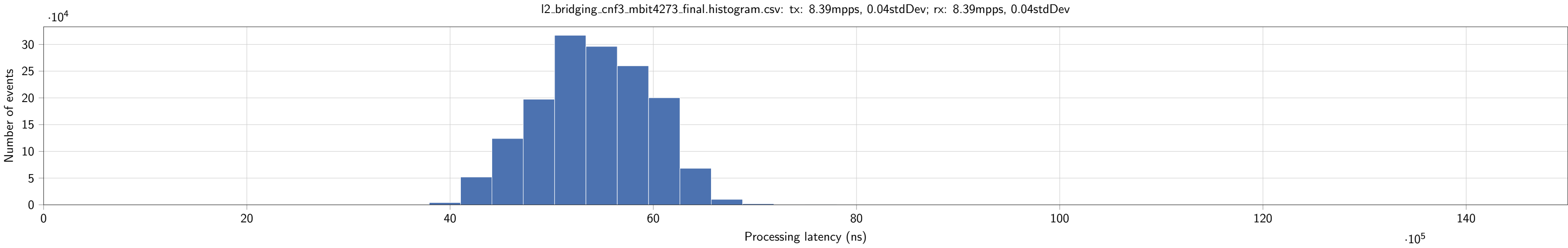


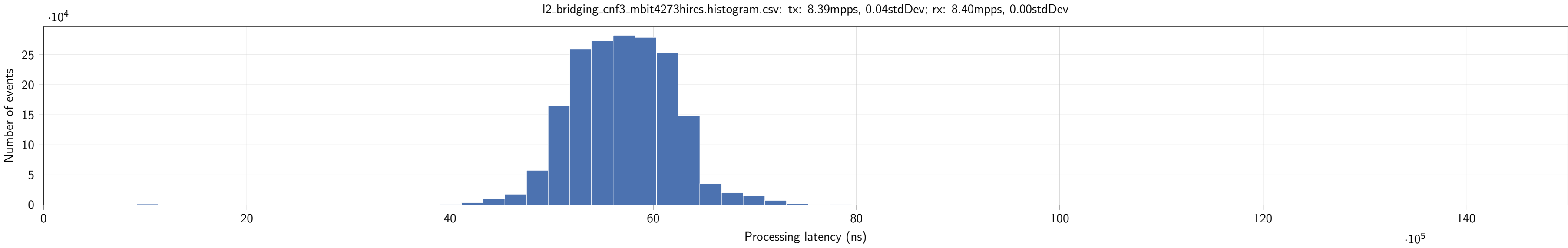
l2_bridging_cnf3_mbit4263hires.histogram.csv: tx: 8.33mpps, 0.04stdDev; rx: 8.34mpps, 0.00stdDev



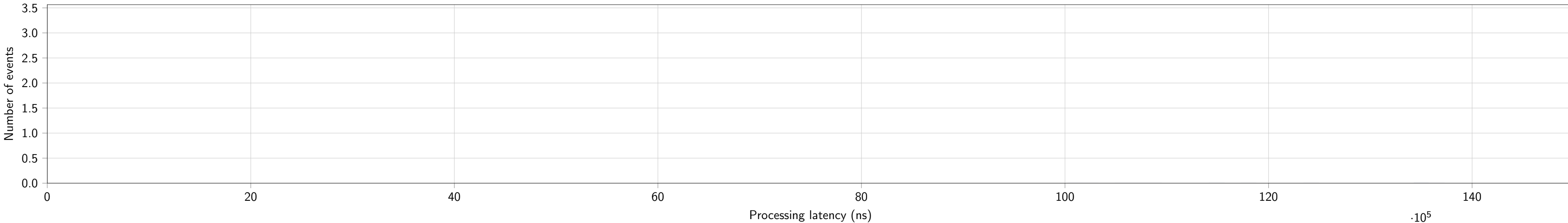
l2_bridging_cnf3_mbit4273_final.histogram.csv: tx: 8.39mpps, 0.04stdDev; rx: 8.39mpps, 0.04stdDev

Number of events

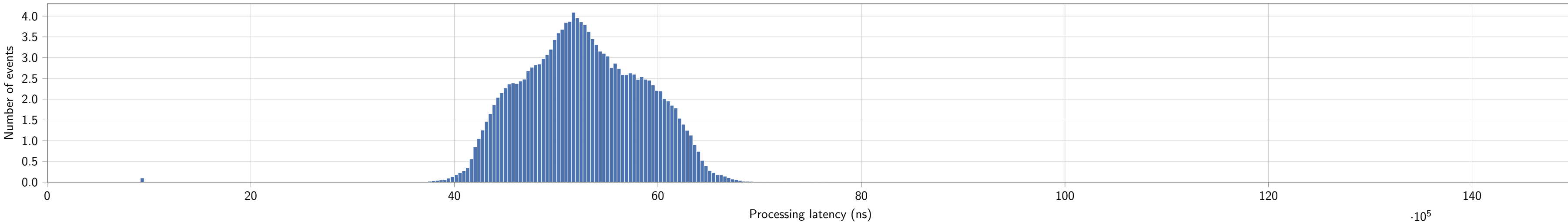




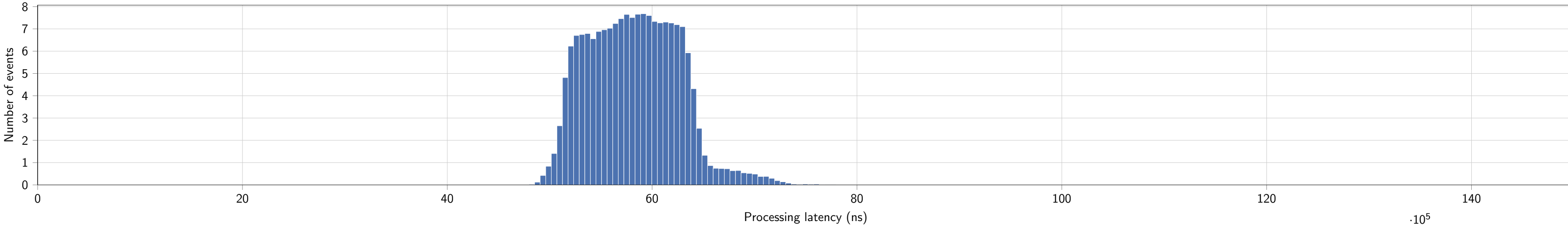
l2_bridging_cnf3_mbit4283hires.histogram.csv: tx: 8.38mpps, 0.04stdDev; rx: 8.39mpps, 0.00stdDev

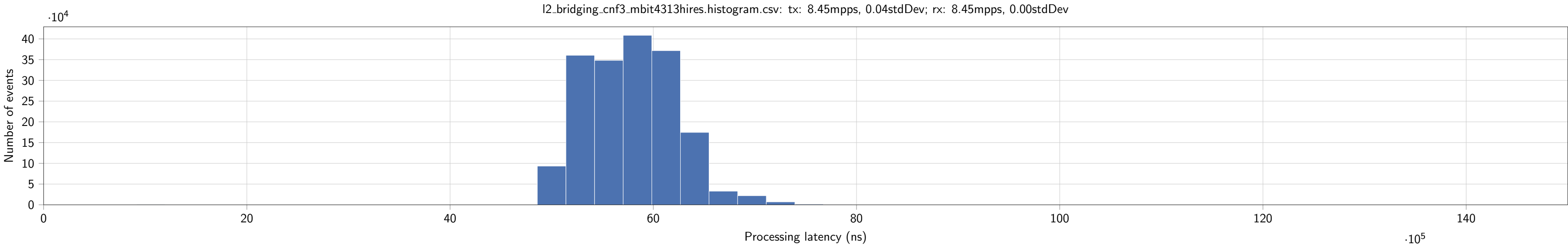


l2_bridging_cnf3_mbit4293hires.histogram.csv: tx: 8.39mpps, 0.04stdDev; rx: 8.40mpps, 0.00stdDev

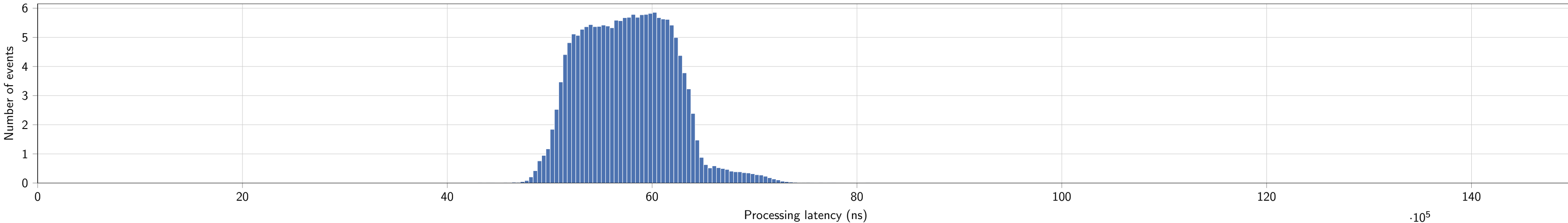


l2_bridging_cnf3_mbit4303hires.histogram.csv: tx: 8.45mpps, 0.04stdDev; rx: 8.46mpps, 0.00stdDev

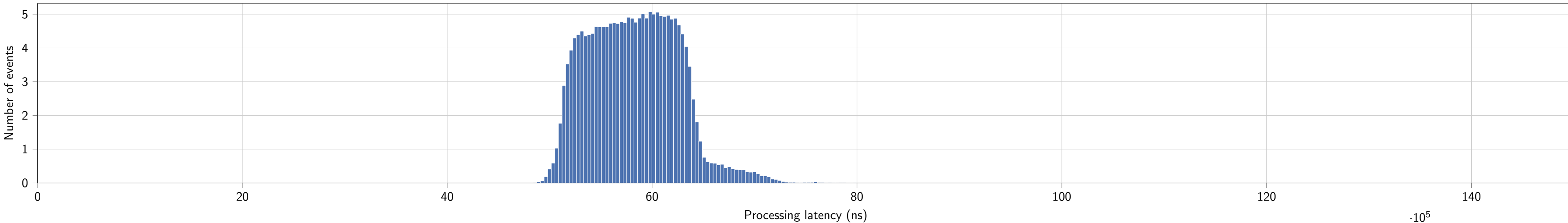




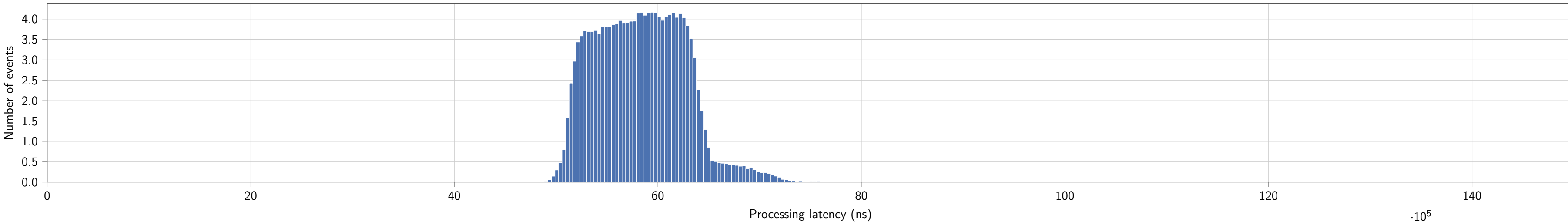
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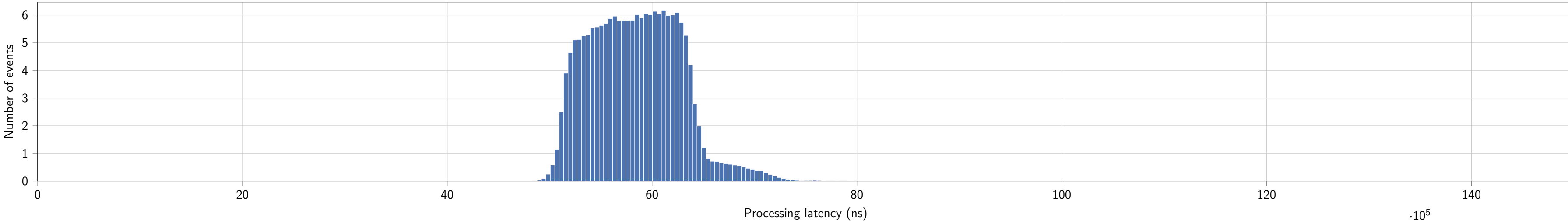
l2_bridging_cnf3_mbit4333hires.histogram.csv: tx: 8.50mpps, 0.04stdDev; rx: 8.51mpps, 0.00stdDev



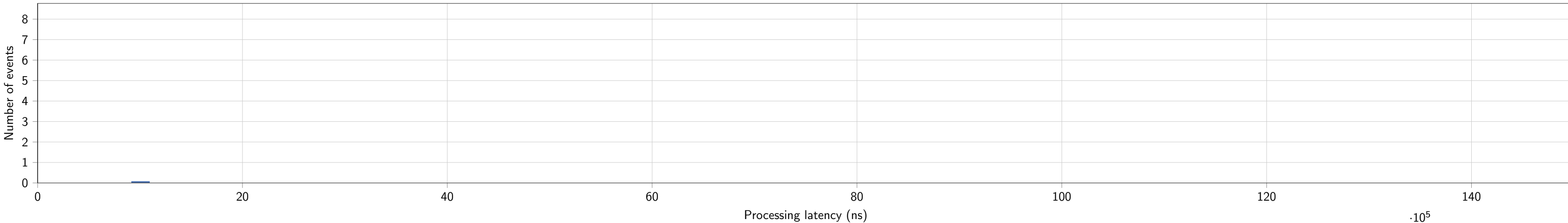
l2_bridging_cnf3_mbit4343hires.histogram.csv: tx: 8.50mpps, 0.04stdDev; rx: 8.51mpps, 0.00stdDev



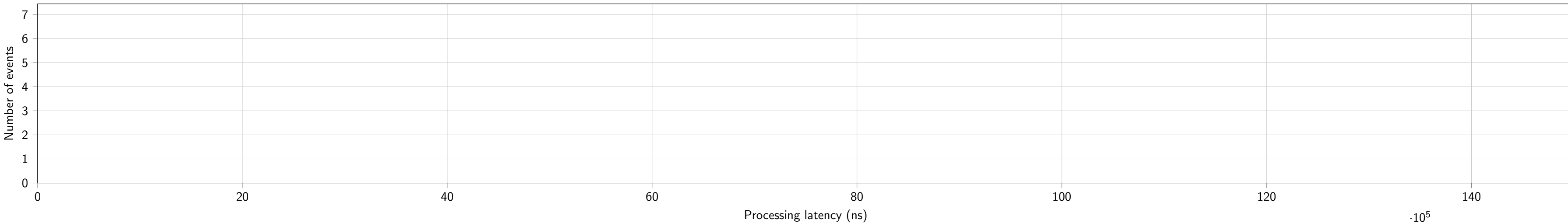
l2_bridging_cnf3_mbit4353hires.histogram.csv: tx: 8.50mpps, 0.04stdDev; rx: 8.51mpps, 0.00stdDev



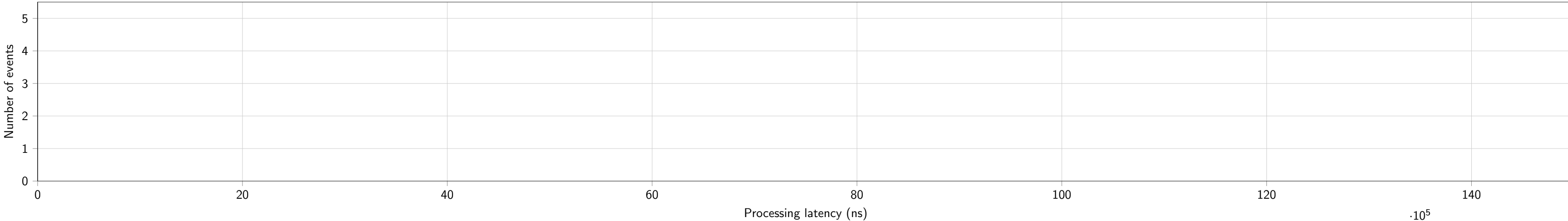
l2_bridging_cnf3_mbit4363hires.histogram.csv: tx: 8.55mpps, 0.04stdDev; rx: 8.51mpps, 0.00stdDev



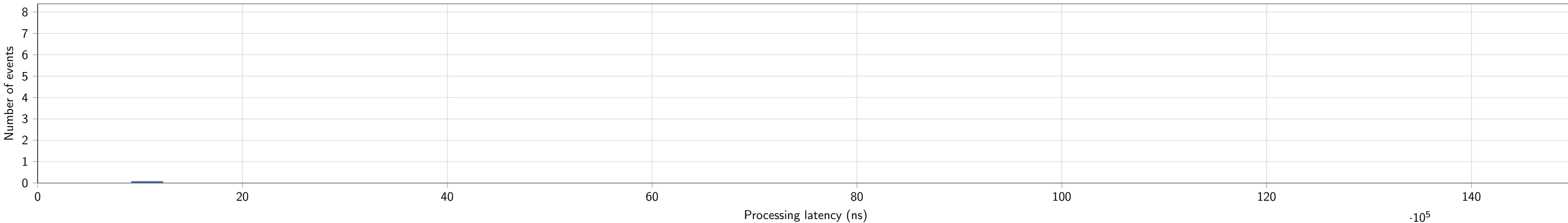
l2_bridging_cnf3_mbit4373hires.histogram.csv: tx: 8.55mpps, 0.04stdDev; rx: 8.51mpps, 0.00stdDev



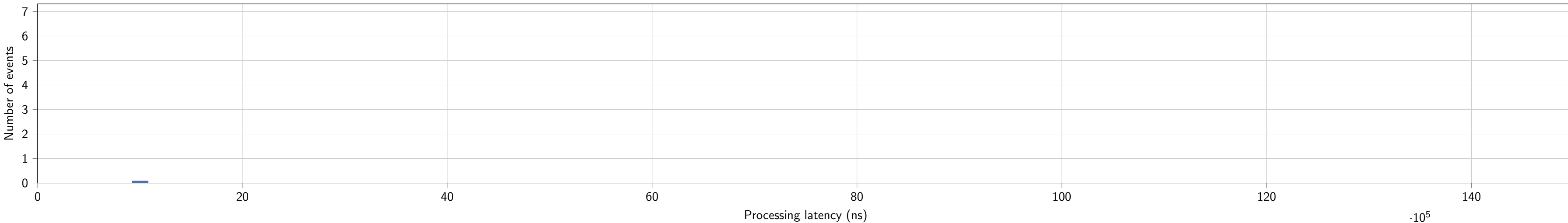
l2_bridging_cnf3_mbit4383hires.histogram.csv: tx: 8.55mpps, 0.04stdDev; rx: 8.51mpps, 0.00stdDev



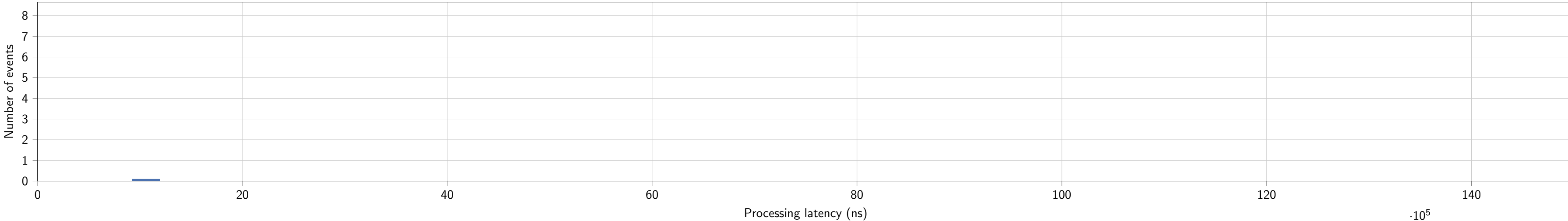
l2_bridging_cnf3_mbit4393hires.histogram.csv: tx: 8.61mpps, 0.04stdDev; rx: 8.47mpps, 0.03stdDev



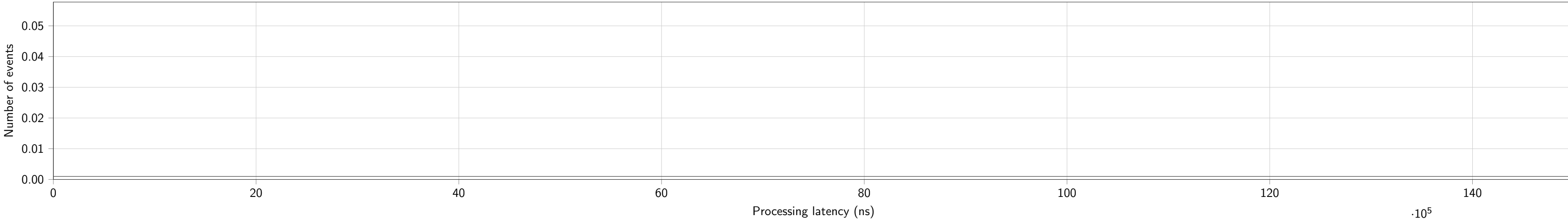
l2_bridging_cnf3_mbit4400.histogram.csv: tx: 8.61mpps, 0.04stdDev; rx: 8.51mpps, 0.00stdDev



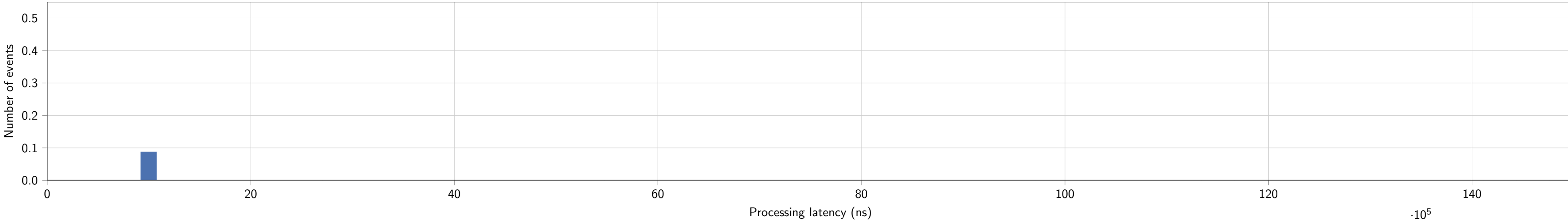
l2_bridging_cnf3_mbit4403hires.histogram.csv: tx: 8.61mpps, 0.05stdDev; rx: 8.50mpps, 0.04stdDev



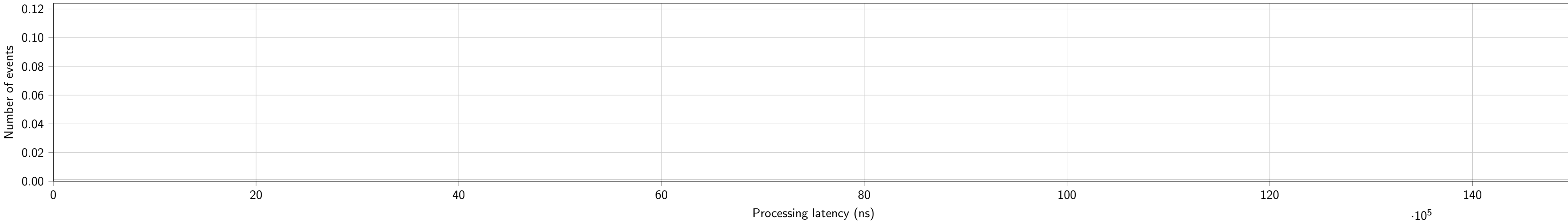
l2_bridging_cnf3_mbit4800.histogram.csv: tx: 9.39mpps, 0.05stdDev; rx: 8.37mpps, 0.00stdDev



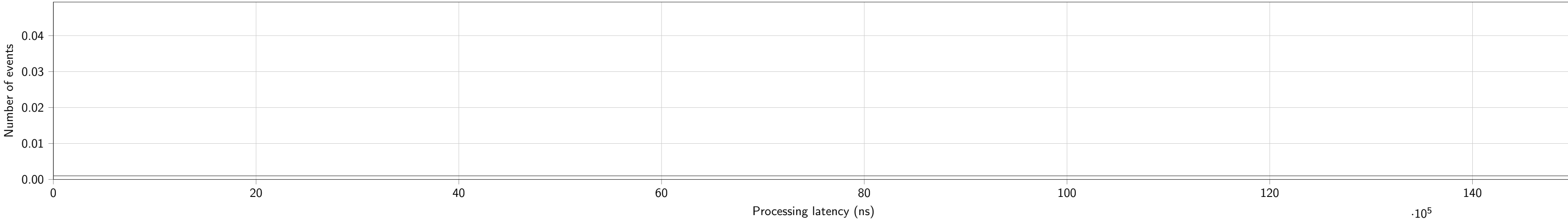
l2_bridging_cnf3_mbit5200.histogram.csv: tx: 10.15mpps, 0.05stdDev; rx: 8.49mpps, 0.00stdDev



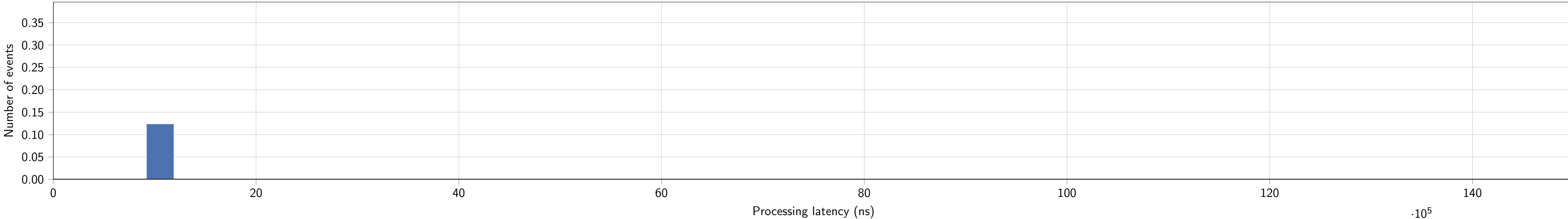
l2_bridging_cnf3_mbit5600.histogram.csv: tx: 10.95mpps, 0.05stdDev; rx: 8.52mpps, 0.00stdDev

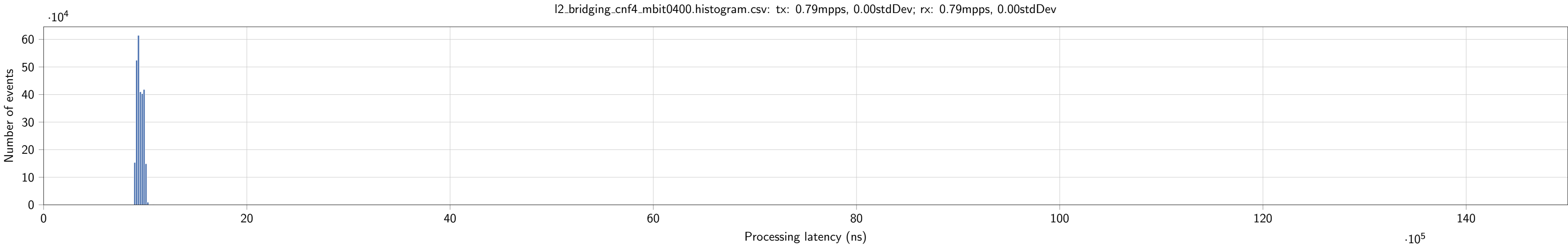


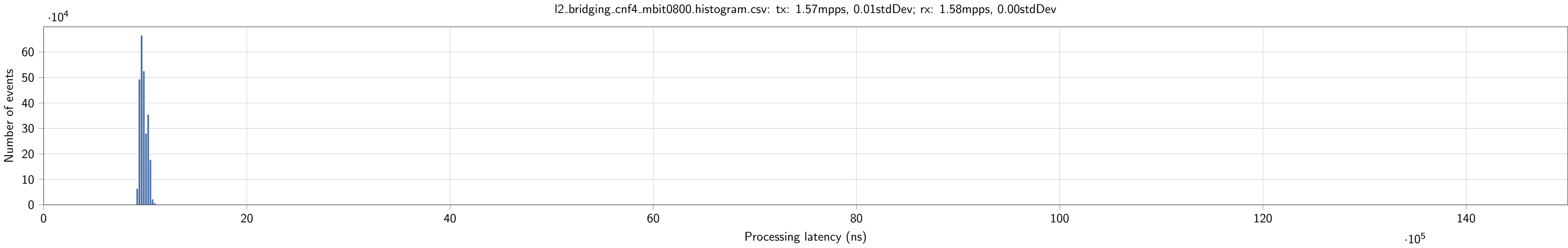
l2_bridging_cnf3_mbit6000.histogram.csv: tx: 11.78mpps, 0.06stdDev; rx: 8.48mpps, 0.00stdDev



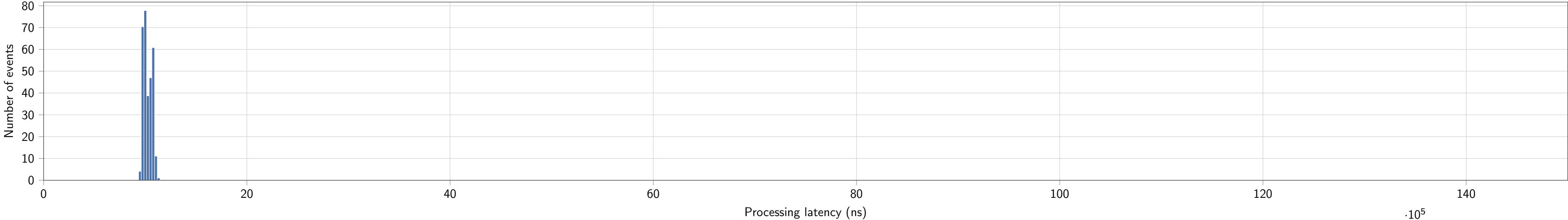
l2_bridging_cnf3_mbit9000.histogram.csv: tx: 14.86mpps, 0.07stdDev; rx: 8.50mpps, 0.04stdDev



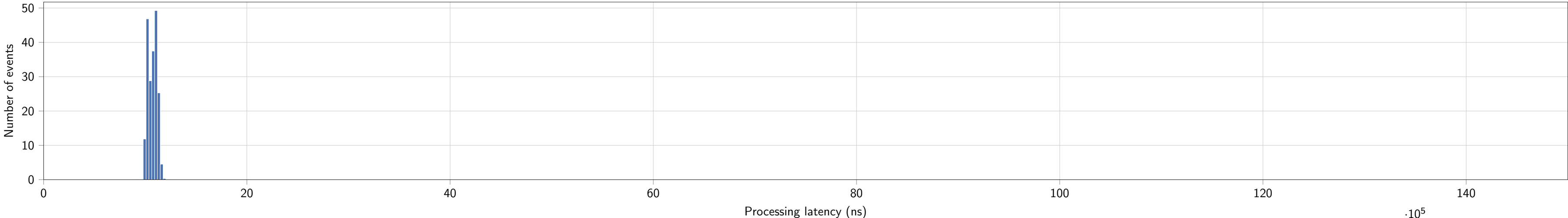


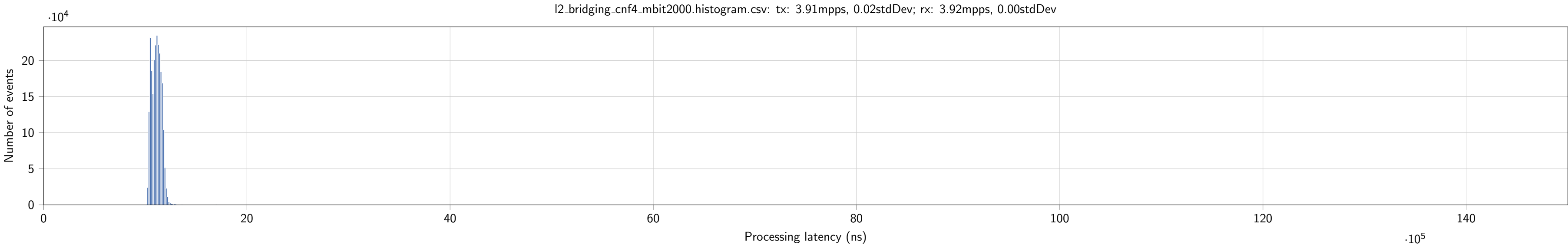


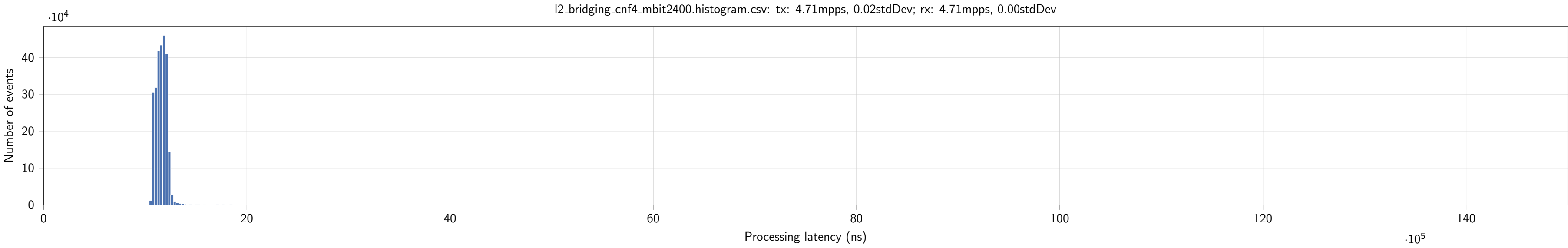
l2_bridging_cnf4_mbit1200.histogram.csv: tx: 2.36mpps, 0.01stdDev; rx: 2.36mpps, 0.00stdDev



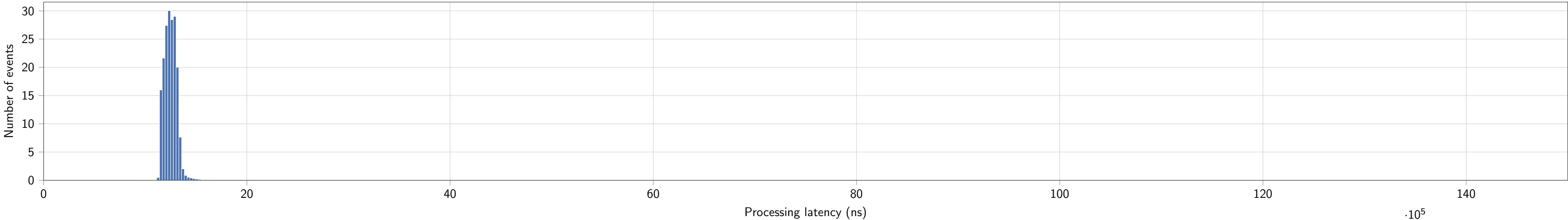
l2_bridging_cnf4_mbit1600.histogram.csv: tx: 3.13mpps, 0.02stdDev; rx: 3.14mpps, 0.00stdDev

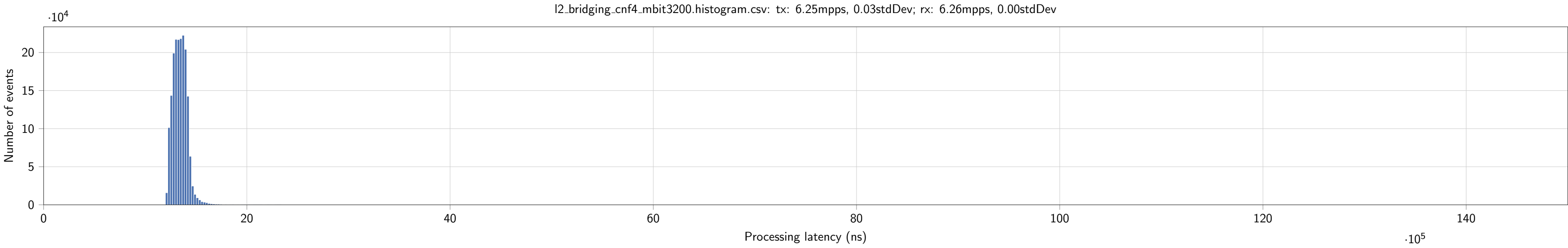




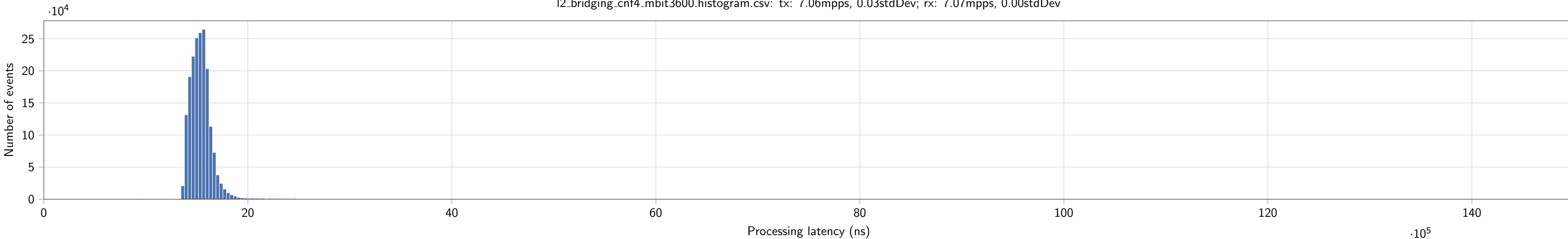


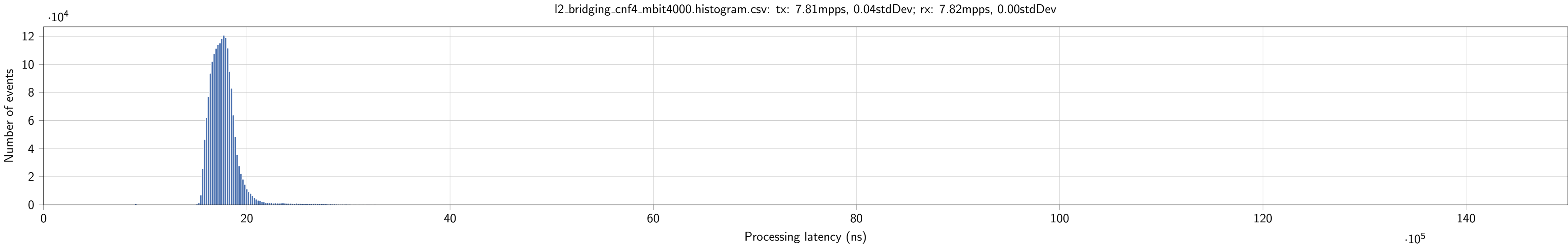
l2_bridging_cnf4_mbit2800.histogram.csv: tx: 5.49mpps, 0.03stdDev; rx: 5.49mpps, 0.00stdDev



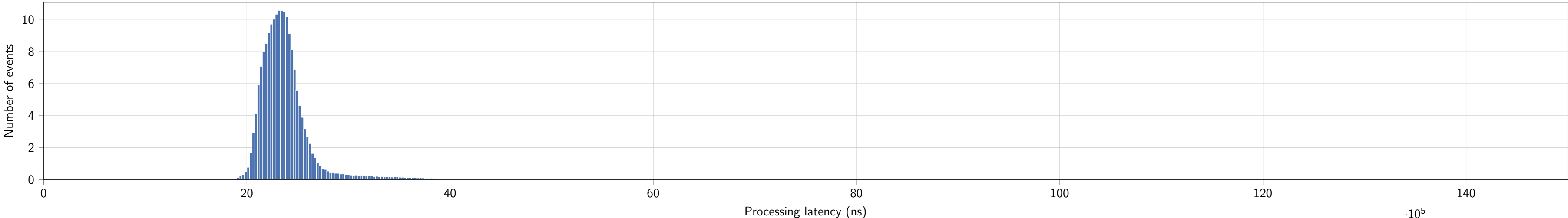


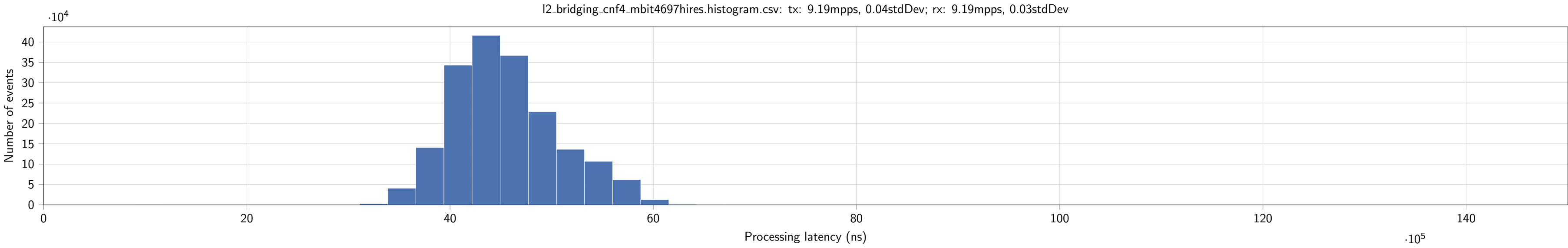
l2_bridging_cnf4_mbit3600.histogram.csv: tx: 7.06mpps, 0.03stdDev; rx: 7.07mpps, 0.00stdDev



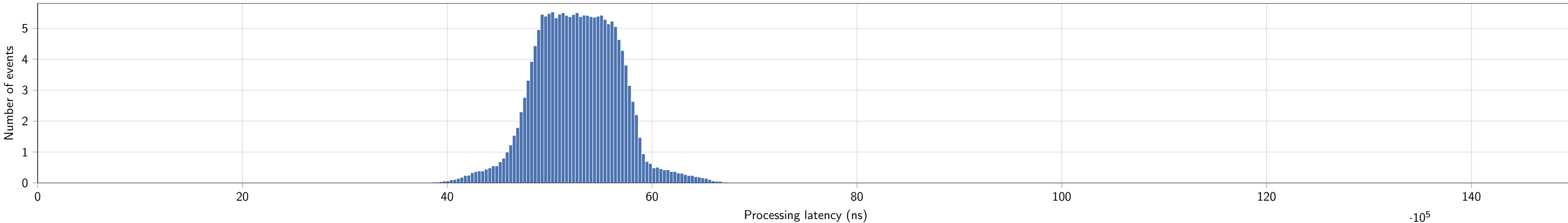


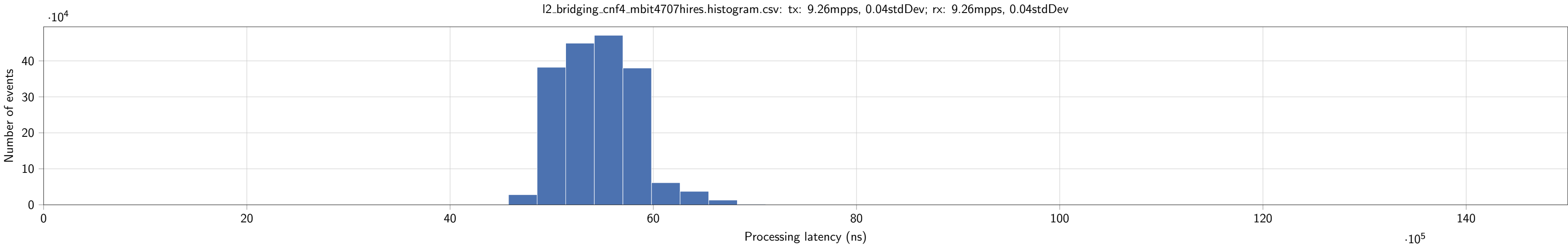
l2_bridging_cnf4_mbit4400.histogram.csv: tx: 8.62mpps, 0.04stdDev; rx: 8.63mpps, 0.00stdDev



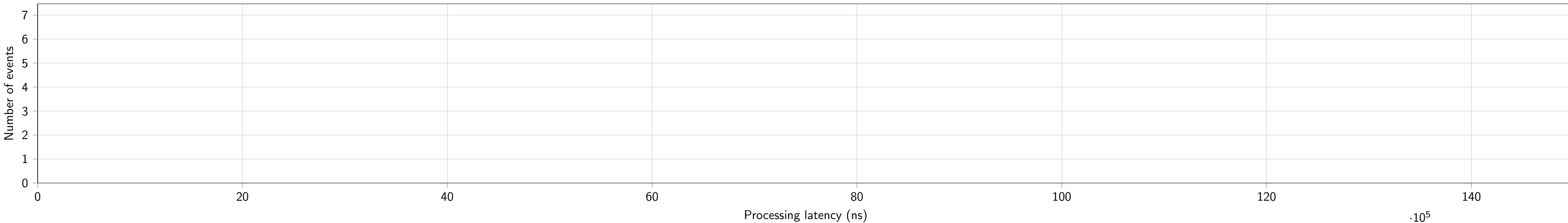


l2_bridging_cnf4_mbit4707_final.histogram.csv: tx: 9.26mpps, 0.05stdDev; rx: 9.27mpps, 0.00stdDev

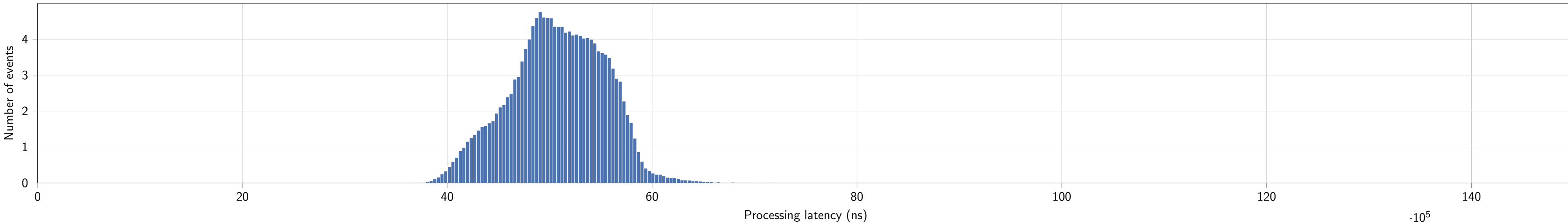




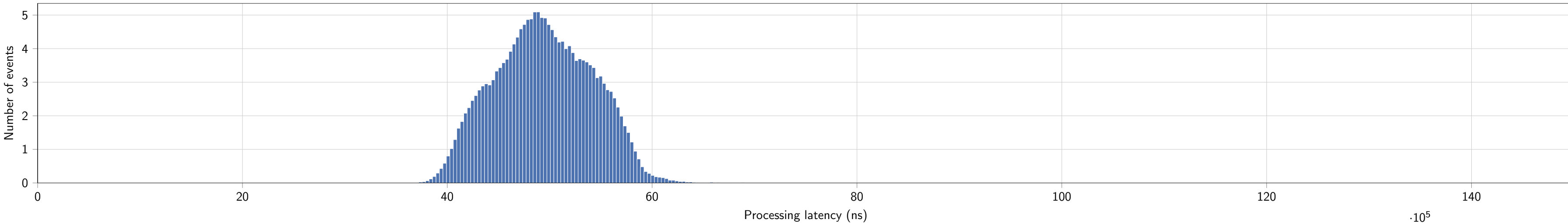
l2_bridging_cnf4_mbit4717hires.histogram.csv: tx: 9.25mpps, 0.04stdDev; rx: 9.22mpps, 0.00stdDev



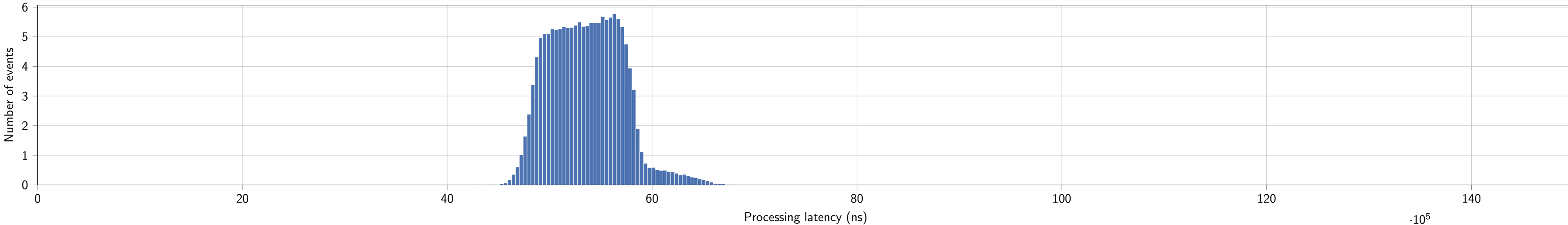
l2_bridging_cnf4_mbit4727hires.histogram.csv: tx: 9.26mpps, 0.05stdDev; rx: 9.27mpps, 0.00stdDev



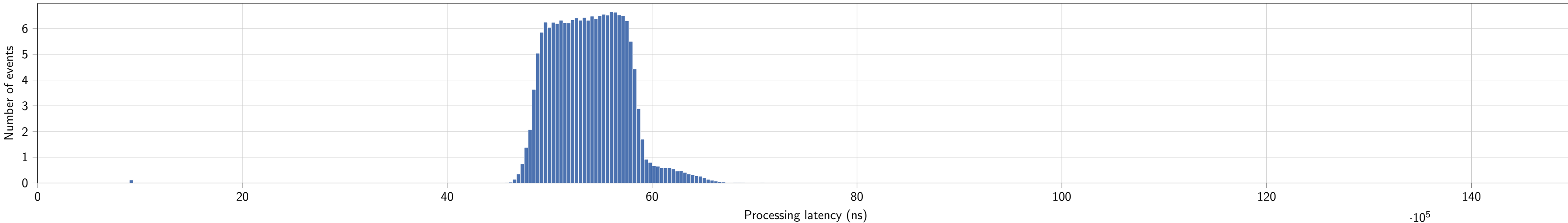
l2_bridging_cnf4_mbit4737hires.histogram.csv: tx: 9.26mpps, 0.04stdDev; rx: 9.27mpps, 0.00stdDev

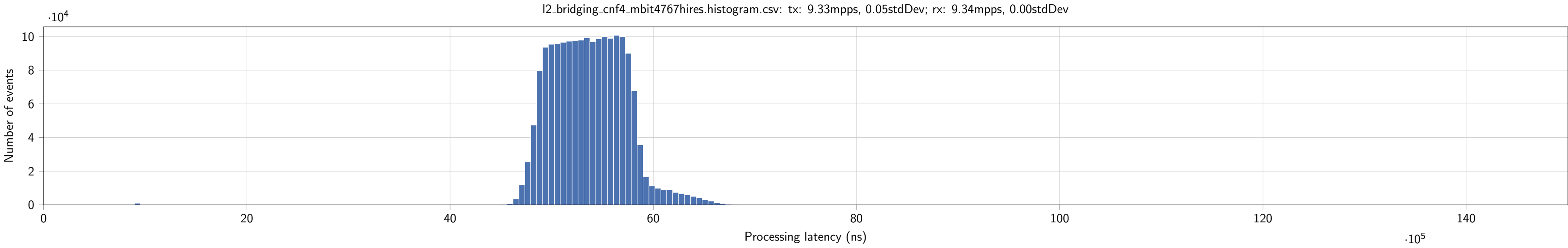


l2_bridging_cnf4_mbit4747hires.histogram.csv: tx: 9.33mpps, 0.05stdDev; rx: 9.34mpps, 0.00stdDev

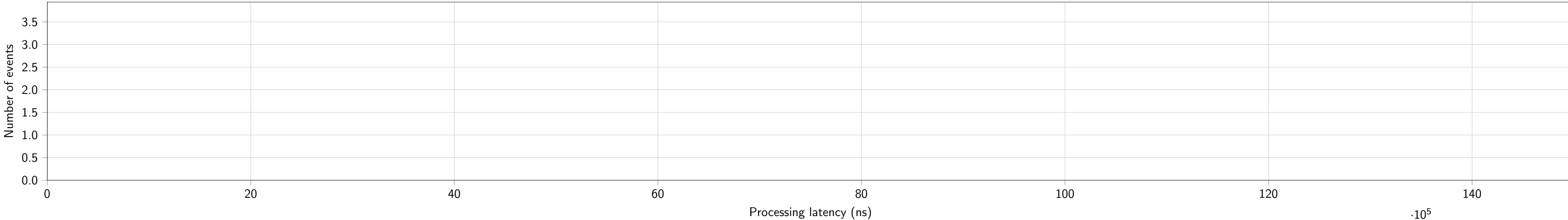


l2_bridging_cnf4_mbit4757hires.histogram.csv: tx: 9.33mpps, 0.05stdDev; rx: 9.34mpps, 0.00stdDev

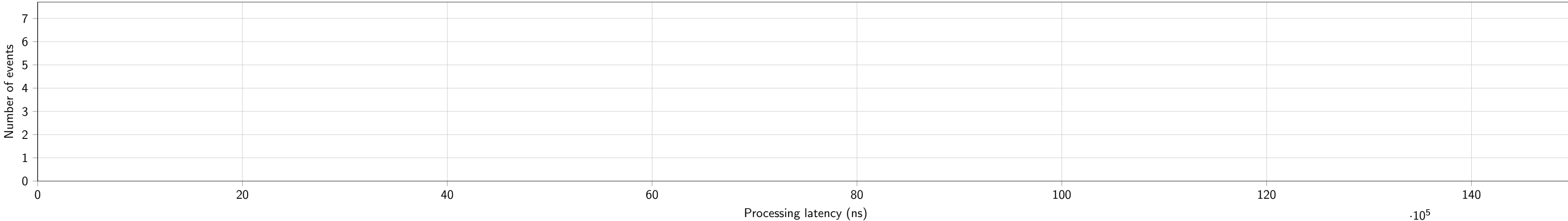




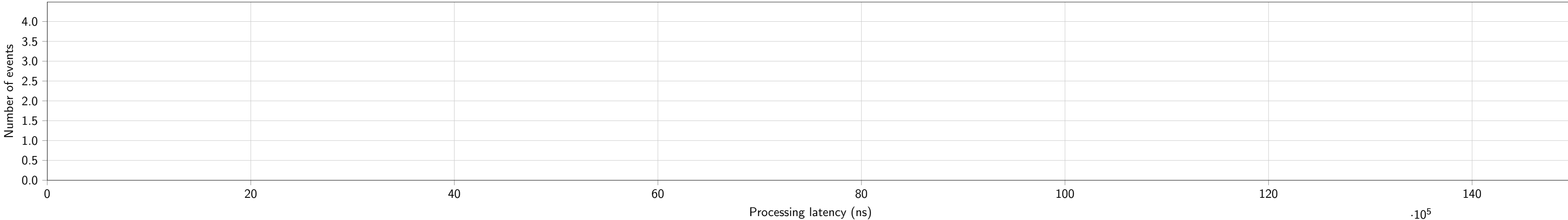
l2_bridging_cnf4_mbit4777hires.histogram.csv: tx: 9.39mpps, 0.05stdDev; rx: 9.38mpps, 0.00stdDev



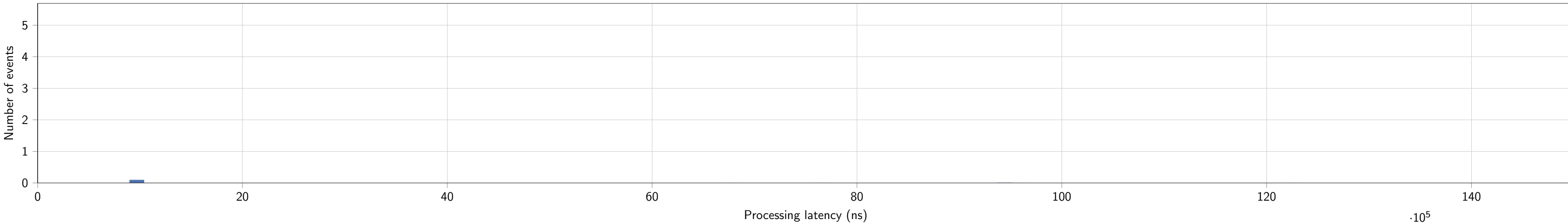
l2_bridging_cnf4_mbit4787hires.histogram.csv: tx: 9.39mpps, 0.04stdDev; rx: 9.37mpps, 0.00stdDev



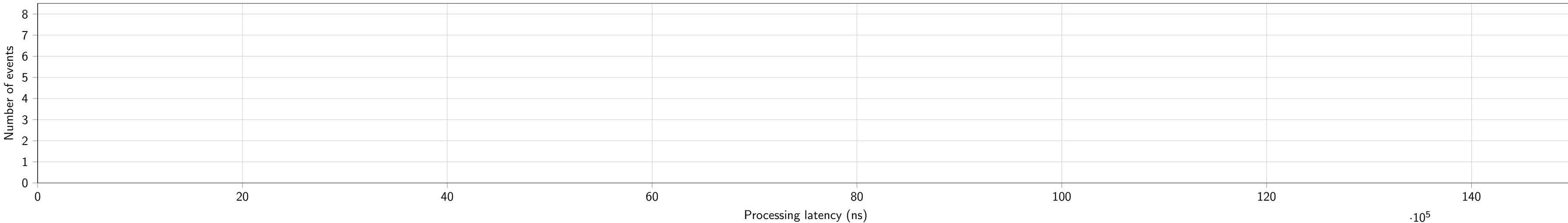
l2_bridging_cnf4_mbit4797hires.histogram.csv: tx: 9.39mpps, 0.05stdDev; rx: 9.33mpps, 0.00stdDev



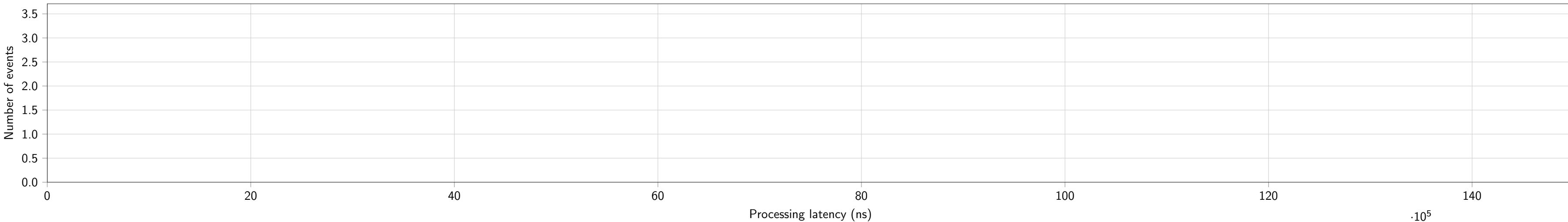
l2_bridging_cnf4_mbit4800.histogram.csv: tx: 9.39mpps, 0.05stdDev; rx: 9.38mpps, 0.00stdDev



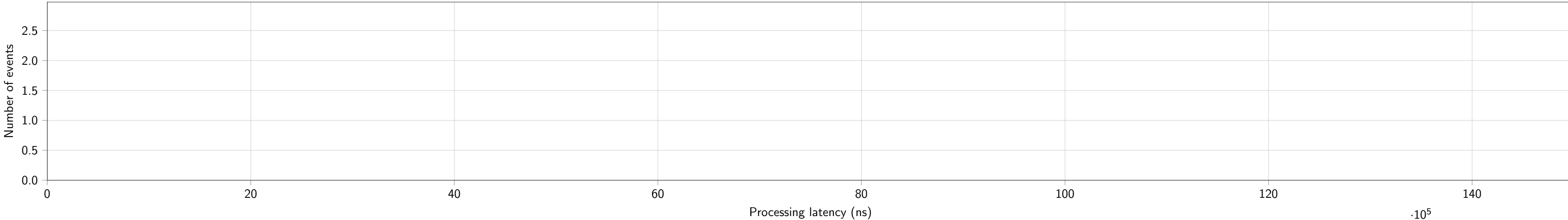
l2_bridging_cnf4_mbit4807hires.histogram.csv: tx: 9.39mpps, 0.05stdDev; rx: 9.33mpps, 0.04stdDev



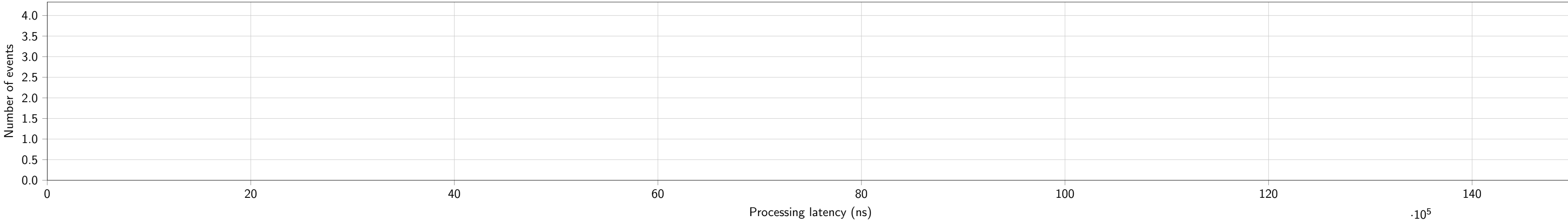
l2_bridging_cnf4_mbit4817hires.histogram.csv: tx: 9.46mpps, 0.05stdDev; rx: 9.37mpps, 0.00stdDev



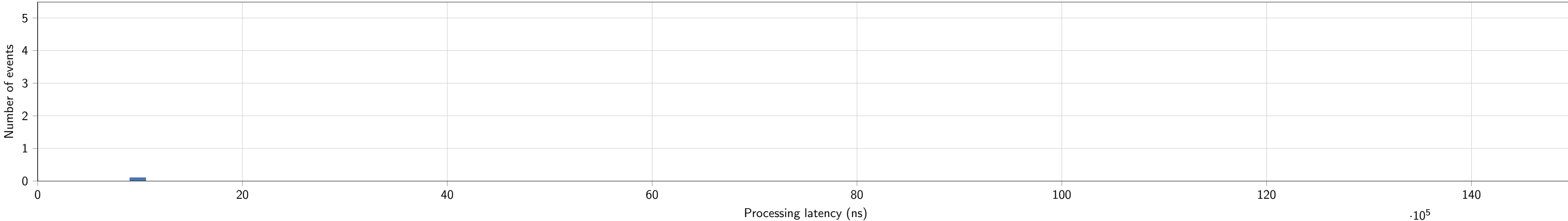
l2_bridging_cnf4_mbit4827hires.histogram.csv: tx: 9.46mpps, 0.05stdDev; rx: 9.36mpps, 0.00stdDev



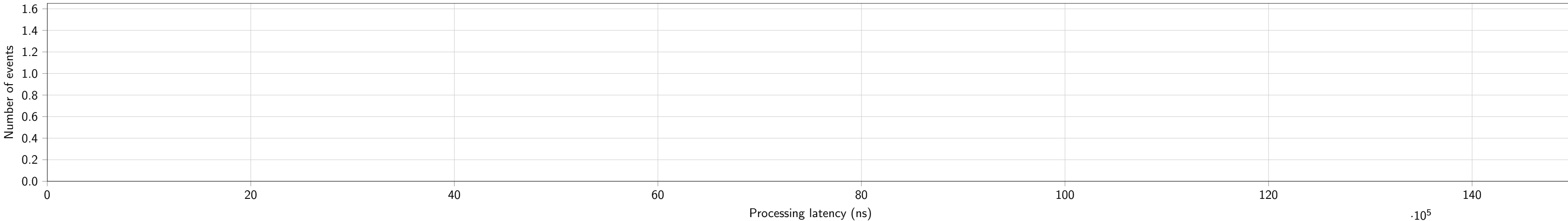
l2_bridging_cnf4_mbit4837hires.histogram.csv: tx: 9.46mpps, 0.05stdDev; rx: 9.37mpps, 0.00stdDev



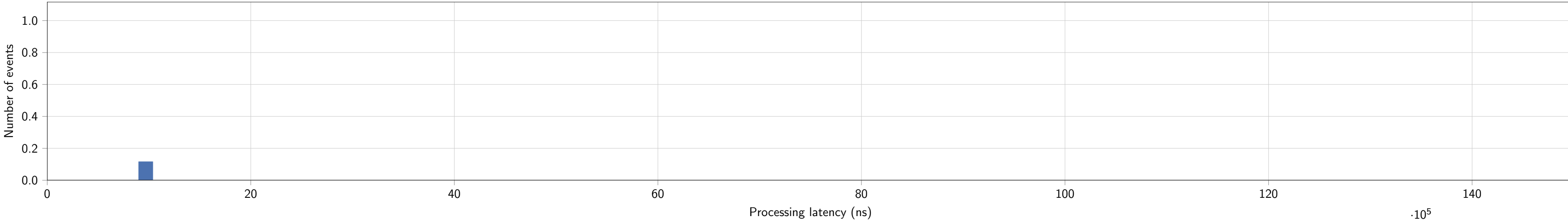
l2_bridging_cnf4_mbit4847hires.histogram.csv: tx: 9.46mpps, 0.05stdDev; rx: 9.37mpps, 0.00stdDev



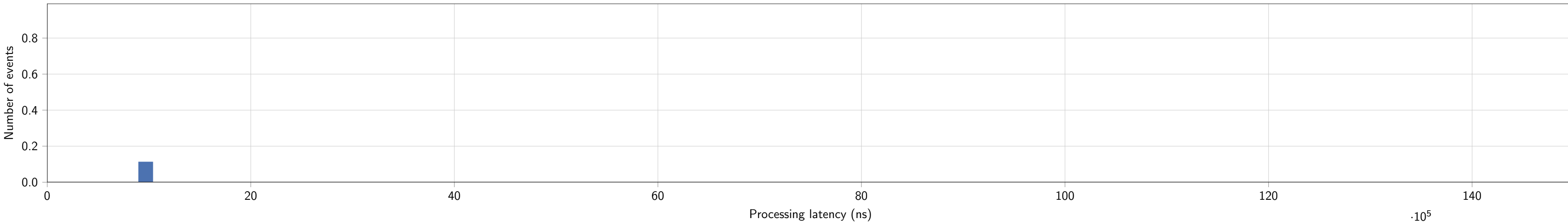
l2_bridging_cnf4_mbit5200.histogram.csv: tx: 10.15mpps, 0.05stdDev; rx: 9.36mpps, 0.04stdDev



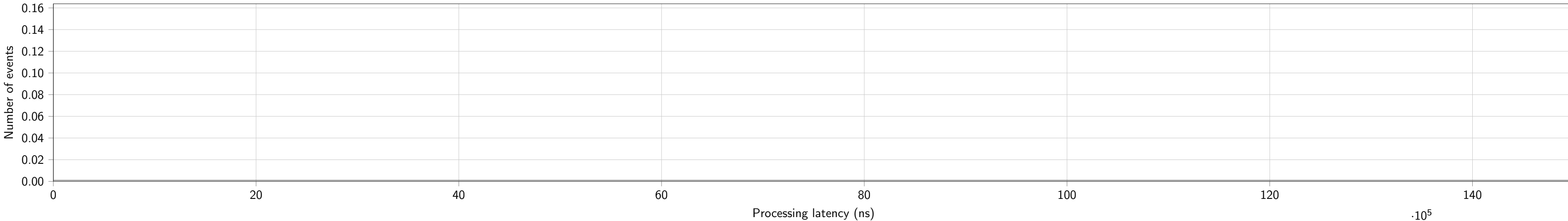
l2_bridging_cnf4_mbit5600.histogram.csv: tx: 10.95mpps, 0.05stdDev; rx: 9.37mpps, 0.00stdDev

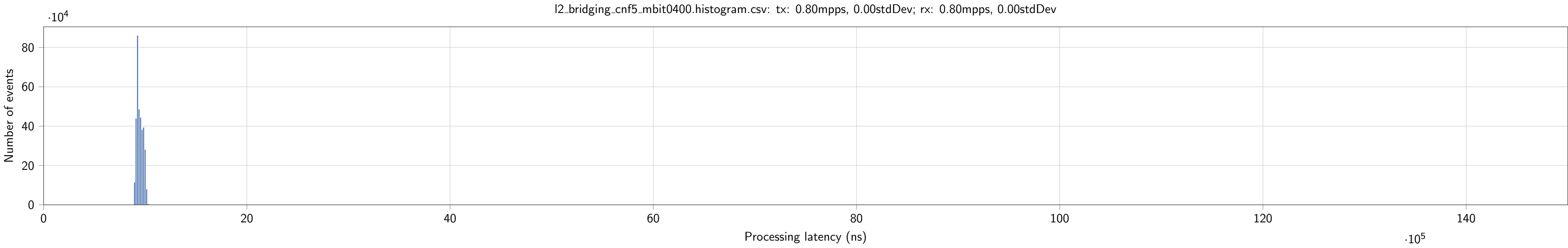


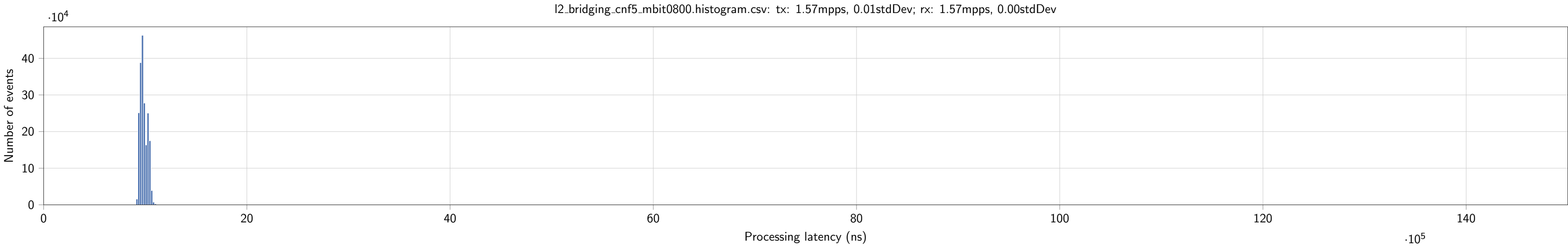
l2_bridging_cnf4_mbit6000.histogram.csv: tx: 11.78mpps, 0.06stdDev; rx: 9.33mpps, 0.00stdDev

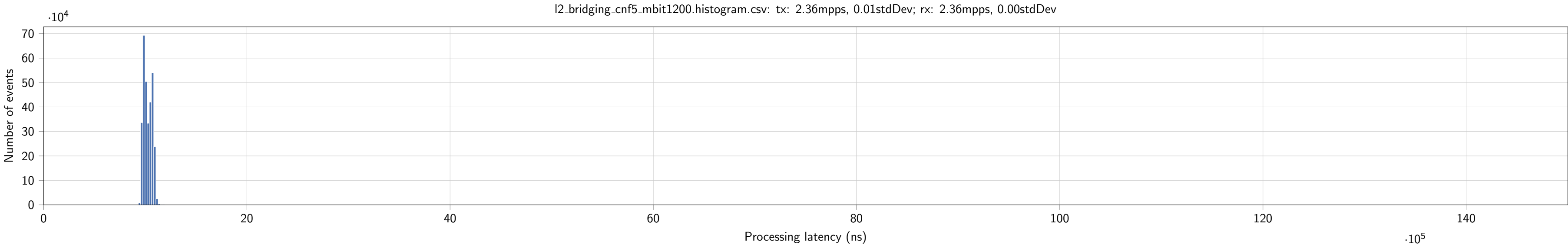


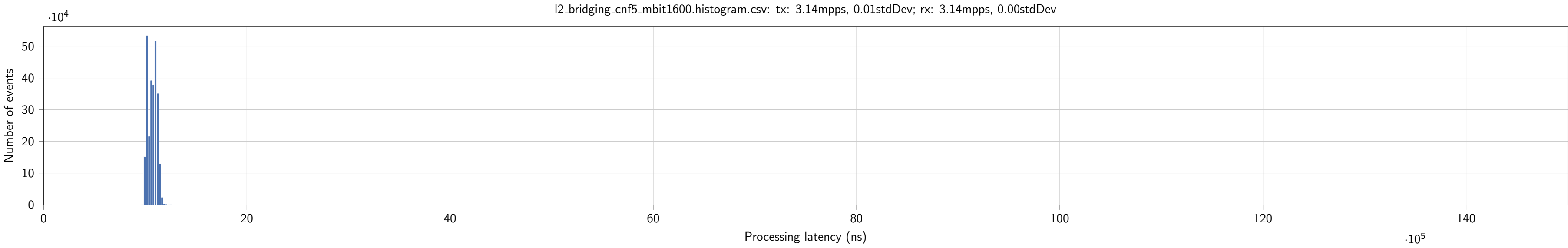
l2_bridging_cnf4_mbit9000.histogram.csv: tx: 14.86mpps, 0.07stdDev; rx: 9.37mpps, 0.00stdDev

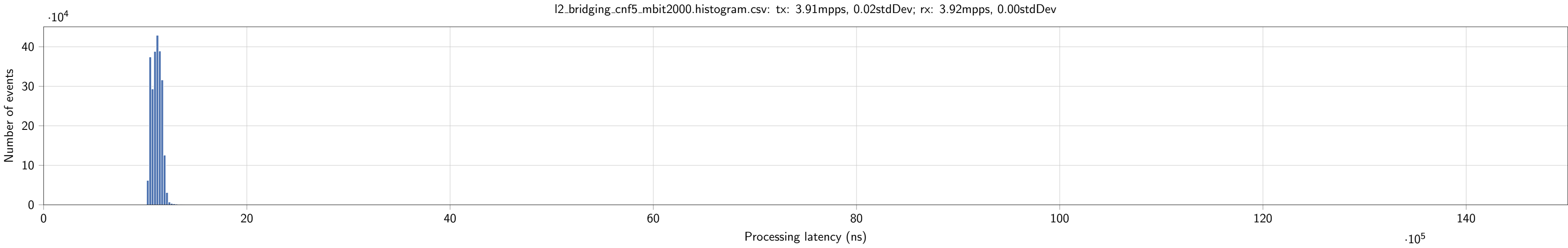






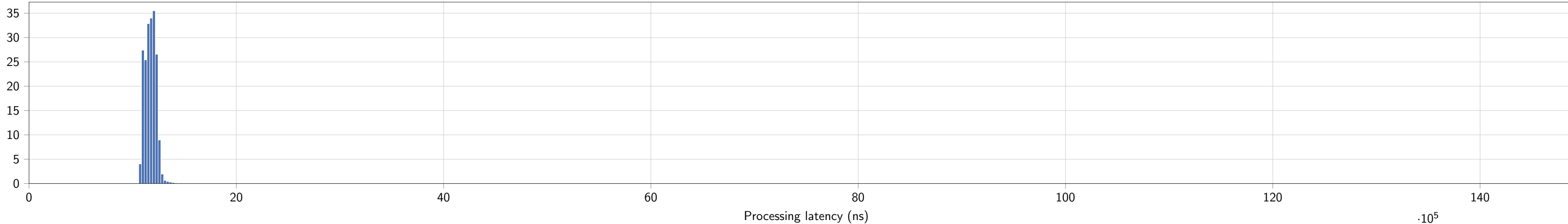




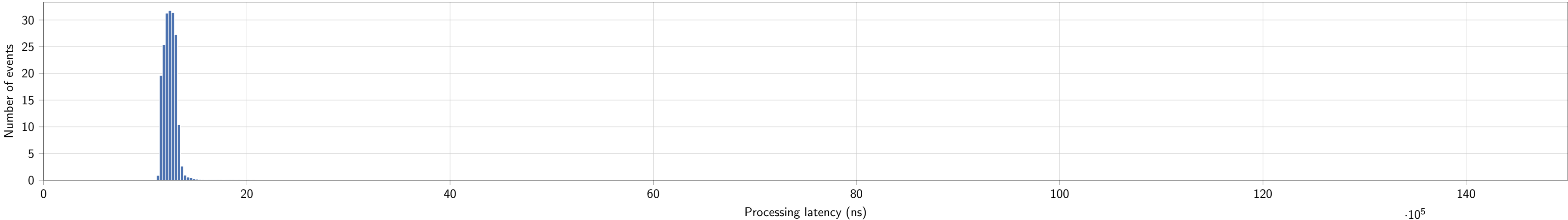


l2_bridging_cnf5_mbit2400.histogram.csv: tx: 4.70mpps, 0.02stdDev; rx: 4.71mpps, 0.00stdDev

Number of events



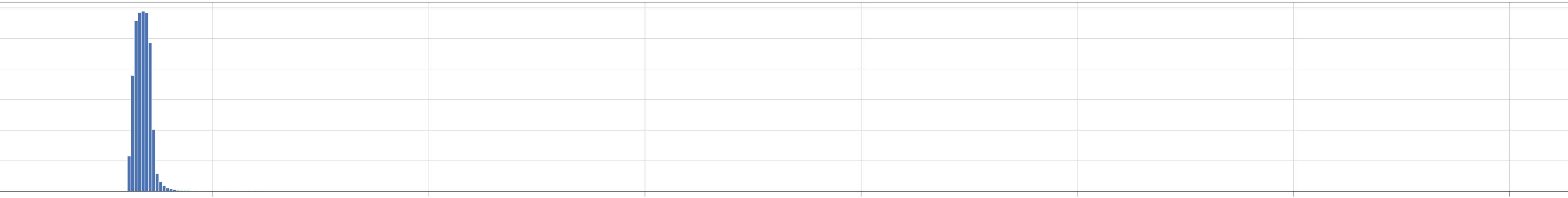
l2_bridging_cnf5_mbit2800.histogram.csv: tx: 5.49mpps, 0.03stdDev; rx: 5.49mpps, 0.00stdDev



l2_bridging_cnf5_mbit3200.histogram.csv: tx: 6.25mpps, 0.03stdDev; rx: 6.26mpps, 0.00stdDev

Number of events

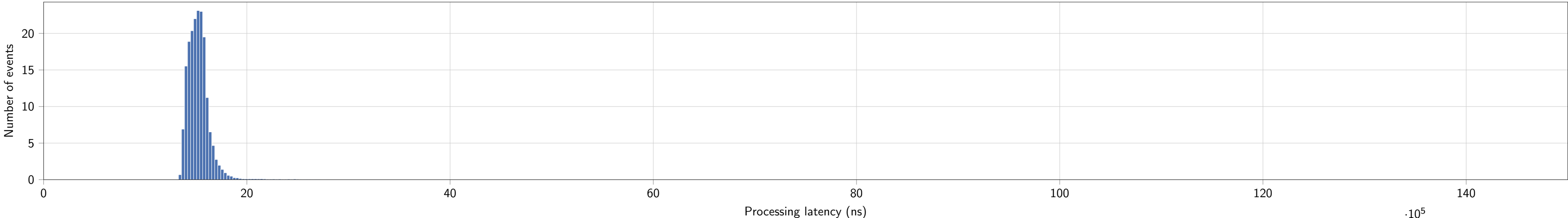
30
25
20
15
10
5
0



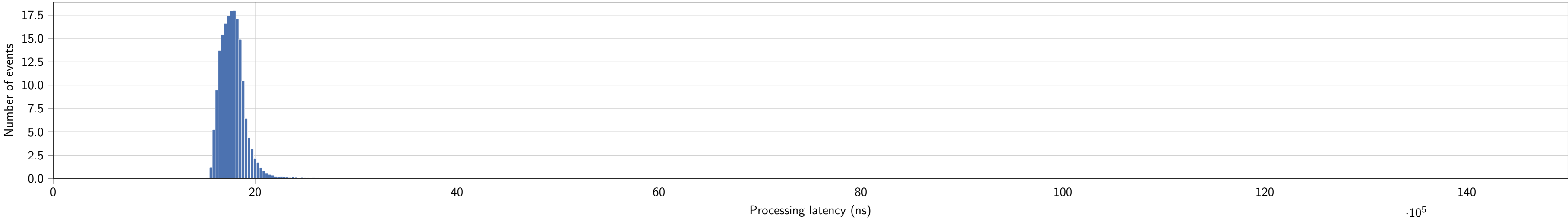
Processing latency (ns)

$\cdot 10^5$

l2_bridging_cnf5_mbit3600.histogram.csv: tx: 7.06mpps, 0.03stdDev; rx: 7.07mpps, 0.00stdDev



l2_bridging_cnf5_mbit4000.histogram.csv: tx: 7.81mpps, 0.04stdDev; rx: 7.82mpps, 0.00stdDev



l2_bridging_cnf5_mbit4400.histogram.csv: tx: 8.62mpps, 0.04stdDev; rx: 8.63mpps, 0.00stdDev

Number of events

16
14
12
10
8
6
4
2
0

$\cdot 10^4$

20

40

60

80

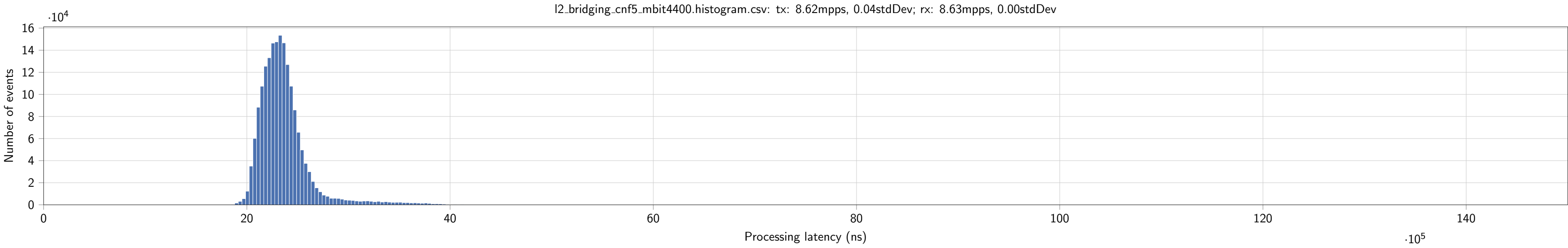
100

120

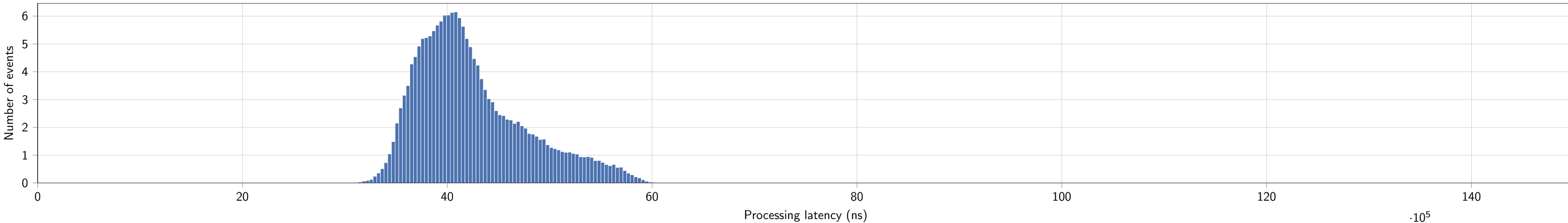
140

Processing latency (ns)

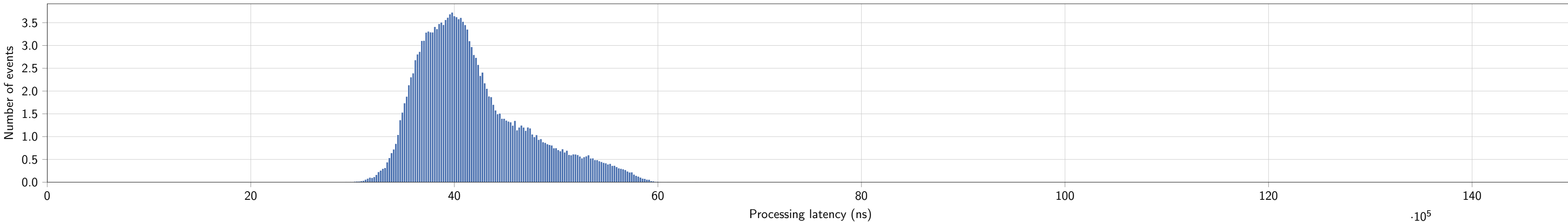
$\cdot 10^5$



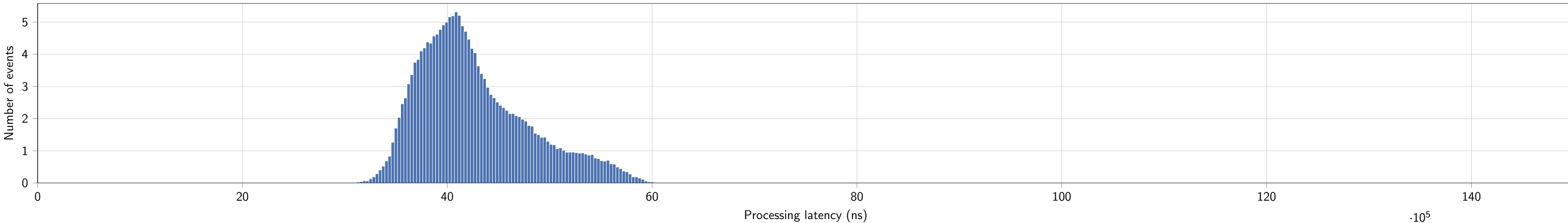
l2_bridging_cnf5_mbit4685hires.histogram.csv: tx: 9.19mpps, 0.04stdDev; rx: 9.20mpps, 0.00stdDev



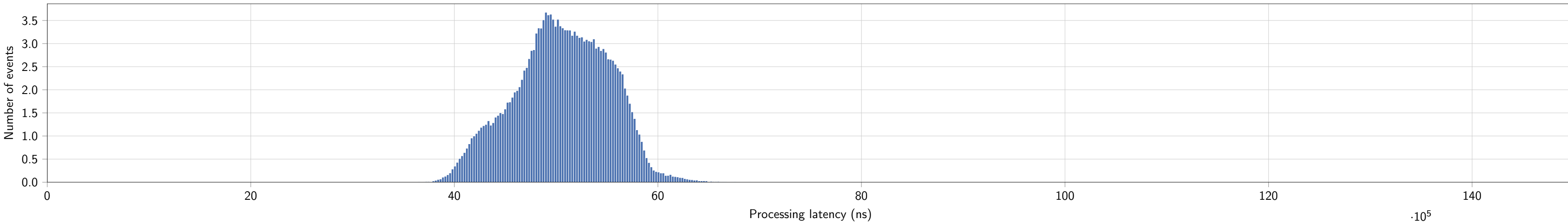
l2_bridging_cnf5_mbit4695hires.histogram.csv: tx: 9.19mpps, 0.04stdDev; rx: 9.20mpps, 0.00stdDev



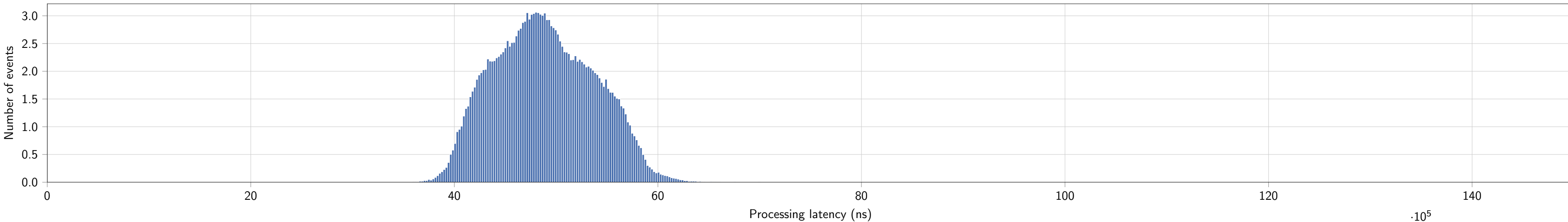
l2_bridging_cnf5_mbit4705hires.histogram.csv: tx: 9.19mpps, 0.04stdDev; rx: 9.20mpps, 0.00stdDev



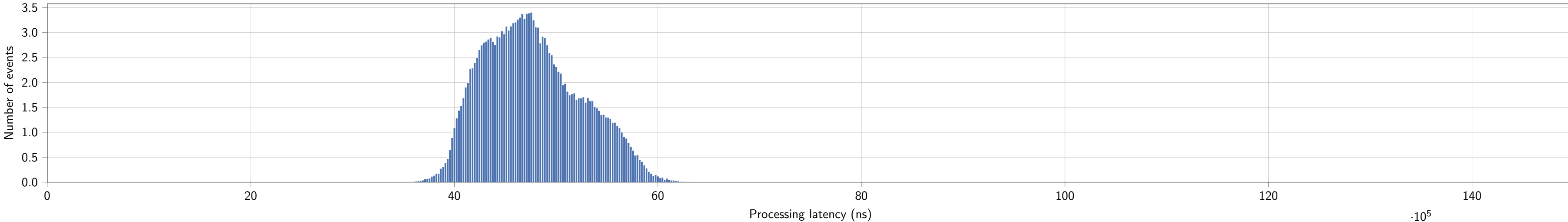
l2_bridging_cnf5_mbit4715hires.histogram.csv: tx: 9.26mpps, 0.05stdDev; rx: 9.27mpps, 0.00stdDev



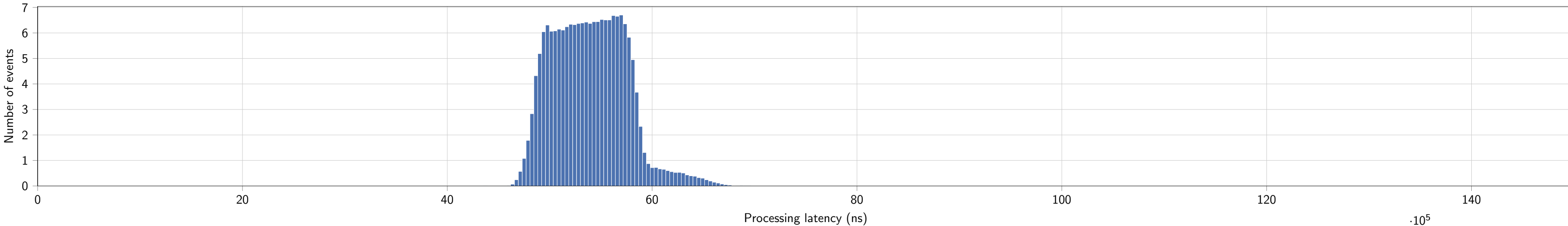
l2_bridging_cnf5_mbit4725hires.histogram.csv: tx: 9.26mpps, 0.04stdDev; rx: 9.27mpps, 0.00stdDev



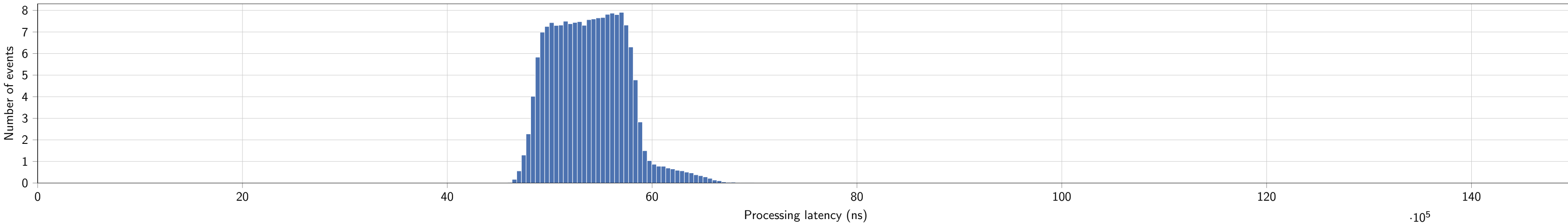
l2_bridging_cnf5_mbit4735hires.histogram.csv: tx: 9.26mpps, 0.04stdDev; rx: 9.27mpps, 0.00stdDev

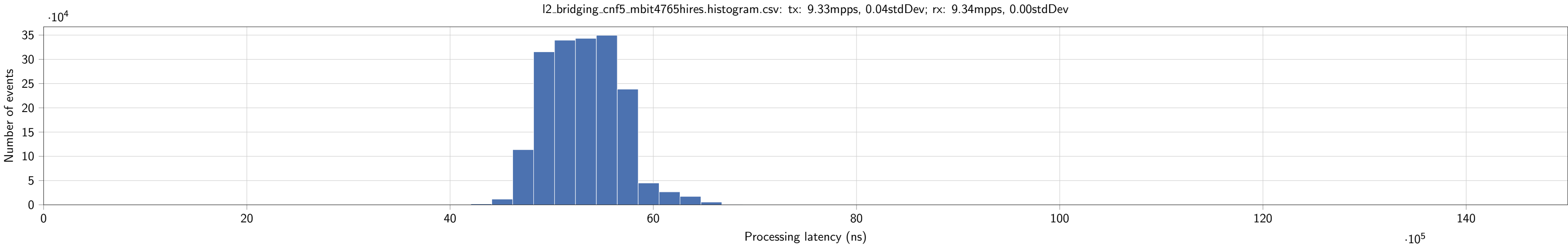


l2_bridging_cnf5_mbit4745hires.histogram.csv: tx: 9.33mpps, 0.05stdDev; rx: 9.34mpps, 0.00stdDev

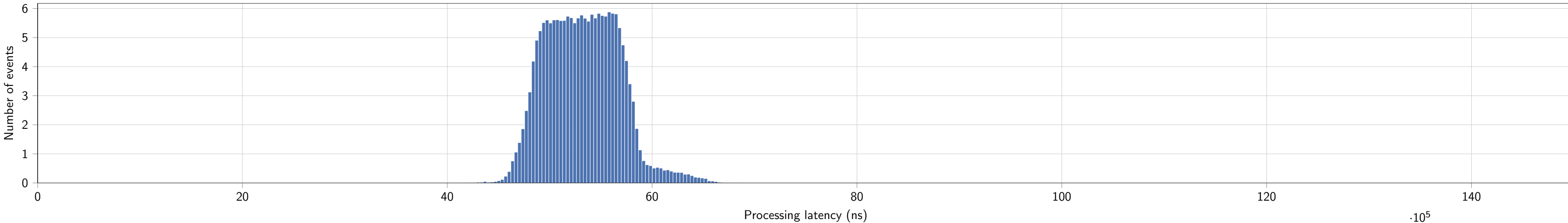


l2_bridging_cnf5_mbit4755hires.histogram.csv: tx: 9.33mpps, 0.05stdDev; rx: 9.34mpps, 0.00stdDev

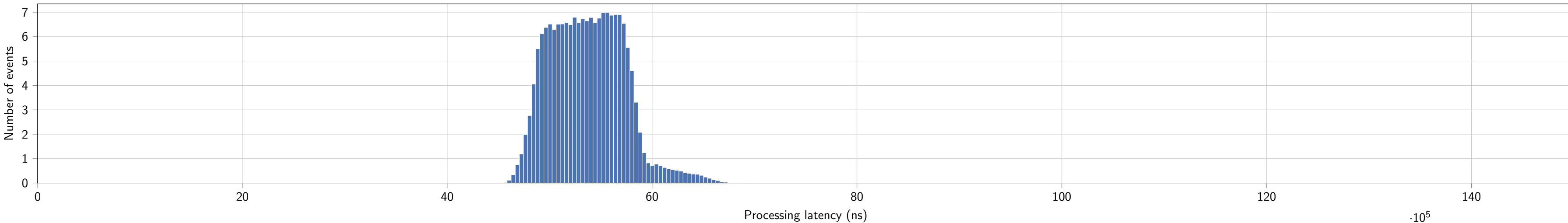




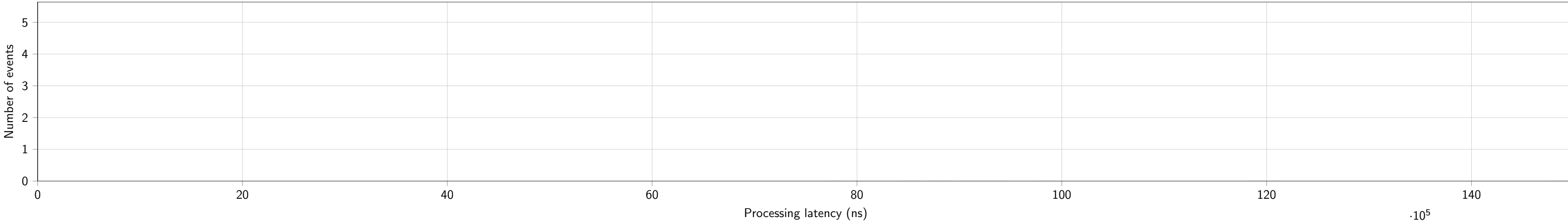
l2_bridging_cnf5_mbit4775_final.histogram.csv: tx: 9.33mpps, 0.04stdDev; rx: 9.34mpps, 0.00stdDev



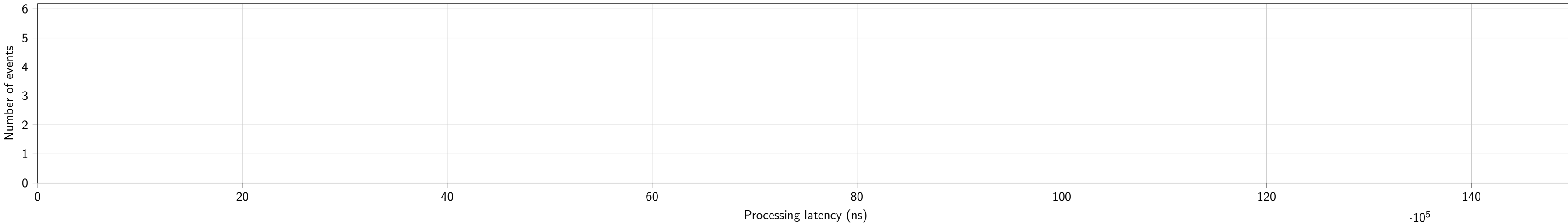
l2_bridging_cnf5_mbit4775hires.histogram.csv: tx: 9.33mpps, 0.05stdDev; rx: 9.34mpps, 0.00stdDev



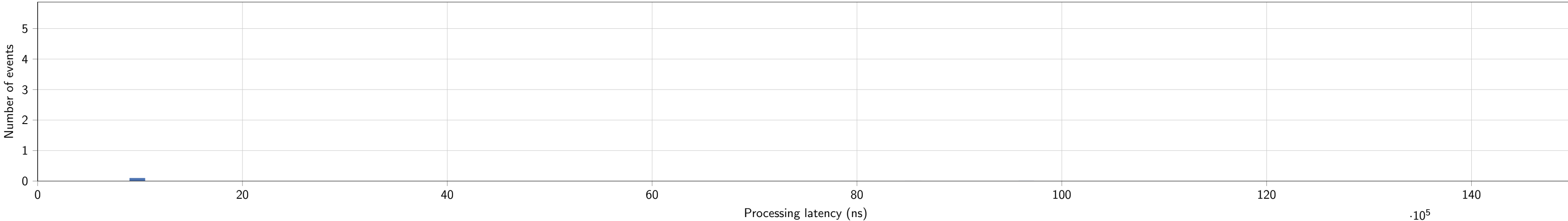
l2_bridging_cnf5_mbit4785hires.histogram.csv: tx: 9.39mpps, 0.04stdDev; rx: 9.39mpps, 0.00stdDev



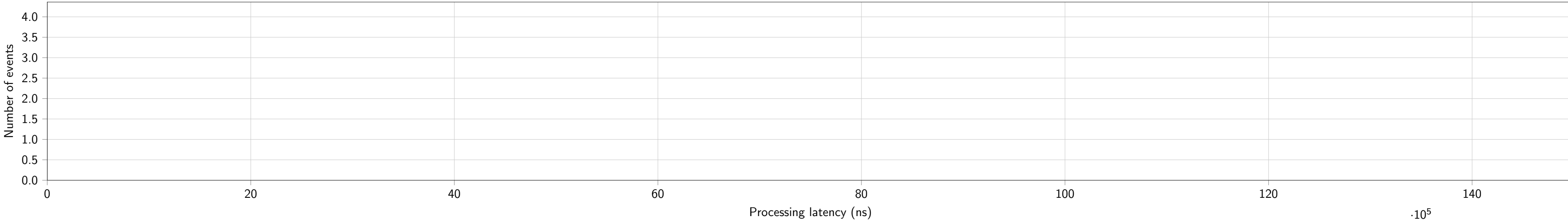
l2_bridging_cnf5_mbit4795hires.histogram.csv: tx: 9.39mpps, 0.05stdDev; rx: 9.37mpps, 0.00stdDev



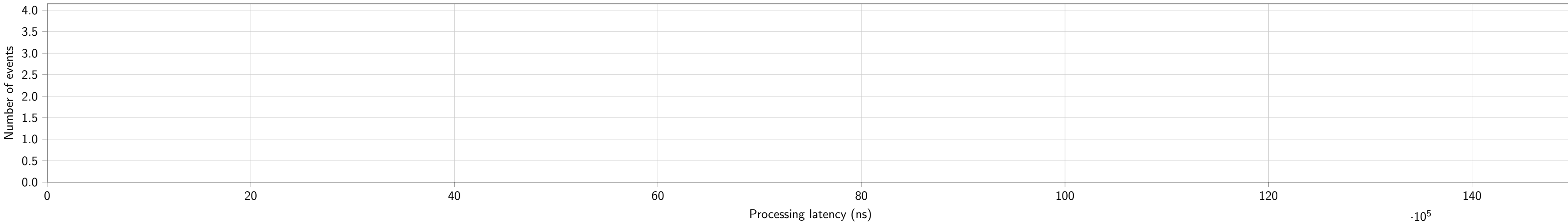
l2_bridging_cnf5_mbit4800.histogram.csv: tx: 9.39mpps, 0.05stdDev; rx: 9.37mpps, 0.00stdDev



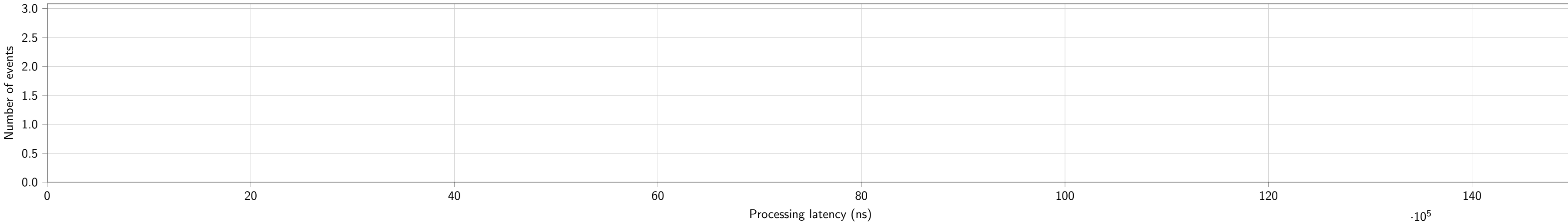
l2_bridging_cnf5_mbit4805hires.histogram.csv: tx: 9.39mpps, 0.04stdDev; rx: 9.36mpps, 0.00stdDev



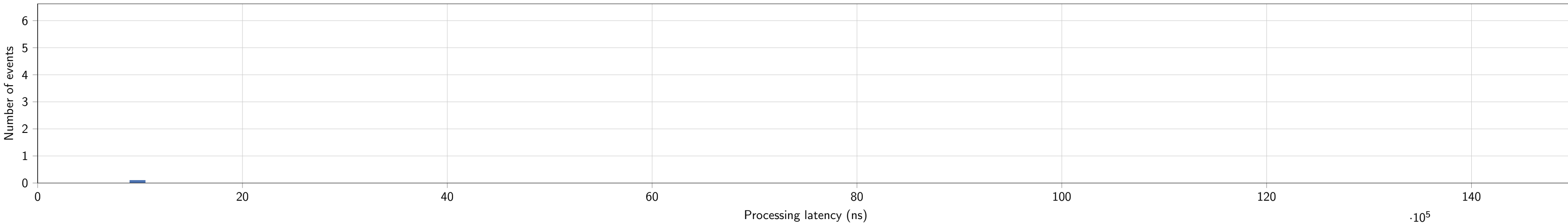
l2_bridging_cnf5_mbit4815hires.histogram.csv: tx: 9.46mpps, 0.05stdDev; rx: 9.36mpps, 0.00stdDev



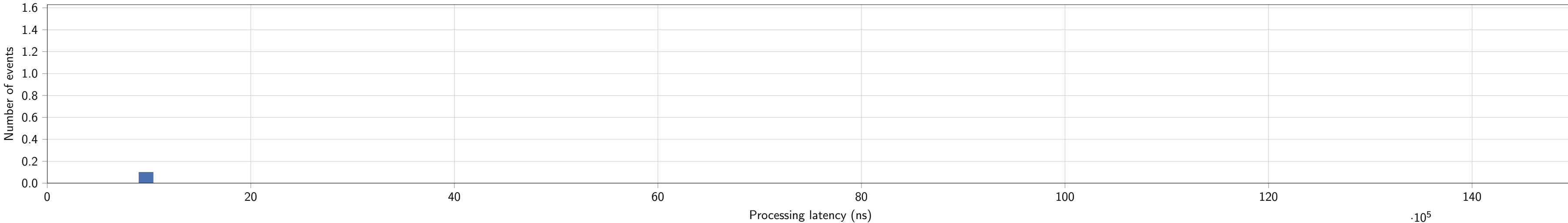
l2_bridging_cnf5_mbit4825hires.histogram.csv: tx: 9.46mpps, 0.05stdDev; rx: 9.35mpps, 0.00stdDev



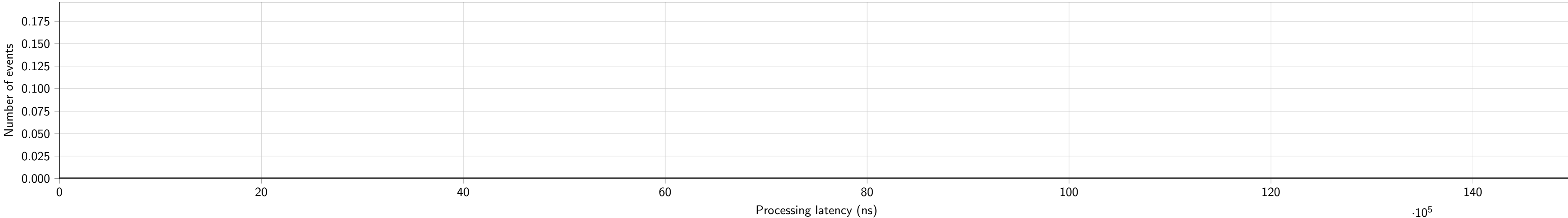
l2_bridging_cnf5_mbit4835hires.histogram.csv: tx: 9.46mpps, 0.05stdDev; rx: 9.37mpps, 0.00stdDev



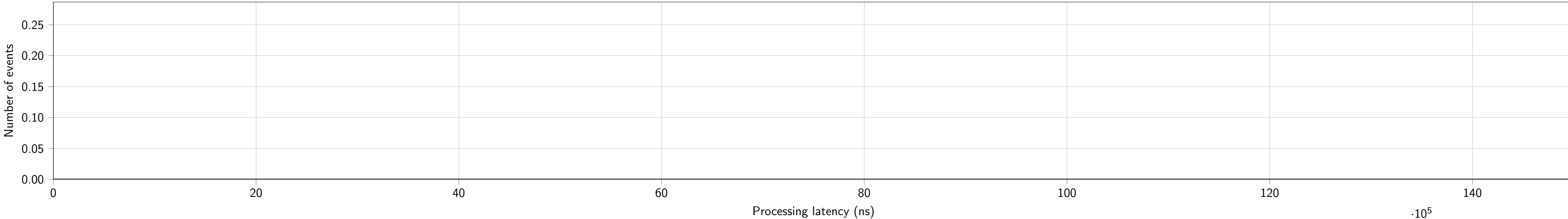
l2_bridging_cnf5_mbit5200.histogram.csv: tx: 10.15mpps, 0.05stdDev; rx: 9.37mpps, 0.00stdDev



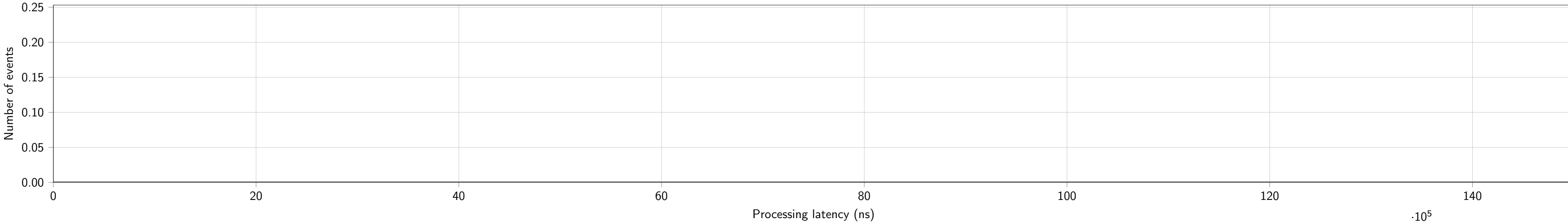
l2_bridging_cnf5_mbit5600.histogram.csv: tx: 10.95mpps, 0.05stdDev; rx: 9.33mpps, 0.00stdDev

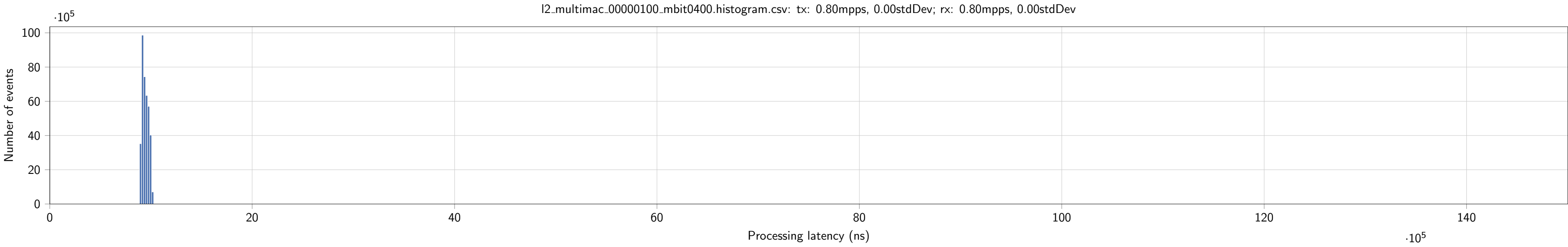


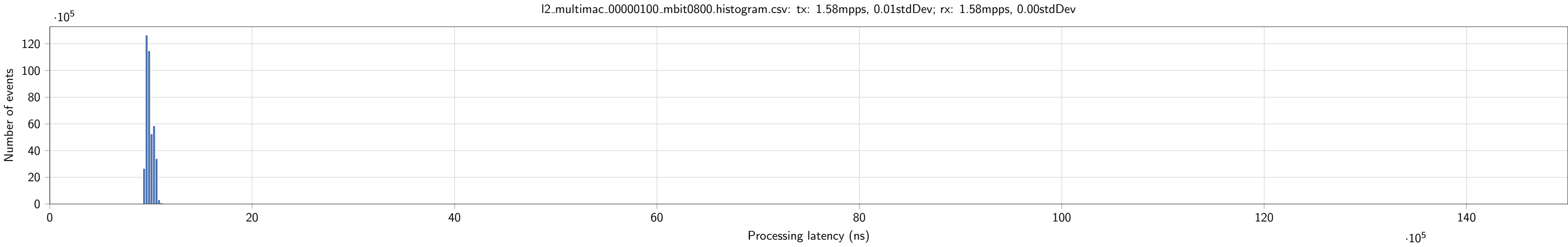
l2_bridging_cnf5_mbit6000.histogram.csv: tx: 11.78mpps, 0.06stdDev; rx: 9.36mpps, 0.00stdDev

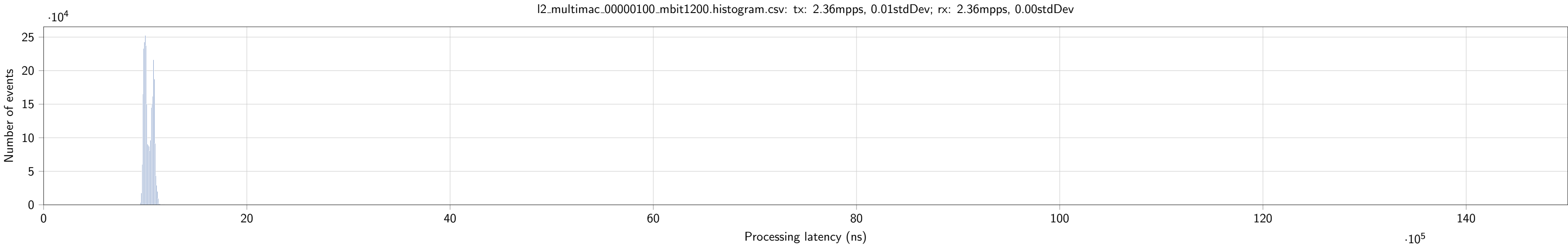


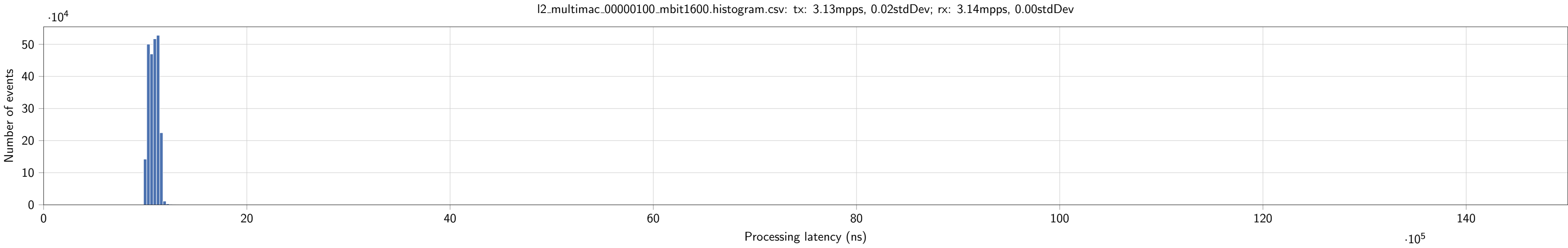
l2_bridging_cnf5_mbit9000.histogram.csv: tx: 14.86mpps, 0.07stdDev; rx: 9.35mpps, 0.00stdDev

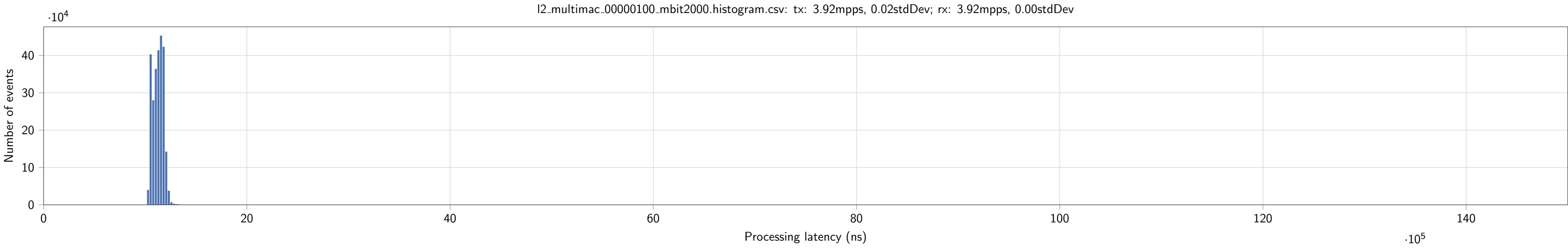


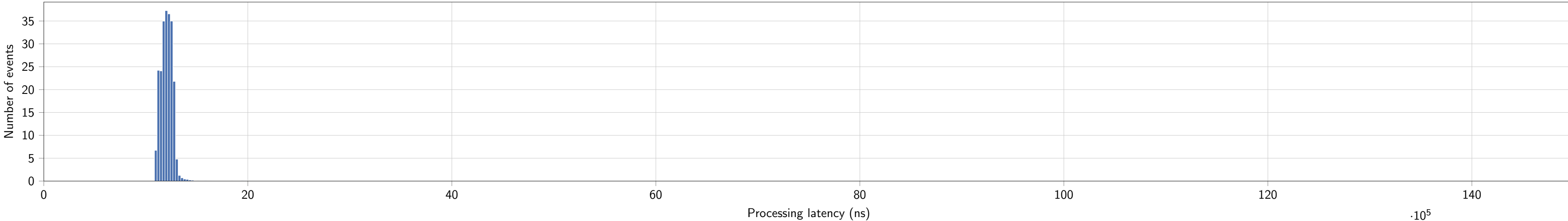












l2_multimac_00000100_mbit2800.histogram.csv: tx: 5.48mpps, 0.04stdDev; rx: 5.49mpps, 0.00stdDev

Number of events

20.0
17.5
15.0
12.5
10.0
7.5
5.0
2.5
0.0

$\cdot 10^4$

0

20

40

60

80

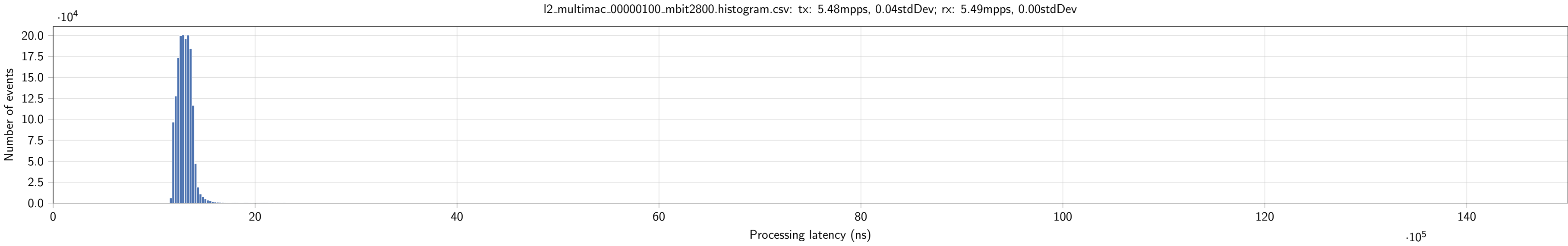
100

120

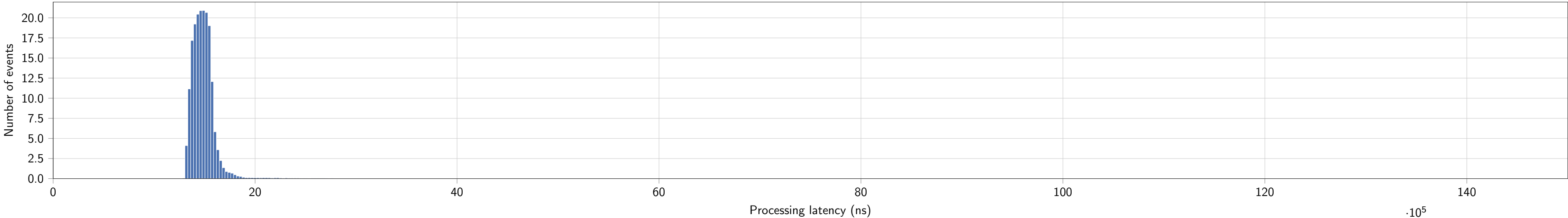
140

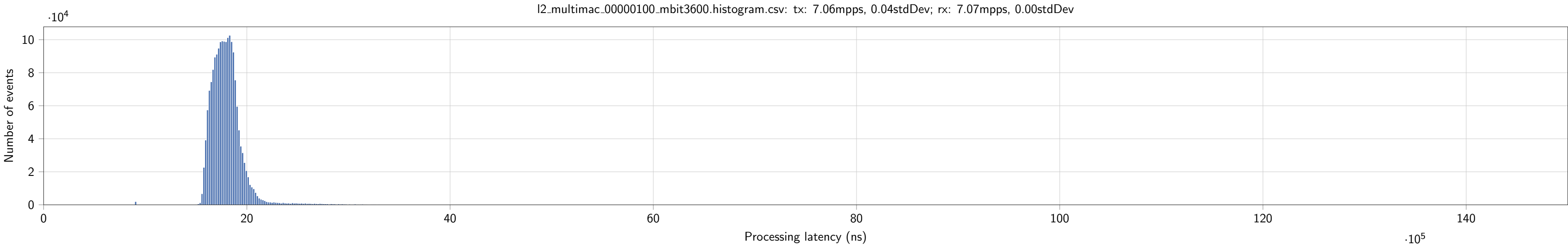
Processing latency (ns)

$\cdot 10^5$

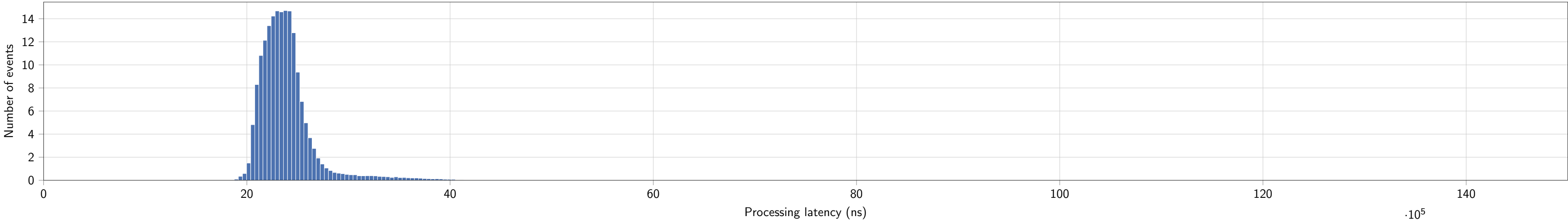


l2_multimac_00000100_mbit3200.histogram.csv: tx: 6.25mpps, 0.04stdDev; rx: 6.26mpps, 0.00stdDev

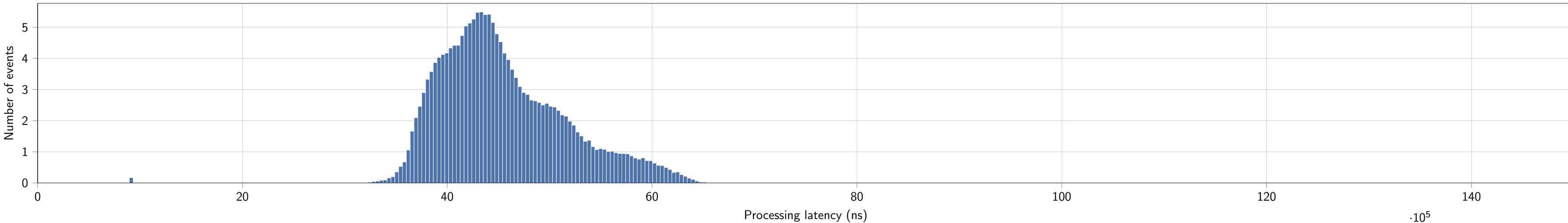




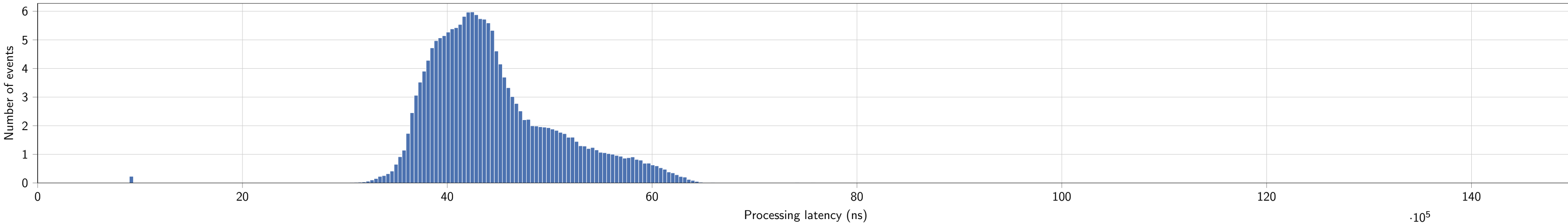
l2_multimac_00000100_mbit4000.histogram.csv: tx: 7.81mpps, 0.05stdDev; rx: 7.82mpps, 0.00stdDev



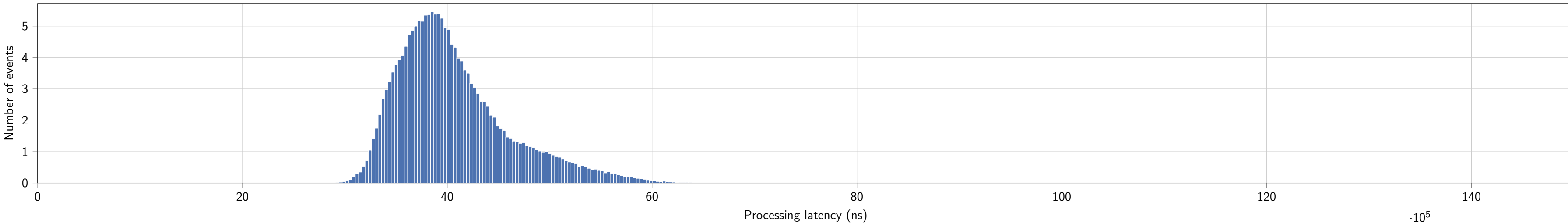
l2_multimac_00000100_mbit4270hires.histogram.csv: tx: 8.39mpps, 0.05stdDev; rx: 8.40mpps, 0.00stdDev



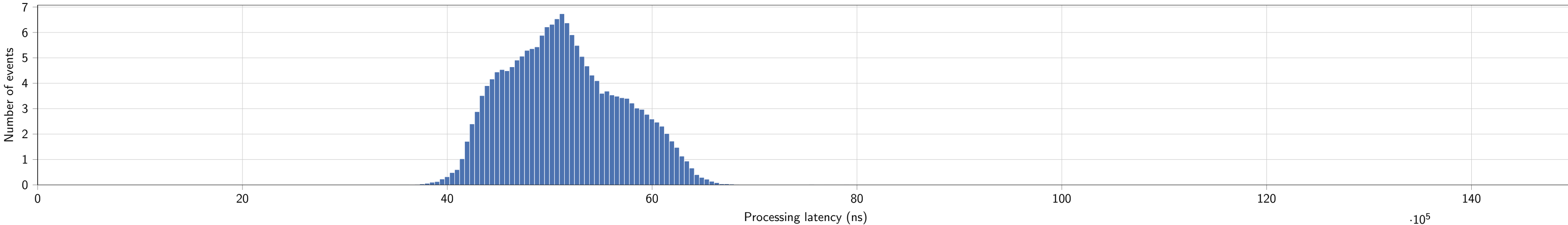
l2_multimac_00000100_mbit4280hires.histogram.csv: tx: 8.39mpps, 0.05stdDev; rx: 8.40mpps, 0.00stdDev



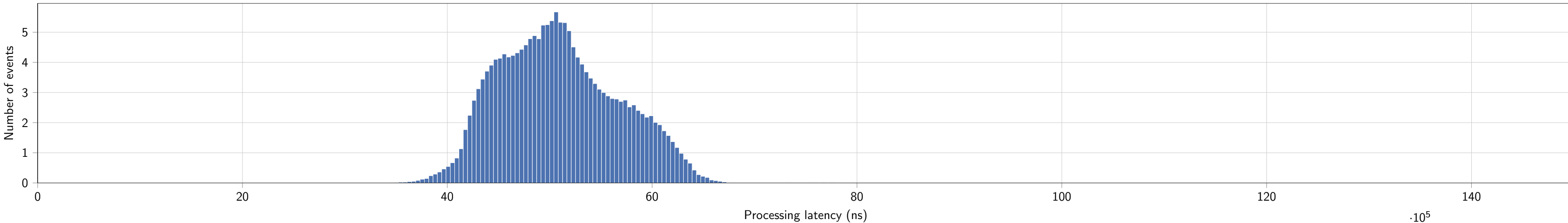
l2_multimac_00000100_mbit4290hires.histogram.csv: tx: 8.39mpps, 0.05stdDev; rx: 8.40mpps, 0.00stdDev



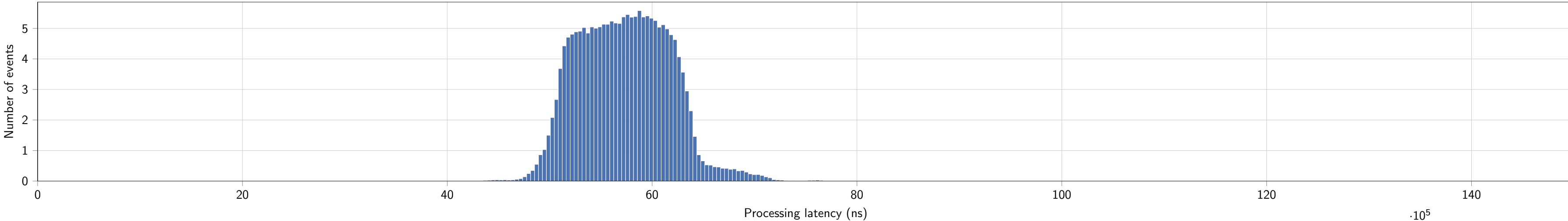
l2_multimac_00000100_mbit4300hires.histogram.csv: tx: 8.44mpps, 0.05stdDev; rx: 8.45mpps, 0.00stdDev



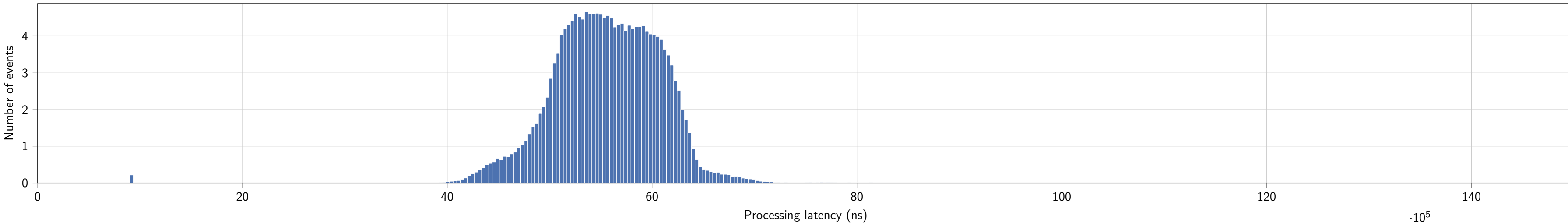
l2_multimac_00000100_mbit4310hires.histogram.csv: tx: 8.44mpps, 0.05stdDev; rx: 8.45mpps, 0.00stdDev



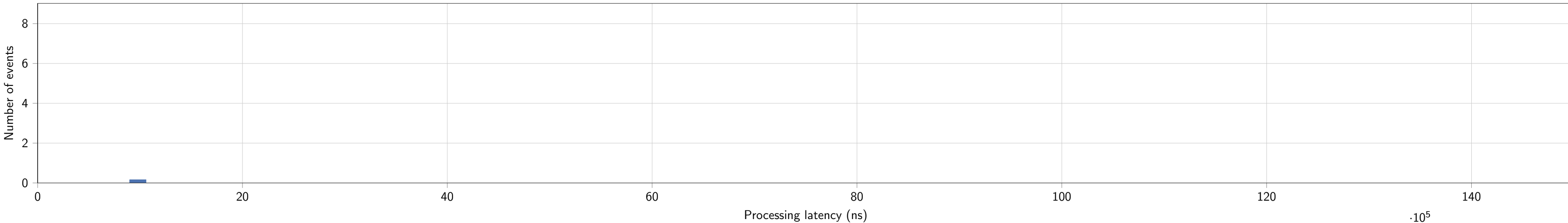
l2_multimac_00000100_mbit4320_final.histogram.csv: tx: 8.44mpps, 0.05stdDev; rx: 8.45mpps, 0.00stdDev



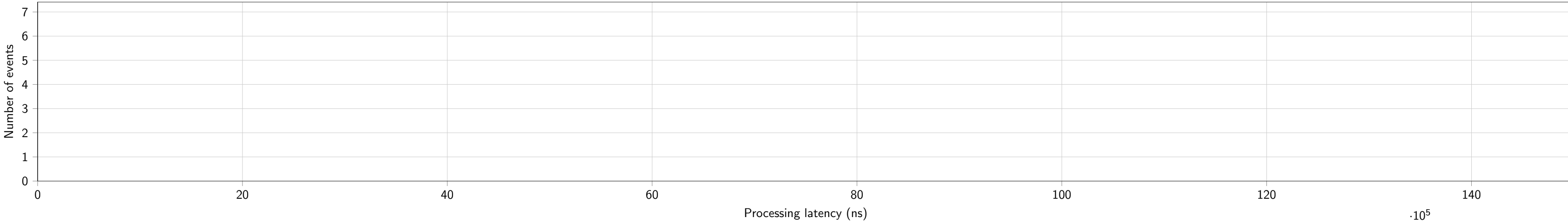
l2_multimac_00000100_mbit4320hires.histogram.csv: tx: 8.44mpps, 0.05stdDev; rx: 8.45mpps, 0.00stdDev



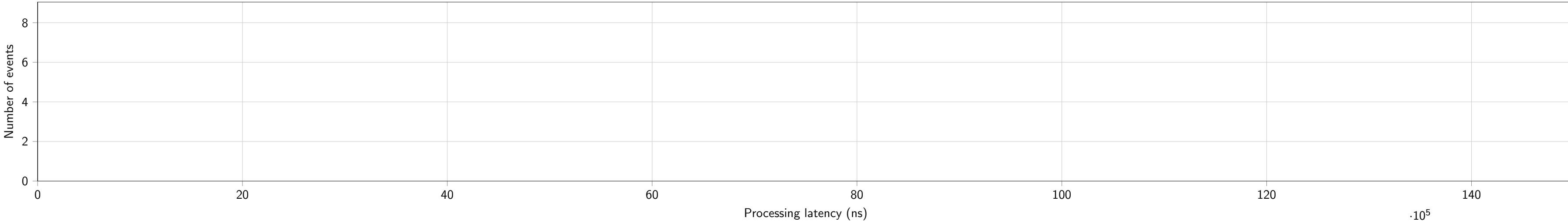
l2_multimac_00000100_mbit4330hires.histogram.csv: tx: 8.49mpps, 0.05stdDev; rx: 8.48mpps, 0.00stdDev



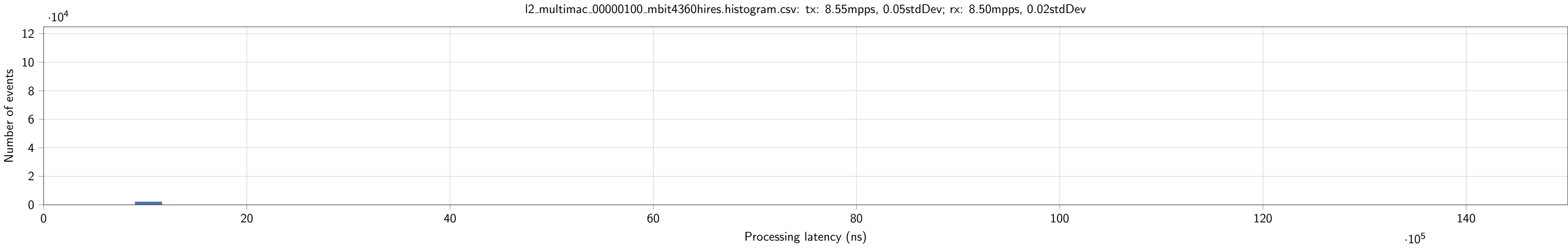
l2_multimac_00000100_mbit4340hires.histogram.csv: tx: 8.49mpps, 0.05stdDev; rx: 8.45mpps, 0.00stdDev

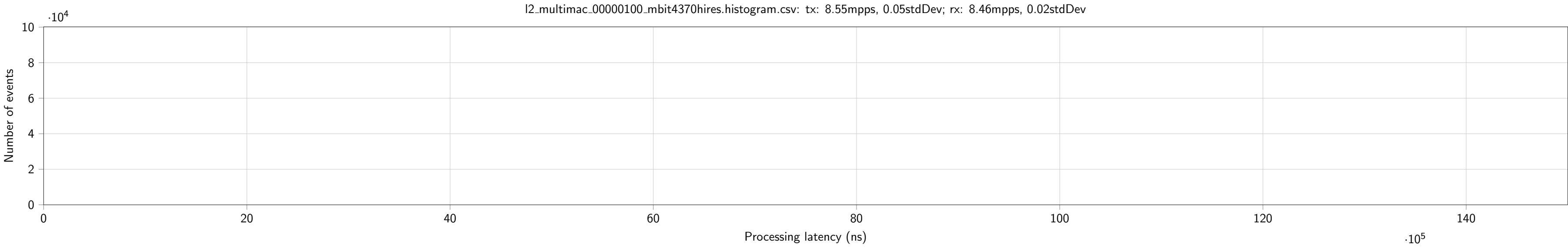


l2_multimac_00000100_mbit4350hires.histogram.csv: tx: 8.49mpps, 0.05stdDev; rx: 8.47mpps, 0.00stdDev

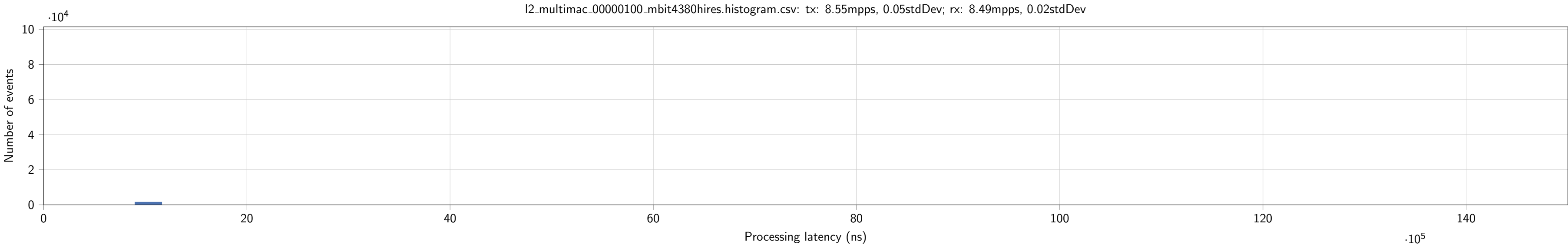


l2_multimac_00000100_mbit4360hires.histogram.csv: tx: 8.55mpps, 0.05stdDev; rx: 8.50mpps, 0.02stdDev

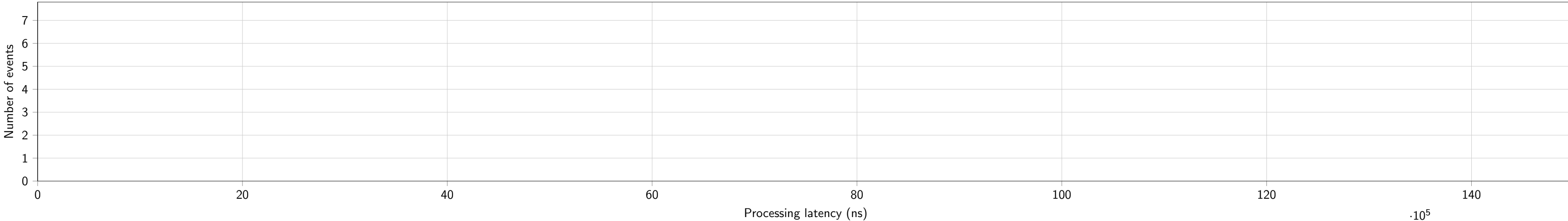




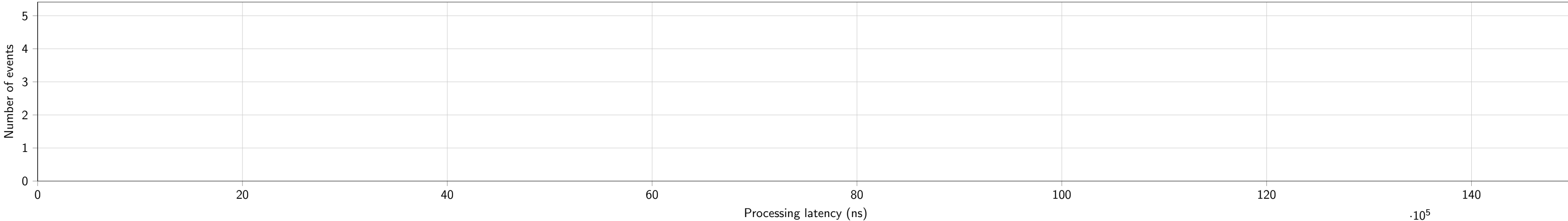
l2_multimac_00000100_mbit4380hires.histogram.csv: tx: 8.55mpps, 0.05stdDev; rx: 8.49mpps, 0.02stdDev



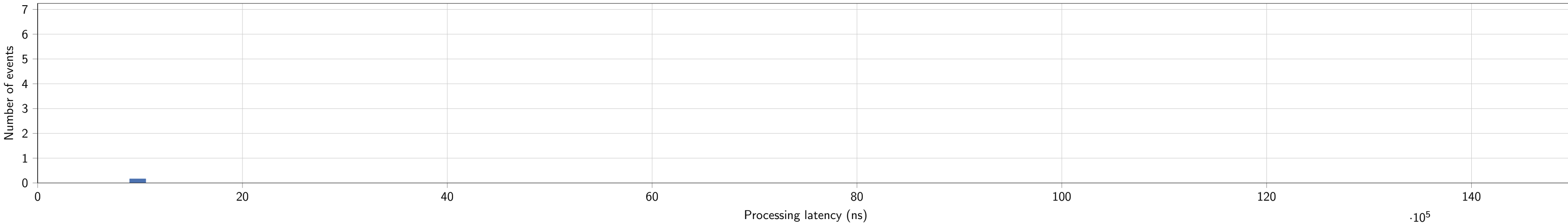
l2_multimac_00000100_mbit4390hires.histogram.csv: tx: 8.61mpps, 0.05stdDev; rx: 8.48mpps, 0.02stdDev



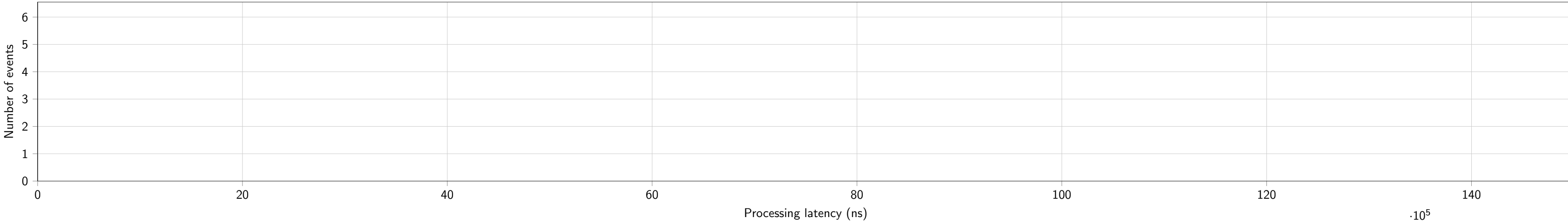
l2_multimac_00000100_mbit4400.histogram.csv: tx: 8.61mpps, 0.05stdDev; rx: 8.50mpps, 0.00stdDev



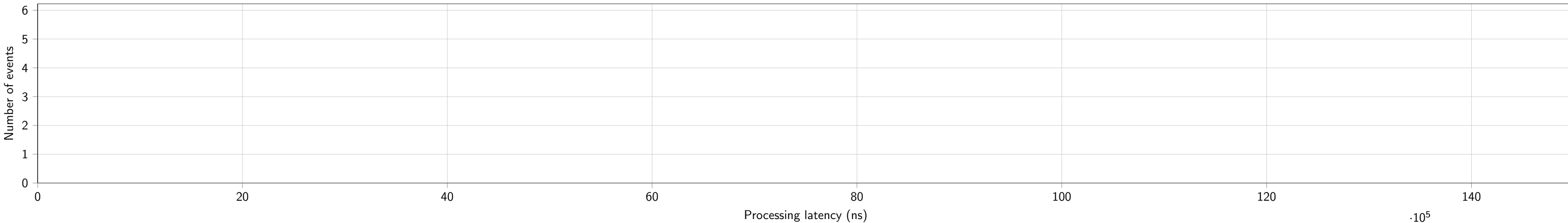
l2_multimac_00000100_mbit4400hires.histogram.csv: tx: 8.61mpps, 0.05stdDev; rx: 8.51mpps, 0.00stdDev



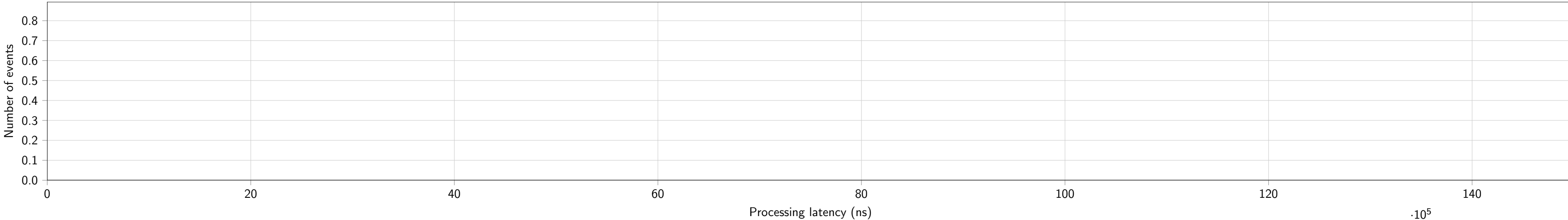
l2_multimac_00000100_mbit4410hires.histogram.csv: tx: 8.61mpps, 0.05stdDev; rx: 8.55mpps, 0.00stdDev



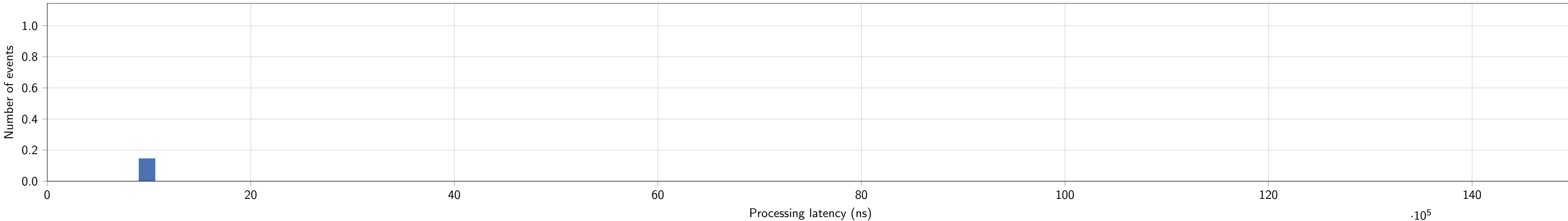
l2_multimac_00000100_mbit4420hires.histogram.csv: tx: 8.67mpps, 0.05stdDev; rx: 8.52mpps, 0.00stdDev



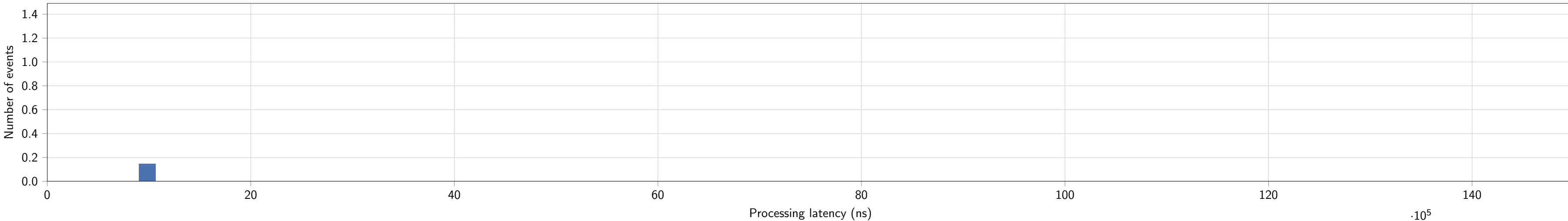
l2_multimac_00000100_mbit4800.histogram.csv: tx: 9.24mpps, 0.05stdDev; rx: 8.52mpps, 0.00stdDev



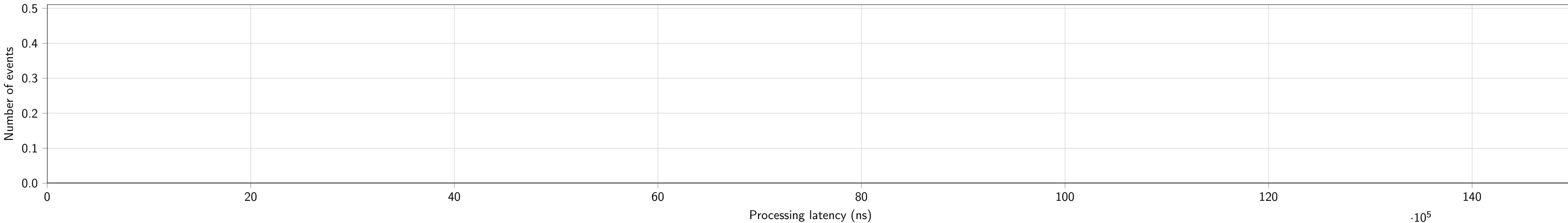
l2_multimac_00000100_mbit5200.histogram.csv: tx: 9.25mpps, 0.05stdDev; rx: 8.52mpps, 0.00stdDev



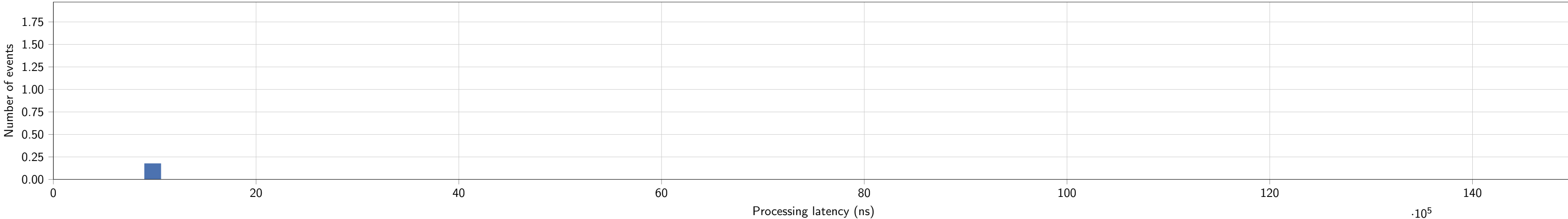
l2_multimac_00000100_mbit5600.histogram.csv: tx: 9.24mpps, 0.05stdDev; rx: 8.54mpps, 0.00stdDev

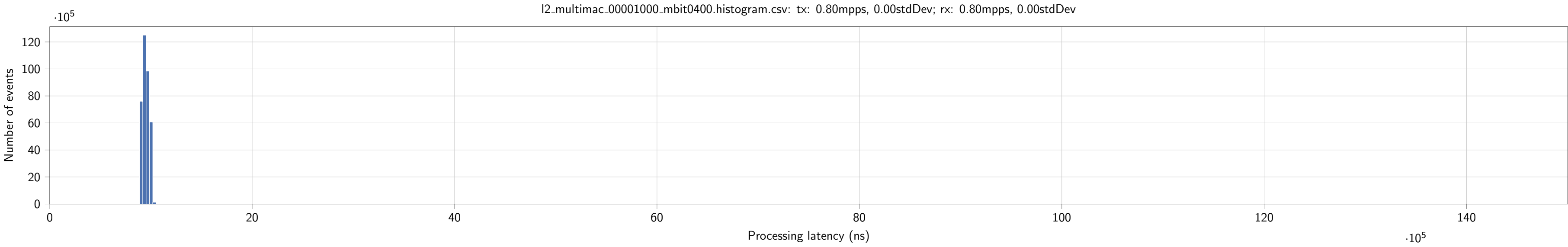


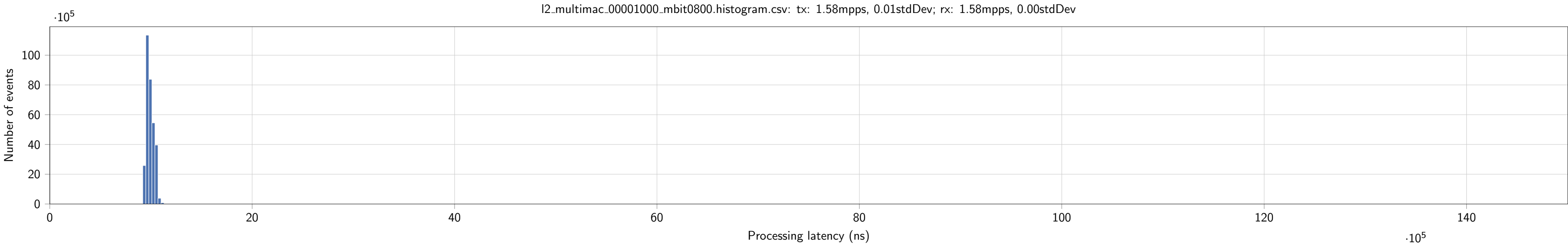
l2_multimac_00000100_mbit6000.histogram.csv: tx: 9.20mpps, 0.05stdDev; rx: 8.55mpps, 0.00stdDev

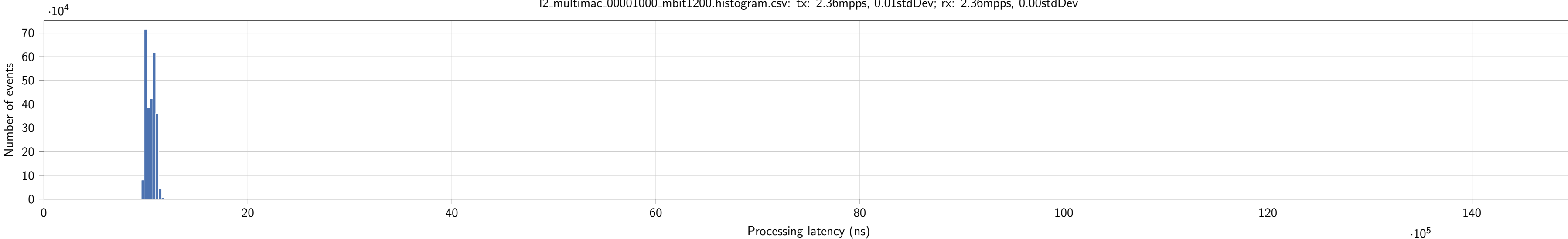


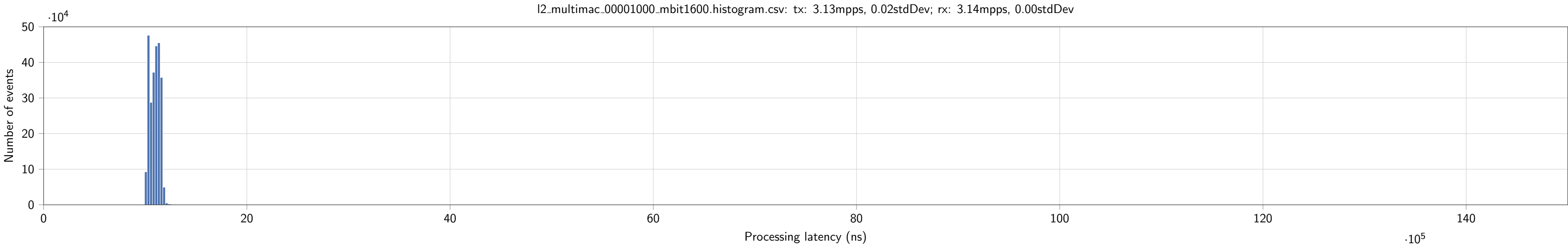
l2_multimac_00000100_mbit9000.histogram.csv: tx: 9.22mpps, 0.05stdDev; rx: 8.53mpps, 0.00stdDev



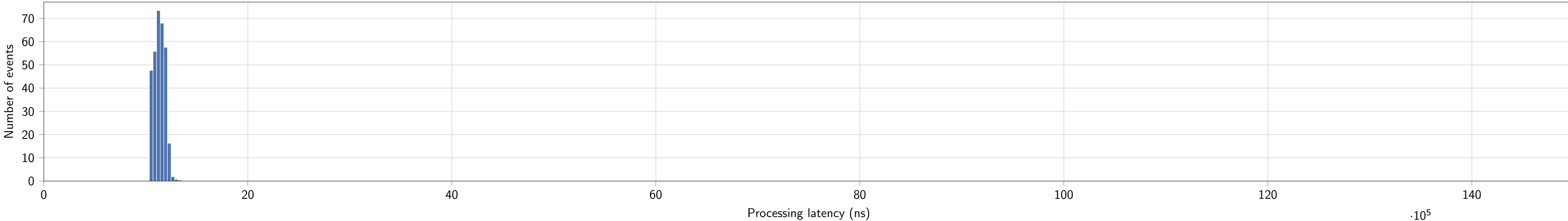








l2_multimac_00001000_mbit2000.histogram.csv: tx: 3.92mpps, 0.02stdDev; rx: 3.92mpps, 0.00stdDev



l2_multimac_00001000_mbit2400.histogram.csv: tx: 4.71mpps, 0.03stdDev; rx: 4.71mpps, 0.00stdDev

Number of events

$\cdot 10^4$

60

50

40

30

20

10

0

20

40

60

80

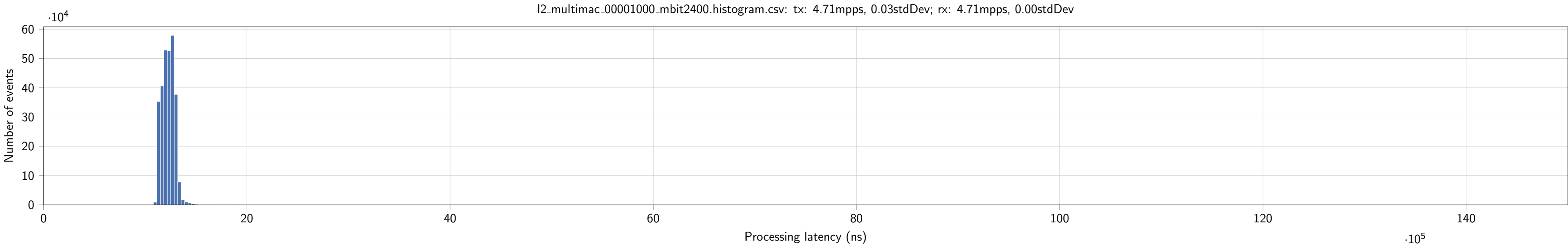
100

120

140

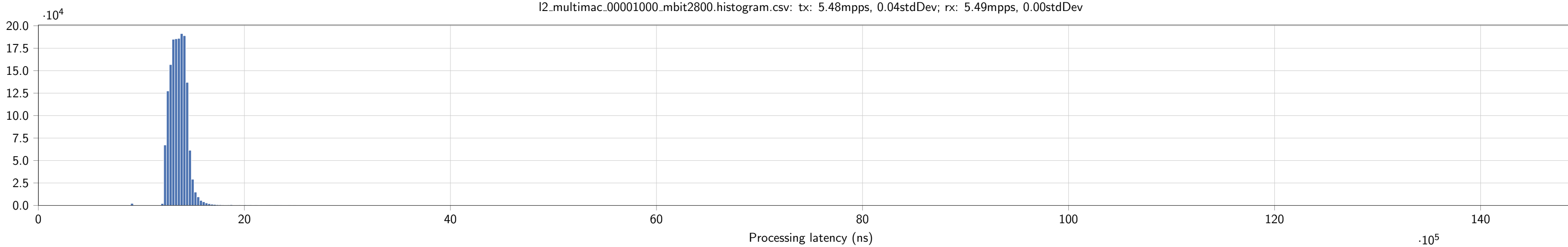
Processing latency (ns)

$\cdot 10^5$



l2_multimac_00001000_mbit2800.histogram.csv: tx: 5.48mpps, 0.04stdDev; rx: 5.49mpps, 0.00stdDev

Number of events



l2_multimac_00001000_mbit3200.histogram.csv: tx: 6.25mpps, 0.04stdDev; rx: 6.26mpps, 0.00stdDev

Number of events

20.0
17.5
15.0
12.5
10.0
7.5
5.0
2.5
0.0

0

20

40

60

80

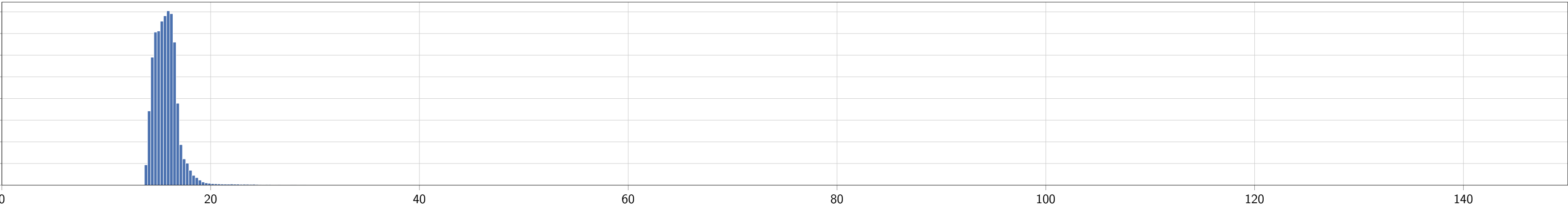
100

120

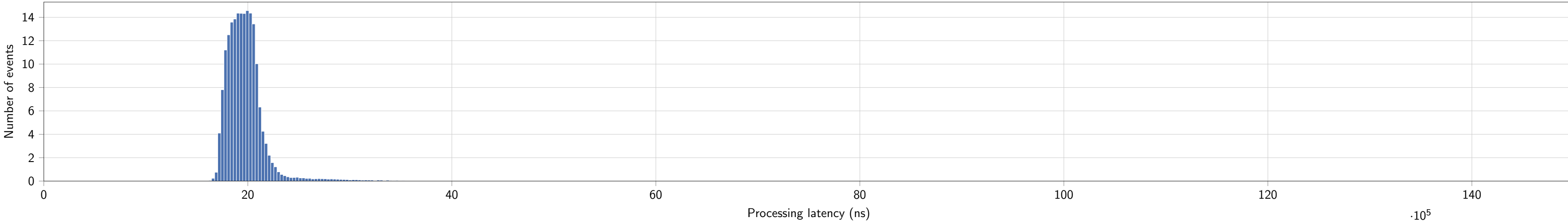
140

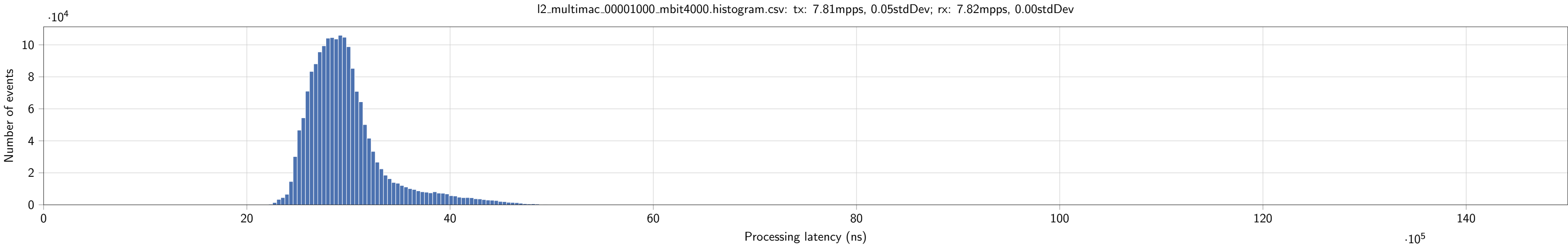
Processing latency (ns)

$\cdot 10^5$

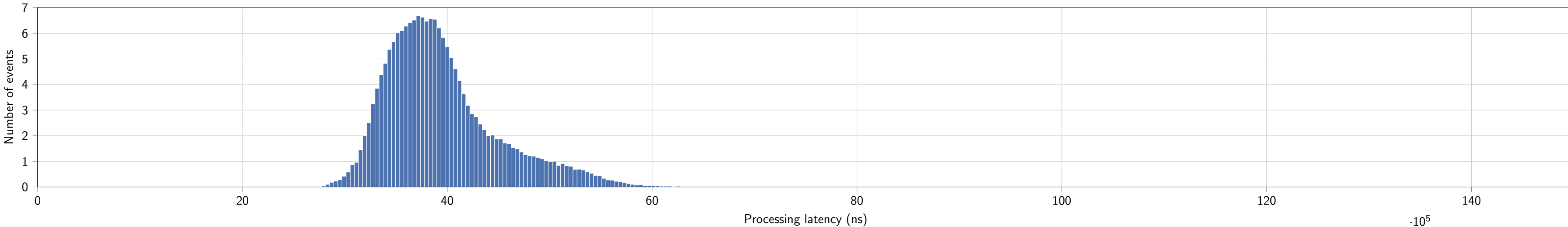


l2_multimac_00001000_mbit3600.histogram.csv: tx: 7.06mpps, 0.04stdDev; rx: 7.07mpps, 0.00stdDev

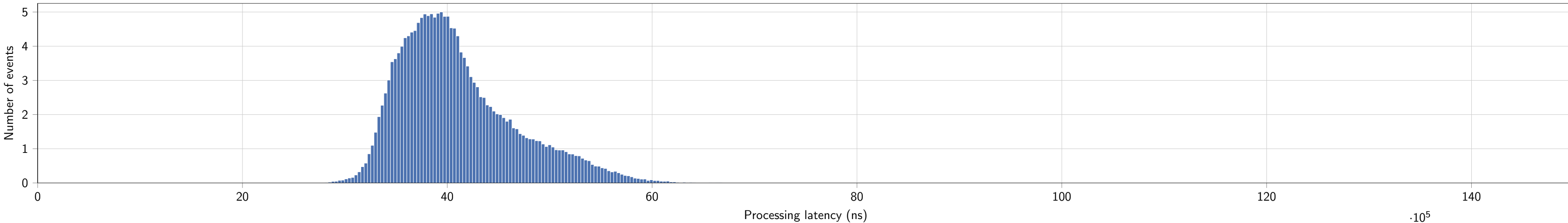




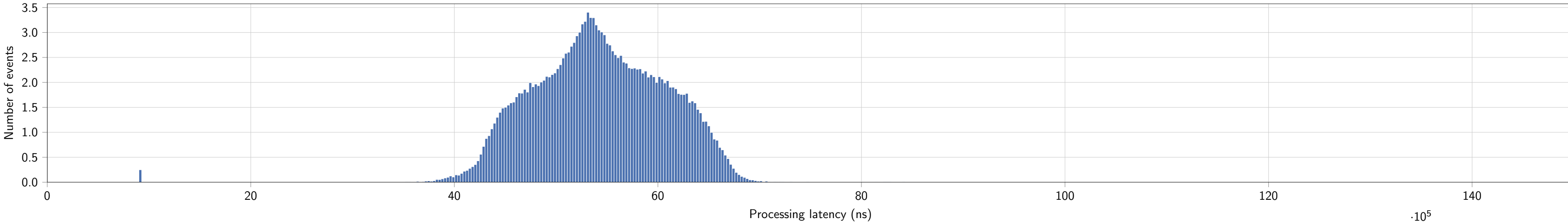
l2_multimac_00001000_mbit4071hires.histogram.csv: tx: 7.96mpps, 0.05stdDev; rx: 7.97mpps, 0.00stdDev



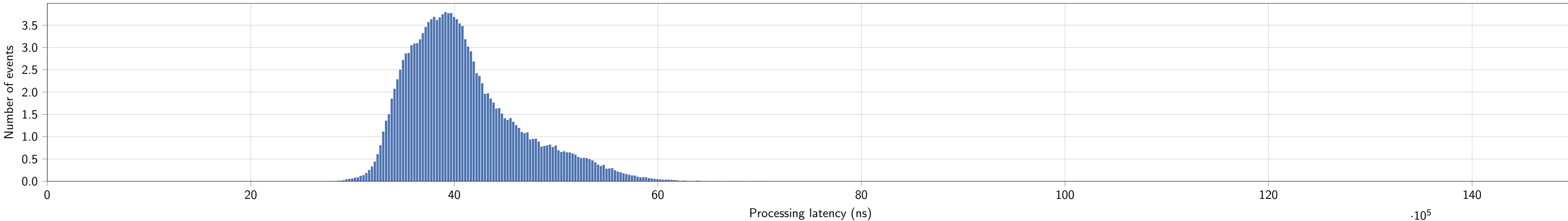
l2_multimac_00001000_mbit4081hires.histogram.csv: tx: 8.01mpps, 0.05stdDev; rx: 8.02mpps, 0.00stdDev



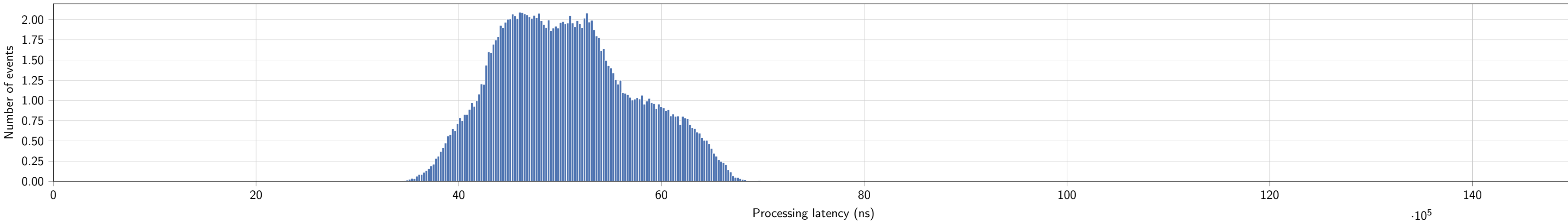
l2_multimac_00001000_mbit4091hires.histogram.csv: tx: 8.01mpps, 0.05stdDev; rx: 8.02mpps, 0.00stdDev



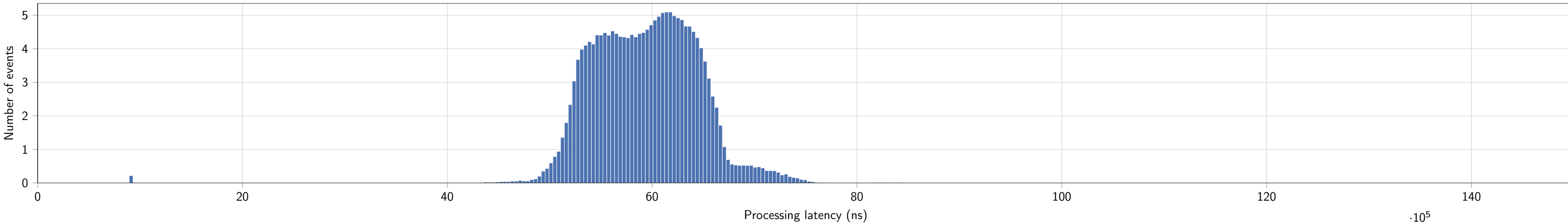
l2_multimac_00001000_mbit4101hires.histogram.csv: tx: 8.01mpps, 0.05stdDev; rx: 8.02mpps, 0.00stdDev



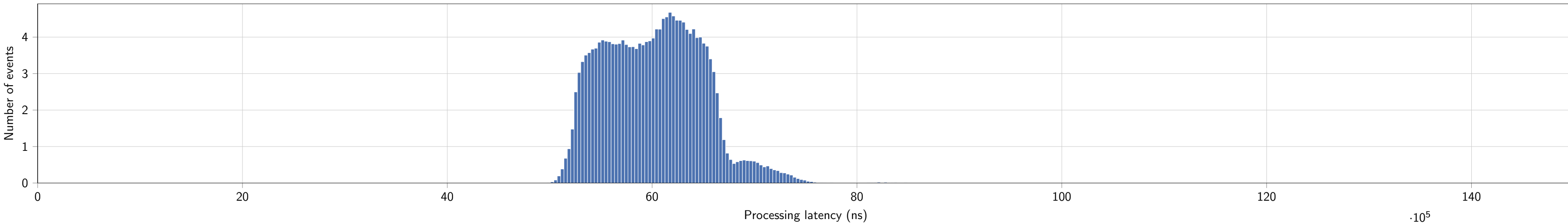
l2_multimac_00001000_mbit4111hires.histogram.csv: tx: 8.06mpps, 0.05stdDev; rx: 8.07mpps, 0.00stdDev



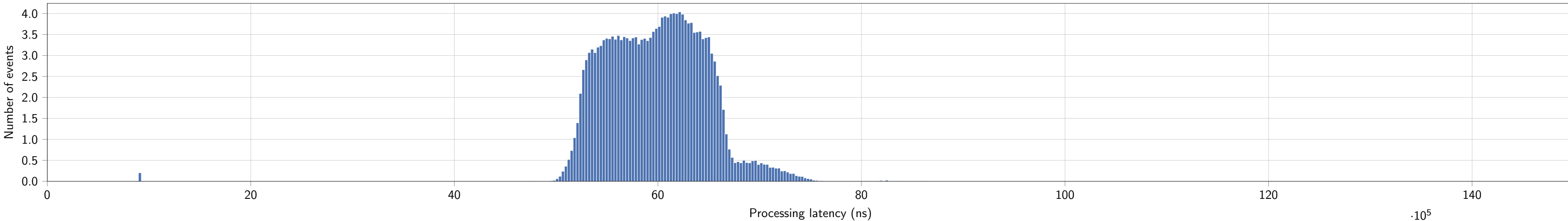
l2_multimac_00001000_mbit4121hires.histogram.csv: tx: 8.06mpps, 0.05stdDev; rx: 8.07mpps, 0.00stdDev



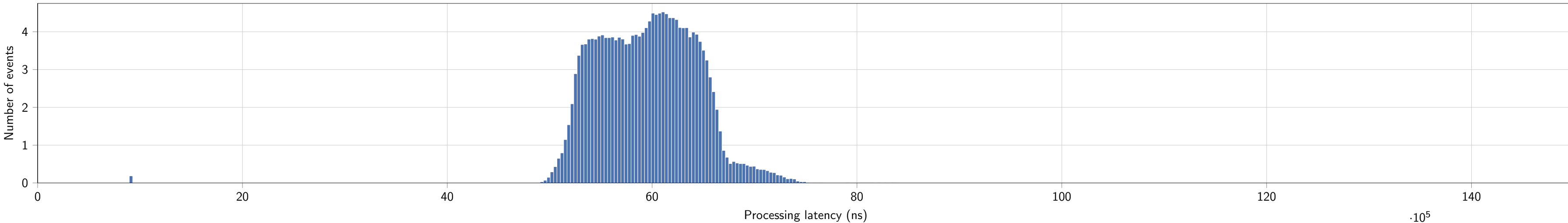
l2_multimac_00001000_mbit4131hires.histogram.csv: tx: 8.11mpps, 0.05stdDev; rx: 8.13mpps, 0.00stdDev



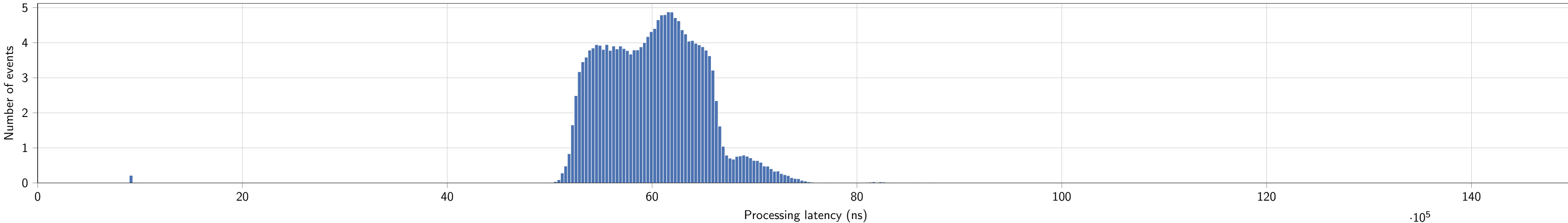
l2_multimac_00001000_mbit4141hires.histogram.csv: tx: 8.11mpps, 0.05stdDev; rx: 8.13mpps, 0.00stdDev



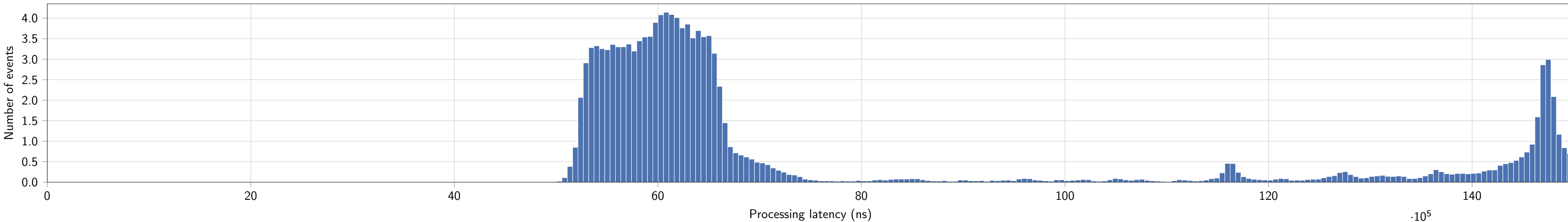
l2_multimac_00001000_mbit4151hires.histogram.csv: tx: 8.11mpps, 0.05stdDev; rx: 8.13mpps, 0.00stdDev



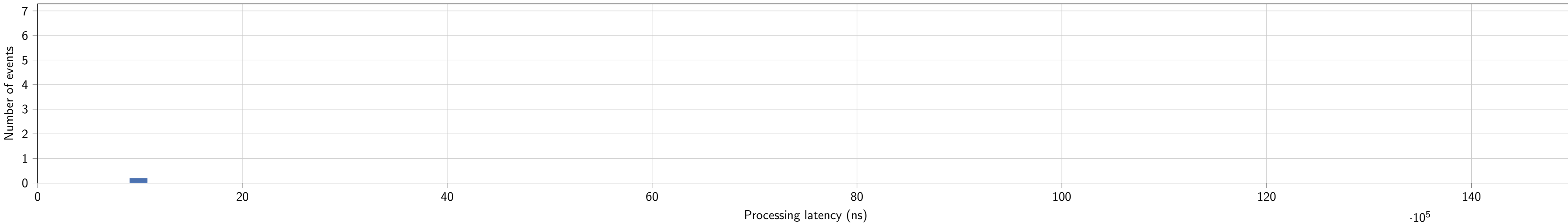
l2_multimac_00001000_mbit4161hires.histogram.csv: tx: 8.17mpps, 0.05stdDev; rx: 8.18mpps, 0.00stdDev



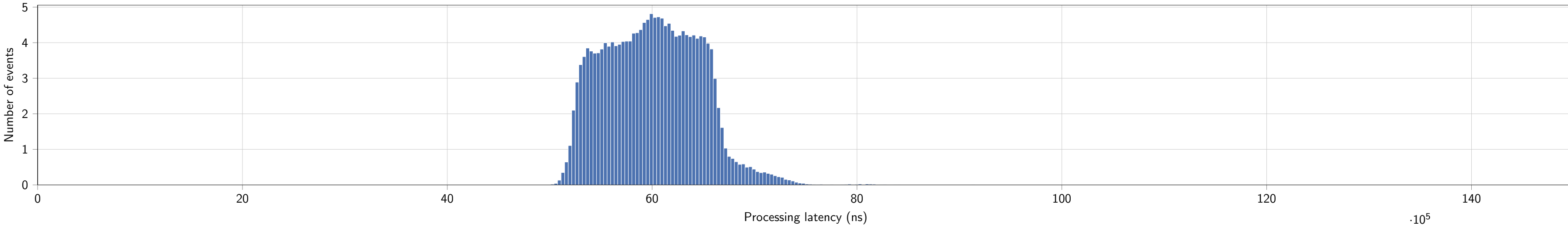
l2_multimac_00001000_mbit4171hires.histogram.csv: tx: 8.17mpps, 0.05stdDev; rx: 8.18mpps, 0.00stdDev



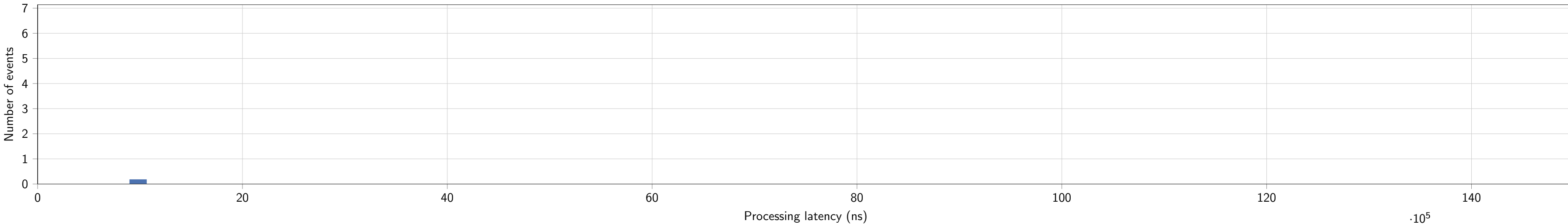
l2_multimac_00001000_mbit4181_final.histogram.csv: tx: 8.16mpps, 0.05stdDev; rx: 8.15mpps, 0.00stdDev



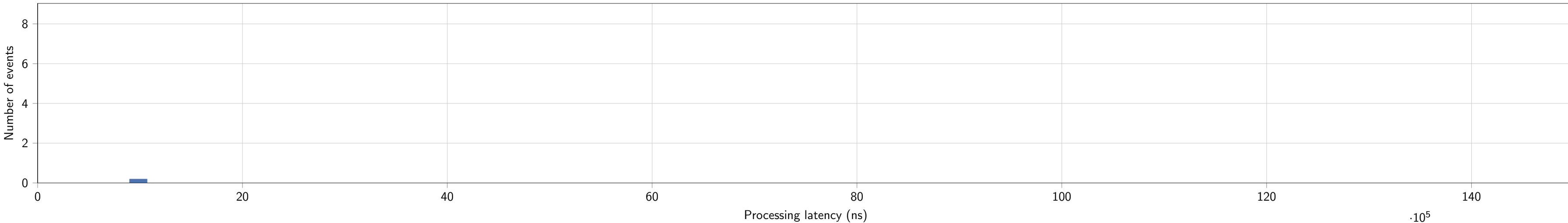
l2_multimac_00001000_mbit4181hires.histogram.csv: tx: 8.17mpps, 0.05stdDev; rx: 8.18mpps, 0.00stdDev



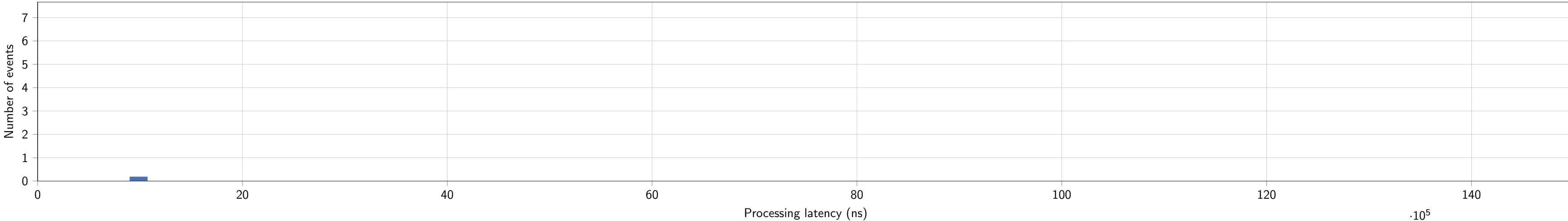
l2_multimac_00001000_mbit4191hires.histogram.csv: tx: 8.21mpps, 0.05stdDev; rx: 8.16mpps, 0.00stdDev



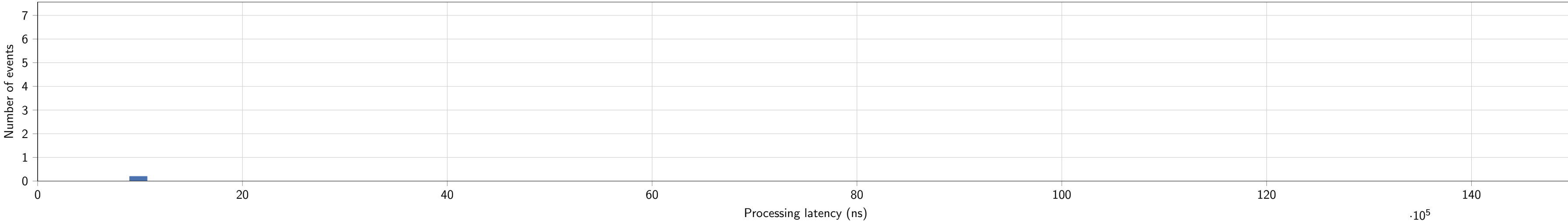
l2_multimac_00001000_mbit4201hires.histogram.csv: tx: 8.21mpps, 0.05stdDev; rx: 8.16mpps, 0.00stdDev



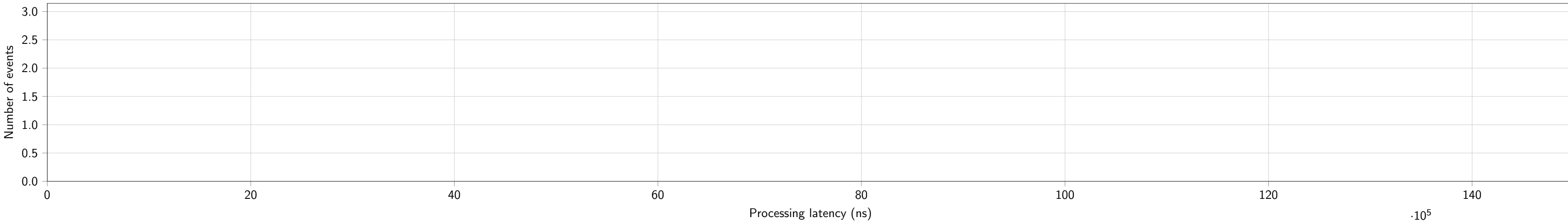
l2_multimac_00001000_mbit4211hires.histogram.csv: tx: 8.27mpps, 0.05stdDev; rx: 8.17mpps, 0.00stdDev



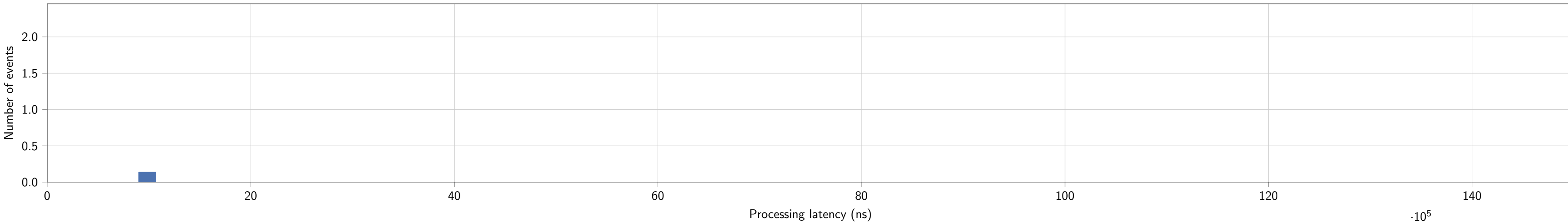
l2_multimac_00001000_mbit4221hires.histogram.csv: tx: 8.27mpps, 0.05stdDev; rx: 8.15mpps, 0.00stdDev



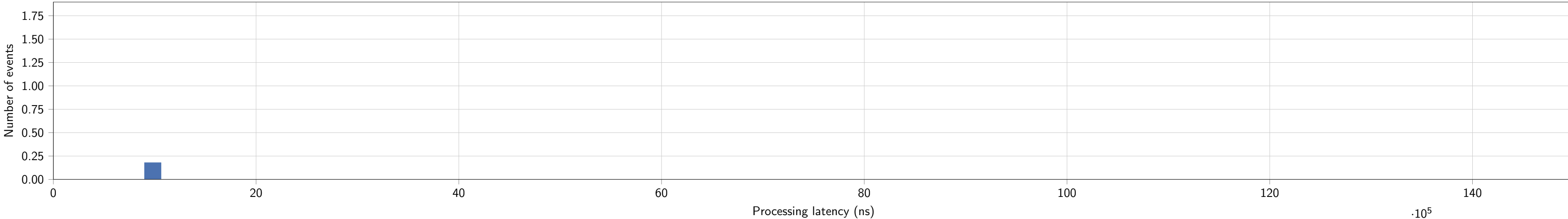
l2_multimac_00001000_mbit4400.histogram.csv: tx: 8.61mpps, 0.05stdDev; rx: 8.15mpps, 0.00stdDev



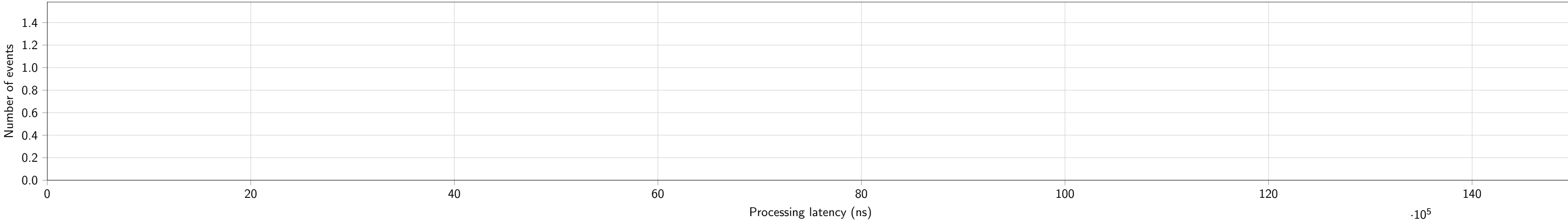
l2_multimac_00001000_mbit4800.histogram.csv: tx: 9.23mpps, 0.05stdDev; rx: 8.17mpps, 0.00stdDev



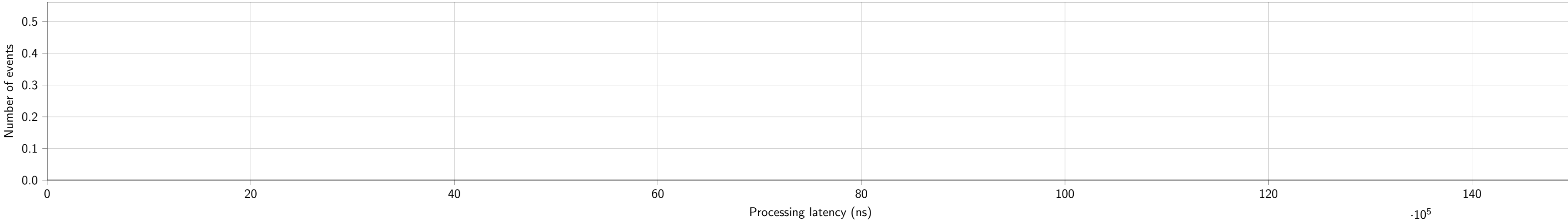
l2_multimac_00001000_mbit5200.histogram.csv: tx: 9.19mpps, 0.05stdDev; rx: 8.15mpps, 0.00stdDev



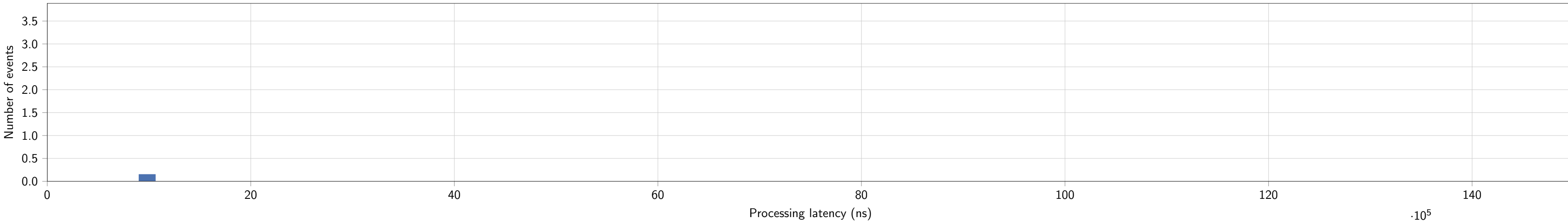
l2_multimac_00001000_mbit5600.histogram.csv: tx: 9.23mpps, 0.06stdDev; rx: 8.14mpps, 0.00stdDev



l2_multimac_00001000_mbit6000.histogram.csv: tx: 9.23mpps, 0.05stdDev; rx: 8.14mpps, 0.00stdDev



l2_multimac_00001000_mbit9000.histogram.csv: tx: 9.21mpps, 0.05stdDev; rx: 8.15mpps, 0.00stdDev



Number of events

70
60
50
40
30
20
10
0

0

20

40

60

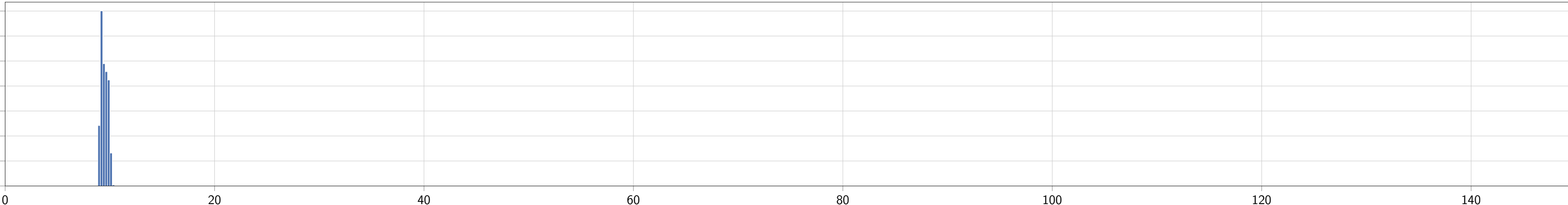
80

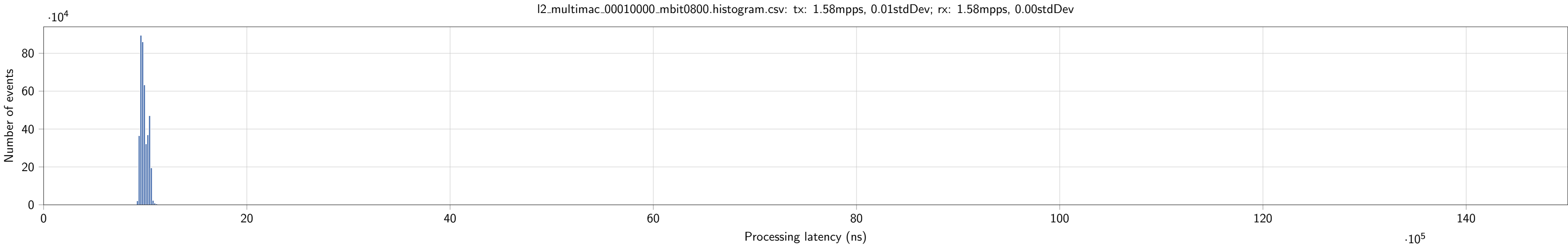
100

120

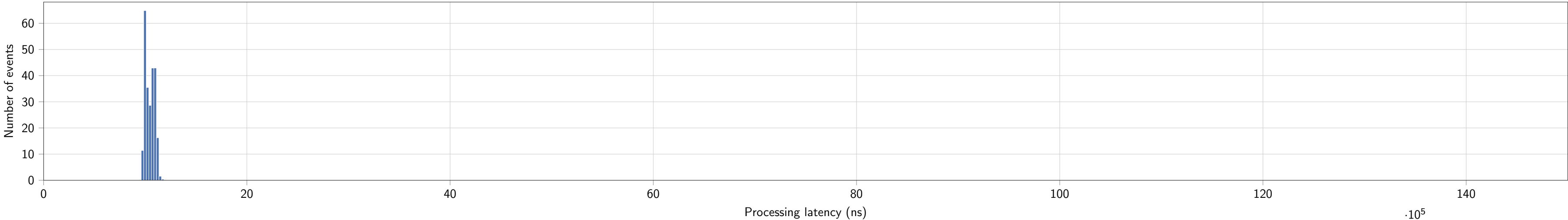
140

Processing latency (ns)

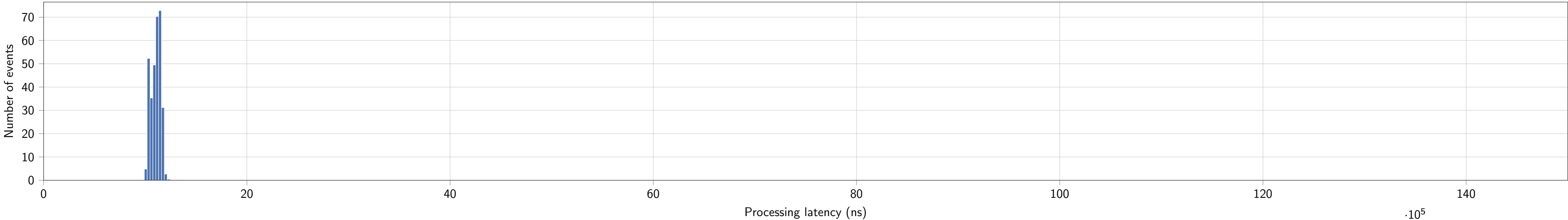
 $\cdot 10^5$ $\cdot 10^4$ 



l2_multimac_00010000_mbit1200.histogram.csv: tx: 2.35mpps, 0.01stdDev; rx: 2.36mpps, 0.00stdDev

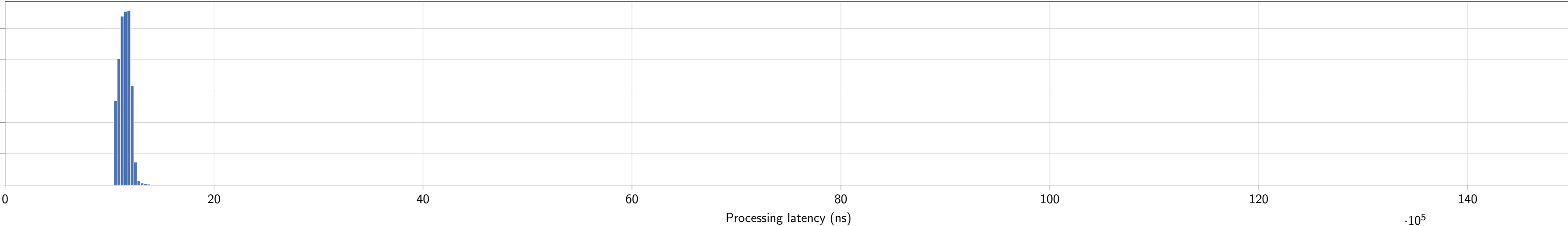


l2_multimac_00010000_mbit1600.histogram.csv: tx: 3.14mpps, 0.02stdDev; rx: 3.14mpps, 0.00stdDev



l2_multimac_00010000_mbit2000.histogram.csv: tx: 3.92mpps, 0.02stdDev; rx: 3.92mpps, 0.00stdDev

Number of events



l2_multimac_00010000_mbit2400.histogram.csv: tx: 4.71mpps, 0.03stdDev; rx: 4.71mpps, 0.00stdDev

Number of events

35
30
25
20
15
10
5
0

$\cdot 10^4$

20

40

60

80

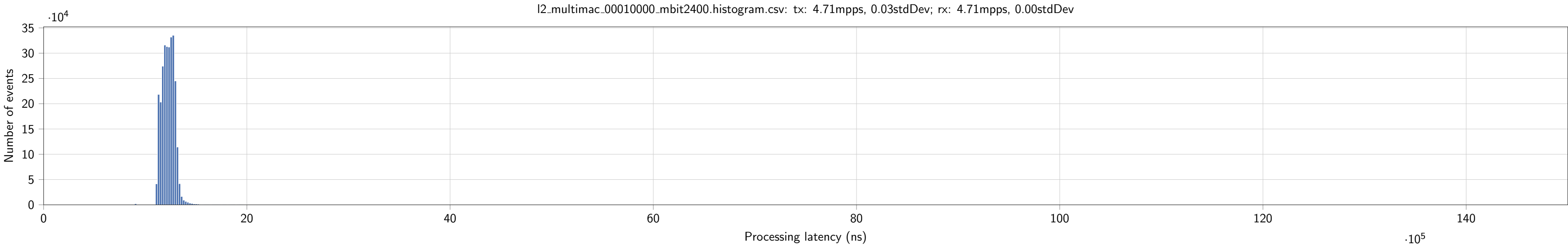
100

120

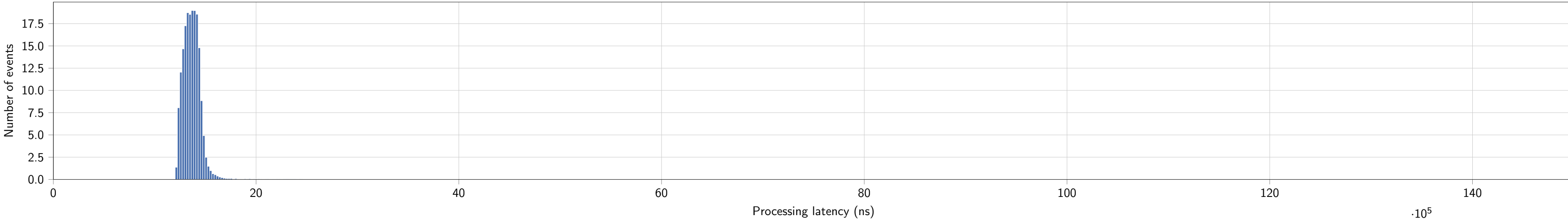
140

Processing latency (ns)

$\cdot 10^5$

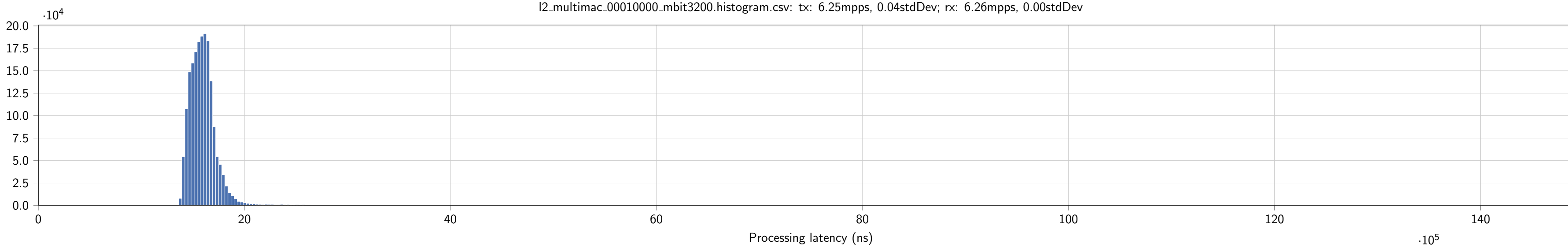


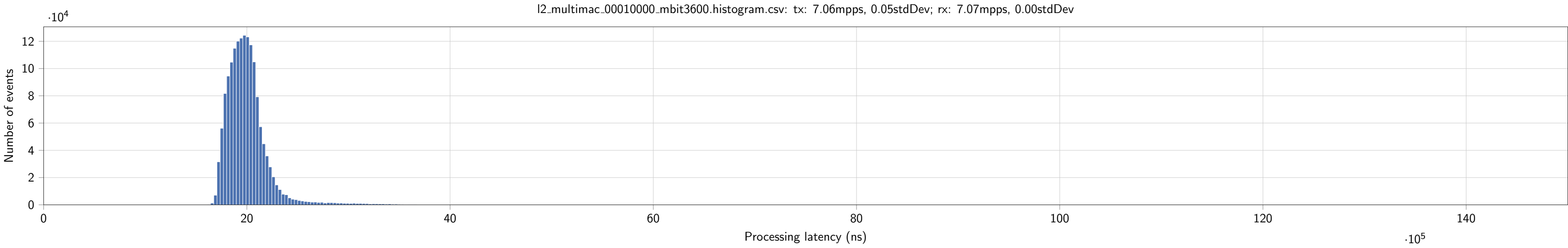
l2_multimac_00010000_mbit2800.histogram.csv: tx: 5.48mpps, 0.03stdDev; rx: 5.49mpps, 0.00stdDev



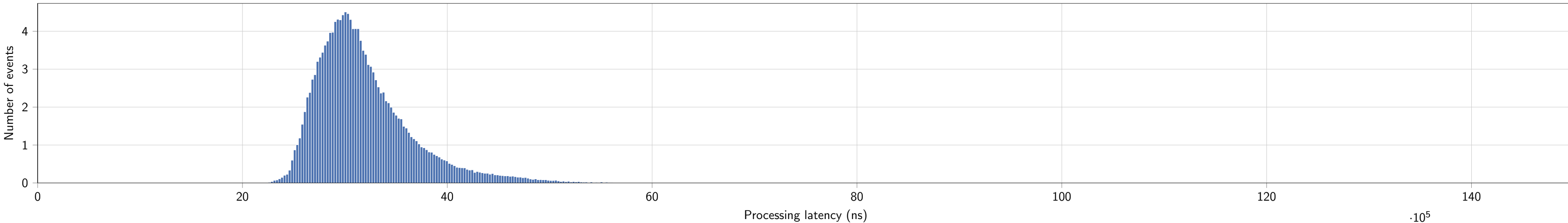
l2_multimac_00010000_mbit3200.histogram.csv: tx: 6.25mpps, 0.04stdDev; rx: 6.26mpps, 0.00stdDev

Number of events

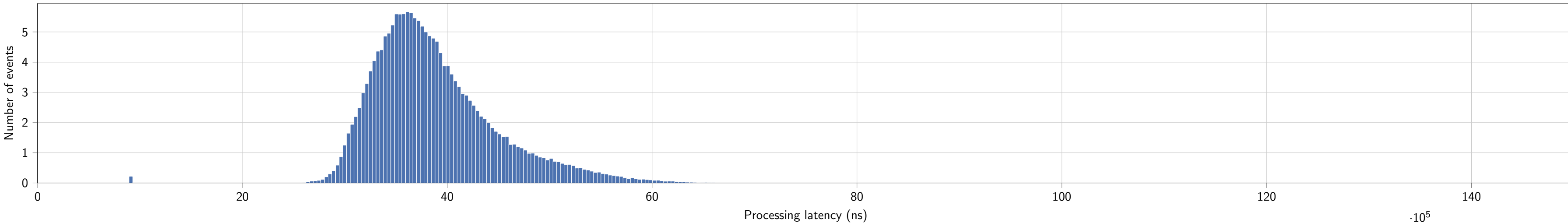




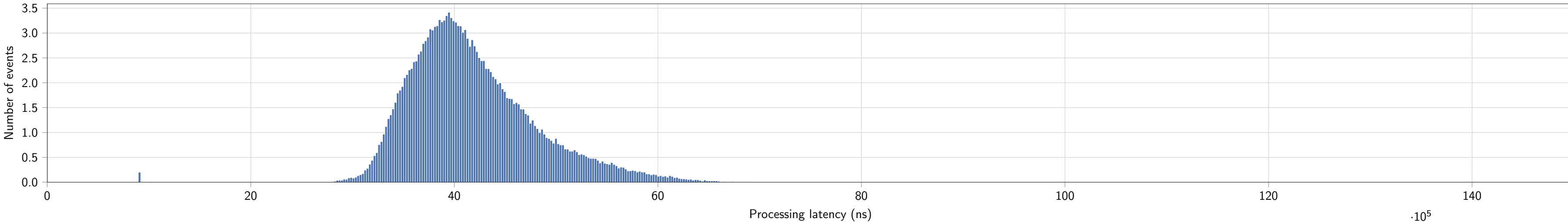
l2_multimac_00010000_mbit4000.histogram.csv: tx: 7.81mpps, 0.05stdDev; rx: 7.82mpps, 0.00stdDev



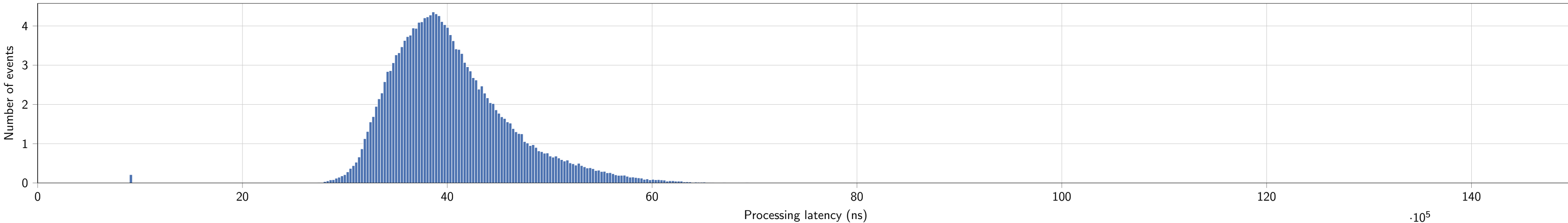
l2_multimac_00010000_mbit4050hires.histogram.csv: tx: 7.91mpps, 0.05stdDev; rx: 7.92mpps, 0.00stdDev



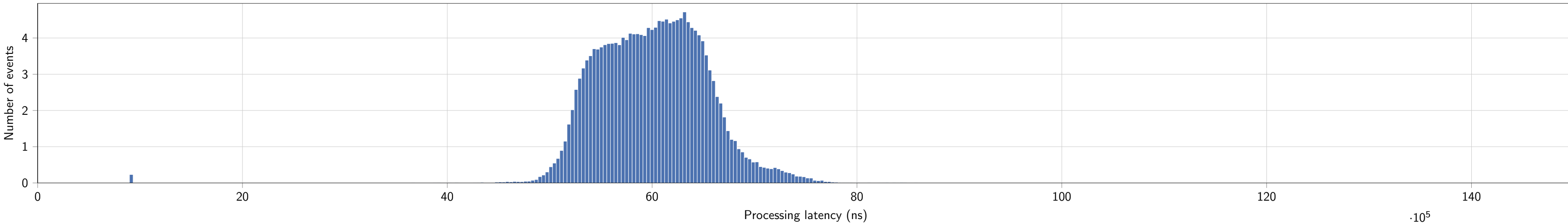
l2_multimac_00010000_mbit4060hires.histogram.csv: tx: 7.96mpps, 0.05stdDev; rx: 7.97mpps, 0.00stdDev



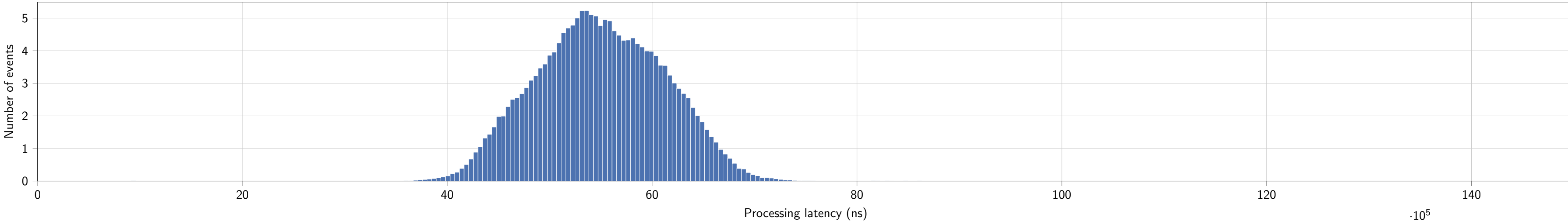
l2_multimac_00010000_mbit4070hires.histogram.csv: tx: 7.96mpps, 0.05stdDev; rx: 7.97mpps, 0.00stdDev



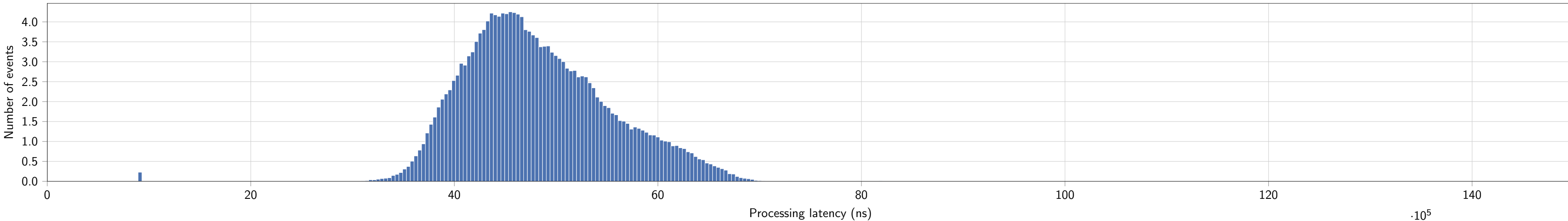
l2_multimac_00010000_mbit4080hires.histogram.csv: tx: 8.01mpps, 0.05stdDev; rx: 8.02mpps, 0.00stdDev



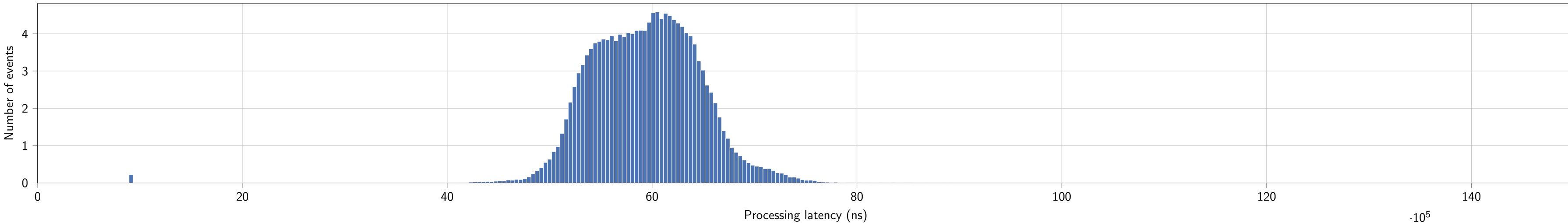
l2_multimac_00010000_mbit4090hires.histogram.csv: tx: 8.01mpps, 0.05stdDev; rx: 8.02mpps, 0.00stdDev



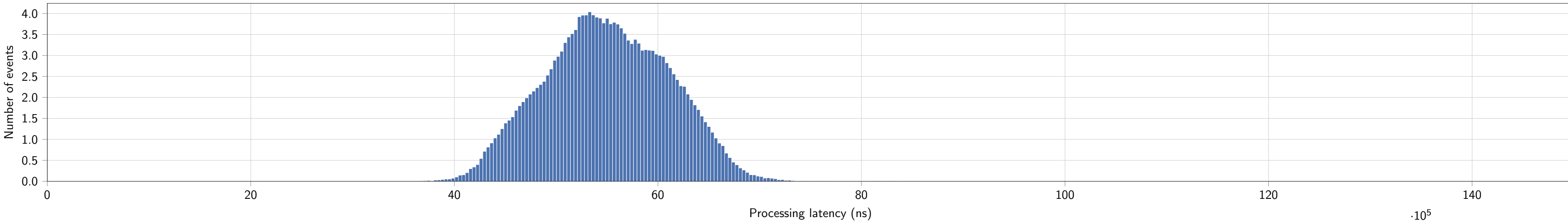
l2_multimac_00010000_mbit4100hires.histogram.csv: tx: 8.01mpps, 0.05stdDev; rx: 8.02mpps, 0.00stdDev



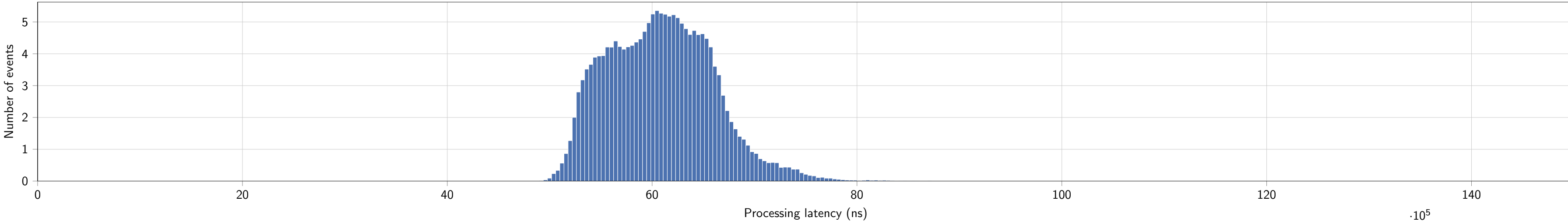
l2_multimac_00010000_mbit4110hires.histogram.csv: tx: 8.06mpps, 0.05stdDev; rx: 8.07mpps, 0.00stdDev



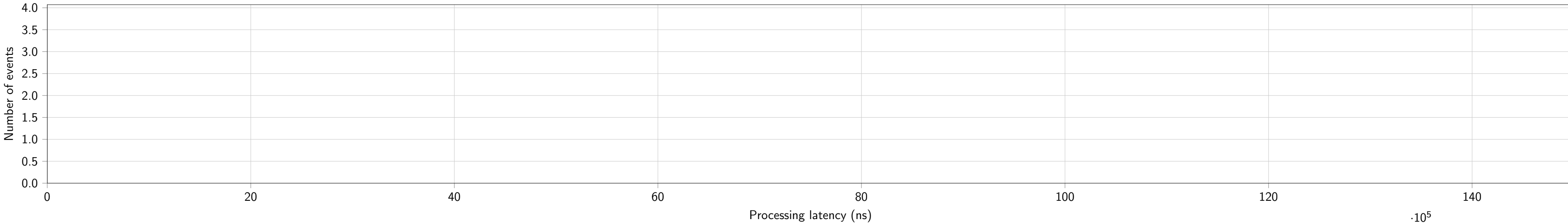
l2_multimac_00010000_mbit4120_final.histogram.csv: tx: 8.06mpps, 0.05stdDev; rx: 8.07mpps, 0.00stdDev



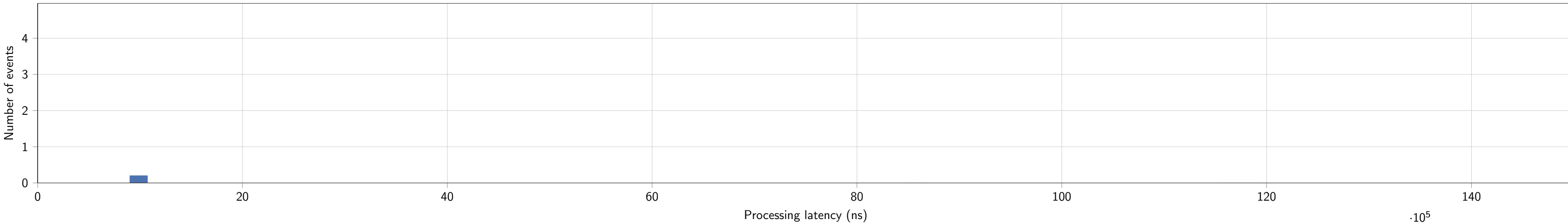
l2_multimac_00010000_mbit4120hires.histogram.csv: tx: 8.06mpps, 0.05stdDev; rx: 8.07mpps, 0.00stdDev



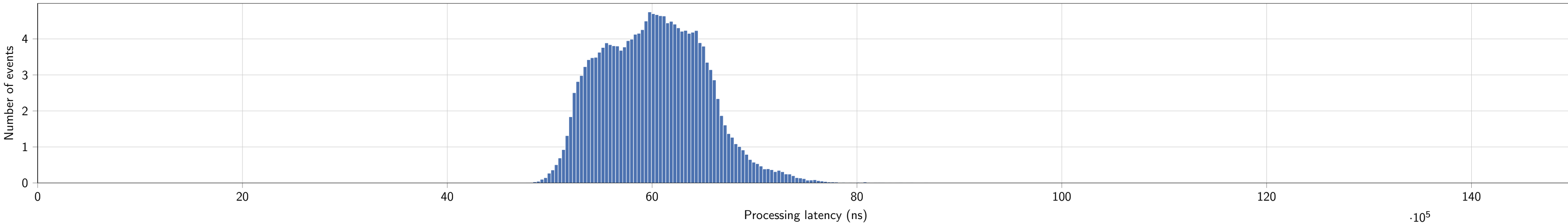
l2_multimac_00010000_mbit4130hires.histogram.csv: tx: 8.11mpps, 0.05stdDev; rx: 8.02mpps, 0.00stdDev



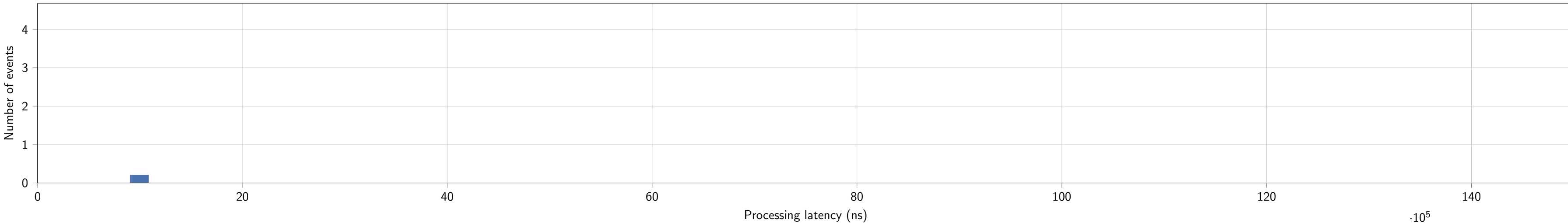
l2_multimac_00010000_mbit4140hires.histogram.csv: tx: 8.11mpps, 0.05stdDev; rx: 8.09mpps, 0.00stdDev



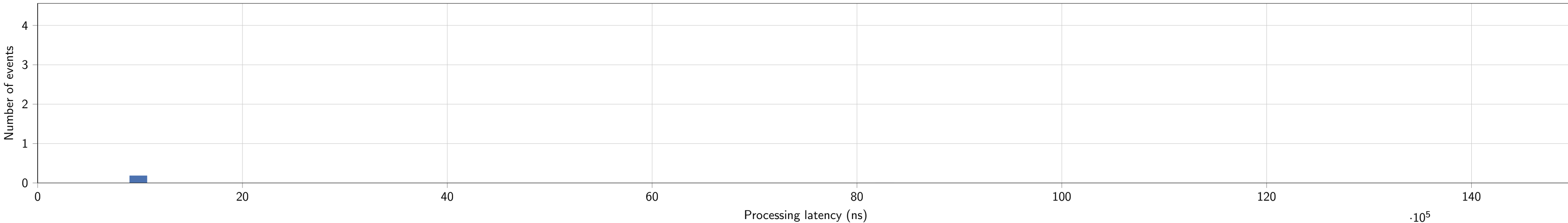
l2_multimac_00010000_mbit4150hires.histogram.csv: tx: 8.11mpps, 0.05stdDev; rx: 8.13mpps, 0.00stdDev



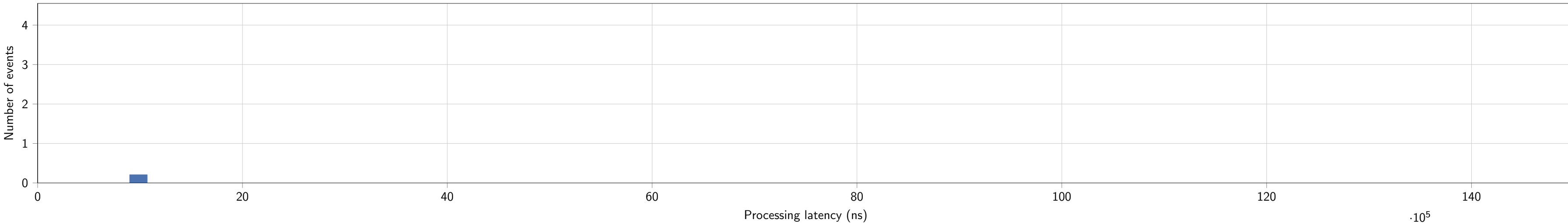
l2_multimac_00010000_mbit4160hires.histogram.csv: tx: 8.16mpps, 0.05stdDev; rx: 8.06mpps, 0.00stdDev



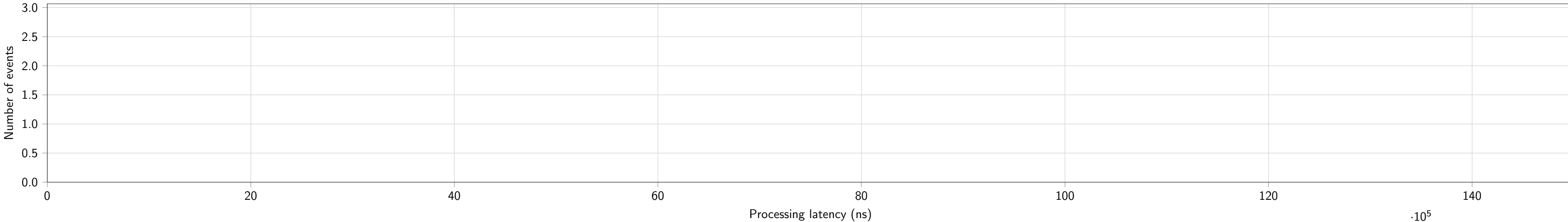
l2_multimac_00010000_mbit4170hires.histogram.csv: tx: 8.16mpps, 0.05stdDev; rx: 8.12mpps, 0.00stdDev



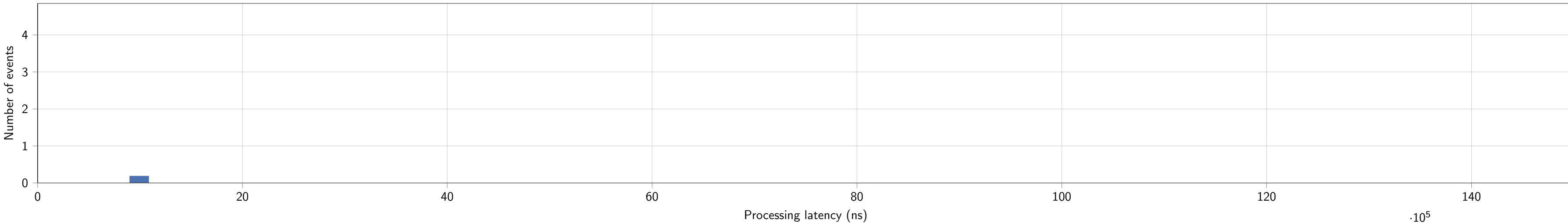
l2_multimac_00010000_mbit4180hires.histogram.csv: tx: 8.16mpps, 0.05stdDev; rx: 8.10mpps, 0.00stdDev



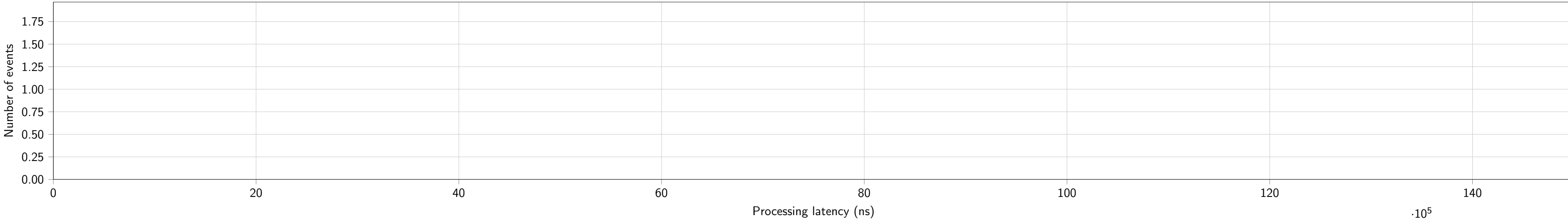
l2_multimac_00010000_mbit4190hires.histogram.csv: tx: 8.21mpps, 0.05stdDev; rx: 8.13mpps, 0.00stdDev



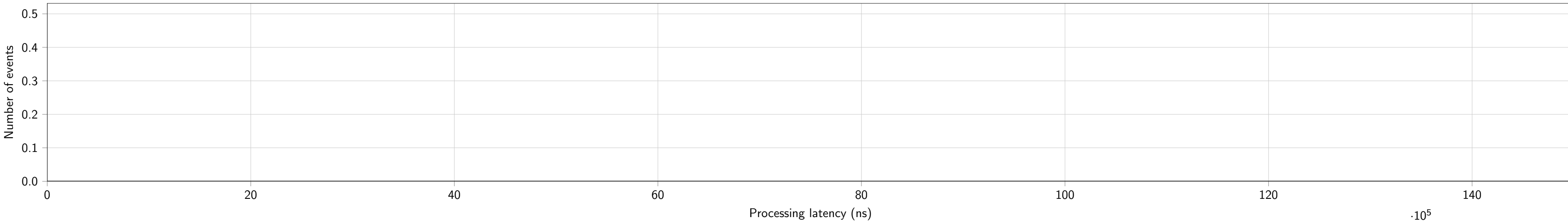
l2_multimac_00010000_mbit4200hires.histogram.csv: tx: 8.21mpps, 0.05stdDev; rx: 8.12mpps, 0.00stdDev



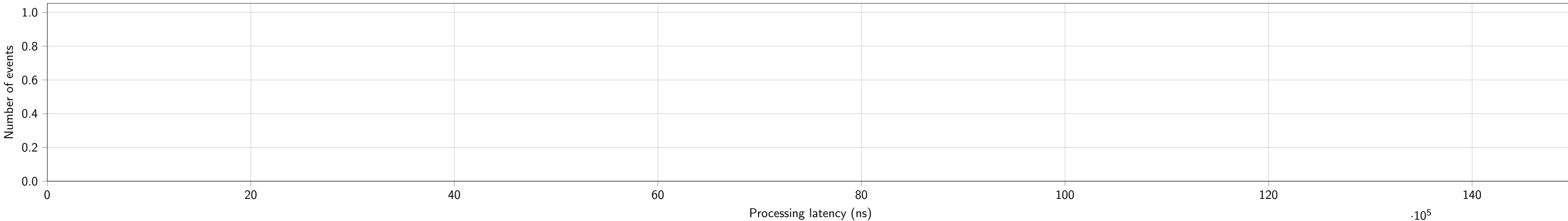
l2_multimac_00010000_mbit4400.histogram.csv: tx: 8.61mpps, 0.05stdDev; rx: 8.13mpps, 0.00stdDev



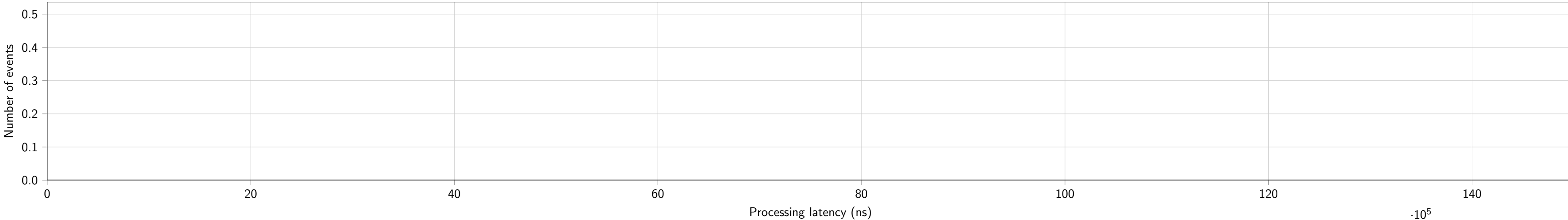
l2_multimac_00010000_mbit4800.histogram.csv: tx: 9.21mpps, 0.05stdDev; rx: 8.11mpps, 0.00stdDev



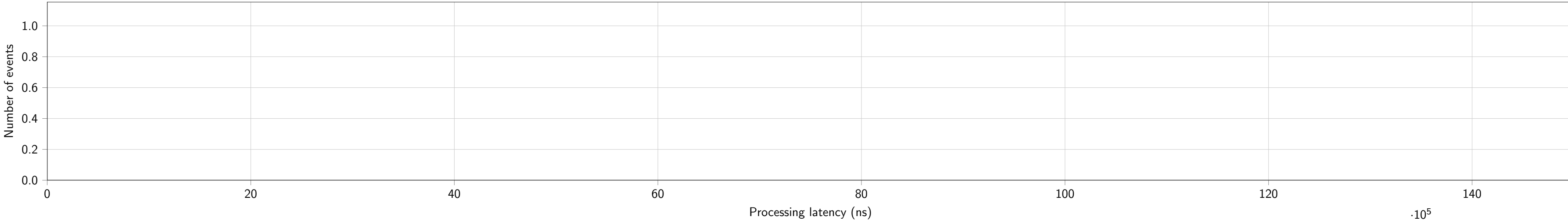
l2_multimac_00010000_mbit5200.histogram.csv: tx: 9.21mpps, 0.05stdDev; rx: 8.08mpps, 0.00stdDev



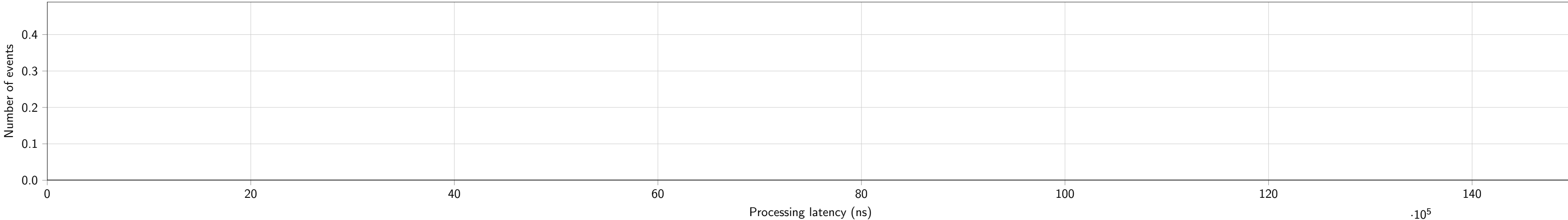
l2_multimac_00010000_mbit5600.histogram.csv: tx: 9.22mpps, 0.05stdDev; rx: 8.14mpps, 0.00stdDev



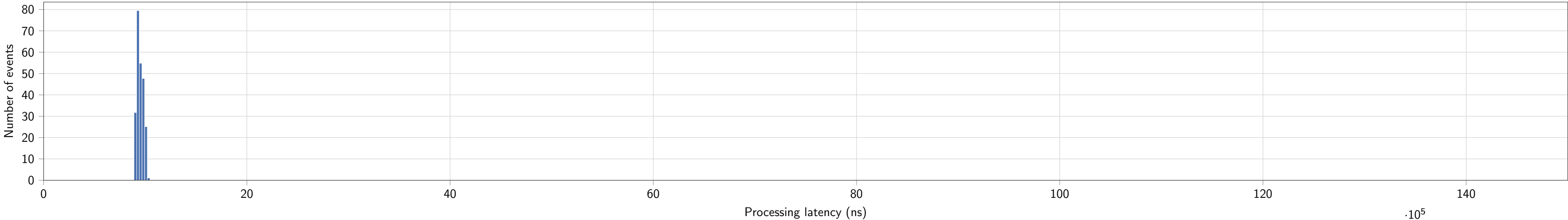
l2_multimac_00010000_mbit6000.histogram.csv: tx: 9.18mpps, 0.05stdDev; rx: 8.07mpps, 0.00stdDev



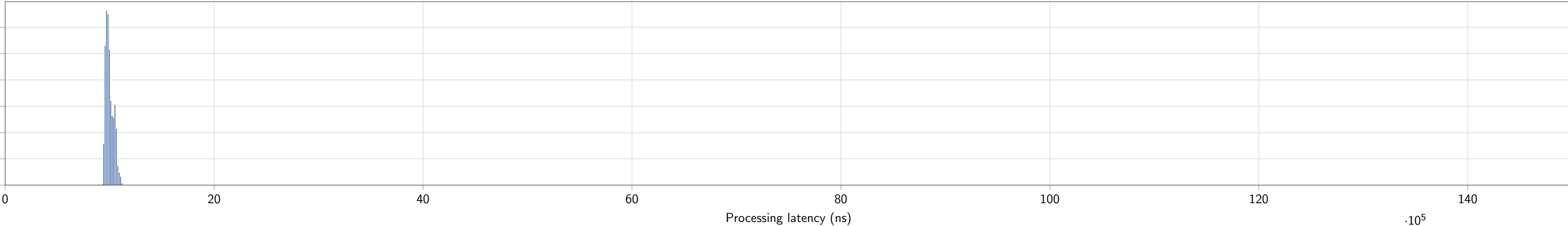
l2_multimac_00010000_mbit9000.histogram.csv: tx: 9.25mpps, 0.05stdDev; rx: 8.11mpps, 0.00stdDev

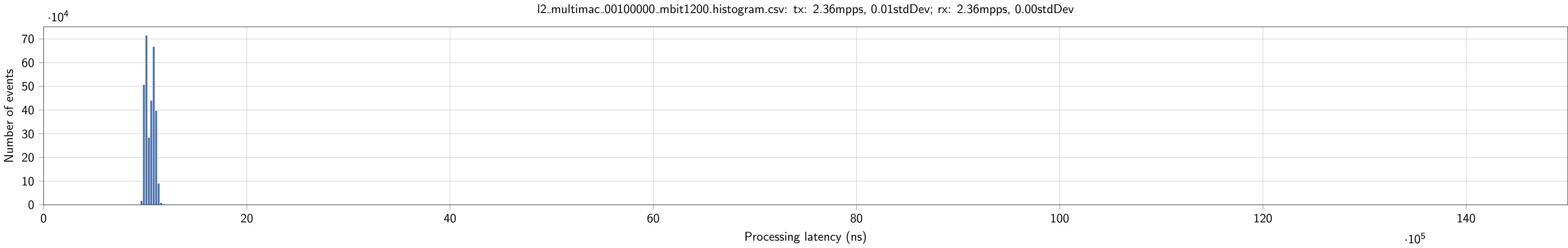


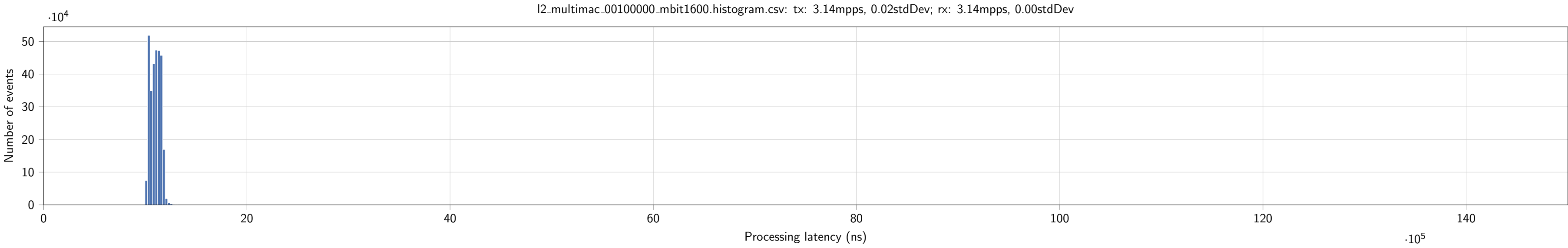
l2_multimac_00100000_mbit0400.histogram.csv: tx: 0.79mpps, 0.00stdDev; rx: 0.80mpps, 0.00stdDev

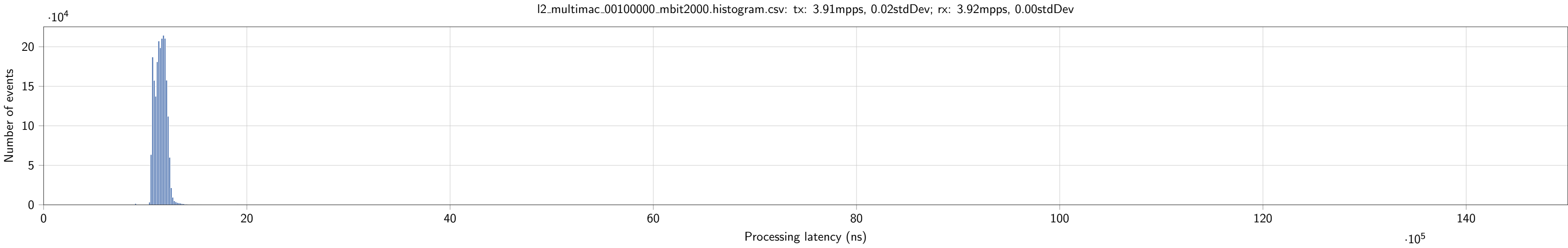


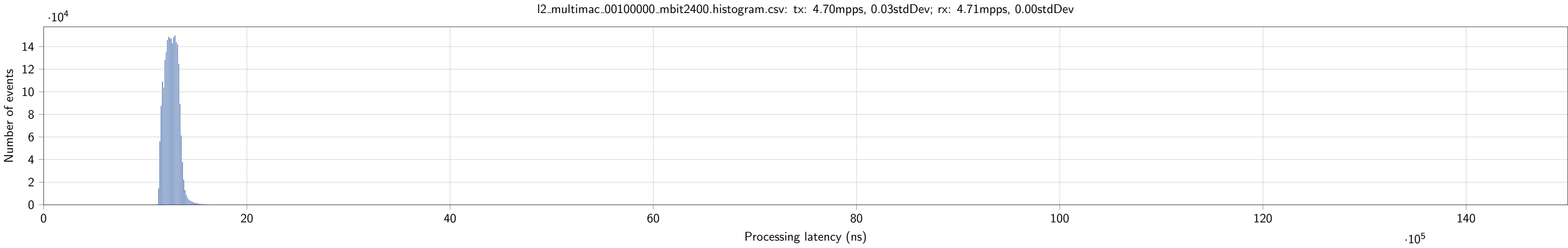
Number of events



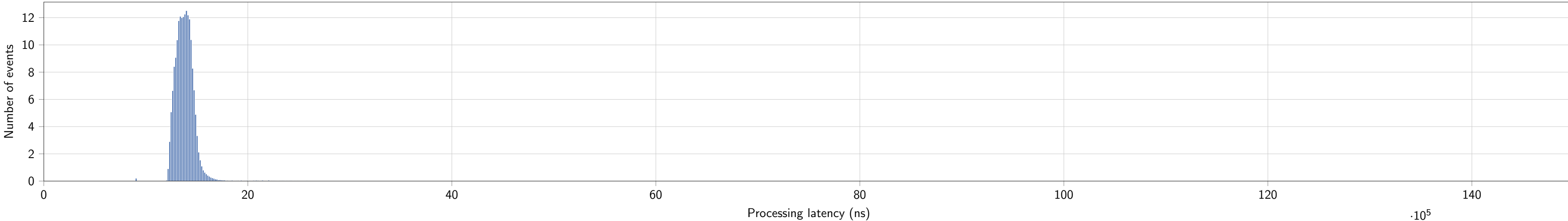




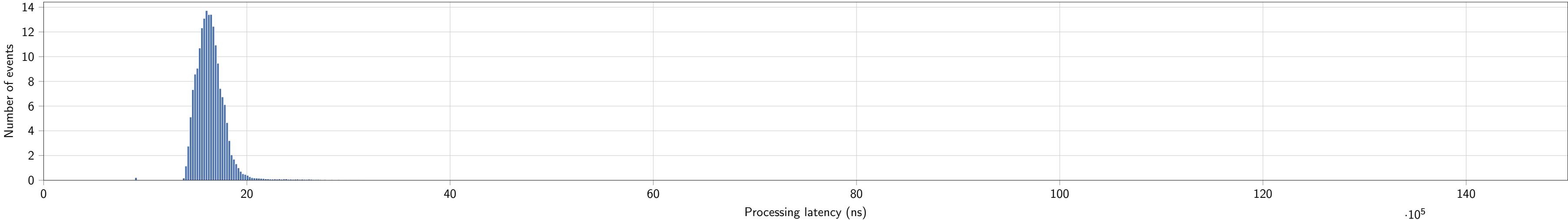




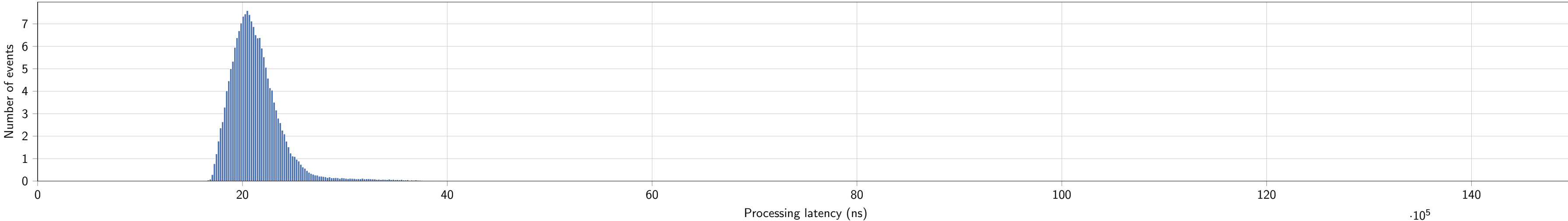
l2_multimac_00100000_mbit2800.histogram.csv: tx: 5.48mpps, 0.04stdDev; rx: 5.49mpps, 0.00stdDev

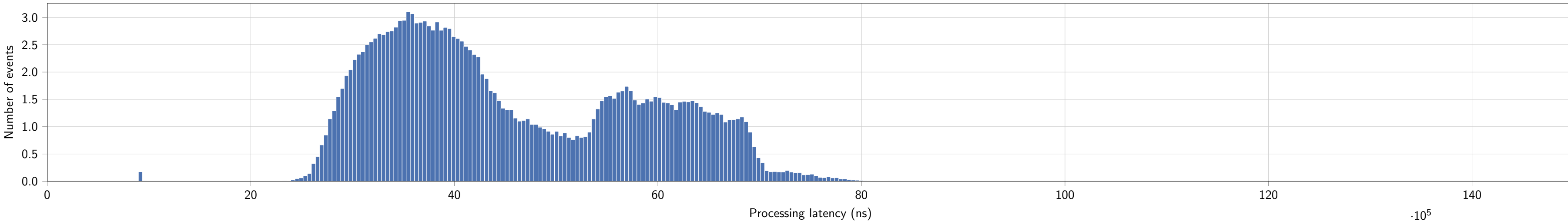


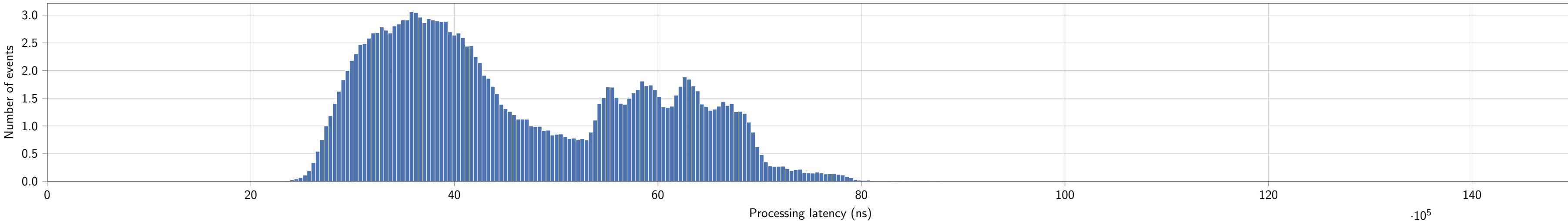
l2_multimac_00100000_mbit3200.histogram.csv: tx: 6.25mpps, 0.04stdDev; rx: 6.26mpps, 0.00stdDev



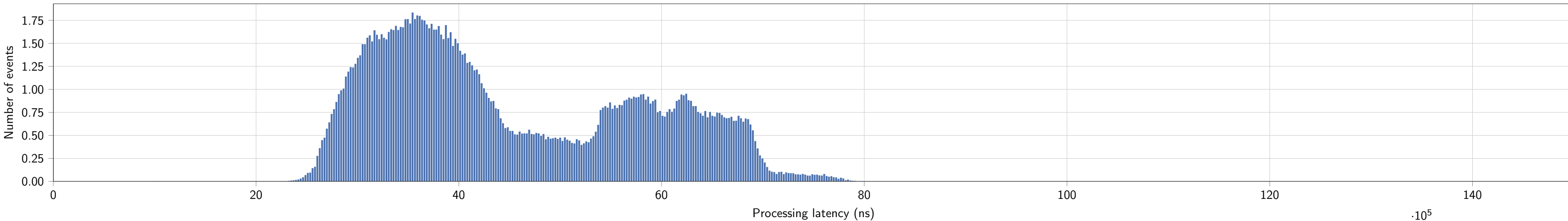
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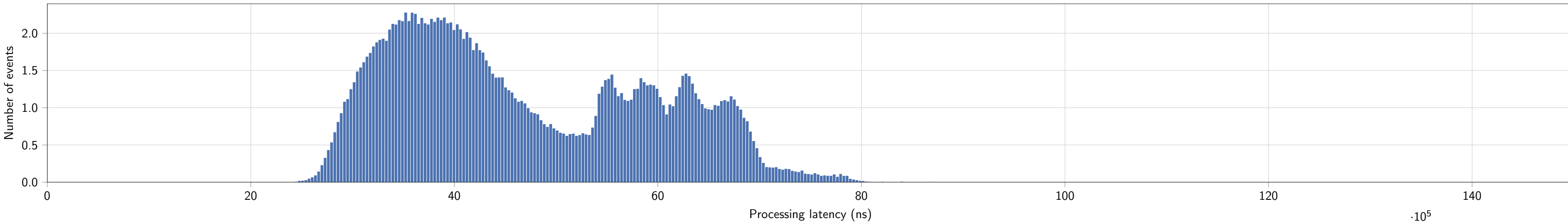




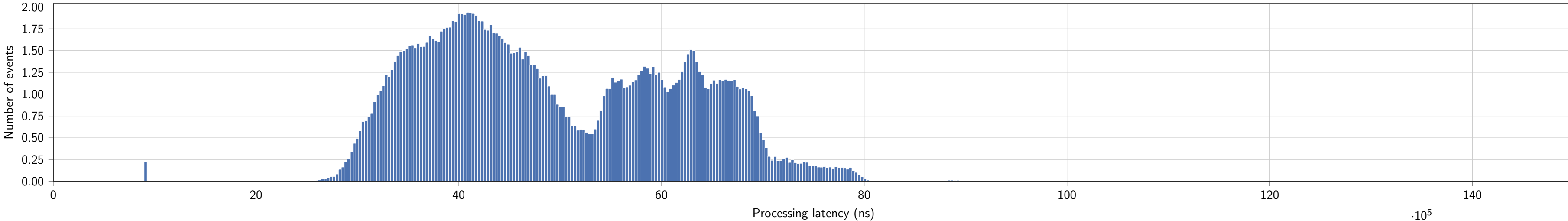
l2_multimac_00100000_mbit3998hires.histogram.csv: tx: 7.81mpps, 0.05stdDev; rx: 7.82mpps, 0.00stdDev



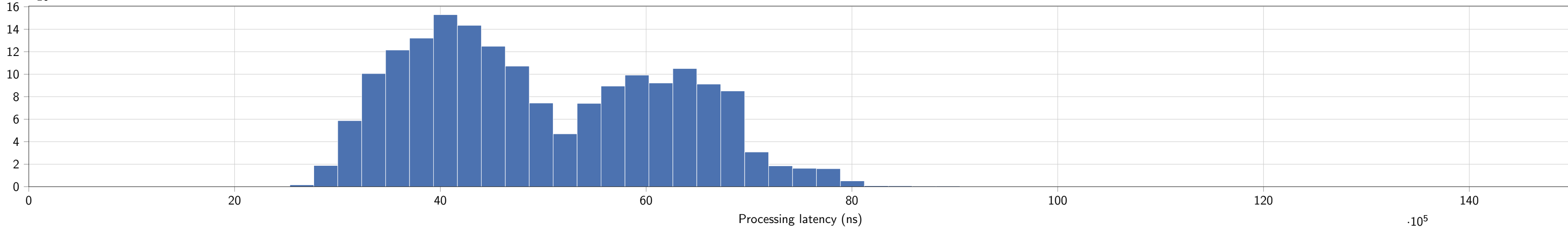
l2_multimac_00100000_mbit4000.histogram.csv: tx: 7.81mpps, 0.05stdDev; rx: 7.82mpps, 0.00stdDev



l2_multimac_00100000_mbit4008hires.histogram.csv: tx: 7.86mpps, 0.05stdDev; rx: 7.87mpps, 0.00stdDev

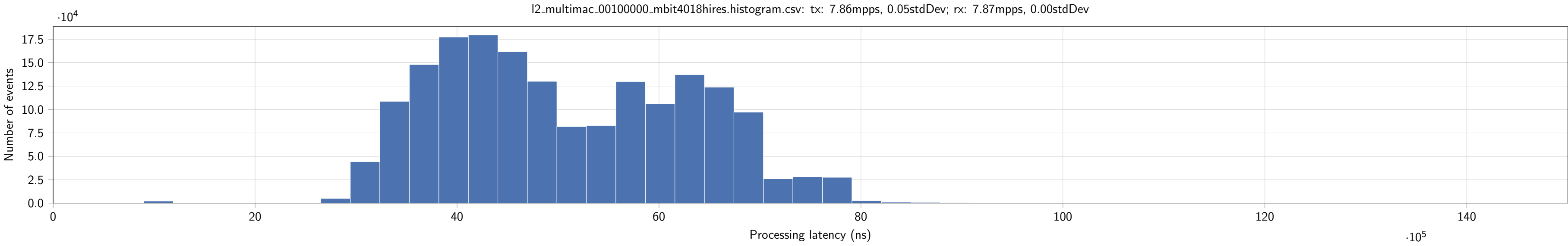


Number of events

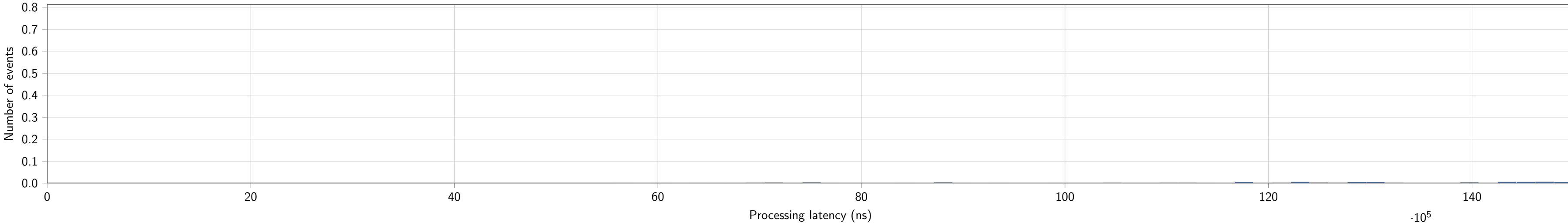
 $\cdot 10^4$ 

Processing latency (ns)

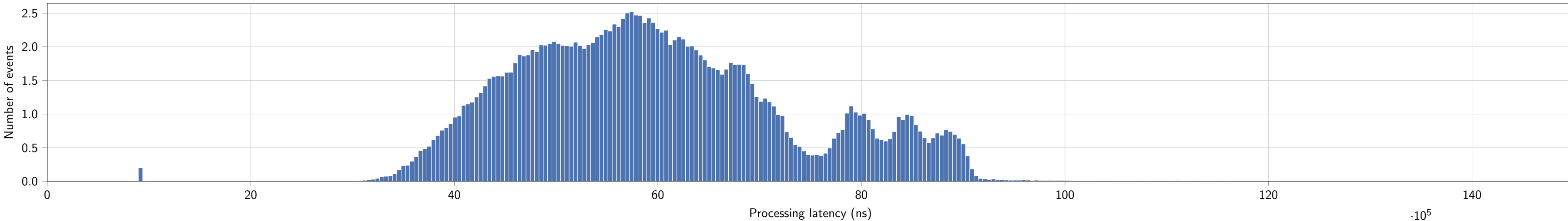
 $\cdot 10^5$



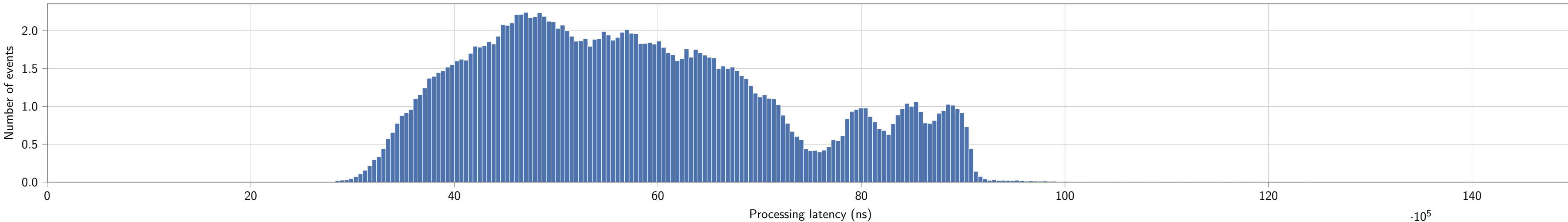
l2_multimac_00100000_mbit4028hires.histogram.csv: tx: 7.90mpps, 0.05stdDev; rx: 7.91mpps, 0.00stdDev



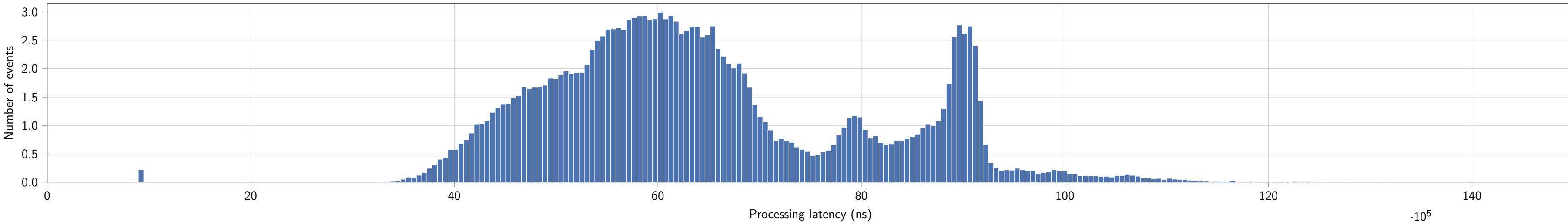
l2_multimac_00100000_mbit4038hires.histogram.csv: tx: 7.91mpps, 0.05stdDev; rx: 7.92mpps, 0.00stdDev

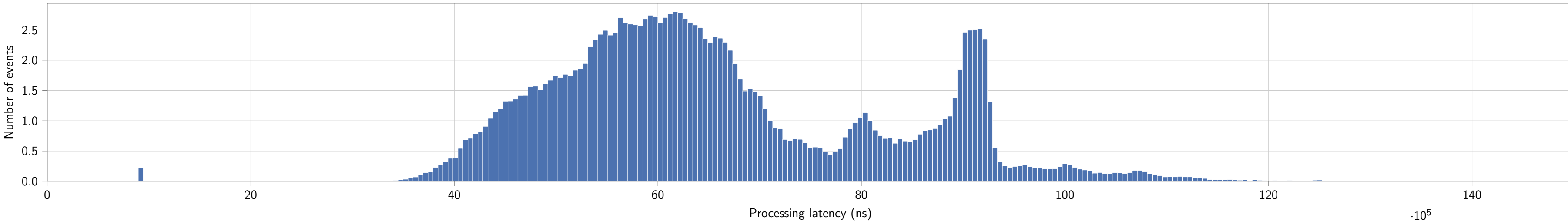


l2_multimac_00100000_mbit4048hires.histogram.csv: tx: 7.91mpps, 0.05stdDev; rx: 7.92mpps, 0.00stdDev

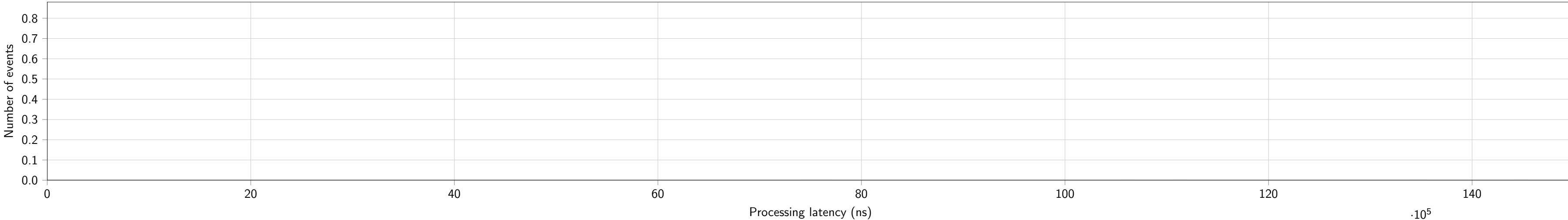


l2_multimac_00100000_mbit4058hires.histogram.csv: tx: 7.96mpps, 0.05stdDev; rx: 7.97mpps, 0.00stdDev

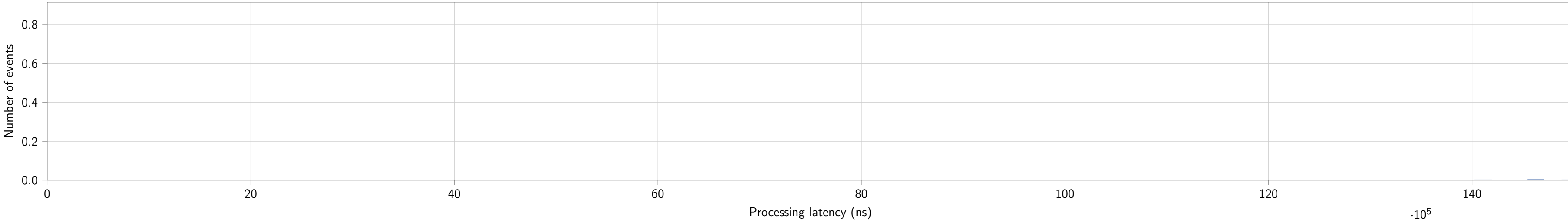




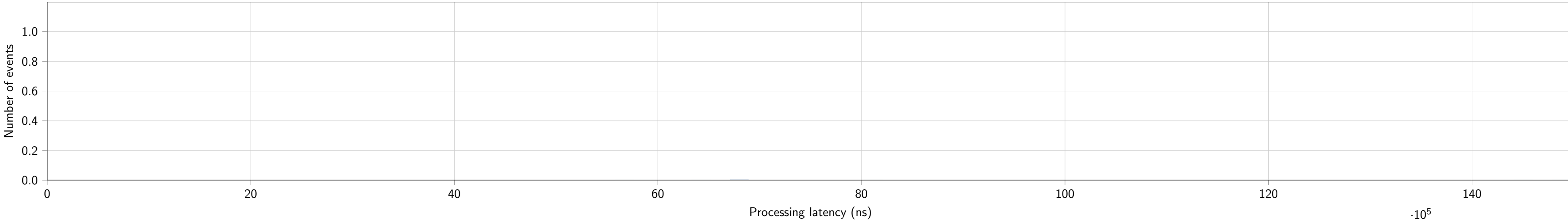
l2_multimac_00100000_mbit4078hires.histogram.csv: tx: 8.00mpps, 0.05stdDev; rx: 7.97mpps, 0.00stdDev



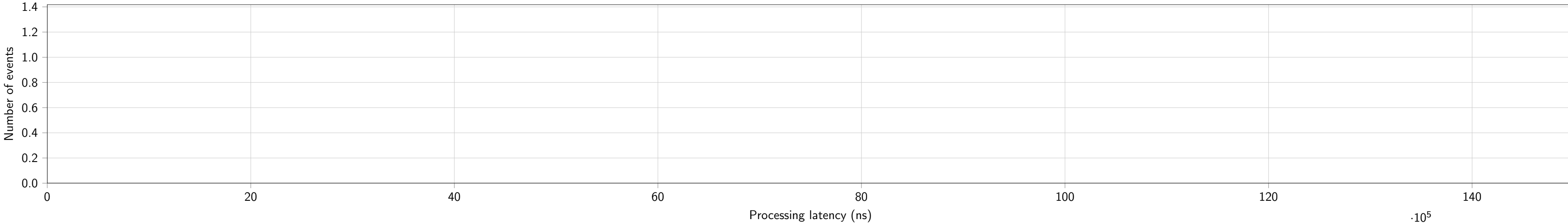
l2_multimac_00100000_mbit4088hires.histogram.csv: tx: 8.00mpps, 0.05stdDev; rx: 7.98mpps, 0.00stdDev



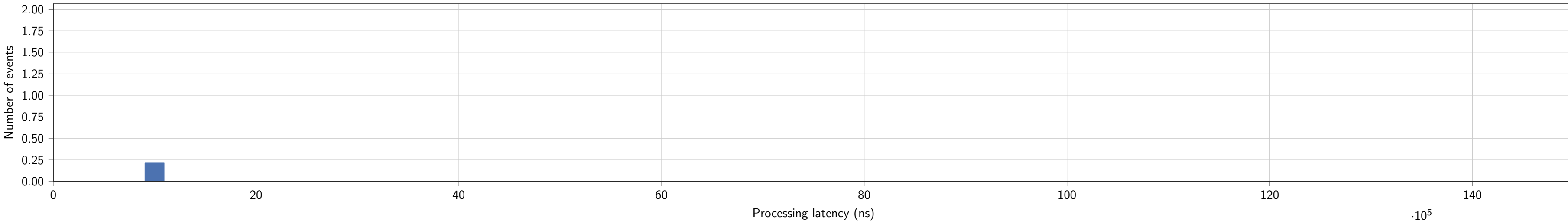
l2_multimac_00100000_mbit4098hires.histogram.csv: tx: 8.00mpps, 0.05stdDev; rx: 7.97mpps, 0.00stdDev



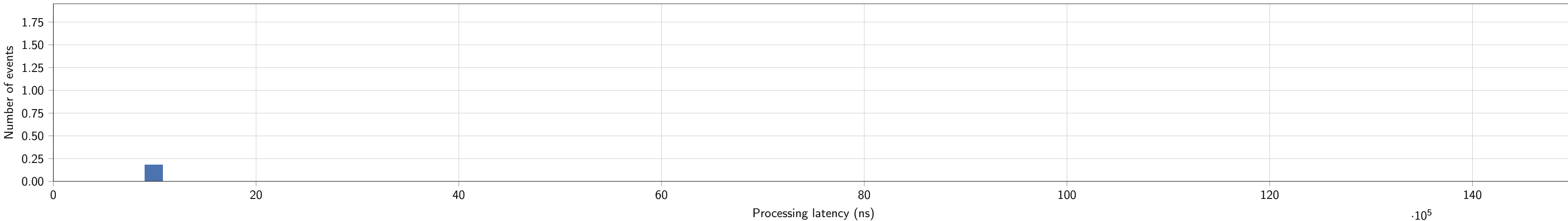
l2_multimac_00100000_mbit4108hires.histogram.csv: tx: 8.05mpps, 0.05stdDev; rx: 7.98mpps, 0.00stdDev



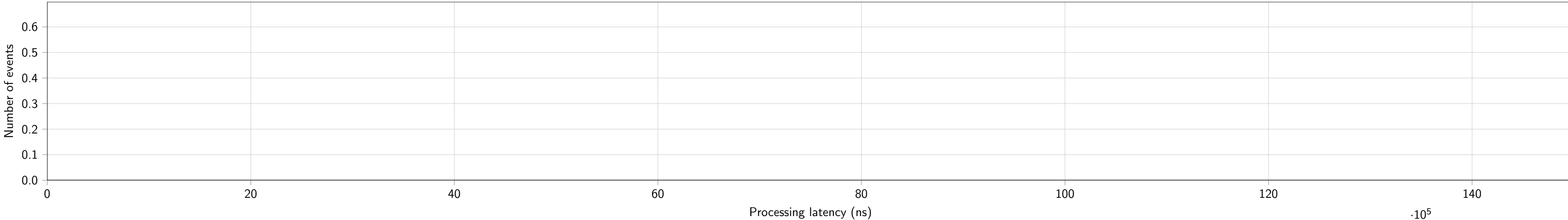
l2_multimac_00100000_mbit4118hires.histogram.csv: tx: 8.05mpps, 0.05stdDev; rx: 7.96mpps, 0.00stdDev



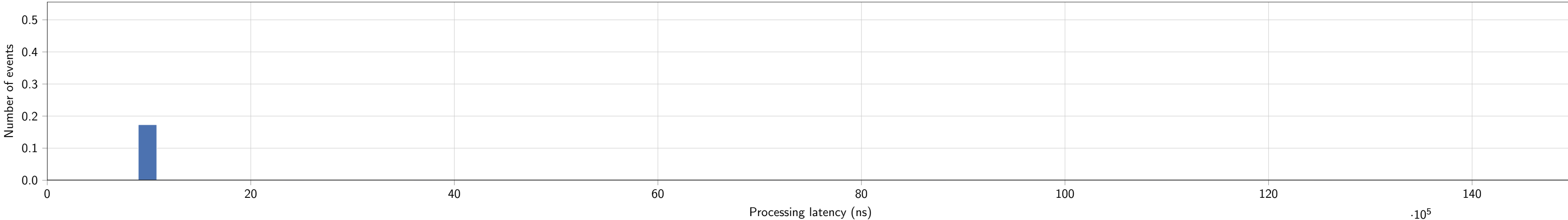
l2_multimac_00100000_mbit4128hires.histogram.csv: tx: 8.05mpps, 0.05stdDev; rx: 7.97mpps, 0.00stdDev



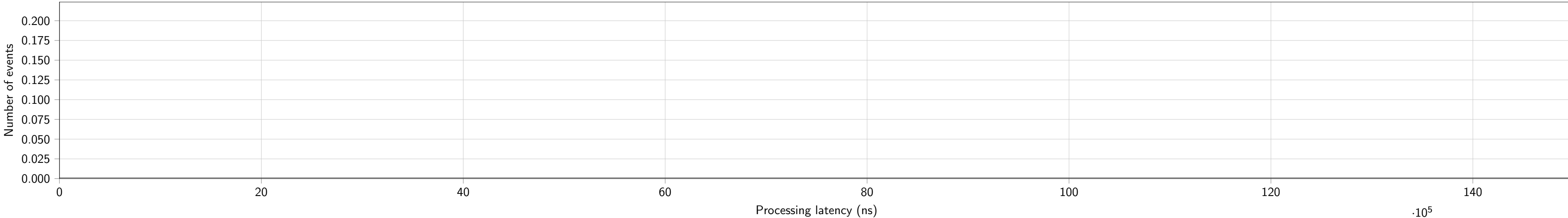
l2_multimac_00100000_mbit4400.histogram.csv: tx: 8.61mpps, 0.05stdDev; rx: 7.96mpps, 0.00stdDev



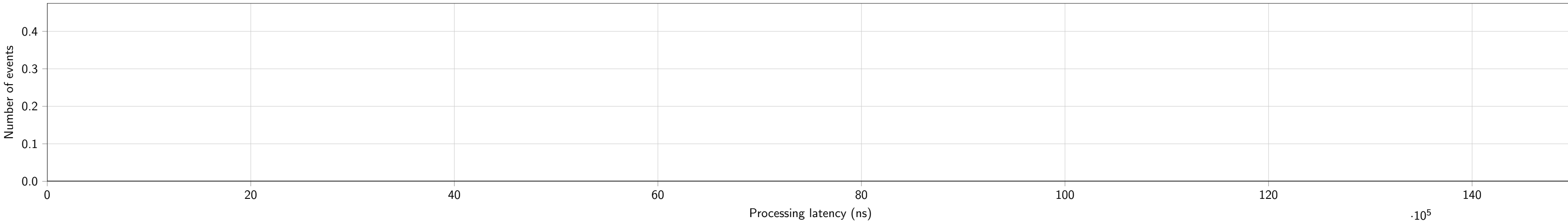
l2_multimac_00100000_mbit4800.histogram.csv: tx: 9.20mpps, 0.05stdDev; rx: 7.94mpps, 0.00stdDev



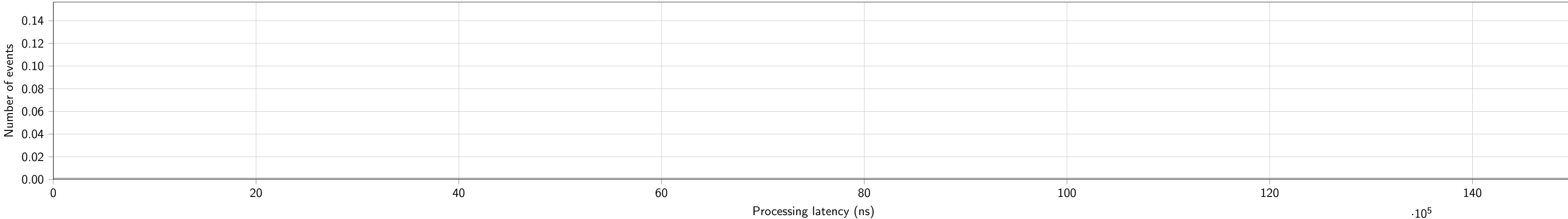
l2_multimac_00100000_mbit5200.histogram.csv: tx: 9.21mpps, 0.05stdDev; rx: 7.93mpps, 0.00stdDev



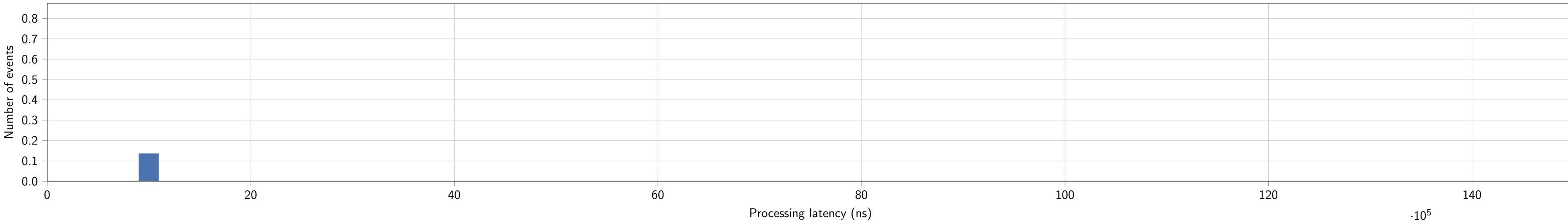
l2_multimac_00100000_mbit5600.histogram.csv: tx: 9.23mpps, 0.05stdDev; rx: 7.93mpps, 0.00stdDev

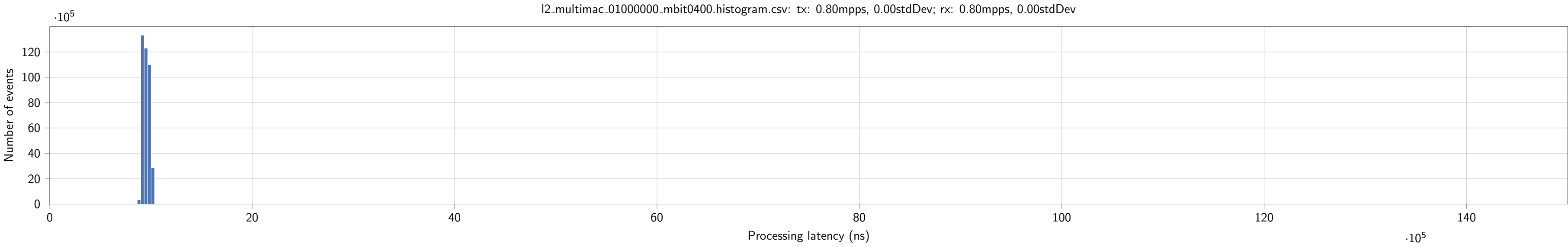


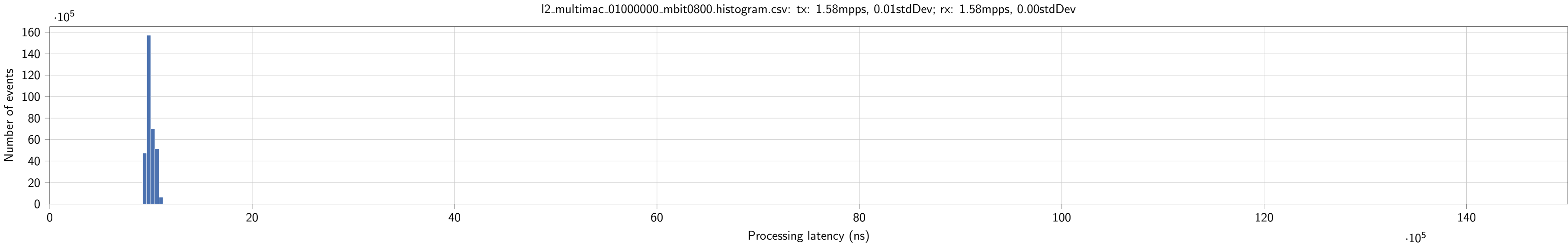
l2_multimac_00100000_mbit6000.histogram.csv: tx: 9.22mpps, 0.05stdDev; rx: 7.94mpps, 0.00stdDev



l2_multimac_00100000_mbit9000.histogram.csv: tx: 9.20mpps, 0.05stdDev; rx: 7.96mpps, 0.00stdDev



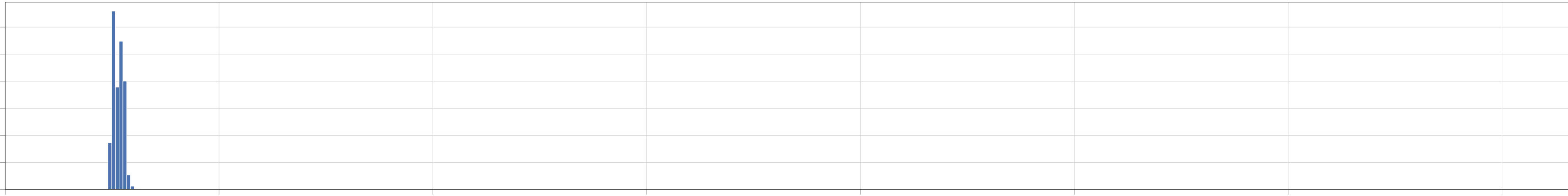




l2_multimac_01000000_mbit1200.histogram.csv: tx: 2.36mpps, 0.01stdDev; rx: 2.36mpps, 0.00stdDev

Number of events

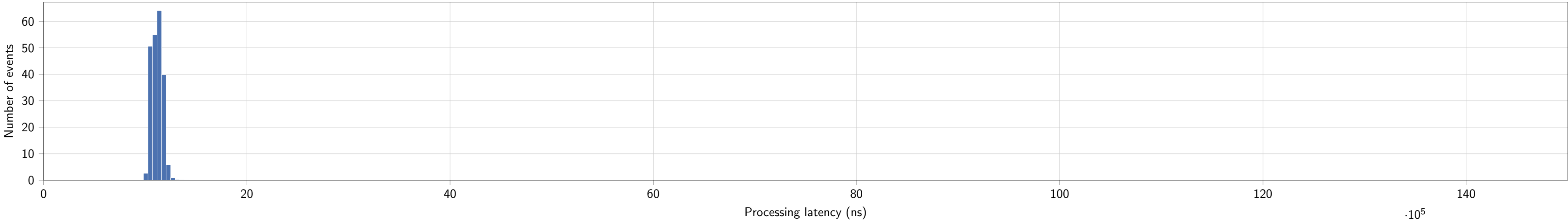
$\cdot 10^4$

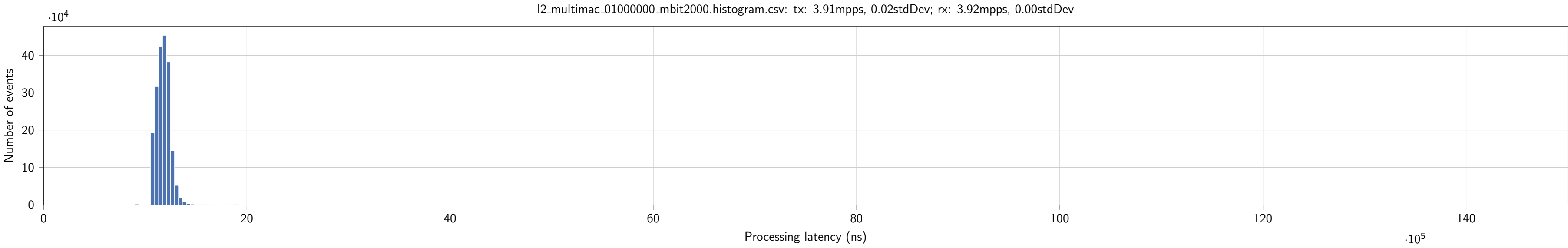


Processing latency (ns)

$\cdot 10^5$

l2_multimac_01000000_mbit1600.histogram.csv: tx: 3.13mpps, 0.02stdDev; rx: 3.14mpps, 0.00stdDev

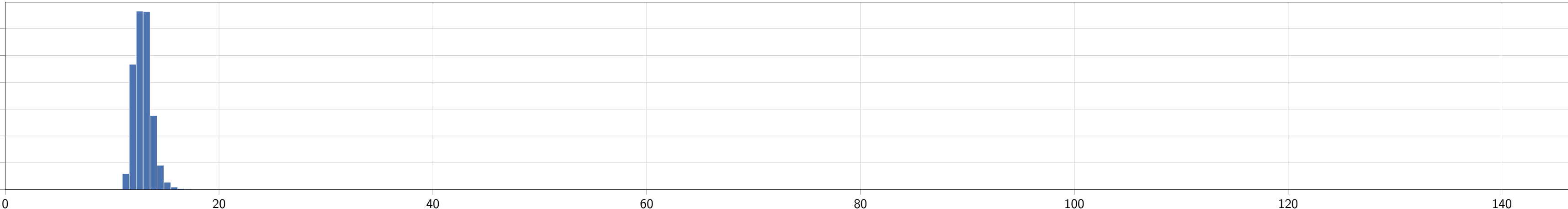




l2_multimac_01000000_mbit2400.histogram.csv: tx: 4.70mpps, 0.03stdDev; rx: 4.71mpps, 0.00stdDev

Number of events

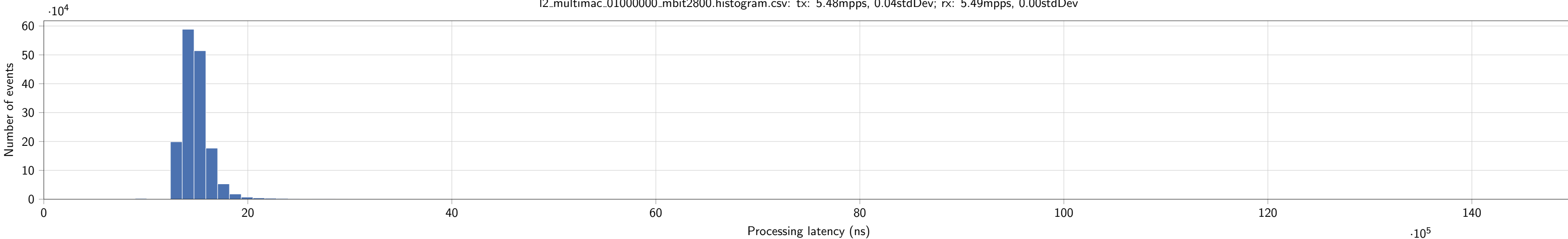
$\cdot 10^4$



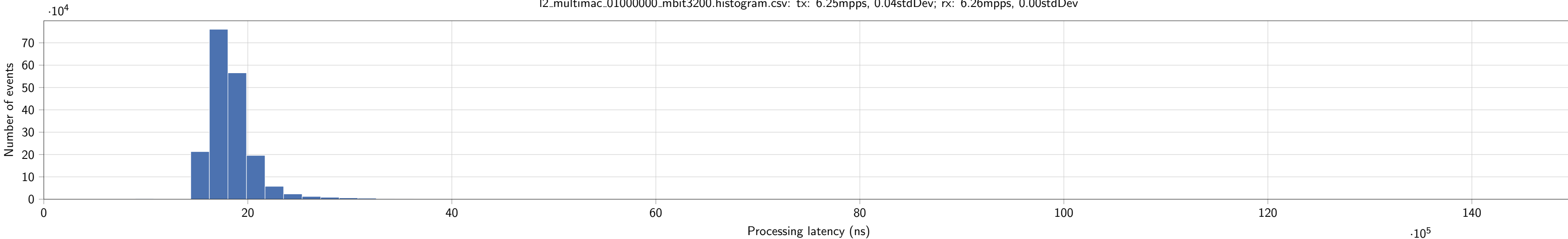
Processing latency (ns)

$\cdot 10^5$

l2_multimac_01000000_mbit2800.histogram.csv: tx: 5.48mpps, 0.04stdDev; rx: 5.49mpps, 0.00stdDev

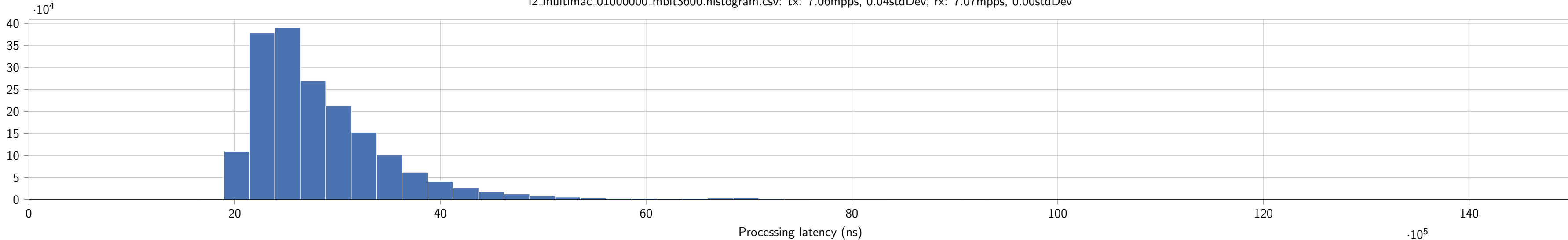


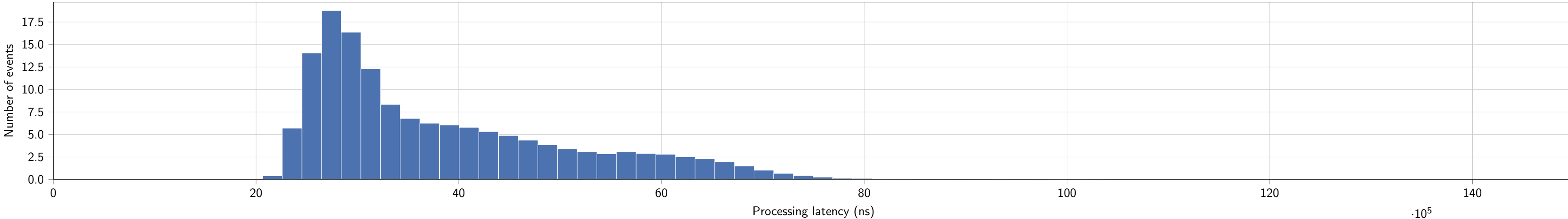
l2_multimac_01000000_mbit3200.histogram.csv: tx: 6.25mpps, 0.04stdDev; rx: 6.26mpps, 0.00stdDev

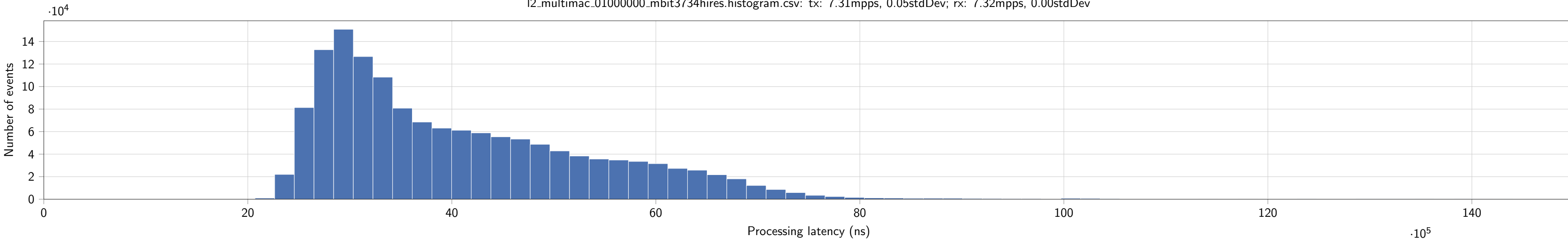


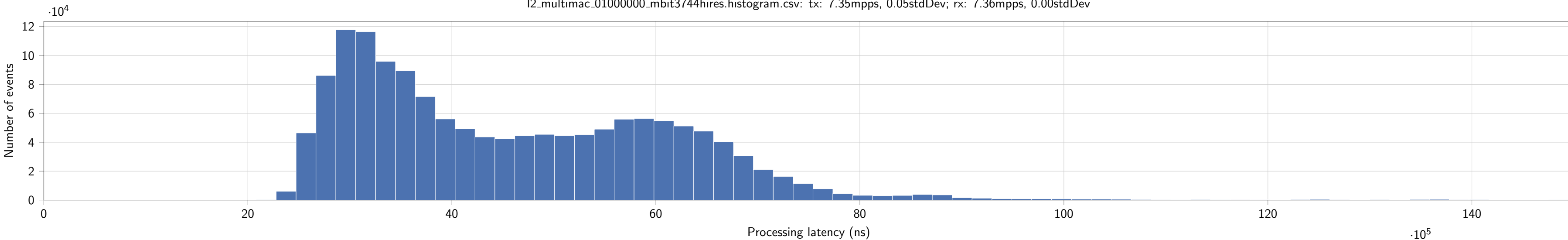
l2_multimac_01000000_mbit3600.histogram.csv: tx: 7.06mpps, 0.04stdDev; rx: 7.07mpps, 0.00stdDev

Number of events

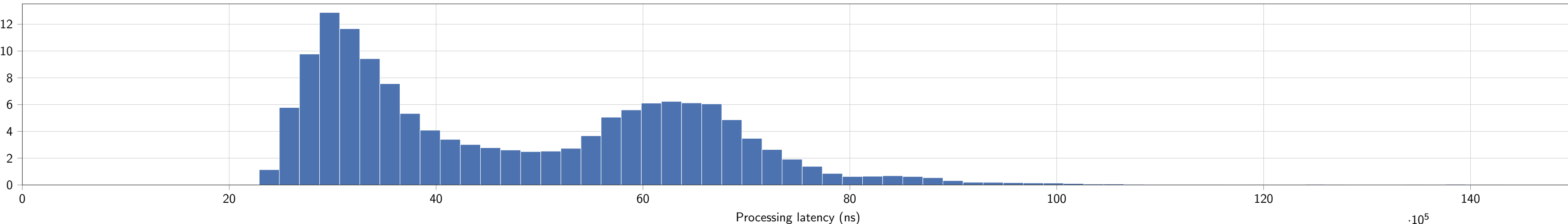




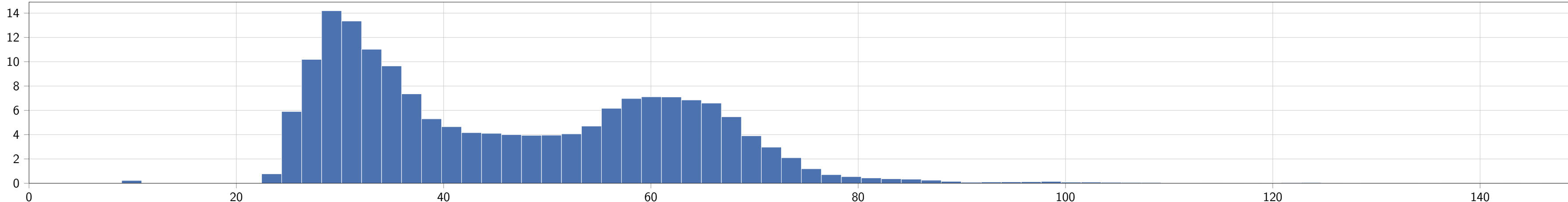




Number of events

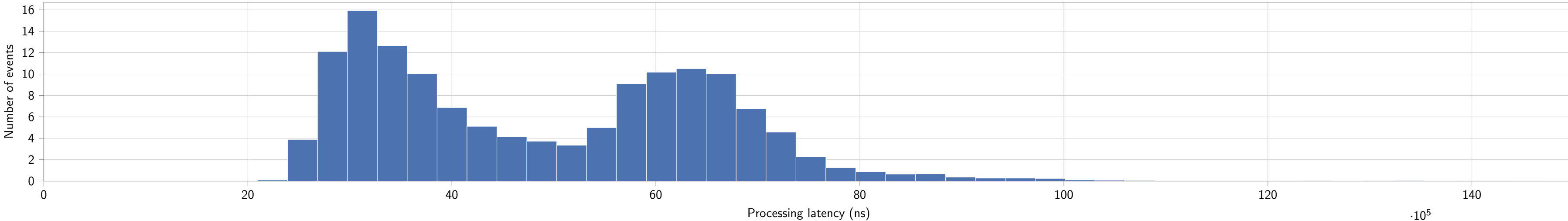
 $\cdot 10^4$ 

Number of events

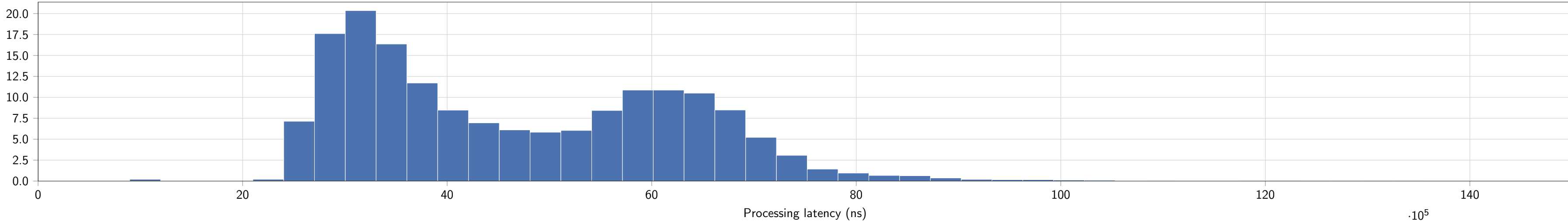
 $\cdot 10^4$ 

Processing latency (ns)

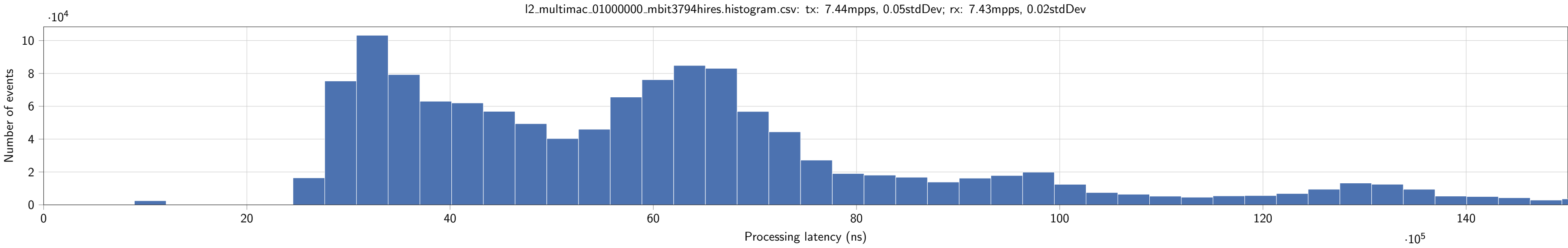
 $\cdot 10^5$

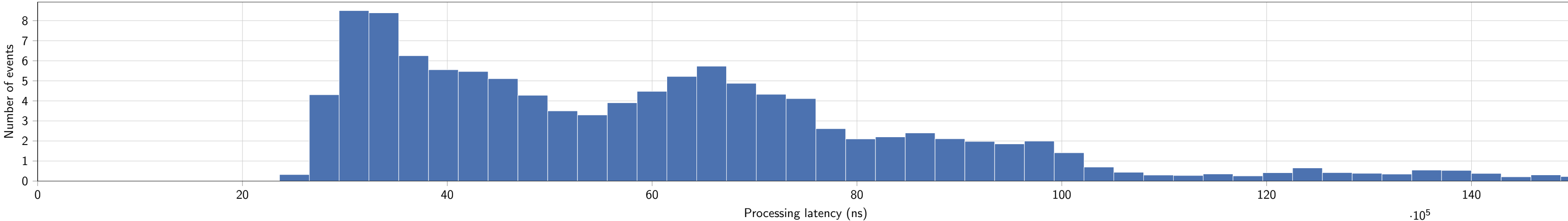


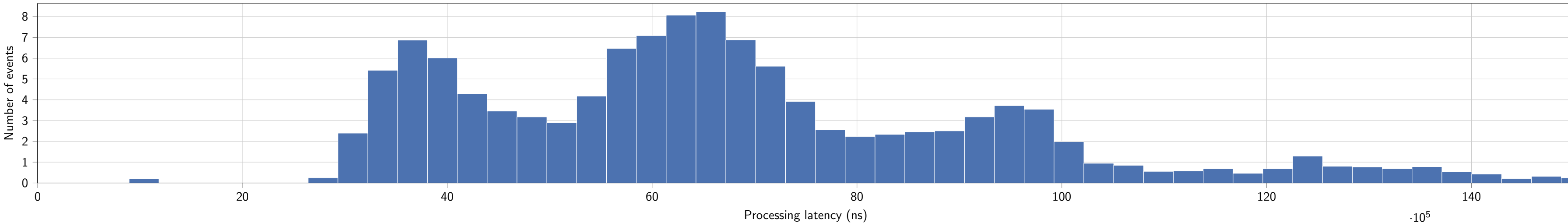
Number of events



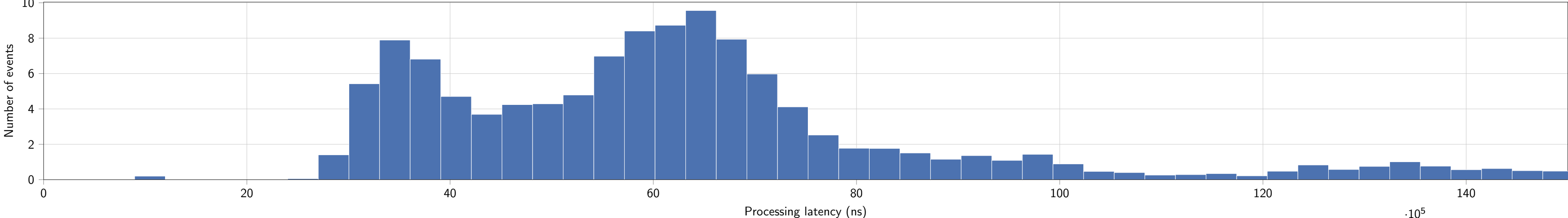
Number of events



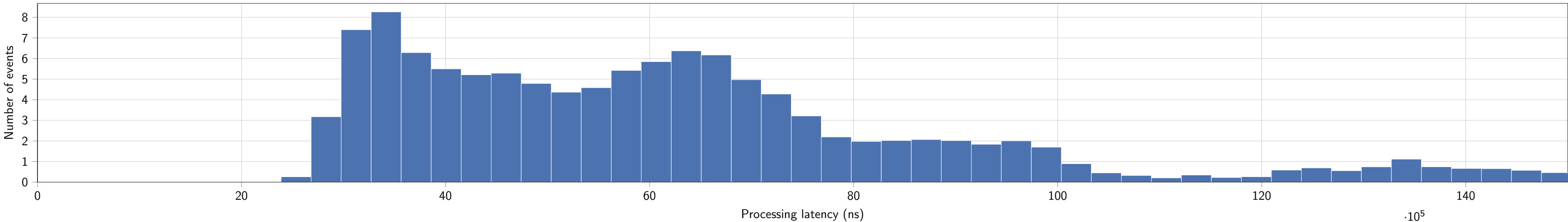




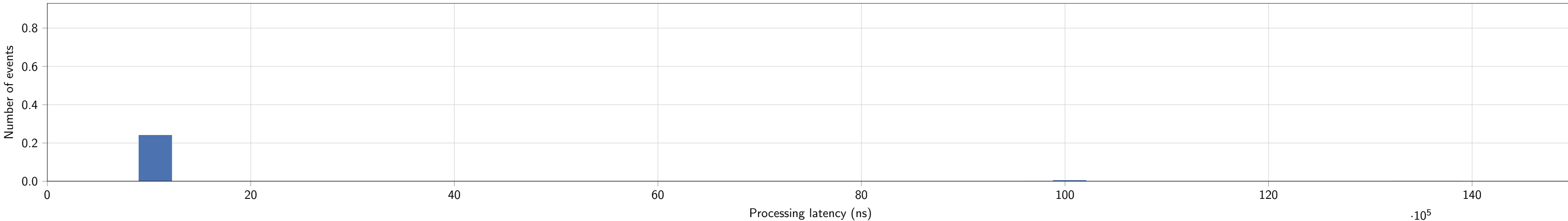
Number of events

 $\cdot 10^4$ 

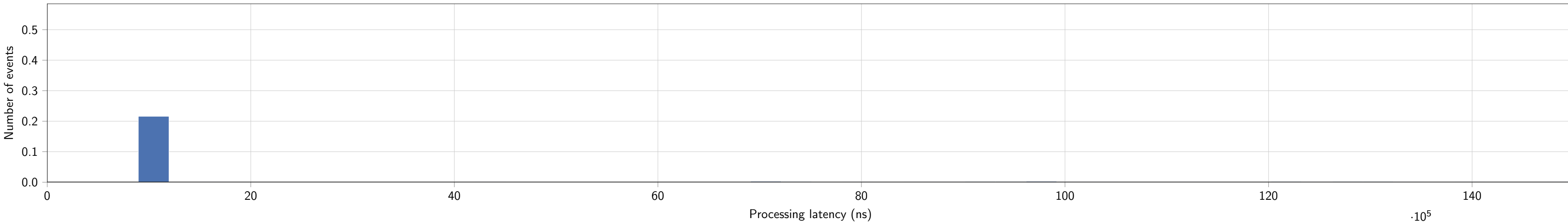
l2_multimac_01000000_mbit3824hires.histogram.csv: tx: 7.48mpps, 0.05stdDev; rx: 7.47mpps, 0.02stdDev



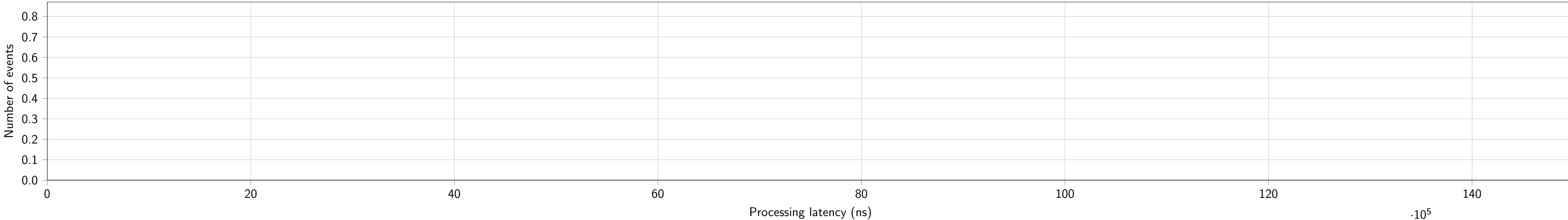
l2_multimac_01000000_mbit3834hires.histogram.csv: tx: 7.52mpps, 0.05stdDev; rx: 7.44mpps, 0.02stdDev



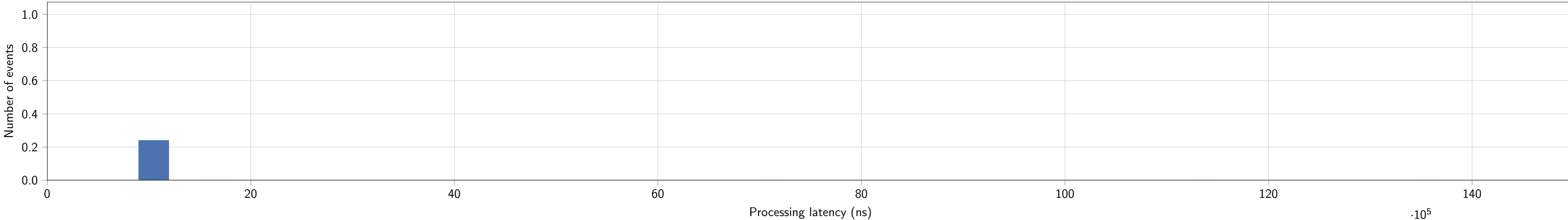
l2_multimac_01000000_mbit3844hires.histogram.csv: tx: 7.52mpps, 0.05stdDev; rx: 7.47mpps, 0.02stdDev



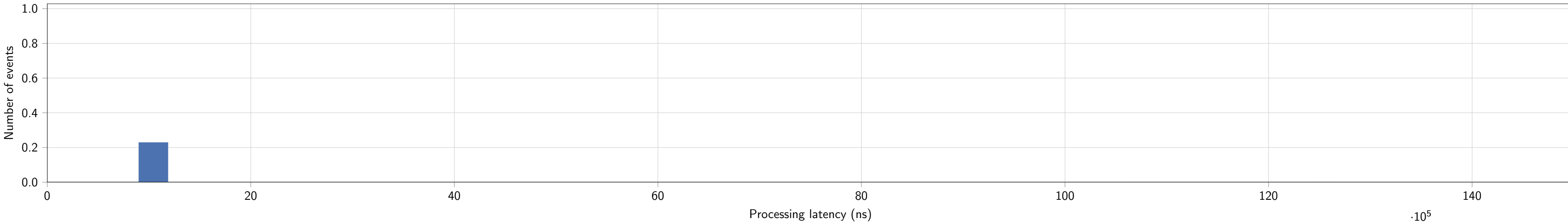
l2_multimac_01000000_mbit3854hires.histogram.csv: tx: 7.52mpps, 0.05stdDev; rx: 7.44mpps, 0.02stdDev



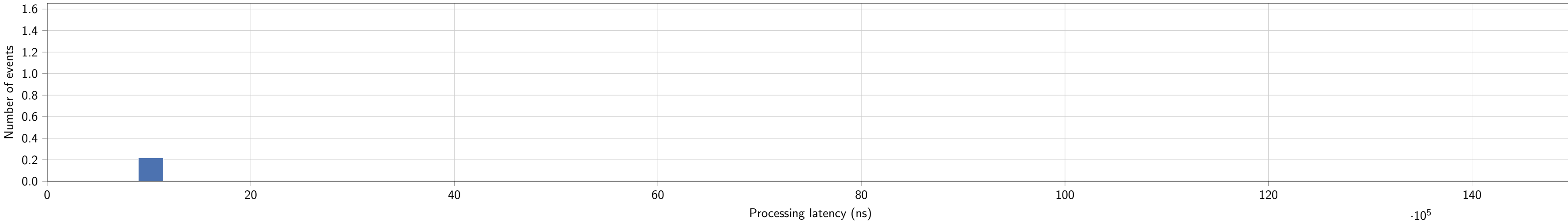
l2_multimac_01000000_mbit3864hires.histogram.csv: tx: 7.56mpps, 0.05stdDev; rx: 7.47mpps, 0.02stdDev



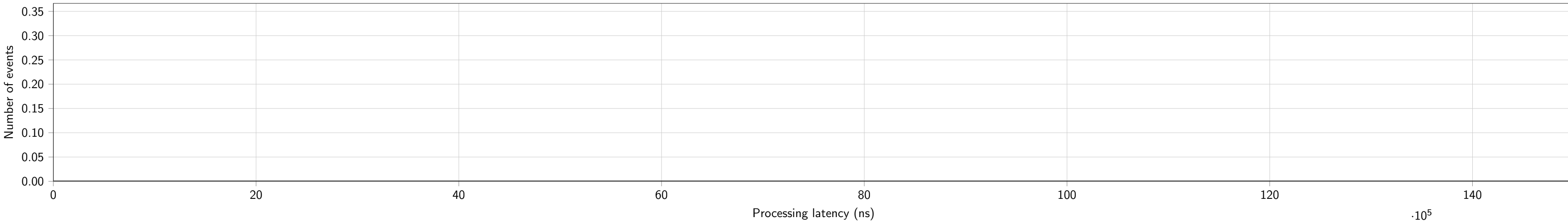
l2_multimac_01000000_mbit3874hires.histogram.csv: tx: 7.56mpps, 0.05stdDev; rx: 7.46mpps, 0.02stdDev



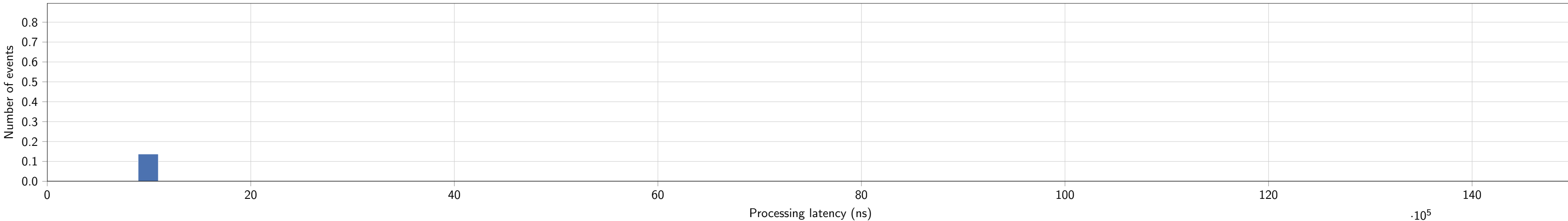
l2_multimac_01000000_mbit4000.histogram.csv: tx: 7.80mpps, 0.05stdDev; rx: 7.47mpps, 0.01stdDev



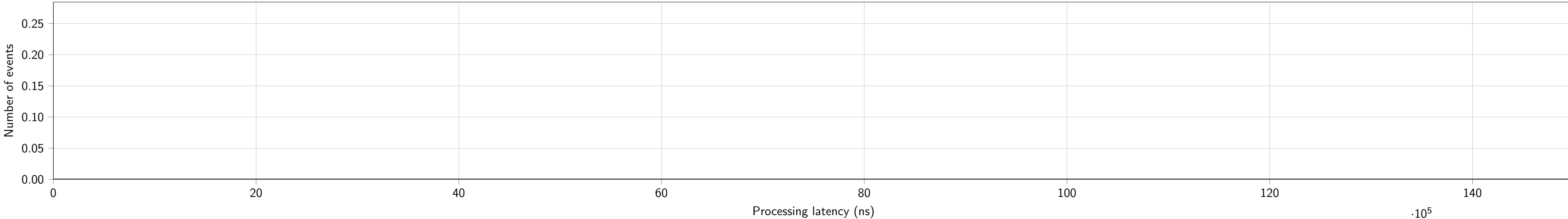
l2_multimac_01000000_mbit4400.histogram.csv: tx: 8.61mpps, 0.05stdDev; rx: 7.46mpps, 0.01stdDev



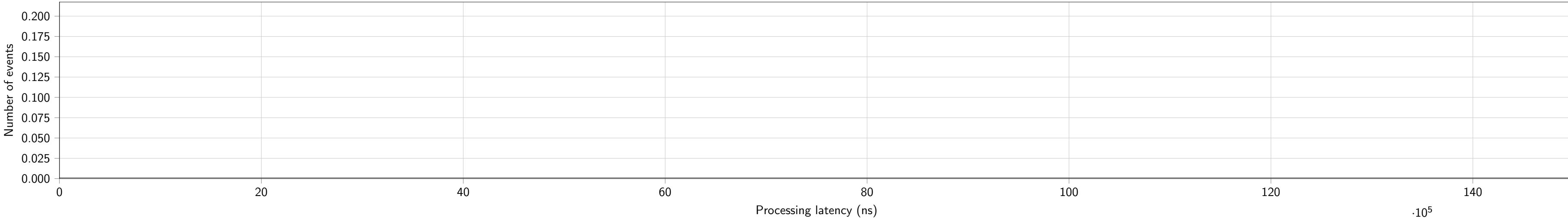
l2_multimac_01000000_mbit4800.histogram.csv: tx: 9.24mpps, 0.05stdDev; rx: 7.46mpps, 0.01stdDev



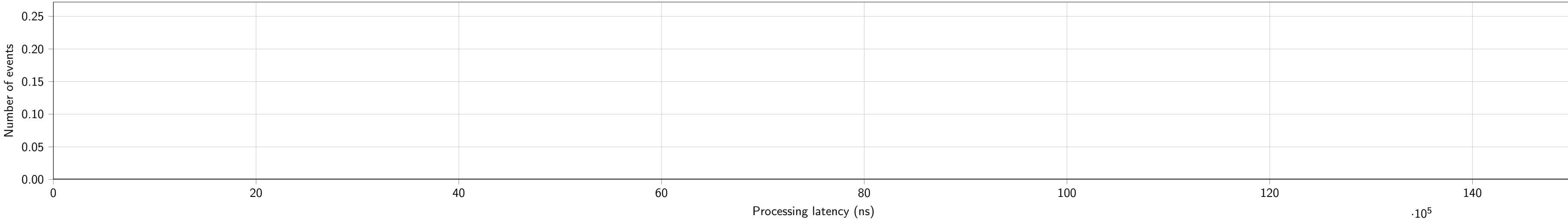
l2_multimac_01000000_mbit5200.histogram.csv: tx: 9.22mpps, 0.05stdDev; rx: 7.44mpps, 0.01stdDev



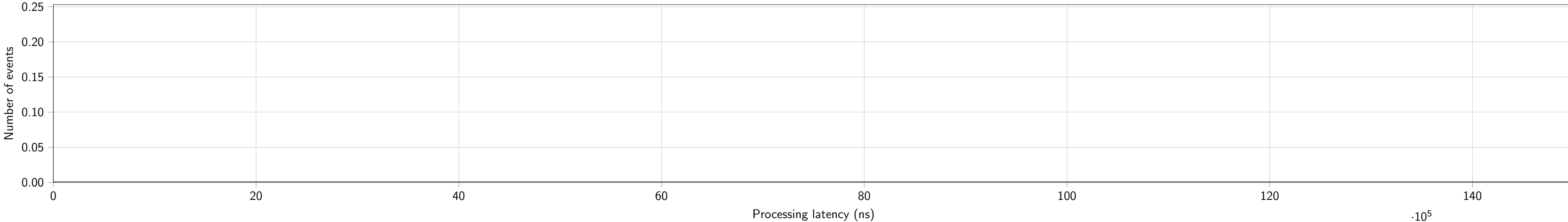
l2_multimac_01000000_mbit5600.histogram.csv: tx: 9.23mpps, 0.05stdDev; rx: 7.47mpps, 0.01stdDev



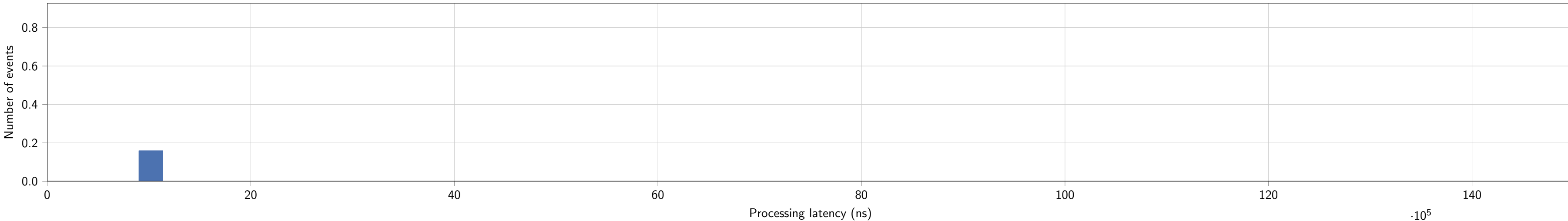
l2_multimac_01000000_mbit6000.histogram.csv: tx: 9.21mpps, 0.05stdDev; rx: 7.45mpps, 0.01stdDev

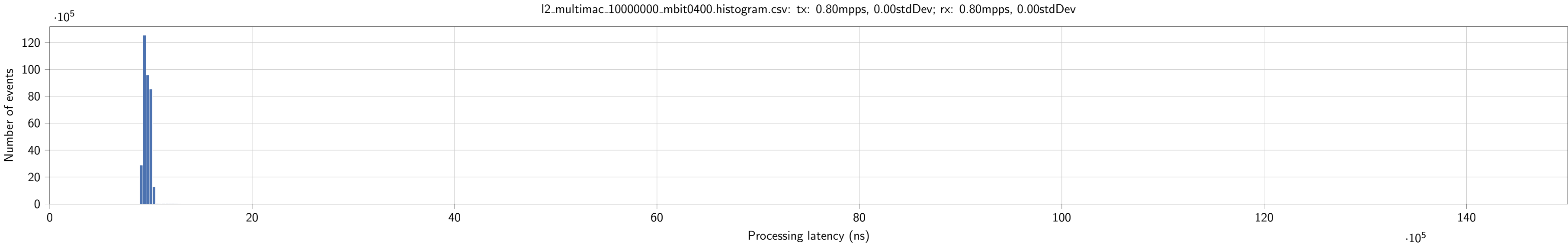


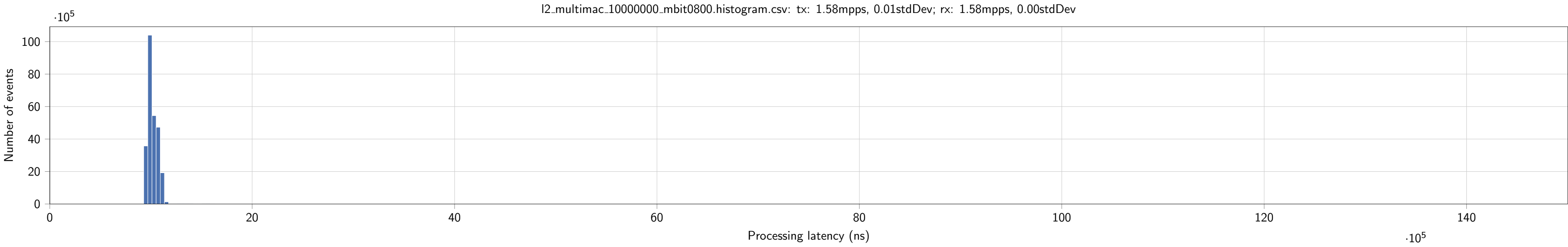
l2_multimac_01000000_mbit9000.histogram.csv: tx: 9.21mpps, 0.05stdDev; rx: 7.47mpps, 0.01stdDev

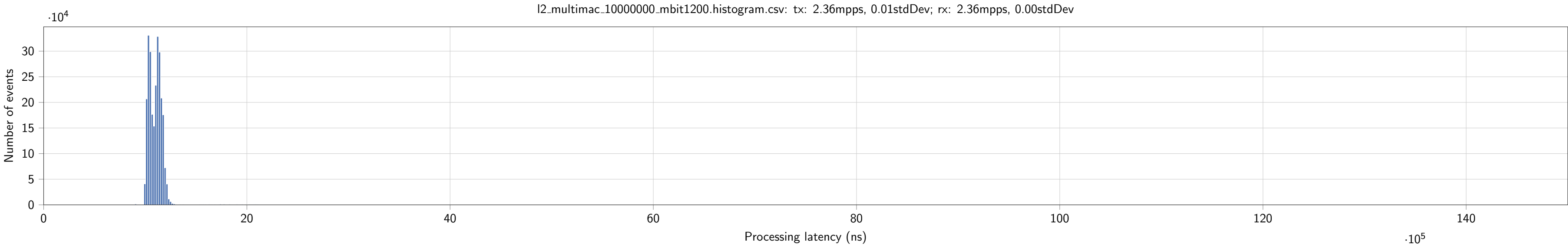


l2_multimac_10000000_mbit0000_final.histogram.csv: tx: 9.21mpps, 0.05stdDev; rx: 6.27mpps, 0.01stdDev









l2_multimac_10000000_mbit1600.histogram.csv: tx: 3.14mpps, 0.02stdDev; rx: 3.14mpps, 0.00stdDev

Number of events

50
40
30
20
10
0

$\cdot 10^4$

0

20

40

60

80

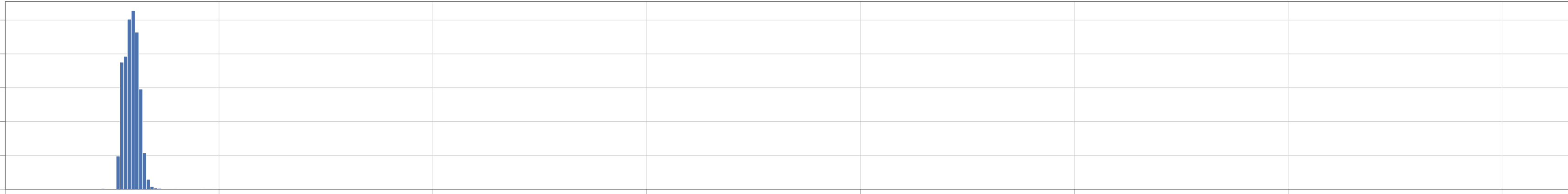
100

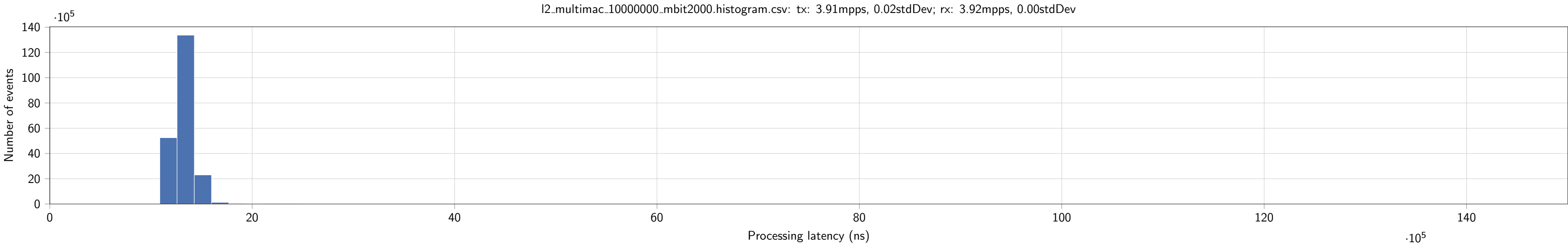
120

140

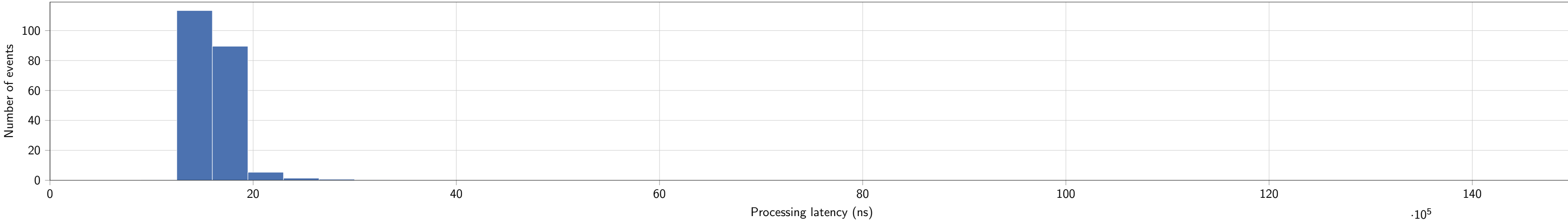
Processing latency (ns)

$\cdot 10^5$

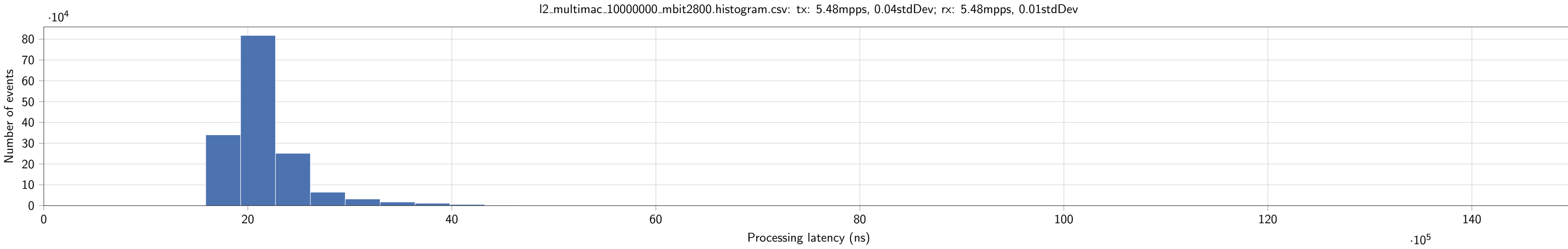




l2_multimac_10000000_mbit2400.histogram.csv: tx: 4.70mpps, 0.03stdDev; rx: 4.71mpps, 0.00stdDev

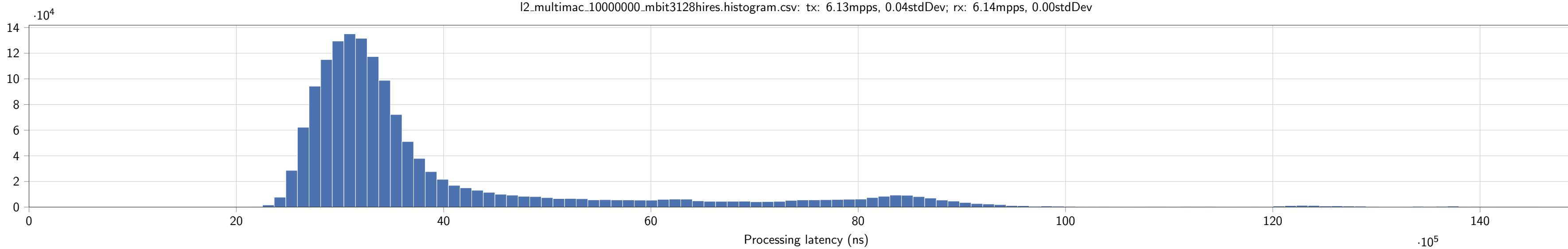


Number of events



l2_multimac_10000000_mbit3128hires.histogram.csv: tx: 6.13mpps, 0.04stdDev; rx: 6.14mpps, 0.00stdDev

Number of events



Number of events

 $\cdot 10^4$
17.5
15.0
12.5
10.0
7.5
5.0
2.5
0.0

0

20

40

60

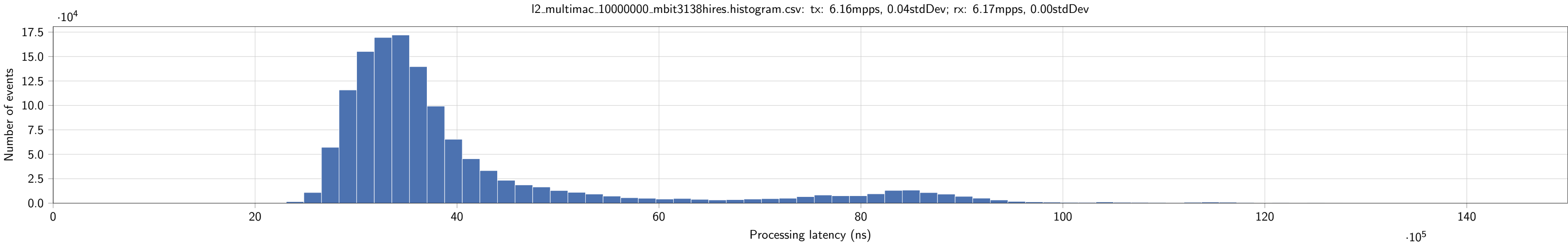
80

100

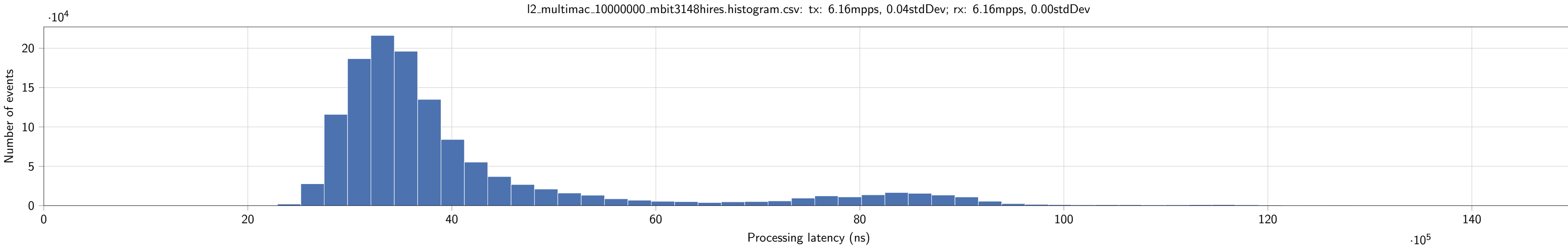
120

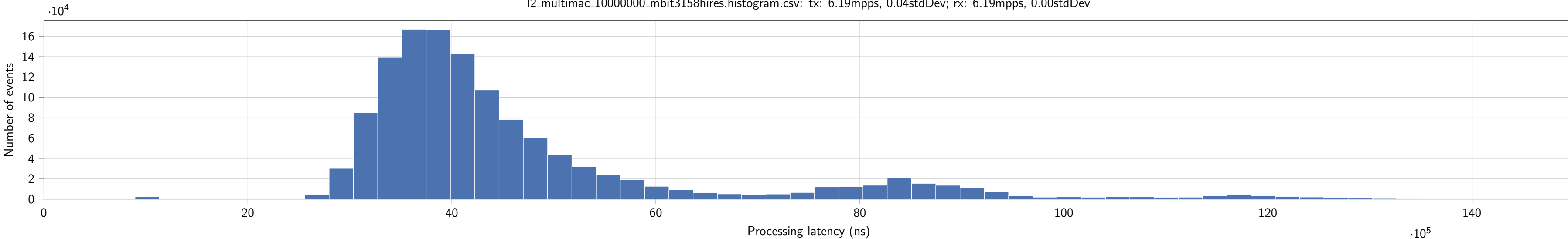
140

Processing latency (ns)

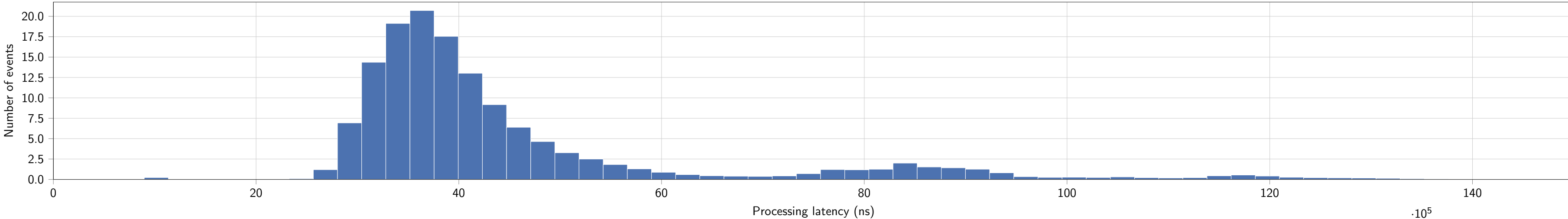
 $\cdot 10^5$ 

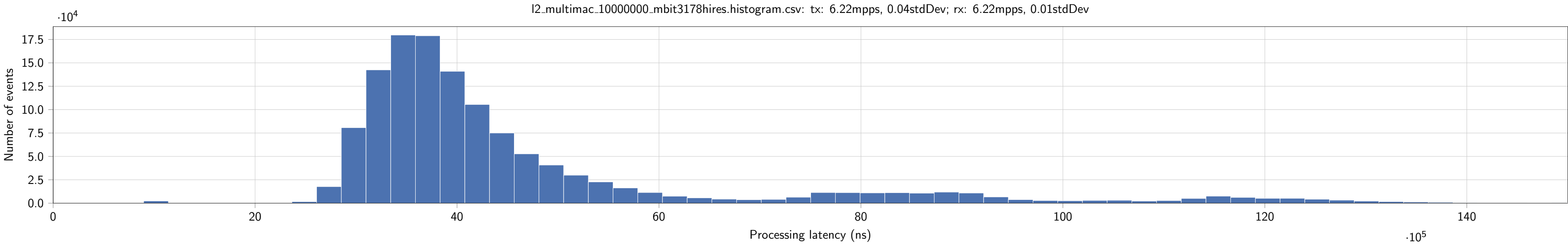
Number of events

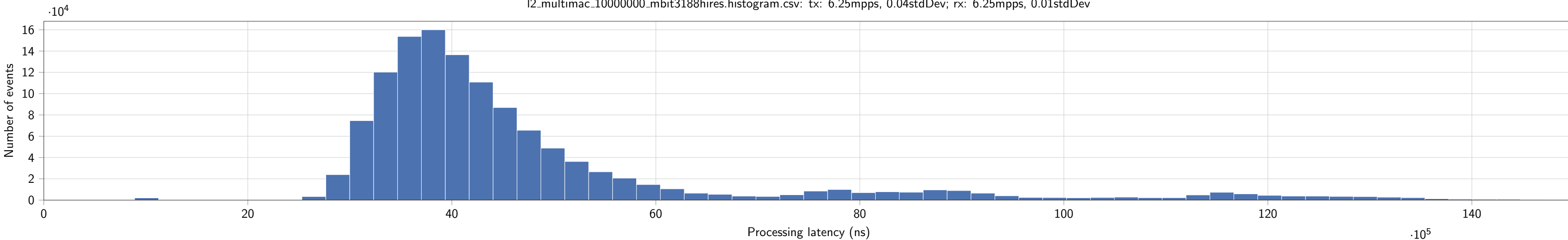




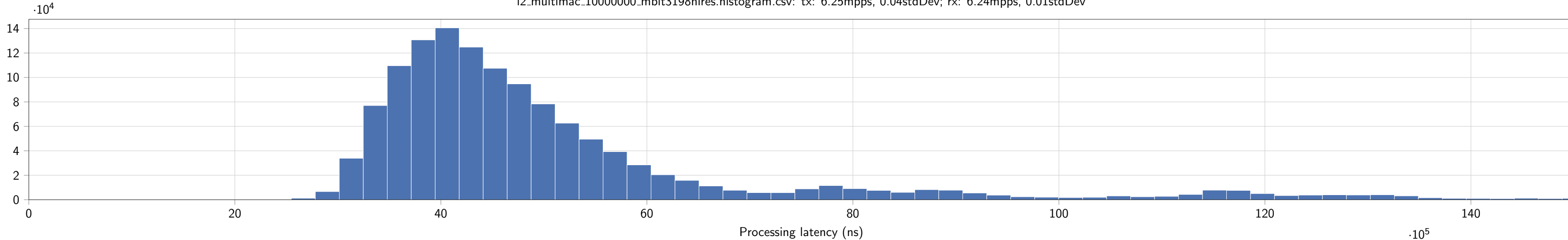
l2_multimac_10000000_mbit3168hires.histogram.csv: tx: 6.19mpps, 0.04stdDev; rx: 6.19mpps, 0.00stdDev

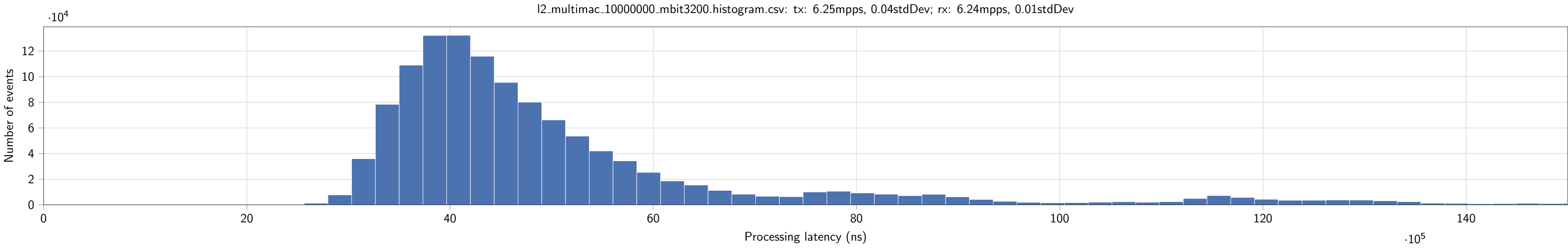


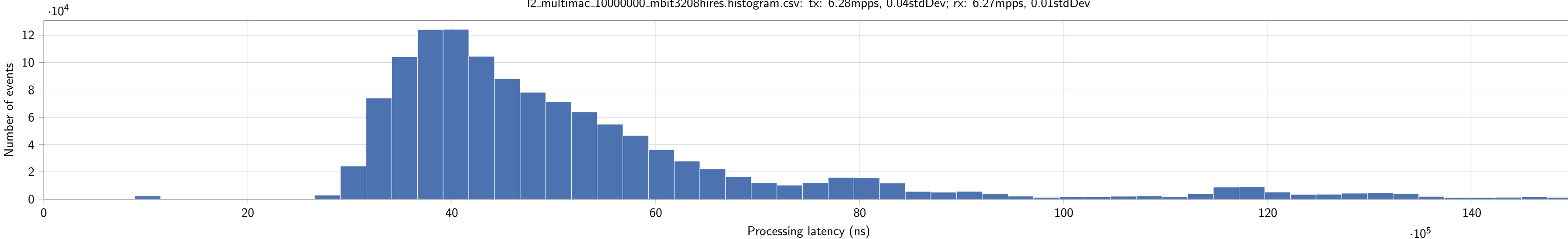




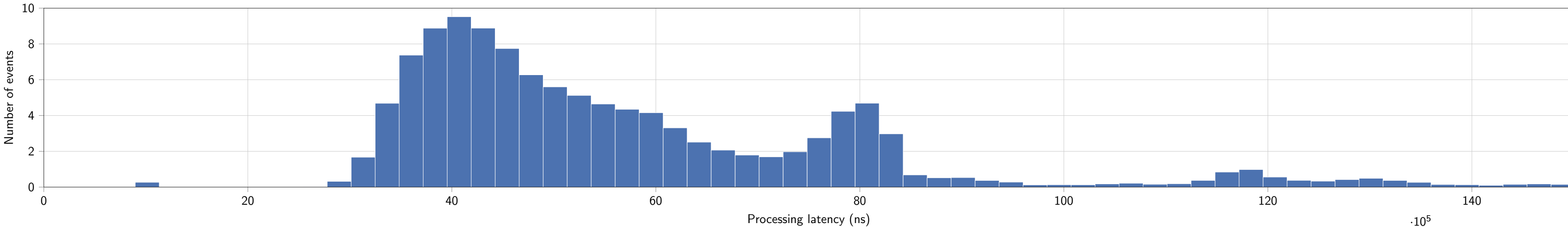
Number of events



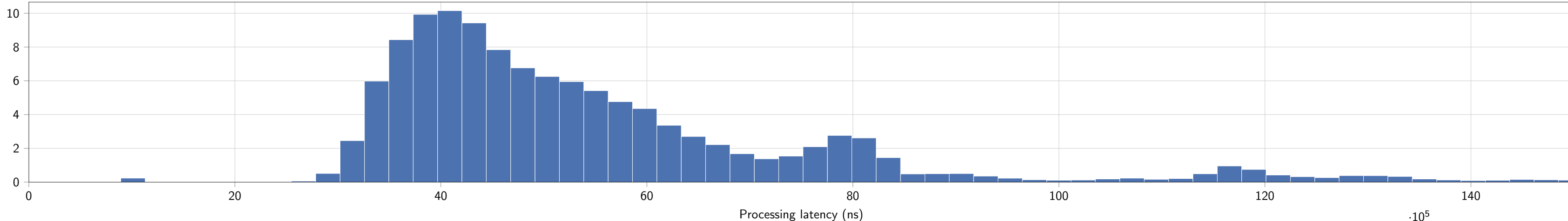




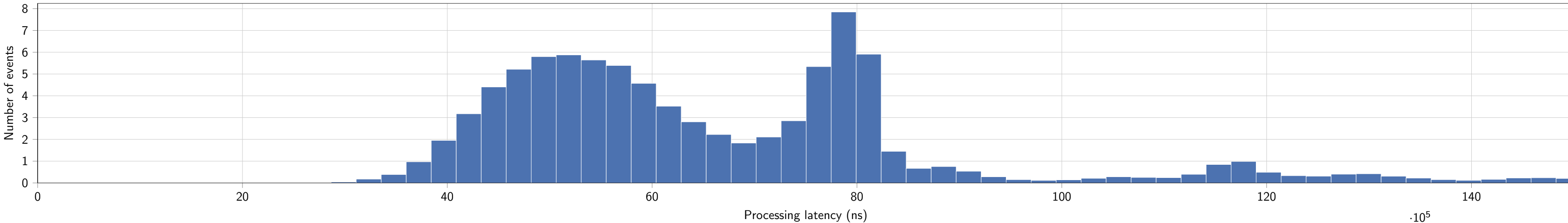
l2_multimac_10000000_mbit3218hires.histogram.csv: tx: 6.31mpps, 0.04stdDev; rx: 6.30mpps, 0.02stdDev



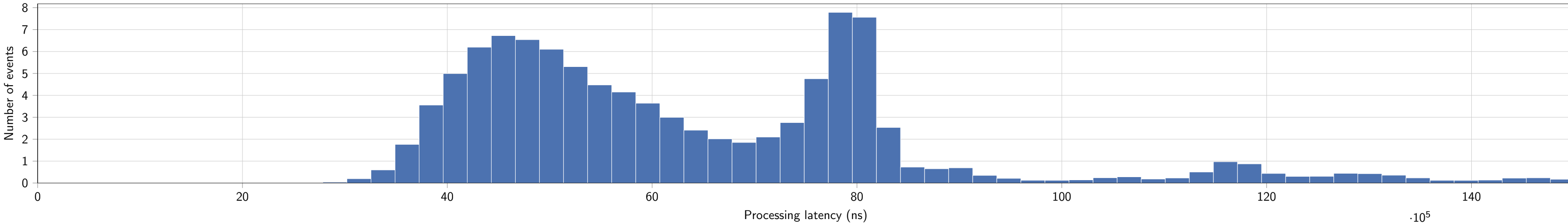
Number of events

 $\cdot 10^4$ 

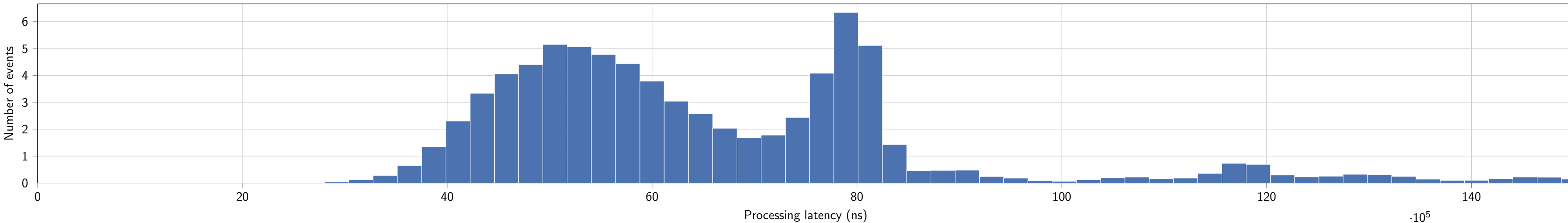
l2_multimac_10000000_mbit3238hires.histogram.csv: tx: 6.34mpps, 0.04stdDev; rx: 6.32mpps, 0.02stdDev



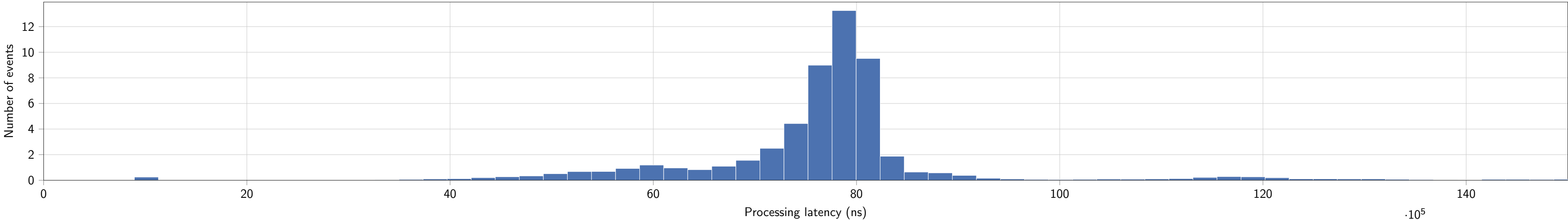
l2_multimac_10000000_mbit3248hires.histogram.csv: tx: 6.34mpps, 0.04stdDev; rx: 6.32mpps, 0.02stdDev



l2_multimac_10000000_mbit3258hires.histogram.csv: tx: 6.37mpps, 0.04stdDev; rx: 6.35mpps, 0.02stdDev

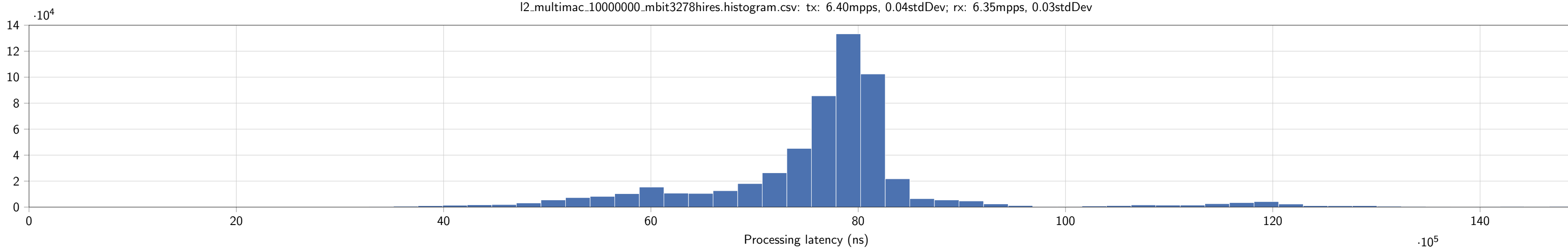


l2_multimac_10000000_mbit3268hires.histogram.csv: tx: 6.40mpps, 0.04stdDev; rx: 6.35mpps, 0.03stdDev

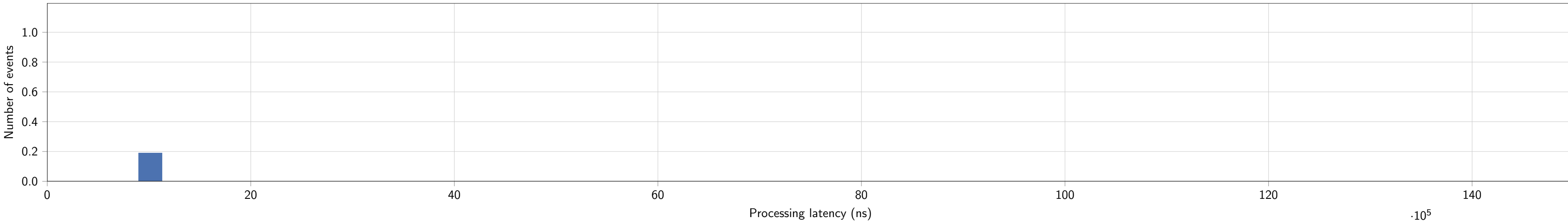


l2_multimac_10000000_mbit3278hires.histogram.csv: tx: 6.40mpps, 0.04stdDev; rx: 6.35mpps, 0.03stdDev

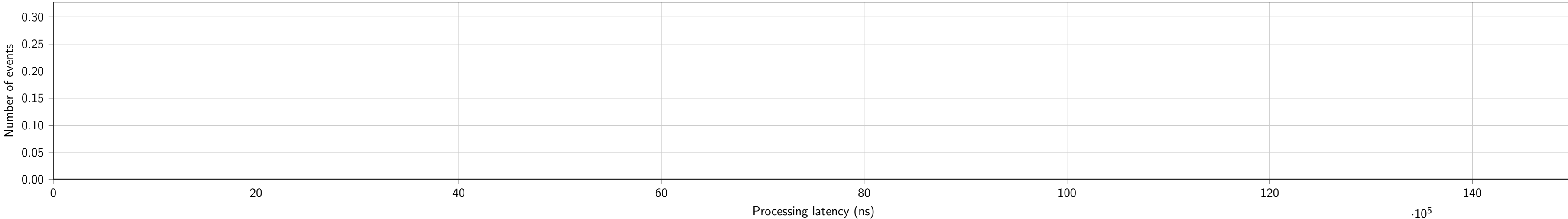
Number of events



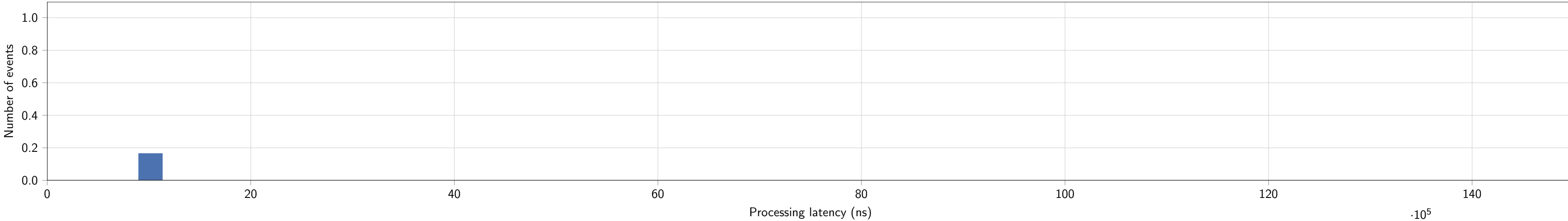
l2_multimac_10000000_mbit3600.histogram.csv: tx: 7.05mpps, 0.05stdDev; rx: 6.29mpps, 0.03stdDev



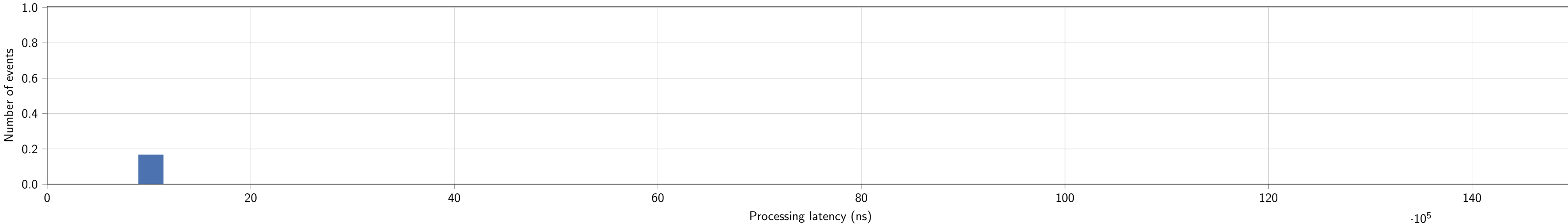
l2_multimac_10000000_mbit4000.histogram.csv: tx: 7.80mpps, 0.05stdDev; rx: 6.30mpps, 0.02stdDev



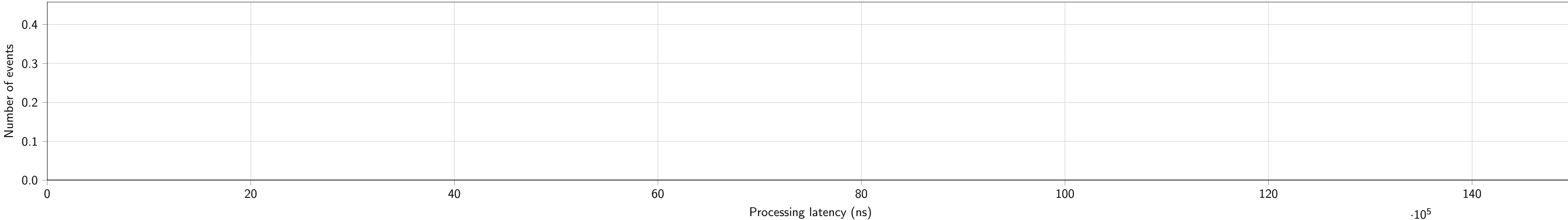
l2_multimac_10000000_mbit4400.histogram.csv: tx: 8.61mpps, 0.05stdDev; rx: 6.29mpps, 0.01stdDev



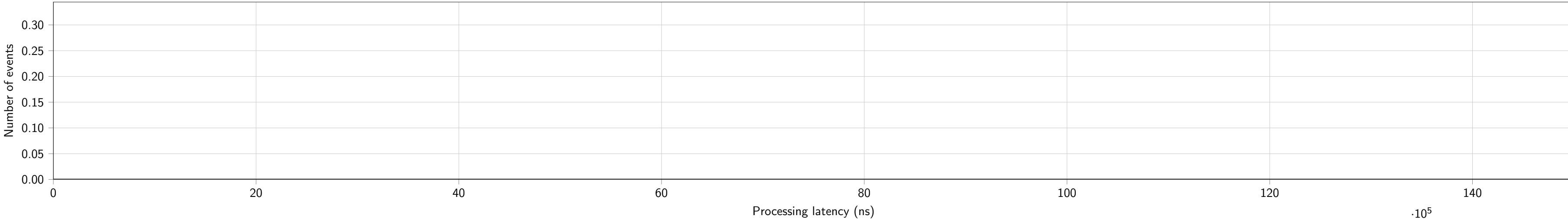
l2_multimac_10000000_mbit4800.histogram.csv: tx: 9.22mpps, 0.05stdDev; rx: 6.32mpps, 0.01stdDev



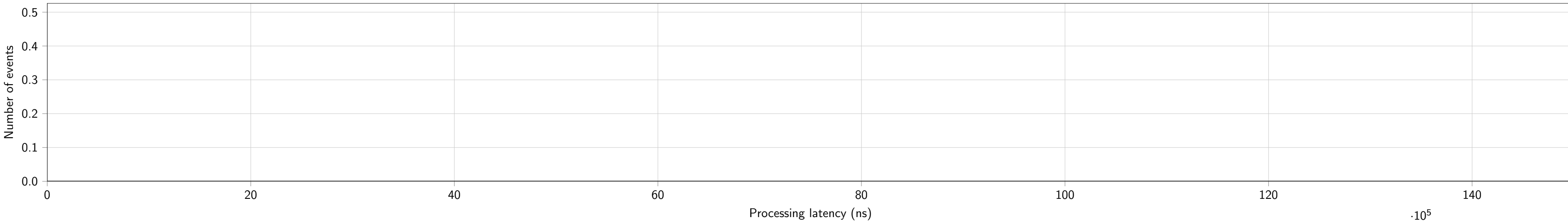
l2_multimac_10000000_mbit5200.histogram.csv: tx: 9.19mpps, 0.06stdDev; rx: 6.32mpps, 0.01stdDev



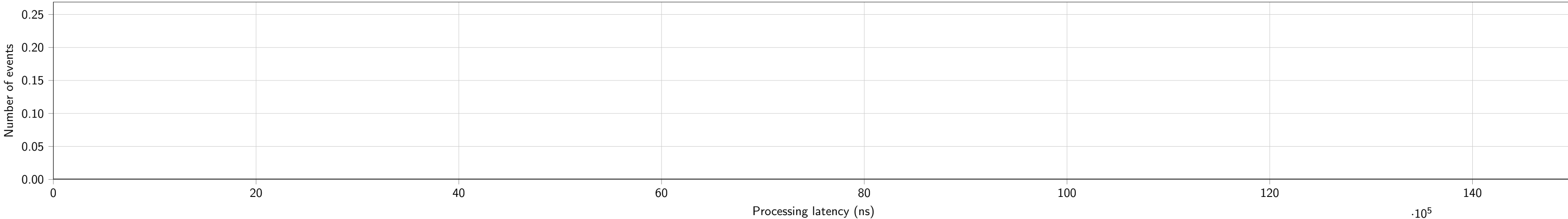
l2_multimac_10000000_mbit5600.histogram.csv: tx: 9.23mpps, 0.05stdDev; rx: 6.30mpps, 0.01stdDev



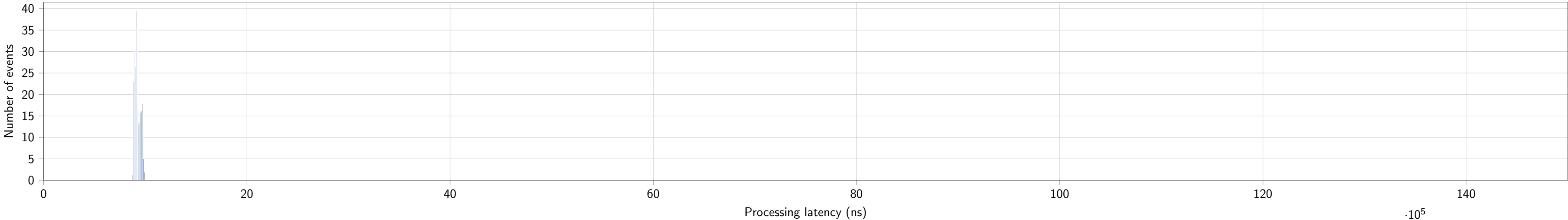
l2_multimac_10000000_mbit6000.histogram.csv: tx: 9.21mpps, 0.05stdDev; rx: 6.30mpps, 0.01stdDev

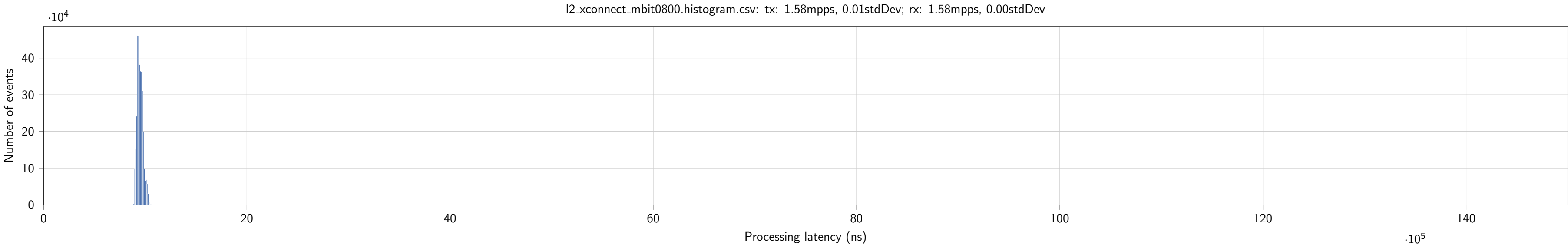


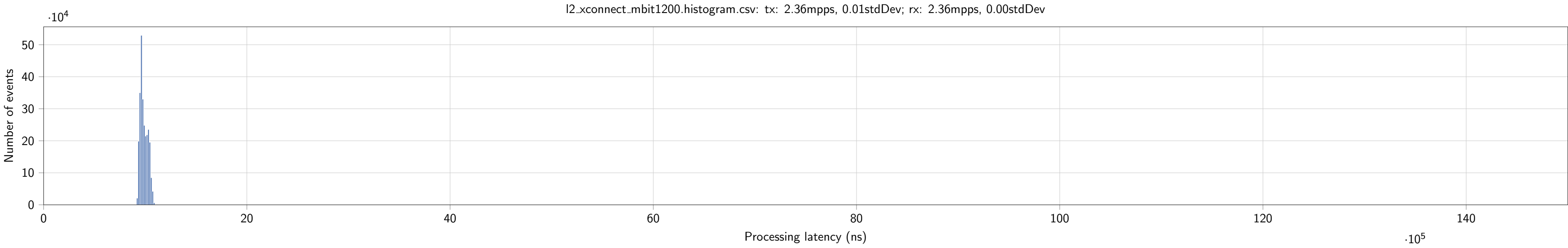
l2_multimac_10000000_mbit9000.histogram.csv: tx: 9.23mpps, 0.05stdDev; rx: 6.30mpps, 0.01stdDev

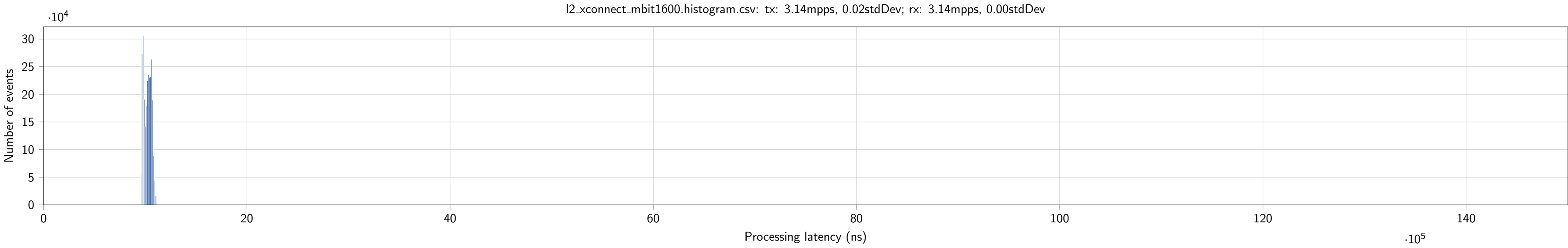


l2_xconnect_mbit0400.histogram.csv: tx: 0.80mpps, 0.00stdDev; rx: 0.80mpps, 0.00stdDev



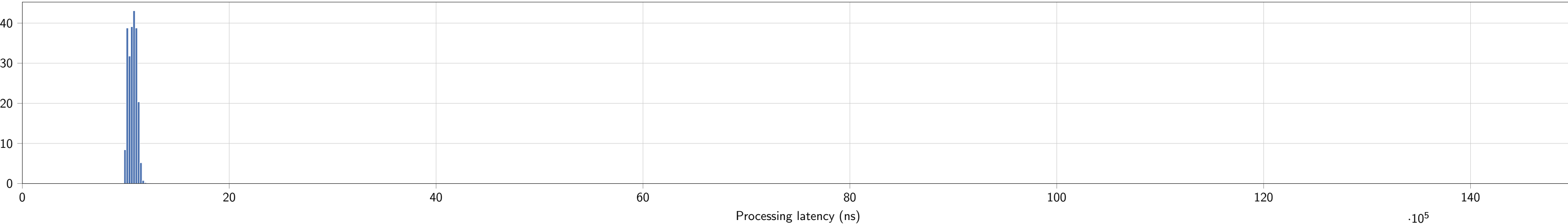






l2_xconnect_mbit2000.histogram.csv: tx: 3.91mpps, 0.02stdDev; rx: 3.92mpps, 0.00stdDev

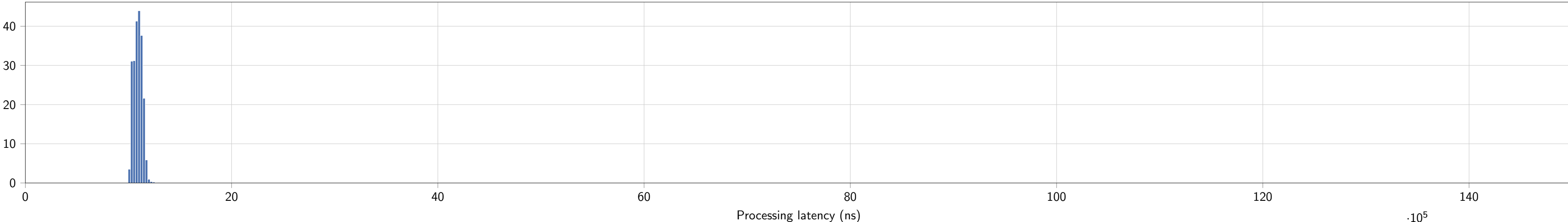
Number of events



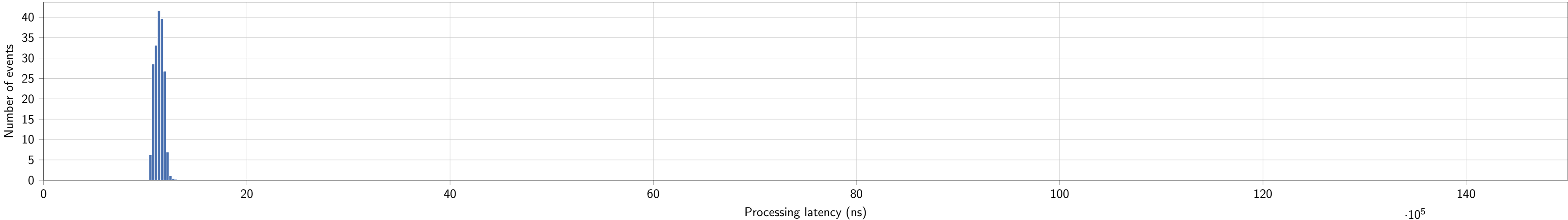
l2_xconnect_mbit2400.histogram.csv: tx: 4.71mpps, 0.02stdDev; rx: 4.71mpps, 0.00stdDev

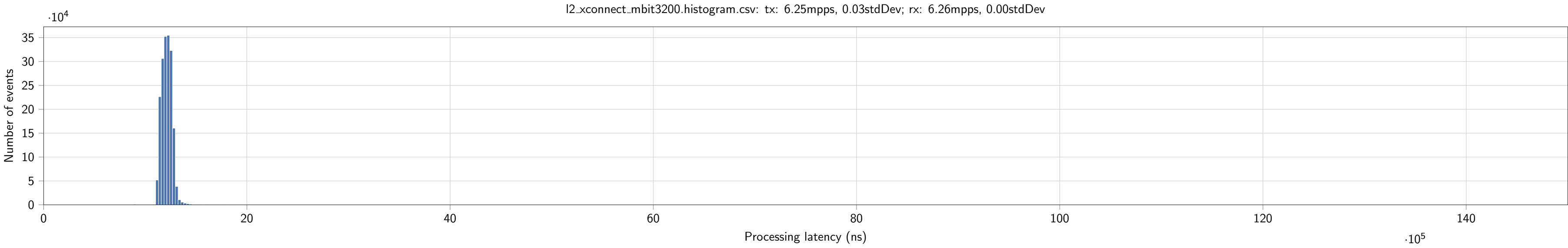
Number of events

$\cdot 10^4$

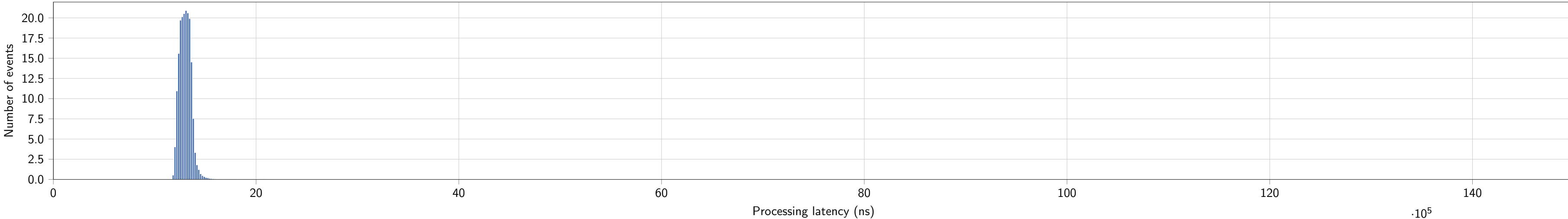


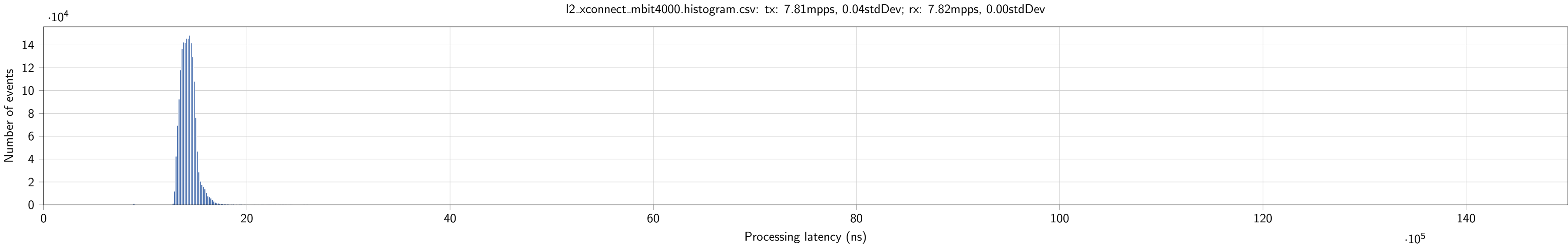
l2_xconnect_mbit2800.histogram.csv: tx: 5.49mpps, 0.03stdDev; rx: 5.49mpps, 0.00stdDev



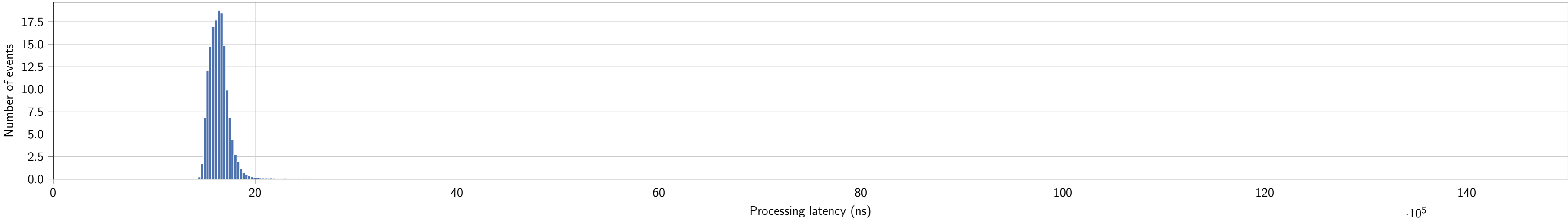


l2_xconnect_mbit3600.histogram.csv: tx: 7.06mpps, 0.03stdDev; rx: 7.07mpps, 0.00stdDev

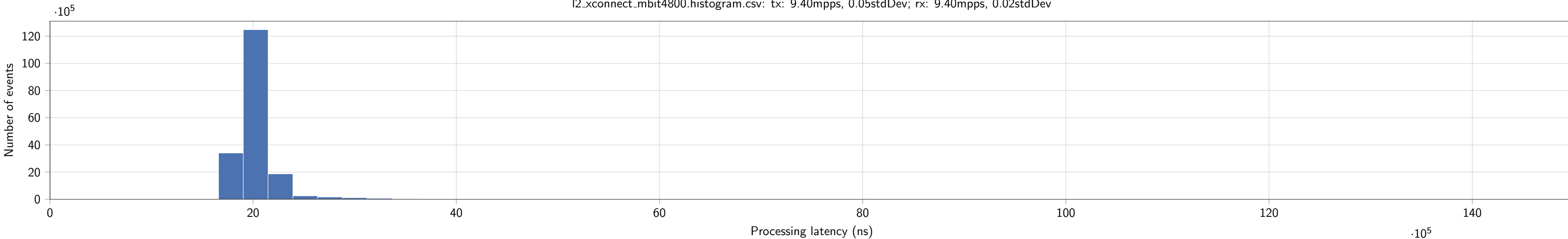




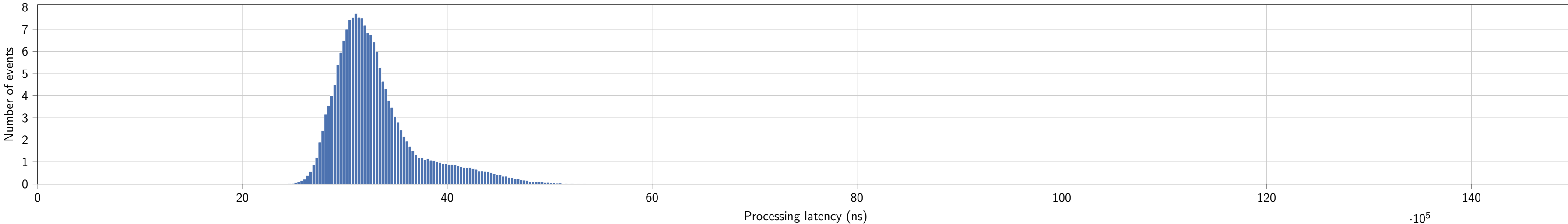
l2_xconnect_mbit4400.histogram.csv: tx: 8.62mpps, 0.05stdDev; rx: 8.63mpps, 0.00stdDev



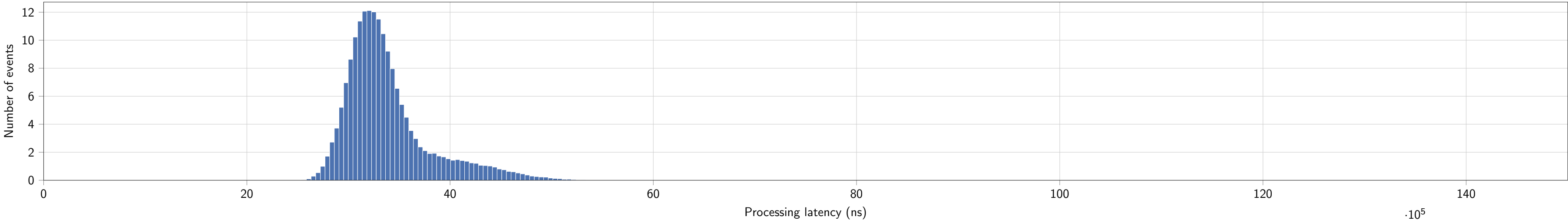
l2_xconnect_mbit4800.histogram.csv: tx: 9.40mpps, 0.05stdDev; rx: 9.40mpps, 0.02stdDev



l2_xconnect_mbit5177hires.histogram.csv: tx: 10.16mpps, 0.05stdDev; rx: 10.17mpps, 0.00stdDev



l2_xconnect_mbit5187hires.histogram.csv: tx: 10.16mpps, 0.05stdDev; rx: 10.17mpps, 0.00stdDev



l2_xconnect_mbit5197hires.histogram.csv: tx: 10.16mpps, 0.05stdDev; rx: 10.17mpps, 0.00stdDev

Number of events

$\cdot 10^4$

12
10
8
6
4
2
0

0

20

40

60

80

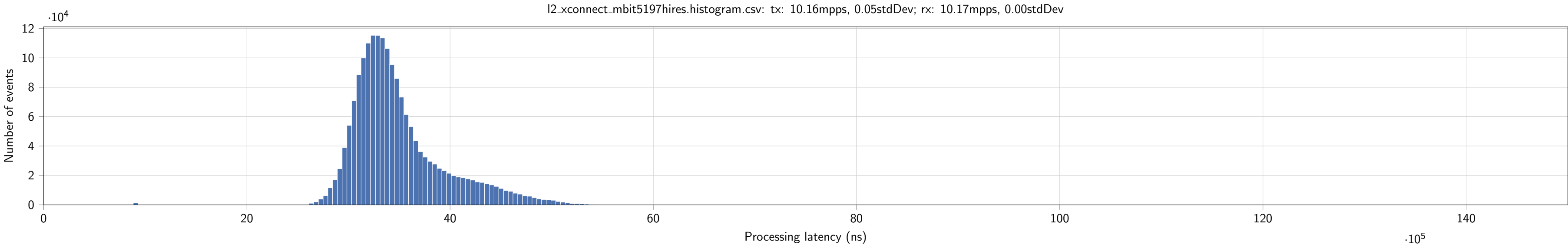
100

120

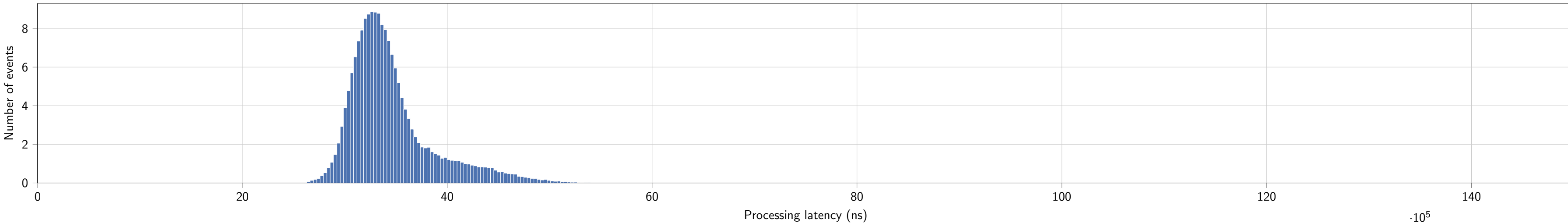
140

Processing latency (ns)

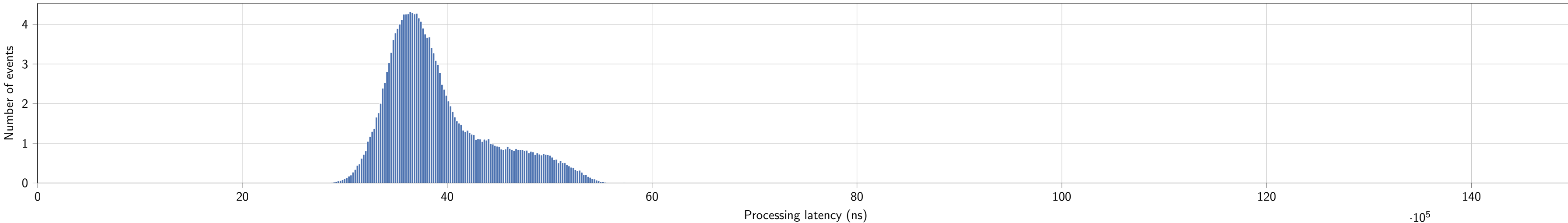
$\cdot 10^5$



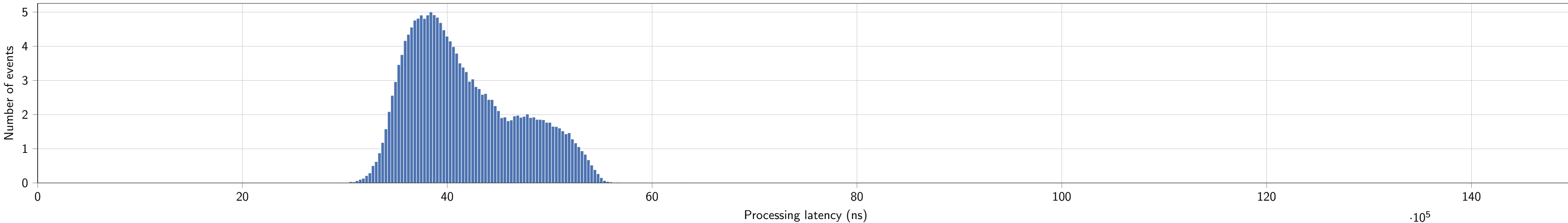
l2_xconnect_mbit5200.histogram.csv: tx: 10.16mpps, 0.05stdDev; rx: 10.17mpps, 0.00stdDev

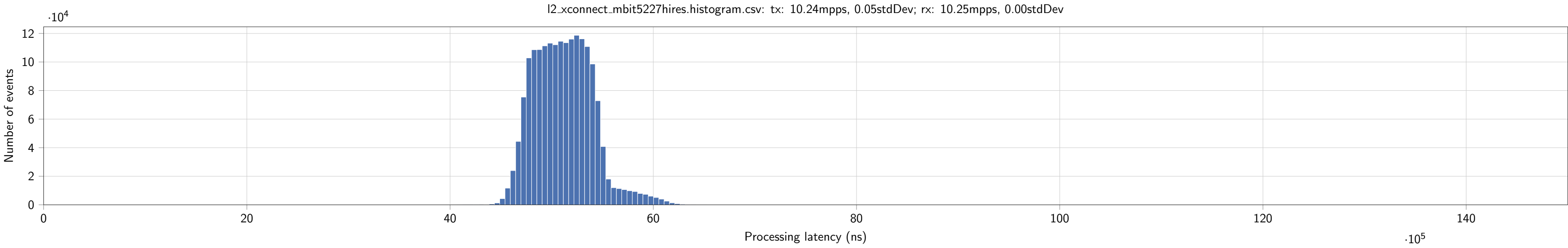


l2_xconnect_mbit5207hires.histogram.csv: tx: 10.24mpps, 0.05stdDev; rx: 10.25mpps, 0.00stdDev

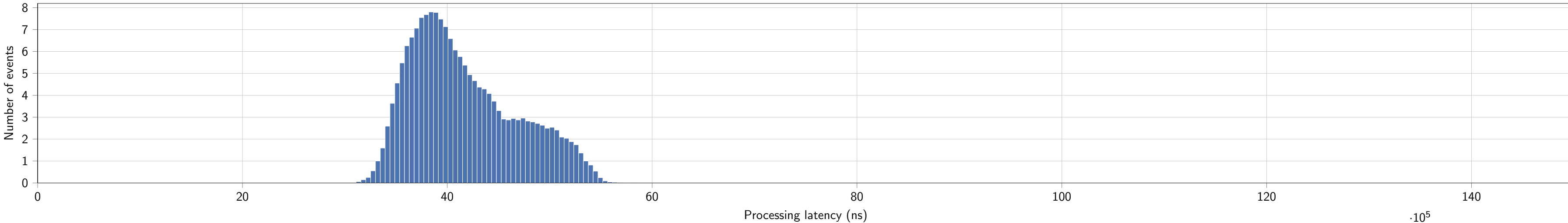


l2_xconnect_mbit5217hires.histogram.csv: tx: 10.24mpps, 0.05stdDev; rx: 10.25mpps, 0.00stdDev

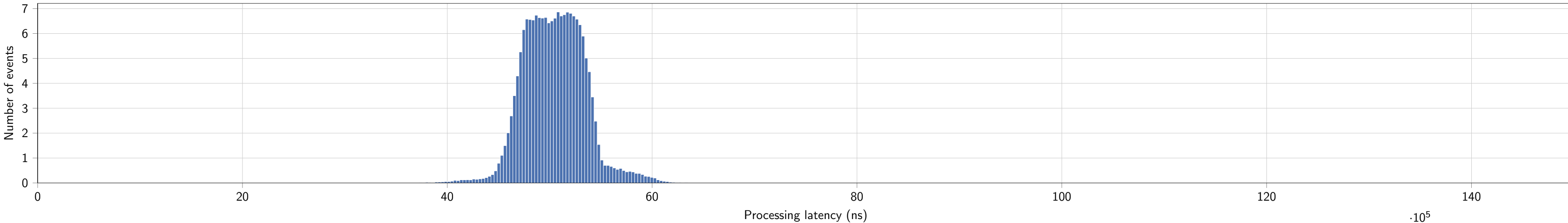




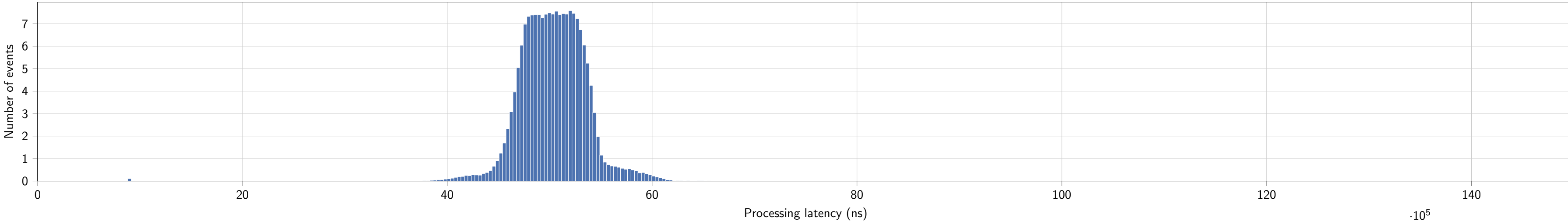
l2_xconnect_mbit5237hires.histogram.csv: tx: 10.24mpps, 0.05stdDev; rx: 10.25mpps, 0.00stdDev



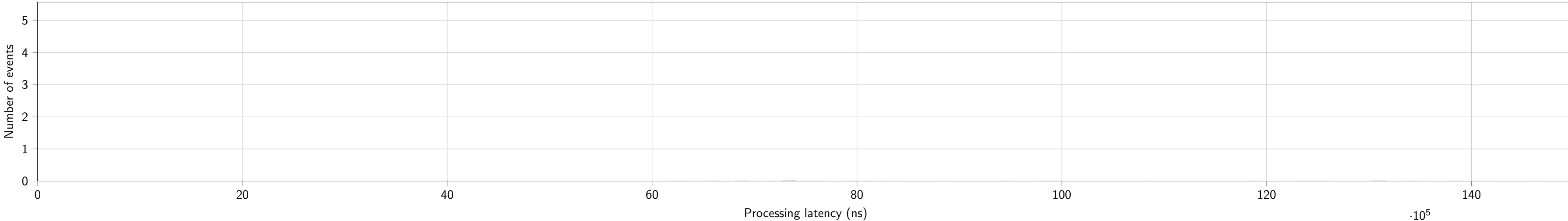
l2_xconnect_mbit5247_final.histogram.csv: tx: 10.33mpps, 0.05stdDev; rx: 10.34mpps, 0.00stdDev



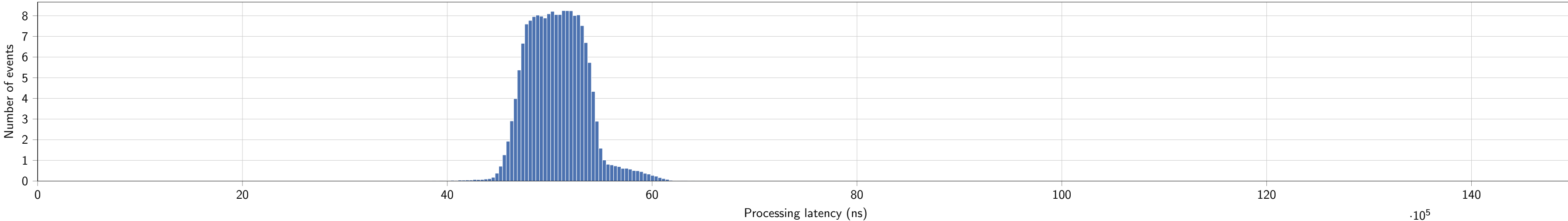
l2_xconnect_mbit5247hires.histogram.csv: tx: 10.33mpps, 0.05stdDev; rx: 10.34mpps, 0.00stdDev



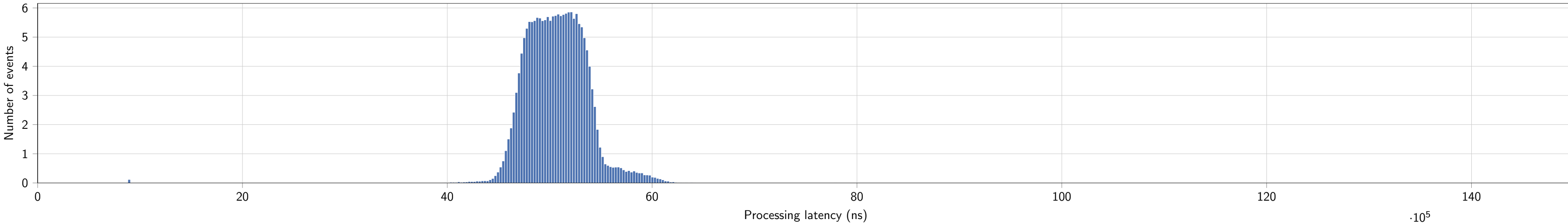
l2_xconnect_mbit5257hires.histogram.csv: tx: 10.32mpps, 0.05stdDev; rx: 10.32mpps, 0.00stdDev



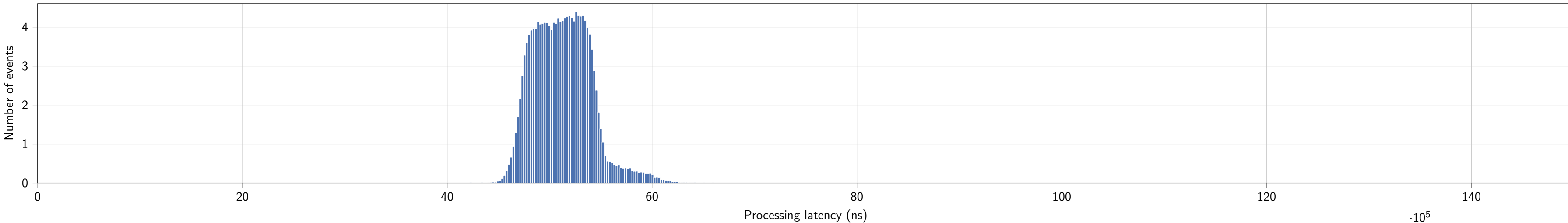
l2_xconnect_mbit5267hires.histogram.csv: tx: 10.33mpps, 0.05stdDev; rx: 10.34mpps, 0.00stdDev



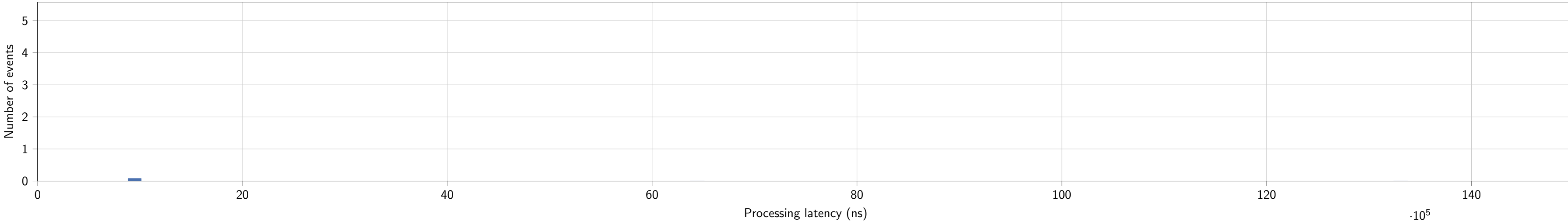
l2_xconnect_mbit5277hires.histogram.csv: tx: 10.33mpps, 0.05stdDev; rx: 10.34mpps, 0.00stdDev



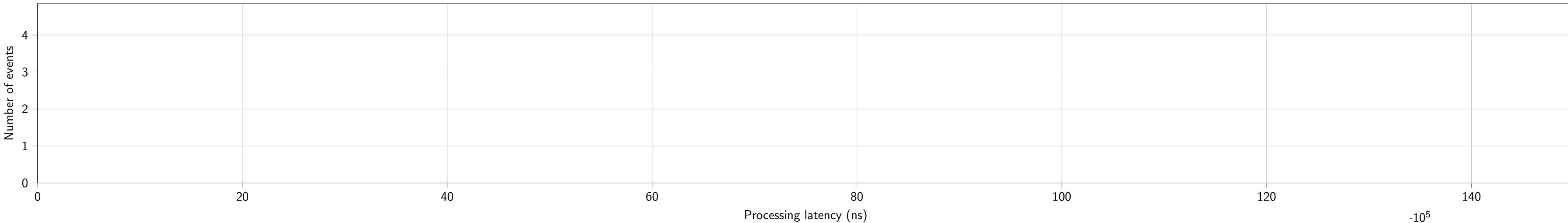
l2_xconnect_mbit5287hires.histogram.csv: tx: 10.33mpps, 0.05stdDev; rx: 10.34mpps, 0.00stdDev



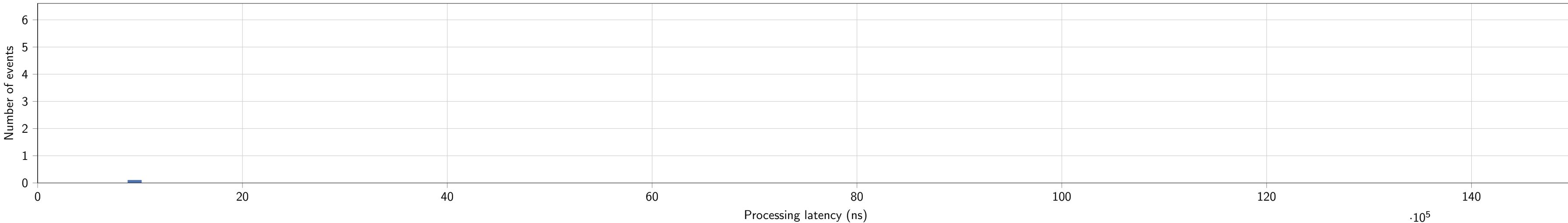
l2_xconnect_mbit5297hires.histogram.csv: tx: 10.41mpps, 0.05stdDev; rx: 10.38mpps, 0.00stdDev



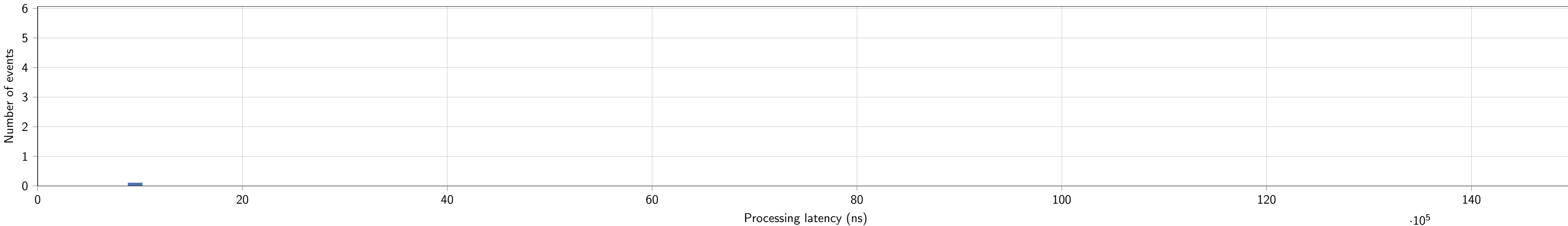
l2_xconnect_mbit5307hires.histogram.csv: tx: 10.41mpps, 0.05stdDev; rx: 10.34mpps, 0.00stdDev



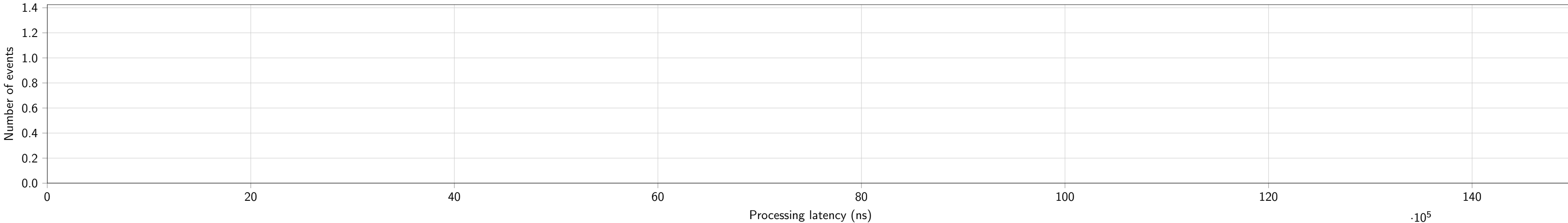
l2_xconnect_mbit5317hires.histogram.csv: tx: 10.41mpps, 0.05stdDev; rx: 10.38mpps, 0.00stdDev



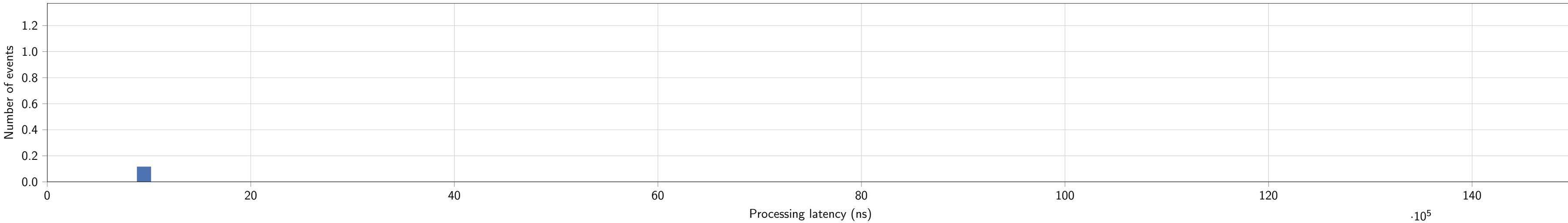
l2_xconnect_mbit5327hires.histogram.csv: tx: 10.41mpps, 0.05stdDev; rx: 10.36mpps, 0.00stdDev



l2_xconnect_mbit5600.histogram.csv: tx: 10.95mpps, 0.05stdDev; rx: 10.37mpps, 0.00stdDev



l2_xconnect_mbit6000.histogram.csv: tx: 11.78mpps, 0.06stdDev; rx: 10.34mpps, 0.00stdDev



l2_xconnect_mbit9000.histogram.csv: tx: 14.86mpps, 0.08stdDev; rx: 10.31mpps, 0.00stdDev

