Digital IC Design

Exercise 5
Supplement

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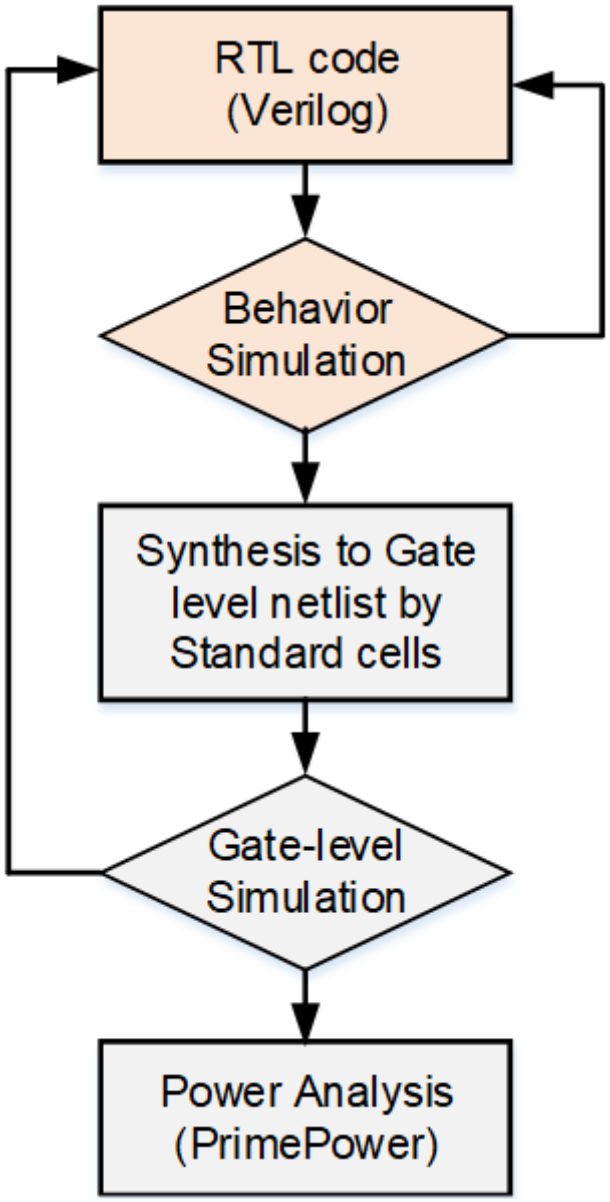
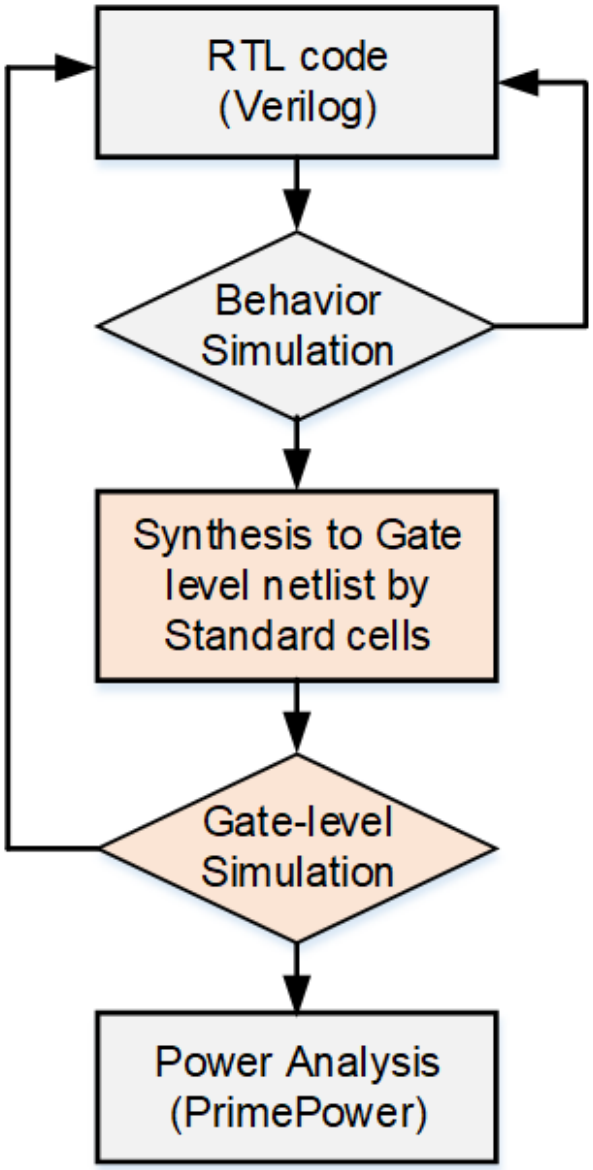
Construct 3x3 convolution kernel



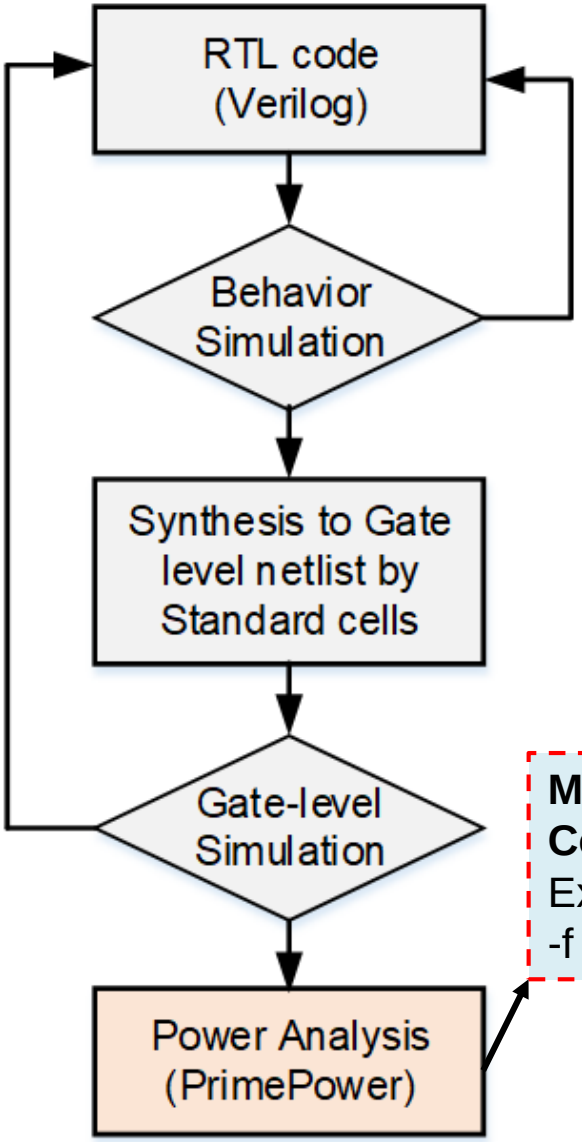
- In this exercise, TA will provide the 3x3 convolution kernel & Pattern
  - w/o using clock gating
  - w/ using clock gating

Synthesis and verify 3x3 convolution kernel



- Synthesis the 3x3 convolution kernel.
  - w/o using clock gating
  - w/ using clock gating **(Done by TA)**
- Run the gate level simulation of both 3x3 convolution kernels to verify the function and generate the **.fsdb for power measurement.**

Measure power of 3x3 convolution kernel



- Use the PrimePower to measure the power of 3x3 convolution kernels

Measure power (PrimePower)
Command:
Export SYNOPSYS_LC_ROOT=SYNOPSYS_LC_ROOTpt_shell -f ptpx.tcl | tee CORE_power.log

Notes for PrimePower

- The warnings and errors are caused by the missing information of asap 7nm cell library
  - The warning and errors can be ignored

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Warning: No timing arc in cell 'DP_OP_42J1_122_5662_U2398(FAx1_ASAP7_75t_R)' with condition '(A&~B&~CI)' from pin 'A' to pin 'SN'. (PTE-011)
Warning: No timing arc in cell 'DP_OP_42J1_122_5662_U2398(FAx1_ASAP7_75t_R)' with condition '(~A&B&CI)' from pin 'A' to pin 'SN'. (PTE-011)
Warning: No timing arc in cell 'DP_OP_42J1_122_5662_U2398(FAx1_ASAP7_75t_R)' with condition '(~A&B&~CI)' from pin 'A' to pin 'SN'. (PTE-011)
Warning: No timing arc in cell 'DP_OP_42J1_122_5662_U2398(FAx1_ASAP7_75t_R)' with condition '(~A&~B&CI)' from pin 'A' to pin 'SN'. (PTE-011)
Warning: No timing arc in cell 'DP_OP_42J1_122_5662_U2398(FAx1_ASAP7_75t_R)' with condition '(A&B&~CI)' from pin 'B' to pin 'SN'. (PTE-011)
Warning: No timing arc in cell 'DP_OP_42J1_122_5662_U2398(FAx1_ASAP7_75t_R)' with condition '(A&~B&CI)' from pin 'B' to pin 'SN'. (PTE-011)
Warning: No timing arc in cell 'DP_OP_42J1_122_5662_U2398(FAx1_ASAP7_75t_R)' with condition '(A&~B&~CI)' from pin 'B' to pin 'SN'. (PTE-011)
Warning: No timing arc in cell 'DP_OP_42J1_122_5662_U2398(FAx1_ASAP7_75t_R)' with condition '(~A&B&CI)' from pin 'B' to pin 'SN'. (PTE-011)
Warning: No timing arc in cell 'DP_OP_42J1_122_5662_U2398(FAx1_ASAP7_75t_R)' with condition '(~A&B&~CI)' from pin 'B' to pin 'SN'. (PTE-011)
Warning: No timing arc in cell 'DP_OP_42J1_122_5662_U2398(FAx1_ASAP7_75t_R)' with condition '(~A&~B&CI)' from pin 'B' to pin 'SN'. (PTE-011)
Warning: No timing arc in cell 'DP_OP_42J1_122_5662_U2398(FAx1_ASAP7_75t_R)' with condition '(A&B&~CI)' from pin 'CI' to pin 'SN'. (PTE-011)
Warning: No timing arc in cell 'DP_OP_42J1_122_5662_U2398(FAx1_ASAP7_75t_R)' with condition '(A&~B&CI)' from pin 'CI' to pin 'SN'. (PTE-011)
Warning: No timing arc in cell 'DP_OP_42J1_122_5662_U2398(FAx1_ASAP7_75t_R)' with condition '(A&~B&~CI)' from pin 'CI' to pin 'SN'. (PTE-011)
Warning: No timing arc in cell 'DP_OP_42J1_122_5662_U2398(FAx1_ASAP7_75t_R)' with condition '(~A&B&CI)' from pin 'CI' to pin 'SN'. (PTE-011)
Warning: No timing arc in cell 'DP_OP_42J1_122_5662_U2398(FAx1_ASAP7_75t_R)' with condition '(~A&B&~CI)' from pin 'CI' to pin 'SN'. (PTE-011)
Warning: No timing arc in cell 'DP_OP_42J1_122_5662_U2398(FAx1_ASAP7_75t_R)' with condition '(~A&~B&CI)' from pin 'CI' to pin 'SN'. (PTE-011)
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Error: No net timing arc from pin 'GATED_CG_U8/RST_N' to pin 'U3128/A'. (PTE-014)
Error: No net timing arc from pin 'GATED_CG_U7/RST_N' to pin 'U3128/A'. (PTE-014)
Error: No net timing arc from pin 'GATED_CG_U6/RST_N' to pin 'U3128/A'. (PTE-014)
Error: No net timing arc from pin 'GATED_CG_U5/RST_N' to pin 'U3128/A'. (PTE-014)
Error: No net timing arc from pin 'GATED_CG_U4/RST_N' to pin 'U3128/A'. (PTE-014)
Error: No net timing arc from pin 'GATED_CG_U3/RST_N' to pin 'U3128/A'. (PTE-014)
Error: No net timing arc from pin 'GATED_CG_U2/RST_N' to pin 'U3128/A'. (PTE-014)
Error: No net timing arc from pin 'GATED_CG_U1/RST_N' to pin 'U3128/A'. (PTE-014)
Error: No net timing arc from pin 'GATED_CG_U0/RST_N' to pin 'U3128/A'. (PTE-014)
Error: No net timing arc from pin 'GATED_CG_U9/CLOCK_GATED' to pin 'Reg_Weight_in_9_reg_0_/CLK'. (PTE-014)
Error: No net timing arc from pin 'GATED_CG_U9/CLOCK_GATED' to pin 'Reg_Weight_in_9_reg_1_/CLK'. (PTE-014)
Error: No net timing arc from pin 'GATED_CG_U9/CLOCK_GATED' to pin 'Reg_Weight_in_9_reg_2_/CLK'. (PTE-014)
Error: No net timing arc from pin 'GATED_CG_U9/CLOCK_GATED' to pin 'Reg_Weight_in_9_reg_3_/CLK'. (PTE-014)
Error: No net timing arc from pin 'GATED_CG_U9/CLOCK_GATED' to pin 'Reg_Weight_in_9_reg_4_/CLK'. (PTE-014)
Error: No net timing arc from pin 'GATED_CG_U9/CLOCK_GATED' to pin 'Reg_Weight_in_9_reg_5_/CLK'. (PTE-014)
Error: No net timing arc from pin 'GATED_CG_U9/CLOCK_GATED' to pin 'Reg_Weight_in_9_reg_6_/CLK'. (PTE-014)
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The asap 7nm cell library do not have the gating cells → The gating cells are constructed by TA
Therefore, the cell library do not have the timing information