Digital IC Design

Exercise 5
Clock Gating

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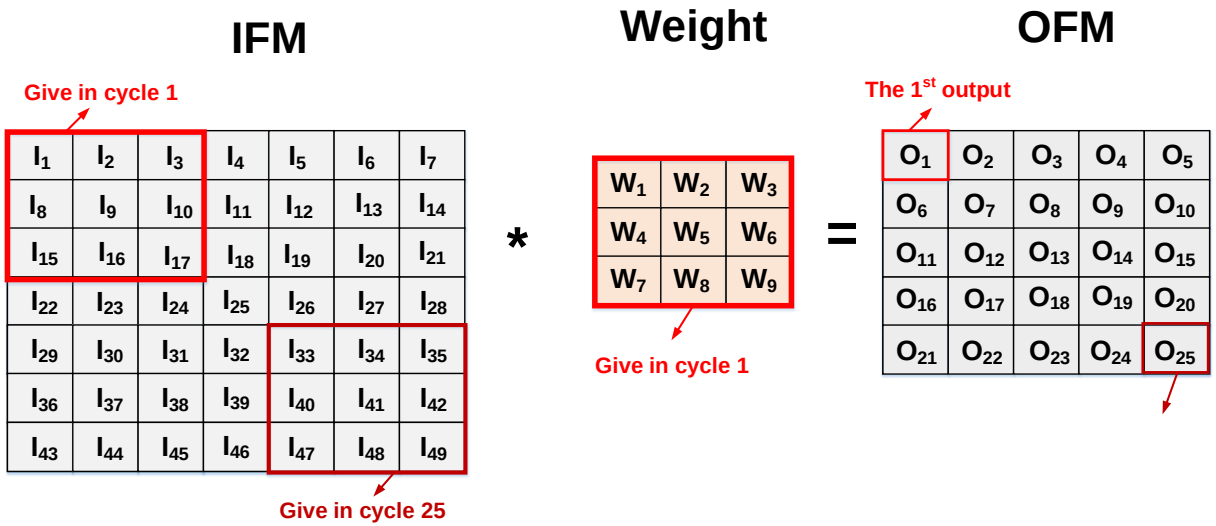
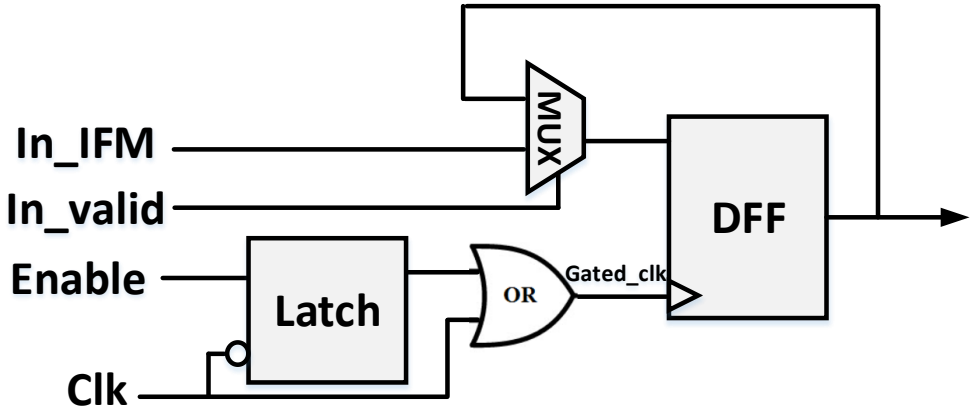
Power Analysis of sequential circuits

- Use the PrimePower to measure the power of a 3x3 convolution kernel provided by TA
  - Using clock gating
  - Without using clock gating
- Draw the architectures of 3x3 convolution kernels, and analysis and discuss the **power consumption** & **critical path** when using and without using clock gating.

Example

- In_IFM = 0 → Enable = 1
- In_IFM != 0 → Enable = 0





Submission of Exerice-5

- Please upload the following files
  - Due day: PM 11:55 on 12/29
  - Report.pdf