Digital IC Design

Final Team Project
128-bit Adder Tree

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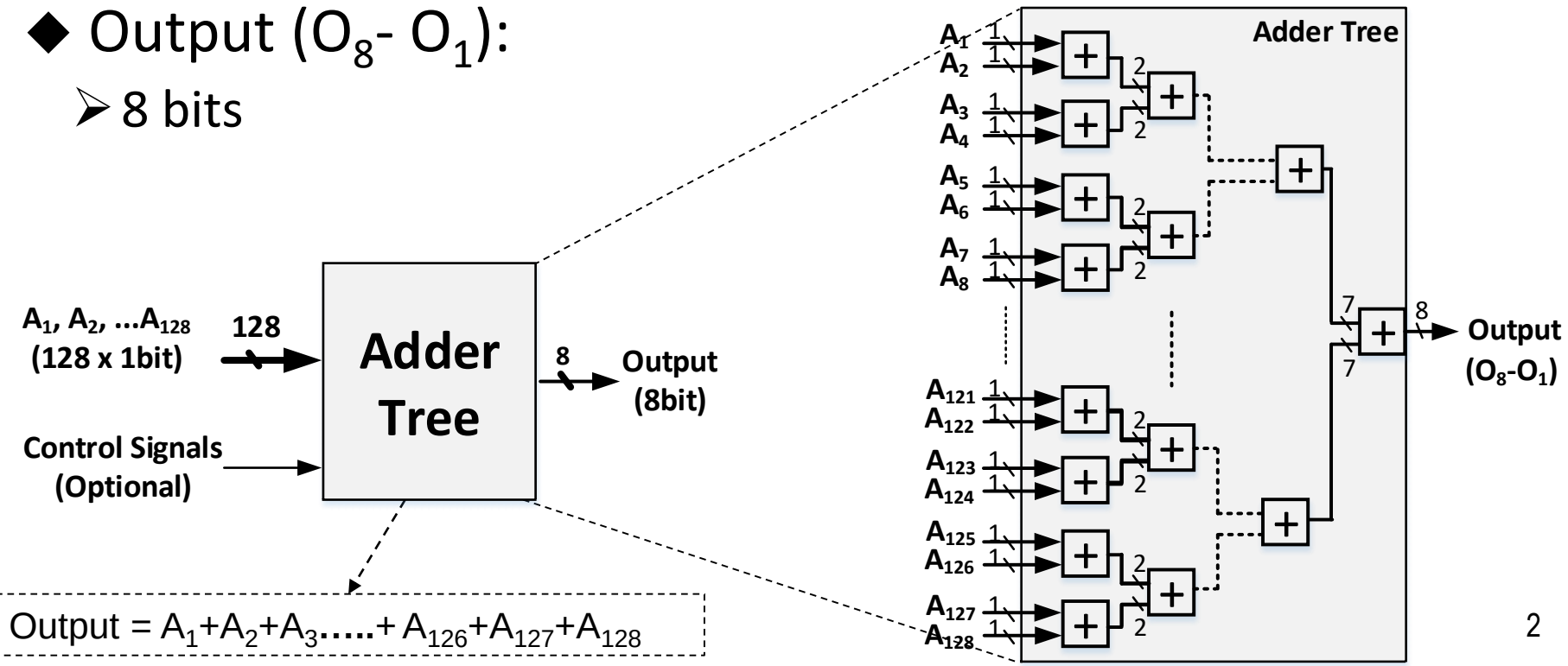
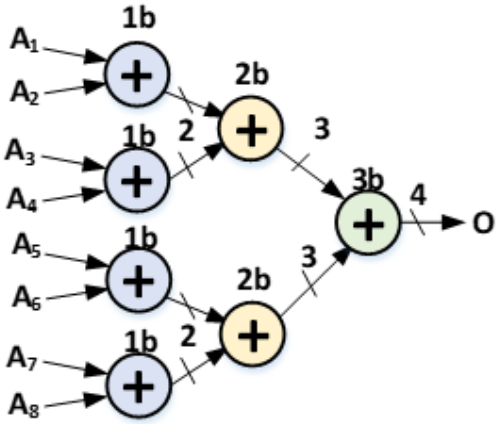
Design an Adder Tree

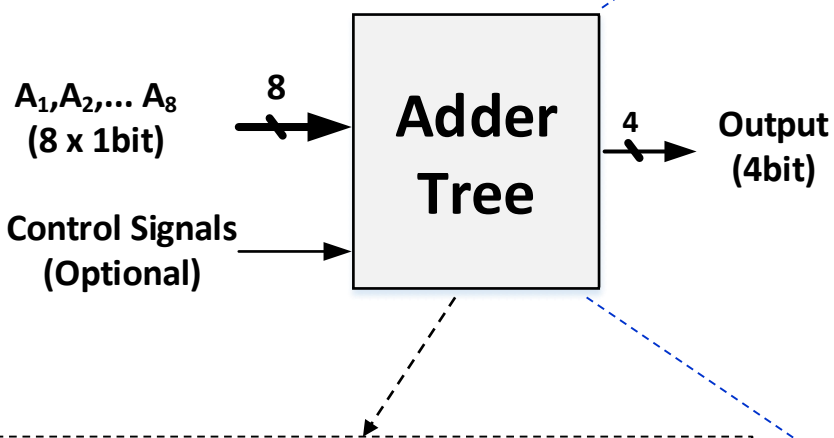
- Spec:
  - Inputs (A_1,A_2,……A_{128}):
    - 128 * 1bit
    - The minimum sampling rate is 2 GHz.
    - You can add any extra control signals for your design
  - Output (O_8- O_1):
    - 8 bits



Adder Tree

- Example:
  - Inputs (A_1, A_2, …A_8):
    - 8 * 1bit
  - Output(O_4 – O_1):
    - 4bits





Output = $A_1+A_2+A_3+A_4+A_5+A_6+A_7+A_8$