Exercise 5 Clock Gating

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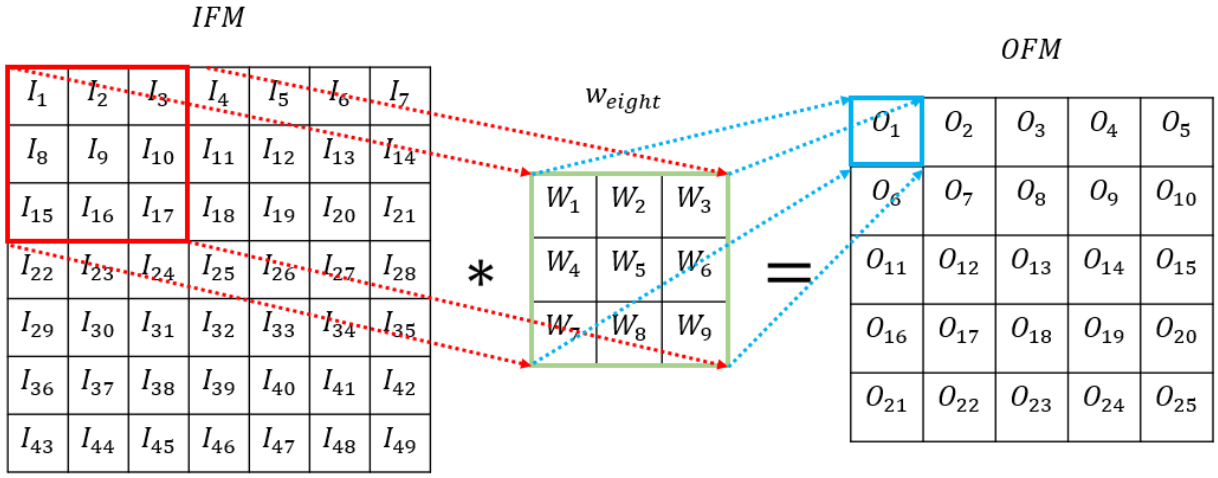
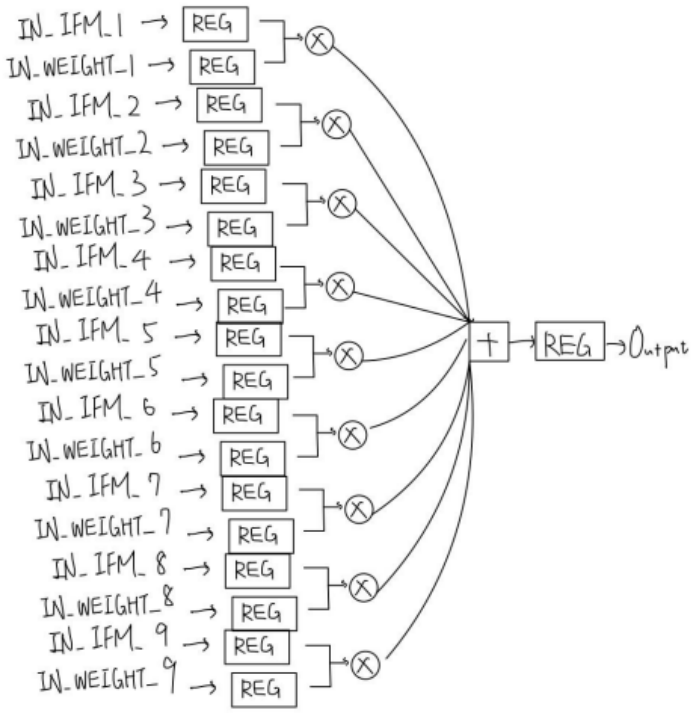
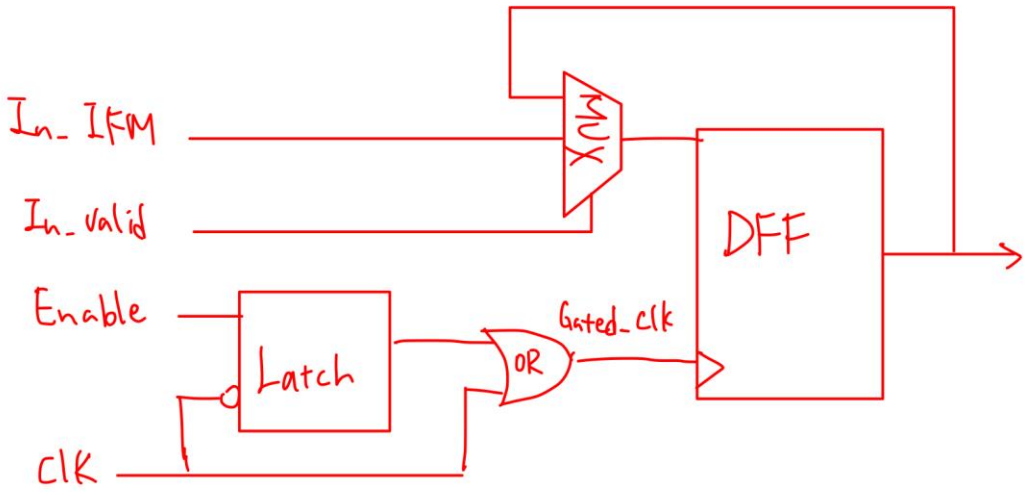
1. Draw the architectures of 3x3 convolution kernels

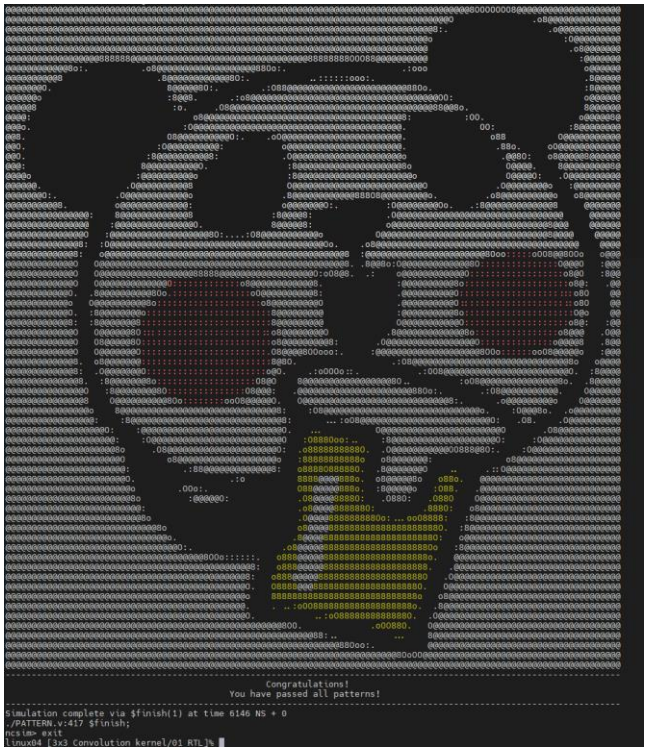






2. Analysis and discuss the power consumption & critical path

RTL pass:



SYN:

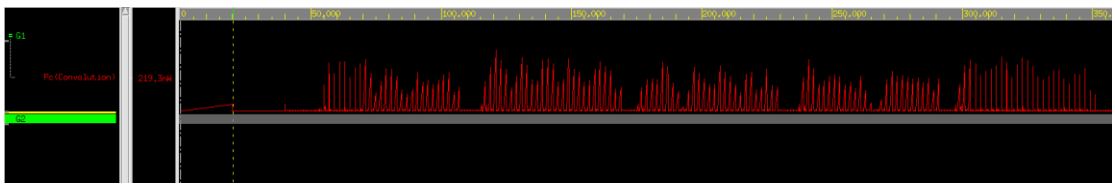
Critical point 由 weight_valid 到 Weight_3_reg[7]。

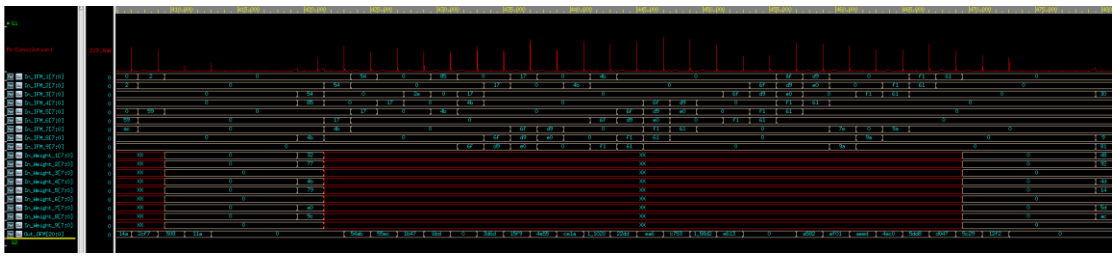
```
Operating Conditions: PVT_0P7V_25C   Library: asap7sc7p5t_INVBUF_RVT_TT_08302018
Wire Load Model Mode: top

  Startpoint: weight_valid
              (input port clocked by clk)
  Endpoint: Weight_3_reg[7]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Point                                                   Incr       Path
  -----------------------------------------------------------------------------
  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  input external delay                                 1000.00    1000.00 r
  weight_valid (in)                                       0.00    1000.00 r
  U648/Y (INVxp33_ASAP7_75t_R)                           34.71    1034.71 f
  U660/Y (INVx1_ASAP7_75t_R)                            123.73    1158.44 r
  U1162/Y (OR2x2_ASAP7_75t_R)                            50.85    1209.29 r
  U658/Y (NAND2xp33_ASAP7_75t_R)                         11.36    1220.65 f
  Weight_3_reg[7]/D (ASYNC_DFFHx1_ASAP7_75t_R)            0.00    1220.65 f
  data arrival time                                               1220.65

  clock clk (rise edge)                                2000.00    2000.00
  clock network delay (ideal)                             0.00    2000.00
  Weight_3_reg[7]/CLK (ASYNC_DFFHx1_ASAP7_75t_R)          0.00    2000.00 r
  library setup time                                    -16.14    1983.86
  data required time                                              1983.86
  -----------------------------------------------------------------------------
  data required time                                              1983.86
  data arrival time                                              -1220.65
  -----------------------------------------------------------------------------
  slack (MET)                                                     763.21
```

Gate simulation pass:

```
--------------------------------------------------------------------------------
                                                  Congratulations!
                                           You have passed all patterns!
--------------------------------------------------------------------------------
Simulation complete via $finish(1) at time 6146 NS + 0
./PATTERN.v:417 $finish;
ncsim> exit
linux04 [3x3_Convolution_kernel/03_GATE_SIM]%
```

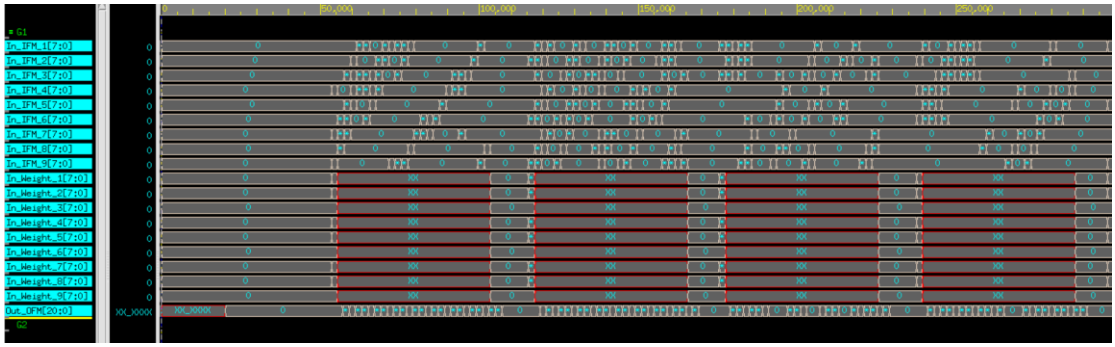
Power Prime wave view:





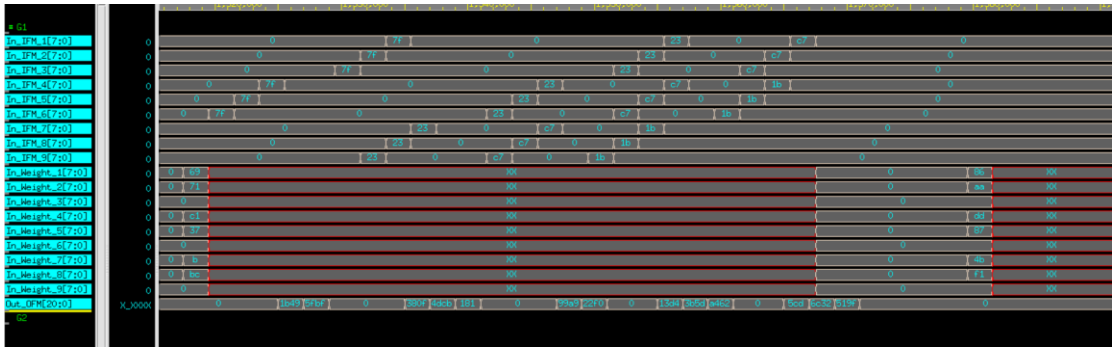
(1) w/o using clock gating

```
task gen_ifm; begin
    for(i=0; i<7; i=i+1) begin
        for(j=0; j<7; j=j+1) begin
            sparse = $random(seed)%10;
            if(sparse<9) Pattern_ifm[i][j] = 0;
            else Pattern_ifm[i][j] = $random(seed);
        end
    end
```



可以發現在 sparse < 9 時，下圖中的波行圖中數值都為 0，因此我有嘗試將 sparse < 5 來改編 pattern 產生 0 機率，並得到不同的波行圖和 power report，下圖為 sparse < 5 的波形圖。

```
task gen_ifm; begin
    for(i=0; i<7; i=i+1) begin
        for(j=0; j<7; j=j+1) begin
            sparse = $random(seed)%10;
            if(sparse<5) Pattern_ifm[i][j] = 0;
            else Pattern_ifm[i][j] = $random(seed);
        end
    end
```

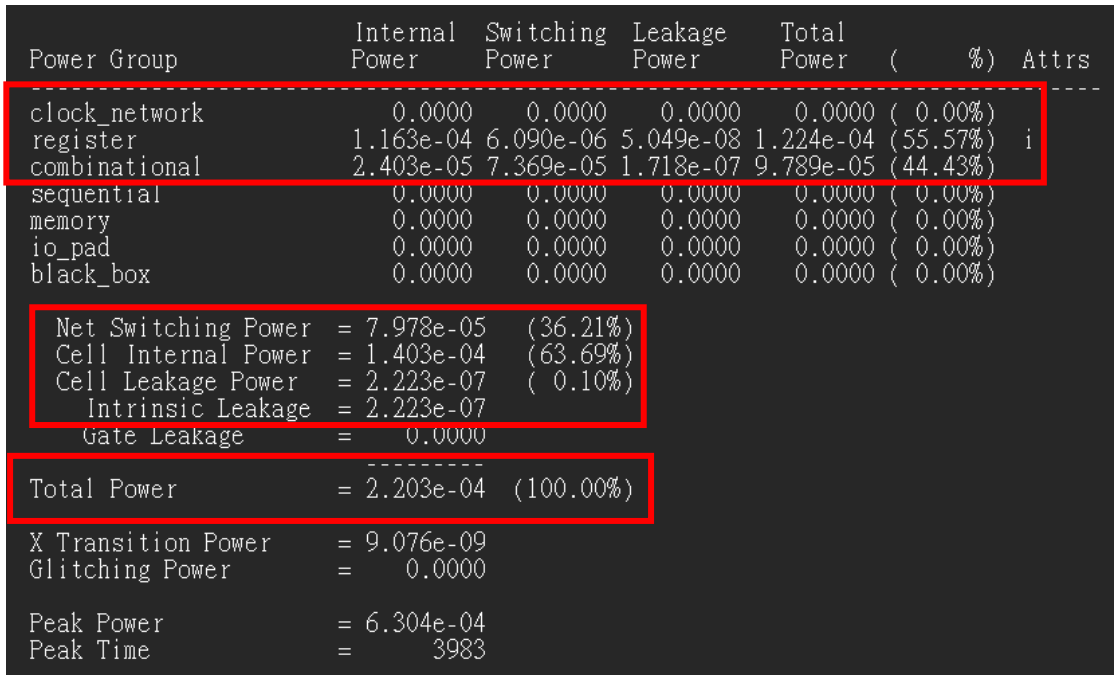


Power anylysis:

(1) sparse < 9:

```
                           Internal  Switching  Leakage    Total
Power Group                Power     Power      Power      Power   (     %)  Attrs
--------------------------------------------------------------------------------
clock_network                0.0000    0.0000     0.0000     0.0000 ( 0.00%)
register                  1.091e-04 2.092e-06 5.025e-08 1.112e-04 (77.53%)  i
combinational             7.380e-06 2.468e-05 1.707e-07 3.223e-05 (22.47%)
sequential                   0.0000    0.0000     0.0000     0.0000 ( 0.00%)
memory                       0.0000    0.0000     0.0000     0.0000 ( 0.00%)
io_pad                       0.0000    0.0000     0.0000     0.0000 ( 0.00%)
black_box                    0.0000    0.0000     0.0000     0.0000 ( 0.00%)

  Net Switching Power  = 2.678e-05   (18.67%)
  Cell Internal Power  = 1.165e-04   (81.18%)
  Cell Leakage Power   = 2.210e-07   ( 0.15%)
    Intrinsic Leakage  = 2.210e-07
    Gate Leakage       =    0.0000

Total Power            = 1.435e-04  (100.00%)

X Transition Power     = 8.906e-09
Glitching Power        =    0.0000

Peak Power             = 6.213e-04
Peak Time              =      2337
```

(2) sparse < 5:



Power Group	Internal Power	Switching Power	Leakage Power	Total Power	(%)	Attrs
clock_network	0.0000	0.0000	0.0000	0.0000	(0.00%)	
register	1.163e-04	6.090e-06	5.049e-08	1.224e-04	(55.57%)	i
combinational	2.403e-05	7.369e-05	1.718e-07	9.789e-05	(44.43%)	
sequential	0.0000	0.0000	0.0000	0.0000	(0.00%)	
memory	0.0000	0.0000	0.0000	0.0000	(0.00%)	
io_pad	0.0000	0.0000	0.0000	0.0000	(0.00%)	
black_box	0.0000	0.0000	0.0000	0.0000	(0.00%)	

Net Switching Power	= 7.978e-05	(36.21%)
Cell Internal Power	= 1.403e-04	(63.69%)
Cell Leakage Power	= 2.223e-07	(0.10%)
Intrinsic Leakage	= 2.223e-07	
Gate Leakage	= 0.0000	
Total Power	= 2.203e-04	(100.00%)
X Transition Power	= 9.076e-09	
Glitching Power	= 0.0000	
Peak Power	= 6.304e-04	
Peak Time	= 3983	

由上方兩張圖可以看出當數值不全為 0 時，消耗的總功率因為值的改變而變大，net switching power 也跟著大了將近 2 倍，唯一改變較小的是 cell leakage power。

(2) w/ using clock gating

Power anylysis:

(1) sparse < 9:

```
                           Internal  Switching  Leakage    Total
Power Group                Power     Power      Power      Power   (     %)  Attrs
--------------------------------------------------------------------------------
clock_network           1.557e-06 2.055e-06 3.484e-09 3.615e-06 ( 5.49%)
register                2.979e-05 1.485e-06 5.196e-08 3.133e-05 (47.55%)  i
combinational           7.023e-06 2.373e-05 1.966e-07 3.095e-05 (46.97%)
sequential                 0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory                     0.0000    0.0000    0.0000    0.0000 ( 0.00%)
io_pad                     0.0000    0.0000    0.0000    0.0000 ( 0.00%)
black_box                  0.0000    0.0000    0.0000    0.0000 ( 0.00%)

  Net Switching Power  = 2.727e-05   (41.39%)
  Cell Internal Power  = 3.837e-05   (58.23%)
  Cell Leakage Power   = 2.521e-07   ( 0.38%)
    Intrinsic Leakage  = 2.521e-07
    Gate Leakage       =    0.0000
                         ---------
Total Power            = 6.590e-05  (100.00%)

X Transition Power     = -1.374e-09
Glitching Power        =    0.0000

Peak Power             = 4.926e-04
Peak Time              =       5545
```

(2) sparse < 5:

```
                           Internal  Switching  Leakage    Total
Power Group                Power     Power      Power      Power   (     %)  Attrs
--------------------------------------------------------------------------------
clock_network           2.770e-06 4.042e-06 3.507e-09 6.815e-06 ( 4.81%)
register                4.305e-05 4.129e-06 5.224e-08 4.723e-05 (33.31%)  i
combinational           2.040e-05 6.716e-05 1.967e-07 8.776e-05 (61.89%)
sequential                 0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory                     0.0000    0.0000    0.0000    0.0000 ( 0.00%)
io_pad                     0.0000    0.0000    0.0000    0.0000 ( 0.00%)
black_box                  0.0000    0.0000    0.0000    0.0000 ( 0.00%)

  Net Switching Power  = 7.533e-05   (53.13%)
  Cell Internal Power  = 6.622e-05   (46.70%)
  Cell Leakage Power   = 2.525e-07   ( 0.18%)
    Intrinsic Leakage  = 2.525e-07
    Gate Leakage       =    0.0000
                         ---------
Total Power            = 1.418e-04  (100.00%)

X Transition Power     = -1.165e-09
Glitching Power        =    0.0000

Peak Power             = 6.096e-04
Peak Time              =       1519
```

結論:

（1） w/ clock gating 會比 w/o clock gating 多一個 clock_network 的 power。

（2） w/ clock gating 會比 w/o clock gating 來的節省 power。

(3) net switching power 會隨著波形圖中不為 0 的值越多而越大。

(4) w/ clock gating 會比 w/o clock gating 來的更多 intrinsic leakage 。

(5) Register power 會比 combinational power 來的大。

(6) 都具有 Cell Internal Power > Net Switching Power >> Cell Leakage Power 的關聯性。

從以上改變 sparse 條件對 pattern 生成 0 的機率不同的比較和 w/ gate、w/o gate 的比較中可以得知 pattern 產生的 0 越多可以減少 switching power ，雖然會增加 register 的 Power，卻能減少 total Power;當使用 gate clock 時會多出 clock network power 以及有較大的 Intrinsic Leakage，但是相比 w/o gate ，w/ gate 的電路會有較小的 register power 和 total Power ，總整理如下方圖表。

	Clock_network	Intrinsic leakage	Register power	Switching power	Total power
Sparse<9			較少	少	較少
Sparse<5			較多	多	較多
w/o gate	有	少	多		大
w/ gate	沒有	多	少		小