Digital IC Design

Exercise 3
Sequential circuits

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Time/Area Analysis of Sequential Circuits

- Use Verilog to design a 3x3 convolution kernel
  - Design the kernel **with/without pipeline techniques**
    - Draw the block diagram of your designs
  - Verify your designs by gate-level simulation using the pattern provided by TA.
  - Analysis on the **area, latency** and **throughput** of your designs by setting **different clock periods**

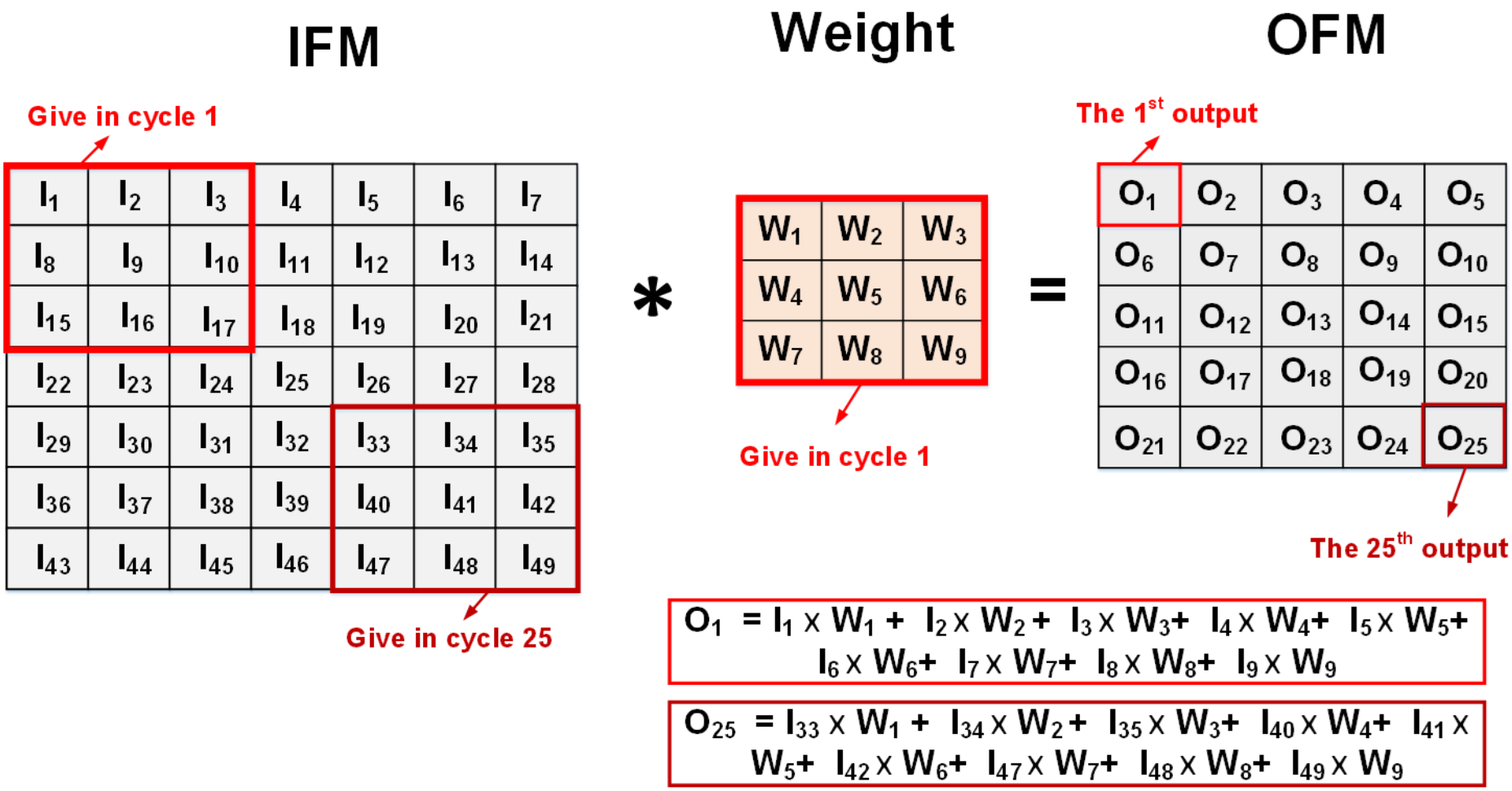
Specifications for 3x3 convolution kernels

- Signals:

Input signals	Bit width	Description
clk	1	Positive edge trigger clock
rst_n	1	Asynchronous active-low reset.
in_valid	1	When High, **In_IFMs** are valid
Weight_valid	1	When High, **In_Weights** are valid
In_IFM_1-9	8	Input feature map **(9 signals), give in 25 cycles**
In_Weight_1-9	8	Weights **(9 signals), give in one cycle**
Output signals	Bit width	Description
Out_valid	1	High when out is valid, then Patten will check Out_OFM. **(It should maintain 25 cycles)**
Out_OFM	21	The answers of the 3x3 convolution. **(It should maintain 25 cycles)**

- Settings:
  - In_IFMs & In_Weights should be received by registers.
  - The output ports should be set as registers.

Introduction of 3x3 Convolution

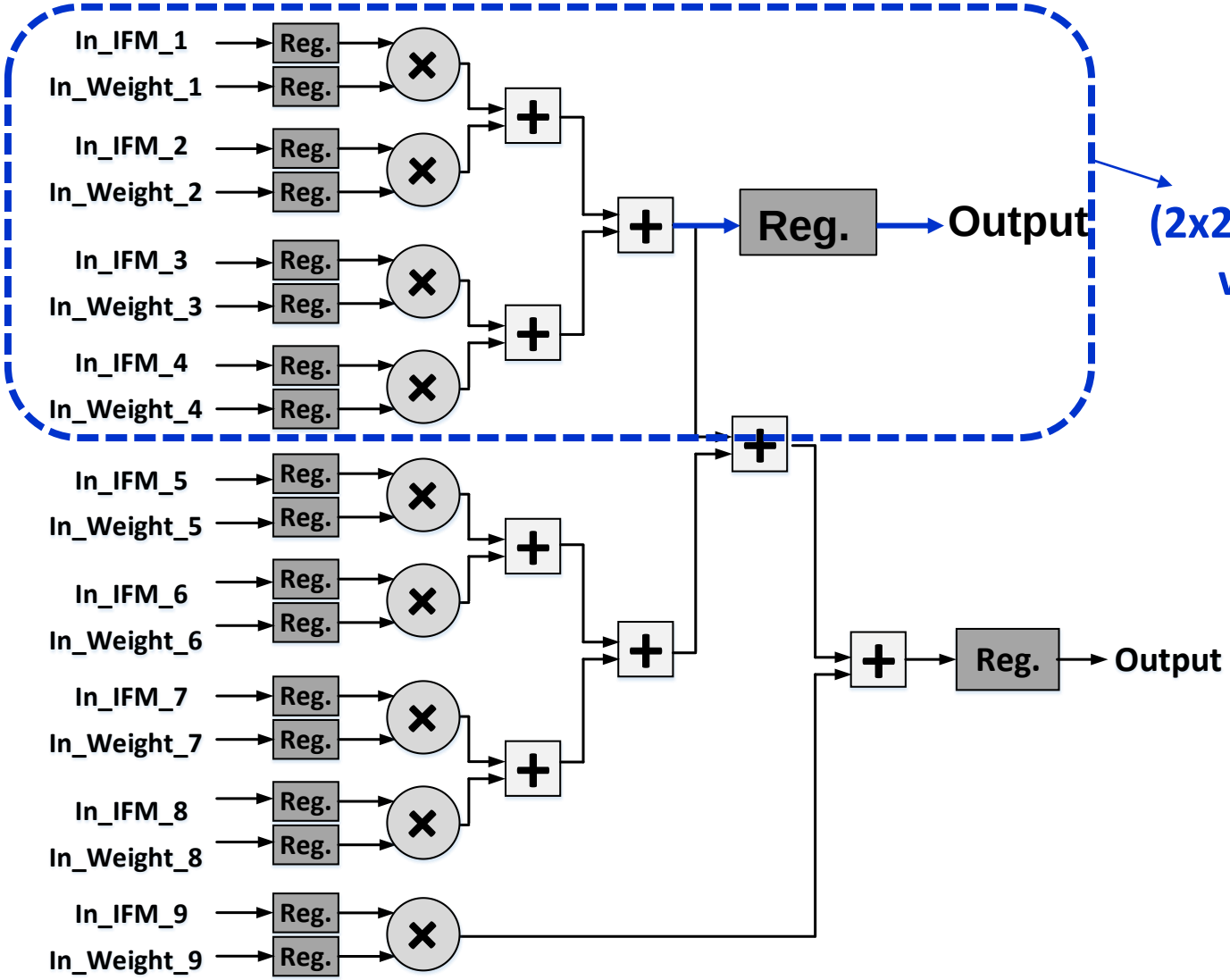


$$O_1 = I_1 \times W_1 + I_2 \times W_2 + I_3 \times W_3 + I_4 \times W_4 + I_5 \times W_5 + I_6 \times W_6 + I_7 \times W_7 + I_8 \times W_8 + I_9 \times W_9$$

$$O_{25} = I_{33} \times W_1 + I_{34} \times W_2 + I_{35} \times W_3 + I_{40} \times W_4 + I_{41} \times W_5 + I_{42} \times W_6 + I_{47} \times W_7 + I_{48} \times W_8 + I_{49} \times W_9$$

Example: Block Diagram of 3x3 Convolution

- 3x3 Convolution kernel without pipeline



Example code
(2x2 Convolution kernel without pipeline)

Submission of Exerice-3

- Please upload the following files
  - Due day: PM 11:55 on 11/24
  - Report.pdf
  - Convolution_without_pipeline.v
  - Convolution_with_pipeline.v
  - Synthesis_clk_period.txt

(Please describe the clock periods, you chose to synthesis in the report, in the “Synthesis_clk_period.txt”. TA will use the clock period to run and check your design correct or not.)