Exercise 2 Combinational circuits

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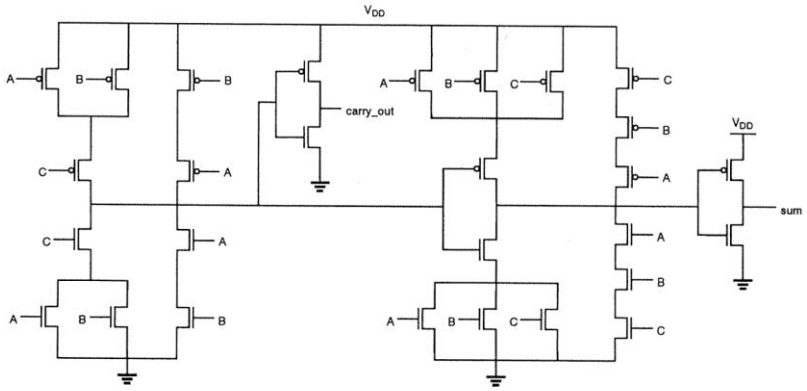
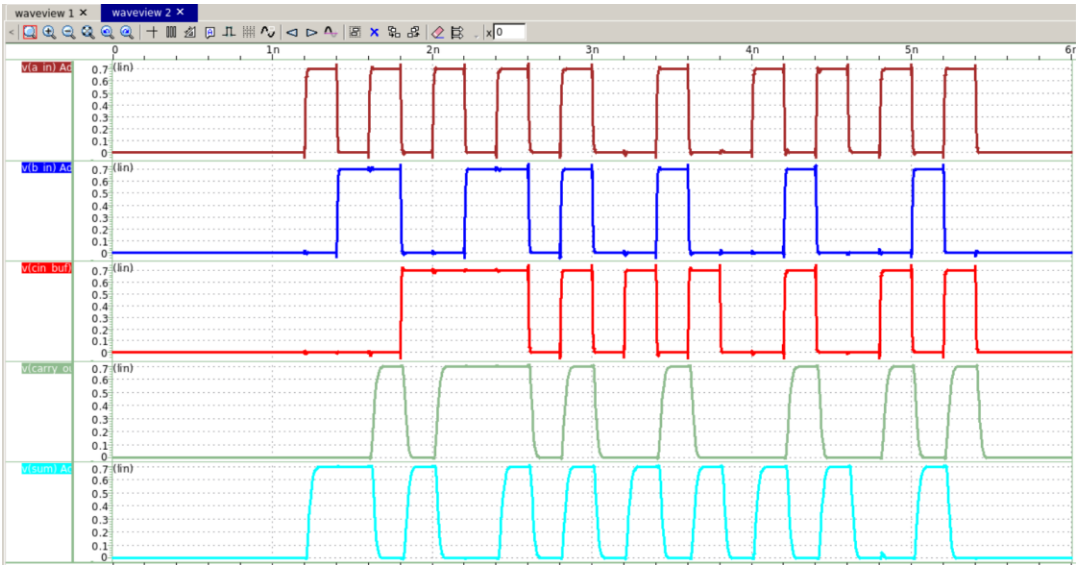
2-1: Design a 1-bit Full Adder

28T:



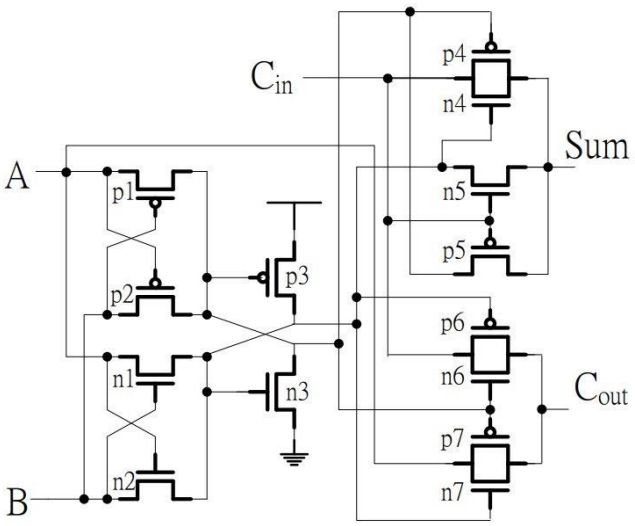


上圖是 28T 的圖形。

```
t_worst_1=  36.4025p
t_worst_2=  34.3011p
worst_case_delay=  36.4025p
```

Area=28, worst case delay = 36.4025ps, Area* worst case delay=1019.27。

14T:

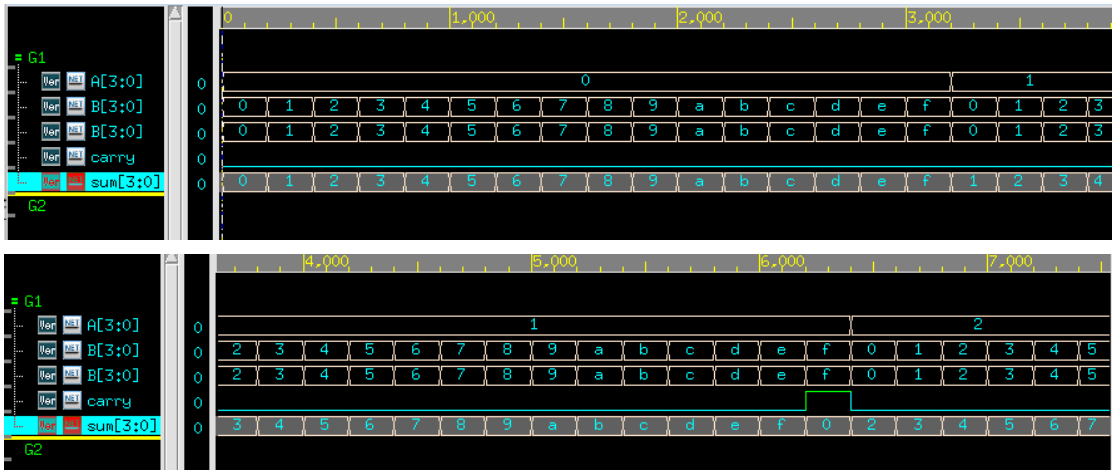


上圖為我用來優化的 1bit adder。

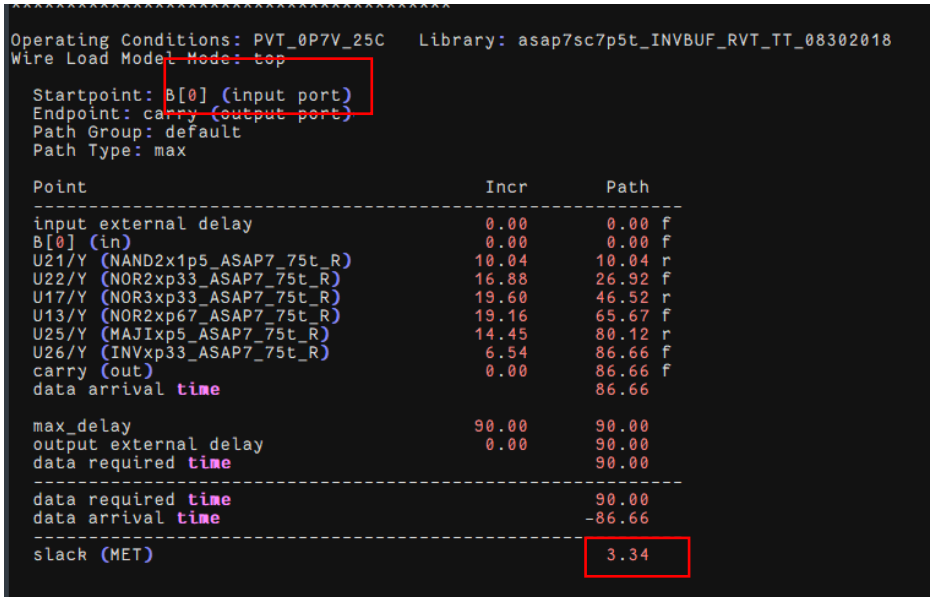
```
t_worst_1=  26.1273p
t_worst_2=  51.6019p
worst_case_delay=  51.6019p
```

Area=14, worst case delay = 51.6019ps, Area* worst case delay=722.4266。

2-2: Design a 4-Bit Adder



有透過 verdi 觀察訊號的變化以驗證自己所設計的確實為一個 4bit adder。



```
Operating Conditions: PVT_0P7V_25C   Library: asap7sc7p5t_INVBUF_RVT_TT_08302018
Wire Load Model Mode: top

  Startpoint: B[0] (input port)
  Endpoint: carry (output port)
  Path Group: default
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 f
  B[0] (in)                                0.00       0.00 f
  U21/Y (NAND2x1p5_ASAP7_75t_R)           10.04      10.04 r
  U22/Y (NOR2xp33_ASAP7_75t_R)            16.88      26.92 f
  U17/Y (NOR3xp33_ASAP7_75t_R)            19.60      46.52 r
  U13/Y (NOR2xp67_ASAP7_75t_R)            19.16      65.67 f
  U25/Y (MAJIxp5_ASAP7_75t_R)             14.45      80.12 r
  U26/Y (INVxp33_ASAP7_75t_R)              6.54      86.66 f
  carry (out)                              0.00      86.66 f
  data arrival time                                  86.66

  max_delay                               90.00      90.00
  output external delay                    0.00      90.00
  data required time                                 90.00
  -----------------------------------------------------------
  data required time                                 90.00
  data arrival time                                 -86.66
  -----------------------------------------------------------
  slack (MET)                                        3.34
```

如 syn.log 中所示 critical path 為從 B[0]或 A[0]開始到 carry 的路徑且 delay 時間為 86.66ps，且發生在 carry 發生訊號變化時，因此我設計了如下的 pattern 來包含 critical path，由左至右順序為 A[3] A[2] A[1] A[0] B[3] B[2] B[1] B[0]，皆只改變 B[0]來使 carry 發生 0 和 1 之間的改變。

```
11010010    00111100
11010011    00111101
11010010    00111100
11010011    00111101

10010110    01111000
10010111    01111001
10010110    01111000
10010111    01111001

10110100    01011010
10110101    01011011
10110100    01011010
10110101    01011011

00011110    11110000
00011111    11110001
00011110    11110000
00011111    11110001
```

2-3: CMOS Logics for 4-Bit Adder

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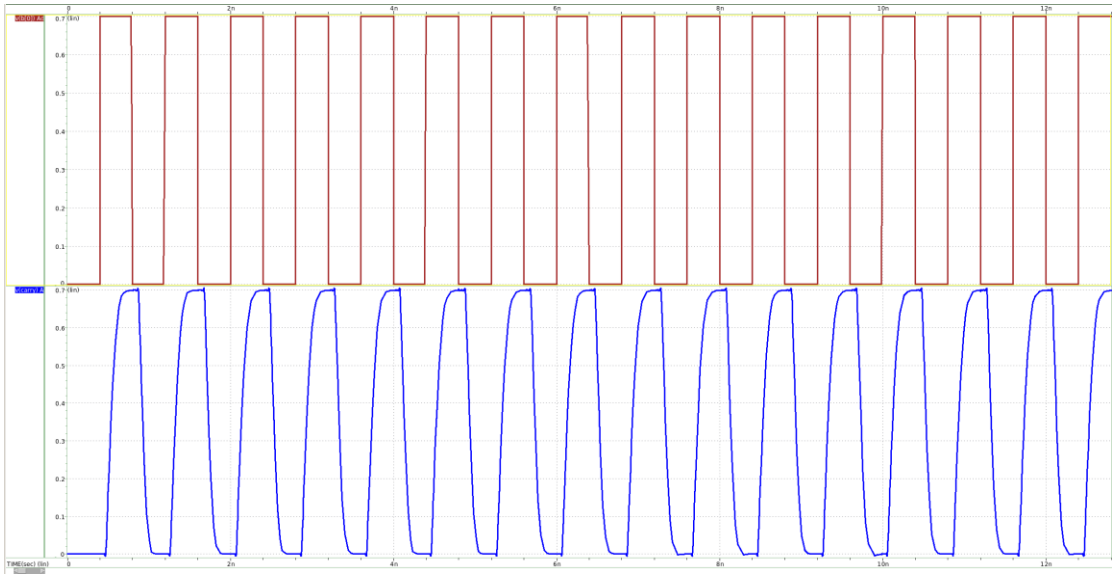

上圖為我輸入自己 pattern 後的波形圖。

```
******
.title ex_2_3

****** transient analysis tnom=  25.000 temp=  25.000 ******
tr1= 132.0343p  targ=   1.3235n   trig=   1.1915n
tf1= 132.6997p  targ=   1.7327n   trig=   1.6000n
tpd1= 132.3670p
tr2= 134.2941p  targ=   2.9343n   trig=   2.8000n
tf2= 132.7219p  targ=   3.3327n   trig=   3.2000n
tpd2= 133.5080p
tr3= 132.8458p  targ=   4.5250n   trig=   4.3922n
tf3= 135.3091p  targ=   4.9353n   trig=   4.8000n
tpd3= 134.0775p
tr4= 130.5157p  targ=   6.1305n   trig=   6.0000n
tf4= 135.0244p  targ=   6.5250n   trig=   6.3900n
tpd4= 132.7701p
tr5= 130.7850p  targ=   7.7308n   trig=   7.6000n
tf5= 134.9862p  targ=   8.1350n   trig=   8.0000n
tpd5= 132.8856p
tr6= 130.7944p  targ=   9.3308n   trig=   9.2000n
tf6= 135.1809p  targ=   9.7352n   trig=   9.6000n
tpd6= 132.9876p
tr7= 130.5822p  targ=  10.9306n   trig=  10.8000n
tf7= 132.1532p  targ=  11.3321n   trig=  11.2000n
tpd7= 131.3677p
tr8= 134.4419p  targ=  11.7344n   trig=  11.6000n
tf8= 132.5014p  targ=  12.1325n   trig=  12.0000n
tpd8= 133.4717p
pwr=  14.3935u  from=   0.              to=  12.8000n

          ***** job concluded
******
```

上圖為 lis 檔透過 measure 所量出各個 pattern 的 delay，由結果得知第 3 組訊號 delay=134.0775ps 為最長(紅框中顯示 B 由 0110 變為 0111 時)，另外可以從紅框中看出 12.8n 內的平均功率約為 14.3925uW。