Digital IC Design

Exercise 4
Voltage Scaling

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Optimal Energy-Delay Product

- Synthesize the 2x2 convolution kernel provided by TA based on ASAP 7nm standard cells.
- Convert the design to HSPICE for voltage scaling and power measurement
  - Input patterns
    - Need cover the critical path for delay measurment
    - Random patterns and the number of vectors should be more than 20 for power measurment
- Find the optimal **energy-delay product** of the 2x2 convolution kernel under different voltages
  - Provide the waveform with the correct function in your report (import .tr0 to nWave)

Submission of Exerice-4

- Please upload the following files on E3
  - Due day: PM 11:55 on 12/8
  - Ex-4_Student ID.tar
    - Report.pdf
    - 2x2_Conv.sp
    - Pattern.vec