Digital IC Design

Exercise 1
Basic Logic Gates

Professor Po-Tsang Huang

International College of Semiconductor Technology
National Yang Ming Chiao Tung University

Exercise 1-1: DC characteristics (30%)

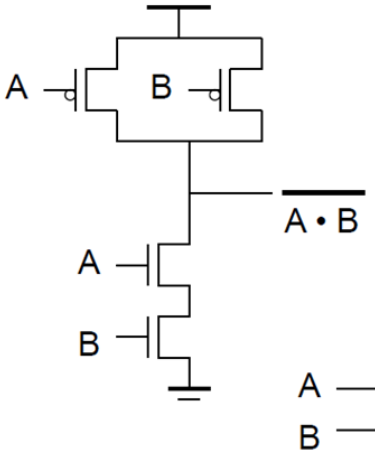
- Simulate DC characteristics of FinFETs and planer MOSs by minimal feature sizes
  - V_{gs}-I_{DS} of FinFET (N-FinFET & P-FinFET) in one figure
    - Number of Fin = 1
    - Vdd = 0.7v
  - V_{gs}-I_{DS} of CMOS (NMOS & P-MOS)in one figure
    - minimal width and Length = 16nm
    - Vdd = 0.7v
  - How to design an unit-sized inverter for these 2 technologies to achieve β = 1 in VTC?

Exercise 1-2: Voltage Transfer Curve (30%)

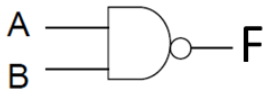
- Select the smallest and largest inverters from ASAP 7nm standard cell library and simulate the voltage transfer characteristic (VTC).
  - Netlist of standard cells: asap7sc7p5t_INVBUF_RVT.sp
  - Plot VTC curves of these 2 inverters under different voltages (Vdd = 0.7V, 0.6V, 0.5V and 0.4V)

Exercise 1-3: Characteristics of Inverter/NAND2 (40%)

- Select the smallest **Inverter** and **NAND2** from ASAP 7nm standard cell library
  - Output loading: FO4 (4 inverters) + 10 fF as wire loading
  - Netlist of standard cells:
    - asap7sc7p5t_INVBUF_RVT.sp
    - asap7sc7p5t_SIMPLE_RVT.sp
  - Vdd = 0.7v
  - Measure Tr, Tf, Tplh, Tphl, power



A	B	F
0	0	1
0	1	1
1	0	1
1	1	0



Submission on e3 platform

- Please compress your **report** & **source codes in a single compressed file (.zip)** and upload this single file on E3 platform

- Naming rules of files
  - Upload file: **Ex1_#ID.zip**
    - Report: **Ex1_#ID.pdf**
    - Hspice code: **Ex1_1.sp**
      Ex1_2.sp
      Ex1_3.sp

- Due date: 10/13 PM 23:55