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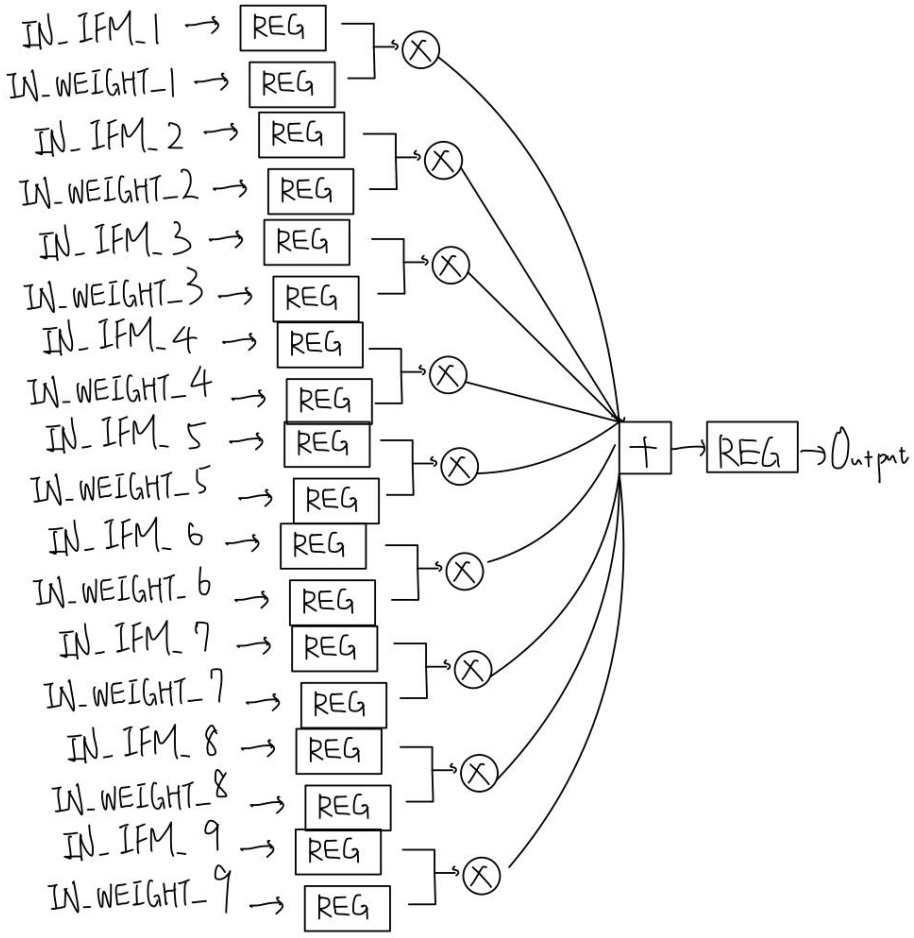
Exercise 3 Sequential circuits

Without pipeline techniques

1. Block diagram



2. Verify your designs by gate-level simulation

```
--------------------------------------------------------------------------------
                                                    Congratulations!
                                                 You have passed all patterns!
--------------------------------------------------------------------------------
Simulation complete via $finish(1) at time 2899500 PS + 0
./PATTERN_v2.v:379 $finish;
ncsim> exit
TOOL: irun  15.20-s084: Exiting on Nov 14, 2022 at 07:04:15 CST  (total: 00:00:05)
```

3. Analysis on the area by setting different clock periods

(1)

```
set DESIGN "Convolution_without_pipeline"
set clk_period 1000.0
# the unit of the clk period  in here is ps
set IN_DLY  [expr 0.5*$clk_period]
set OUT_DLY [expr 0.5*$clk_period]
```

set clk_period =1000.0 ps:

```
****************************************
Report : area
Design : Convolution_without_pipeline
Version: R-2020.09
Date   : Mon Nov 14 06:58:16 2022
****************************************

Library(s) Used:

    asap7sc7p5t_SIMPLE_RVT_TT_08302018 (File: /RAID2/COURSE/DIC/DIC143/hw3/3x3_Kernel/02_SYN_without/asap7sc7p5t_SIMPLE_RVT_TT_08302018.db)
    asap7sc7p5t_INVBUF_RVT_TT_08302018 (File: /RAID2/COURSE/DIC/DIC143/hw3/3x3_Kernel/02_SYN_without/asap7sc7p5t_INVBUF_RVT_TT_08302018.db)
    asap7sc7p5t_SEQ_RVT_TT_08302018 (File: /RAID2/COURSE/DIC/DIC143/hw3/3x3_Kernel/02_SYN_without/asap7sc7p5t_SEQ_RVT_TT_08302018.db)

Number of ports:                          170
Number of nets:                          2755
Number of cells:                         2069
Number of combinational cells:           1898
Number of sequential cells:               171
Number of macros/black boxes:               0
Number of buf/inv:                        231
Number of references:                      21

Combinational area:              3105.190053
Buf/Inv area:                     162.829442
Noncombinational area:           1037.162873
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                 4142.352926
Total area:                 undefined
1
```

Area = 4142.352926

(2)

```
set DESIGN "Convolution_without_pipeline"
set clk_period 850.0
# the unit of the clk period  in here is ps
set IN_DLY  [expr 0.5*$clk_period]
set OUT_DLY [expr 0.5*$clk_period]
```

set clk_period =850.0 ps:

```
****************************************
Report : area
Design : Convolution_without_pipeline
Version: R-2020.09
Date   : Sun Nov 20 05:55:48 2022
****************************************

Library(s) Used:

    asap7sc7p5t_SIMPLE_RVT_TT_08302018 (File: /RAID2/COURSE/DIC/DIC143/hw3/3x3_Kernel/02_SYN_without/asap7sc7p5t_SIMPLE_RVT_TT_08302018.db)
    asap7sc7p5t_INVBUF_RVT_TT_08302018 (File: /RAID2/COURSE/DIC/DIC143/hw3/3x3_Kernel/02_SYN_without/asap7sc7p5t_INVBUF_RVT_TT_08302018.db)
    asap7sc7p5t_SEQ_RVT_TT_08302018 (File: /RAID2/COURSE/DIC/DIC143/hw3/3x3_Kernel/02_SYN_without/asap7sc7p5t_SEQ_RVT_TT_08302018.db)

Number of ports:                          170
Number of nets:                          2995
Number of cells:                         2311
Number of combinational cells:           2140
Number of sequential cells:               171
Number of macros/black boxes:               0
Number of buf/inv:                        401
Number of references:                      24

Combinational area:              3222.296616
Buf/Inv area:                     282.268804
Noncombinational area:           1037.162873
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                 4259.459489
Total area:                 undefined
1
```

Area = 4259.459489

(3)

```
set DESIGN "Convolution_without_pipeline"
set clk_period 750.0
# the unit of the clk period  in here is ps
set IN_DLY  [expr 0.5*$clk_period]
set OUT_DLY [expr 0.5*$clk_period]
```

set clk_period =750.0ps :

```
****************************************
Report : area
Design : Convolution_without_pipeline
Version: R-2020.09
Date   : Sun Nov 20 05:49:39 2022
****************************************

Library(s) Used:

    asap7sc7p5t_SIMPLE_RVT_TT_08302018 (File: /RAID2/COURSE/DIC/DIC143/hw3/3x3_Kernel/02_SYN_without/asap7sc7p5t_SIMPLE_RVT_TT_08302018.db)
    asap7sc7p5t_INVBUF_RVT_TT_08302018 (File: /RAID2/COURSE/DIC/DIC143/hw3/3x3_Kernel/02_SYN_without/asap7sc7p5t_INVBUF_RVT_TT_08302018.db)
    asap7sc7p5t_SEQ_RVT_TT_08302018 (File: /RAID2/COURSE/DIC/DIC143/hw3/3x3_Kernel/02_SYN_without/asap7sc7p5t_SEQ_RVT_TT_08302018.db)

Number of ports:                          170
Number of nets:                          3026
Number of cells:                         2368
Number of combinational cells:           2197
Number of sequential cells:               171
Number of macros/black boxes:               0
Number of buf/inv:                        375
Number of references:                      28

Combinational area:               3334.504296
Buf/Inv area:                      266.172483
Noncombinational area:            1037.162873
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  4371.667169
Total area:                 undefined
```

Area = 4371.667169

(4)

```
set DESIGN "Convolution_without_pipeline"
set clk_period 590.0
# the unit of the clk period  in here is ps
set IN_DLY  [expr 0.5*$clk_period]
set OUT_DLY [expr 0.5*$clk_period]
```

set clk_period =590.0ps :

```
****************************************
Report : area
Design : Convolution_without_pipeline
Version: R-2020.09
Date   : Sun Nov 20 05:44:03 2022
****************************************

Library(s) Used:

    asap7sc7p5t_SIMPLE_RVT_TT_08302018 (File: /RAID2/COURSE/DIC/DIC143/hw3/3x3_Kernel/02_SYN_without/asap7sc7p5t_SIMPLE_RVT_TT_08302018.db)
    asap7sc7p5t_INVBUF_RVT_TT_08302018 (File: /RAID2/COURSE/DIC/DIC143/hw3/3x3_Kernel/02_SYN_without/asap7sc7p5t_INVBUF_RVT_TT_08302018.db)
    asap7sc7p5t_SEQ_RVT_TT_08302018 (File: /RAID2/COURSE/DIC/DIC143/hw3/3x3_Kernel/02_SYN_without/asap7sc7p5t_SEQ_RVT_TT_08302018.db)

Number of ports:                          170
Number of nets:                          3901
Number of cells:                         3697
Number of combinational cells:           3526
Number of sequential cells:               171
Number of macros/black boxes:               0
Number of buf/inv:                        758
Number of references:                      43

Combinational area:            5187.214053
Buf/Inv area:                   661.815364
Noncombinational area:         1037.162873
Macro/Black Box area:             0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:               6224.376927
Total area:                 undefined
```

Area = 6224.376927

(5)

```
set DESIGN "Convolution_without_pipeline"
set clk_period 589.0
# the unit of the clk period  in here is ps
set IN_DLY  [expr 0.5*$clk_period]
set OUT_DLY [expr 0.5*$clk_period]
```

set clk_period =589.0ps :

```
clock clk (rise edge)                                   589.00     589.00
clock network delay (ideal)                               0.00     589.00
Out_OFM_reg[17]/CLK (ASYNC_DFFHx1_ASAP7_75t_R)            0.00     589.00 r
library setup time                                      -14.98     574.02
data required time                                                 574.02
--------------------------------------------------------------------------
data required time                                                 574.02
data arrival time                                                 -578.83
--------------------------------------------------------------------------
slack (VIOLATED)                                                    -4.81
```

將 clk_period 下降至 589 後，slack 會變為負的。

從結果中可以看出隨著 clk_period 的下降，面積也會跟著上升來配合時間下降的限制。

4. Analysis on the latency by setting different clock periods

(1) **set clk_period = 1000.0 ps:**

```
clock clk (rise edge)                                  1000.00    1000.00
clock network delay (ideal)                               0.00    1000.00
Out_OFM_reg[17]/CLK (ASYNC_DFFHx1_ASAP7_75t_R)            0.00    1000.00 r
library setup time                                      -20.78     979.22
data required time                                                 979.22
-------------------------------------------------------------------------
data required time                                                 979.22
data arrival time                                                 -975.46
-------------------------------------------------------------------------
slack (MET)                                                          3.77
```

Latency = 975.46 ps

(2) **set clk_period = 850.0 ps:**

```
clock clk (rise edge)                                  850.00     850.00
clock network delay (ideal)                               0.00    850.00
Out_OFM_reg[18]/CLK (ASYNC_DFFHx1_ASAP7_75t_R)            0.00    850.00 r
library setup time                                      -16.89     833.11
data required time                                                 833.11
-------------------------------------------------------------------------
data required time                                                 833.11
data arrival time                                                 -832.99
-------------------------------------------------------------------------
slack (MET)                                                          0.12
```

Latency = 832.99 ps

(3) **set clk_period = 750.0 ps:**

```
clock clk (rise edge)                                  750.00     750.00
clock network delay (ideal)                               0.00    750.00
Out_OFM_reg[17]/CLK (ASYNC_DFFHx1_ASAP7_75t_R)            0.00    750.00 r
library setup time                                      -19.18     730.82
data required time                                                 730.82
-------------------------------------------------------------------------
data required time                                                 730.82
data arrival time                                                 -730.58
-------------------------------------------------------------------------
slack (MET)                                                          0.24
```

Latency = 730.58 ps

(4) **set clk_period = 590.0 ps:**

```
clock clk (rise edge)                                  590.00     590.00
clock network delay (ideal)                               0.00    590.00
Out_OFM_reg[18]/CLK (ASYNC_DFFHx1_ASAP7_75t_R)            0.00    590.00 r
library setup time                                      -19.34     570.66
data required time                                                 570.66
-------------------------------------------------------------------------
data required time                                                 570.66
data arrival time                                                 -570.63
-------------------------------------------------------------------------
slack (MET)                                                          0.02
```

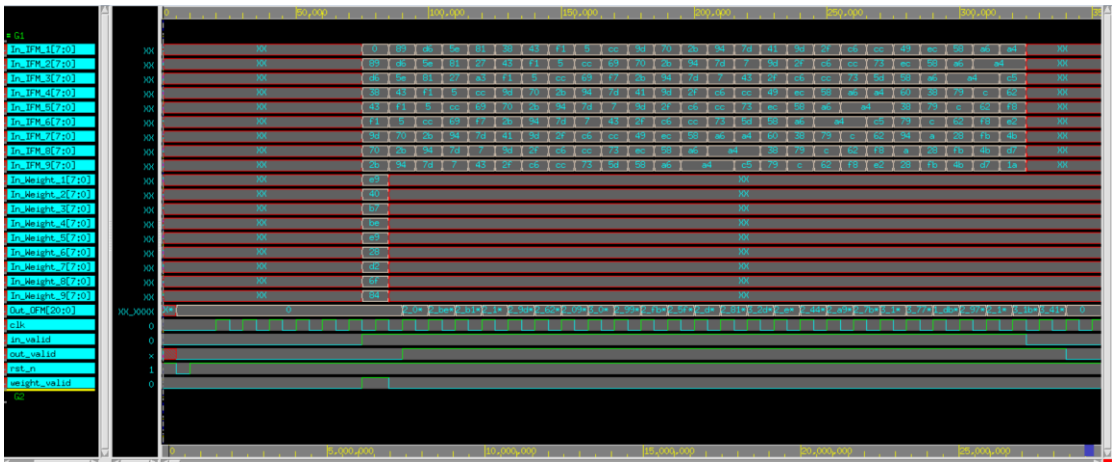
Latency = 570.63 ps

5. Analysis on the throughput by setting different clock periods

Throughput = 25*9 /(latency+25 個 cycle 的時間)(MAC/s)

(1) set clk_period = 1000.0 ps:
Latency = 975.46 ps
Throughput = 25*9/(975.46 + 25*1000) = 8662021770(MAC/s)
(2) set clk_period = 850.0 ps:
Latency = 832.99 ps
Throughput = 25*9/(832.99 + 25*850) = 10188837660(MAC/s)
(3) set clk_period = 750.0 ps:
Latency = 730.58 ps
Throughput = 25*9/(730.58 + 25*750) = 11549964110(MAC/s)
(4) set clk_period = 590.0 ps:
Latency = 570.63 ps
Throughput = 25*9/(570.63 + 25*590) = 14686080140(MAC/s)

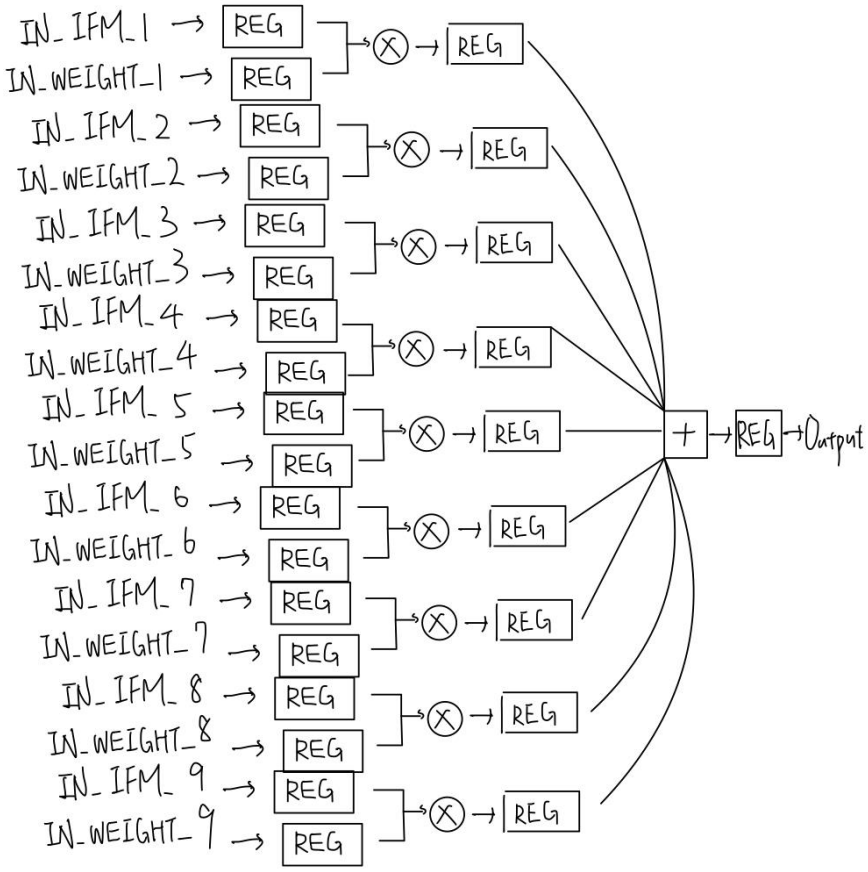
6. 波形圖



With pipeline techniques

1. Block diagram

我透過在每個乘法後面加上 register 作為 pipeline 來縮短時間。



2. Verify your designs by gate-level simulation

```
                                                    Congratulations!
                                             You have passed all patterns!
Simulation complete via $finish(1) at time 2999500 PS + 0
./PATTERN_v2.v:379 $finish;
ncsim> exit
TOOL: irun  15.20-s084: Exiting on Nov 20, 2022 at 03:18:24 CST  (total: 00:00:05)
```

3. Analysis on the area by setting different clock periods

(1)

```
set DESIGN "Convolution_without_pipeline"
set clk_period 1000.0
# the unit of the clk period  in here is ps
set IN_DLY  [expr 0.5*$clk_period]
set OUT_DLY [expr 0.5*$clk_period]
```

set clk_period = 1000.0 ps:

```
****************************************
Report : area
Design : Convolution_with_pipeline
Version: R-2020.09
Date   : Sun Nov 20 03:16:34 2022
****************************************

Library(s) Used:

    asap7sc7p5t_SIMPLE_RVT_TT_08302018 (File: /RAID2/COURSE/DIC/DIC143/hw3/3x3_Kernel/02_SYN/asap7sc7p5t_SIMPLE_RVT_TT_08302018.db)
    asap7sc7p5t_INVBUF_RVT_TT_08302018 (File: /RAID2/COURSE/DIC/DIC143/hw3/3x3_Kernel/02_SYN/asap7sc7p5t_INVBUF_RVT_TT_08302018.db)
    asap7sc7p5t_SEQ_RVT_TT_08302018 (File: /RAID2/COURSE/DIC/DIC143/hw3/3x3_Kernel/02_SYN/asap7sc7p5t_SEQ_RVT_TT_08302018.db)

Number of ports:                          170
Number of nets:                          3781
Number of cells:                         3212
Number of combinational cells:           2896
Number of sequential cells:               316
Number of macros/black boxes:               0
Number of buf/inv:                        538
Number of references:                      24

Combinational area:               3968.326058
Buf/Inv area:                      380.246405
Noncombinational area:            1916.628468
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  5884.954525
Total area:                 undefined
1
```

Area = 5884.954525

(2)

```
set DESIGN "Convolution_with_pipeline"
set clk_period 900.0
# the unit of the clk period  in here is ps
set IN_DLY  [expr 0.5*$clk_period]
set OUT_DLY [expr 0.5*$clk_period]
```

set clk_period = 900.0 ps:

```
****************************************
Report : area
Design : Convolution_with_pipeline
Version: R-2020.09
Date   : Sun Nov 20 07:14:13 2022
****************************************

Library(s) Used:

    asap7sc7p5t_INVBUF_RVT_TT_08302018 (File: /RAID2/COURSE/DIC/DIC143/hw3/3x3_Kernel/02_SYN/asap7sc7p5t_INVBUF_RVT_TT_08302018.db)
    asap7sc7p5t_SIMPLE_RVT_TT_08302018 (File: /RAID2/COURSE/DIC/DIC143/hw3/3x3_Kernel/02_SYN/asap7sc7p5t_SIMPLE_RVT_TT_08302018.db)
    asap7sc7p5t_SEQ_RVT_TT_08302018 (File: /RAID2/COURSE/DIC/DIC143/hw3/3x3_Kernel/02_SYN/asap7sc7p5t_SEQ_RVT_TT_08302018.db)

Number of ports:                          170
Number of nets:                          3778
Number of cells:                         3209
Number of combinational cells:           2893
Number of sequential cells:               316
Number of macros/black boxes:               0
Number of buf/inv:                        535
Number of references:                      27

Combinational area:               3968.326058
Buf/Inv area:                      377.447045
Noncombinational area:            1916.628468
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  5884.954525
Total area:                 undefined
1
```

Area = 5884.954525

(3)

```
set DESIGN "Convolution_with_pipeline"
set clk_period 800.0
# the unit of the clk period  in here is ps
set IN_DLY  [expr 0.5*$clk_period]
set OUT_DLY [expr 0.5*$clk_period]
```

set clk_period = 800.0 ps:

```
****************************************
Report : area
Design : Convolution_with_pipeline
Version: R-2020.09
Date   : Sun Nov 20 07:07:03 2022
****************************************

Library(s) Used:

    asap7sc7p5t_INVBUF_RVT_TT_08302018 (File: /RAID2/COURSE/DIC/DIC143/hw3/3x3_Kernel/02_SYN/asap7sc7p5t_INVBUF_RVT_TT_08302018.db)
    asap7sc7p5t_SIMPLE_RVT_TT_08302018 (File: /RAID2/COURSE/DIC/DIC143/hw3/3x3_Kernel/02_SYN/asap7sc7p5t_SIMPLE_RVT_TT_08302018.db)
    asap7sc7p5t_SEQ_RVT_TT_08302018 (File: /RAID2/COURSE/DIC/DIC143/hw3/3x3_Kernel/02_SYN/asap7sc7p5t_SEQ_RVT_TT_08302018.db)

Number of ports:                          170
Number of nets:                          3715
Number of cells:                         3146
Number of combinational cells:           2830
Number of sequential cells:               316
Number of macros/black boxes:               0
Number of buf/inv:                        517
Number of references:                      24

Combinational area:               3952.929577
Buf/Inv area:                      365.083205
Noncombinational area:            1916.628468
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  5869.558045
Total area:                 undefined
1
```

Area = 5869.558045

(4)

```
set DESIGN "Convolution_with_pipeline"
set clk_period 700.0
# the unit of the clk period  in here is ps
set IN_DLY  [expr 0.5*$clk_period]
set OUT_DLY [expr 0.5*$clk_period]
```

set clk_period = 700.0 ps:

```
****************************************
Report : area
Design : Convolution_with_pipeline
Version: R-2020.09
Date   : Sun Nov 20 08:03:15 2022
****************************************

Library(s) Used:

    asap7sc7p5t_SIMPLE_RVT_TT_08302018 (File: /RAID2/COURSE/DIC/DIC143/hw3/3x3_Kernel/02_SYN/asap7sc7p5t_SIMPLE_RVT_TT_08302018.db)
    asap7sc7p5t_INVBUF_RVT_TT_08302018 (File: /RAID2/COURSE/DIC/DIC143/hw3/3x3_Kernel/02_SYN/asap7sc7p5t_INVBUF_RVT_TT_08302018.db)
    asap7sc7p5t_SEQ_RVT_TT_08302018 (File: /RAID2/COURSE/DIC/DIC143/hw3/3x3_Kernel/02_SYN/asap7sc7p5t_SEQ_RVT_TT_08302018.db)

Number of ports:                          170
Number of nets:                          3730
Number of cells:                         3162
Number of combinational cells:           2846
Number of sequential cells:               316
Number of macros/black boxes:               0
Number of buf/inv:                        530
Number of references:                      28

Combinational area:               3976.490858
Buf/Inv area:                      375.814085
Noncombinational area:            1916.628468
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  5893.119326
Total area:                 undefined
1
```

Area = 5893.119326

(5)

```
set DESIGN "Convolution_with_pipeline"
set clk_period 650.0
# the unit of the clk period  in here is ps
set IN_DLY  [expr 0.5*$clk_period]
set OUT_DLY [expr 0.5*$clk_period]
```

set clk_period =650.0 ps:

```
1
****************************************
Report : area
Design : Convolution_with_pipeline
Version: R-2020.09
Date   : Sun Nov 20 08:20:35 2022
****************************************

Library(s) Used:

    asap7sc7p5t_SIMPLE_RVT_TT_08302018 (File: /RAID2/COURSE/DIC/DIC143/hw3/3x3_Kernel/02_SYN/asap7sc7p5t_SIMPLE_RVT_TT_08302018.db)
    asap7sc7p5t_INVBUF_RVT_TT_08302018 (File: /RAID2/COURSE/DIC/DIC143/hw3/3x3_Kernel/02_SYN/asap7sc7p5t_INVBUF_RVT_TT_08302018.db)
    asap7sc7p5t_SEQ_RVT_TT_08302018 (File: /RAID2/COURSE/DIC/DIC143/hw3/3x3_Kernel/02_SYN/asap7sc7p5t_SEQ_RVT_TT_08302018.db)

Number of ports:                          170
Number of nets:                          3850
Number of cells:                         3283
Number of combinational cells:           2967
Number of sequential cells:               316
Number of macros/black boxes:               0
Number of buf/inv:                        573
Number of references:                      30

Combinational area:               4059.071981
Buf/Inv area:                      407.540165
Noncombinational area:            1916.628468
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  5975.700448
Total area:                 undefined
1
```

Area = 5975.700448

4. Analysis on the latency by setting different clock period

(1)set clk_period = 1000.0 ps:

```
clock clk (rise edge)                                  1000.00    1000.00
clock network delay (ideal)                               0.00    1000.00
Out_OFM_reg[17]/CLK (ASYNC_DFFHx1_ASAP7_75t_R)            0.00    1000.00 r
library setup time                                      -22.05     977.95
data required time                                                 977.95
-----------------------------------------------------------------------------
data required time                                                 977.95
data arrival time                                                 -942.65
-----------------------------------------------------------------------------
slack (MET)                                                         35.30
```

Latency = 942.65*2=1885.3 ps

(2)set clk_period = 900.0 ps:

```
clock clk (rise edge)                                  900.00     900.00
clock network delay (ideal)                               0.00    900.00
Out_OFM_reg[17]/CLK (ASYNC_DFFHx1_ASAP7_75t_R)            0.00    900.00 r
library setup time                                      -23.97     876.03
data required time                                                 876.03
-----------------------------------------------------------------------------
data required time                                                 876.03
data arrival time                                                 -874.84
-----------------------------------------------------------------------------
slack (MET)                                                          1.19
```

Latency = 874.84*2=1749.68 ps

(3)set clk_period = 800.0 ps:

```
clock clk (rise edge)                                  800.00     800.00
clock network delay (ideal)                               0.00    800.00
Out_OFM_reg[18]/CLK (ASYNC_DFFHx1_ASAP7_75t_R)            0.00    800.00 r
library setup time                                      -16.84     783.16
data required time                                                 783.16
-----------------------------------------------------------------------------
data required time                                                 783.16
data arrival time                                                 -782.53
-----------------------------------------------------------------------------
slack (MET)                                                          0.63
```

Latency = 782.53 *2=1565.06ps

(4)set clk_period = 700.0 ps:

```
clock clk (rise edge)                                  700.00     700.00
clock network delay (ideal)                               0.00    700.00
multiple7_reg[14]/CLK (ASYNC_DFFHx1_ASAP7_75t_R)          0.00    700.00 r
library setup time                                      -24.05     675.95
data required time                                                 675.95
-----------------------------------------------------------------------------
data required time                                                 675.95
data arrival time                                                 -675.77
-----------------------------------------------------------------------------
slack (MET)                                                          0.18
```

Latency = 675.77 *2=1351.54ps

(5) set clk_period = 650.0 ps:

```
clock clk (rise edge)                                  650.00     650.00
clock network delay (ideal)                              0.00     650.00
multiple4_reg[14]/CLK (ASYNC_DFFHx1_ASAP7_75t_R)         0.00     650.00 r
library setup time                                     -24.07     625.93
data required time                                                625.93
-----------------------------------------------------------------------
data required time                                                625.93
data arrival time                                                -625.87
-----------------------------------------------------------------------
slack (MET)                                                         0.06
```

Latency = 625.87 *2=1251.74ps

5. Analysis on the throughput by setting different clock periods

Throughput = 25*9 /(latency+25 個 cycle 的時間)(MAC/s)

(1) set clk_period = 1000.0 ps:

Latency = 1885.3 ps

Throughput = 25*9/(1885.3 + 25*1000) = 8368885599(MAC/s)

(2) set clk_period = 900.0 ps:

Latency = 1749.68 ps

Throughput = 25*9/(1749.68 + 25*900) = 9278472953(MAC/s)

(3) set clk_period = 800.0 ps:

Latency = 1565.06 ps

Throughput = 25*9/(1565.06 + 25*800) = 10433543890(MAC/s)

(4) set clk_period = 700.0 ps:

Latency = 1351.54ps

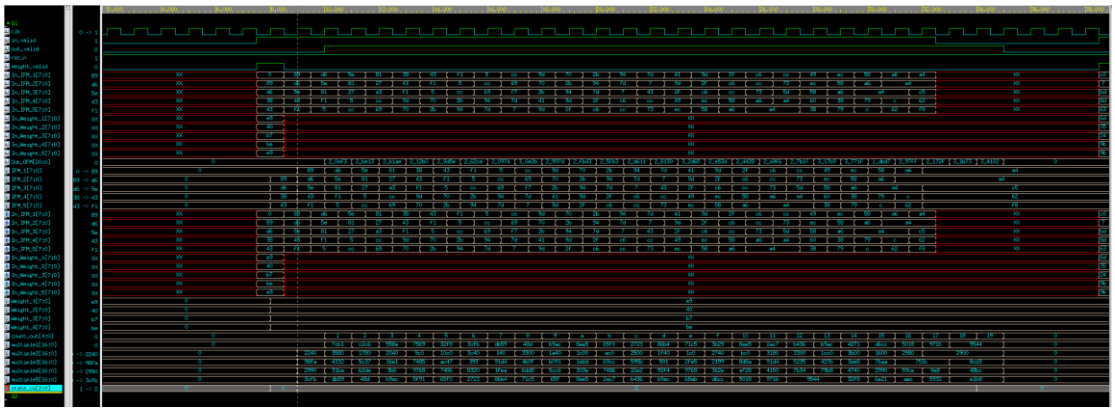
Throughput = 25*9/(1351.54 + 25*700) = 11935364430(MAC/s)

(5) set clk_period = 650.0 ps:

Latency = 1251.74 ps

Throughput = 25*9/(1251.74 + 25*650) = 1285586462(MAC/s)

6. 波形圖



圖中只叫出了 1-5 的訊號出來觀察，我利用了 state IN_DATA 來進行 IN_IFM 和 IN_WEIGHT 傳值進 IFM 和 WEIGHT 後的香橙計算傳給我設的 register multiple，並延長 state EXE 來之前的時間使 multiple 有足夠時間做運算並在 state EXE 來的時候將值傳到 Out_OFM，接著都在 state EXE 做運算和傳值直到做滿 25CYCLE 後再回歸 state IDLE 等待 In_valid 升起。