Digital IC Design

Exercise 2
Combinational circuits

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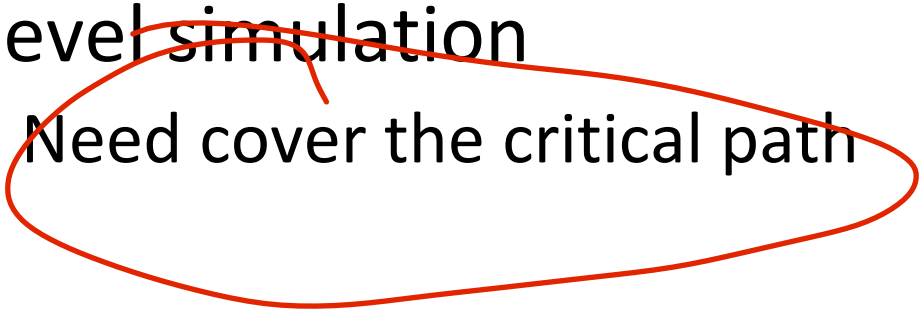
2-1: Design a 1-bit Full Adder [40%]

- Measure the delay & area of 1-bit full adder.
  - By CMOS logic
- Design 1-bit full adder and minimize the (delay × area). ⇒ transistor count
- Settings:
  - Inputs
    - A, B, Cin (TA will provide the input pattern)
  - Outputs
    - Output: {carry_out, sum}
    - The output loading of each output is **5fF.**
  - Using 7nm FinFET model.
  - Area: transistor counts
  - Delay: worst case delay

2-2: Design a 4-Bit Adder [30%]

- Design a 4-bit adder in Verilog
  - Input: a[3:0], b[3:0]
  - Output: {carry_out, sum[3:0]}
  - The sampling rate of inputs is 5GHz
- Synthesis using ASAP 7nm Technology
  - **Find out the critical paths**
- Design a pattern to verify your design in gate-level simulation
  - Need cover the critical path



2-3: CMOS Logics for 4-Bit Adder [30%]

- Covert the Verilog gate-level netlist to HSPICE netlist
  - Adder_4bit_SYN.v to Adder_4bit_SYN.sp.

- Measure the delay and power of the 4-bit adder in HSPICE
  - The tested patterns (vectors) should cover the worst case delay and power consumption.
  - **Please point out the pattern covered the worst case delay.**

Vector for HSPICE

- Use high level language (C, python, script) to generate vector files for HSPICE

```
radix   1 1 1 1 1 44 44444444444444444444444444444444
vname clk reset wen_in ren_in cen_in wl_in[[7:0]] data_in[[127:0]]
io    i i i i i ii iiiiiiiiiiiiiiiiiiiiiiiiiiiiiiii

tunit ns
slope  0.1
tdelay 0.1
vih 1.0
vil 0

0.00          1 1 0 0 0 00 00000000000000000000000000000000
1.20          1 0 0 0 0 00 00000000000000000000000000000000
2.00          0 0 0 0 0 00 00000000000000000000000000000000
4.00          1 0 0 0 0 00 00000000000000000000000000000000
6.00          0 0 1 0 0 10 ffe6dba4adae6b963e23751c19c40236
8.00          1 0 1 0 0 10 ffe6dba4adae6b963e23751c19c40236
10.00          0 0 1 0 0 20 9afde6d8e5c528b5e9dc22300da2fe6a
```

.vec test.vec

.vec test.txt

Submission on e3 platform

- Please compress your **report** & **source codes in a single compressed file (.zip)** and upload this single file on E3 platform

- Due date: 11/03 PM 23:55