



Holtek 32-bit Microcontroller with ARM® Cortex™-M3 Core

HT32F1655 / HT32F1656 Series User Manual

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1 Introduction

Overview

This user manual provides detailed information including how to use the HT32F1656/1655 devices, system and bus architecture, memory organization and peripheral instructions. The target audiences for this document are software developers, application developers and hardware developers. For more information regarding pin assignment, package and electrical characteristics, please refer to the HT32F1656/1655 datasheet.

The Holtek HT32F1656/1655 devices are high performance and low power consumption 32-bit microcontrollers based around an ARM® Cortex™-M3 processor core. The Cortex™-M3 is a next-generation processor core which is tightly coupled with Nested Vectored Interrupt Controller (NVIC), SysTick timer, and including advanced debug support.

The HT32F1656/1655 devices operate at a frequency of up to 72 MHz with a Flash accelerator to obtain maximum efficiency. It provides up to 256 KB of embedded Flash memory for code/data storage and 32 KB of embedded SRAM memory for system operation and application program usage. A variety of peripherals, such as ADC, I²C, USART, UART, SPI, I²S, PDMA, GPTM, MCTM, SCI, EBI, CRC-16/32, USB2.0 FS, SW-DP (Serial Wire Debug Port), etc., are also implemented in the device series. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features ensure that the HT32F1656/1655 devices are suitable for use in a wide range of applications, especially in areas such as white goods application control, power monitors, alarm systems, consumer products, handheld equipment, data logging applications, motor control, fingerprint recognition and so on.



Features

- Core
 - 32-bit ARM® Cortex™-M3 processor core
 - Up to 72 MHz operating frequency
 - 1.25 DMIPS/MHz (Dhrystone 2.1)
 - Single-cycle multiplication and hardware division
 - Integrated Nested Vectored Interrupt Controller (NVIC)
 - 24-bit SysTick timer
- On-chip Memory
 - Up to 256 KB on-chip Flash memory for instruction/data and options storage
 - 32 KB on-chip SRAM
 - Supports multiple boot modes
- Flash Memory Controller
 - Flash accelerator for maximum efficiency
 - 32-bit word programming with In System Programming Interface (ISP) and In Application Programming (IAP)
 - Flash protection capability to prevent illegal access
- Reset and Clock Control Units
 - Supply supervisor: Power-on Reset (POR), Brown-out Detector (BOD) and Programmable Low Voltage Detector (LVD)
 - External 4 to 16 MHz crystal oscillator
 - External 32,768 Hz crystal oscillator
 - Internal 8MHz RC oscillator trimmed to 1% accuracy at 3.3 V operating voltage and 25°C operating temperature
 - Internal 32kHz RC oscillator
 - Integrated system clock PLL
 - Independent clock gating bits for peripheral clock sources
- Power management
 - Single 3.3 V power supply: 2.7 V to 3.6 V
 - Integrated 1.8 V LDO regulator for core and peripheral power supply
 - V_{BAT} battery power supply for RTC and backup registers
 - Three power domains: 3.3 V, 1.8 V and Backup
 - Four power saving modes: Sleep, Deep-Sleep1, Deep-Sleep2, Power-Down
- Analog to Digital Converter
 - 12-bit SAR ADC engine
 - Up to 1 Msps conversion rate - 1 μ s at 56 MHz, 1.17 μ s at 72 MHz
 - Up to 16 external analog input channels
 - Supply voltage range: 2.7 V ~ 3.6 V
 - Conversion range: $V_{REF+} \sim V_{REF-}$
- Analog Operational Amplifier/Comparator
 - Two Operational Amplifiers or Comparator functions which are software configurable
 - Supply voltage range: 2.7 V ~ 3.6 V

- IO ports
 - Up to 80 GPIOs
 - Port A, B, C, D, E are mapped as 16 external interrupts – EXTI
 - Almost all I/O pins are 5 V-tolerant except for pins shared with analog inputs
- PWM Generation and Capture Timers – GPTM
 - Two 16-bit General-Purpose Timers – GPTM
 - Up to 4-channel with PWM, Compare Output or Input Capture function for each GPTM
 - External trigger input
- Motor Control Timer – MCTM
 - Two 16-bit up, down, up/down auto-reload counters
 - 16-bit programmable prescaler allowing dividing the counter clock frequency by any factor between 1 and 65536
 - Input Capture function
 - Compare Match Output
 - PWM waveform generation with Edge-aligned and Center-aligned Counting Modes
 - Single Pulse Mode Output
 - Complementary Outputs with programmable dead-time insertion
 - Encoder interface controller with two inputs using quadrature decoder
 - Supports 3-phase motor control and hall sensor interface
 - Break input to force the timer's output signals into a reset or fixed condition
- Basic Function Timer – BFTM
 - Two 32-bit compare/match count-up counters – no I/O control features
 - One shot mode – counting stops after a match condition
 - Repetitive mode – restart counter after a match condition
- Watchdog Timer
 - 12-bit down counter with 3-bit prescaler
 - Interrupt or reset event for the system
 - Programmable watchdog timer window function
 - Registers write protection function
- Real Time Clock
 - 32-bit up-counter with a programmable prescaler
 - Alarm function
 - Interrupt and Wake-up event
- Inter-integrated Circuit – I²C
 - Supports both master and slave modes with a frequency of up to 1 MHz
 - Provide an arbitration function and clock synchronization
 - Supports 7-bit and 10-bit addressing modes and general call addressing
 - Supports slave multi-addressing mode with maskable address
- Serial Peripheral Interface – SPI
 - Supports both master and slave mode
 - Frequency of up to 36 MHz for master mode and 24MHz for slave mode
 - FIFO Depth: 8 levels
 - Multi-master and multi-slave operation

- Universal Synchronous Asynchronous Receiver Transmitter – USART
 - Supports both asynchronous and clocked synchronous serial communication modes
 - Asynchronous operating baud rate up to 4.5 MHz and synchronous operating rate up to 9 MHz
 - Capability of full duplex communication
 - Fully programmable characteristics of serial communication including: word length, parity bit, stop bit and bit order
 - Error detection: Parity, overrun, and frame error
 - Support Auto hardware flow control mode - RTS, CTS
 - IrDA SIR encoder and decoder
 - RS485 mode with output enable control
 - FIFO Depth: 16×9 bits for both receiver and transmitter
- Universal Asynchronous Receiver Transmitter – UART
 - Asynchronous serial communication operating baud-rate up to 4.5 MHz
 - Capability of full duplex communication
 - Fully programmable characteristics of serial communication including: word length, parity bit, stop bit and bit order
 - Error detection: Parity, overrun, and frame error
 - FIFO Depth: 16×9 bits for both receiver and transmitter
- Smart Card Interface – SCI
 - Supports ISO 7816-3 Standard
 - Character mode
 - Single transmit buffer and single receive buffer
 - 11-bit ETU (elementary time unit) counter
 - 9-bit guard time counter
 - 24-bit general purpose waiting time counter
 - Parity generation and checking
 - Automatic character retry on parity error detection in transmission and reception modes
- Inter-IC Sound – I²S
 - Master or slave mode
 - Mono and stereo
 - I²S-justified, Left-justified, and Right-justified mode
 - 8/16/24/32-bit sample size with 32-bit channel extended
 - 8×32 -bit Tx & Rx FIFO with PDMA supported
 - 8-bit Fractional Clock Divider with rate control
- Cyclic Redundancy Check – CRC
 - Support CRC16 polynomial: 0x8005, X₁₆+X₁₅+X₂+1
 - Support CCITT CRC16 polynomial: 0x1021, X₁₆+X₁₂+X₅+1
 - Support IEEE-802.3 CRC32 polynomial: 0x04C11DB7, X₃₂+X₂₆+X₂₃+X₂₂+X₁₆+X₁₂+X₁+X₁₀+X₈+X₇+X₅+X₄+X₂+X+1
 - Support 1's complement, byte reverse & bit reverse operation on data and checksum
 - Support byte, half-word & word data size
 - Programmable CRC initial seed value
 - CRC computation done in 1 AHB clock cycle for 8-bit data and 4 AHB clock cycles for 32-bit data
 - Support PDMA to complete a CRC computation of a block of memory

- Peripheral Direct Memory Access – PDMA
 - 8 channels with trigger source grouping
 - 8-/16-/32-bit width data transfer
 - Supports Address increment, decrement or fixed mode
 - 4-level programmable channel priority
 - Auto reload mode
 - Supports trigger sources:
ADC, SPI, USART, UART, I²C, I²S, EBI, GPTM, MCTM, SCI and software request
- External Bus Interface – EBI
 - Programmable interface for various memory types
 - Translate the AHB transactions into the appropriate external device protocol
 - Memory bank regions and independent chip select control for each memory bank
 - Programmable timings to support a wide range of devices
 - Support page read mode
 - Automatic translation when AHB transaction width and external memory interface width is different
 - Write buffer to decrease the stalling of the AHB write burst transaction
 - Support multiplexed and non-multiplexed address and data line configurations
 - Up to 25 affress lines
 - Up to 16-bit data bus width
- Universal Serial Bus Device Controller – USB
 - Complies with USB 2.0 full-speed (12Mbps) specification
 - On-chip USB full-speed transceiver
 - 1 control endpoint (EP0) for control transfer
 - 3 single-buffered endpoints for bulk and interrupt transfer
 - 4 double-buffered endpoints for bulk, interrupt and isochronous transfer
 - 1KB EP-SRAM used as the endpoint data buffers
- Debug Support
 - Serial Wire Debug Port – SW-DP
 - 6 instruction comparators and 2 literal comparators for hardware breakpoint or code / literal patch
 - 4 comparators for hardware watchpoints
 - 1-bit asynchronous trace (TRACESWO)
- Package and Operation Temperature
 - 40-pin QFN; 48/64/100-pin LQFP package
 - Operation temperature range: -40°C to +85°C

Device Information

Table 1. HT32F1656/1655 Series Features and Peripheral List

Peripherals		HT32F1656	HT32F1655
Main Flash (KB)		255	128
Option Bytes Flash		1	1
SRAM (KB)		32	32
Timers	MCTM	2	
	GPTM	2	
	BFTM	2	
	RTC	1	
	WDT	1	
Communication	USB	1	
	SPI	2	
	USART	2	
	UART	2	
	I ² C	2	
	I ² S	1	
	SCI	1	
	EBI	1	
	CRC-16/32	1	
GPIO		Up to 80	
EXTI		16	
12-bit ADC		1	
Number of channels		16 Channels	
OPA/Comparator		2	
GPIO		Up to 80	
CPU frequency		Up to 72 MHz	
Operating voltage		2.7 V ~ 3.6 V	
Operating temperature		-40°C ~ +85°C	
Package		40-pin QFN; 48/64/100-pin LQFP	

Block Diagram

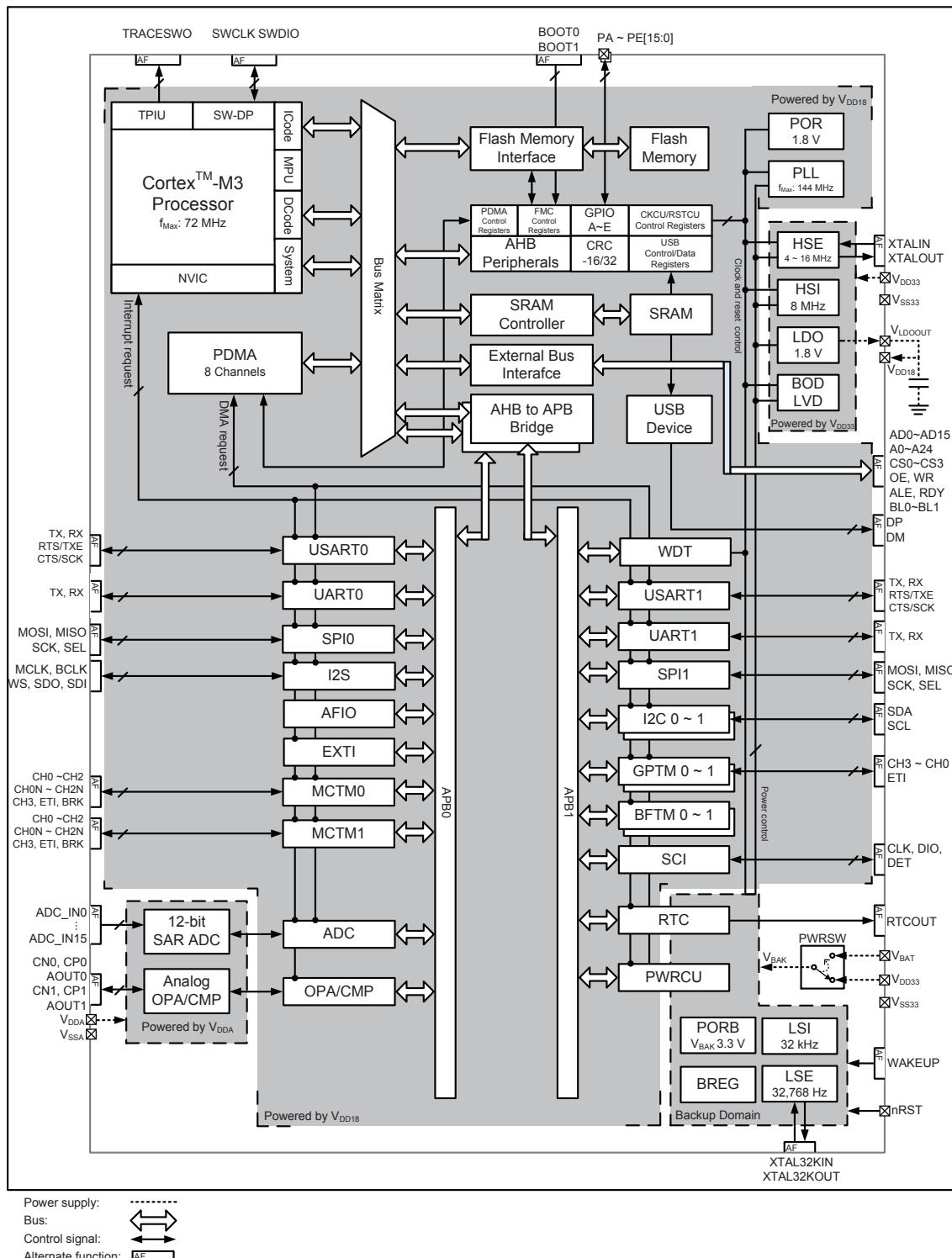


Figure 1. HT32F1656/1655 Block Diagram

2 Document Conventions

The conventions used in this document are shown in the following table.

Table 2. Document Conventions

Notation	Example	Description						
0x	0x5a05	The number string with a 0x prefix indicates a hexadecimal number.						
0xnnnn_nnnn	0x2000_0100	32-bit Hexadecimal address or data.						
b	b0101	The number string with a lowercase b prefix indicates a binary number.						
NAME [n]	ADDR [5]	Specific bit of NAME. NAME can be a register or field of register. For example, ADDR [5] means bit 5 of ADDR register (field).						
NAME [m:n]	ADDR [11:5]	Specific bits of NAME. NAME can be a register or field of register. For example, ADDR [11:5] means bit 11 to 5 of ADDR register (field).						
X	b10X1	Don't care notation which means any value is allowed.						
RW	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td style="text-align: center;">19</td> <td style="text-align: center;">18</td> </tr> <tr> <td>SERDYIE</td> <td>PLLRDYIE</td> </tr> <tr> <td>RW 0</td> <td>RW 0</td> </tr> </table>	19	18	SERDYIE	PLLRDYIE	RW 0	RW 0	Software can read and write to this bit.
19	18							
SERDYIE	PLLRDYIE							
RW 0	RW 0							
RO	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td style="text-align: center;">3</td> <td style="text-align: center;">2</td> </tr> <tr> <td>HSIRDY</td> <td>HSERDY</td> </tr> <tr> <td>RO 1</td> <td>RO 0</td> </tr> </table>	3	2	HSIRDY	HSERDY	RO 1	RO 0	Software can only read this bit. A write operation will have no effect.
3	2							
HSIRDY	HSERDY							
RO 1	RO 0							
RC	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> </tr> <tr> <td>PDF</td> <td>BAK_PORF</td> </tr> <tr> <td>RC 0</td> <td>RC 1</td> </tr> </table>	1	0	PDF	BAK_PORF	RC 0	RC 1	Software can only read this bit. Read operation will clear it to 0 automatically.
1	0							
PDF	BAK_PORF							
RC 0	RC 1							
WC	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td style="text-align: center;">3</td> <td style="text-align: center;">2</td> </tr> <tr> <td>SERDYF</td> <td>PLLRDYF</td> </tr> <tr> <td>WC 0</td> <td>WC 0</td> </tr> </table>	3	2	SERDYF	PLLRDYF	WC 0	WC 0	Software can read this bit or clear it by writing 1. Writing a 0 will have no effect.
3	2							
SERDYF	PLLRDYF							
WC 0	WC 0							
WO	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td style="text-align: center;">31</td> <td style="text-align: center;">30</td> </tr> <tr> <td>DB_CKSRC</td> <td></td> </tr> <tr> <td>WO 0</td> <td>WO 0</td> </tr> </table>	31	30	DB_CKSRC		WO 0	WO 0	Software can only write to this bit. A read operation always returns 0.
31	30							
DB_CKSRC								
WO 0	WO 0							
Reserved	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> </tr> <tr> <td>LLRDY</td> <td>Reserved</td> </tr> <tr> <td>RO 0</td> <td></td> </tr> </table>	1	0	LLRDY	Reserved	RO 0		Reserved bit(s) for future use. Data read from these bits is not well defined and should be treated as random data. Normally these reserved bits should be set to a 0 value. Note that reserved bit must be kept at reset value.
1	0							
LLRDY	Reserved							
RO 0								
Word		Data length of a word is 32-bit.						
Half-word		Data length of a half-word is 16-bit.						
Byte		Data length of a byte is 8-bit.						

3 System Architecture

The system architecture of the HT32F1656/1655 series of devices that includes the ARM® Cortex™-M3 processor, bus architecture and memory organization will be described in the following sections. The Cortex™-M3 is a next generation processor core which offers many new features. Integrated and advanced features make the Cortex™-M3 processor suitable for market products that require microcontrollers with high performance and low power consumption. In brief, The Cortex™-M3 processor includes three AHB-Lite buses known as ICode, DCode and System buses. All memory accesses of the Cortex™-M3 processor are executed on the three buses according to the different purposes and the target memory spaces. The memory organization uses a Harvard architecture, pre-defined memory map and up to 4 GB of memory space, making the system flexible and extendable.

ARM® Cortex™-M3 Processor

The Cortex™-M3 is a general purpose 32-bit processor core especially suitable for products requiring high performance and low power consumption microcontrollers. It offers many new features such as a Thumb-2 instruction sets, hardware divider, low latency interrupt respond time, atomic bit-banding access and multiple buses for simultaneous accesses. The Cortex™-M3 processor is based on the ARMv7 architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex™-M3:

- Internal Bus Matrix connected with ICode bus, DCode bus, System bus, Private Peripheral Bus (PPB) and debug accesses (AHB-AP)
- Nested Vectored Interrupt Controller (NVIC)
- Flash Patch and Breakpoint (FPB)
- Data Watchpoint and Trace (DWT)
- Instrument Trace Macrocell (ITM)
- Memory Protection Unit (MPU)
- Serial Wire debug Port (SW-DP)
- Serial Wire JTAG Debug Port (SWJ-DP)
- Embedded Trace Macrocell (ETM)
- Trace Port Interface Unit (TPIU)

The following figure shows the Cortex™-M3 processor block diagram. For more information, refer to the ARM® Cortex™-M3 Technical Reference Manual.

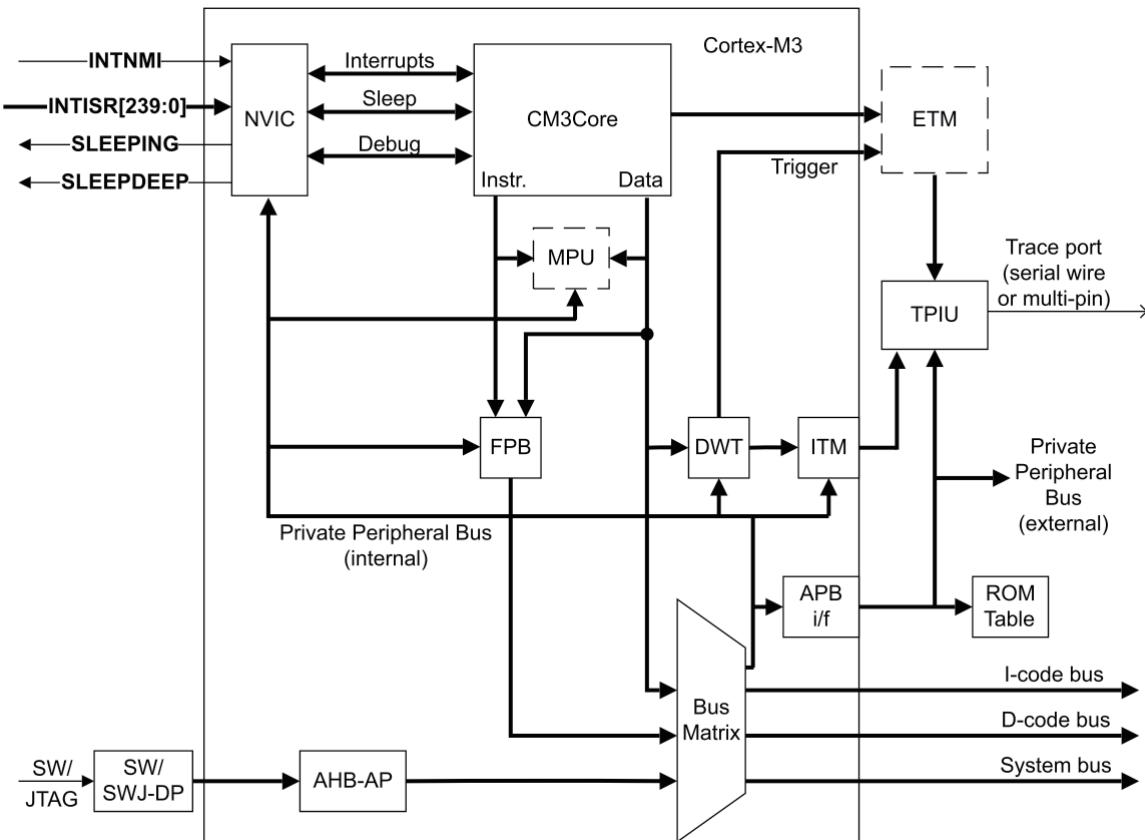


Figure 2. Cortex™-M3 Block Diagram

Bus Architecture

The HT32F1656/1655 series consist of four masters and six slaves in the bus architecture. The Cortex™-M3 ICode, DCode, System bus and Peripheral Direct Memory Access (PDMA) are the masters while the internal SRAM access bus, the internal Flash memory access bus, the AHB peripherals access bus, External Bus Interface (EBI) and the two AHB to APB bridges are the slaves. The ICode bus is used for instruction and vector fetches from the Code region (0x0000_0000 ~ 0x1FFF_FFFF) to the Cortex™-M3 core. The DCode bus is used for loading/storing data and also for debug access of the Code region. Similarly, the System bus is used for instruction/vector fetches, data loading/storing and debugging access of the system regions. The system regions include the internal SRAM region and the peripheral region. All of the four master buses are based on 32-bit Advanced High-performance Bus-Lite (AHB-Lite) protocol. The following figure shows the bus architecture of the HT32F1656/1655 series.

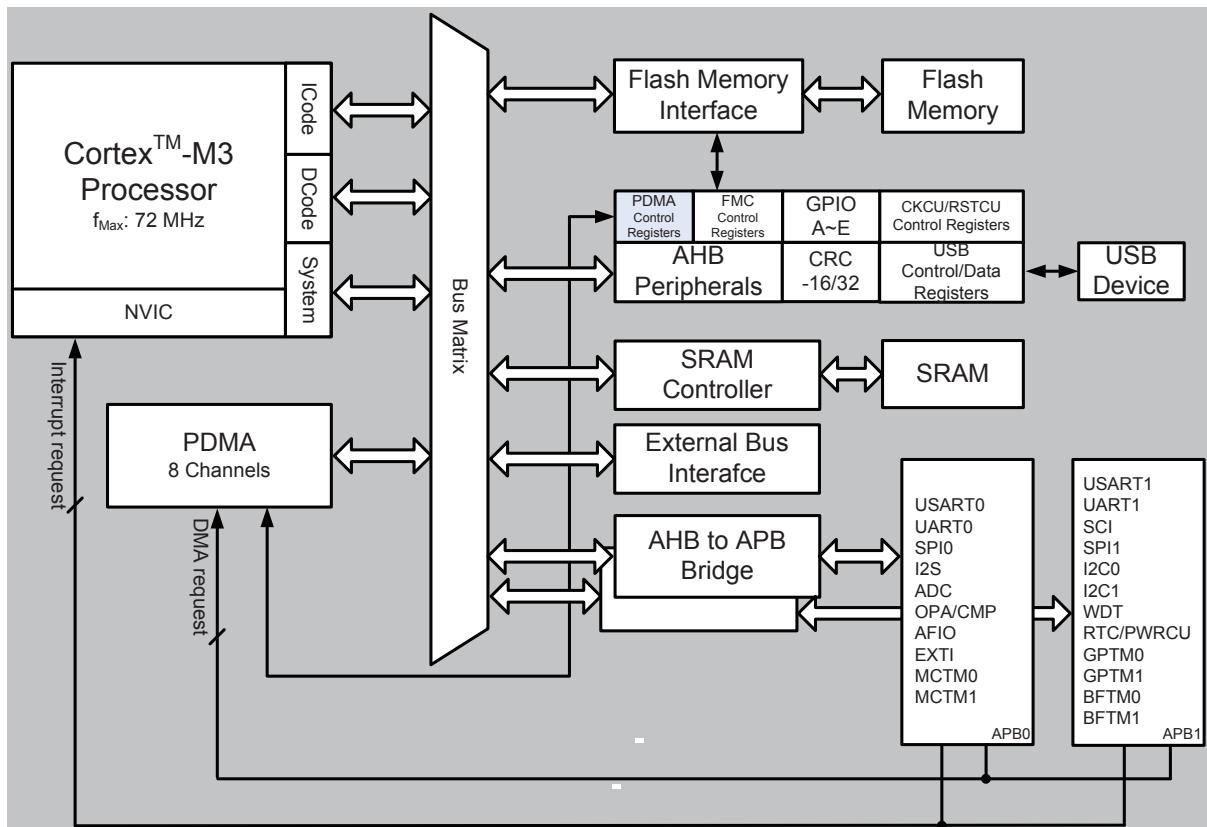


Figure 3. HT32F1656/1655 Bus Architecture

Memory Organization

The ARM® Cortex™-M3 processor is structured in Harvard architecture which can use separate buses to fetch instructions and load/store data. The instruction code and data are both located in the same memory address space but in different address ranges. The maximum address range of the Cortex™-M3 is 4 GB since it has 32-bit bus address width. Additionally, a pre-defined memory map is provided by the Cortex™-M3 processor to reduce the software complexity of repeated implementation of different device vendors. However, some regions are used by the ARM® Cortex™-M3 system peripherals. Refer to the ARM® Cortex™-M3 Technical Reference Manual for more information. The following figure shows the memory map of HT32F1656/1655 series of devices, including Code, SRAM, peripheral, and other pre-defined regions.

Memory Map

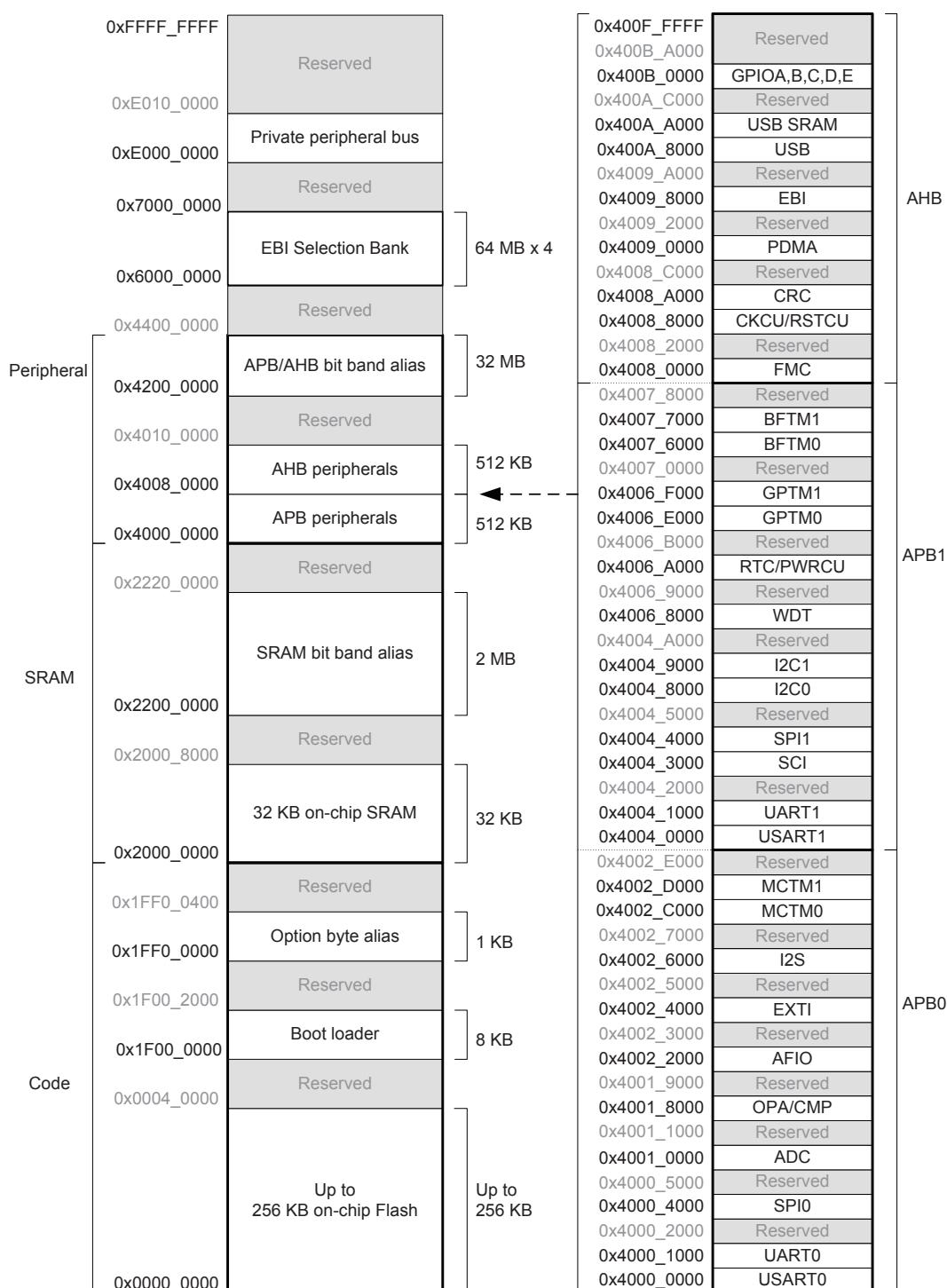


Figure 4. HT32F1656/1655 Memory Map

Table 3. HT32F1656/1655 Register Map

Start Address	End Address	Peripheral	Bus	Register map
0x4000_0000	0x4000_0FFF	USART0		
0x4000_1000	0x4000_1FFF	UART0		
0x4000_2000	0x4000_3FFF	Reserved		
0x4000_4000	0x4000_4FFF	SPI0		
0x4000_5000	0x4000_FFFF	Reserved		
0x4001_0000	0x4001_0FFF	ADC		
0x4001_1000	0x4001_7FFF	Reserved		
0x4001_8000	0x4001_8FFF	OPA/Comparator		
0x4001_9000	0x4002_1FFF	Reserved		
0x4002_2000	0x4002_2FFF	AFIO		
0x4002_3000	0x4002_3FFF	Reserved		
0x4002_4000	0x4002_4FFF	EXTI		
0x4002_5000	0x4002_5FFF	Reserved		
0x4002_6000	0x4002_6FFF	I ² S		
0x4002_7000	0x4002_BFFF	Reserved		
0x4002_C000	0x4002_CFFF	MCTM0		
0x4002_D000	0x4002_DFFF	MCTM1		
0x4002_E000	0x4003_FFFF	Reserved		
0x4004_0000	0x4004_0FFF	USART1	APB	
0x4004_1000	0x4004_1FFF	UART1		
0x4004_2000	0x4004_2FFF	Reserved		
0x4004_3000	0x4004_3FFF	SCI		
0x4004_4000	0x4004_4FFF	SPI1		
0x4004_5000	0x4004_7FFF	Reserved		
0x4004_8000	0x4004_8FFF	I ² C0		
0x4004_9000	0x4004_9FFF	I ² C1		
0x4004_A000	0x4006_7FFF	Reserved		
0x4006_8000	0x4006_8FFF	WDT		
0x4006_9000	0x4006_9FFF	Reserved		
0x4006_A000	0x4006_AFFF	RTC/PWRCU		
0x4006_B000	0x4006_DFFF	Reserved		
0x4006_E000	0x4006_EFFF	GPTM0		
0x4006_F000	0x4006_FFFF	GPTM1		
0x4007_0000	0x4007_5FFF	Reserved		
0x4007_6000	0x4007_6FFF	BFTM0		
0x4007_7000	0x4007_7FFF	BFTM1		
0x4007_8000	0x4007_FFFF	Reserved		

Start Address	End Address	Peripheral	Bus	Register map
0x4008_0000	0x4008_1FFF	FMC		
0x4008_2000	0x4008_7FFF	Reserved		
0x4008_8000	0x4008_9FFF	CKCU/RSTCU		
0x4008_A000	0x4008_BFFF	CRC		
0x4008_C000	0x4008_FFFF	Reserved		
0x4009_0000	0x4009_1FFF	PDMA		
0x4009_2000	0x4009_7FFF	Reserved		
0x4009_8000	0x4009_9FFF	EBI		
0x4009_A000	0x400A_7FFF	Reserved	AHB	
0x400A_8000	0x400A_9FFF	USB		
0x400A_A000	0x400A_BFFF	USB SRAM		
0x400A_C000	0x400A_FFFF	Reserved		
0x400B_0000	0x400B_1FFF	GPIOA		
0x400B_2000	0x400B_3FFF	GPIOB		
0x400B_4000	0x400B_5FFF	GPIOC		
0x400B_6000	0x400B_7FFF	GPIOD		
0x400B_8000	0x400B_9FFF	GPIOE		
0x400B_A000	0x400F_FFFF	Reserved		

Embedded Flash Memory

The Holtek HT32F1656/1655 devices provide 256/128 KB on-chip Flash memory which is located at address 0x0000_0000. It supports byte, half-word, and word access operations. Note that the Flash memory only supports read operations for the Cortex™-M3 ICode or DCode bus access. Any write operations to the Flash memory (via DCode bus) will cause a bus fault exception. The Flash memory has a capacity of 256/128 pages. Each page has a memory capacity of 1 KB and can be erased independently. A 32-bit programming interface provides the capability of changing bits from 1 to 0. A data storage or firmware upgrade can be implemented using several methods such as In System Programming (ISP), In Application Programming (IAP) or In Circuit Programming (ICP). For more information, refer to the Flash Memory Controller section.

Embedded SRAM Memory

The Holtek HT32F1656/1655 devices contain 32 KB on-chip SRAM which is located at address 0x2000_0000. It support byte, half-word and word access operations. In order to reduce the time of read-modify-write operations, the Cortex™-M3 provides a bit-banding function to perform a single atomic bit operation. Users can modify a single bit in the SRAM bit-band region by accessing the corresponding bit-band alias. For more information about bit-binding, refer to the ARM® Cortex™-M3 Technical Reference Manual. The following formulas and examples show how to access a bit in the bit-band region by calculating the bit-band alias.

$$\text{Bit-band alias} = \text{Bit-band base} + (\text{byte offset} * 32) + (\text{bit number} * 4)$$

For example, if you want to access bit 7 of address 0x2000_0200, the bit-band alias is:

$$\text{Bit-band alias} = 0x2200_0000 + (0x200 * 32) + (7 * 4) = 0x2200_401C$$

Writing to address 0x2200_401C will cause bit 7 of address 0x2000_0200 change while a read to address 0x2200_401C will return 0x01 or 0x00 according to the value of bit 7 at the SRAM address 0x2000_0200.

AHB Peripherals

The address of the AHB peripherals ranges from 0x4008_0000 to 0x400F_FFFF. Some peripherals such as Clock Control Unit, Reset Control Unit and Flash Memory Controller are connected to the AHB bus directly. The AHB peripherals clocks are always enabled after a system reset. Access to registers for these peripherals can be achieved directly via the AHB bus. Note that all peripheral registers in the AHB bus support only word access.

APB Peripherals

The address of APB peripherals ranges from 0x4000_0000 to 0x4007_FFFF. An APB to AHB bridge provides access capability between the Cortex™-M3 and the APB peripherals. Additionally, the APB peripheral clocks are disabled after a system reset. Software must enable the peripheral clock by setting up the APBCCRn register in the Clock Control Unit before accessing the corresponding peripheral register. Note that the APB to AHB bridge will duplicate the half-word or byte data to word width when a half-word or byte access is performed on the APB peripheral registers. In other words, the access result of a half-word or byte access on the APB peripheral register will vary depending on the data bit width of the access operation on the peripheral registers.

4

Flash Memory Controller (FMC)

Introduction

The Flash Memory Controller, FMC, provides all the necessary functions, pre-fetch buffer and branch cache for the embedded on-chip Flash Memory. Since the access speed of the Flash Memory is slower than the CPU, a wide access interface with a pre-fetch buffer is provided for the Flash Memory in order to reduce the CPU waiting time which will cause CPU instruction execution delays. Flash Memory word program/page erase functions are also provided.

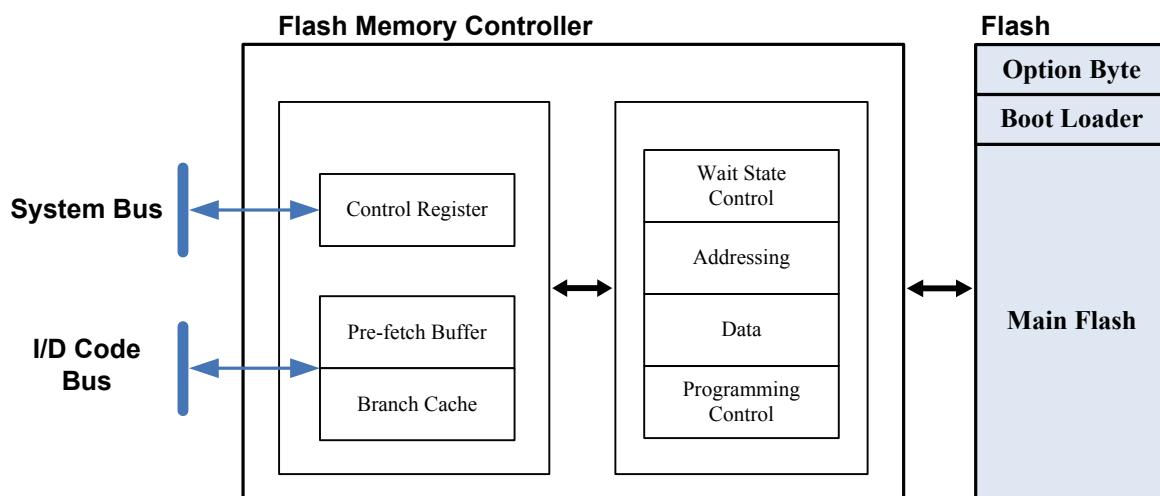


Figure 5. Flash Memory Controller Block Diagram

Features

- Up to 256 KB on-chip Flash memory for storing instruction/data and options
 - HT32F1656: 255 KB + 1 KB (instruction/data + option byte)
 - HT32F1655: 128 KB + 1 KB (instruction/data + option byte)
- Page size of 1 KB
- Wide access interface with pre-fetch buffer and branch cache to reduce instruction gaps
- Page erase and mass erase capability
- 32-bit word programming
- Interrupt function to indicate end of Flash memory operations or an error occurs
- Flash read protection to prevent illegal code/data access
- Page erase/program protection to prevent unexpected operation

Functional Descriptions

Flash Memory Map

The following figure is the Flash memory map of the HT32F1656/1655 devices in which the address ranges from 0x0000_0000 to 0x1FFF_FFFF (0.5 GB). The address from 0x1F00_0000 to 0x1F00_1FFF is mapped to the Boot Loader with a capacity of 8 KB. Additionally, the region addressed from 0x1FF0_0000 to 0x1FF0_03FF is the Option Byte Block with a capacity of 1 KB. The memory mapping on system view is shown as below.

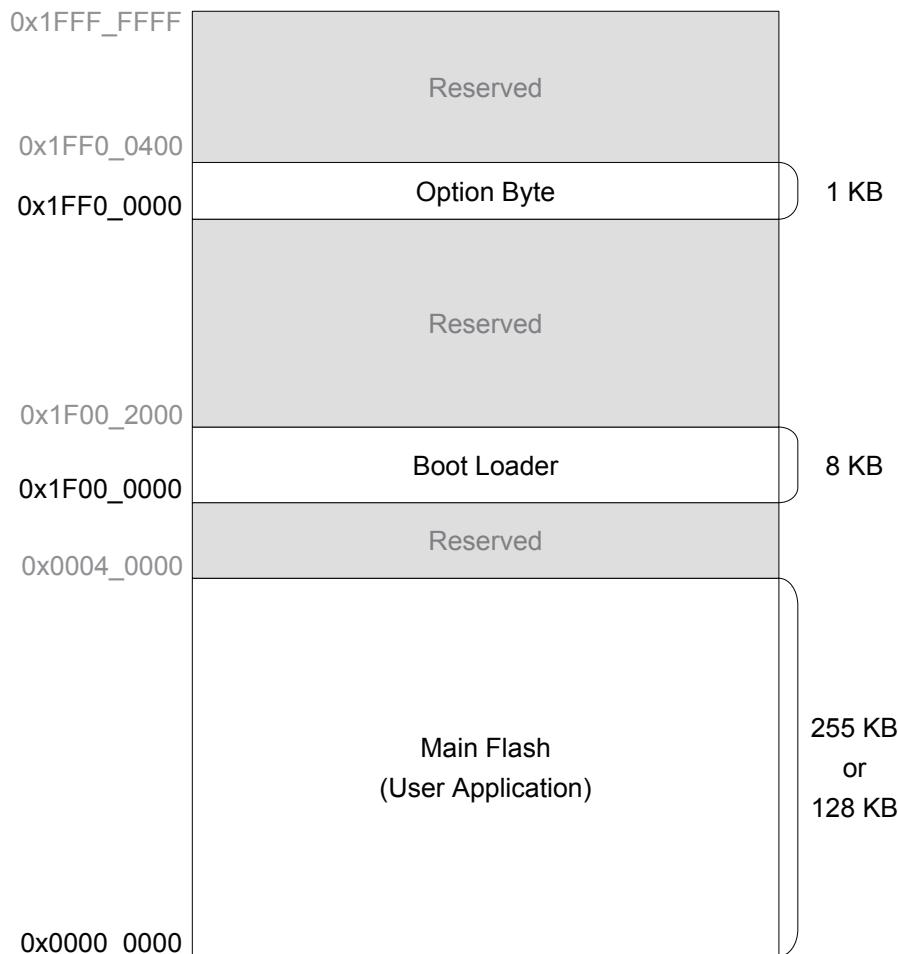


Figure 6. Flash Memory Map

Flash Memory Architecture

The Flash memory consists of 129/256 KB Main Flash organized into 129/256 pages with 1 KB capacity per page and a 8 KB Information Block for the Boot Loader. The main Flash memory contains a total of 129/256 pages which can be erased individually. The following table shows the base address, size and protection setting bit of each page.

Table 4. Flash Memory and Option Byte

Block	Name	Address	Page Protection Bit	Size
Main Flash	Page 0	0x0000_0000 ~ 0x0000_03FF	OB_PP [0]	1 KB
	Page 1	0x0000_0400 ~ 0x0000_07FF		1 KB
	Page 2	0x0000_0800 ~ 0x0000_0BFF		1 KB
	Page 3	0x0000_0C00 ~ 0x0000_0FFF	OB_PP [1]	1 KB

	Page 252	0x0003_F000 ~ 0x0003_F3FF	OB_PP [126]	1 KB
	Page 253	0x0003_F400 ~ 0x0003_F7FF		1 KB
	Page 254	0x0003_F800 ~ 0x0003_FBFF	OB_PP [127]	1 KB
	Option Byte	0x1FF0_0000 ~ 0x1FF0_03FF	OB_CP [1]	1 KB
Information Block	Boot Loader	0x1F00_0000 ~ 0x1F00_1FFF	NA	8 KB

Notes: The Information Block stores the boot loader - this block can not be programmed or erased by user.

Wait State Setting

When the CPU clock, HCLK, is greater than the access speed of the Flash memory, then wait state cycles must be inserted during the CPU fetch instructions or load data from Flash memory. The wait state can be changed by setting the WAIT [2:0] bits of the Flash Cache and Pre-fetch Control Register, CFCR. In order to match the wait state requirement, the following two rules should be considered.

- HCLK clock is switched from low to high frequency:
Change the wait state setting first and then switch the HCLK clock.
- HCLK clock is switched from high to low frequency:
Switch the HCLK clock first and then change the wait state setting.

The following table shows the relationship between the wait state cycle and the CPU clock HCLK. The default wait state is 0 since the High Speed Internal oscillator HSI which operates at a frequency of 8 MHz is selected as the HCLK clock source after reset.

Table 5. Relationship between wait state cycle and HCLK

Wait State Cycle	HCLK
0	0 MHz < HCLK ≤ 24 MHz
1	24 MHz < HCLK ≤ 48 MHz
2	48 MHz < HCLK ≤ 72 MHz

Booting Configuration

The devices provide three kinds of boot modes which can be selected using the BOOT0 and BOOT1 pins. The BOOT0 and BOOT1 pins are sampled during a power-on reset or a system reset. Once the logic value on these pins has been determined, the first 4 words of vector will be remapped to the corresponding source according to the boot mode. The boot modes are shown in the following table.

Table 6. Booting Modes

Boot mode selection pins		Mode	Descriptions
BOOT1	BOOT0		
0	0	SRAM	Vector source is SBVT0 ~ SBVT3
0	1	Boot Loader	Vector source is Boot Loader
1	X	Main Flash	Vector source is Main Flash memory

The Vector Mapping Control Register (VMCR) is provided to change the vector remapping setting temporarily after a device reset. The initial reset value of the VMCR register is determined by the BOOT0 and BOOT1 pins which will be sampled during the reset duration.

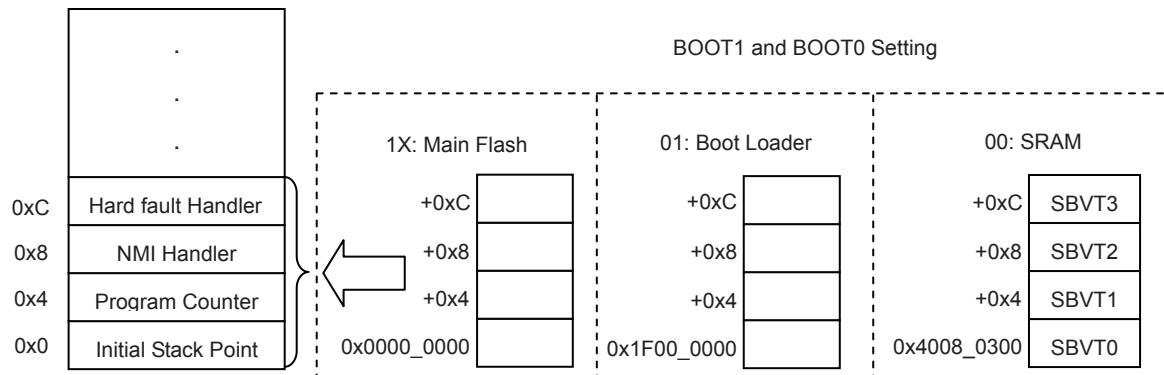


Figure 7. Vector Remapping

Page Erase

The FMC provides a page erase function which is used to initialize the contents of a Flash memory page to a high state. Each page can be erased independently without affecting the contents of other pages. The following steps show the access sequence of the register for a page erase operation.

- Check the OPCR register to confirm that no Flash memory operation is in progress (OPM [3:0] equal to 0xE or 0x6). Otherwise, wait until the previous operation has been finished.
- Write the page address into the TADR register
- Write the page erase command into the OCMR register (CMD [3:0] = 0x8).
- Send the page erase command to the FMC by setting the OPCR register (set OPM [3:0] = 0xA).
- Wait until all the operations have been completed by checking the value of the OPCR register (OPM [3:0] equal to 0xE).
- Read and verify the page if required using DCODE access.

Note that a correct target page address must be confirmed. The software may run out of control if the target erase page is being used to fetch codes or to access data. The FMC will not provide any notification when this occurs. Additionally, the page erase operation will be ignored on protected pages. A Flash operation error interrupt will be triggered by the FMC if the OREIEN bit in the OIER register is set. The software can check the PPEF bit in the OISR register to detect this condition in the interrupt handler. The following figure shows the page erase operation flow.

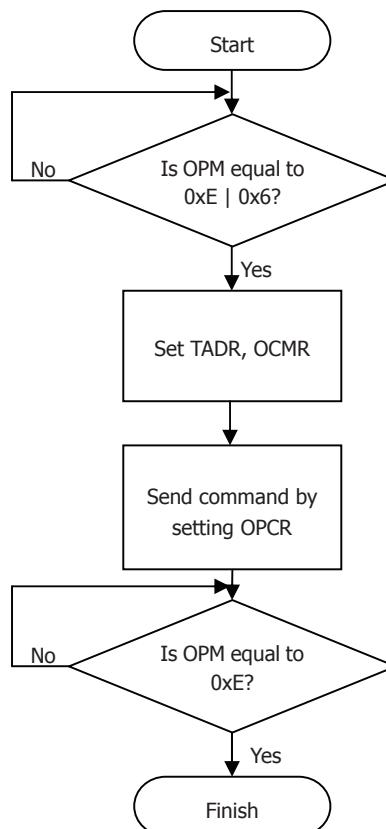


Figure 8. Page Erase Operation Flowchart

Mass Erase

The FMC provides a mass erase function which is used to initialize the complete Flash memory contents to a high state. The following steps show the mass erase operation register access sequence.

- Check the OPCR register to confirm that no Flash memory operation is in progress (OPM [3:0] equal to 0xE or 0x6). Otherwise, wait until the previous operation has been finished.
- Write the mass erase command into the OCMR register (CMD [3:0] = 0xA).
- Send the mass erase command to the FMC by setting the OPCR register (set OPM [3:0] = 0xA).
- Wait until all operations have been completed by checking the value of the OPCR register (OPM [3:0] equal to 0xE).
- Read and verify the Flash memory if required using DCODE access.

Since all Flash contents will be reset to the value of 0xFFFF_FFFF, the mass erase operation can be implemented by an application that runs in SRAM or by the debug tool that accesses the FMC registers directly. An application executes on the Flash memory will not trigger a mass erase operation. The following figure shows the mass erase operation flow.

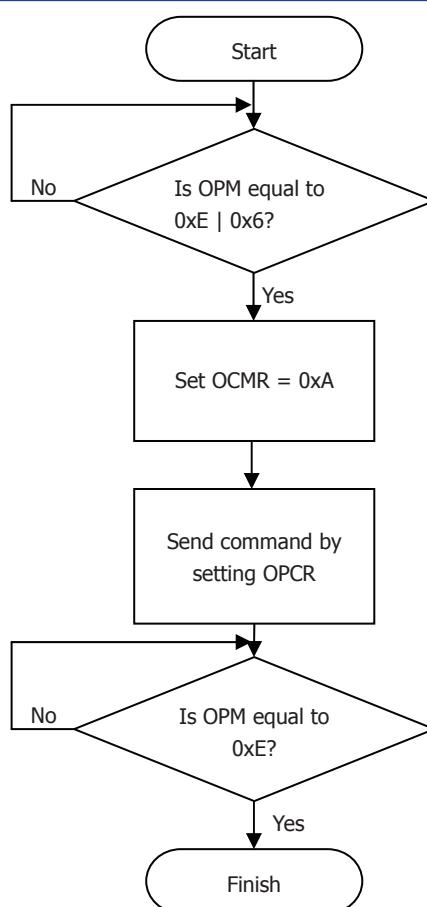


Figure 9. Mass Erase Operation Flowchart

Word Programming

The FMC provides a 32-bit word programming function which is used to modify the Flash memory contents. The following steps show the word programming operation register access sequence.

- Check the OPCR register to confirm that no Flash memory operation is in progress (OPM [3:0] equal to 0xE, or 0x6). Otherwise, wait until the previous operation has been finished.
- Write the word address into the TADR register. Write the word data into the WRDR register.
- Write the word programming command into the OCMR register (CMD [3:0] = 0x4).
- Send the word programming command to the FMC by setting the OPCR register (set OPM [3:0] = 0xA).
- Wait until all operations have been completed by checking the value of the OPCR register (OPM [3:0] equal to 0xE).
- Read and verify the Flash memory if required using DCODE access.

Note that the word programming operation can not be applied to the same address twice. Successive word programming operations to the same address must be separated by a page erase operation. Additionally, the word programming operation will be ignored on protected pages. A Flash operation error interrupt will be triggered by the FMC if the OREIEN bit in the OIER register is set. The software can check the PPEF bit in the OISR register to detect this condition in the interrupt handler. The following figure shows the word programming operation flow.

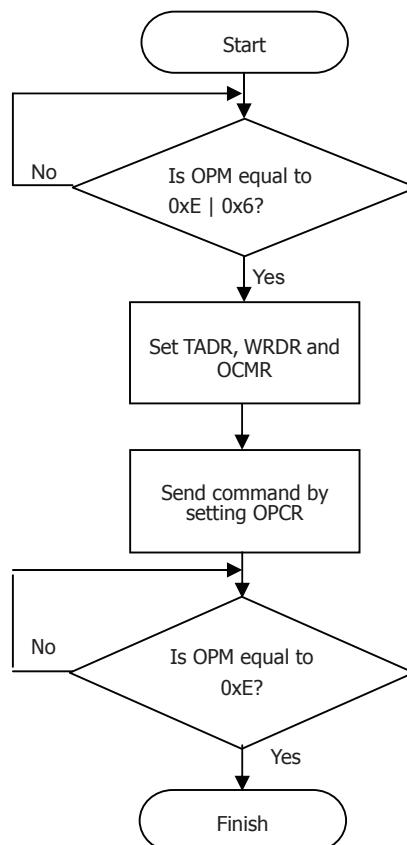


Figure 10. Word Programming Operation Flowchart

Option Byte Description

The Option Byte region can be treated as an independent Flash memory in which the base address is **0x1FF0_0000**. The following table shows the functional description and the Option Byte memory map.

Table 7. Option Byte Memory Map

Option Byte	Offset	Description	Reset Value
Option Byte Base Address = 0x1FF0_0000			
OB_PP	0x000	OB_PP [n]: Main Flash Page Erase/Program Protection (n = 0 ~ 127 for page 0 ~ page 254)	0xFFFF_FFFF
	0x004	0: Main Flash Page 2n and 2n+1 Erase/Program Protection is enabled 1: Main Flash Page 2n and 2n+1 Erase/Program Protection is disabled	0xFFFF_FFFF
	0x008		0xFFFF_FFFF
	0x00C		0xFFFF_FFFF
OB_CP	0x010	OB_CP [0]: Flash Security Protection 0: Flash Security protection is enabled 1: Flash Security protection is disabled	0xFFFF_FFFF
		OB_CP [1]: Option Byte Erase/Program Protection 0: Option Byte protection is enabled 1: Option Byte protection is disabled	
		OB_CP [31:2]: Reserved	
OB_CK	0x020	OB_CK [31:0]: Option Byte Checksum OB_CK should be set as the sum of the 5 words Option Byte content, of which the address offset ranges from 0x000 to 0x010 (0x000 + 0x004 + 0x008 + 0x00C + 0x010), when the content of the OB_PP or OB_CP register is not equal to 0xFFFF_FFFF.	0xFFFF_FFFF

Page Erase/Program Protection

The FMC provides page erase/program protection functions to prevent inadvertent operations on the Flash memory. The page erase or word programming command will not be accepted by the FMC on protected pages. When the page erase or word programming command is sent to the FMC on a protected page, the PPEF bit in the OISR register will then be set by the FMC. If the OREIEN bit in the OIER register is also set to 1 then the Flash operation error interrupt will be triggered by the FMC. The page protection function can be individually enabled for each page by configuring the OB_PP [127:0] bit field in the Option Byte. If a page erase operation is executed on the Option Byte region, all the Flash Memory page protection functions will be disabled. The page protection function of the Option Byte is enabled by clearing the OB_CP [1] bit to 0. Once the Option Byte has been protected, the only way to disable its protection function is to execute a mass erase operation. The following table shows the access permission of the Main Flash page when the page protection is enabled.

Table 8. Access Permission of Protected Main Flash Page

Mode Operation	ISP/IAP	ICP/Debug mode	Boot from SRAM
DCODE Read	O	O	O
Program	X	X	X
Page Erase	X	X	X
Mass Erase	O	O	O

Notes: 1. The write protection setup is based on specific pages. The above access permission only affects the pages that the protection function has enabled. Other pages are not affected.
2. The Main Flash page protection is configured by OB_PP [127:0]. The Option Byte page protection is configured by the OB_CP [1] bit.

The following steps show the page erase/program protection procedure register access sequence:

- Check the OPCR register to confirm that no Flash memory operation is in progress (OPM [3:0] equal to 0xE or 0x6). Otherwise, wait until the previous operation has been finished.
- Write the OB_PP address into the TADR register (TADR = 0x1FF0_0000 ~ 0x1FF0_000C).
- Write the data which indicates the protection function of the corresponding page is enabled or disabled into the WRDR register (0: Enabled, 1: Disabled).
- Write the word programming command into the OCMR register (CMD [3:0] = 0x4).
- Send the word programming command to the FMC by setting the OPCR register (set OPM [3:0] = 0xA).
- Wait until all operations have been finished by checking the value of the OPCR register (OPM [3:0] equals to 0xE).
- Read and verify the OB_PP if required using DCODE access.
- Before to active the new OB_PP setting, the OB_CK must be updated according to the Option Byte checksum rule.
- Apply a system reset to active the new setting.

Security Protection

The FMC provides a security protection function to prevent illegal code/data access on the Flash memory. This function is useful for protecting the software/firmware from illegal users. The function is activated by configuring the OB_CP [0] bit in the Option Byte. Once the function has been enabled, all the main Flash DCODE access, programming and page erase operations will not be allowed except for the user's application. However, the mass erase operation will still be accepted by the FMC in order to disable this security protection function. The following table shows the access permission of Flash memory when the security protection is enabled.

Table 9. Access Permission When Security Protection Is Enabled

Mode Operation	User application ⁽¹⁾	ICP/Debug mode	Boot from SRAM
DCODE Read	O	X ⁽²⁾	X ⁽²⁾
Program	O ⁽¹⁾	X	X
Page Erase	O ⁽¹⁾	X	X
Mass Erase	O	O	O

Notes: 1. User application means the software that is executed or booted from the Main Flash memory with the SW debugger disconnected. However the Option Byte and the page 0 are still protected in which Programming and Page Erase operations can not be executed.
2. When the SW debugger is connected or the executing application is booted from SRAM, all the DCODE read operation to all Flash memory regions will return with the value of 0.

The following steps show the security protection procedure register access sequence:

- Check the OPCR register to confirm that no Flash memory operation is in progress (OPM [3:0] equal to 0xE or 0x6). Otherwise, wait until the previous operation has been finished.
- Write the OB_CP address to the TADR register (TADR = 0x1FF0_0010).
- Write the data into the WRDR register to clear OB_CP [0] bit to 0.
- Write the word programming command into the OCMR register (CMD [3:0] = 0x4).
- Send the word programming command to the FMC by setting the OPCR register (set OPM = 0xA).
- Wait until all operations have been finished by checking the value of the OPCR register (OPM [3:0] equals to 0xE).
- Read and verify the OB_CP if required using DCODE access.
- Before to activate the security protection function, the OB_CK field must be updated according to the Option Byte checksum rule.
- Apply a system reset to active the new setting.

Register Map

The following table shows the FMC registers and reset values.

Table 10. FMC Register Map

Register	Offset	Description	Reset Value
FMC Base Address = 0x4008_0000			
TADR	0x000	Flash Target Address Register	0x0000_0000
WRDR	0x004	Flash Write Data Register	0x0000_0000
OCMR	0x00C	Flash Operation Command Register	0x0000_0000
OPCR	0x010	Flash Operation Control Register	0x0000_000C
OIER	0x014	Flash Operation Interrupt Enable Register	0x0000_0000
OISR	0x018	Flash Operation Interrupt Status Register	0x0001_0000
PPSR	0x020		0xFFFF_FFFF
	0x024		0xFFFF_FFFF
	0x028	Flash Page Erase/Program Protection Status Register	0xFFFF_FFFF
	0x02C		0xFFFF_FFFF
CPSR	0x030	Flash Security Protection Status Register	0xFFFF_FFFF
VMCR	0x100	Flash Vector Mapping Control Register	0x0000_000X
CFCR	0x200	Flash Cache and Pre-fetch Control Register	0x0000_13D1
SBVT0	0x300	SRAM Booting Vector 0 (Stack Point)	0x2000_8000
SBVT1	0x304	SRAM Booting Vector 1 (Program Counter)	0x2000_0155
SBVT2	0x308	SRAM Booting Vector 2 (NMI Handler)	0x0000_0000
SBVT3	0x30C	SRAM Booting Vector 3 (Hard Fault Handler)	0x0000_0000

Note: "X" means various reset values which depend on the Device, Flash value, option byte value, or power on reset setting.

Register Descriptions

Flash Target Address Register – TADR

This register specifies the target address of the page erase and word programming operations.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
TADB								
Type/Reset	RW 0							
23 22 21 20 19 18 17 16								
TADB								
Type/Reset	RW 0							
15 14 13 12 11 10 9 8								
TADB								
Type/Reset	RW 0							
7 6 5 4 3 2 1 0								
TADB								
Type/Reset	RW 0							

Bits	Field	Descriptions
[31:0]	TADB	<p>Flash Target Address Bits</p> <p>For programming operations, the TADR register specifies the address where the data is written. Since the programming length is 32 bits, TADR shall be set as word-aligned (4 bytes). The TADB [1:0] will be ignored during programming operations. For page erase operations, the TADR register contains the page address which is going to be erased. Since the page size is 1 KB, TADB [9:0] will be ignored in order to limit the target address as 1 KB-aligned. The Option Byte which has a 1KB capacity ranges from 0x1FF0_0000 to 0x1FF0_03FF is the. This field is used to specify the Flash Memory address which must be within the range from 0x0000_0000 to 0xFFFF_FFFF. Otherwise, an Invalid Target Address interrupt will be generated if the corresponding interrupt enable bit is set.</p>

Flash Write Data Register – WRDR

This register stores the data to be written into the TADR register for programming operations.

Offset: 0x004

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
WRDB								
Type/Reset	RW 0							
23 22 21 20 19 18 17 16								
WRDB								
Type/Reset	RW 0							
15 14 13 12 11 10 9 8								
WRDB								
Type/Reset	RW 0							
7 6 5 4 3 2 1 0								
WRDB								
Type/Reset	RW 0							

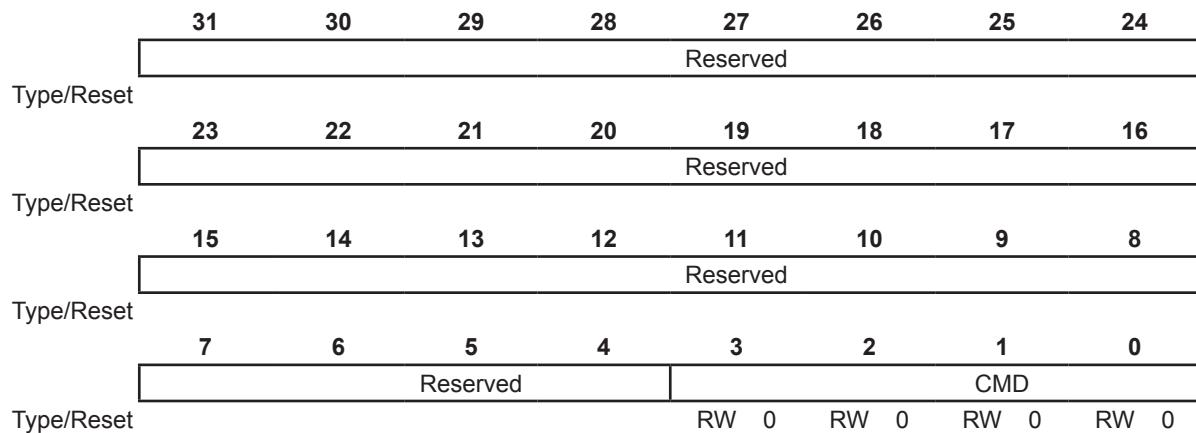
Bits	Field	Descriptions
[31:0]	WRDB	Flash Write Data Bits The data value for programming operation.

Flash Operation Command Register – OCMR

This register is used to specify the Flash operation commands that include word program, page erase and mass erase.

Offset: 0x00C

Reset value: 0x0000_0000



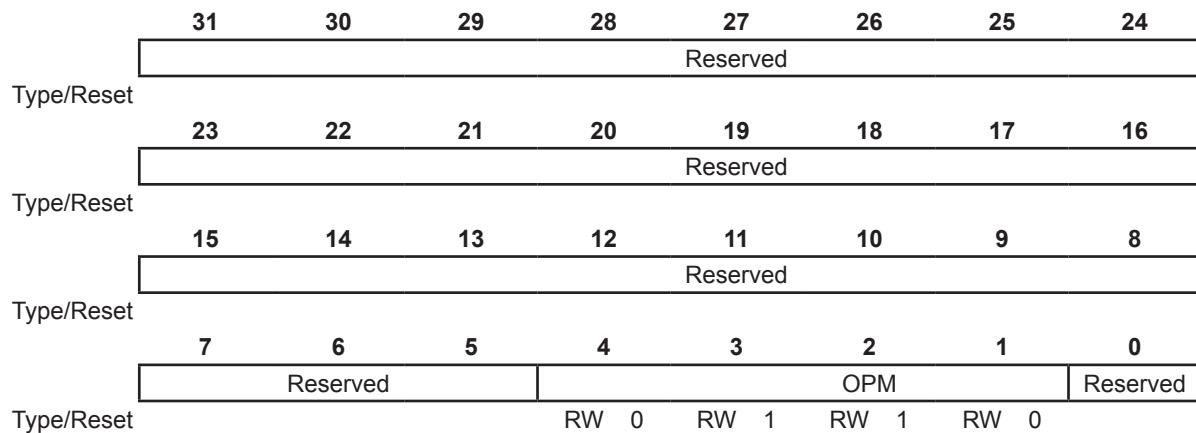
Bits	Field	Descriptions												
[3:0]	CMD	<p>Flash Operation Command</p> <p>The following table shows the definitions of the operation command bits CMD [3:0] which determine the Flash Memory operation. If an invalid command is set and the IOCMIEN bit is equal to 1, an Invalid Operation Command interrupt will occur.</p> <table border="1"> <thead> <tr> <th>CMD [3:0]</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0x0</td><td>Idle - default</td></tr> <tr> <td>0x4</td><td>Word program</td></tr> <tr> <td>0x8</td><td>Page erase</td></tr> <tr> <td>0xA</td><td>Mass erase</td></tr> <tr> <td>Others</td><td>Reserved</td></tr> </tbody> </table>	CMD [3:0]	Description	0x0	Idle - default	0x4	Word program	0x8	Page erase	0xA	Mass erase	Others	Reserved
CMD [3:0]	Description													
0x0	Idle - default													
0x4	Word program													
0x8	Page erase													
0xA	Mass erase													
Others	Reserved													

Flash Operation Control Register – OPCR

This register is used for controlling the command commitment and checking the status of the FMC operations.

Offset: 0x010

Reset value: 0x0000_000C



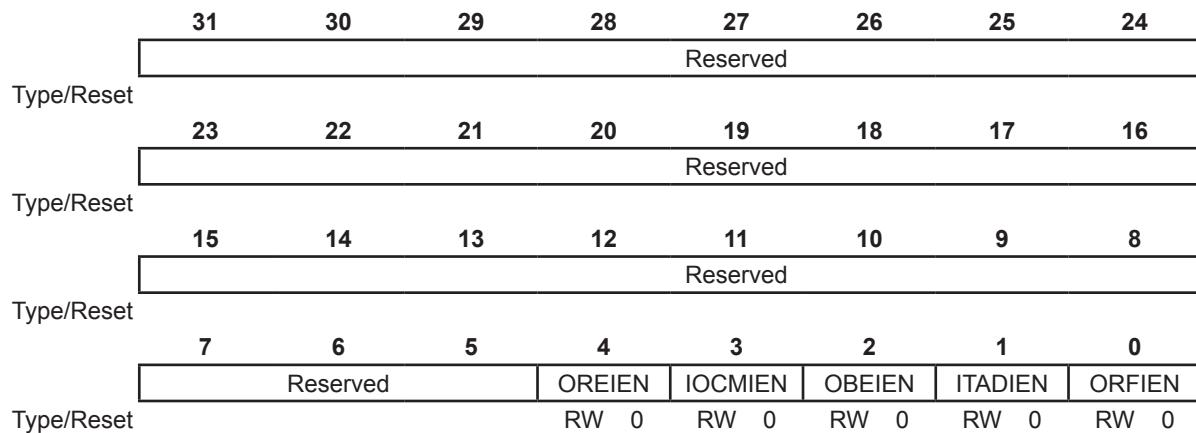
Bits	Field	Descriptions										
[4:1]	OPM	<p>Operation Mode</p> <p>The following table shows the operation modes of the FMC. User can commit the command which is set by the OCMR register for the FMC according to the address alias setting in the TADR register. The contents of the TADR, WRDR, and OCMR registers should be prepared before setting this register. After all the operations have been finished, the OPM field will be set as 0xE by the FMC hardware. The Idle mode can be set when all the operations have been finished for power saving purposes. Note that the operation status should be checked before the next operation is executed on the FMC. The contents of the TADR, WRDR, OCMR, and OPCR registers should not be changed until the previous operation has been finished.</p>										
<table border="1"> <thead> <tr> <th>OPM [3:0]</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0x6</td><td>Idle (default)</td></tr> <tr> <td>0xA</td><td>Commit command to Main Flash</td></tr> <tr> <td>0xE</td><td>All operation finished on Main Flash</td></tr> <tr> <td>Others</td><td>Reserved</td></tr> </tbody> </table>			OPM [3:0]	Description	0x6	Idle (default)	0xA	Commit command to Main Flash	0xE	All operation finished on Main Flash	Others	Reserved
OPM [3:0]	Description											
0x6	Idle (default)											
0xA	Commit command to Main Flash											
0xE	All operation finished on Main Flash											
Others	Reserved											

Flash Operation Interrupt Enable Register – OIER

This register is used to enable or disable the FMC interrupt function. The FMC generates interrupts to the controller when corresponding interrupt enable bits are set.

Offset: 0x014

Reset value: 0x0000_0000



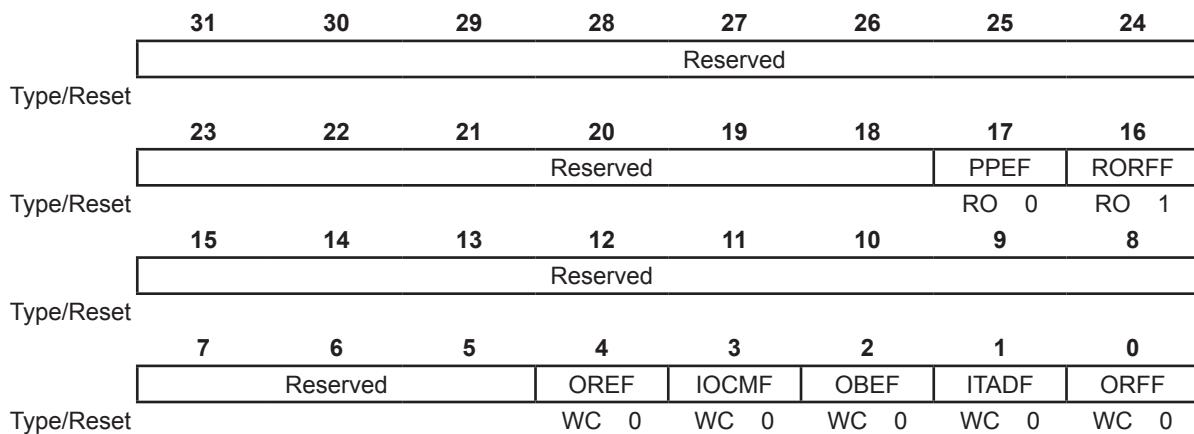
Bits	Field	Descriptions
[4]	OREIEN	Operation Error Interrupt Enable 0: Operation Error interrupt is disabled 1: Operation Error interrupt is enabled
[3]	IOCMIEN	Invalid Operation Command Interrupt Enable 0: Invalid Operation Command interrupt is disabled 1: Invalid Operation Command interrupt is enabled
[2]	OBEIEN	Option Byte Check Sum Error Interrupt Enable 0: Option Byte Check Sum Error interrupt is disabled 1: Option Byte Check Sum Error interrupt is enabled
[1]	ITADIEN	Invalid Target Address Interrupt Enable 0: Invalid Target Address interrupt is disabled 1: Invalid Target Address interrupt is enabled
[0]	ORFIEN	Operation Finished Interrupt Enable 0: Operation Finish interrupt is disabled 1: Operation Finish interrupt is enabled

Flash Operation Interrupt and Status Register – OISR

This register indicates the FMC interrupt status which is used to check if a Flash operation has finished otherwise an error occurs. The status bits are available when the corresponding interrupt enable bits in the OIER register are set.

Offset: 0x018

Reset value: 0x0001_0000



Bits	Field	Descriptions
[17]	PPEF	Page Erase/Program Protected Error Flag 0: Page Erase/Program Protected Error does not occur 1: Operation error occurs due to an invalid page erase/program operation being applied to a protected page This bit is reset by hardware once a new Flash operation command is committed.
[16]	RORFF	Raw Operation Finished Flag 0: The last Flash operation command has not yet finished 1: The last Flash operation command has finished This bit is directly connected to the Flash memory for debugging purpose.
[4]	OREF	Operation Error Flag 0: No Flash operation error occurred 1: The last Flash operation is failed This bit will be set when any Flash operation error such as an invalid command, program error and erase error, etc., occurs. The OREIEN bit in the OIER register is set. Reset this bit by writing a 1.

Bits	Field	Descriptions
[3]	IOCMF	Invalid Operation Command Flag 0: No invalid Flash operation command was set 1: An invalid Flash operation command has been written to the OCMR register The IOCM interrupt will occur if the IOCMEN bit in the OIER register is set. Reset this bit by writing a 1.
[2]	OBEF	Option Byte Checksum Error Flag 0: Option Byte Checksum is correct 1: Option Byte Checksum is incorrect The OBE interrupt will occur if the OBEIEN bit in the OIER register is set. Reset this bit by writing a 1.
[1]	ITADF	Invalid Target Address Flag 0: The target address TADR is valid 1: The target address TADR is invalid The data in the TADR field must have a range from 0x0000_0000 to 0x1FFF_FFFF. An ITAD interrupt will occur if the ITADIEN bit in the OIER register is set. Reset this bit by writing a 1.
[0]	ORFF	Operation Finished Flag 0: Flash operation has not finished 1: Last Flash operation has finished The ORF interrupt will occur if the ORFIEN bit in the OIER register is set. Reset this bit by writing a 1.

Flash Page Erase/Program Protection Status Register – PPSR

This register indicates the page protection status of the Flash Memory.

Offset: 0x020 ~ 0x02C

Reset value: 0xFFFF_FFFF

	31	30	29	28	27	26	25	24
PPSBn								
Type/Reset	RO X							
	23	22	21	20	19	18	17	16
PPSBn								
Type/Reset	RO X							
	15	14	13	12	11	10	9	8
PPSBn								
Type/Reset	RO X							
	7	6	5	4	3	2	1	0
PPSBn								
Type/Reset	RO X							

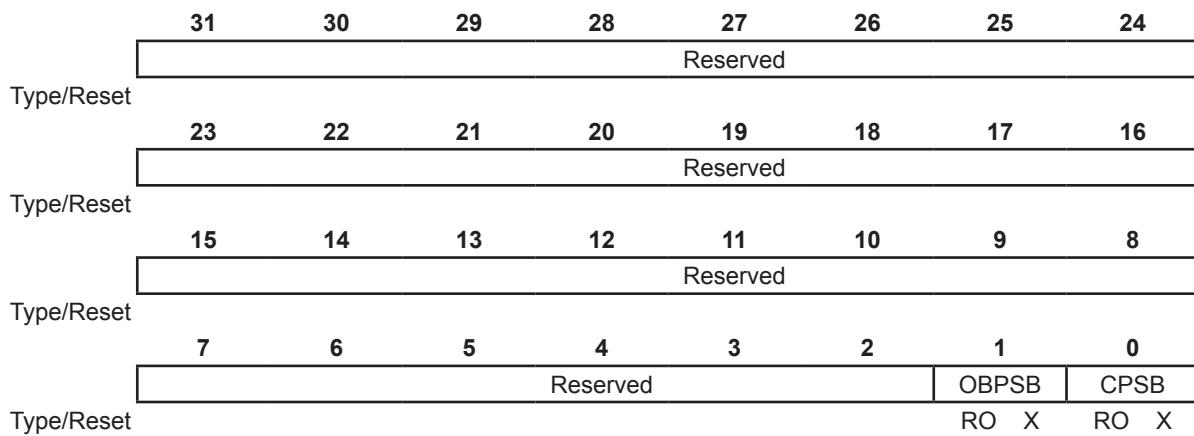
Bits	Field	Descriptions
[126:0]	PPSBn	<p>Page n Erase/Program Protection Status Bits (n = 0 ~ 127)</p> <p>0: The corresponding page are protected 1: The corresponding page are not protected</p> <p>The content of this register is not dynamically updated and will only be reloaded by the Option Byte loader which is activated when any kind of reset occurs. The erase or program function of the specific pages is not allowed when the corresponding bits of the PPSR registers are reset. The reset value of the bits PPSR [127:0] is determined by the Option Byte, OB_PP [127:0]. The other bits of the OB_PP and PPSR registers are reserved for future usage.</p>

Flash Security Protection Status Register – CPSR

This register indicates the Flash Memory Security protection status. The content of this register is not dynamically updated and will only be reloaded by the Option Byte loader which is activated when any kind of reset occurs.

Offset: 0x030

Reset value: 0xFFFF_FFFF



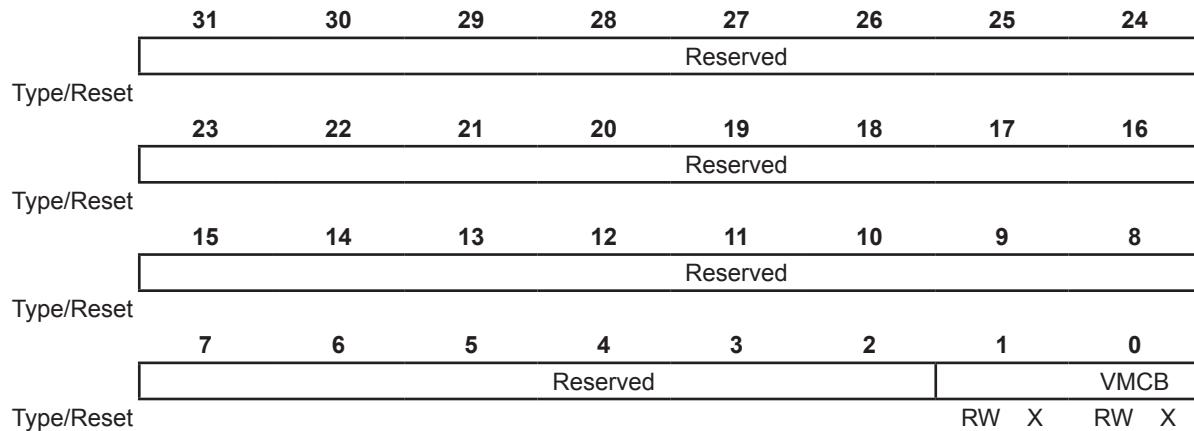
Bits	Field	Descriptions
[1]	OBPSB	Option Byte Page Erase/Program Protection Status Bit 0: The Option Byte page is protected. 1: The Option Byte page is not protected. The reset value of OPBSB is determined by the OB_CP [1] bit in the Option Byte.
[0]	CPSB	Flash Memory Security Protection Status Bit 0: Flash Memory Security protection is enabled 1: Flash Memory Security protection is disabled The reset value of the CPSB bit is determined by the OB_CP [0] bit in the Option Byte.

Flash Vector Mapping Control Register – VMCR

This register is used to control the vector mapping. The reset value of the VMCR register is determined by the status of the external booting pins, BOOT0 and BOOT1 during the power on reset period.

Offset: 0x100

Reset value: 0x0000_000X



Bits	Field	Descriptions							
[1:0]	VMCB	Vector Mapping Control Bit The VMCB bits are used to control the mapping source of the first 4-word vectors addressed from 0x0 to 0xC. The following table shows the vector mapping setup.							
		BOOT1	BOOT0	VMCB [1:0]	Descriptions				
		Low	Low	00	SRAM booting mode The vector mapping source is SBVT0~3.				
		Low	High	01	Boot Loader mode The vector mapping source is the Boot Loader area.				
		High	Low	10	Main Flash mode The vector mapping source is the Main Flash Memory area.				
		High	High	11					

The reset value of the VMCR register is determined by the pins status of the external booting pins BOOT1 and BOOT0 during a power on reset and system reset. However, when the application program is executed, the vector mapping setting can be temporarily changed by configuring the VMCB bits to correctly access the first 4-word vectors in the Flash memory, especially when the CPU is booted from the Boot Loader or the SRAM region.

Flash Cache and Pre-fetch Control Register – CFCR

This register is used for controlling the FMC cache and pre-fetch module.

Offset: 0x200

Reset value: 0x0000_13D1

	31	30	29	28	27	26	25	24	
Reserved									
Type/Reset	23	22	21	20	19	18	17	16	
Reserved									
Type/Reset	15	14	13	12	11	10	9	8	
FHLAEN Reserved CE Reserved									
Type/Reset	RW	0	RW 1						
7 6 5 4 3 2 1 0									
Type/Reset	RW	1	RW 1			RW	0	RW	1
DCDB Reserved PFBE Reserved WAIT									

Bits	Field	Descriptions
[16]	FZWPSEN	<p>Flash Zero Wait-state Power Saving Enable Bit</p> <p>0: Flash zero wait-state power saving is disabled 1: Flash zero wait-state power saving is enabled</p> <p>This bit can only be set to 1 to reduce the Flash memory operating current when the Flash memory is operated in zero wait-state. This bit has no effect when the wait-state setting is changed to non-zero.</p>
[15]	FHLAEN	<p>Flash Memory Half-cycle Access Enable Bit</p> <p>0: Half-cycle access is disabled 1: Half-cycle access is enabled</p> <p>This bit can only be set when the Flash memory is operated in zero wait-state. Setting this bit to 1 will reduce the Flash memory operation current further when the system frequency HCLK is less than a frequency of 12 MHz. This bit has no effect when the wait-state setting is changed to non-zero.</p>
[12]	CE	<p>Branch Cache Enable Bit</p> <p>0: Branch cache is disabled 1: Branch cache is enabled</p> <p>The branch cache is enabled in default state.</p>

Bits	Field	Descriptions															
[7]	DCDB	<p>DCODE data Cacheable Enable Bit</p> <p>0: DCODE data is Cacheable 1: DCODE data is Non-cacheable</p> <p>The DCODE data is non-cacheable in default state.</p>															
[4]	PFBE	<p>Pre-fetch Buffer Enable Bit</p> <p>0: Pre-fetch buffer is disabled 1: Pre-fetch buffer is enabled</p> <p>The pre-fetch buffer is enabled in default state. When the pre-fetch buffer is disabled, the instruction and data are provided directly by the Flash memory.</p>															
[2:0]	WAIT	<p>Flash Wait-state Setting</p> <p>These bits are used to set the HCLK wait clock during a non-sequential Flash access. The actual value of the wait clocks is given by (WAIT [2:0] - 1). Since a wide access interface with a pre-fetch buffer and branch cache is provided, the wait-state of sequential Flash access is very close to zero.</p> <table border="1"> <thead> <tr> <th>WAIT [2:0]</th><th>Wait Status</th><th>Allowed HCLK Range</th></tr> </thead> <tbody> <tr> <td>001</td><td>0</td><td>0 MHz < HCLK ≤ 24 MHz</td></tr> <tr> <td>010</td><td>1</td><td>24 MHz < HCLK ≤ 48 MHz</td></tr> <tr> <td>011</td><td>2</td><td>48 MHz < HCLK ≤ 72 MHz</td></tr> <tr> <td>Others</td><td>Reserved</td><td>Reserved</td></tr> </tbody> </table>	WAIT [2:0]	Wait Status	Allowed HCLK Range	001	0	0 MHz < HCLK ≤ 24 MHz	010	1	24 MHz < HCLK ≤ 48 MHz	011	2	48 MHz < HCLK ≤ 72 MHz	Others	Reserved	Reserved
WAIT [2:0]	Wait Status	Allowed HCLK Range															
001	0	0 MHz < HCLK ≤ 24 MHz															
010	1	24 MHz < HCLK ≤ 48 MHz															
011	2	48 MHz < HCLK ≤ 72 MHz															
Others	Reserved	Reserved															

SRAM Booting Vector Register n – SBVTn, n = 0 ~3

These registers specify the initial values of the Stack Point, Program Counter, NMI handler address and Hard Fault handler address for the SRAM Booting mode.

Offset: 0x300 ~ 0x30C

Reset value: Various depending on the address offset

	31	30	29	28	27	26	25	24	
Type/Reset	RW	X	RW	X	RW	X	RW	X	
	23	22	21	20	19	18	17	16	
	SBVTn								
Type/Reset	RW	X	RW	X	RW	X	RW	X	
	15	14	13	12	11	10	9	8	
	SBVTn								
Type/Reset	RW	X	RW	X	RW	X	RW	X	
	7	6	5	4	3	2	1	0	
	SBVTn								
Type/Reset	RW	X	RW	X	RW	X	RW	X	

Bits	Field	Descriptions																				
[31:0]	SBVTn	<p>SRAM Booting Vector n (n = 0 ~ 3)</p> <p>The SRAM Booting Vector 0 ~ 3 provides a SRAM booting capability for application debugging. The contents of the SBVTn registers are re-mapped into the addresses 0x0 to 0xC of the Flash memory CODE area under the SRAM booting mode. Refer to the description of the VMCR register and BOOT1/BOOT0 boot pins. The following table shows the purpose and reset value of the SBVTn register. The reset value provides a fixed setting for program execution during the SRAM booting mode. These registers can be modified by the debugging tool in order to change the program execution setting. The reset values of the SBVTn register will be reloaded only by a power-on reset. Other reset sources will have no effect.</p>																				
<table border="1"> <thead> <tr> <th>Name</th><th>Address Offset</th><th>Purpose Descriptions</th><th>Reset Value</th></tr> </thead> <tbody> <tr> <td>SBVT0</td><td>0x300</td><td>Stack point</td><td>0x2000_8000</td></tr> <tr> <td>SBVT1</td><td>0x304</td><td>Program counter</td><td>0x2000_0155</td></tr> <tr> <td>SBVT2</td><td>0x308</td><td>NMI handler address</td><td>0x0000_0000</td></tr> <tr> <td>SBVT3</td><td>0x30C</td><td>Hard fault handler address</td><td>0x0000_0000</td></tr> </tbody> </table>			Name	Address Offset	Purpose Descriptions	Reset Value	SBVT0	0x300	Stack point	0x2000_8000	SBVT1	0x304	Program counter	0x2000_0155	SBVT2	0x308	NMI handler address	0x0000_0000	SBVT3	0x30C	Hard fault handler address	0x0000_0000
Name	Address Offset	Purpose Descriptions	Reset Value																			
SBVT0	0x300	Stack point	0x2000_8000																			
SBVT1	0x304	Program counter	0x2000_0155																			
SBVT2	0x308	NMI handler address	0x0000_0000																			
SBVT3	0x30C	Hard fault handler address	0x0000_0000																			

This access width of the registers SBVT0 ~ SBVT3 must be 32-bit (Word access). 8 or 16-bit (Byte or Half-Word) access is not allowed.

5 Power Control Unit (PWRCU)

Introduction

The power consumption can be regarded as one of the most important issues for many embedded system applications. Accordingly the Power Control Unit, PWRCU, provides many types of power saving modes such as Sleep, Deep-Sleep1, Deep-Sleep2, and Power-Down modes. These modes reduce the power consumption and allow the application to achieve the best trade-off between the conflicting demands of CPU operating time, speed and power consumption. The dash line in the Figure 11 indicates the power supply source of three digital power domains.

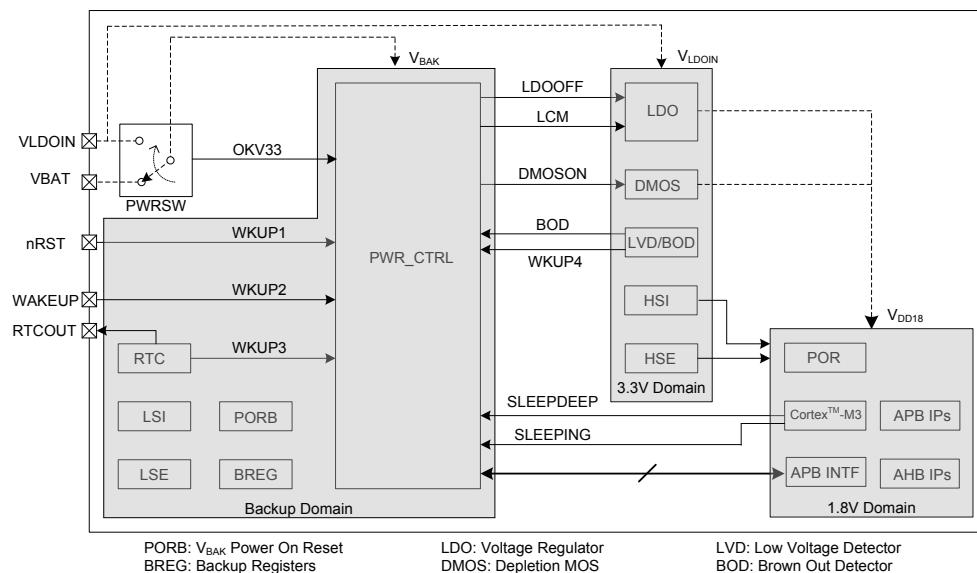


Figure 11. PWRCU Block Diagram

Features

- Three power domains: Backup, 3.3V and 1.8V power domains.
- Four power saving modes: Sleep, Deep-Sleep1, Deep-Sleep2 and Power-Down modes.
- Internal Voltage regulator supplies 1.8 V voltage source.
- Additional Depletion MOS supplies 1.8 V voltage source with low leakage and low operating current.
- Brown Out Detector can issue a system reset or an interrupt when 3.3 V power source (V_{LDOIN}) is lower than 2.6 V.
- Low Voltage Detector can issue an interrupt or wakeup event when V_{LDOIN} is lower than a programmable threshold voltage ranging from 2.7 V to 3.5 V (except 3.3V).
- Battery power (V_{BAT}) for backup domain when V_{LDOIN} is shut down.
- 40 bytes of backup registers powered by V_{BAK} for data storage of user application data when in the Power-Down mode.

Functional Descriptions

Backup Domain

Power Switch

The Backup Domain is powered by the 3.3V power source, V_{LDOIN} , or the battery power source, V_{BAT} , which is selected by the power switch PWRSW. The operating voltage of the power switch ranges from 2.7V to 3.6V. If V_{LDOIN} is lower than V_{BAT} , then the power source will be switched from V_{LDOIN} to V_{BAT} . Therefore, even if V_{LDOIN} is powered down, all the circuitry in the backup domain can operate normally. This means that the backup register contents will be retained, the RTC circuitry will operate normally and the low speed oscillators can keep running.

Backup Domain Reset

The Backup Domain reset sources include the Backup Domain power-on-reset (PORB) and the Backup Domain software reset which is activated by setting the BAKRST bit in the BAKCR register. The PORB signal forces the device to stay in the reset mode until the V_{BAK} is greater than 2.1V. The slew rate of PORB signal is approximately $V_{BAK}/100ms$. Also the application software can trigger Backup Domain software reset by setting the BAKRST bit in the BAKCR register. All registers of PWRCU and RTC will be reset only by the Backup Domain reset.

LSE, LSI and RTC

The Real Time Clock circuitry clock source can be derived from either the Low Speed Internal RC oscillator, LSI, or the Low Speed External Crystal oscillator, LSE. Before entering the power saving mode by executing WFI/WFE instruction, the Cortex™-M3 needs to setup the compare register with an expected wakeup time and enable the wakeup function to achieve the RTC timer wakeup event. After entering the power saving mode for a certain amount of time, the Compare Match flag, CMFLAG, will be asserted to wakeup the device when the compare match event occurs. The details of the RTC configuration for wakeup timer will be described in the RTC chapter.

Backup Registers and Isolation Cells

Ten 32-bit registers, up to 40 bytes, are located in the Backup Domain for user application data storage. These registers are powered by V_{BAK} which constantly supplies power when the 1.8V power is switched off. The Backup Registers are only reset by the Backup Domain power-on-reset, PORB, or the Backup Domain software reset, BAKRST. When the device resumes operation from the 1.8V power, either by Hardware or Software, access to the Backup registers and the RTC registers are disabled by the isolation cells which protect these registers against possible parasitic write accesses. To resume access operations, users can disable these isolation cells by setting the BKISO bit in the LPCR register of the Clock Control Unit to 1.

LDO Power Control

The LDO will be automatically switched off when one of the following conditions occurs:

- The Power-Down or Deep-Sleep 2 mode is entered
- The control bits BODEN = 1, BODRIS=0 and the supply power $V_{LDOIN} \leq 2.6V$

The LDO will be automatically switched on by hardware if any of the following conditions occurs:

- Resume operation from the power saving mode - RTC wakeup, LVD wakeup or WAKEUP pin rising edge
- Detect a falling edge on the external reset pin (nRST)
- The control bit BODEN = 1 and the supply power $V_{LDOIN} > 2.6V$

To enter the Deep-Sleep1 mode, the PWRCU will request the LDO to operate in a low current mode, LCM. To enter the Deep-Sleep2 mode, the PWRCU will turn off the LDO and turn on the DMOS to supply an alternative 1.8V power.

3.3V Power Domain

Voltage Regulator

The voltage regulator, LDO, Depletion MOS, DMOS, Low voltage Detector, LVD, the Brown out Detector, BOD and High Speed Internal oscillator, HSI, all operate under the 3.3 V power domain. The LDO can be configured to operate in either normal mode (LDOOFF=0, SLEEPDEEP=0, I=200mA) or low current mode (LDOOFF=0, SLEEPDEEP=1, I= 100 mA) to supply the 1.8 V power. An alternative 1.8 V power source is the output of the DMOS which has low leakage and drive current characteristics. It is controlled using the DMOSON bit in the BAKCR register. The DMOS output has weak drive current capability and can operate only in the Deep-Sleep2 mode for data retention purposes in the V_{DD18} power domain.

Low Voltage Detector/Brown Out Detector

The Brown Out Detector, BOD, is used to detect if the 3.3 V supply voltage is equal to or lower than 2.6V. When the BODEN bit in the LVDCSR register is set to 1 and the 3.3 V supply voltage is lower than 2.6 V then the BODF flag is active. The PWRCU will regard this as a power down reset situation and then immediately disable the internal LDO regulator when the BODRIS bit is cleared to 0 or issue an interrupt to notify the Cortex™-M3 to execute a power down procedure when the BODRIS bit is set to 1. The Low Voltage Detector, LVD, can also detect whether the supply voltage is lower than a programmable threshold voltage ranging from 2.7 V to 3.5 V. It is selected by the LVDS bits in the LVDCSR register. When a low voltage on the V_{LDOIN} power pin is detected, the LVDF flag will be active and an interrupt will be generated and sent to the Cortex™-M3 if the LVDEN and LVDIWEN bits in the LVDCSR register are set.

High Speed Internal Oscillator

The High Speed Internal Oscillator, HSI, is located in the 3.3 V power domain. When exiting from the Deep-Sleep mode, the HSI clock will be configured as the system clock for a certain period by setting the PSRCEN bit to 1 This bit is located in the Global Clock Control Register, GCCR, in the Clock Control Unit, CKCU. The system clock will not be switched back to the original clock source used before entering the Deep-Sleep mode until the original clock source, which may be either sourced from the PLL or HSE, stabilizes. Also the system will force the HSI oscillator to be the system clock after a wake up from Power-Down mode since a 1.8 V power on reset will occur.

1.8V Power Domain

The main functions that include the APB interface for the backup domain, 1.8 V power on reset (POR), Cortex™-M3 logic, AHB/APB peripherals, and so on are located in this power domain. Once the 1.8V is powered up, the POR will generate a reset sequence (Refer to PORB) on the 1.8 V power domain. Subsequently, to enter the expected power saving mode, the associated control bits including the LDOOFF, DMOSON, and SLEEPDEEP bits must be configured. Then, once a WFI or WFE instruction is executed, the device will enter an expected power saving mode which will be discussed in the following section.

Operation Modes

Run Mode

In the Run mode, the system operates with full functions and all power domains are active. There are two ways to reduce the power consumption in this mode. The first is to slow down the system clock by setting the AHBPRE field in the CKCU AHBCFGR register, and the second is to turn off the unused peripherals clock by setting the APBCCR0 and APBCCR1 registers. Reducing the system clock speed before entering the sleep mode will also help to minimize power consumption.

Additionally, there are several power saving modes to provide maximum optimization between device performance and power consumption.

Table 11. Operation Mode Definitions

Mode name	Hardware Action
Run	After system reset, Cortex™-M3 fetches instructions to execute.
Sleep	1. Cortex™-M3 core clock will be stopped. 2. Peripherals, Flash and SRAM clocks can be stopped.
Deep-Sleep	1. Stop all clocks in the 1.8 V power domain. 2. Disable HSI, HSE, and PLL. 3. Reduce the 1.8 V power domain current by turning on the LDO low current mode or DMOS.
Power-Down	Shut down the 1.8 V power domain

Sleep Mode

By default, only the Cortex™-M3 clock will be stopped in the Sleep mode. Clearing the FMCEN or SRAMEN bit in the CKCU AHBCCR register to 0 will have the effect of stopping the Flash clock or SRAM clock after the system enters the Sleep mode. If it is not necessary for the CPU to access the Flash memory and SRAM in the Sleep mode, it is recommended to clear the FMCEN and SRAMEN bits in the AHBCCR register to minimize power consumption. To enter the Sleep mode, it is only necessary to clear the SLEEPDEEP bit to 0 and execute a WFI or WFE instruction. The system will exit from the Sleep mode via any interrupt or event trigger. The accompanying table provides more information about the power saving modes.

Table 12. Enter/Exit Power Saving Modes

Mode	Mode Entry				Mode Exit
	Cortex™-M3 Instruction	Cortex™-M3 SLEEPDEEP	LDOOFF	DMOSON	
Sleep	WFI or WFE (Takes effect)	0	X	X	WFI: Any interrupt WFE: Any wakeup event ⁽¹⁾ or Any interrupt (NVIC on) or Any interrupt with SEVONPEND=1(NVIC off)
Deep-Sleep1		1	0	0	Any EXTI in event mode or WDT timeout or RTC wakeup or LVD wakeup ⁽²⁾ or WAKEUP pin rising edge USB resume
Deep-Sleep2		1	X	1	RTC wakeup or LVD wakeup ⁽²⁾ or WAKEUP pin rising edge
Power-Down		1	1	0	RTC wakeup or LVD wakeup ⁽²⁾ or WAKEUP pin rising edge or External reset (nRST)

Note: 1. Wakeup event means EXTI line in event mode, RTC, LVD, and WAKEUP pin rising edge

2. If the system allows the LVD activity to wake it up after the system has entered the power saving mode, the LVDEWEN and LVDEN bits in the LVDCSR register must be set to 1 to make sure that the system can be waked up by a LVD event and then the LDO regulator can be turned on when system is woken up from the Deep-Sleep2 and Power-Down modes.

Deep-Sleep Mode

To enter Deep-Sleep mode, configure the registers as shown in the preceding table and execute the WFI or WFE instruction. In the Deep-Sleep mode, all clocks including PLL and high speed oscillator, known as HSI and HSE, will be stopped. In addition, Deep-Sleep1 turns the LDO into low current mode while Deep-Sleep2 turns off the LDO and uses a DMOS to keep 1.8V power. Once the PWRCU receives a wakeup event or an interrupt as shown in the preceding Mode-Exiting table, the LDO will then operate in normal mode and the high speed oscillator will be enabled. Finally, the Cortex™-M3 will return to Run mode to handle the wakeup interrupt if required. A Low Voltage Detection also can be regarded as a wakeup event if the corresponding wakeup control bit LVDEWEN in the LVDCSR register is enabled. The last wakeup event is a transition from low to high on the external WAKEUP pin sent to the PWRCU to resume from Deep-Sleep mode. During the Deep-Sleep mode, retaining the register and memory contents will shorten the wakeup latency.

Power-Down Mode

The Power-Down mode is derived from the Deep-Sleep mode of the Cortex™-M3 together with the additional control bits LDOOFF and DMOSON. To enter the Power-Down mode, users can configure the registers shown in the preceding Mode-Entering table and execute the WFI or WFE instruction. A RTC wakeup trigger event, a LVD wakeup, a low to high transition on the external WAKEUP pin or an external reset (nRST) signal will force the microcontroller out of the Power-Down mode. In the Power-Down mode, the 1.8 V power supply will be turned off. The remaining active power supplies are the 3.3 V I/O power (V_{DD33}) and the Backup Domain power (V_{BAK}).

After a system reset, the PORSTF bit in the RSTCU GRSR register, the PDF and BAKPORF bits in the BAKSR register should be checked by software to confirm if the device is being resumed from the Power-Down mode by a backup domain power on reset, an unexpected loss of the 1.8 V power or other reset events (nRST, WDT,...). If the device has entered the Power-Down mode under the correct firmware procedure, then the PDF bit will be set. The System information could be saved in the Backup Registers and be retrieved when the 1.8 V power domain is powered on again. More information about the PDF and BAKPORF bits in the BAKSR register and PORSTF bit in the RSTCU GRSR register is shown in the following table.

Table 13. Power Status After System Reset

BAKPORF	PDF	PORSTF	Description
1	0	1	Power-up for the first time after the backup domain is reset: Power on reset when VBAK is applied for the first time or executing a software reset command on the backup domain.
0	0	1	Restart from unexpected loss of the 1.8 V power or other reset (nRST, WDT,...)
0	1	1	Restart from the Power-Down mode
1	1	x	Reserved

Register Map

The following table shows the PWRCU registers and reset values. Note all the registers in this unit are located in the V_{BAK} backup power domain.

Table 14. PWRCU Register Map

Register	Offset	Description	Reset Value
PWRCU Base Address = 0x4006_A000			
BAKSR	0x100	Backup Domain Status Register	0x0000_0001
BAKCR	0x104	Backup Domain Control Register	0x0000_0000
BAKTEST	0x108	Backup Domain Test Register	0x0000_0027
HSIRCR	0x10C	HSI Ready Counter Control Register	0x0000_0003
LVDCSR	0x110	Low Voltage/Brown Out Detect Control and Status Register	0x0000_0000
BAKREG0	0x200	Backup Register 0	0x0000_0000
BAKREG1	0x204	Backup Register 1	0x0000_0000
BAKREG2	0x208	Backup Register 2	0x0000_0000
BAKREG3	0x20C	Backup Register 3	0x0000_0000
BAKREG4	0x210	Backup Register 4	0x0000_0000
BAKREG5	0x214	Backup Register 5	0x0000_0000
BAKREG6	0x218	Backup Register 6	0x0000_0000
BAKREG7	0x21C	Backup Register 7	0x0000_0000
BAKREG8	0x220	Backup Register 8	0x0000_0000
BAKREG9	0x224	Backup Register 9	0x0000_0000

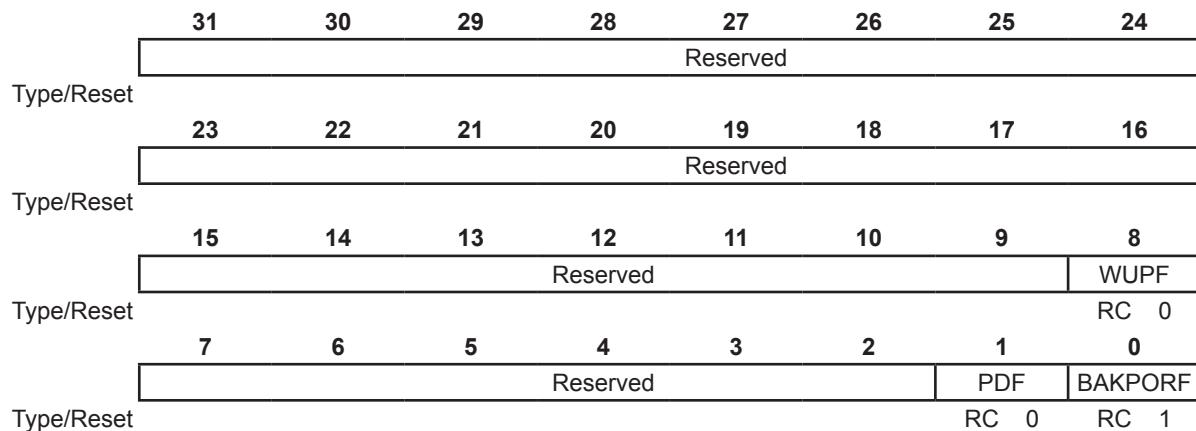
Register Descriptions

Backup Domain Status Register – BAKSR

This register indicates backup domain status.

Offset: 0x100

Reset value: 0x0000_0001 (Reset only by Backup Domain reset)



Bits	Field	Descriptions
[8]	WUPF	<p>External WAKEUP Pin Flag</p> <p>0: The Wakeup pin is not asserted 1: The Wakeup pin is asserted</p> <p>This bit is set by hardware when the WAKEUP pin asserts and is cleared by a software read. Software should read this bit to clear it after a system wake up from the power saving mode.</p>
[1]	PDF	<p>Power Down Flag</p> <p>0: Wakeup from abnormal V_{DD18} shutdown (Loss of V_{DD18} is unexpected) 1: Wakeup from Power-Down mode. The loss of V_{DD18} is under expectation.</p> <p>This bit is set by hardware when the system has successfully entered the Power-Down mode This bit is cleared by a software read.</p>
[0]	BAKPORF	<p>Backup Domain Reset Flag</p> <p>0: Backup Domain reset does not occur 1: Backup Domain reset occurs</p> <p>This bit is set by hardware when Backup Domain reset occurs, either a Backup Domain power on reset or Backup Domain software reset. The bit is cleared by a software read. This bit must be cleared after the system is first powered, otherwise it will be impossible to detect when a Backup Domain reset has been triggered. When this bit is read as 1, a read software loop must be implemented until the bit returns again to 0. This software loop is necessary to confirm that the Backup Domain is ready for access. It must be implemented after the Backup Domain is first powered up.</p>

Backup Domain Control Register – BAKCR

This register provides power control bits for the Deep-Sleep and Power-Down modes.

Offset: 0x104

Reset value: 0x0000_0000 (Reset only by Backup Domain reset)

	31	30	29	28	27	26	25	24
Reserved								
Type/Reset								
Reserved								
Type/Reset	23	22	21	20	19	18	17	16
Reserved								
Type/Reset	15	14	13	12	11	10	9	8
	DMOSSTS	Reserved		V18RDYSC	Reserved		WUPIEN	WUPEN
Type/Reset	RO 0			RW 0			RW 0	RW 0
	7	6	5	4	3	2	1	0
Type/Reset	DMOSON	Reserved			LDOOFF	Reserved		BAKRST
	RW 0				RW 0			WO 0

Bits	Field	Descriptions
[15]	DMOSSTS	Depletion MOS Status This bit is set to 1 if the DMOSON bit in this register has been set to 1. This bit is cleared to 0 if the DMOSON bit has been set to 0 or if a BOD reset occurred.
[12]	V18RDYSC	V_{DD18} Ready Source Selection. Setting this bit to determine what control signal of isolation cells is used to disable the isolation function of the V_{18} to V_{33} power domain level shifter. 0: BKISO bit in the LPCR register located in the CKCU 1: V_{DD18} POR
[9]	WUPIEN	External WAKEUP Pin Interrupt Enable 0: Disable WAKEUP pin interrupt function 1: Enable WAKEUP pin interrupt function The software can set the WUPIEN bit to 1 to assert the LPWUP interrupt in the NVIC unit when both the WUPEN and WUPF bits are set to 1.

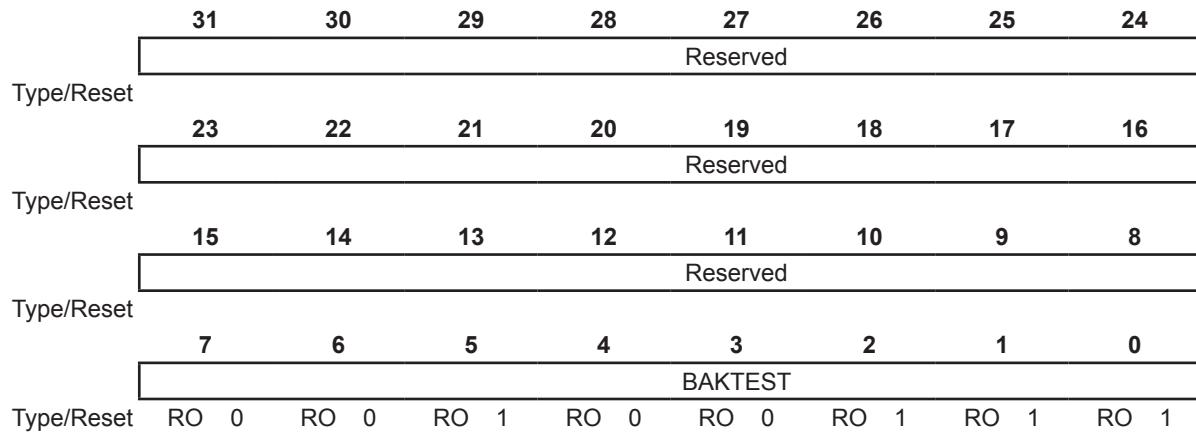
Bits	Field	Descriptions
[8]	WUPEN	<p>External WAKEUP Pin Enable</p> <p>0: Disable WAKEUP pin function. 1: Enable WAKEUP pin function.</p> <p>The Software can set the WUPEN bit as 1 to enable the WAKEUP pin function before entering the power saving mode. When WUPEN = 1, a rising edge on the WAKEUP pin wakes up the system from the power saving mode. As the WAKEUP pin is active high, this bit will set an input pull down mode when the bit is high. The corresponding register bits which should be properly setup are the PCPD [15] to 1 in the PCPDR register, the PCPU [15] to 0 in the PCPUR register and the PCCFG15 field to 0x01 in the GPCCFGHR register.</p> <p>Note: This bit is reset by a system reset or a Backup Domain reset. Because this bit is located in the Backup Domain, after reset activity there will be a delay until the bit is active. The bit will not be active until the system reset finished and the Backup Domain ISO signal has been disabled. This means that the bit can not be immediately set by software after a system reset finished and the Backup domain ISO signal disabled. The delay time needed is a minimum of three 32KHz clock periods until the bit reset activity has finished.</p>
[7]	DMOSON	<p>DMOS Control</p> <p>0: DMOS is OFF 1: DMOS is ON</p> <p>A DMOS is implemented to provide an alternative voltage source for the 1.8 V power domain when the Cortex™-M3 enters the Deep-Sleep mode (SLEEPDEEP=1). The control bit DMOSON is set by software and cleared by software or PORB. If the DMOSON bit is set to 1, the LDO will automatically be turned off when the Cortex™-M3 enters the Deep-Sleep mode.</p>
[3]	LDOOFF	<p>LDO Operating Mode Control</p> <p>0: The LDO operates in a low current mode when Cortex™-M3 enters the Deep-Sleep mode (SLEEPDEEP = 1). The VDD18 power is available. 1: The LDO is turned off when the Cortex™-M3 enters the Deep-Sleep mode (SLEEPDEEP=1). The VDD18 power is not available.</p> <p>Note: This bit is only available when the DMOSON bit is cleared to 0.</p>
[0]	BAKRST	<p>Backup Domain Software Reset</p> <p>0: No action 1: Backup Domain Software Reset is activated - includes all the related RTC and PWRCU registers.</p>

Backup Domain Test Register – BAKTEST

This register specifies a read-only value for the software to recognize whether backup domain is ready for access.

Offset: 0x108

Reset value: 0x0000_0027



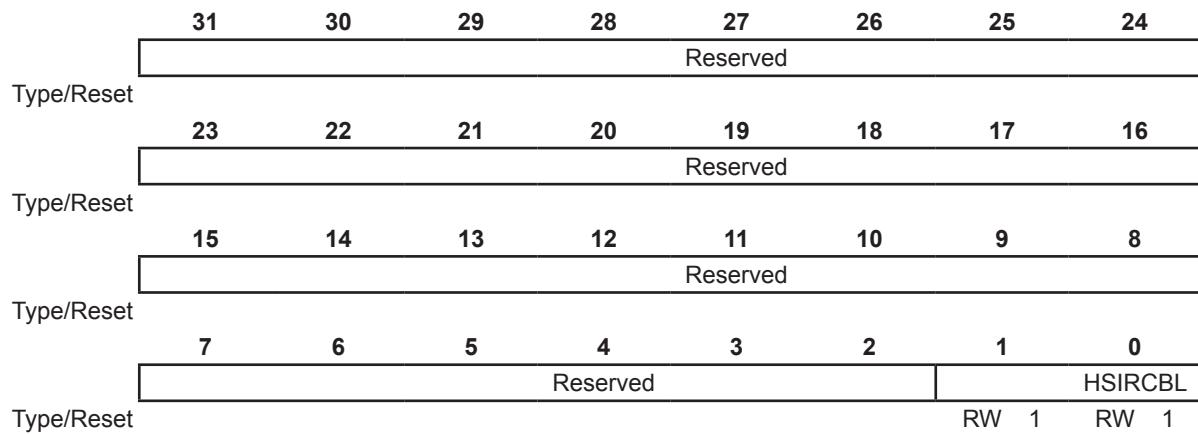
Bits	Field	Descriptions
[7:0]	BAKTEST	Backup Domain Test Bits A constant 0x27 will be read when the Backup Domain is ready for Cortex™-M3 access

HSI Ready Counter Control Register – HSIRCR

This register specifies the counter bit length of the HSI ready counter.

Offset: 0x10C

Reset value: 0x0000_0003 (Reset only by Backup Domain reset)



Bits	Field	Descriptions
[1:0]	HSIRCBL	<p>HSI Ready Counter Bit Length</p> <p>00: 4 bits 01: 5 bits 10: 6 bits 11: 7 bits</p> <p>The HSIRCBL field specifies the bit length of the HSI ready counter. Software can set the HSIRCBL field to shorten the startup waiting time of the HSI oscillator before entering the Deep-Sleep mode or Power-Down mode. (HSICRBL is reset only by Backup Domain reset)</p>

Low Voltage/Brown Out Detect Control and Status Register – LVCSR

This register specifies flags, enable bits, and option bits for Low-Voltage/Brown-out detector.

Offset: 0x110

Reset value: 0x0000_0000 (Reset only by Backup Domain reset)

	31	30	29	28	27	26	25	24	
Reserved									
Type/Reset									
	23	22	21	20	19	18	17	16	
Type/Reset	Reserved	LVDS [2]	LVDEWEN	LVDIWEN	LVDF	LVDS [1:0]		LVDEN	
	RW	0	RW	0	RO	0	RW	0	
	15	14	13	12	11	10	9	8	
Reserved									
Type/Reset									
	7	6	5	4	3	2	1	0	
Type/Reset	Reserved				BODF	Reserved	BODRIS	BODEN	
					RO	0	RW	0	

Bits	Field	Descriptions
[21]	LVDEWEN	<p>LVD Event Wakeup Enable</p> <p>0: LVD event wakeup is disabled 1: LVD event wakeup is enabled</p> <p>Setting this bit to 1 will enable the LVD event wakeup function to wake up the system when a LVD condition occurs which result in the LVDF bit being asserted. If the system requires to be waked up from the Deep-Sleep or Power-Down mode by a LVD condition, this bit must be set to 1.</p>
[20]	LVDIWEN	<p>LVD Interrupt Wakeup Enable</p> <p>0: LVD interrupt wakeup is disabled 1: LVD interrupt wakeup is enabled</p> <p>Setting this bit to 1 will enable the LVD interrupt function. When a LVD condition occurs and the LVDIWEN bit is set to 1, a LVD interrupt will be generated and sent to the Cortex™-M3 NVIC unit.</p>
[19]	LVDF	<p>Low Voltage Detect Status Flag</p> <p>0: V_{DD33} is higher than the specific voltage level 1: V_{DD33} is equal to or lower than the specific voltage level</p> <p>When the LVD condition occurs, the LVDF flag will be asserted. When the LVDF flag is asserted, a LVD interrupt will be generated for Cortex™-M3 if the LVDIWEN bit is set to 1. However, if the LVDEWEN bit is set to 1 and the LVDIWEN bit is cleared to 0, only a LVD event will be generated rather than a LVD interrupt when the LVDF flag is asserted.</p>

Bits	Field	Descriptions
[22], [18:17]	LVDS [2:0]	Low Voltage Detect Level Selection 000: 2.7 V (nominal, default) 001: 2.8 V (nominal) 010: 2.9 V (nominal) 011: 3.0 V (nominal) 100: 3.1 V (nominal) 101: 3.2 V (nominal) 110: 3.4 V (nominal) 111: 3.5 V (nominal)
[16]	LVDEN	Low Voltage Detect Enable 0: Disable Low Voltage Detect 1: Enable Low Voltage Detect Setting this bit to 1 will generate a LVD event when the 3.3V power is lower than the voltage set by LVDS bits. Therefore when the LVD function is enabled before the system is into the Deep-Sleep2 (DMOS is turn on and LDO is power down) or Power-Down mode (DMOS and LDO is power down), the LVDEWEN bit has to be enabled to avoid the LDO does not activate in the meantime when the CPU is woken up by the low voltage detection activity.
[3]	BODF	Brown Out Detection Flag If $V_{DD33} < 2.6$ V, BODF = 1. Otherwise, BODF = 0.
[1]	BODRIS	BOD Reset or Interrupt Selection 0: Reset the whole device 1: Generate Interrupt
[0]	BODEN	Brown Out Detect Enable 0: Disable Brown Out Detect 1: Enable Brown Out Detect

Backup Register n – BAKREGn, n = 0 ~ 9

This register specifies backup register n for storing data during the VDD18 power-off period.

Offset: 0x200 ~ 0x224

Reset value: 0x0000_0000 (Reset only by Backup Domain reset)

	31	30	29	28	27	26	25	24
BAKREGn								
Type/Reset	RW 0							
23 22 21 20 19 18 17 16								
Type/Reset	RW 0							
15 14 13 12 11 10 9 8								
Type/Reset	RW 0							
7 6 5 4 3 2 1 0								
Type/Reset	RW 0							
BAKREGn								

Bits	Field	Descriptions
[31:0]	BAKREGn	Backup Register n (n = 0 ~ 9) These registers are used for data storage in general purpose. The contents of BAKREGn registers will remain even if the V _{DD18} power is lost.

6 Clock Control Unit (CKCU)

Introduction

The Clock Control unit, CKCU, provides a range of frequencies and clock functions. These include a High Speed Internal RC oscillator (HSI), a High Speed External crystal oscillator (HSE), a Low Speed Internal RC oscillator (LSI), a Low Speed External crystal oscillator (LSE), a Phase Lock Loop (PLL), a HSE clock monitor, clock prescalers, clock multiplexers and clock gating circuitry. The clocks of the AHB, APB and Cortex™-M3 are derived from the system clock (CK_SYS) which can source from the HSI, HSE or PLL. The Watchdog Timer and Real Time Clock (RTC) use either the LSI or LSE as their clock source. The maximum operating frequency of the system core clock (CK_AHB) can be up to 72 MHz.

Some of the internal clocks can also be wired out via the CKOUT pin for debugging purposes. The clock monitor circuit can be used to detect an HSE clock failure. Once the HSE clock has ceased to operate, for whatever reason, the CKCU will force the system clock source to switch to the HSI clock to prevent a system halt from occurring.

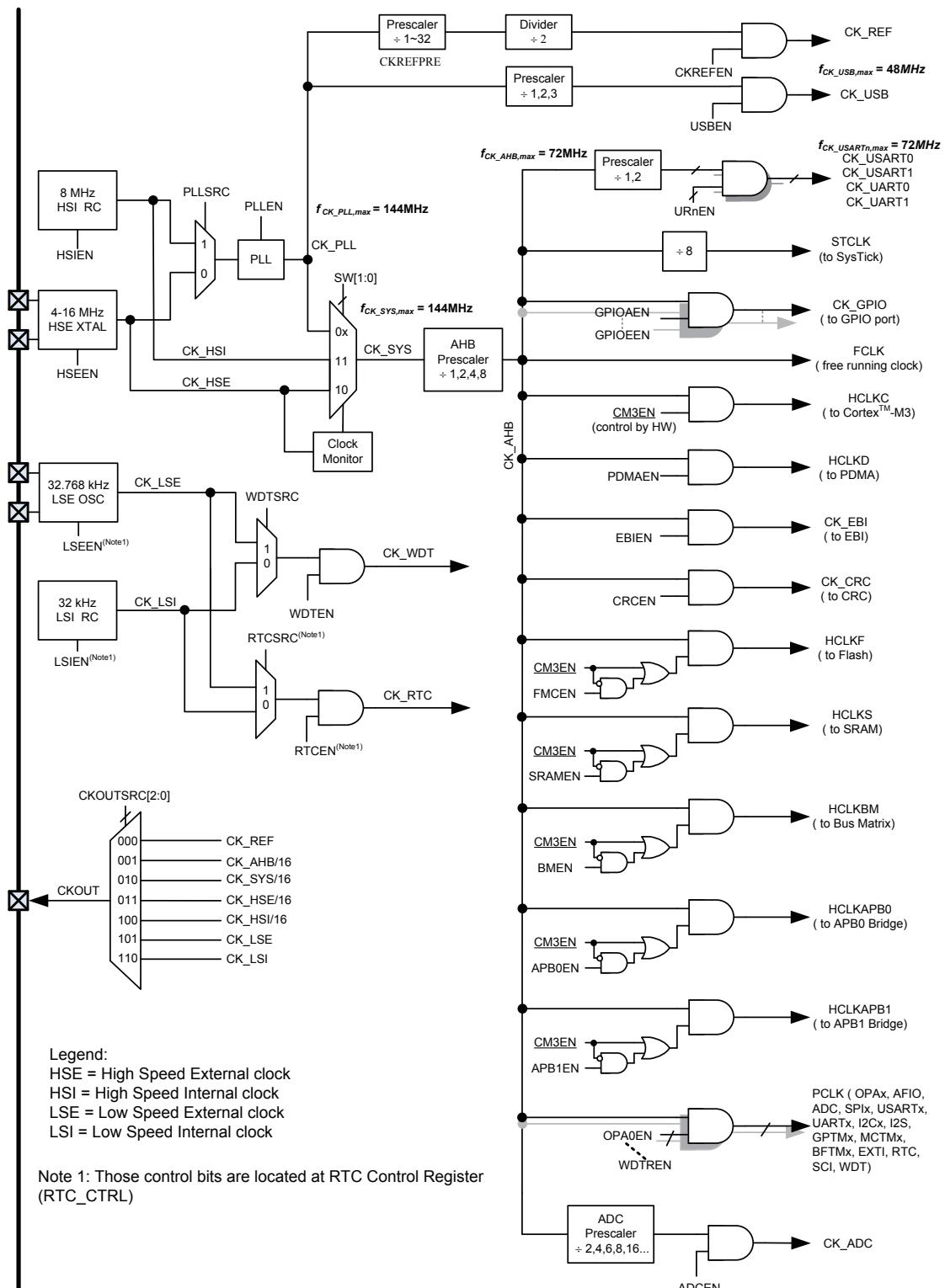


Figure 12. CKCU Block Diagram

Features

- 4 to 16 MHz High Speed External crystal oscillator – HSE
- 8 MHz High Speed Internal RC oscillator – HSI
- 32,768 Hz Low Speed External crystal oscillator – LSE
- 32kHz Low Speed Internal RC oscillator – LSI
- PLL clock source can be HSE or HSI
- HSE clock monitor

Functional Descriptions

High Speed External Crystal Oscillator – HSE

The high speed external crystal oscillator, HSE, which has a frequency from 4 to 16 MHz, produces a highly accurate clock source for use as the system clock. The crystal with a specific frequency must be connected and located close to the two HSE pins, XTALIN / XTALOUT. The external resistor and capacitor components connected to the crystal are necessary for proper oscillation.

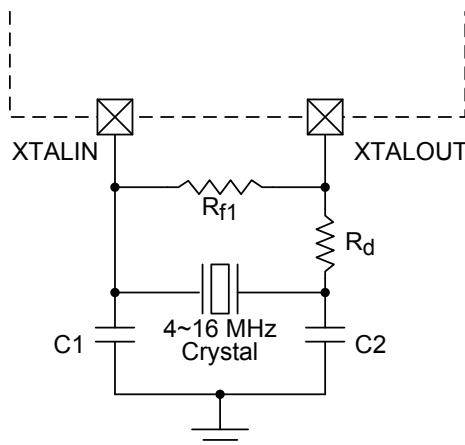


Figure 13. External HSE Crystal, Ceramic, and Resonator

The HSE crystal oscillator can be switched on or off using the HSEEN bit in the Global Clock Control Register GCCR. The HSERDY flag in the Global Clock Status Register GCSR indicates if the high-speed external crystal oscillator is stable. When the HSE is powered up, it will not be released for use until this HSERDY bit is set by the hardware. This specific delay period is known as the oscillator “Start-up time”. As the HSE becomes stable, an interrupt will be generated if the related interrupt enable bit HSERDYIE in the Global Clock Interrupt Register GCIR is set. At this point the HSE clock can be used directly as the system clock source or the PLL input clock.

High Speed Internal RC Oscillator – HSI

The high speed internal RC oscillator, HSI, has a fixed frequency of 8 MHz and is the default clock source selection for the CPU when the device is powered up. The HSI oscillator provides a lower cost type clock source as no external components are required. The HSI RC oscillator can be switched on or off using the HSIEN bit in the Global Clock Control Register GCCR. The HSIRDY flag in the Global Clock Status Register GCSR is used to indicate if the internal RC oscillator is stable. The start-up time of the HSI oscillator is shorter than the HSE crystal oscillator. An interrupt can be generated if the related interrupt enable bit, HSIRDYIE, in the Global Clock Interrupt Register, GCIR, is set when the HSI becomes stable. The HSI clock can also be used as the PLL input clock.

The frequency accuracy of the HSI can be calibrated by the manufacturer, but its operating frequency is still less accurate than HSE. The applications requirements, environment and cost will determine which oscillator type is selected.

If the HSE or PLL is the system clock source, to minimize the time required for the system to recover from the Deep-Sleep Mode, the software can set the PSRCEN bit (Power Saving Wakeup RC Clock Enable) to 1 to force the HSI clock to be system clock when the system initially wake-up. Subsequently, the system clock will automatically be switched back to the original clock source, HSE or PLL, when the original clock source ready flag is asserted. This function will reduce the wakeup time when using the HSE or PLL as the system clock.

Phase Locked Loop – PLL

The internal Phase Locked Loop, PLL, can provide 8 ~ 144 MHz clock output which is 2 ~ 36 multiples of a fundamental reference frequency of 4 ~ 16 MHz. The PLL includes a reference divider, feedback dividers, a digital phase frequency detector (PD), a current-controlled charge pump (CP), an internal loop filter and a voltage-controlled oscillator (VCO) to achieve a stable phase-locked state.

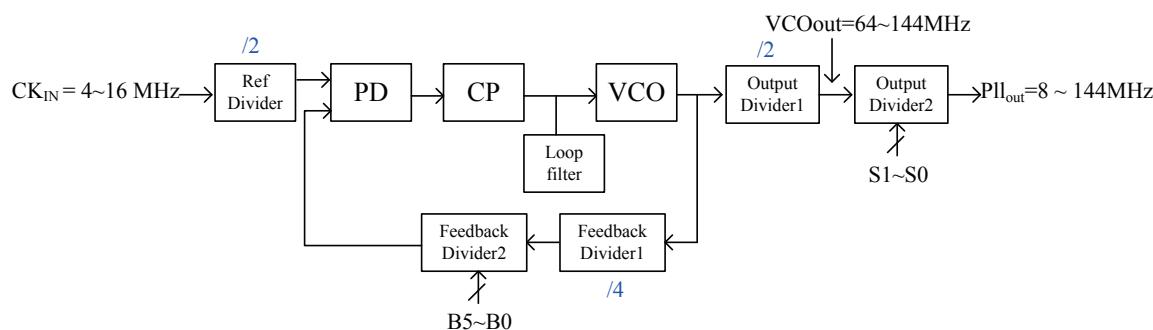


Figure 14. PLL Block Diagram

The PLL output clock frequency can be determined by the following formula:

$$PLL_{OUT} = CK_{IN} * \frac{NF1 * NF2}{NR * NO1 * NO2} = CK_{IN} * \frac{4 * NF2}{2 * 2 * NO2} = CK_{IN} * \frac{NF2}{NO2}$$

where NR = Ref divider = 2, NF1 = Feedback divider1 = 4, NF2 = Feedback divider2 = 1 ~ 64,

NO1 = Output divider1 = 2,

NO2 = Output divider2 = 1, 2, 4, or 8

Consider a duty cycle of 50% and where both input and output frequencies are divided by 2. If a given clock PLL input clock source frequency, CK_{IN} , generates a specific PLL output frequency, then it is recommended to use a higher value for NF2 in order to increase PLL stability and reduce jitter at the expense of settling time. The setup bits of the output and feedback divider2 are described in the following two tables. All the setup bits named S1~S0 and B5~B0 in the tables are defined in the PLL Configuration Register PLLCFGR and the PLL Control Register PLLCR in the Register Definition section. Note that the VCO_{OUT} frequency must have a range from 64 MHz to 144 MHz. If the selected configuration exceeds this range, the PLL output frequency cannot be guaranteed to match the above PLL_{OUT} formula.

The PLL can be switched on or off by using the PLLLEN bit in the Global Clock Control Register GCCR. The PLLRDY flag in the Global Clock Status Register GCSR will indicate if the PLL clock is stable. An interrupt can be generated if the related interrupt enable bit, PLLRDYIE, in the Global Clock Interrupt Register, GCIR, is set as the PLL becomes stable.

Table 15. Output Divider2 Setting

Output divider 2 setup bits S1~S0 (POTD bits in the PLLCFGR register)	NO2 (Output divider2 value)
00	1
01	2
10	4
11	8

Table 16. Feedback Divider2 value Setting

Feedback divider 2 setup bits B5~B0 (PFBD bits in the PLLCFGR register)	NF2 (Feedback divider2 value)
000000	64
000001	1
000010	2
000011	3
000100	4
000101	5
000110	6
000111	7
001000	8
001001	9
001010	10
001011	11
001100	12
001101	13
001110	14
⋮	⋮
111111	63

Low Speed External Crystal Oscillator – LSE

The low speed external crystal or ceramic resonator oscillator, which has a frequency of 32,768 Hz, produces a low power but highly accurate clock source for the Real-Time-Clock circuit and the Watchdog Timer. The crystal or ceramic resonator must be located close to the two LSE pins, XTAL32KIN and XTAL32KOUT. Their external resistors and capacitors are necessary for proper oscillation. The LSE oscillator can be switched on or off using the LSEEN bit in the RTC Control Register RTCCR. The LSERDY flag in the Global Clock Status Register GCSR will indicate if the LSE clock is stable. An interrupt can be generated if the related interrupt enable bit LSERDYIE, in the Global Clock Interrupt Register GCIR is set when the LSE becomes stable.

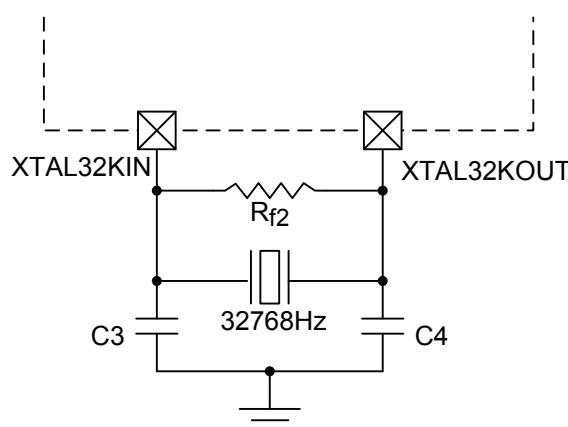


Figure 15. External Crystal, Ceramic, and Resonator for LSE

Low Speed Internal RC Oscillator – LSI

The low speed internal RC oscillator has a frequency of about 32kHz and is a low power clock source for the Real Time Clock circuit or the Watchdog Timer. The LSI offers a low cost clock source as no external components are required. The LSI RC oscillator can be switched on or off by using the LSIEN bit in the RTC Control Register, RTCCR. The frequency accuracy can be calibrated using the configuration options. The LSIRDY flag in the Global Clock Status Register GCSR will indicate if the LSI clock is stable. An interrupt can be generated if the related interrupt enable bit LSIRDYIE in the Global Clock Interrupt Register GCIR is set when the LSI becomes stable.

Clock Ready Flag

The CKCU provides the corresponding clock ready flags of the HSI, HSE, PLL, LSI, and LSE to indicate if these clocks are stable. Before users select the clock as the system clock source or other purpose, it is necessary to confirm the specific clock ready flag is set. Software can check the specific clock is ready or not by polling the individual clock ready status bit in the GCSR register. Additionally, the CKCU can trigger an interrupt to notify the specific clock is ready if the corresponding interrupt enable bit in the GCIR register is set. Software should clear the interrupt status bit in the GCIR register in the interrupt service routine.

System Clock Selection – CK_SYS

After the system reset, the default CK_SYS source will be HSI and can be switched to HSE or PLL by changing the System Clock Switch bits, SW, in the Global Clock Control Register, GCCR. When the SW value is changed, the CK_SYS will continue to operate using the original clock source until the target clock source is stable. The corresponding clock ready status is in the Global Clock Status Register, GCSR, and the clock source usage can be found in the Clock Source Status Register, CKST. When a clock source is used directly by the CK_SYS or the PLL, it is not possible to stop it.

HSE Clock Monitor

The HSE clock monitor function is enabled by the HSE Clock Monitor Enable bit, CKMEN, in the Global Clock Control Register, GCCR. This function should be enabled after the HSE start-up delay and disabled when the HSE is stopped. Once the HSE failure is detected, the HSE will be automatically disabled. The HSE Clock Stuck Flag, CKSF, in the Global Clock Interrupt Register, GCIR, will be set and the HSE failure event will be generated if the Clock Stuck Interrupt Enable bit, CKSIE, in the GCIR register is set. This failure interrupt is connected to the Non-Maskable Interrupt, NMI, of the Cortex-M3. If the HSE is selected as the clock source of CK_SYS or PLL, the HSE failure will force the CK_SYS source to HSI and the PLL will be disabled automatically.

Clock Output Capability

The clock output capability of HT32 series MCU is ranging from 32kHz to 9 MHz. There are several clock signals can be selected via the CKOUT Clock Source Selection bits, CKOUTSRC, in the Global Clock Configuration Register, GCFGR. The corresponding GPIO pin should be configured in the properly Alternate Function I/O (AFIO) mode to output the selected clock signal.

Table 17. CKOUT Clock Source

CKOUTSRC	Clock Source
000	CK_REF
001	CK_AHB / 16
010	CK_SYS / 16
011	CK_HSE / 16
100	CK_HSI / 16
101	CK_LSE
110	CK_LSI
111	Reserved

Register Map

The following table shows the CKCU registers and their reset value.

Table 18. CKCU Register Map

Register	Offset	Description	Reset Value
CKCU Base Address = 0x4008_8000			
GCFGR	0x000	Global Clock Configuration Register	0x0000_0102
GCCR	0x004	Global Clock Control Register	0x0000_0803
GCSR	0x008	Global Clock Status Register	0x0000_0028
GCIR	0x00C	Global Clock Interrupt Register	0x0000_0000
PLLCFGR	0x018	PLL Configuration Register	0x0000_0000
PLLCR	0x01C	PLL Control Register	0x0000_0000
AHBCFGR	0x020	AHB Configuration Register	0x0000_0000
AHBCCR	0x024	AHB Clock Control Register	0x0000_00E5
APBCFGR	0x028	APB Configuration Register	0x0001_0000
APBCCR0	0x02C	APB Clock Control Register 0	0x0000_0000
APBCCR1	0x030	APB Clock Control Register 1	0x0000_0000
CKST	0x034	Clock Source Status Register	0xC100_0000
LPCR	0x300	Low Power Control Register	0x0000_0000
MCUDBGCR	0x304	MCU Debug Control Register	0x0000_0000

Register Descriptions

Global Clock Configuration Register – GCFGR

This register specifies the clock source for the CSIF/USB/PLL/USART/Watchdog Timer/CKOUT circuit.

Offset: 0x000

Reset value: 0x0000_0102

	31	30	29	28	27	26	25	24
	LPMOD			Reserved				
Type/Reset	RO 0	RO 0	RO 0					
	23	22	21	20	19	18	17	16
	USBPRE		URPRE			Reserved		
Type/Reset	RW 0	RW 0	RW 0	RW 0				
	15	14	13	12	11	10	9	8
	CKREFPRE					Reserved	PLLSRC	
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0		RW 1	
	7	6	5	4	3	2	1	0
	Reserved					CKOUTSRC	RW 1	RW 0
Type/Reset						RW 0	RW 1	RW 0

Bits	Field	Descriptions
[31:29]	LPMOD	<p>Lower Power Mode Status</p> <p>000: Device in initial status 001: Device has been waken up from Sleep mode 010: Device has been waken up from Deep Sleep mode1 011: Device has been waken up from Deep Sleep mode2 100: Device has been waken up from Power Down mode Others: Reserved</p> <p>This field is set and reset by hardware.</p>
[23:22]	USBPRE	<p>USB Clock Prescaler Selection</p> <p>00: CK_USB = CK_PLL 01: CK_USB = CK_PLL / 2 10: CK_USB = CK_PLL / 3 11: Reserved</p> <p>This field is set and reset by software to control the USB clock prescaler division.</p>
[21:20]	URPRE	<p>USART Clock Prescaler Selection</p> <p>00:CK_USART = CK_AHB 01: CK_USART = CK_AHB / 2 Others: Reserved</p> <p>This field is set and reset by software to control the USART clock prescaler value.</p>

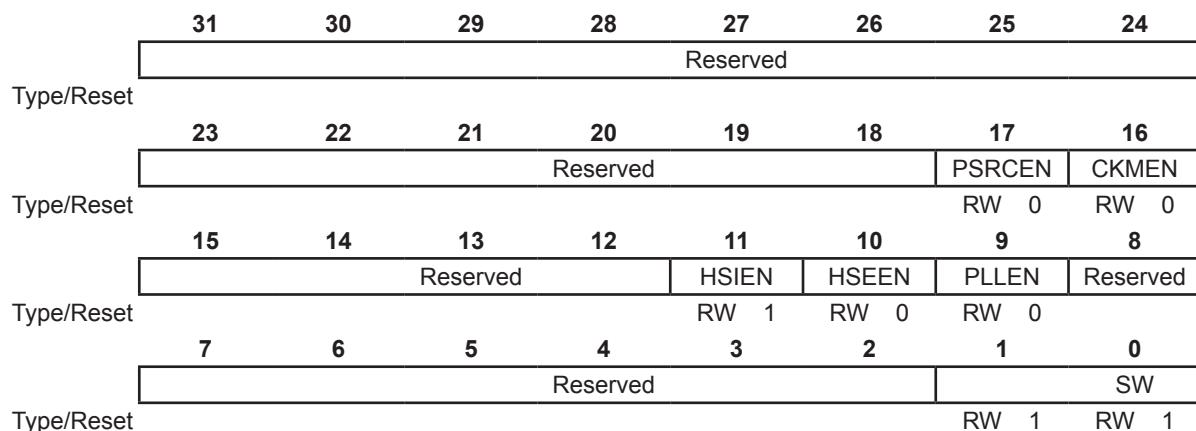
Bits	Field	Descriptions
[15:11]	CKREFPRE	CK_REF Clock Prescaler Selection CK_REF = CK_PLL / (CKREFPRE + 1) / 2 00000:CK_REF = CK_PLL / 2 00001:CK_REF = CK_PLL / 4 ... 11111:CK_REF = CK_PLL / 64 This field is set and reset by software to control CK_REF clock prescaler division.
[8]	PLLSRC	PLL Clock Source Selection 0: External 4 ~ 16 MHz crystal oscillator clock is selected (HSE) 1: Internal 8 MHz RC oscillator clock is selected (HSI) This bit is set and reset by software to control the PLL clock source.
[2:0]	CKOUTSRC	CKOUT Clock Source Selection 000: CK_REF selected 001: (CK_AHB / 16) selected 010: (CK_SYS / 16) selected 011: (CK_HSE / 16) selected 100: (CK_HSI / 16) selected 101: CK_LSE selected 110: CK_LSI selected 111: Reserved This field is set and reset by software to control CKOUT clock source.

Global Clock Control Register – GCCR

This register specifies the clock enable bits.

Offset: 0x004

Reset value: 0x0000_0803



Bits	Field	Descriptions
[17]	PSRCEN	<p>Power Saving Wakeup RC Clock Enable</p> <p>0: No action</p> <p>1: Use HSI as the temporary CK_SYS source after waking up from Deep-Sleep1 or Deep-Sleep2.</p> <p>When the PSRCEN bit is set to 1, the HSI will be used as the clock source of the CK_SYS after waking up from the Deep-Sleep1 or Deep-Sleep2 mode. This means that the instruction can be executed early before the original CK_SYS source such as HSE or PLL is stable.</p>
[16]	CKMEN	<p>HSE Clock Monitor Enable</p> <p>0: Disable the External 4 ~ 16 MHz crystal oscillator (HSE) clock monitor</p> <p>1: Enable the External 4 ~ 16 MHz crystal oscillator (HSE) clock monitor</p> <p>When the hardware detects that the HSE clock is stuck at a low or high state, the internal hardware will switch the system clock to be the internal high speed HSI RC clock. The way to recover the original system clock is by either an external reset, power on reset or clearing CKSF by software.</p> <p>NOTE: When the HSE clock monitor is enabled, the hardware will automatically enable the HSI internal RC oscillator regardless of the control bit, HSIEN, state.</p>

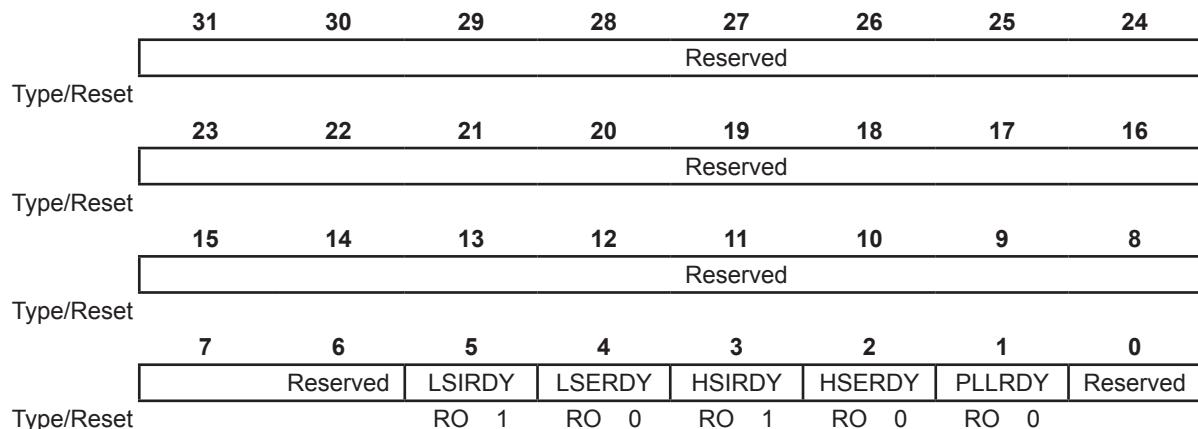
Bits	Field	Descriptions
[11]	HSIEN	Internal High Speed oscillator Enable 0: Internal 8 MHz RC oscillator disabled 1: Internal 8 MHz RC oscillator enabled Set and reset by software. This bit cannot be reset if the HSI clock is used as the system clock.
[10]	HSEEN	External High Speed oscillator Enable 0: External 4 ~ 16 MHz crystal oscillator disabled 1: External 4 ~ 16 MHz crystal oscillator enabled Set and reset by software. This bit cannot be reset if the HSE clock is used as the system clock or the PLL input clock.
[9]	PLLEN	PLL Enable 0: PLL is switched off 1: PLL is switched on Set and reset by software. This bit cannot be reset if the PLL clock is used as the system clock.
[1:0]	SW	System Clock Switch 0X: Select CK_PLL as the CK_SYS source 10: Select CK_HSE as the CK_SYS source 11: Select CK_HSI as the CK_SYS source Set by software to select the CK_SYS source. Because the change of CK_SYS has inherent latency, software should read these bits to confirm whether the switching is complete or not. The switch will be forced to HSI by HSE clock monitor when the HSE failure is detected and the HSE is selected as the clock source of CK_SYS or PLL.

Global Clock Status Register – GCSR

This register indicates the clock ready status.

Offset: 0x008

Reset value: 0x0000_0028



Bits	Field	Descriptions
[5]	LSIRDY	LSI Internal Low Speed Oscillator Ready Flag. 0: LSI oscillator not ready 1: LSI oscillator ready This bit is set by hardware to indicate if the LSI oscillator is stable and ready for use
[4]	LSERDY	LSE External Low Speed Oscillator Ready Flag. 0: LSE oscillator not ready 1: LSE oscillator ready This bit is set by hardware to indicate if the LSE oscillator is stable and ready for use.
[3]	HSIRDY	HSI High Speed Internal Oscillator Ready Flag 0: HSI oscillator not ready 1: HSI oscillator ready This bit is set by hardware to indicate if the HSI oscillator is stable and ready for use.
[2]	HSERDY	HSE High Speed External Clock Ready Flag 0: HSE oscillator not ready 1: HSE oscillator ready This bit is set by hardware to indicate if the HSE oscillator is stable and ready for use.
[1]	PLL RDY	PLL Clock Ready Flag 0: PLL not ready 1: PLL ready This bit is set by hardware to indicate if the PLL output clock is stable and ready for use.

Global Clock Interrupt Register – GCIR

This register specifies the interrupt enable and flag bits.

Offset: 0x00C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24	
Reserved									
Type/Reset									
	23	22	21	20	19	18	17	16	
Reserved LSIRDYIE LSERDYIE HSIRDYIE HSERDYIE PLLRDYIE Reserved CKSIE									
Type/Reset	RW	0	RW	0	RW	0	RW	0	
	15	14	13	12	11	10	9	8	
Reserved									
Type/Reset		7	6	5	4	3	2	1	
	Reserved	LSIRDYF	LSERDYF	HSIRDYF	HSERDYF	PLLRDYF	Reserved	CKSF	
Type/Reset		WC	0	WC	0	WC	0	WC	0

Bits	Field	Descriptions
[22]	LSIRDYIE	LSI Ready Interrupt Enable 0: Disable the LSI stabilization interrupt 1: Enable the LSI stabilization interrupt This bit is used to control whether the LSI stabilization interrupt is enabled or disabled.
[21]	LSERDYIE	LSE Ready Interrupt Enable 0: Disable the LSE stabilization interrupt 1: Enable the LSE stabilization interrupt This bit is used to control whether the LSE stabilization interrupt is enabled or disabled.
[20]	HSIRDYIE	HSI Ready Interrupt Enable 0: Disable the HSI stabilization interrupt 1: Enable the HSI stabilization interrupt This bit is set and reset by software used to enable or disable the HSI stabilization interrupt.
[19]	HSERDYIE	HSE Ready Interrupt Enable 0: Disable the HSE stabilization interrupt 1: Enable the HSE stabilization interrupt This bit is set and reset by software used to enable or disable the HSE stabilization interrupt.
[18]	PLLRDYIE	PLL Ready Interrupt Enable 0: Disable the PLL stabilization interrupt 1: Enable the PLL stabilization interrupt This bit is set and reset by software used to enable or disable the PLL stabilization interrupt.
[16]	CKSIE	Clock Stuck Interrupt Enable 0: Disable the clock fail interrupt 1: Enable the clock fail interrupt This bit is set and reset by software used to enable or disable the clock monitor interrupt.

Bits	Field	Descriptions
[6]	LSIRDYF	LSI Ready Interrupt Flag 0: No LSI stabilization clock ready interrupt generated 1: LSI stabilization interrupt generated This bit is cleared by software writing a data “1” into it and set by hardware when the Internal 32kHz RC oscillator clock is stable and the LSIRDYIE bit is set.
[5]	LSERDYF	LSE Ready Interrupt Flag 0: No LSE stabilization interrupt generated 1: LSE stabilization interrupt generated This bit is cleared by software writing a data “1” into it and set by hardware when the External 32,768 Hz crystal oscillator clock is stable and the LSERDYIE bit is set.
[4]	HSIRDYF	HSI Ready Interrupt Flag 0: No HSI stabilization interrupt generated 1: HSI stabilization interrupt generated This bit is cleared by software writing a data “1” into it and set by hardware when the internal 8MHz RC oscillator clock is stable and the HSIRDYIE bit is set.
[3]	HSERDYF	HSE Ready Interrupt Flag 0: No HSE stabilization interrupt generated 1: HSE stabilization interrupt generated This bit is cleared by software writing a data “1” into it and set by hardware when the External 4~16 MHz crystal oscillator clock is stable and the HSERDYIE bit is set.
[2]	PLLRDYF	PLL Ready Interrupt Flag 0: No PLL stabilization interrupt generated 1: PLL stabilization interrupt generated This bit is cleared by software writing a data “1” into it and set by hardware when the PLL is stable and the PLLRDYIE bit is set.
[0]	CKSF	HSE Clock Stuck Interrupt Flag 0: Clock operating normally 1: HSE clock stuck This bit is cleared by software writing a data “1” into it and set by hardware when the HSE clock is stuck and the CKSIE bit is set.

PLL Configuration Register – PLLCFGR

This register specifies the PLL configuration.

Offset: 0x018

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Type/Reset	Reserved			PFBD [5:1]				
				RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
Type/Reset	PFBD[0]	POTD			Reserved			
	RW 0	RW 0	RW 0					
	15	14	13	12	11	10	9	8
Type/Reset	Reserved							
	7	6	5	4	3	2	1	0
Type/Reset	Reserved							

Bits	Field	Descriptions
[28:23]	PFBD	PLL VCO Output Clock Feedback Divider (B5 ~ B0 in Figure 14) Feedback Divider divides the output clock from the PLL VCO.
[22:21]	POTD	PLL Output Clock Divider (S1 ~ S0 in Figure 14)

PLL Control Register – PLLCR

This register specifies the PLL Bypass mode.

Offset: 0x01C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Type/Reset	PLLbps				Reserved			
	RW	0						
	23	22	21	20	19	18	17	16
Type/Reset					Reserved			
	15	14	13	12	11	10	9	8
Type/Reset					Reserved			
	7	6	5	4	3	2	1	0
Type/Reset					Reserved			

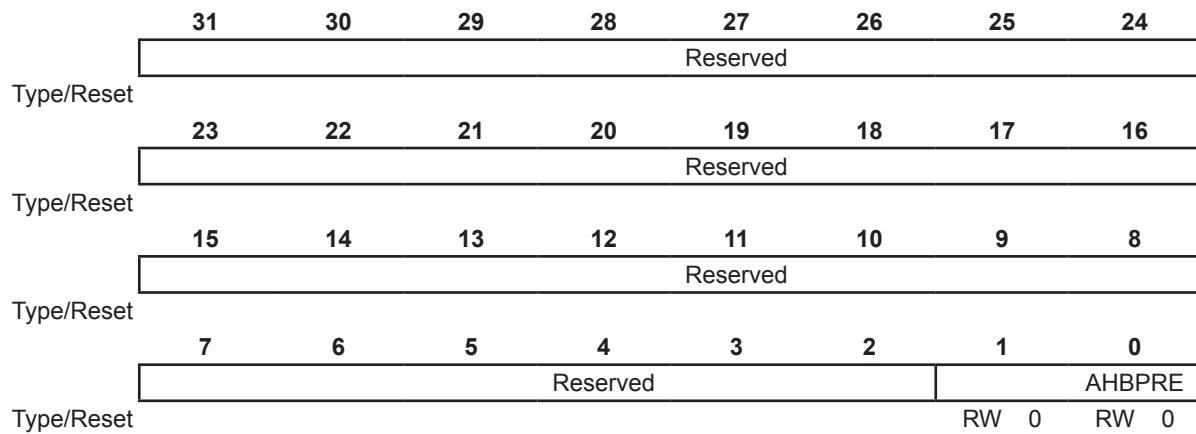
Bits	Field	Descriptions
[31]	PLLbps	PLL Bypass Mode Enable 0: Disable the PLL Bypass mode 1: Enable the PLL Bypass mode in which the PLL output clock PLLOUT is equal to the CK _{IN} clock (refer to the PLL Block diagram)

AHB Configuration Register – AHBCFGR

This register specifies the system clock frequency.

Offset: 0x020

Reset value: 0x0000_0000



Bits	Field	Descriptions
[1:0]	AHBPREG	AHB Pre-Scaler 00: CK_AHB = CK_SYS 01: CK_AHB = CK_SYS / 2 10: CK_AHB = CK_SYS / 4 11: CK_AHB = CK_SYS / 8 This field is set and reset by software to control the AHB clock division ratio.

AHB Clock Control Register – AHBCCR

This register specifies the AHB clock enable bits.

Offset: 0x024

Reset value: 0x0000_00E5

	31	30	29	28	27	26	25	24
Reserved								
Type/Reset	23	22	21	20	19	18	17	16
	Reserved		PEEN	PDEN	PCEN	PBEN	PAEN	
Type/Reset	15	14	13	12	11	10	9	8
	Reserved	CRCEN	EBIEN	CKREFEN	USBEN	Reserved		
Type/Reset	7	6	5	4	3	2	1	0
	APB1EN	APB0EN	BMEN	PDMAEN	Reserved	SRAMEN	Reserved	FMCEN
Type/Reset	RW 1	RW 1	RW 1	RW 0		RW 1		RW 1

Bits	Field	Descriptions
[20]	PEEN	GPIO Port E Clock Enable 0: Port E clock disabled 1: Port E clock enabled This bit is set and reset by software.
[19]	PDEN	GPIO Port D Clock Enable 0: Port D clock disabled 1: Port D clock enabled This bit is set and reset by software.
[18]	PCEN	GPIO Port C Clock Enable 0: Port C clock disabled 1: Port C clock enabled This bit is set and reset by software.
[17]	PBEN	GPIO Port B Clock Enable 0: Port B clock disabled 1: Port B clock enabled This bit is set and reset by software.
[16]	PAEN	GPIO Port A Clock Enable 0: Port A clock disabled 1: Port A clock enabled This bit is set and reset by software.
[13]	CRCEN	CRC Clock Enable 0: CRC clock disable 1: CRC clock enable This bit is set and reset by software.
[12]	EBIEN	EBI Clock Enable 0: EBI clock disable 1: EBI clock enable This bit is set and reset by software.

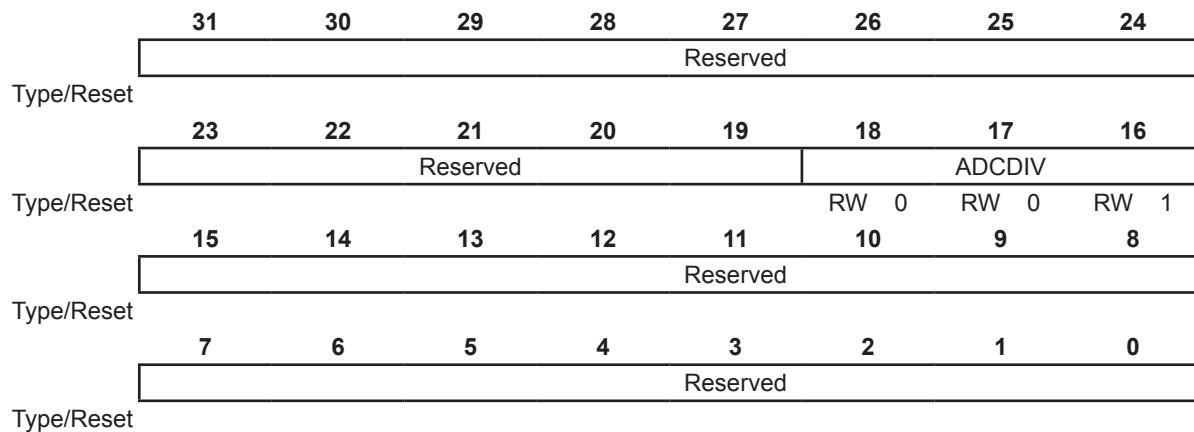
Bits	Field	Descriptions
[11]	CKREFEN	CK_REF Clock Enable 0: CK_REF clock is disabled 1: CK_REF clock is enabled This bit is set and reset by software.
[10]	USBEN	USB Clock Enable 0: USB clock disabled 1: USB clock enabled This bit is set and reset by software.
[7]	APB1EN	APB1 bridge Clock Enable 0: APB1 bridge clock disabled in Sleep mode 1: APB1 bridge clock enabled in Sleep mode This bit is set and reset by software. Note that this bit is only available in the Sleep mode. If the APB1 bridge is not used in the Sleep mode, users can clear the APB1EN bit to 0 to reduce the power consumption before the device enters the Sleep mode.
[6]	APB0EN	APB0 bridge Clock Enable 0: APB0 bridge clock disabled in Sleep mode 1: APB0 bridge clock enabled in Sleep mode This bit is set and reset by software. Note that this bit is only available in the Sleep mode. If the APB0 bridge is not used in the Sleep mode, users can clear the APB0EN bit to 0 to reduce the power consumption before the device enters the Sleep mode.
[5]	BMEN	Bus Matrix Clock Enable 0: Bus Matrix clock disabled in Sleep mode 1: Bus Matrix clock enabled in Sleep mode This bit is set and reset by software. Note that this bit is only available in the Sleep mode. If the Bus Matrix bridge is not used in the Sleep mode, users can clear the BMEN bit to 0 to reduce the power consumption before the device enters the Sleep mode.
[4]	PDMAEN	Peripheral DMA Clock Enable 0: PDMA clock disabled 1: PDMA clock enabled This bit is set and reset by software. The PDMA can operate when the processor is in the Sleep mode. However, the relevant clocks of the AHB bus slave, such as SRAM or Flash, or the APB peripherals, such as I ² C or SPI, which communicate with the PDMA in the Sleep mode have to be enabled before entering the Sleep mode.
[2]	SRAMEN	SRAM Clock Enable 0: SRAM clock disabled in Sleep mode 1: SRAM clock enabled in Sleep mode This bit is set and reset by software. Note that this bit is only available in the Sleep mode. If the SRAM is not used in the Sleep mode, users can clear the SRAMEN bit to 0 to reduce the power consumption before the device enters the Sleep mode.
[0]	FMCEN	Flash Memory Controller Clock Enable 0: FMCEN clock disabled in Sleep mode 1: FMCEN clock enabled in Sleep mode This bit is set and reset by software. Note that this bit is only available in the Sleep mode. If the Flash Memory is not used in the Sleep mode, users can clear the FMCEN bit to 0 to reduce the power consumption before the device enters the Sleep mode.

APB Configuration Register – APBCFGR

This register specifies the frequency of the A/D Converter clock.

Offset: 0x028

Reset value: 0x0001_0000



Bits	Field	Descriptions
[18:16]	ADCDIV	<p>A/D Converter Clock Frequency Division Selection</p> <p>000: Reserved 001: CK_ADC = (CK_AHB / 2) 010: CK_ADC = (CK_AHB / 4) 011: CK_ADC = (CK_AHB / 8) 100: CK_ADC = (CK_AHB / 16) 101: CK_ADC = (CK_AHB / 32) 110: CK_ADC = (CK_AHB / 64) 111: CK_ADC = (CK_AHB / 6)</p> <p>This field is set and reset by software to select the A/D Converter clock division ratio.</p>

APB Clock Control Register 0 – APBCCR0

This register specifies several APB peripheral clock enable bits.

Offset: 0x02C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Type/Reset				Reserved				
						I2SEN	SCIEN	
	23	22	21	20	19	18	17	16
Type/Reset				Reserved				
Type/Reset	15	14	13	12	11	10	9	8
	EXTIEN	AFIOEN		Reserved	UR1EN	UR0EN	USR1EN	USR0EN
Type/Reset	RW 0	RW 0			RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
Type/Reset			Reserved	SPI1EN	SPI0EN		Reserved	I2C1EN
				RW 0	RW 0			RW 0
								RW 0

Bits	Field	Descriptions
[25]	I2SEN	I ² S Interface Enable 0: I ² S clock is disabled 1: I ² S clock is enabled This bit is set and reset by software.
[24]	SCIEN	Smart Card Interface Clock Enable 0: Smart Card clock disabled 1: Smart Card clock enabled This bit is set and reset by software.
[15]	EXTIEN	External Interrupt Clock Enable 0: EXTI clock disabled 1: EXTI clock enabled This bit is set and reset by software.
[14]	AFIOEN	Alternate Function I/O Clock Enable 0: AFIO clock disabled 1: AFIO clock enabled This bit is set and reset by software.
[11]	UR1EN	UART1 Clock Enable 0: UART1 clock disabled 1: UART1 clock enabled This bit is set and reset by software.
[10]	UR0EN	UART0 Clock Enable 0: UART0 clock disabled 1: UART0 clock enabled This bit is set and reset by software.

Bits	Field	Descriptions
[9]	USR1EN	USART1 Clock Enable 0: USART1 clock disabled 1: USART1 clock enabled This bit is set and reset by software.
[8]	USR0EN	USART0 Clock Enable 0: USART0 clock disabled 1: USART0 clock enabled This bit is set and reset by software.
[5]	SPI1EN	SPI1 Clock Enable 0: SPI1 clock disabled 1: SPI1 clock enabled This bit is set and reset by software.
[4]	SPI0EN	SPI0 Clock Enable 0: SPI0 clock disabled 1: SPI0 clock enabled This bit is set and reset by software.
[1]	I2C1EN	I ² C1 Clock Enable 0: I ² C1 clock disabled 1: I ² C1 clock enabled This bit is set and reset by software.
[0]	I2C0EN	I ² C0 Clock Enable 0: I ² C0 clock disabled 1: I ² C0 clock enabled This bit is set and reset by software.

APB Clock Control Register 1 – APBCCR1

This register specifies several APB peripheral clock enable bits.

Offset: 0x030

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Type/Reset	Reserved							
	RW 0							
	23	22	21	20	19	18	17	16
Type/Reset	OPA1EN	OPA0EN		Reserved			BFTM1EN	BFTM0EN
	RW 0	RW 0		RW 0			RW 0	RW 0
	15	14	13	12	11	10	9	8
Type/Reset	Reserved						GPTM1EN	GPTM0EN
	RW 0						RW 0	RW 0
	7	6	5	4	3	2	1	0
Type/Reset	Reserved	BKPREN	Reserved	WDTREN		Reserved	MCTM1EN	MCTM0EN
	RW 0		RW 0			RW 0		RW 0

Bits	Field	Descriptions
[24]	ADCEN	ADC Clock Enable 0: ADC clock disabled 1: ADC clock enabled This bit is set and reset by software.
[23]	OPA1EN	OPA/CMP 1 Clock Enable 0: OPA/CMP 1 clock disabled 1: OPA/CMP 1 clock enabled This bit is set and reset by software.
[22]	OPA0EN	OPA/CMP 0 Clock Enable 0: OPA /CMP 0 clock disabled 1: OPA /CMP 0 clock enabled This bit is set and reset by software.
[17]	BFTM1EN	BFTM1 Clock Enable 0: BFTM1 clock disabled 1: BFTM1 clock enabled This bit is set and reset by software.
[16]	BFTM0EN	BFTM0 Clock Enable 0: BFTM0 clock disabled 1: BFTM0 clock enabled This bit is set and reset by software.
[9]	GPTM1EN	GPTM1 Clock Enable 0: GPTM1 clock disabled 1: GPTM1 clock enabled This bit is set and reset by software.

Bits	Field	Descriptions
[8]	GPTM0EN	GPTM0 Clock Enable 0: GPTM0 clock disabled 1: GPTM0 clock enabled This bit is set and reset by software.
[6]	BKPREN	Backup Domain Registers Access Enable 0: Backup domain registers access disabled 1: Backup domain registers access enabled This bit is set and reset by software.
[4]	WDTREN	Watchdog Timer Registers Access Enable 0: Watchdog Timer registers access disabled 1: Watchdog Timer registers access enabled This bit is set and reset by software.
[1]	MCTM1EN	MCTM1 Clock Enable 0: MCTM1 clock disabled 1: MCTM1 clock enabled This bit is set and reset by software.
[0]	MCTM0EN	MCTM0 Clock Enable 0: MCTM0 clock disabled 1: MCTM0 clock enabled This bit is set and reset by software.

Clock Source Status Register – CKST

This register specifies the clock source status.

Offset: 0x034

Reset value: 0xC100_0000

	31	30	29	28	27	26	25	24
Type/Reset		CKSWST	Reserved					HSIST
	RO 1	RO 1				RO 0	RO 0	RO 1
	23	22	21	20	19	18	17	16
Type/Reset	Reserved					HSEST		
						RO 0	RO 0	
	15	14	13	12	11	10	9	8
Type/Reset	Reserved					PLLST		
	7	6	5	4	3	2	1	0
Type/Reset	Reserved							

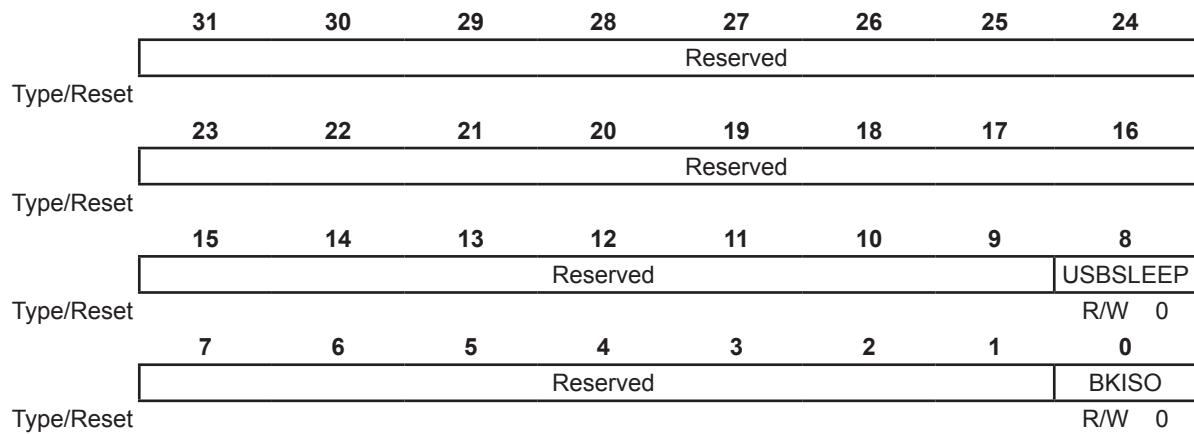
Bits	Field	Descriptions
[31:30]	CKSWST	Clock Switch Status 0X: CK_PLL used as system clock 10: CK_HSE used as system clock 11: CK_HSI used as system clock
[26:24]	HSIST	High Speed Internal Clock Occupation Status (CK_HSI) xx1: HSI used by System Clock (CK_SYS) (SW = 0x03) x1x: HSI used by PLL 1xx: HSI used by Clock Monitor
[17:16]	HSEST	High Speed External Clock Occupation Status (CK_HSE) x1: HSE used by System Clock (CK_SYS) (SW = 0x02) 1x: HSE used by PLL
[11:8]	PLLST	PLL Clock Occupation Status xxx1: PLL used by System Clock (CK_SYS) xx1x: PLL used by USART x1xx: PLL used by USB 1xxx: PLL used by CSIF

Low Power Control Register – LPCR

This register specifies low power control.

Offset: 0x300

Reset value: 0x0000_0000



Bits	Field	Descriptions
[8]	USBSLEEP	USB Sleep Software Control Enable Set and reset by software. Please refer to the Power Control Unit chapter for more information 0: Disable 1: Enable USB Software Sleeping
[0]	BKISO	Backup Domain Isolation Control 0: Backup domain isolated from other power domain 1: Backup domain accessible by other power domain This bit is set and reset by software. Refer to the Power Control Unit chapter for more information.

MCU Debug Control Register – MCUDBGCR

This register specifies the MCU debug control bits.

Offset: 0x304

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Reserved								
Type/Reset	23	22	21	20	19	18	17	16
Reserved								
Type/Reset	15	14	13	12	11	10	9	8
R/W 0								
Type/Reset	7	6	5	4	3	2	1	0
DBGPTM1 DBGPTM0 DBMCTM1 DBMCTM0 DBWDT DBPD DBDSLP1 DBSLP								
Type/Reset	R/W 0							

Bits	Field	Descriptions
[20]	DBTRACE	TRACESWO Debug Mode Enable 0: disable TRACESWO output 1: enable TRACESWO output Set and reset by software.
[19]	DB_UR1	UART1 Debug Mode Enable 0: Same behavior as in normal mode 1: UART1 FIFO timeout is frozen Set and reset by software. This bit is used to control whether the UART1 timeout mode is stopped or not when the core is halted.
[18]	DB_URO	UART0 Debug Mode Enable 0: Same behavior as in normal mode 1: UART0 FIFO timeout is frozen Set and reset by software. This bit is used to control whether the UART0 timeout mode is stopped or not when the core is halted.
[17]	DBBFTM1	BFTM1 Debug Mode Enable 0: BFTM1 counter keeps counting even if the core is halted 1: BFTM1 counter is stopped when the core is halted Set and reset by software. This bit is used to control whether the BFTM1 counter is stopped or not when the core is halted.
[16]	DBBFTM0	BFTM0 Debug Mode Enable 0: BFTM0 counter keeps counting even if the core is halted 1: BFTM0 counter is stopped when the core is halted Set and reset by software. This bit is used to control whether the BFTM0 counter is stopped or not when the core is halted.
[15]	DBSCI	SCI Debug Mode Enable 0: Same behavior as normal mode 1: SCI timeout is stopped Set and reset by software. This bit is used to control whether the SCI timeout mode is stopped or not when the core is halted.

Bits	Field	Descriptions
[14]	DBDSL2	Debug Deep-Sleep2 0: LDO = Off, DMOS = On, FCLK = Off and HCLK = Off in Deep-Sleep2 1: LDO = On, FCLK = On and HCLK = On in Deep-Sleep2 This bit is set and reset by software.
[13]	DBI2C1	I ² C1 Debug Mode Enable 0: Same behavior as normal mode 1: I ² C1 timeout is stopped Set and reset by software. This bit is used to control whether the I ² C1 timeout mode is stopped or not when the core is halted.
[12]	DBI2C0	I ² C0 Debug Mode Enable 0: Same behavior as normal mode 1: I ² C0 timeout is stopped Set and reset by software. This bit is used to control whether the I ² C0 timeout mode is stopped or not when the core is halted.
[11]	DBSPI1	SPI1 Debug Mode Enable 0: Same behavior as normal mode 1: SPI1 FIFO timeout is stopped Set and reset by software. This bit is used to control whether the SPI1 timeout mode is stopped or not when the core is halted.
[10]	DBSPI0	SPI0 Debug Mode Enable 0: Same behavior as normal mode 1: SPI0 FIFO timeout is stopped Set and reset by software. This bit is used to control whether the SPI0 timeout mode is stopped or not when the core is halted.
[9]	DBUSR1	USART1 Debug Mode Enable 0: Same behavior as normal mode 1: USART1 FIFO timeout is stopped Set and reset by software. This bit is used to control whether the USART1 timeout mode is stopped or not when the core is halted.
[8]	DBUSR0	USART0 Debug Mode Enable 0: Same behavior as normal mode 1: USART0 FIFO timeout is stopped Set and reset by software. This bit is used to control whether the USART0 timeout mode is stopped or not when the core is halted.
[7]	DBGPTM1	GPTM1 Debug Mode Enable 0: GPTM1 counter keeps counting even if the core is halted 1: GPTM1 counter is stopped when the core is halted Set and reset by software. This bit is used to control whether the GPTM1 counter is stopped or not when the core is halted.
[6]	DBGPTM0	GPTM0 Debug Mode Enable 0: GPTM0 counter keeps counting even if the core is halted 1: GPTM0 counter is stopped when the core is halted Set and reset by software. This bit is used to control whether the GPTM0 counter is stopped or not when the core is halted.
[5]	DBMCTM1	MCTM1 Debug Mode Enable 0: MCTM1 counter keeps counting even if the core is halted 1: MCTM1 counter is stopped when the core is halted Set and reset by software. This bit is used to control whether the MCTM1 counter is stopped or not when the core is halted.

Bits	Field	Descriptions
[4]	DBMCTM0	MCTM0 Debug Mode Enable 0: MCTM0 counter keeps counting even if the core is halted 1: MCTM0 counter is stopped when the core is halted Set and reset by software. This bit is used to control whether the MCTM0 counter is stopped or not when the core is halted.
[3]	DBWDT	Watchdog Timer Debug Mode Enable 0: Watchdog Timer counter keeps counting even if the core is halted 1: Watchdog Timer counter is stopped when the core is halted Set and reset by software. This bit is used to control whether the Watchdog Timer counter is stopped or not when the core is halted.
[2]	DBPD	Debug Power-Down Mode 0: LDO = Off, FCLK = Off, and HCLK = Off in Power-Down mode 1: LDO = On, FCLK = On, and HCLK = On in Power-Down mode This bit is set and reset by software.
[1]	DBDSLP1	Debug Deep-Sleep1 0: LDO = Low power mode, FCLK = Off, and HCLK = Off in Deep-Sleep1 1: LDO = On, FCLK = On, and HCLK = On in Deep-Sleep1 This bit is set and reset by software.
[0]	DBSLP	Debug Sleep Mode 0: LDO = On, FCLK = On, and HCLK = Off in Sleep mode 1: LDO = On, FCLK = On, and HCLK = On in Sleep mode This bit is set and reset by software.

7

Reset Control Unit (RSTCU)

Introduction

The Reset Control Unit, RSTCU, has three kinds of reset, the power on reset, system reset and APB unit reset. The power on reset, known as a cold reset, resets the full system during a power up. A system reset resets the processor core and peripheral IP components with the exception of the debug port controller. The resets can be triggered by an external signal, internal events and the reset generators. More information about these resets will be described in the following section

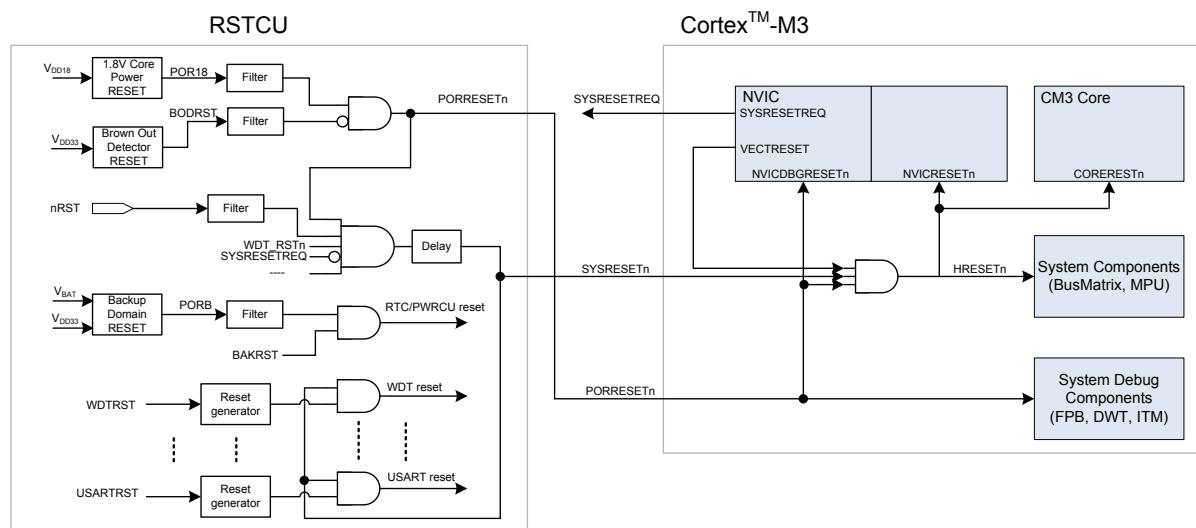


Figure 16. RSTCU Block Diagram

Functional Descriptions

Power On Reset

The Power on reset, POR, is generated by either an external reset or the internal reset generator. Both types have an internal filter to prevent glitches from causing erroneous reset operations. By referring to Figure 16, the POR18 active low signal will be de-asserted when the internal LDO voltage regulator is ready to provide 1.8 V power. In addition to the POR18 signal, the Power Control Unit, PWRCU, will assert the BODF signal as a Power Down Reset, PDR, when the BODEN bit in the LVDCSR register is set and the brown-out event occurs. For more details about the PWRCU function, refer to the PWRCU chapter.

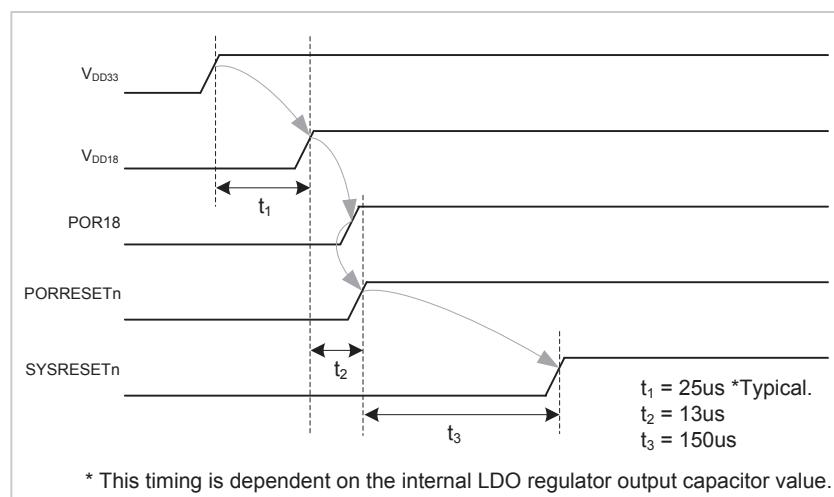


Figure 17. Power On Reset Sequence

System Reset

A system reset is generated by a power on reset (PORRESETn), a Watchdog Timer reset (WDT_RSTn), nRST pin or a software reset (SYSRESETREQ) event. For more information about SYSRESETREQ and VECTRESET events, refer to the related chapter in the Cortex™-M3 reference manual.

AHB and APB Unit Reset

The AHB and APB unit reset can be divided into hardware and software resets. A hardware reset can be generated by either power on reset or system reset for all AHB and APB units. Each functional IP connected to the AHB and APB buses can be reset individually through the associated software reset bits in the RSTCU. For example, the application software can generate a USART0 reset via the USR0RST bit in the APBPRSTR0 register.

Register Map

The following table shows the RSTCU registers and reset values.

Table 19. RSTCU Register Map

Register	Offset	Description	Reset Value
RSTCU Base Address = 0x4008_8000			
GRSR	0x100	Global Reset Status Register	0x0000_0008
AHBPRSTR	0x104	AHB Peripheral Reset Register	0x0000_0000
APBPRSTR0	0x108	APB Peripheral Reset Register 0	0x0000_0000
APBPRSTR1	0x10C	APB Peripheral Reset Register 1	0x0000_0000

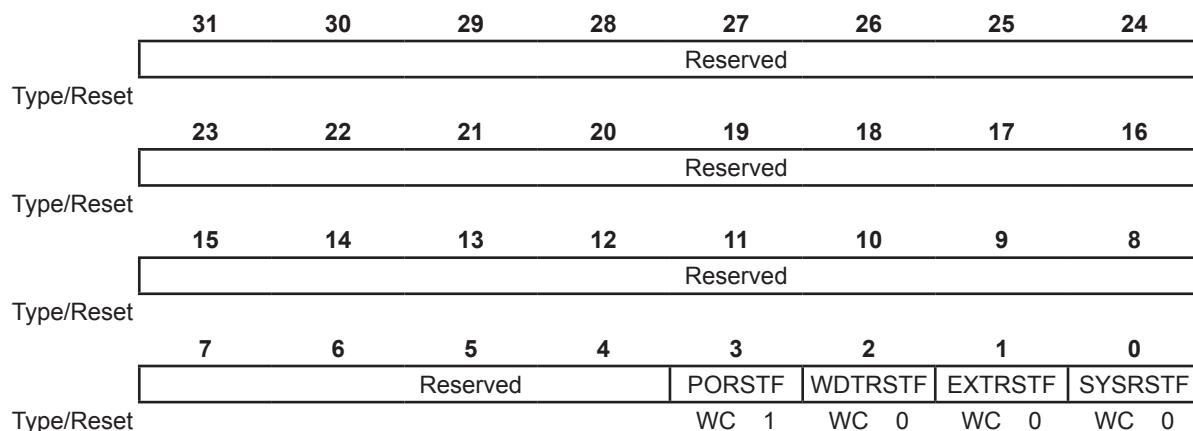
Register Descriptions

Global Reset Status Register – GRSR

This register specifies a variety of reset status conditions.

Offset: 0x100

Reset value: 0x0000_0008



Bits	Field	Descriptions
[3]	PORSTF	Core 1.8V Power On Reset Flag 0: No POR occurred 1: POR occurred This bit is set by hardware when a power on reset occurs and reset by writing 1 into it.
[2]	WDTRSTF	Watchdog Timer Reset Flag 0: No Watchdog Timer reset occurred 1: Watchdog Timer reset occurred This bit is set by hardware when a watchdog timer reset occurs and reset by writing 1 into it or by hardware when a power on reset occurs.
[1]	EXTRSTF	External Pin Reset Flag 0: No pin reset occurred 1: Pin reset occurred This bit is set by hardware when an external pin reset occurs and reset by writing 1 into it or by hardware when a power on reset occurs.

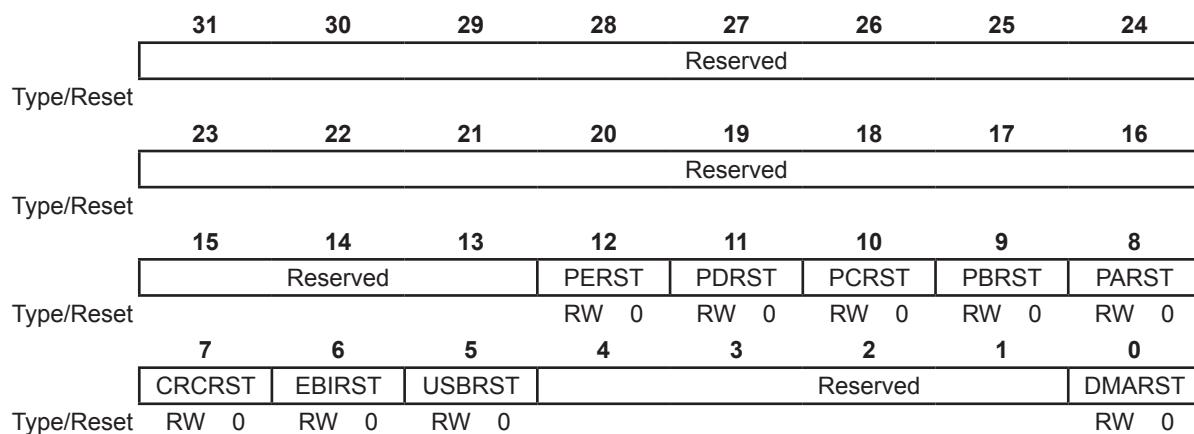
Bits	Field	Descriptions
[0]	SYSRSTF	<p>System Reset Flag</p> <p>0: No NVIC asserting system reset occurred</p> <p>1: NVIC asserting system reset occurred</p> <p>This bit is set by hardware when a system reset occurs and reset by writing 1 into it or by hardware when a power on reset occurs.</p>

AHB Peripheral Reset Register – AHBPRSTR

This register specifies several AHB peripheral software reset control bits.

Offset: 0x104

Reset value: 0x0000_0000



Bits	Field	Descriptions
[12]	PERST	<p>GPIO Port E Reset Control</p> <p>0: No reset</p> <p>1: Reset Port E</p> <p>This bit is set by software and cleared to 0 by hardware automatically.</p>
[11]	PDRST	<p>GPIO Port D Reset Control</p> <p>0: No reset</p> <p>1: Reset Port D</p> <p>This bit is set by software and cleared to 0 by hardware automatically.</p>
[10]	PCRST	<p>GPIO Port C Reset Control</p> <p>0: No reset</p> <p>1: Reset Port C</p> <p>This bit is set by software and cleared to 0 by hardware automatically.</p>
[9]	PBRST	<p>GPIO Port B Reset Control</p> <p>0: No reset</p> <p>1: Reset Port B</p> <p>This bit is set by software and cleared to 0 by hardware automatically.</p>
[8]	PARST	<p>GPIO Port A Reset Control</p> <p>0: No reset</p> <p>1: Reset Port A</p> <p>This bit is set by software and cleared to 0 by hardware automatically.</p>

Bits	Field	Descriptions
[7]	CRCRST	CRC Reset Control 0: No reset 1: Reset CRC This bit is set by software and cleared to 0 by hardware automatically.
[6]	EBIRST	EBI Reset Control 0: No reset 1: Reset EBI This bit is set by software and cleared to 0 by hardware automatically.
[5]	USBRST	USB Reset Control 0: No reset 1: Reset USB This bit is set by software and cleared to 0 by hardware automatically.
[0]	DMARST	Peripheral DMA (PDMA) Reset Control 0: No reset 1: Reset Peripheral DMA (PDMA) This bit is set by software and cleared to 0 by hardware automatically.

APB Peripheral Reset Register 0 – APBPRSTR0

This register specifies several APB peripheral software reset control bits.

Offset: 0x108

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Type/Reset	Reserved					I2SRST	SCIRST	
						RW 0	RW 0	
	23	22	21	20	19	18	17	16
Type/Reset	Reserved							
	15	14	13	12	11	10	9	8
Type/Reset	EXTIRST	AFIORST	Reserved		UR1RST	UR0RST	USR1RST	USR0RST
	RW 0	RW 0			RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
Type/Reset	Reserved		SPI1RST	SPI0RST	Reserved		I2C1RST	I2C0RST
			RW 0	RW 0			RW 0	RW 0

Bits	Field	Descriptions
[25]	I2SRST	I ² S Reset Control 0: No reset 1: Reset I ² S This bit is set by software and cleared to 0 by hardware automatically.
[24]	SCIRST	Smart Card Interface Reset Control 0: No reset 1: Reset Smart Card Interface This bit is set by software and cleared to 0 by hardware automatically.

Bits	Field	Descriptions
[15]	EXTIRST	External Interrupt Controller Reset Control 0: No reset 1: Reset EXTI This bit is set by software and cleared to 0 by hardware automatically.
[14]	AFIORST	Alternate Function I/O Reset Control 0: No reset 1: Reset Alternate Function I/O This bit is set by software and cleared to 0 by hardware automatically.
[11]	UR1RST	UART1 Reset Control 0: No reset 1: Reset UART1 This bit is set by software and cleared to 0 by hardware automatically.
[10]	UR0RST	UART0 Reset Control 0: No reset 1: Reset UART0 This bit is set by software and cleared to 0 by hardware automatically.
[9]	USR1RST	USART1 Reset Control 0: No reset 1: Reset USART1 This bit is set by software and cleared to 0 by hardware automatically.
[8]	USR0RST	USART0 Reset Control 0: No reset 1: Reset USART0 This bit is set by software and cleared to 0 by hardware automatically.
[5]	SPI1RST	SPI1 Reset Control 0: No reset 1: Reset SPI1 This bit is set by software and cleared to 0 by hardware automatically.
[4]	SPI0RST	SPI0 Reset Control 0: No reset 1: Reset SPI0 This bit is set by software and cleared to 0 by hardware automatically.
[1]	I2C1RST	I ² C1 Reset Control 0: No reset 1: Reset I ² C1 This bit is set by software and cleared to 0 by hardware automatically.
[0]	I2C0RST	I ² C0 Reset Control 0: No reset 1: Reset I ² C0 This bit is set by software and cleared to 0 by hardware automatically.

APB Peripheral Reset Register 1 – APBPRSTR1

This register specifies several APB peripheral software reset control bits.

Offset: 0x10C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Type/Reset	Reserved							
	23	22	21	20	19	18	17	16
Type/Reset	OPA1RST	OPA0RST	Reserved				BFTM1RST	BFTM0RST
	RW 0	RW 0						
	15	14	13	12	11	10	9	8
Type/Reset	Reserved				GPTM1RST		GPTM0RST	
					RW 0	RW 0		
	7	6	5	4	3	2	1	0
Type/Reset	Reserved		WDTRST	Reserved		MCTM1RST	MCTM0RST	
			RW 0			RW 0	RW 0	

Bits	Field	Descriptions
[24]	ADCRST	A/D Converter Reset Control 0: No reset 1: Reset A/D Converter This bit is set by software and cleared to 0 by hardware automatically.
[23]	OPA1RST	Comparator and OPA1 Controller Reset Control 0: No reset 1: Reset CMP/OPA1 This bit is set by software and cleared to 0 by hardware automatically.
[22]	OPA0RST	Comparator and OPA0 Controller Reset Control 0: No reset 1: Reset CMP/OPA0 This bit is set by software and cleared to 0 by hardware automatically.
[17]	BFTM1RST	BFTM1 Reset Control 0: No reset 1: Reset BFTM1 This bit is set by software and cleared to 0 by hardware automatically.
[16]	BFTM0RST	BFTM0 Reset Control 0: No reset 1: Reset BFTM0 This bit is set by software and cleared to 0 by hardware automatically.

Bits	Field	Descriptions
[9]	GPTM1RST	GPTM1 Reset Control 0: No reset 1: Reset GPTM1 This bit is set by software and cleared to 0 by hardware automatically.
[8]	GPTM0RST	GPTM0 Reset Control 0: No reset 1: Reset GPTM0 This bit is set by software and cleared to 0 by hardware automatically.
[4]	WDTRST	Watchdog Timer Reset Control 0: No reset 1: Reset Watchdog Timer This bit is set by software and cleared to 0 by hardware automatically.
[1]	MCTM1RST	MCTM1 Reset Control 0: No reset 1: Reset MCTM1 This bit is set by software and cleared to 0 by hardware automatically.
[0]	MCTM0RST	MCTM0 Reset Control 0: No reset 1: Reset MCTM0 This bit is set by software and cleared to 0 by hardware automatically.

8 General Purpose I/O (GPIO)

Introduction

There are up to 80 General Purpose I/O port, GPIO, named PA0 ~ PA15, PB0 ~ PB15, PC0 ~ PC15, PD0 ~ PD15 and PE0 ~ PE15 for the device to implement the logic input/output functions. Each of the GPIO ports has related control and configuration registers to satisfy the requirement of specific applications.

The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the AF input or output pins.

The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit (EXTI).

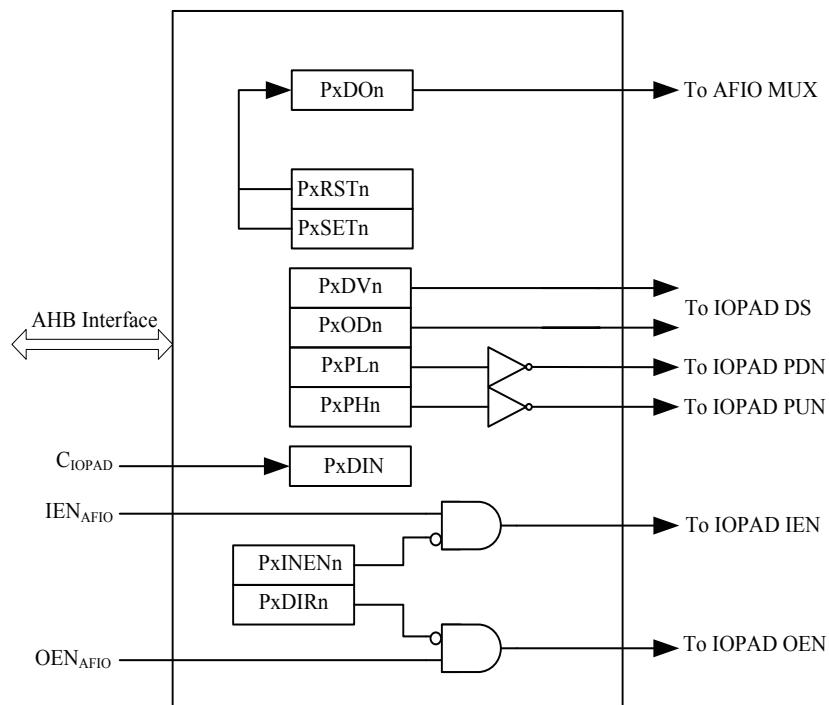


Figure 18. GPIO Block Diagram

Features

- Input/output direction control
- Schmitt Trigger Input function enable control
- Input weak pull-up/pull-down control
- Output push-pull/open drain enable control
- Output set/reset control
- Output drive current selection
- External interrupt with programmable trigger edge - using EXTI configuration registers
- Analog input/output configurations – using AFIO configuration registers
- Alternate function input/output configurations - using AFIO configuration registers
- Port configuration lock

Functional Descriptions

Default GPIO Pin Configuration

During or just after the reset period, the alternative functions are all inactive and the GPIO ports are configured into the input disable floating mode, i.e. input disabled without pull-up/pull-down resistors. Only the boot and Serial-Wired Debug pins which are pin-shared with the I/O pins PA8, PA9, PA11, PA12 and PA13 are active after a device reset.

- PA8/BOOT0: Input enable with internal pull-up
- PA9/BOOT1: Input enable with internal pull-up
- PA11/TRACESWO: Output
- PA12/SWCLK: Input enable with internal pull-up
- PA13/SWDIO: Input enable with internal pull-up

General Purpose I/O – GPIO

The GPIO pins can be configured as inputs or outputs via the data direction control registers PxDIRCR (where x = A ~ E). When the GPIO pins are configured as input pins, the data on the external pads can be read if the enable bits in the input enable function register PxINER are set. The GPIO pull-up/pull-down registers PxPUR/PxPDR can be configured to fit specific applications. When the pull-up and pull-down functions are both enabled, the pull-up function has the higher priority while the pull-down function will be blocked until the pull-up function is released.

The GPIO pins can be configured as output pins where the output data is latched into the data register PxDOUTR. The output type can be setup to be either push-pull or open-drain by the open drain selection register PxODR. Only one or several specific bits of the output data will be set or reset by configuring the port output set and reset control register PxSRR or the port output reset control register PxRR without affecting the unselected bits. As the port output set and reset functions are both enabled, the port output set function has the higher priority and the port output reset function will be blocked. The output driving current of the GPIO pins can be selected by configuring the drive current selection register PxDRVVR.

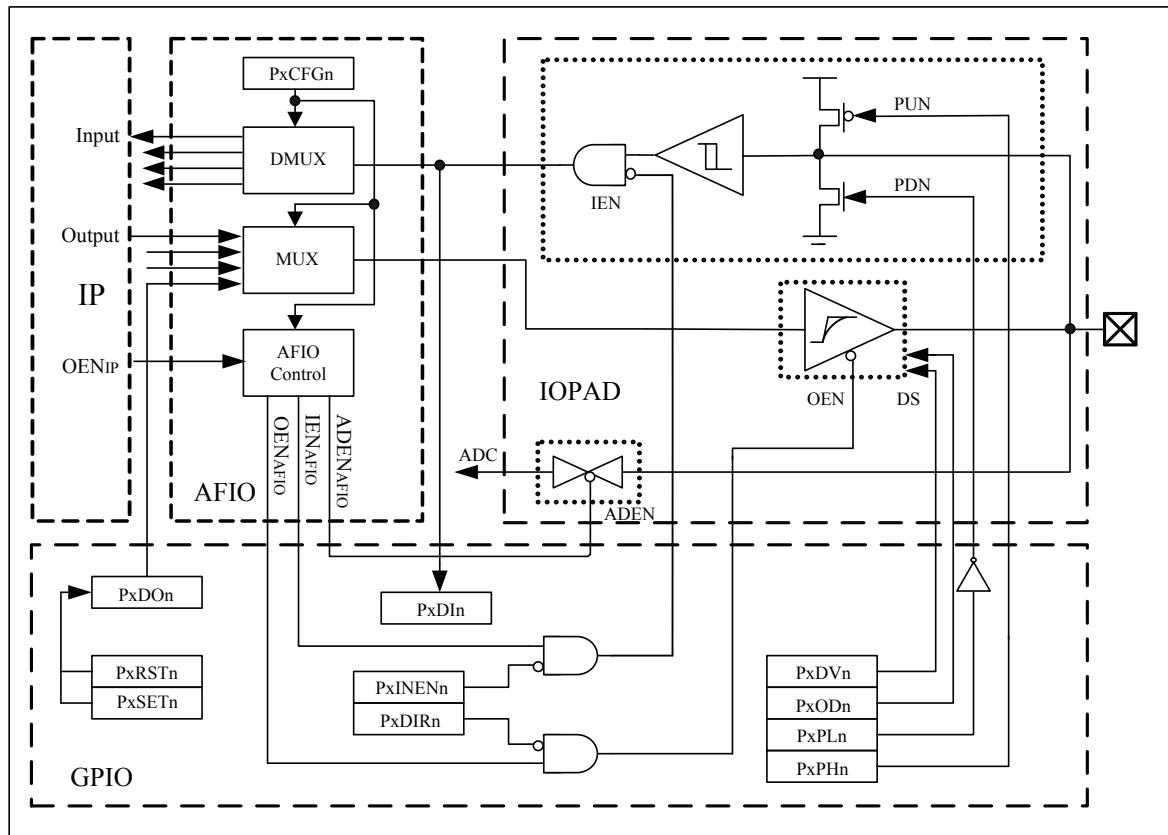


Figure 19. AFIO(GPIO) Control Signal

PxDIn/PxDO_n(x=A~E): Data Input/Data Output PxRSTn/PxSETn(x=A~E): Reset/Set

PxDIR_n(x=A~E): Direction PxINEN_n(x=A~E): Input Enable

PxDVn(x=A~E): Output Drive PxODn(x=A~E): Open Drain

PxPLn/PxPHn(x=A~E): Pull Low/High PxCFGn(x=A~E): AFIO Configuration

Table 20. AFIO, GPIO and IO Pad Control Signal True Table

Type	AFIO			GPIO		PAD		
	ADEN _{AFIO}	OEN _{AFIO}	IEN _{AFIO}	PxDIR _n	PxINEN _n	ADEN	OEN	IEN
GPIO Input ^(Note)	1	1	1	0	1	1	1	0
GPIO Output ^(Note)	1	1	1	1	0 (1 if need)	1	0	1 (0)
AFIO Input	1	1	0	0	X	1	1	0
AFIO Output	1	0	1	X	0 (1 if need)	1	0	1 (0)
ADC Input	0	1	1	0	0 (1 if need)	0	1	1 (0)
OSC Output	0	1	1	0	0 (1 if need)	0	1	1 (0)

Note: The signals, IEN and OEN, for I/O pads are derived from the GPIO register bits PxINEN_n and PxDIR_n respectively when the associated pin is configured in the GPIO input/output mode.

GPIO Locking Mechanism

The GPIO also offers a lock function to lock the port until a reset event occurs. The PxLOCKR ($x = A \sim E$) registers are used to lock the port x and lock control options. The value 0x5FA0 is written into the PxLKEY field in the PxLOCKR registers to freeze the PxDIRCR, PxINER, PxPUR, PxPDR, PxODR, PxDRVVR control and AFIO mode configuration (GPxCFGHR or GPxCFGLR, where $x = A \sim E$). If the value in the PxLOCKR is 0x5FA0_0001, it means that the Port x Lock function is enabled and the Port x pin 0 is frozen.

Register Map

The following table shows the GPIO registers and reset values of the Port A ~ E.

Table 21. GPIO Register Map

Register	Offset	Description	Reset Value
GPIO A Base Address = 0x400B_0000			
PADIRCR	0x000	Port A Data Direction Control Register	0x0000_0000
PAINER	0x004	Port A Input Function Enable Control Register	0x0000_C300
PAPUR	0x008	Port A Pull-Up Selection Register	0x0000_F300
PAPDR	0x00C	Port A Pull-Down Selection Register	0x0000_0000
PAODR	0x010	Port A Open Drain Selection Register	0x0000_0000
PADRVR	0x014	Port A Drive Current Selection Register	0x0000_0000
PALOCKR	0x018	Port A Lock Register	0x0000_0000
PADINR	0x01C	Port A Data Input Register	0x0000_F300
PADOUTR	0x020	Port A Data Output Register	0x0000_0000
PASRR	0x024	Port A Output Set and Reset Control Register	0x0000_0000
PARR	0x028	Port A Output Reset Control Register	0x0000_0000
GPIO B Base Address = 0x400B_2000			
PBDIRCR	0x000	Port B Data Direction Control Register	0x0000_0000
PBINER	0x004	Port B Input Function Enable Control Register	0x0000_0000
PBPUR	0x008	Port B Pull-Up Selection Register	0x0000_0000
PBPDR	0x00C	Port B Pull-Down Selection Register	0x0000_0000
PBODR	0x010	Port B Open Drain Selection Register	0x0000_0000
PBDRVVR	0x014	Port B Drive Current Selection Register	0x0000_0000
PBLOCKR	0x018	Port B Lock Register	0x0000_0000
PBDINR	0x01C	Port B Data Input Register	0x0000_0000
PBDOUTR	0x020	Port B Data Output Register	0x0000_0000
PBSRR	0x024	Port B Output Set and Reset Control Register	0x0000_0000
PBRR	0x028	Port B Output Reset Control Register	0x0000_0000
GPIO C Base Address = 0x400B_4000			
PCDIRCR	0x000	Port C Data Direction Control Register	0x0000_0000
PCINER	0x004	Port C Input Function Enable Control Register	0x0000_0000
PCPUR	0x008	Port C Pull-Up Selection Register	0x0000_0000
PCPDR	0x00C	Port C Pull-Down Selection Register	0x0000_0000
PCODR	0x010	Port C Open Drain Selection Register	0x0000_0000
PCDRVVR	0x014	Port C Drive Current Selection Register	0x0000_0000
PCLOCKR	0x018	Port C Lock Register	0x0000_0000
PCDINR	0x01C	Port C Data Input Register	0x0000_0000

PCDOUTR	0x020	Port C Data Output Register	0x0000_0000
PCSRR	0x024	Port C Output Set and Reset Control Register	0x0000_0000
PCRR	0x028	Port C Output Reset Control Register	0x0000_0000

GPIO D Base Address = 0x400B_6000

PDDIRCR	0x000	Port D Data Direction Control Register	0x0000_0000
PDINER	0x004	Port D Input Function Enable Control Register	0x0000_0000
PDPUR	0x008	Port D Pull-Up Selection Register	0x0000_0000
PDPDR	0x00C	Port D Pull-Down Selection Register	0x0000_0000
PDODR	0x010	Port D Open Drain Selection Register	0x0000_0000
PDDRVR	0x014	Port D Drive Current Selection Register	0x0000_0000
PDLOCKR	0x018	Port D Lock Register	0x0000_0000
PDDINR	0x01C	Port D Data Input Register	0x0000_0000
PDDOUTR	0x020	Port D Data Output Register	0x0000_0000
PDSRR	0x024	Port D Output Set and Reset Control Register	0x0000_0000
PDRR	0x028	Port D Output Reset Control Register	0x0000_0000

GPIO E Base Address = 0x400B_8000

PEDIRCR	0x000	Port E Data Direction Control Register	0x0000_0000
PEINER	0x004	Port E Input Function Enable Control Register	0x0000_0000
PEPUR	0x008	Port E Pull-Up Selection Register	0x0000_0000
PEPDR	0x00C	Port E Pull-Down Selection Register	0x0000_0000
PEODR	0x010	Port E Open Drain Selection Register	0x0000_0000
PEDRVR	0x014	Port E Drive Current Selection Register	0x0000_0000
PELOCKR	0x018	Port E Lock Register	0x0000_0000
PEDINR	0x01C	Port E Data Input Register	0x0000_0000
PEDOUTR	0x020	Port E Data Output Register	0x0000_0000
PESRR	0x024	Port E Output Set and Reset Control Register	0x0000_0000
PERR	0x028	Port E Output Reset Control Register	0x0000_0000

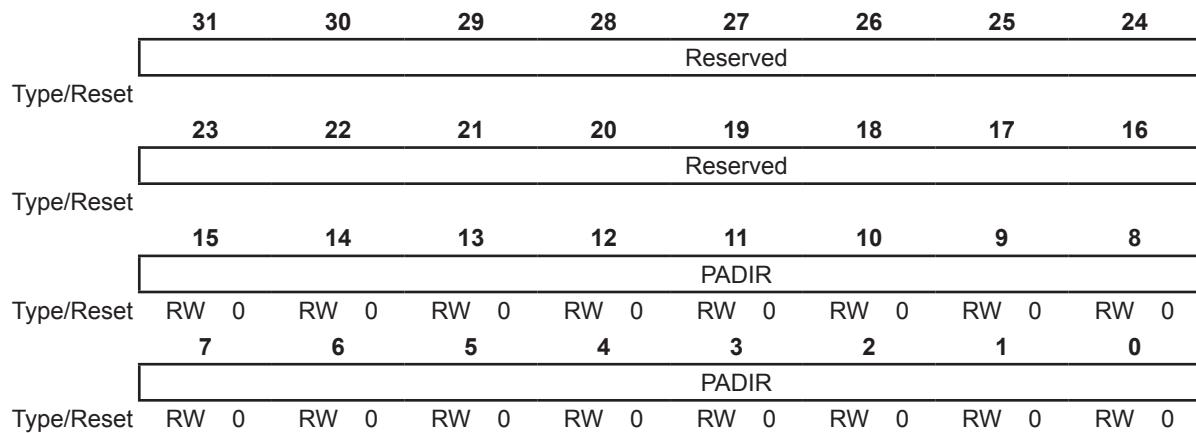
Register Descriptions

Port A Data Direction Control Register – PADIRCR

This register is used to control the direction of the GPIO Port A pin as input or output.

Offset: 0x000

Reset value: 0x0000_0000



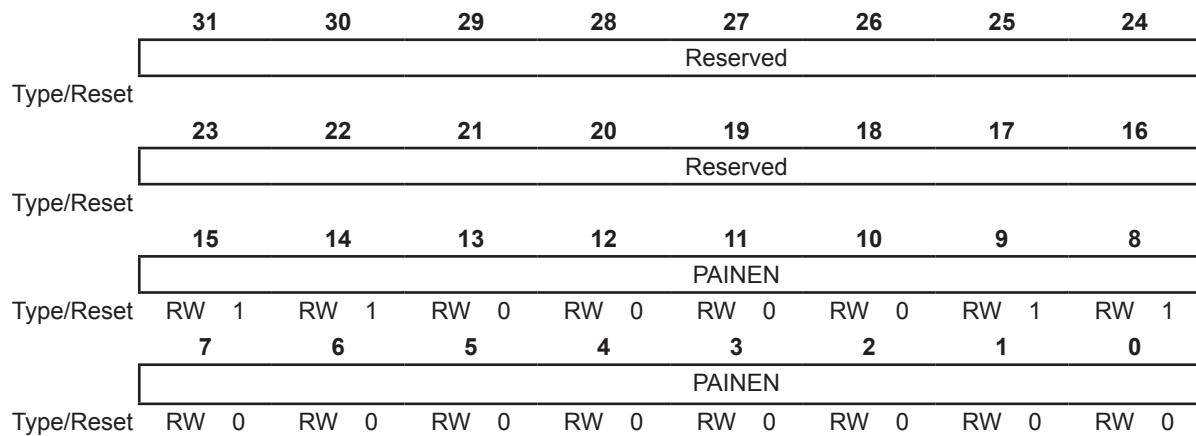
Bits	Field	Descriptions
[15:0]	PADIRn	GPIO Port A pin n Direction Control Bits (n = 0 ~ 15) 0: Pin n is input mode 1: Pin n is output mode

Port A Input Function Enable Control Register – PAINER

This register is used to enable or disable the GPIO Port A input function.

Offset: 0x004

Reset value: 0x0000_C300



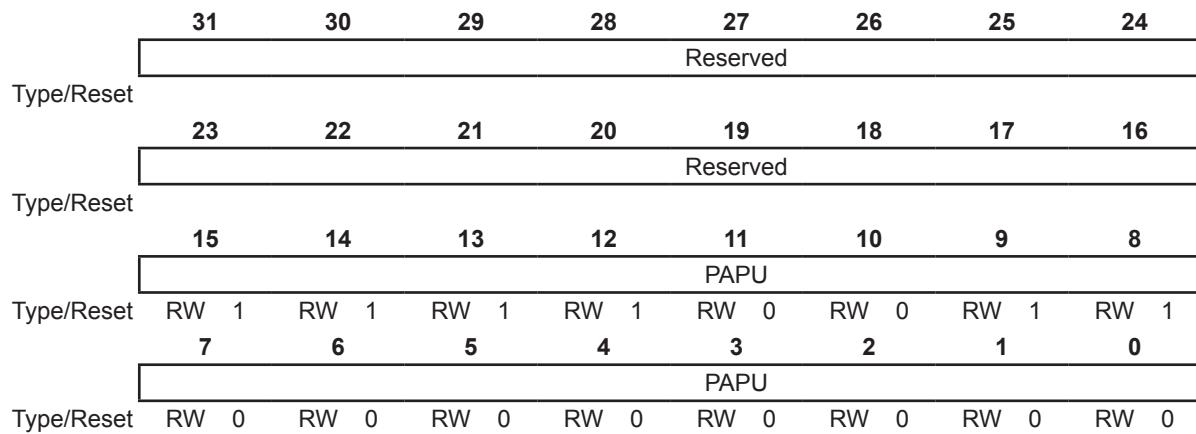
Bits	Field	Descriptions
[15:0]	PAINENn	<p>GPIO Port A pin n Input Enable Control Bits (n = 0 ~ 15)</p> <p>0: Pin n input function is disabled. 1: Pin n input function is enabled.</p> <p>When the pin n input function is disabled, the input Schmitt trigger will be turned off and the Schmitt trigger output will remain at a zero state.</p>

Port A Pull-Up Selection Register – PAPUR

This register is used to enable or disable the GPIO Port A pull-up function.

Offset: 0x008

Reset value: 0x0000_F300



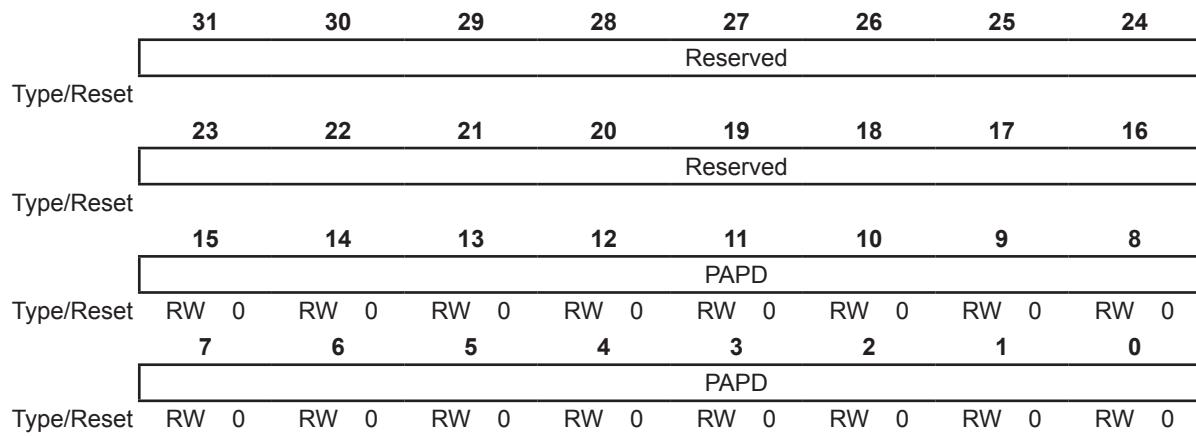
Bits	Field	Descriptions
[15:0]	PAPUn	<p>GPIO Port A pin n Pull-Up Selection Control Bits (n = 0 ~ 15)</p> <p>0: Pin n pull-up function is disabled 1: Pin n pull-up function is enabled</p> <p>Note: When the pull-up and pull-down functions are both enabled, the pull-up function will have the higher priority and therefore the pull-down function will be blocked and disabled.</p>

Port A Pull-Down Selection Register – PAPDR

This register is used to enable or disable the GPIO Port A pull-down function.

Offset: 0x00C

Reset value: 0x0000_0000



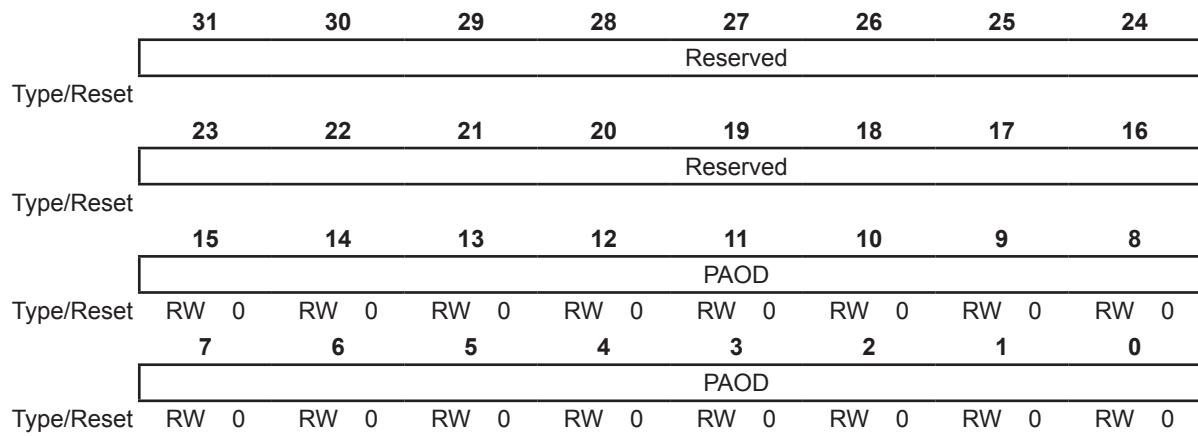
Bits	Field	Descriptions
[15:0]	PAPDn	<p>GPIO Port A pin n Pull-Down Selection Control Bits (n = 0 ~ 15)</p> <p>0: Pin n pull-down function is disabled 1: Pin n pull-down function is enabled</p> <p>Note: When the pull-up and pull-down functions are both enabled, the pull-up function will have the higher priority and therefore the pull-down function will be blocked and disabled.</p>

Port A Open Drain Selection Register – PAODR

This register is used to enable or disable the GPIO Port A open drain function.

Offset: 0x010

Reset value: 0x0000_0000



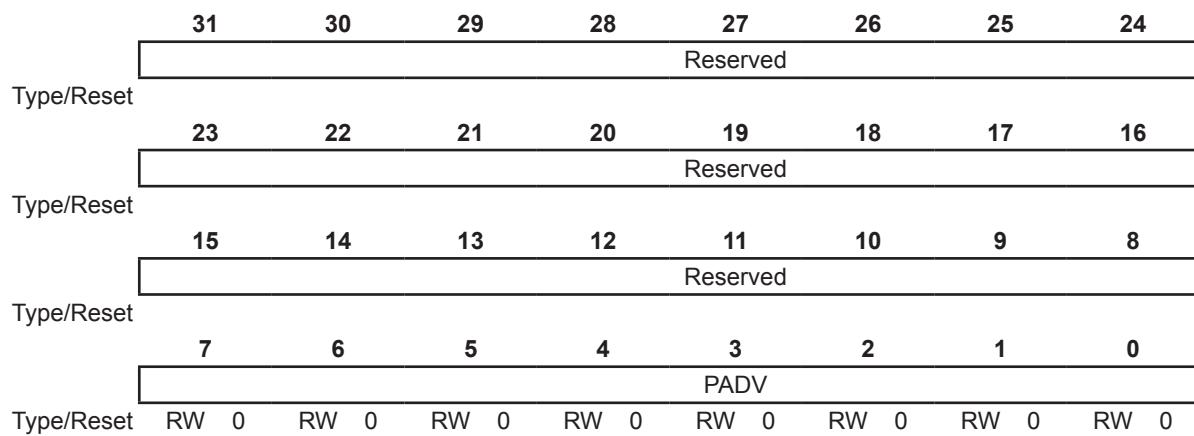
Bits	Field	Descriptions
[15:0]	PAODn	GPIO Port A pin n Open Drain Selection Control Bits (n = 0 ~ 15) 0: Pin n Open Drain output is disabled. (The output type is CMOS output) 1: Pin n Open Drain output is enabled. (The output type is open-drain output)

Port A Output Current Drive Selection Register – PADRVR

This register specifies the GPIO Port A output driving current.

Offset: 0x014

Reset value: 0x0000_0000



Port A Lock Register – PALOCKR

This register specifies the GPIO Port A lock configuration.

Offset: 0x018

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
PALKEY								
Type/Reset	RW 0							
23 22 21 20 19 18 17 16								
PALKEY								
Type/Reset	RW 0							
15 14 13 12 11 10 9 8								
PALOCK								
Type/Reset	RW 0							
7 6 5 4 3 2 1 0								
PALOCK								
Type/Reset	RW 0							

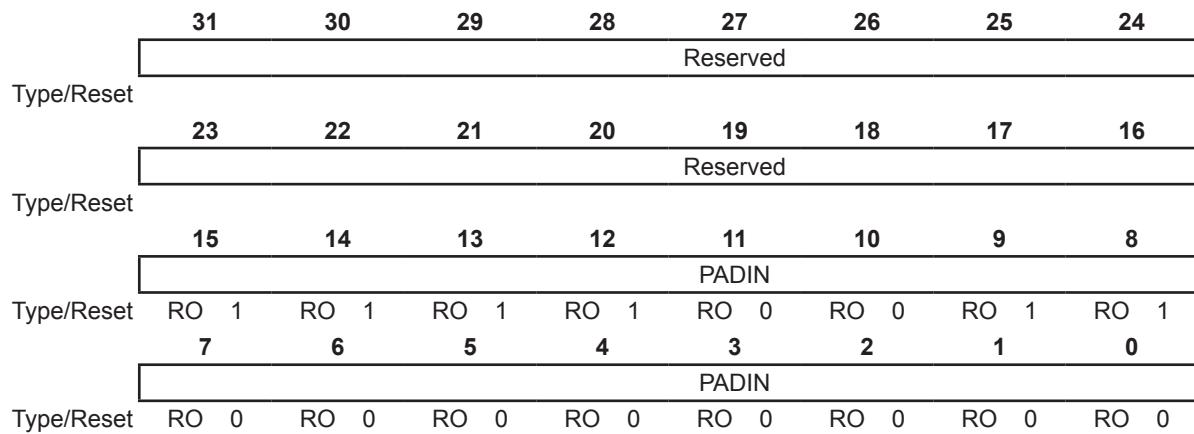
Bits	Field	Descriptions
[31:16]	PALKEY	<p>GPIO Port A Lock Key</p> <p>0x5FA0: Port A Lock function is enable</p> <p>Others: Port A Lock function is disable</p> <p>To lock the Port A function, a value 0x5FA0 should be written into the PALKEY field in this register. To execute a successful write operation on this lock register, the value written into the PALKEY field must be 0x5FA0. If the value written into this field is not equal to 0x5FA0, any write operations on the PALOCKR register will be aborted. The result of a read operation on the PALKEY field returns the GPIO Port A Lock Status which indicates whether the GPIO Port A is locked or not. If the read value of the PALKEY field is 0, this indicates that the GPIO Port A Lock function is disabled. Otherwise, it indicates that the GPIO Port A Lock function is enabled as the read value is equal to 1.</p>
[15:0]	PALOCKn	<p>GPIO Port A Pin n Lock Control Bits (n = 0 ~ 15)</p> <p>0: Port A Pin n is not locked</p> <p>1: Port A Pin n is locked</p> <p>The PALOCKn bits are used to lock the configurations of corresponding GPIO Pins when the correct Lock Key is applied to the PALKEY field. The locked configurations including PADIRn, PAINENn, PAPUn, PAPDn, PAODn and PADVn setting in the related GPIO registers. Additionally, the GPACFGHR or GPACFGLR field which is used to configure the alternative function of the associated GPIO pin will also be locked. Note that the PALOCKR can only be written once which means that PALKEY and PALOCKn (lock control bit) should be written together and can not be changed until a system reset or GPIO Port A reset occurs.</p>

Port A Data Input Register – PADINR

This register specifies the GPIO Port A input data.

Offset: 0x01C

Reset value: 0x0000_F300



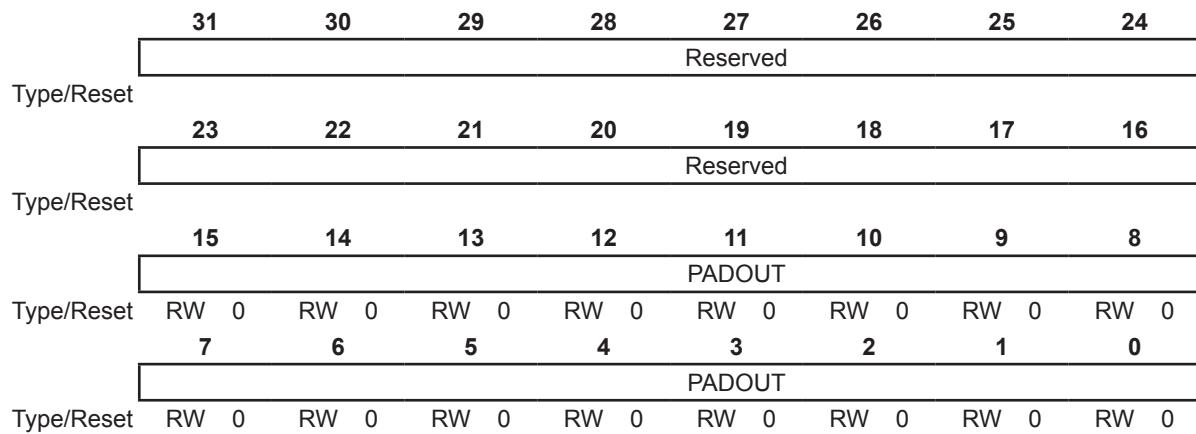
Bits	Field	Descriptions
[15:0]	PADINn	GPIO Port A pin n Data Input Bits (n = 0 ~ 15) 0: The input data of pin is 0 1: The input data of pin is 1

Port A Output Data Register – PADOUTR

This register specifies the GPIO Port A output data.

Offset: 0x020

Reset value: 0x0000_0000



Bits	Field	Descriptions
[15:0]	PADOUTn	GPIO Port A pin n Data Output Bits (n = 0 ~ 15) 0: Data to be output on pin n is 0 1: Data to be output on pin n is 1

Port A Output Set/Reset Control Register – PASRR

This register is used to set or reset the corresponding bit of the GPIO Port A output data.

Offset: 0x024

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
PARST								
Type/Reset	WO 0							
23 22 21 20 19 18 17 16								
PARST								
Type/Reset	WO 0							
15 14 13 12 11 10 9 8								
PASET								
Type/Reset	WO 0							
7 6 5 4 3 2 1 0								
PASET								
Type/Reset	WO 0							

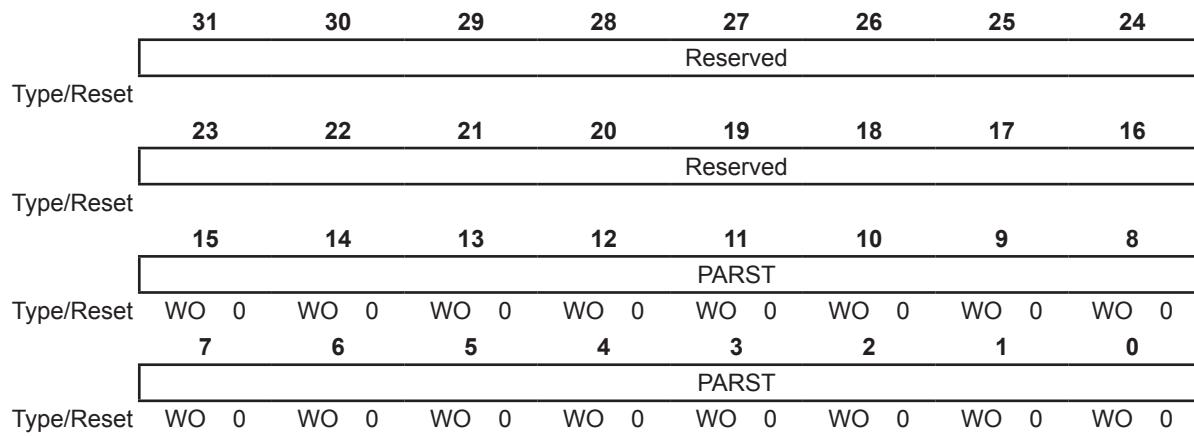
Bits	Field	Descriptions
[31:16]	PARSTn	GPIO Port A pin n Output Reset Control Bits (n = 0 ~ 15) 0: No effect on the PADOUTn bit 1: Reset the PADOUTn bit
[15:0]	PASETn	GPIO Port A pin n Output Set Control Bits (n = 0 ~ 15) 0: No effect on the PADOUTn bit 1: Set the PADOUTn bit Note that the function enabled by the PASETn bit has the higher priority if both the PASETn and PARSTn bits are set at the same time.

Port A Output Reset Register – PARR

This register is used to reset the corresponding bit of the GPIO Port A output data.

Offset: 0x028

Reset value: 0x0000_0000



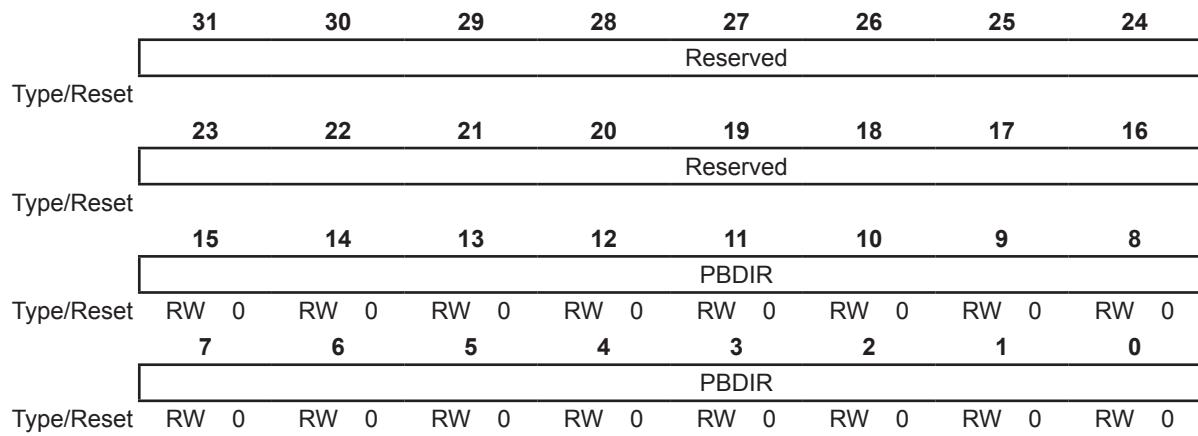
Bits	Field	Descriptions
[15:0]	PARSTn	GPIO Port A pin n Output Reset Bits (n = 0 ~ 15) 0: No effect on the PADOUTn bit 1: Reset the PADOUTn bit

Port B Data Direction Control Register – PBDIRCR

This register is used to control the direction of GPIO Port B pin as input or output.

Offset: 0x000

Reset value: 0x0000_0000



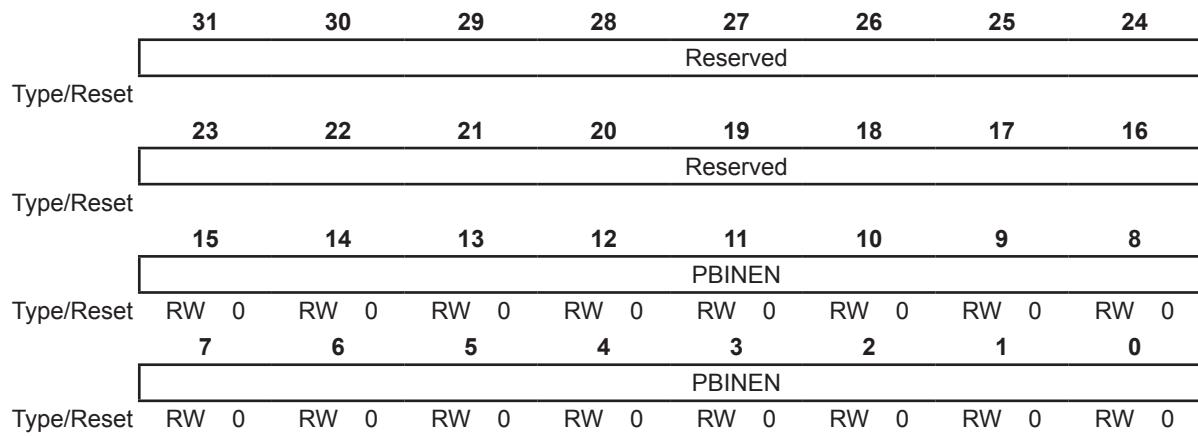
Bits	Field	Descriptions
[15:0]	PBDIRn	GPIO Port B pin n Direction Control Bits (n = 0 ~ 15) 0: Pin n is input mode 1: Pin n is output mode

Port B Input Function Enable Control Register – PBINER

This register is used to enable or disable the GPIO Port B input function.

Offset: 0x004

Reset value: 0x0000_0000



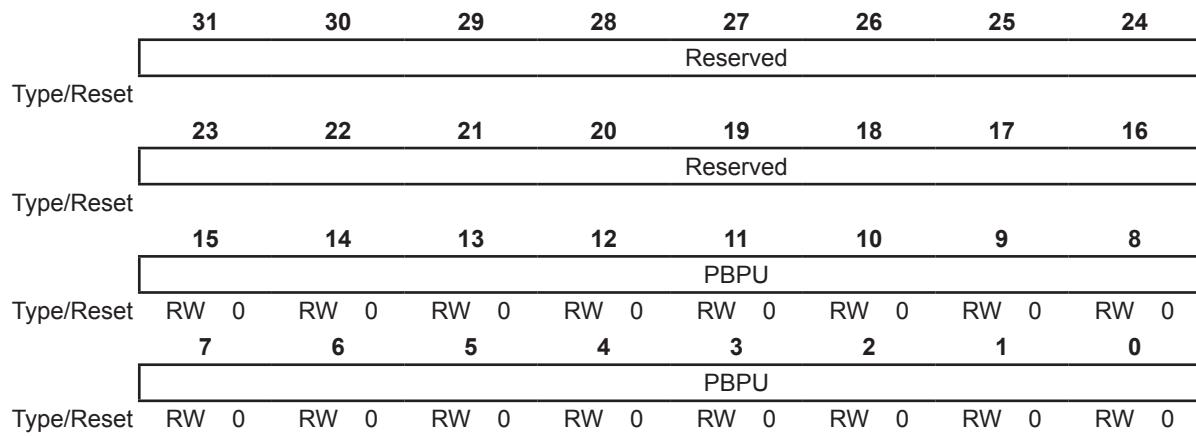
Bits	Field	Descriptions
[15:0]	PBINENn	<p>GPIO Port B pin n Input Enable Control Bits (n = 0 ~ 15)</p> <p>0: Pin n input function is disabled. 1: Pin n input function is enabled.</p> <p>When the pin n input function is disabled, the input Schmitt trigger will be turned off and the Schmitt trigger output will remain at a zero state.</p>

Port B Pull-Up Selection Register – PBPUR

This register is used to enable or disable the GPIO Port B pull-up function.

Offset: 0x008

Reset value: 0x0000_0000



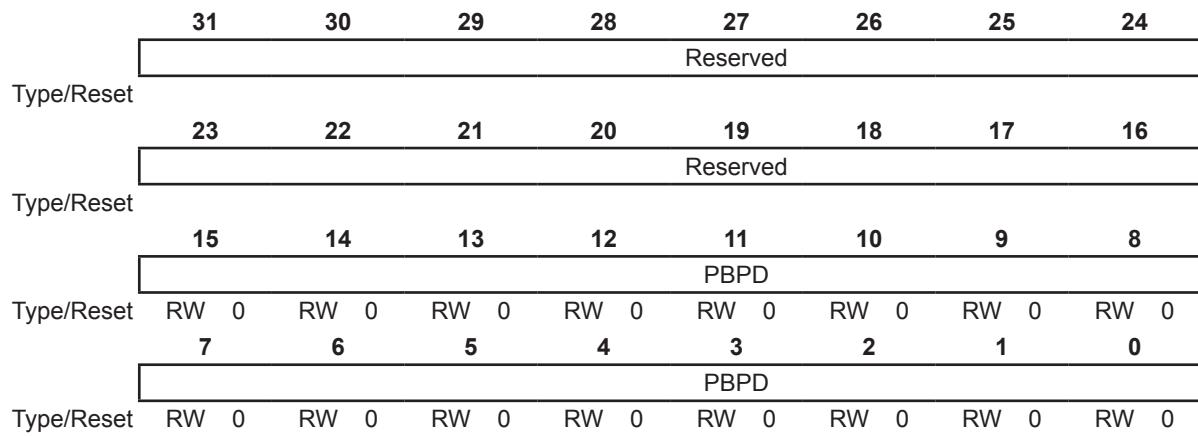
Bits	Field	Descriptions
[15:0]	PBPUn	<p>GPIO Port B pin n Pull-Up Selection Control Bits (n = 0 ~ 15)</p> <p>0: Pin n pull-up function is disabled 1: Pin n pull-up function is enabled</p> <p>Note: When the pull-up and pull-down functions are both enabled, the pull-up function will have the higher priority and therefore the pull-down function will be blocked and disabled.</p>

Port B Pull-Down Selection Register – PBPDR

This register is used to enable or disable the GPIO Port B pull-down function.

Offset: 0x00C

Reset value: 0x0000_0000



Bits	Field	Descriptions
[15:0]	PBPDn	<p>GPIO Port B pin n Pull-Down Selection Control Bits (n = 0 ~ 15)</p> <p>0: Pin n pull-down function is disabled</p> <p>1: Pin n pull-down function is enabled</p> <p>Note: When the pull-up and pull-down functions are both enabled, the pull-up function will have the higher priority and therefore the pull-down function will be blocked and disabled.</p>

Port B Open Drain Selection Register – PBODR

This register is used to enable or disable the GPIO Port B open drain function.

Offset: 0x010

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24	
Type/Reset	Reserved								
	23	22	21	20	19	18	17	16	
Type/Reset	Reserved								
	15	14	13	12	11	10	9	8	
Type/Reset	RW	0	RW	0	RW	0	RW	0	
	7	6	5	4	3	2	1	0	
Type/Reset	RW	0	RW	0	RW	0	RW	0	
	PBOD								
Type/Reset	RW	0	RW	0	RW	0	RW	0	

Bits	Field	Descriptions
[15:0]	PBODn	GPIO Port B pin n Open Drain Selection Control Bits (n = 0 ~ 15) 0: Pin n Open Drain output is disabled. (The output type is CMOS output) 1: Pin n Open Drain output is enabled. (The output type is open-drain output)

Port B Output Current Drive Selection Register – PBDRVVR

This register specifies the GPIO Port B output driving current.

Offset: 0x014

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24	
Type/Reset	Reserved								
	23	22	21	20	19	18	17	16	
Type/Reset	Reserved								
	15	14	13	12	11	10	9	8	
Type/Reset	RW	0	RW	0	Reserved		PBDV		
	7	6	5	4	3	2	1	0	
Type/Reset	RW	0	RW	0	Reserved				

Bits	Field	Descriptions
[15:14]	PBDVn	GPIO Port B pin n Output Current Drive Selection Control Bits (n = 6 ~ 11, 14~15)
[11:6]		0: 4mA source/sink current 1: 8mA source/sink current

Port B Lock Register – PBLOCKR

This register specifies the GPIO Port B lock configuration.

Offset: 0x018

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
PBLKEY								
Type/Reset	RW 0							
23 22 21 20 19 18 17 16								
PBLKEY								
Type/Reset	RW 0							
15 14 13 12 11 10 9 8								
PBLOCK								
Type/Reset	RW 0							
7 6 5 4 3 2 1 0								
PBLOCK								
Type/Reset	RW 0							

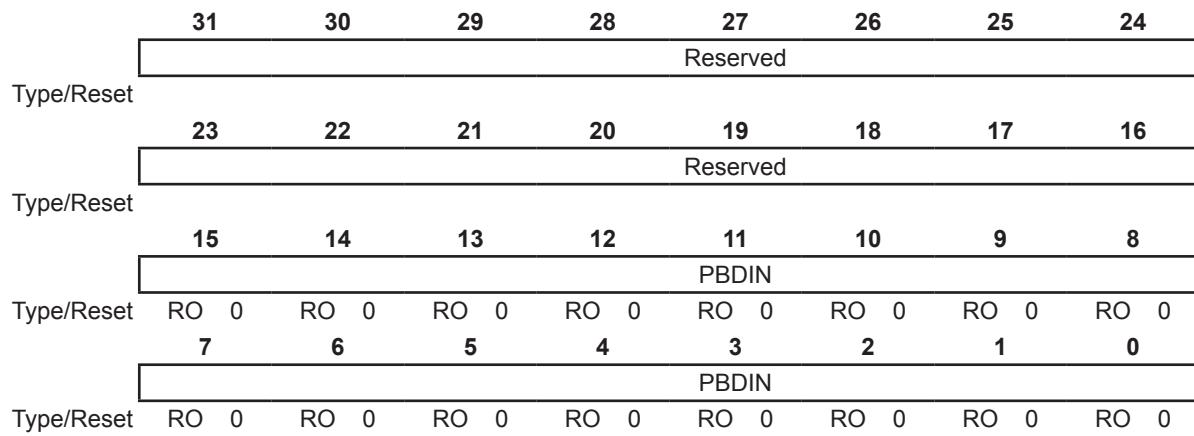
Bits	Field	Descriptions
[31:16]	PBLKEY	<p>GPIO Port Block Key</p> <p>0x5FA0: Port Block function is enable</p> <p>Others: Port B Lock function is disable</p> <p>To lock the Port B function, a value 0x5FA0 should be written into the PBLKEY field in this register. To execute a successful write operation on this lock register, the value written into the PBLKEY field must be 0x5FA0. If the value written into this field is not equal to 0x5FA0, any write operations on the PBLOCKR register will be aborted. The result of a read operation on the PBLKEY field returns the GPIO Port B Lock Status which indicates whether the GPIO Port B is locked or not. If the read value of the PBLKEY field is 0, this indicates that the GPIO Port B Lock function is disabled. Otherwise, it indicates that the GPIO Port B Lock function is enabled as the read value is equal to 1.</p>
[15:0]	PBLOCKn	<p>GPIO Port B pin n Lock Control Bits (n = 0 ~ 15)</p> <p>0: Port B pin n is not locked</p> <p>1: Port B pin n is locked</p> <p>The PBLOCKn bits are used to lock the configurations of corresponding GPIO Pins when the correct Lock Key is applied to the PBLKEY field. The locked configurations including PBDIRn, PBINENn, PBPUn, PBPDn and PBODn setting in the related GPIO registers. Additionally, the GPBCFGHR or GPBCFGLR field which is used to configure the alternative function of the associated GPIO pin will also be locked. Note that the PBLOCKR can only be written once which means that PBLKEY and PBLOCKn (lock control bit) should be written together and can not be changed until a system reset or GPIO Port B reset occurs.</p>

Port B Data Input Register – PBDINR

This register specifies the GPIO Port B input data.

Offset: 0x01C

Reset value: 0x0000_0000



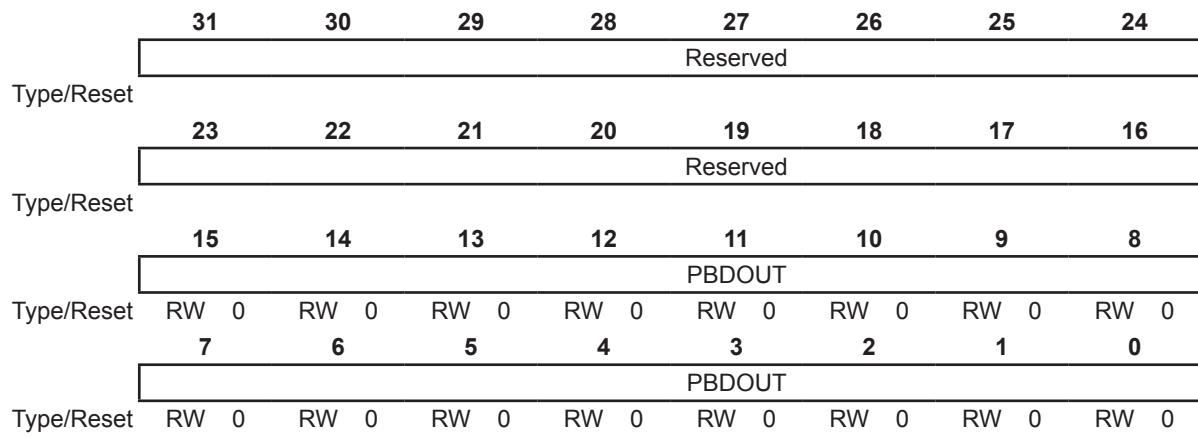
Bits	Field	Descriptions
[15:0]	PBDINn	GPIO Port B pin n Data Input Bits (n = 0 ~ 15) 0: The input data of corresponding pin is 0 1: The input data of corresponding pin is 1

Port B Output Data Register – PBDOUTR

This register specifies the GPIO Port B output data.

Offset: 0x020

Reset value: 0x0000_0000



Bits	Field	Descriptions
[15:0]	PBDOUTn	GPIO Port B pin n Data Output Bits (n = 0 ~ 15) 0: Data to be output on pin n is 0 1: Data to be output on pin n is 1

Port B Output Set/Reset Control Register – PBSRR

This register is used to set or reset the corresponding bit of the GPIO Port B output data.

Offset: 0x024

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
PBRST								
Type/Reset	WO 0							
23 22 21 20 19 18 17 16								
PBRST								
Type/Reset	WO 0							
15 14 13 12 11 10 9 8								
PBSET								
Type/Reset	WO 0							
7 6 5 4 3 2 1 0								
PBSET								
Type/Reset	WO 0							

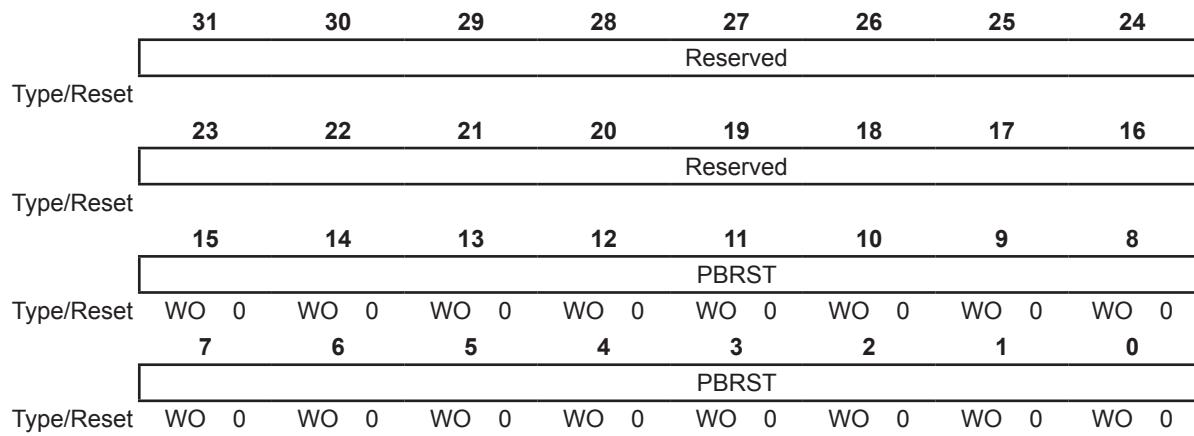
Bits	Field	Descriptions
[31:16]	PBRSTn	GPIO Port B pin n Output Reset Control Bits (n = 0 ~ 15) 0: No effect on the PBDOUTn bit 1: Reset the PBDOUTn bit
[15:0]	PBSETn	GPIO Port B pin n Output Set Control Bits (n = 0 ~ 15) 0: No effect on the PBDOUTn bit 1: Set the PBDOUTn bit Note that the function enabled by the PBSETn bit has the higher priority if both the PBRSTn and PBSETn bits are set at the same time.

Port B Output Reset Register – PBRR

This register is used to reset the corresponding bit of the GPIO Port B output data.

Offset: 0x028

Reset value: 0x0000_0000



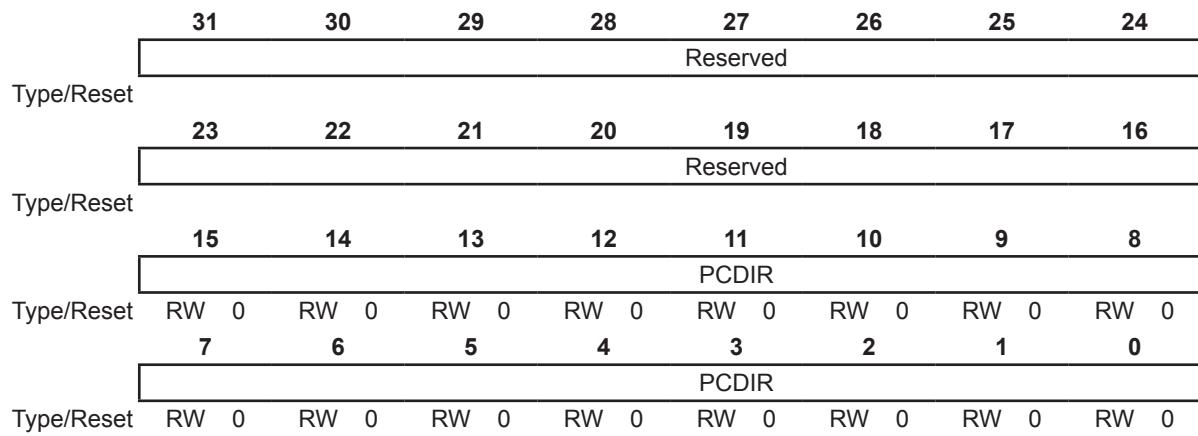
Bits	Field	Descriptions
[15:0]	PBRSTn	GPIO Port B pin n Output Reset Bits (n = 0 ~ 15) 0: No effect on the PBDOUTn bit 1: Reset the PBDOUTn bit

Port C Data Direction Control Register – PCDIRCR

This register is used to control the direction of GPIO Port C pin as input or output.

Offset: 0x000

Reset value: 0x0000_0000



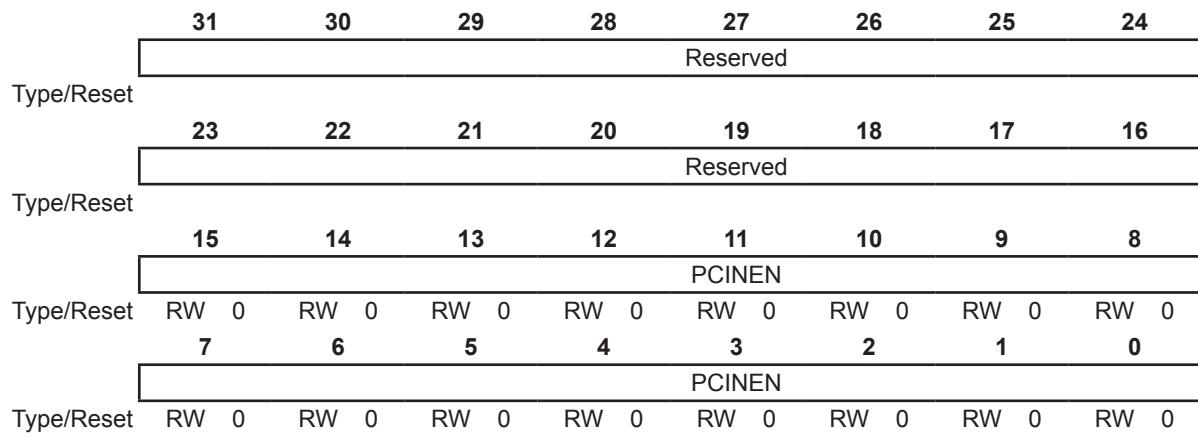
Bits	Field	Descriptions
[15:0]	PCDIRn	GPIO Port C pin n Direction Control Bits (n = 0 ~ 15) 0: Pin n is input mode 1: Pin n is output mode

Port C Input Function Enable Control Register – PCINER

This register is used to enable or disable the GPIO Port C input function.

Offset: 0x004

Reset value: 0x0000_0000



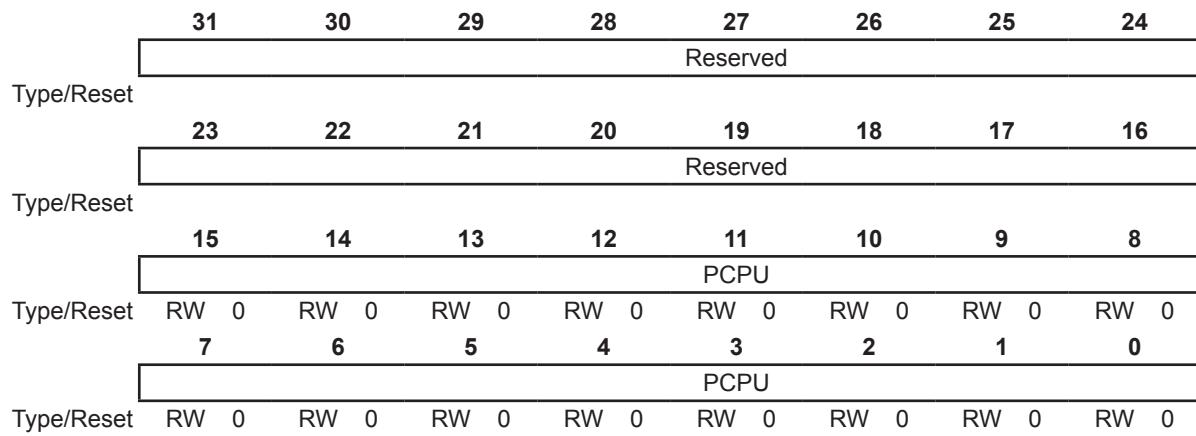
Bits	Field	Descriptions
[15:0]	PCINENn	<p>GPIO Port C pin n Input Enable Control Bits (n = 0 ~ 15)</p> <p>0: Pin n input function is disabled. 1: Pin n input function is enabled.</p> <p>When the pin n input function is disabled, the input Schmitt trigger will be turned off and the Schmitt trigger output will remain at a zero state.</p>

Port C Pull-Up Selection Register – PCPUR

This register is used to enable or disable the GPIO Port C pull-up function.

Offset: 0x008

Reset value: 0x0000_0000



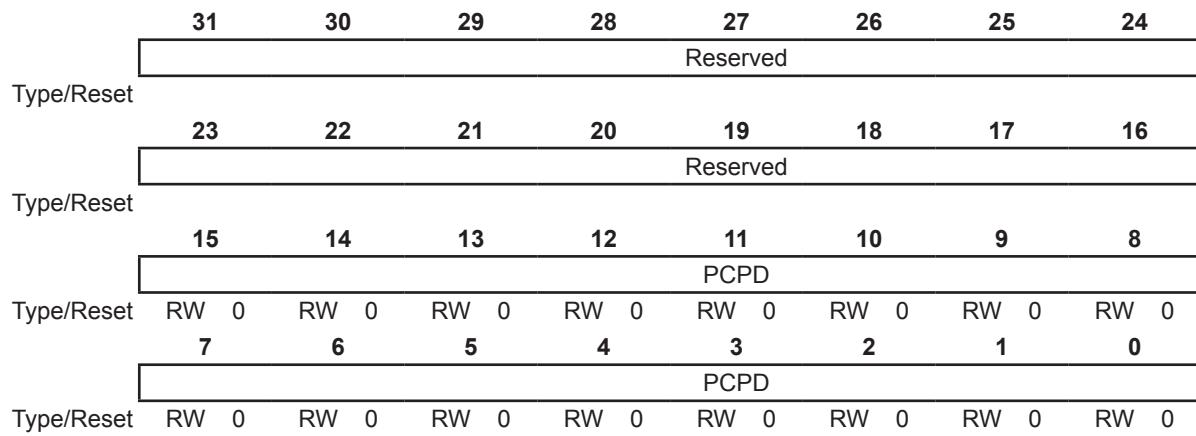
Bits	Field	Descriptions
[15:0]	PCPUn	<p>GPIO Port C pin n Pull-Up Selection Control Bits (n = 0 ~ 15)</p> <p>0: Pin n pull-up function is disabled 1: Pin n pull-up function is enabled</p> <p>Note: When the pull-up and pull-down functions are both enabled, the pull-up function will have the higher priority and therefore the pull-down function will be blocked and disabled.</p>

Port C Pull-Down Selection Register – PCPDR

This register is used to enable or disable the GPIO Port C pull-down function.

Offset: 0x00C

Reset value: 0x0000_0000



Bits	Field	Descriptions
[15:0]	PCPDn	<p>GPIO Port C pin n Pull-Down Selection Control Bits (n = 0 ~ 15)</p> <p>0: Pin n pull-down function is disabled 1: Pin n pull-down function is enabled</p> <p>Note: When the pull-up and pull-down functions are both enabled, the pull-up function will have the higher priority and therefore the pull-down function will be blocked and disabled.</p>

Port C Open Drain Selection Register – PCODR

This register is used to enable or disable the GPIO Port C open drain function.

Offset: 0x010

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Reserved								
Type/Reset	23	22	21	20	19	18	17	16
Reserved								
Type/Reset	15	14	13	12	11	10	9	8
PCOD								
Type/Reset	RW	0	RW	0	RW	0	RW	0
	7	6	5	4	3	2	1	0
Type/Reset	RW	0	RW	0	RW	0	RW	0

Bits	Field	Descriptions
[15:0]	PCODn	GPIO Port C pin n Open Drain Selection Control Bits (n = 0 ~ 15) 0: Pin n Open Drain output is disabled. (The output type is CMOS output) 1: Pin n Open Drain output is enabled. (The output type is open-drain output)

Port C Output Current Drive Selection Register – PCDRVR

This register specifies the GPIO Port C output driving current.

Offset: 0x014

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Reserved								
Type/Reset	23	22	21	20	19	18	17	16
Reserved								
Type/Reset	15	14	13	12	11	10	9	8
Reserved				PCDV				Reserved
Type/Reset				RW	0	RW	0	RW
	7	6	5	4	3	2	1	0
Type/Reset	Reserved							

Bits	Field	Descriptions
[12:9]	PCDVn	GPIO Port C pin n Output Current Drive Selection Control Bits (n = 9 ~ 12) 0: 4mA source/sink current 1: 8mA source/sink current

Port C Lock Register – PCLOCKR

This register specifies the GPIO Port C lock configuration.

Offset: 0x018

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
PCLKEY								
Type/Reset	RW 0							
23 22 21 20 19 18 17 16								
PCLKEY								
Type/Reset	RW 0							
15 14 13 12 11 10 9 8								
PCLOCK								
Type/Reset	RW 0							
7 6 5 4 3 2 1 0								
PCLOCK								
Type/Reset	RW 0							

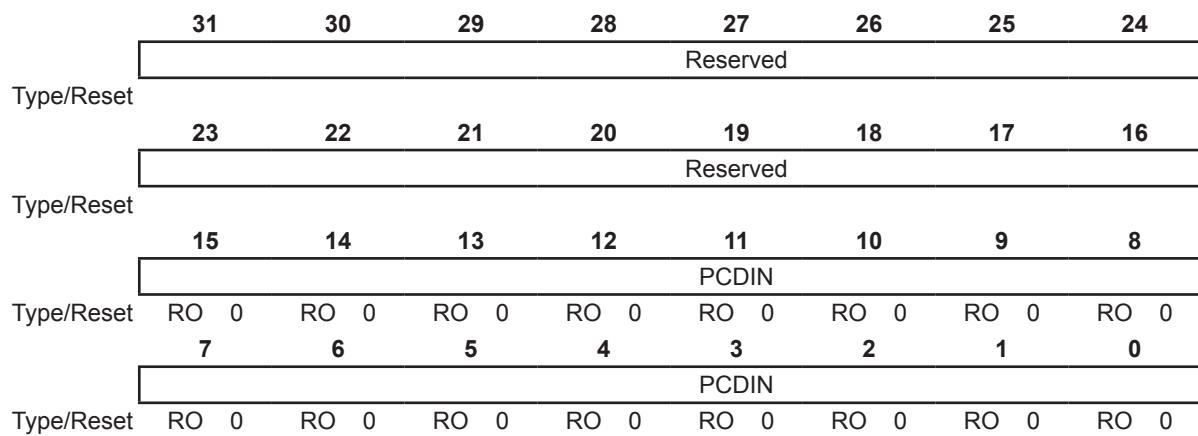
Bits	Field	Descriptions
[31:16]	PCLKEY	<p>GPIO Port C lock Key</p> <p>0x5FA0: Port C Lock function is enable</p> <p>Others: Port C Lock function is disable</p> <p>To lock the Port C function, a value 0x5FA0 should be written into the PCLKEY field in this register. To execute a successful write operation on this lock register, the value written into the PCLKEY field must be 0x5FA0. If the value written into this field is not equal to 0x5FA0, any write operations on the PCLOCKR register will be aborted. The result of a read operation on the PCLKEY field returns the GPIO Port C Lock Status which indicates whether the GPIO Port C is locked or not. If the read value of the PCLKEY field is 0, this indicates that the GPIO Port C Lock function is disabled. Otherwise, it indicates that the GPIO Port C Lock function is enabled as the read value is equal to 1.</p>
[15:0]	PCLOCKn	<p>GPIO Port C pin n Lock Control Bits (n = 0 ~ 15)</p> <p>0: Port C pin n is not locked</p> <p>1: Port C pin n is locked</p> <p>The PCLOCKn bits are used to lock the configurations of corresponding GPIO Pins when the correct Lock Key is applied to the PCLKEY field. The locked configurations including PCDIRn, PCINENn, PCPUn, PCPDn and PCODn setting in the related GPIO registers. Additionally, the GPCCFGHR or GPCCFGLR field which is used to configure the alternative function of the associated GPIO pin will also be locked. Note that the PCLOCKR can only be written once which means that PCLKEY and PCLOCKn (lock control bit) should be written together and can not be changed until a system reset or GPIO Port C reset occurs.</p>

Port C Data Input Register – PCDINR

This register specifies the GPIO Port C input data.

Offset: 0x01C

Reset value: 0x0000_0000



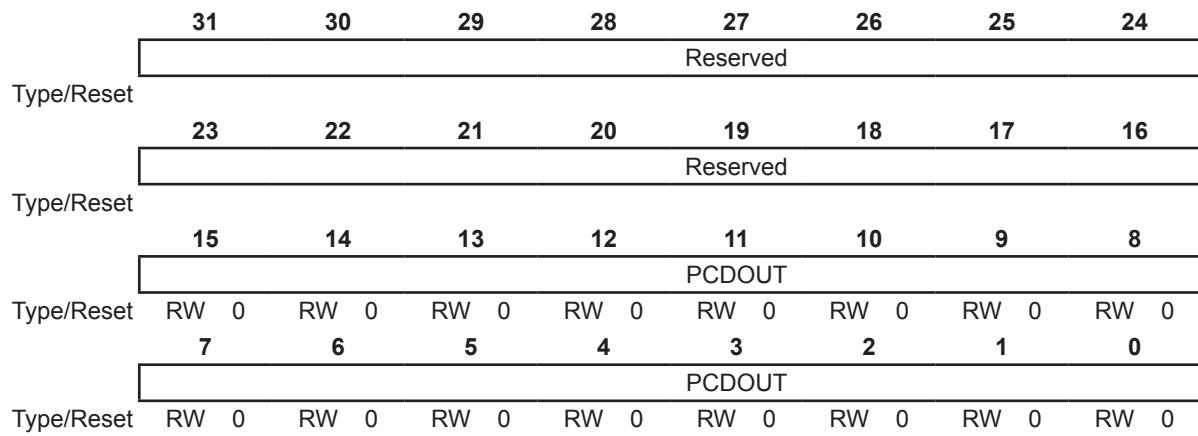
Bits	Field	Descriptions
[15:0]	PCDINn	GPIO Port C pin n Data Input Bits (n = 0 ~ 15) 0: The input data of corresponding pin is 0 1: The input data of corresponding pin is 1

Port C Output Data Register – PCDOUTR

This register specifies the GPIO Port C output data.

Offset: 0x020

Reset value: 0x0000_0000



Bits	Field	Descriptions
[15:0]	PCDOUTn	GPIO Port C pin n Data Output Bits (n = 0 ~ 15) 0: Data to be output on pin n is 0 1: Data to be output on pin n is 1

Port C Output Set/Reset Control Register – PCSRR

This register is used to set or reset the corresponding bit of the GPIO Port C output data.

Offset: 0x024

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
PCRST								
Type/Reset	WO 0							
23 22 21 20 19 18 17 16								
PCRST								
Type/Reset	WO 0							
15 14 13 12 11 10 9 8								
PCSET								
Type/Reset	WO 0							
7 6 5 4 3 2 1 0								
PCSET								
Type/Reset	WO 0							

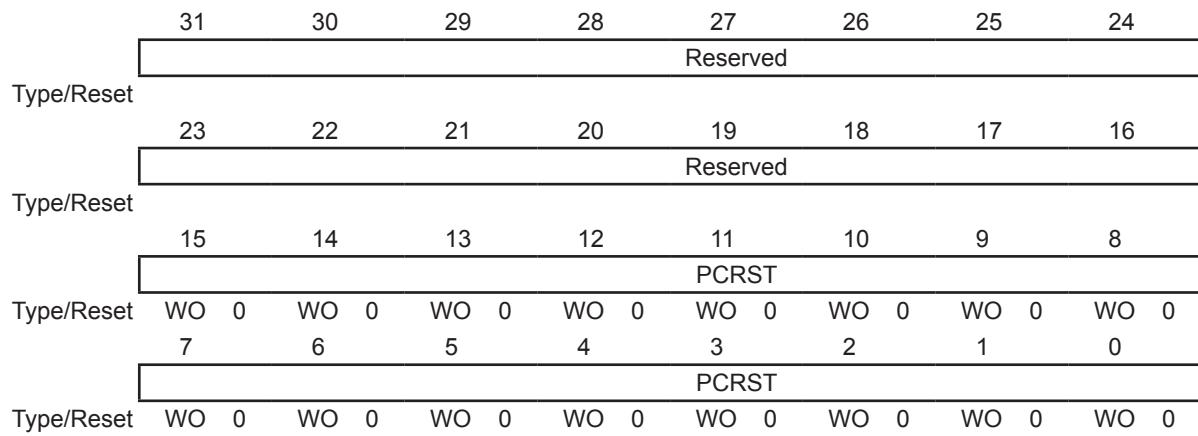
Bits	Field	Descriptions
[31:16]	PCRSTn	GPIO Port C pin n Output Reset Control Bits (n = 0 ~ 15) 0: No effect on the PCDOUTn bit 1: Reset the PCDOUTn bit
[15:0]	PCSETn	GPIO Port C pin n Output Set Control Bits (n = 0 ~ 15) 0: No effect on the PCDOUTn bit 1: Set the PCDOUTn bit Note that the function enabled by the PCSETn bit has the higher priority if both the PCSETn and PCRSTn bits are set at the same time.

Port C Output Reset Register – PCRR

This register is used to reset the corresponding bit of the GPIO Port C output data.

Offset: 0x028

Reset value: 0x0000_0000



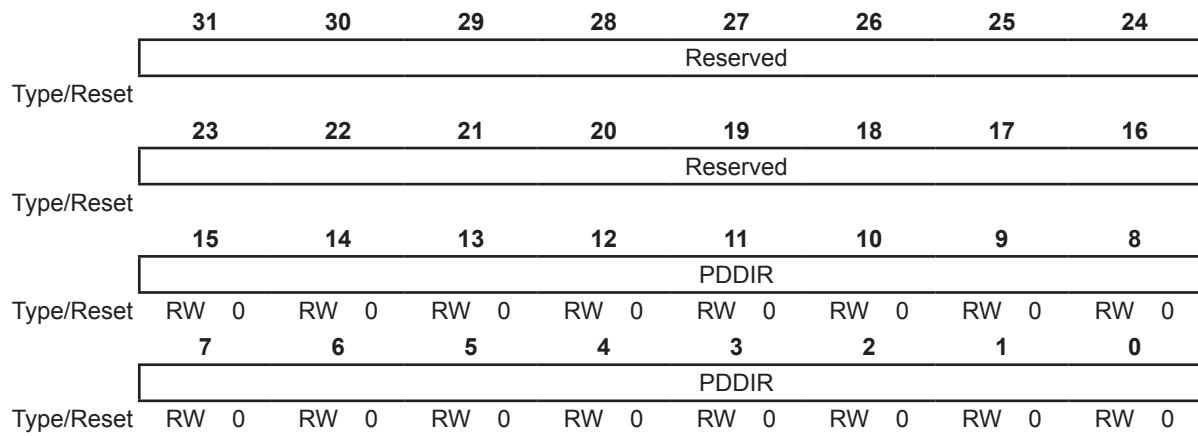
Bits	Field	Descriptions
[15:0]	PCRSTn	GPIO Port C pin n Output Reset Bits (n = 0 ~ 15) 0: No effect on the PCDOUTn bit 1: Reset the PCDOUTn bit

Port D Data Direction Control Register – PDDIRCR

This register is used to control the direction of GPIO Port D pin as input or output.

Offset: 0x000

Reset value: 0x0000_0000



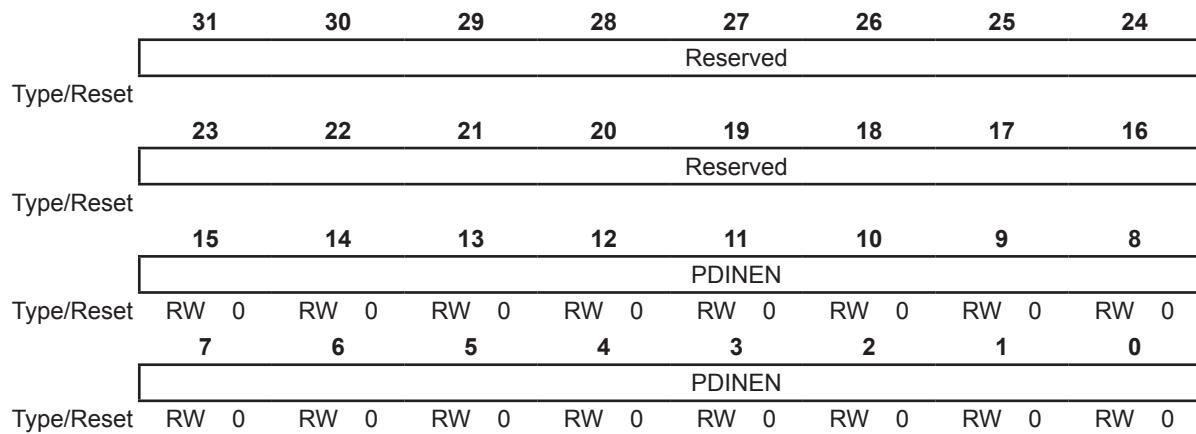
Bits	Field	Descriptions
[15:0]	PDDIRn	GPIO Port D pin n Direction Control Bits (n = 0 ~ 15) 0: Pin n is input mode 1: Pin n is output mode

Port D Input Function Enable Control Register – PDINER

This register is used to enable or disable the GPIO Port D input function.

Offset: 0x004

Reset value: 0x0000_0000



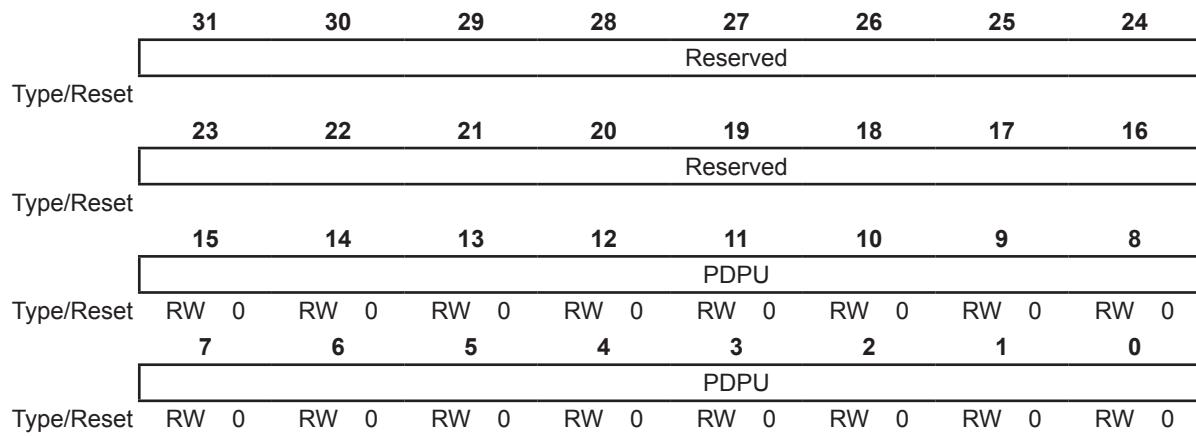
Bits	Field	Descriptions
[15:0]	PDINENn	<p>GPIO Port D pin n Input Enable Control Bits (n = 0 ~ 15)</p> <p>0: Pin n input function is disabled. 1: Pin n input function is enabled.</p> <p>When the pin n input function is disabled, the input Schmitt trigger will be turned off and the Schmitt trigger output will remain at a zero state.</p>

Port D Pull-Up Selection Register – PDPUR

This register is used to enable or disable the GPIO Port D pull-up function.

Offset: 0x008

Reset value: 0x0000_0000



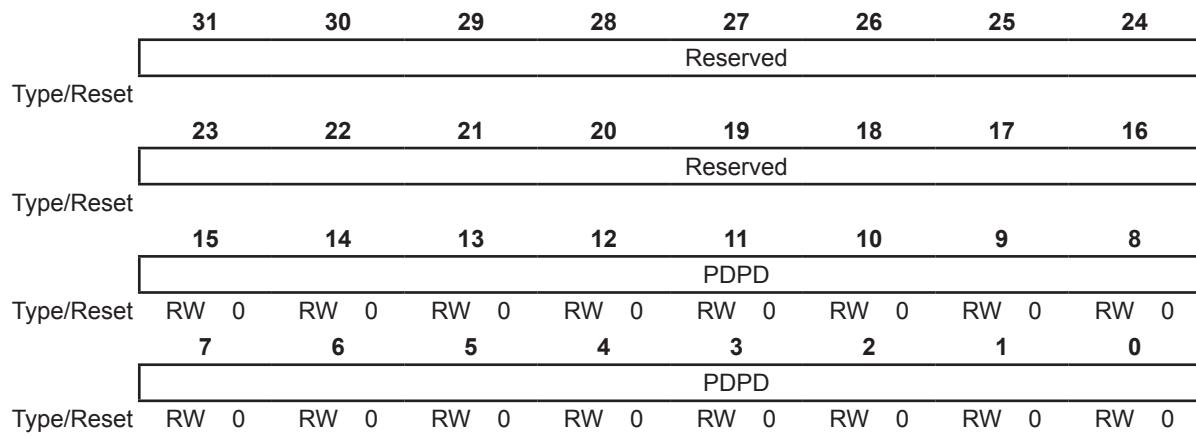
Bits	Field	Descriptions
[15:0]	PDPUn	<p>GPIO Port D pin n Pull-Up Selection Control Bits (n = 0 ~ 15)</p> <p>0: Pin n pull-up function is disabled 1: Pin n pull-up function is enabled</p> <p>Note: When the pull-up and pull-down functions are both enabled, the pull-up function will have the higher priority and therefore the pull-down function will be blocked and disabled.</p>

Port D Pull-Down Selection Register – PDPDR

This register is used to enable or disable the GPIO Port D pull-down function.

Offset: 0x00C

Reset value: 0x0000_0000



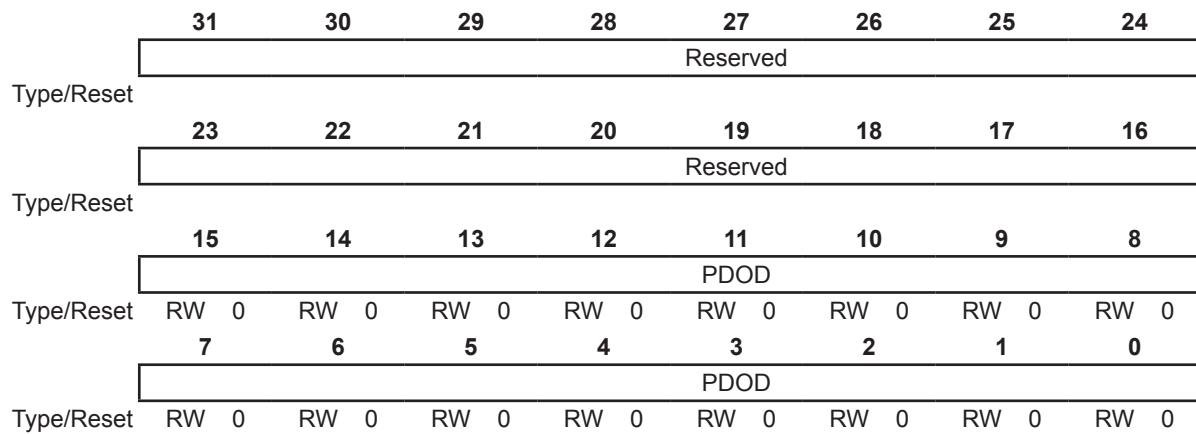
Bits	Field	Descriptions
[15:0]	PDPDn	<p>GPIO Port D pin n Pull-Down Selection Control Bits (n = 0 ~ 15)</p> <p>0: Pin n pull-down function is disabled</p> <p>1: Pin n pull-down function is enabled</p> <p>Note: When the pull-up and pull-down functions are both enabled, the pull-up function will have the higher priority and therefore the pull-down function will be blocked and disabled.</p>

Port D Open Drain Selection Register – PDODR

This register is used to enable or disable the GPIO Port D open drain function.

Offset: 0x010

Reset value: 0x0000_0000



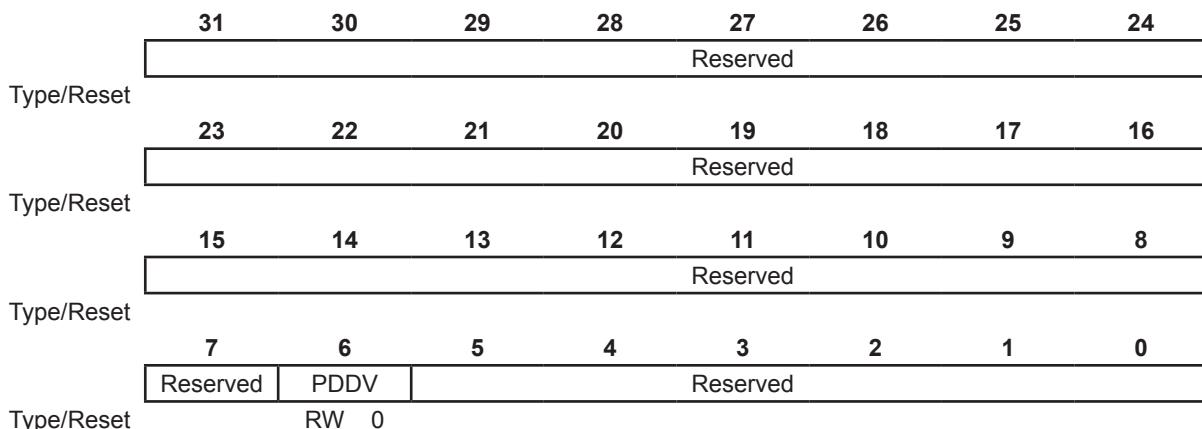
Bits	Field	Descriptions
[15:0]	PDODn	GPIO Port D pin n Open Drain Selection Control Bits (n = 0 ~ 15) 0: Pin n Open Drain output is disabled. (The output type is CMOS output) 1: Pin n Open Drain output is enabled. (The output type is open-drain output)

Port D Output Current Drive Selection Register – PDDRVR

This register specifies the GPIO Port D output driving current.

Offset: 0x014

Reset value: 0x0000_0000



Bits	Field	Descriptions
[6]	PDDVn	GPIO Port D pin n Output Current Drive Selection Control Bits (n = 6) 0: 4mA source/sink current 1: 8mA source/sink current

Port D Lock Register – PDLOCKR

This register specifies the GPIO Port D lock configuration.

Offset: 0x018

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
PDLKEY								
Type/Reset	RW 0							
23 22 21 20 19 18 17 16								
PDLKEY								
Type/Reset	RW 0							
15 14 13 12 11 10 9 8								
PDLOCK								
Type/Reset	RW 0							
7 6 5 4 3 2 1 0								
PDLOCK								
Type/Reset	RW 0							

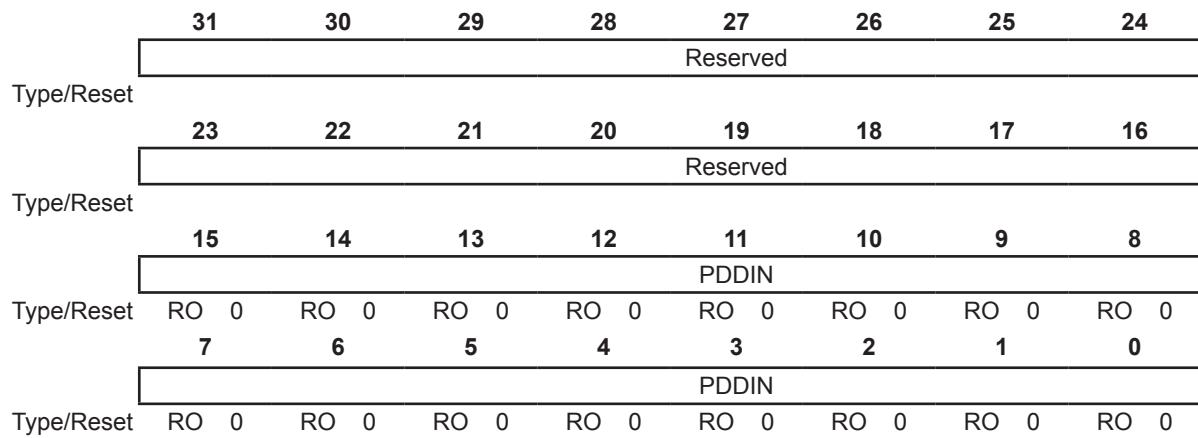
Bits	Field	Descriptions
[31:16]	PDLKEY	<p>GPIO Port D Lock Key</p> <p>0x5FA0: Port D Lock function is enable</p> <p>Others: Port D Lock function is disable</p> <p>To lock the Port D function, a value 0x5FA0 should be written into the PDLKEY field in this register. To execute a successful write operation on this lock register, the value written into the PDLKEY field must be 0x5FA0. If the value written into this field is not equal to 0x5FA0, any write operations on the PDLOCKR register will be aborted. The result of a read operation on the PDLKEY field returns the GPIO Port D Lock Status which indicates whether the GPIO Port D is locked or not. If the read value of the PDLKEY field is 0, this indicates that the GPIO Port D Lock function is disabled. Otherwise, it indicates that the GPIO Port D Lock function is enabled as the read value is equal to 1.</p>
[15:0]	PDLOCKn	<p>GPIO Port D pin n Lock Control Bits (n = 0 ~ 15)</p> <p>0: Port D pin n is not locked</p> <p>1: Port D pin n is locked</p> <p>The PDLOCKn bits are used to lock the configurations of corresponding GPIO Pins when the correct Lock Key is applied to the PDLKEY field. The locked configurations including PDIRn, PDINENn, PDPUn, PDPDn and PDODn setting in the related GPIO registers. Additionally, the GPDCFGHR or GPDCFGLR field which is used to configure the alternative function of the associated GPIO pin will also be locked. Note that the PDLOCKR can only be written once which means that PDLKEY and PDLOCKn (lock control bit) should be written together and can not be changed until a system reset or GPIO Port D reset occurs.</p>

Port D Data Input Register – PDDINR

This register specifies the GPIO Port D input data.

Offset: 0x01C

Reset value: 0x0000_0000



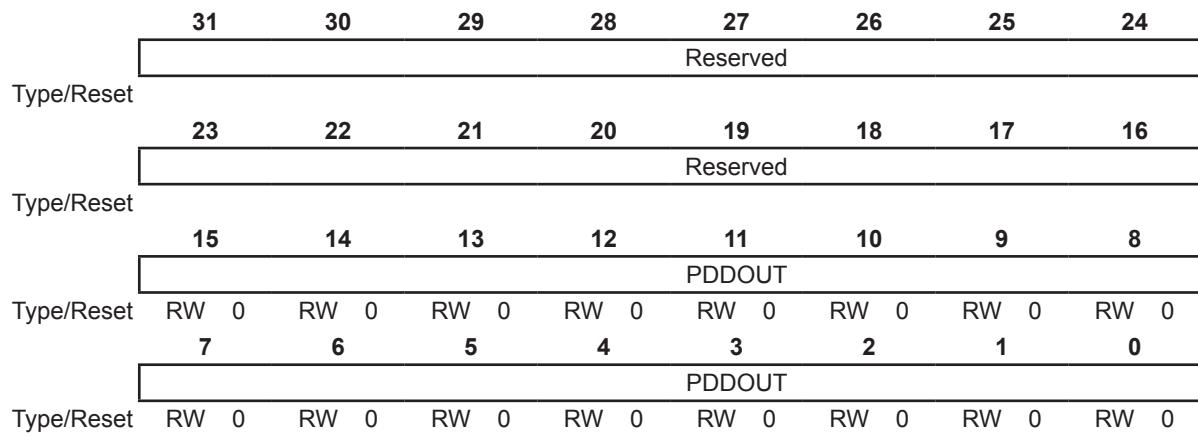
Bits	Field	Descriptions
[15:0]	PDDINn	GPIO Port D pin n Data Input Bits (n = 0 ~ 15) 0: The input data of corresponding pin is 0 1: The input data of corresponding pin is 1

Port D Output Data Register – PDDOUTR

This register specifies the GPIO Port D output data.

Offset: 0x020

Reset value: 0x0000_0000



Bits	Field	Descriptions
[15:0]	PDDOUTn	GPIO Port D pin n Data Output Bits (n = 0 ~ 15) 0: Data to be output on pin n is 0 1: Data to be output on pin n is 1

Port D Output Set/Reset Control Register – PDSRR

This register is used to set or reset the corresponding bit of the GPIO Port D output data.

Offset: 0x024

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
PDRST								
Type/Reset	WO 0							
23 22 21 20 19 18 17 16								
PDRST								
Type/Reset	WO 0							
15 14 13 12 11 10 9 8								
PDSET								
Type/Reset	WO 0							
7 6 5 4 3 2 1 0								
PDSET								
Type/Reset	WO 0							

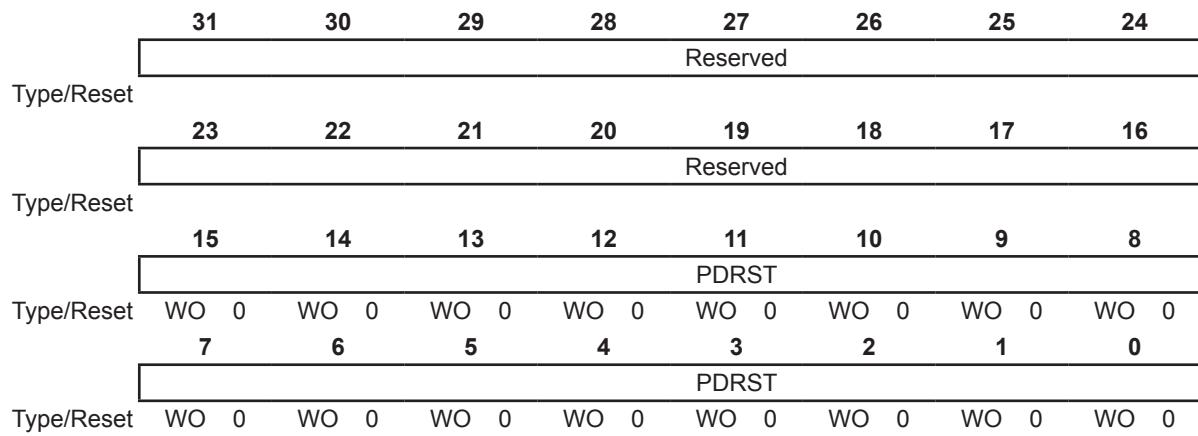
Bits	Field	Descriptions
[31:16]	PDRSTn	GPIO Port D pin n Output Reset Control Bits (n = 0 ~ 15) 0: No effect on the PDDOUTn bit 1: Reset the PDDOUTn bit
[15:0]	PDSETn	GPIO Port D pin n Output Set Control Bits (n = 0 ~ 15) 0: No effect on the PDDOUTn bit 1: Set the PDDOUTn bit Note that the function enabled by the PDSETn bit has the higher priority if both the PDSETn and PDRSTn bits are set at the same time.

Port D Output Reset Register – PDRR

This register is used to reset the corresponding bit of the GPIO Port D output data.

Offset: 0x028

Reset value: 0x0000_0000



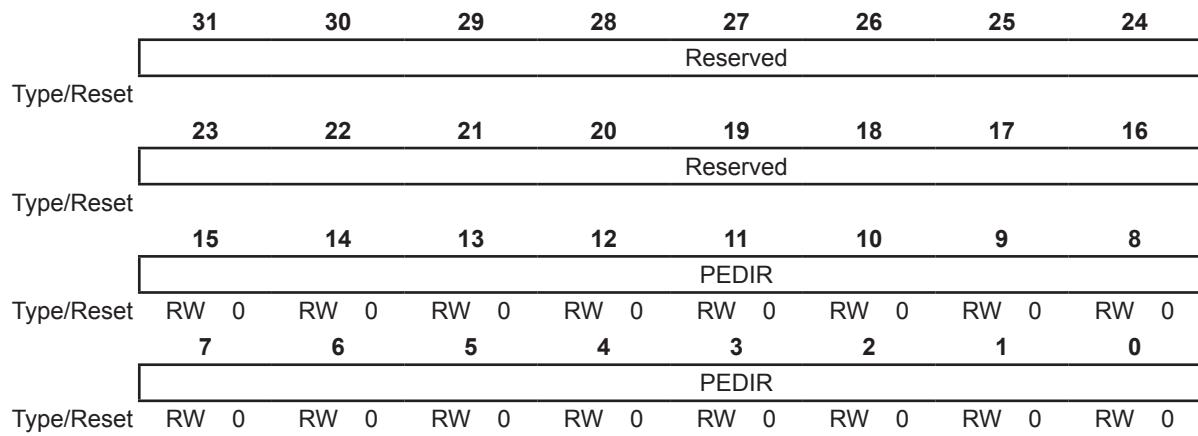
Bits	Field	Descriptions
[15:0]	PDRSTn	GPIO Port D pin n Output Reset Bits (n = 0 ~ 15) 0: No effect on the PDDOUTn bit 1: Reset the PDDOUTn bit

Port E Data Direction Control Register – PEDIRCR

This register is used to control the direction of GPIO Port E pin as input or output.

Offset: 0x000

Reset value: 0x0000_0000



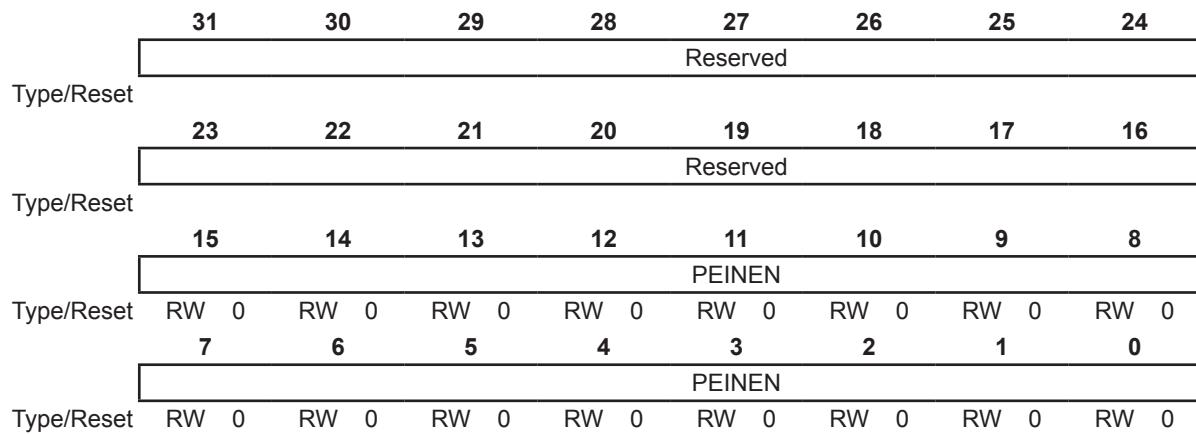
Bits	Field	Descriptions
[15:0]	PEDIRn	GPIO Port E pin n Direction Control Bits (n = 0 ~ 15) 0: Pin n is input mode 1: Pin n is output mode

Port E Input Function Enable Control Register – PEINER

This register is used to enable or disable the GPIO Port E input function.

Offset: 0x004

Reset value: 0x0000_0000



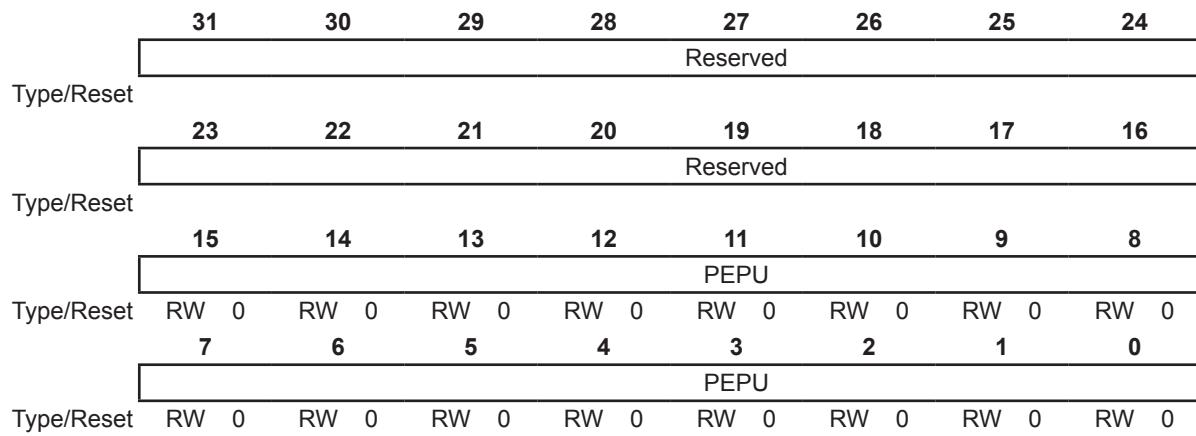
Bits	Field	Descriptions
[15:0]	PEINENn	<p>GPIO Port E pin n Input Enable Control Bits (n = 0 ~ 15)</p> <p>0: Pin n input function is disabled. 1: Pin n input function is enabled.</p> <p>When the pin n input function is disabled, the input Schmitt trigger will be turned off and the Schmitt trigger output will remain at a zero state.</p>

Port E Pull-Up Selection Register – PEPUR

This register is used to enable or disable the GPIO Port E pull-up function.

Offset: 0x008

Reset value: 0x0000_0000



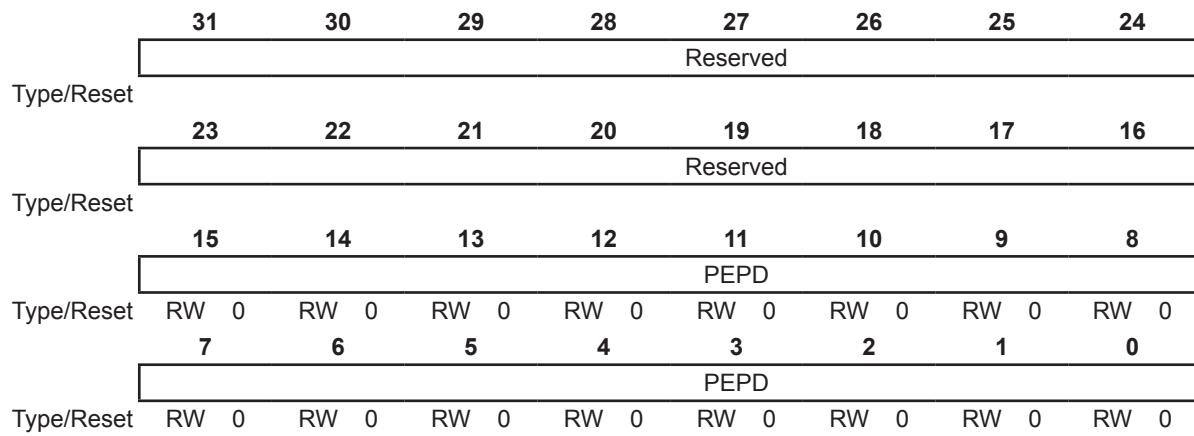
Bits	Field	Descriptions
[15:0]	PEPUn	<p>GPIO Port E pin n Pull-Up Selection Control Bits (n = 0 ~ 15)</p> <p>0: Pin n pull-up function is disabled 1: Pin n pull-up function is enabled</p> <p>Note: When the pull-up and pull-down functions are both enabled, the pull-up function will have the higher priority and therefore the pull-down function will be blocked and disabled.</p>

Port E Pull-Down Selection Register – PEPDR

This register is used to enable or disable the GPIO Port E pull-down function.

Offset: 0x00C

Reset value: 0x0000_0000



Bits	Field	Descriptions
[15:0]	PEPD _n	<p>GPIO Port E pin n Pull-Down Selection Control Bits (n = 0 ~ 15)</p> <p>0: Pin n pull-down function is disabled 1: Pin n pull-down function is enabled</p> <p>Note: When the pull-up and pull-down functions are both enabled, the pull-up function will have the higher priority and therefore the pull-down function will be blocked and disabled.</p>

Port E Open Drain Selection Register – PEODR

This register is used to enable or disable the GPIO Port E open drain function.

Offset: 0x010

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Reserved								
Type/Reset								
Reserved								
Type/Reset								
PEOD								
Type/Reset	RW	0	RW	0	RW	0	RW	0
	7	6	5	4	3	2	1	0
Type/Reset	RW	0	RW	0	RW	0	RW	0

Bits	Field	Descriptions
[15:0]	PEODn	GPIO Port E pin n Open Drain Selection Control Bits (n = 0 ~ 15) 0: Pin n Open Drain output is disabled. (The output type is CMOS output) 1: Pin n Open Drain output is enabled. (The output type is open-drain output)

Port E Output Current Drive Selection Register – PEDRVR

This register specifies the GPIO Port E output driving current.

Offset: 0x014

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Reserved								
Type/Reset								
Reserved								
Type/Reset								
PEDV								
Type/Reset				RW	0	RW	0	RW
	7	6	5	4	3	2	1	0
Type/Reset								

Bits	Field	Descriptions
[10:5]	PEDVn	GPIO Port E pin n Output Current Drive Selection Control Bits (n = 8 ~ 12) 0: 4mA source/sink current 1: 8mA source/sink current

Port E Lock Register – PELOCKR

This register specifies the GPIO Port E lock configuration.

Offset: 0x018

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
PELKEY								
Type/Reset	RW 0							
23 22 21 20 19 18 17 16								
PELKEY								
Type/Reset	RW 0							
15 14 13 12 11 10 9 8								
PELOCK								
Type/Reset	RW 0							
7 6 5 4 3 2 1 0								
PELOCK								
Type/Reset	RW 0							

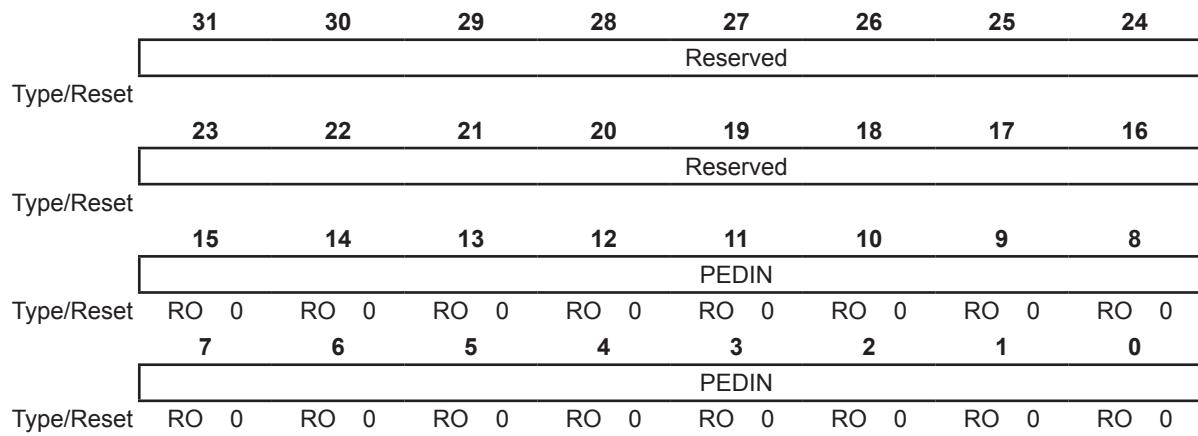
Bits	Field	Descriptions
[31:16]	PELKEY	<p>GPIO Port E Lock Key</p> <p>0x5FA0: Port E Lock function is enable</p> <p>Others: Port E Lock function is disable</p> <p>To lock the Port E function, a value 0x5FA0 should be written into the PELKEY field in this register. To execute a successful write operation on this lock register, the value written into the PELKEY field must be 0x5FA0. If the value written into this field is not equal to 0x5FA0, any write operations on the PELOCKR register will be aborted. The result of a read operation on the PELKEY field returns the GPIO Port E Lock Status which indicates whether the GPIO Port E is locked or not. If the read value of the PELKEY field is 0, this indicates that the GPIO Port E Lock function is disabled. Otherwise, it indicates that the GPIO Port E Lock function is enabled as the read value is equal to 1.</p>
[15:0]	PELOCKn	<p>GPIO Port E pin n Lock Control Bits (n = 0 ~ 15)</p> <p>0: Port E pin n is not locked</p> <p>1: Port E pin n is locked</p> <p>The PELOCKn bits are used to lock the configurations of corresponding GPIO Pins when the correct Lock Key is applied to the PELKEY field. The locked configurations including PEDIRn, PEINENn, PEPUN, PEPDn, PEODn and PEDVn setting in the related GPIO registers. Additionally, the GPECFGHR or GPECFGLR field which is used to configure the alternative function of the associated GPIO pin will also be locked. Note that the PELOCKR can only be written once which means that PELKEY and PELOCKn (lock control bit) should be written together and can not be changed until a system reset or GPIO Port E reset occurs.</p>

Port E Data Input Register – PEDINR

This register specifies the GPIO Port E input data.

Offset: 0x01C

Reset value: 0x0000_0000



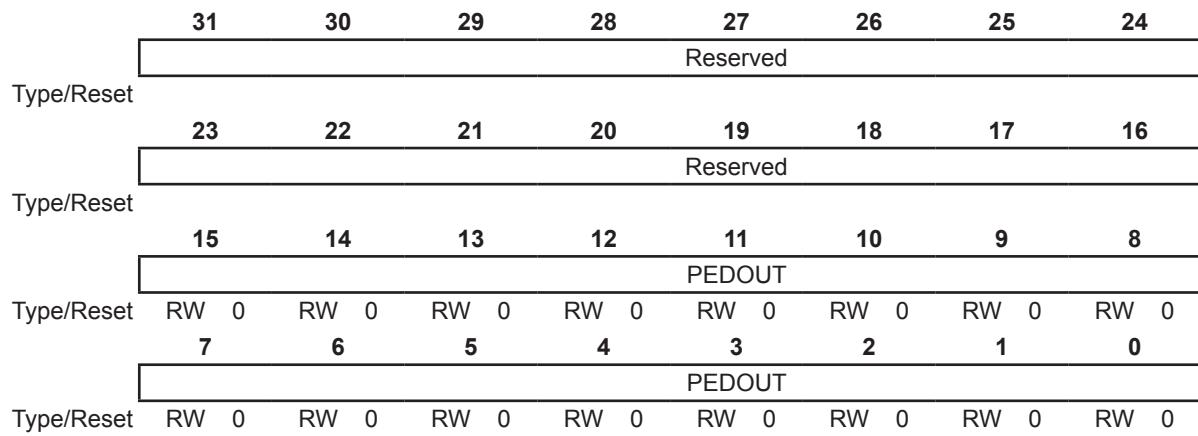
Bits	Field	Descriptions
[15:0]	PEDINn	GPIO Port E pin n Data Input Bits (n = 0 ~ 15) 0: The input data of corresponding pin is 0 1: The input data of corresponding pin is 1

Port E Output Data Register – PEDOUTR

This register specifies the GPIO Port E input data.

Offset: 0x020

Reset value: 0x0000_0000



Bits	Field	Descriptions
[15:0]	PEDOUTn	GPIO Port E pin n Data Output Bits (n = 0 ~ 15) 0: Data to be output on pin n is 0 1: Data to be output on pin n is 1

Port E Output Set/Reset Control Register – PESRR

This register is used to set or reset the corresponding bit of the GPIO Port E output data.

Offset: 0x024

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
PERST								
Type/Reset	WO 0							
23 22 21 20 19 18 17 16								
PERST								
Type/Reset	WO 0							
15 14 13 12 11 10 9 8								
PESET								
Type/Reset	WO 0							
7 6 5 4 3 2 1 0								
PESET								
Type/Reset	WO 0							

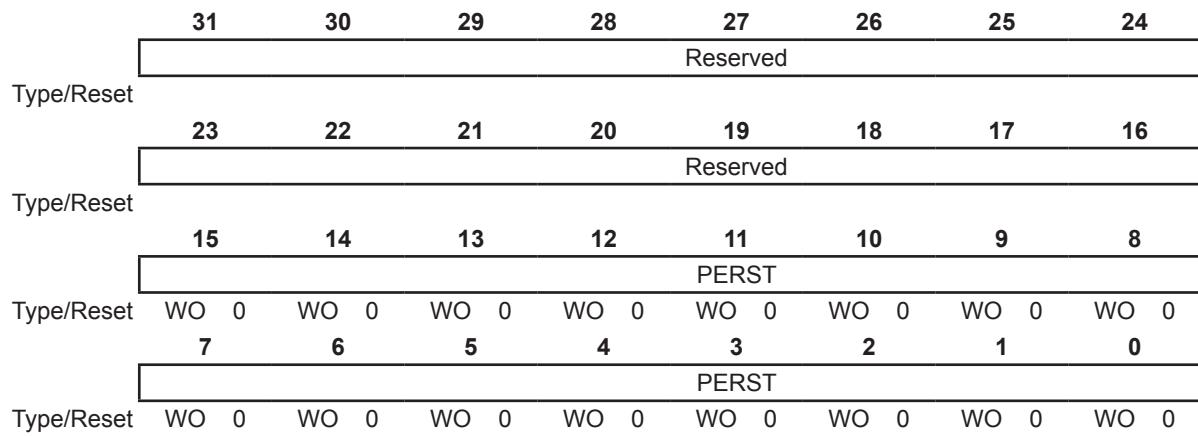
Bits	Field	Descriptions
[31:16]	PERSTn	GPIO Port E pin n Output Reset Control Bits (n = 0 ~ 15) 0: No effect on the PEDOUTn bit 1: Reset the PEDOUTn bit
[15:0]	PESETn	GPIO Port E pin n Output Set Control Bits (n = 0 ~ 15) 0: No effect on the PEDOUTn bit 1: Set the PEDOUTn bit Note that the function enabled by the PESETn bit has the higher priority if both the PESETn and PERSTn bits are set at the same time.

Port E Output Reset Register – PERR

This register is used to reset the corresponding bit of the GPIO Port E output data.

Offset: 0x028

Reset value: 0x0000_0000



Bits	Field	Descriptions
[15:0]	PERSTn	GPIO Port E pin n Output Reset Bits (n = 0 ~ 15) 0: No effect on the PEDOUTn bit 1: Reset the PEDOUTn bit

9

Alternate Function Input/Output Control Unit (AFIO)

Introduction

In order to expand the flexibility of the GPIO or the usage of peripheral functions, each IO pin can be configured to have up to sixteen different functions such as GPIO or IP functions by setting the GPxCFGRL or GPxCFGHR register where x is the different port name. According to the usage of the IP resource and application requirements, suitable pin-out locations can be selected by using the peripheral IO remapping mechanism. Additionally, various GPIO pins can be selected to be the EXTI interrupt line by setting the EXTInPIN [3:0] field in the ESSRn register to trigger an interrupt or event. Please refer to the EXTI section for more details.

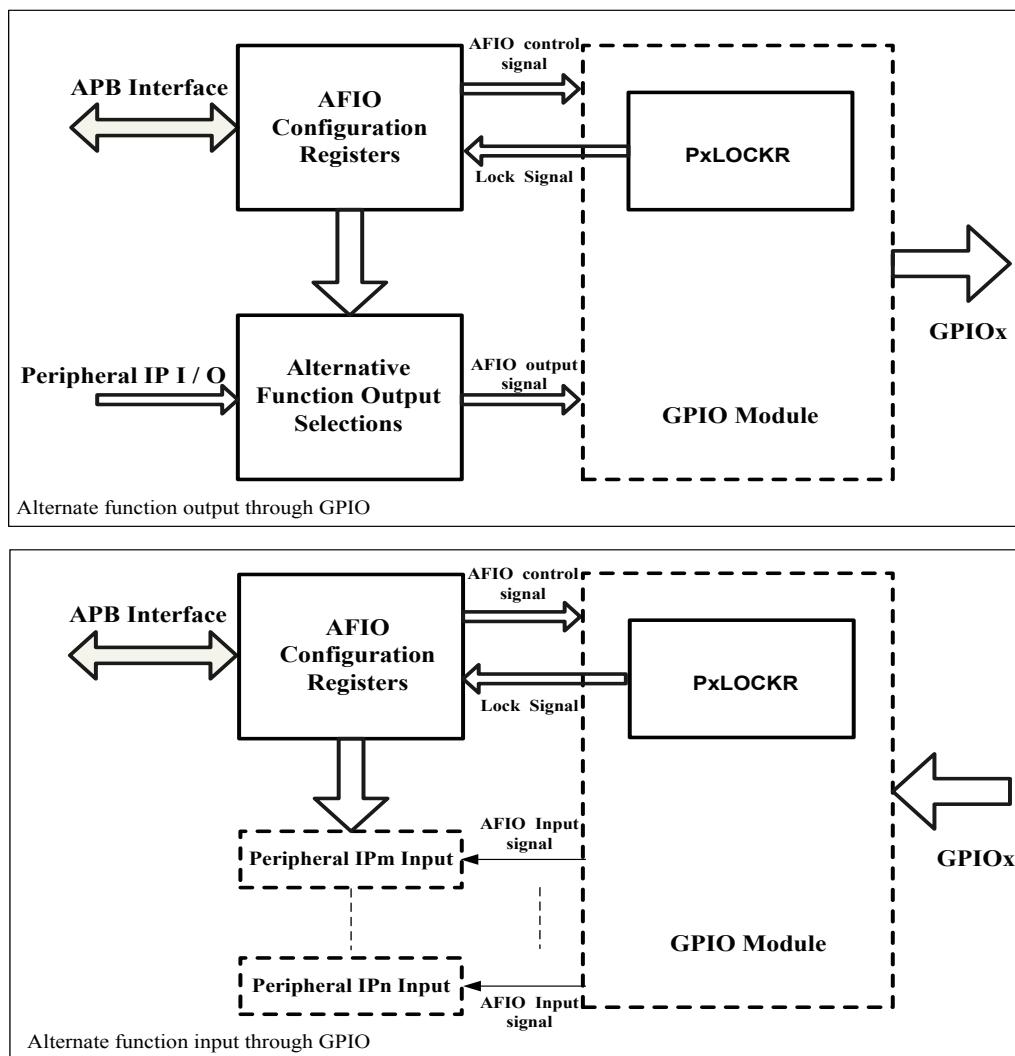


Figure 20. AFIO Block Diagram

Features

- APB slave interface for register access
- EXTI source selection
- Configurable pin function for each GPIO, up to four alternative functions on each pin
- AFIO lock mechanism

Functional Descriptions

External Interrupt Pin Selection

The GPIO pins are connected to the 16 EXTI lines as shown in the accompanying figure. For example, the user can set the EXTI0PIN [3:0] field in the ESSR0 register to b0000 to select the GPIO PA0 pin as EXTI line 0 input. Since not all the pins of the Port A ~ E pins are available in all package types, please refer to the pin assignment section for detailed pin information. The setting of the EXTInPIN [3:0] field is invalid when the corresponding pin is not available.

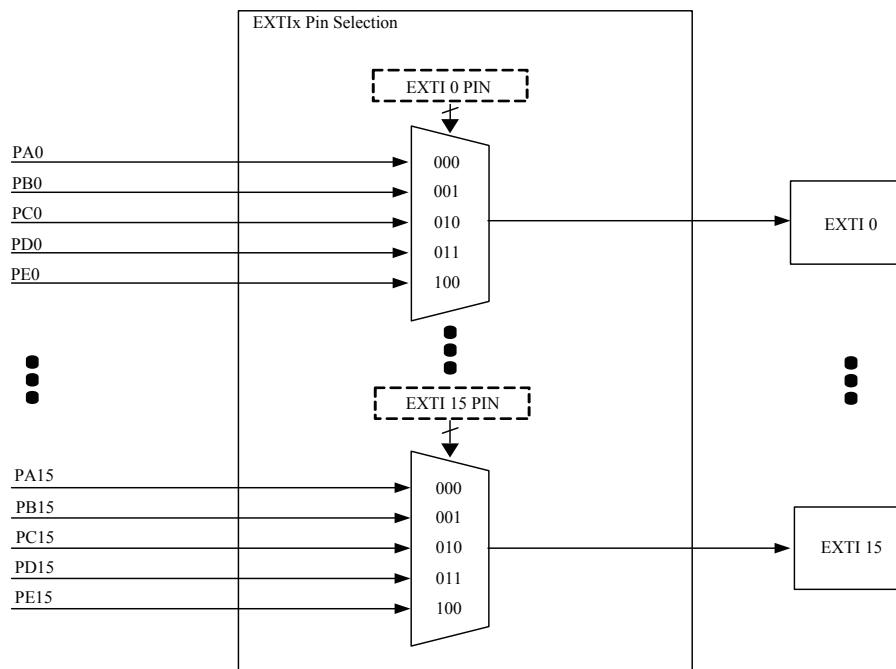


Figure 21. EXTI Channel Input Selection

Alternate Function

Up to sixteen alternative functions can be chosen for each I/O pad by setting the PxCFGn [3:0] field in the GPxCFGCLR or GPxCFGHHR (n = 0~15, x = A~E) registers. Refer to the “Alternate function mapping” table in the device datasheet for the detailed mapping of the alternate function I/O pins. In addition to this flexible I/O multiplexing architecture, each peripheral has alternate functions mapped onto different I/O pins to optimize the number of peripherals available in smaller packages. The following description shows the setting of the PxCFGn [3:0] field. Note that if the Operational Amplifier/Comparator is active, then pins PB [8:6] or PB [11:9] can not be set as other AFIO functional pins simultaneously.

- PxCFGn [3:0] = 0000: The default alternated function (after reset, AF0)
- PxCFGn [3:0] = 0001: Alternate Function 1 (AF1)
- PxCFGn [3:0] = 0010: Alternate Function 2 (AF2)
-
- PxCFGn [3:0] = 1110: Alternate Function 14 (AF14)
- PxCFGn [3:0] = 1111: Alternate Function 15 (AF15)

Table 22. AFIO Selection for Peripheral Map

AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
System Default	GPIO	ADC	CMP	MCTM /GPTM	SPI	USART /UART	I ² C	SCI	EBI	I ² S	N/A	N/A	N/A	N/A	System Other

Lock Mechanism

The GPIO PxLOCKR (i.e. x = A ~E) also offer lock key 0x5FA0 to lock AFIO input and output status until Reset.

Register Map

The following table shows the AFIO registers and reset value.

Table 23. AFIO Register Map

Register	Offset	Description	Reset Value
AFIO Base Address = 0x4002_2000			
ESSR0	0x000	EXTI Source Selection Register 0	0x0000_0000
ESSR1	0x004	EXTI Source Selection Register 1	0x0000_0000
GPACFGLR	0x020	GPIO Port A Configuration Register 0	0x0000_0000
GPACFGHR	0x024	GPIO Port A Configuration Register 1	0x0000_0000
GPBCFGLR	0x028	GPIO Port B Configuration Register 0	0x0000_0000
GPBCFGHR	0x02C	GPIO Port B Configuration Register 1	0x0000_0000
GPCCFGLR	0x030	GPIO Port C Configuration Register 0	0x0000_0000
GPCCFGHR	0x034	GPIO Port C Configuration Register 1	0x0000_0000
GPDCFGLR	0x038	GPIO Port D Configuration Register 0	0x0000_0000
GPDCFGHR	0x03C	GPIO Port D Configuration Register 1	0x0000_0000
GPECFGLR	0x040	GPIO Port E Configuration Register 0	0x0000_0000
GPECFGHR	0x044	GPIO Port E Configuration Register 1	0x0000_0000

Register Descriptions

EXTI Source Selection Register 0 – ESSR0

This register specifies the IO selection of EXTI0 ~ EXTI7.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Type/Reset	RW 0							
	23	22	21	20	19	18	17	16
Type/Reset	RW 0							
	15	14	13	12	11	10	9	8
Type/Reset	RW 0							
	7	6	5	4	3	2	1	0
Type/Reset	RW 0							

Bits	Field	Descriptions
[31:0]	EXTInPIN[3:0]	<p>EXTIn Pin Selection (n = 0 ~ 7)</p> <p>0000: PA Bit n is selected as EXTIn source signal 0001: PB Bit n is selected as EXTIn source signal 0010: PC Bit n is selected as EXTIn source signal 0011: PD Bit n is selected as EXTIn source signal 0100: PE Bit n is selected as EXTIn source signal Others: Reserved</p> <p>Note: Since not all GPIO pins are available in all products and package types, refer to the pin assignment section for detailed pin information. The EXTInPIN [3:0] field setting is invalid when the corresponding pin is not available.</p>

EXTI Source Selection Register 1 – ESSR1

This register specifies the IO selection of EXTI8~EXTI15.

Offset: 0x004

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Type/Reset	RW	0	RW	0	RW	0	RW	0
	23	22	21	20	19	18	17	16
	EXTI15PIN							
Type/Reset	RW	0	RW	0	RW	0	RW	0
	15	14	13	12	11	10	9	8
	EXTI13PIN							
Type/Reset	RW	0	RW	0	RW	0	RW	0
	7	6	5	4	3	2	1	0
	EXTI11PIN							
Type/Reset	RW	0	RW	0	RW	0	RW	0
	EXTI9PIN							
	EXTI8PIN							
	RW	0	RW	0	RW	0	RW	0

Bits	Field	Descriptions
[31:0]	EXTInPIN[3:0]	EXTIn Pin Selection (n = 8 ~ 15) 0000: PA Bit n is selected as EXTIn source signal 0001: PB Bit n is selected as EXTIn source signal 0010: PC Bit n is selected as EXTIn source signal 0011: PD Bit n is selected as EXTIn source signal 0100: PE Bit n is selected as EXTIn source signal Others: Reserved Note: Since not all GPIO pins are available in all products and package types, refer to the pin assignment section for detailed pin information. The EXTInPIN [3:0] field setting is invalid when the corresponding pin is not available.

GPIO x Configuration Low Register – GPxCFGLR, x = A, B, C, D, E

This low register specifies the alternate function of GPIO Port x. x = A, B, C, D, E

Offset: 0x020, 0x028, 0x030, 0x038, 0x040

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	PxCFG7					PxCFG6		
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	PxCFG5					PxCFG4		
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	PxCFG3					PxCFG2		
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PxCFG1					PxCFG0		
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:0]	PxCFGn[3:0]	<p>Alternate function selection for port x pin n (n = 0~7)</p> <p>0000: Port x pin n is selected as AF0.</p> <p>0001: Port x pin n is selected as AF1.</p> <p>1110: Port x pin n is selected as AF14</p> <p>1111: Port x pin n is selected as AF15</p> <p>Please refer to the “Alternate function mapping” table in the device datasheet for the detailed mapping of the alternate function I/O pins.</p>

GPIO x Configuration High Register – GPxCFGHR, x = A, B, C, D, E

This high register specifies the alternate function of GPIO Port x. x = A, B, C, D, E

Offset: 0x024, 0x02C, 0x034, 0x03C, 0x044

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	PxCFG15					PxCFG14		
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	PxCFG13					PxCFG12		
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	PxCFG11					PxCFG10		
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PxCFG9					PxCFG8		
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:0]	PxCFGn[3:0]	<p>Alternate function selection for port x pin n (n = 8~15)</p> <p>0000: Port x pin n is selected as AF0.</p> <p>0001: Port x pin n is selected as AF1.</p> <p>1110: Port x pin n is selected as AF14</p> <p>1111: Port x pin n is selected as AF15</p> <p>Please refer to the “Alternate function mapping” table in the device datasheet for the detailed mapping of the alternate function I/O pins.</p>

10 Nested Vectored Interrupt Controller (NVIC)

Introduction

In order to reduce the latency and increase the interrupt processing efficiency, a tightly coupled integrated section, which is named as Nested Vectored Interrupt Controller (NVIC) is provided by the Cortex™-M3. The NVIC controls the system exceptions and the peripheral interrupt which include functions such as the enable/disable control, priority, clear-pending, active status report, software trigger and vector table remapping. Refer to the Technical Reference Manual of Cortex™-M3 for more details.

Additionally, an integrated simple, 24-bit down count timer (SysTick) is provided by the Cortex™-M3 to be used as a tick timer for the Real Timer Operation System (RTOS) or as a simple counter. The SysTick counts down from the reloaded value and generates a system interrupt when it reached zero.

The accompanying table lists the 16 system exceptions types and a variety of peripheral interrupts.

Table 24. Exception types

Exception type	Priority	Interrupt Number	Exception Number	Vector Address	Description
	—	—	0	0x000	Initial Stack Point value
Reset	-3 (Highest)	—	1	0x004	Reset
NMI	-2	—	2	0x008	Non-Maskable Interrupt. The clock stuck interrupt signal (clock monitor function provided by Clock Control Unit) is connected to the NMI input
Hard Fault	-1	—	3	0x00C	All fault classes
Memory Management	Configurable ^(Note1)	—	4	0x010	Memory Protection Unit (MPU) mismatch, including access violation and no match
Bus Fault	Configurable ⁽¹⁾	—	5	0x014	Pre-fetch fault, memory access fault, and other address/memory related
Usage Fault	Configurable ⁽¹⁾	—	6	0x018	Usage fault, such as undefined executed instruction or illegal attempt of state transition
—	—	—	7	0x01C	Reserved
—	—	—	8	0x020	Reserved
—	—	—	9	0x024	Reserved
—	—	—	10	0x028	Reserved
SVCCall	Configurable ⁽¹⁾	—	11	0x02C	SVC instruction System service call
Debug Monitor	Configurable ⁽¹⁾	—	12	0x030	Debug monitor, when not halted
—	Configurable ⁽¹⁾	—	13	0x034	Reserved
PendSV	Configurable ⁽¹⁾	—	14	0x038	System Service Pendable request
SySTick	Configurable ⁽¹⁾	—	15	0x03C	SysTick timer decremented to zero
CKRDY	Configurable ^(Note 2)	0	16	0x040	Clock ready interrupt (HSE, HSI, LSE, LSI, or PLL)
LVD	Configurable ⁽²⁾	1	17	0x044	Low voltage detection interrupt
BOD	Configurable ⁽²⁾	2	18	0x048	Brown-out detection interrupt

Exception type	Priority	Interrupt Number	Exception Number	Vector Address	Description
WDT	Configurable ⁽²⁾	3	19	0x04C	Watchdog timer global interrupt
RTC	Configurable ⁽²⁾	4	20	0x050	RTC global interrupt
FMC	Configurable ⁽²⁾	5	21	0x054	FMC global interrupt
EVWUP	Configurable ⁽²⁾	6	22	0x058	EXTI event wakeup interrupt
LPWUP	Configurable ⁽²⁾	7	23	0x05C	WAKEUP pin interrupt
EXTI0	Configurable ⁽²⁾	8	24	0x060	EXTI Line 0 interrupt
EXTI1	Configurable ⁽²⁾	9	25	0x064	EXTI Line 1 interrupt
EXTI2	Configurable ⁽²⁾	10	26	0x068	EXTI Line 2 interrupt
EXTI3	Configurable ⁽²⁾	11	27	0x06C	EXTI Line 3 interrupt
EXTI4	Configurable ⁽²⁾	12	28	0x070	EXTI Line 4 interrupt
EXTI5	Configurable ⁽²⁾	13	29	0x074	EXTI Line 5 interrupt
EXTI6	Configurable ⁽²⁾	14	30	0x078	EXTI Line 6 interrupt
EXTI7	Configurable ⁽²⁾	15	31	0x07C	EXTI Line 7 interrupt
EXTI8	Configurable ⁽²⁾	16	32	0x080	EXTI Line 8 interrupt
EXTI9	Configurable ⁽²⁾	17	33	0x084	EXTI Line 9 interrupt
EXTI10	Configurable ⁽²⁾	18	34	0x088	EXTI Line 10 interrupt
EXTI11	Configurable ⁽²⁾	19	35	0x08C	EXTI Line 11 interrupt
EXTI12	Configurable ⁽²⁾	20	36	0x090	EXTI Line 12 interrupt
EXTI13	Configurable ⁽²⁾	21	37	0x094	EXTI Line 13 interrupt
EXTI14	Configurable ⁽²⁾	22	38	0x098	EXTI Line 14 interrupt
EXTI15	Configurable ⁽²⁾	23	39	0x09C	EXTI Line 15 interrupt
COMP	Configurable ⁽²⁾	24	40	0xA0	Comparator global interrupt
ADC	Configurable ⁽²⁾	25	41	0xA4	ADC global interrupt
—	—	26	42	0xA8	Reserved
MCTM0_BRK	Configurable ⁽²⁾	27	43	0xAC	MCTM0 break interrupt
MCTM0_UP	Configurable ⁽²⁾	28	44	0xB0	MCTM0 update interrupt
MCTM0_TR_UP2	Configurable ⁽²⁾	29	45	0xB4	MCTM0 trigger/update event 2 interrupt
MCTM0_CC	Configurable ⁽²⁾	30	46	0xB8	MCTM0 capture/compare interrupt
MCTM1_BRK	Configurable ⁽²⁾	31	47	0xBC	MCTM1 break interrupt
MCTM1_UP	Configurable ⁽²⁾	32	48	0xC0	MCTM1 update interrupt
MCTM1_TR_UP2	Configurable ⁽²⁾	33	49	0xC4	MCTM1 trigger/update event 2 interrupt
MCTM1_CC	Configurable ⁽²⁾	34	50	0xC8	MCTM1 capture/compare interrupt
GPTM0	Configurable ⁽²⁾	35	51	0xCC	GPTM0 global interrupt
GPTM1	Configurable ⁽²⁾	36	52	0xD0	GPTM1 global interrupt
—	—	37	53	0xD4	Reserved
—	—	38	54	0xD8	Reserved
—	—	39	55	0xDC	Reserved
—	—	40	56	0xE0	Reserved
BFTM0	Configurable ⁽²⁾	41	57	0xE4	BFTM0 global interrupt
BFTM1	Configurable ⁽²⁾	42	58	0xE8	BFTM1 global interrupt
I ² C0	Configurable ⁽²⁾	43	59	0xEC	I ² C0 global interrupt
I ² C1	Configurable ⁽²⁾	44	60	0xF0	I ² C1 global interrupt

Exception type	Priority	Interrupt Number	Exception Number	Vector Address	Description
SPI0	Configurable ⁽²⁾	45	61	0x0F4	SPI0 global interrupt
SPI1	Configurable ⁽²⁾	46	62	0x0F8	SPI1 global interrupt
USART0	Configurable ⁽²⁾	47	63	0x0FC	USART0 global interrupt
USART1	Configurable ⁽²⁾	48	64	0x100	USART1 global interrupt
UART0	Configurable ⁽²⁾	49	65	0x104	UART0 global interrupt
UART1	Configurable ⁽²⁾	50	66	0x108	UART1 global interrupt
SCI	Configurable ⁽²⁾	51	67	0x10C	SCI global interrupt
I ² S	Configurable ⁽²⁾	52	68	0x110	I ² S global interrupt
USB	Configurable ⁽²⁾	53	69	0x114	USB global interrupt
—	—	54	70	0x118	Reserved
PDMA_CH0	Configurable ⁽²⁾	55	71	0x11C	PDMA channel 0 global interrupt
PDMA_CH1	Configurable ⁽²⁾	56	72	0x120	PDMA channel 1 global interrupt
PDMA_CH2	Configurable ⁽²⁾	57	73	0x124	PDMA channel 2 global interrupt
PDMA_CH3	Configurable ⁽²⁾	58	74	0x128	PDMA channel 3 global interrupt
PDMA_CH4	Configurable ⁽²⁾	59	75	0x12C	PDMA channel 4 global interrupt
PDMA_CH5	Configurable ⁽²⁾	60	76	0x130	PDMA channel 5 global interrupt
PDMA_CH6	Configurable ⁽²⁾	61	77	0x134	PDMA channel 6 global interrupt
PDMA_CH7	Configurable ⁽²⁾	62	78	0x138	PDMA channel 7 global interrupt
—	—	63	79	0x13C	Reserved
—	—	64	80	0x140	Reserved
—	—	65	81	0x144	Reserved
—	—	66	82	0x148	Reserved
—	—	67	83	0x14C	Reserved
EBI	Configurable ⁽²⁾	68	84	0x150	EBI global interrupt

- Note: 1. The exception priority can be changed using the NVIC System Handler Priority Registers. For more information, refer to the ARM “Technical Reference Manual of Cortex™-M3” document.
2. The interrupt priority can be changed using the NVIC Interrupt Priority Registers. For more information, refer to the ARM “Technical Reference Manual of Cortex™-M3” document.

Features

- 16 system Cortex™-M3 exceptions
- Up to 58 Maskable peripheral interrupts
- 16 programmable priority levels (4 bits for interrupt priority setting)
- Non-Maskable interrupt
- Low-latency exception and interrupt handling
- Vector table remapping capability
- Integrated simple, 24-bit system timer, SYSTICK
 - 24-bit down counter
 - Auto-reloading capability
 - Maskable system interrupt generation when counter decrements to 0
 - SysTick clock source derived from the HCLK or AHB clock divided by 8

Functional Descriptions

SysTick Calibration

The SysTick Calibration Value Register (SCALIB) is provided by the NVIC to give a reference time base for the RTOS tick timer or other purpose. The TENMS field in the SCALIB register has a fixed value of 9000 which is the counter reload value to indicate 1 ms when the clock source comes from the SysTick reference input clock STCLK with a frequency of 9 MHz (72 MHz divide by 8).

Register Map

The following table shows the NVIC registers and reset values.

Table 25. NVIC Register Map

Register	Offset	Description	Reset Value
NVIC Base Address = 0xE000_E000			
ICTR	0x004	Interrupt Control Type Register	0x0000_0001
SCTRL	0x010	SysTick Control and Status Register	0x0000_0000
SLOAD	0x014	SysTick Reload Value Register	Unpredictable
SVAL	0x018	SysTick Current Value Register	Unpredictable
SCALIB	0x01C	SysTick Calibration Value Register	0x4000_2328
ISER0_31	0x100	Irq 0 to 31 Set Enable Register	0x0000_0000
ISER32_63	0x104	Irq 32 to 63 Set Enable Register	0x0000_0000
ISER64_95	0x108	Irq 64 to 95 Set Enable Register	0x0000_0000
ICER0_31	0x180	Irq 0 to 31 Clear Enable Register	0x0000_0000
ICER32_63	0x184	Irq 32 to 63 Clear Enable Register	0x0000_0000
ICER64_95	0x188	Irq 64 to 95 Clear Enable Register	0x0000_0000
ISPR0_31	0x200	Irq 0 to 31 Set Pending Register	0x0000_0000
ISPR32_63	0x204	Irq 32 to 63 Set Pending Register	0x0000_0000
ISPR64_95	0x208	Irq 64 to 95 Set Pending Register	0x0000_0000
ICPR0_31	0x280	Irq 0 to 31 Clear Pending Register	0x0000_0000
ICPR32_63	0x284	Irq 32 to 63 Clear Pending Register	0x0000_0000
ICPR64_95	0x288	Irq 64 to 95 Clear Pending Register	0x0000_0000
IABR0_31	0x300	Irq 0 to 31 Active Bit Register	0x0000_0000
IABR32_63	0x304	Irq 32 to 63 Active Bit Register	0x0000_0000
IABR64_95	0x308	Irq 64 to 95 Active Bit Register	0x0000_0000
IRQ0_3	0x400	Irq 0 to 3 Priority Register	0x0000_0000
IRQ4_7	0x404	Irq 4 to 7 Priority Register	0x0000_0000
IRQ8_11	0x408	Irq 8 to 11 Priority Register	0x0000_0000
IRQ12_15	0x40C	Irq 12 to 15 Priority Register	0x0000_0000
IRQ16_19	0x410	Irq 16 to 19 Priority Register	0x0000_0000
IRQ20_23	0x414	Irq 20 to 23 Priority Register	0x0000_0000
IRQ24_27	0x418	Irq 24 to 27 Priority Register	0x0000_0000
IRQ28_31	0x41C	Irq 28 to 31 Priority Register	0x0000_0000
IRQ32_35	0x420	Irq 32 to 35 Priority Register	0x0000_0000
IRQ36_39	0x424	Irq 36 to 39 Priority Register	0x0000_0000
IRQ40_43	0x428	Irq 40 to 43 Priority Register	0x0000_0000
IRQ44_47	0x42C	Irq 44 to 47 Priority Register	0x0000_0000

Register	Offset	Description	Reset Value
IRQ48_51	0x430	Irq 48 to 51 Priority Register	0x0000_0000
IRQ52_55	0x434	Irq 52 to 55 Priority Register	0x0000_0000
IRQ56_59	0x438	Irq 56 to 59 Priority Register	0x0000_0000
IRQ60_63	0x43C	Irq 60 to 63 Priority Register	0x0000_0000
IRQ64_67	0x440	Irq 64 to 67 Priority Register	0x0000_0000
IRQ68_71	0x444	Irq 68 to 71 Priority Register	0x0000_0000
ICSR	0xD04	Interrupt Control State Register	0x0000_0000
VTOR	0xD08	Vector Table Offset Register	0x0000_0000
AIRCR	0xD0C	Application Interrupt/Reset Control Register	0xFA05_0000
SCR	0xD10	System Control Register	0x0000_0000
CCR	0xD14	Configuration Control Register	0x0000_0000
SHPR4-7	0xD18	System Handlers 4-7 Priority Register	0x0000_0000
SHPR8_11	0xD1C	System Handlers 8-11 Priority Register	0x0000_0000
SHPR12_15	0xD20	System Handlers 12-15 Priority Register	0x0000_0000
SHCSR	0xD24	System Handler Control and State Register	0x0000_0000
CFSR	0xD28	Configurable Fault Status Registers	0x0000_0000
HFSR	0xD2C	Hard Fault Status Register	0x0000_0000
DFSR	0xD30	Debug Fault Status Register	0x0000_0000
MMFAR	0xD34	Mem Manage Address Register	Unpredictable
BFAR	0xD38	Bus Fault Address Register	Unpredictable
AFSR	0xD3C	Auxiliary Fault Status Register	0x0000_0000
STIR	0xF00	Software Trigger Interrupt Register	0x0000_0000

Note: For more information of the above detail register descriptions, please refer to the “Technical Reference Manual of Cortex™-M3” document from ARM.

11

External Interrupt/Event Controller (EXTI)

Introduction

The External Interrupt/Event Controller, EXTI, comprises 16 edge detectors which can generate a wake-up event or interrupt requests independently. In interrupt mode there are five trigger types which can be selected as the external interrupt trigger type, low level, high level, negative edge, positive edge and both edges, selectable using the SRCnTYPE field in the EXTICFGRn register. In the wake-up event mode, the wake-up event polarity can be configured by setting the EXTInPOL field in the EXTIWAKUPPOLR register. If the EVWUPIEN bit in the EXTIWAKUPCR Register is set, the EVWUP interrupt can be generated when the associated wake-up event occurs and the corresponding EXTI wake-up enable bit is set. Each EXTI line can also be masked independently.

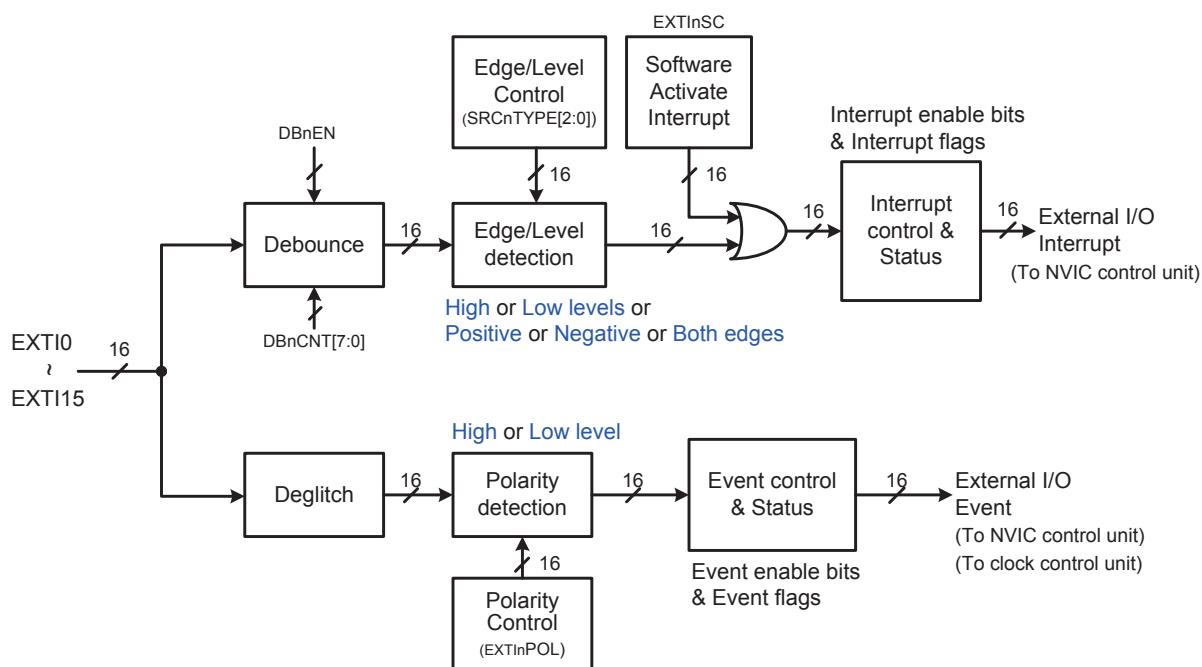


Figure 22. EXTI Block Diagram

Features

- Up to 16 EXTI lines with configurable trigger source and type
 - All GPIO pins can be selected as EXTI trigger source
 - Source trigger type includes high level, low level, negative edge, positive edge, or both edge
- Individual interrupt enable, wakeup enable and status bits for each EXTI line
- Software interrupt trigger mode for each EXTI line
- Integrated deglitch filter for short pulse blocking

Functional Descriptions

Wakeup Event Management

In order to wakeup the system from the power saving mode, the EXTI controller provides a function which can monitor external events and send them to the Cortex™-M3 core and the Clock Control Unit, CKCU. These external events include EXTI events, Low Voltage Detection, WAKEUP input pin and RTC wakeup functions. By configuring the wakeup event enable bit in the corresponding peripheral, the wakeup signal will be sent to the Cortex™-M3 and the CKCU via the EXTI controller when the corresponding wakeup event occurs. Additionally, the software can enable the event wakeup interrupt function by setting the EVWUPIEN bit in the EXTIWAKUPCR register and the EXTI controller will then assert an interrupt when the wakeup event occurs

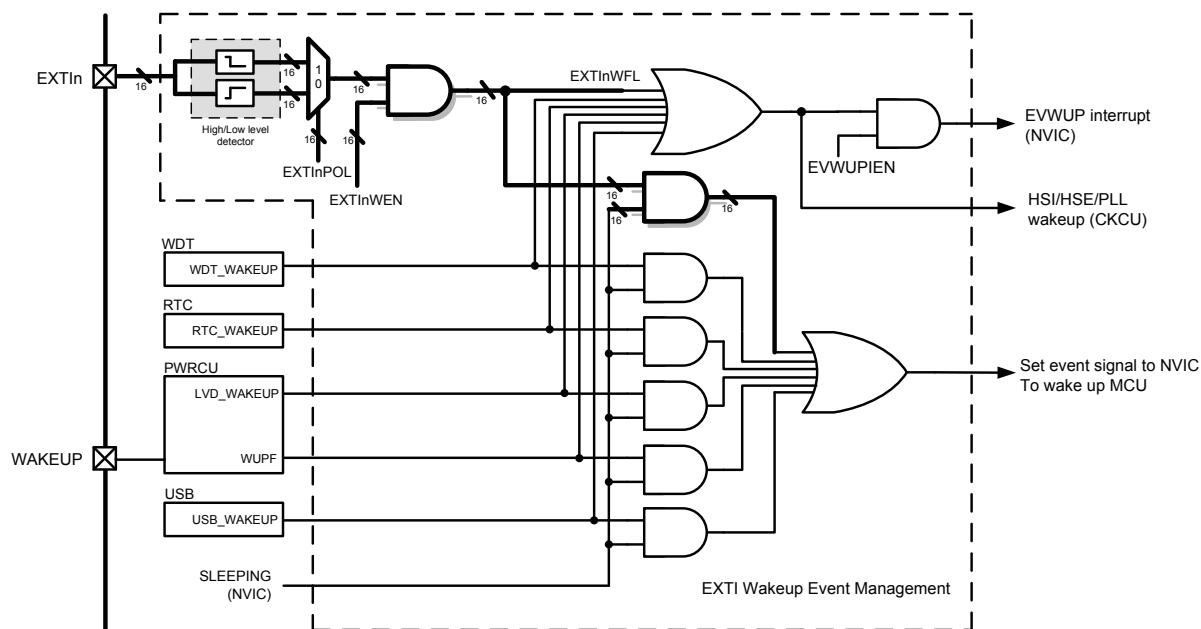


Figure 23. EXTI Wake-up Event Management

External Interrupt/Event Line Mapping

All GPIO pins can be selected as EXTI trigger sources by configuring the EXTInPIN [3:0] field in the AFIO ESSRn register to trigger an interrupt or event. Refer to the AFIO section for more details.

Interrupt and Debounce

The application software can set the DBnEN bit in the EXTIn Interrupt Configuration Register EXTICFGn to enable the corresponding pin de-bounce function and configure the DBnCNT field in the EXTICFGn so as to select an appropriate de-bounce time for specific applications. The interrupt signal will however be delayed due to the de-bounce function. When the device is woken up from the power saving mode by an external interrupt, an interrupt request will be generated by the EXTI wakeup flag. After the device has been woken up and the clock has recovered, the EXTI wake-up flag that was triggered by the EXTI line must be read and then cleared by application software. The accompanying diagram shows the relationship between the EXTI input signal and the EXTI interrupt/event request signal

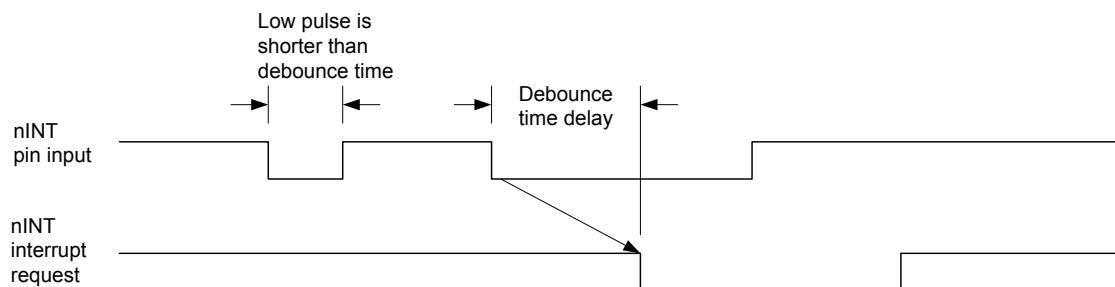


Figure 24. EXTI Debounce Function

Register Map

The following table shows the EXTI registers and reset values.

Table 26. EXTI Register Map

Register	Offset	Description	Reset Value
EXTI Base Address = 0x4002_4000			
EXTICFGR0	0x000	EXTI Interrupt 0 Configuration Register	0x0000_0000
EXTICFGR1	0x004	EXTI Interrupt 1 Configuration Register	0x0000_0000
EXTICFGR2	0x008	EXTI Interrupt 2 Configuration Register	0x0000_0000
EXTICFGR3	0x00C	EXTI Interrupt 3 Configuration Register	0x0000_0000
EXTICFGR4	0x010	EXTI Interrupt 4 Configuration Register	0x0000_0000
EXTICFGR5	0x014	EXTI Interrupt 5 Configuration Register	0x0000_0000
EXTICFGR6	0x018	EXTI Interrupt 6 Configuration Register	0x0000_0000
EXTICFGR7	0x01C	EXTI Interrupt 7 Configuration Register	0x0000_0000
EXTICFGR8	0x020	EXTI Interrupt 8 Configuration Register	0x0000_0000
EXTICFGR9	0x024	EXTI Interrupt 9 Configuration Register	0x0000_0000
EXTICFGR10	0x028	EXTI Interrupt 10 Configuration Register	0x0000_0000
EXTICFGR11	0x02C	EXTI Interrupt 11 Configuration Register	0x0000_0000
EXTICFGR12	0x030	EXTI Interrupt 12 Configuration Register	0x0000_0000
EXTICFGR13	0x034	EXTI Interrupt 13 Configuration Register	0x0000_0000
EXTICFGR14	0x038	EXTI Interrupt 14 Configuration Register	0x0000_0000
EXTICFGR15	0x03C	EXTI Interrupt 15 Configuration Register	0x0000_0000
EXTICR	0x040	EXTI Interrupt Control Register	0x0000_0000
EXTIEDGEFLGR	0x044	EXTI Interrupt Edge Flag Register	0x0000_0000
EXTIEDGESR	0x048	EXTI Interrupt Edge Status Register	0x0000_0000
EXTISCR	0x04C	EXTI Interrupt Software Set Command Register	0x0000_0000
EXTIWAKUPCR	0x050	EXTI Interrupt Wakeup Control Register	0x0000_0000
EXTIWAKUPPOLR	0x054	EXTI Interrupt Wakeup Polarity Register	0x0000_0000
EXTIWAKUPFLG	0x058	EXTI Interrupt Wakeup Flag Register	0x0000_0000

Register Descriptions

EXTI Interrupt Configuration Register n – EXTICFGRn, n = 0 ~ 15

This register is used to specify the debounce function and select the trigger type.

Offset: 0x000 (0) ~ 0x03C (15)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Type/Reset	DBnEN		SRCnTYPE				Reserved	
	RW 0	RW 0	RW 0	RW 0				
	23	22	21	20	19	18	17	16
Type/Reset					Reserved			
	15	14	13	12	11	10	9	8
Type/Reset					Reserved			
	7	6	5	4	3	2	1	0
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
					DBnCNT			

Bits	Field	Descriptions																								
[31]	DBnEN	EXTIn De-bounce Circuit Enable Bit (n = 0 ~ 15) 0: De-bounce circuit is disabled 1: De-bounce circuit is enabled																								
[30:28]	SRCnTYPE	EXTIn Interrupt Source Trigger Type (n = 0 ~ 15) No matter if the interrupt source is configured to be active by the EXTI, it should always be configured as level-sensitive. <table border="1"><thead><tr><th colspan="3">SRCnTYPE [2:0]</th><th>Interrupt Source Type</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>0</td><td>Low-level Sensitive</td></tr><tr><td>0</td><td>0</td><td>1</td><td>High-level Sensitive</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Negative-edge Triggered</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Positive-edge Triggered</td></tr><tr><td>1</td><td>X</td><td>X</td><td>Both-edge Triggered</td></tr></tbody></table>	SRCnTYPE [2:0]			Interrupt Source Type	0	0	0	Low-level Sensitive	0	0	1	High-level Sensitive	0	1	0	Negative-edge Triggered	0	1	1	Positive-edge Triggered	1	X	X	Both-edge Triggered
SRCnTYPE [2:0]			Interrupt Source Type																							
0	0	0	Low-level Sensitive																							
0	0	1	High-level Sensitive																							
0	1	0	Negative-edge Triggered																							
0	1	1	Positive-edge Triggered																							
1	X	X	Both-edge Triggered																							
[7:0]	DBnCNT	EXTIn De-bounce Counter (n = 0 ~ 15) The de-bounce time is calculated with DBnCNT x APB clock period and should be long enough to take effect on the input signal.																								

EXTI Interrupt Control Register – EXTICR

This register is used to control the EXTI interrupt.

Offset: 0x040

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24	
Reserved									
Type/Reset									
	23	22	21	20	19	18	17	16	
Reserved									
Type/Reset									
	15	14	13	12	11	10	9	8	
EXTI15EN EXTI14EN EXTI13EN EXTI12EN EXTI11EN EXTI10EN EXTI9EN EXTI8EN									
Type/Reset	RW	0	RW	0	RW	0	RW	0	
	7	6	5	4	3	2	1	0	
EXTI7EN EXTI6EN EXTI5EN EXTI4EN EXTI3EN EXTI2EN EXTI1EN EXTI0EN									
Type/Reset	RW	0	RW	0	RW	0	RW	0	

Bits	Field	Descriptions
[15:0]	EXTInEN	EXTIn Interrupt Enable Bit (n = 0 ~ 15) 0: EXTI line n interrupt is disabled 1: EXTI line n interrupt is enabled

EXTI Interrupt Edge Flag Register – EXTIEDGEFLGR

This register is used to indicate if an EXTI edge has been detected.

Offset: 0x044

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Reserved								
Type/Reset								
	23	22	21	20	19	18	17	16
Reserved								
Type/Reset								
	15	14	13	12	11	10	9	8
Type/Reset	EXTI15EDF	EXTI14EDF	EXTI13EDF	EXTI12EDF	EXTI11EDF	EXTI10EDF	EXTI9EDF	EXTI8EDF
	WC 0	WC 0	WC 0					
	7	6	5	4	3	2	1	0
Type/Reset	EXTI7EDF	EXTI6EDF	EXTI5EDF	EXTI4EDF	EXTI3EDF	EXTI2EDF	EXTI1EDF	EXTI0EDF
	WC 0	WC 0	WC 0					

Bits	Field	Descriptions
[15:0]	EXTInEDF	EXTIn Both Edge Detection Flag (n = 0 ~ 15) 0: No edge is detected 1: Positive or negative edge is detected This bit is set by the hardware circuitry when a positive or negative edge is detected on the corresponding EXTI line. Software should write 1 to clear it.

EXTI Interrupt Edge Status Register – EXTIEDGESR

This register indicates the polarity of a detected EXTI edge.

Offset: 0x048

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24	
Type/Reset	Reserved								
	23	22	21	20	19	18	17	16	
Type/Reset	Reserved								
	15	14	13	12	11	10	9	8	
Type/Reset	EXTI15EDS	EXTI14EDS	EXTI13EDS	EXTI12EDS	EXTI11EDS	EXTI10EDS	EXTI9EDS	EXTI8EDS	
	WC	0	WC	0	WC	0	WC	0	
	7	6	5	4	3	2	1	0	
Type/Reset	EXTI7EDS	EXTI6EDS	EXTI5EDS	EXTI4EDS	EXTI3EDS	EXTI2EDS	EXTI1EDS	EXTI0EDS	
	WC	0	WC	0	WC	0	WC	0	

Bits	Field	Descriptions
[15:0]	EXTInEDS	EXTIn Both Edge Detection Status (n = 0 ~ 15) 0: Negative edge is detected 1: Positive edge is detected Software should write 1 to clear it.

EXTI Interrupt Software Set Command Register – EXTISSCR

This register is used to activate the EXTI interrupt.

Offset: 0x04C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24	
Type/Reset	Reserved								
	23	22	21	20	19	18	17	16	
Type/Reset	Reserved								
	15	14	13	12	11	10	9	8	
Type/Reset	EXTI15SC	EXTI14SC	EXTI13SC	EXTI12SC	EXTI11SC	EXTI10SC	EXTI9SC	EXTI8SC	
	RW	0	RW	0	RW	0	RW	0	
	7	6	5	4	3	2	1	0	
Type/Reset	EXTI7SC	EXTI6SC	EXTI5SC	EXTI4SC	EXTI3SC	EXTI2SC	EXTI1SC	EXTI0SC	
	RW	0	RW	0	RW	0	RW	0	

Bits	Field	Descriptions
[15:0]	EXTInSC	EXTIn Software Set Command (n = 0 ~ 15) 0: Deactivates the corresponding EXTI interrupt 1: Activates the corresponding EXTI interrupt

EXTI Interrupt Wakeup Control Register – EXTIWAKUPCR

This register is used to control the EXTI interrupt and wakeup function.

Offset: 0x050

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	EVWUPIEN Reserved							
Type/Reset	RW 0							
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	EXTI15WEN	EXTI14WEN	EXTI13WEN	EXTI12WEN	EXTI11WEN	EXTI10WEN	EXTI9WEN	EXTI8WEN
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	EXTI7WEN	EXTI6WEN	EXTI5WEN	EXTI4WEN	EXTI3WEN	EXTI2WEN	EXTI1WEN	EXTI0WEN
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31]	EVWUPIEN	EXTI Event Wakeup Interrupt Enable Bit 0: Disable EVWUP interrupt 1: Enable EVWUP interrupt
[15:0]	EXTInWEN	EXTIn Wakeup Enable Bit (n = 0 ~ 15) 0: Power saving mode wakeup is disabled 1: Power saving mode wakeup is enabled

EXTI Interrupt Wakeup Polarity Register – EXTIWAKUPPOLR

This register is used to select the EXTI line interrupt wakeup polarity.

Offset: 0x054

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Reserved								
Type/Reset								
Reserved								
Type/Reset	23	22	21	20	19	18	17	16
Reserved								
Type/Reset	15	14	13	12	11	10	9	8
EXTI15POL EXTI14POL EXTI13POL EXTI12POL EXTI11POL EXTI10POL EXTI9POL EXTI8POL								
Type/Reset	RW	0	RW	0	RW	0	RW	0
	7	6	5	4	3	2	1	0
EXTI7POL EXTI6POL EXTI5POL EXTI4POL EXTI3POL EXTI2POL EXTI1POL EXTI0POL								
Type/Reset	RW	0	RW	0	RW	0	RW	0

Bits	Field	Descriptions
[15:0]	EXTInPOL	EXTIn Wakeup Polarity (n = 0 ~ 15) 0: EXTIn wakeup is high level active 1: EXTIn wakeup is low level active

EXTI Interrupt Wakeup Flag Register – EXTIWAKUPFLG

This register is the EXTI interrupt wake flag register.

Offset: 0x058

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24	
Reserved									
Type/Reset									
Reserved									
Type/Reset	23	22	21	20	19	18	17	16	
Reserved									
Type/Reset	15	14	13	12	11	10	9	8	
EXTI15WFL EXTI14WFL EXTI13WFL EXTI12WFL EXTI11WFL EXTI10WFL EXTI9WFL EXTI8WFL									
Type/Reset	WC 0								
	7	6	5	4	3	2	1	0	
EXTI7WFL EXTI6WFL EXTI5WFL EXTI4WFL EXTI3WFL EXTI2WFL EXTI1WFL EXTI0WFL									
Type/Reset	WC 0								

Bits	Field	Descriptions
[15:0]	EXTInWFL	EXTIn Wakeup Flag (n = 0 ~ 15) 0: No wakeup occurs 1: System is waken up by EXTIn Software should write 1 to clear it.

12 Analog to Digital Converter (ADC)

Introduction

A 12-bit multi-channel Analog to Digital Converter is integrated within the device. There are a total of 18 multiplexed channels including 16 external channels on which the external analog signal can be supplied as well as 2 internal channels. An Analog Watchdog function is also provided to ensure that the A/D input voltages remain within a specific threshold window, otherwise an interrupt will be generated to indicate that the input voltage is higher or lower than the set thresholds. There are three conversion modes to convert an analog signal to digital data. The A/D conversion can be operated in one shot, continuous and discontinuous conversion modes. A left-aligned or right-aligned 16-bit data register is provided to store the data after conversion.

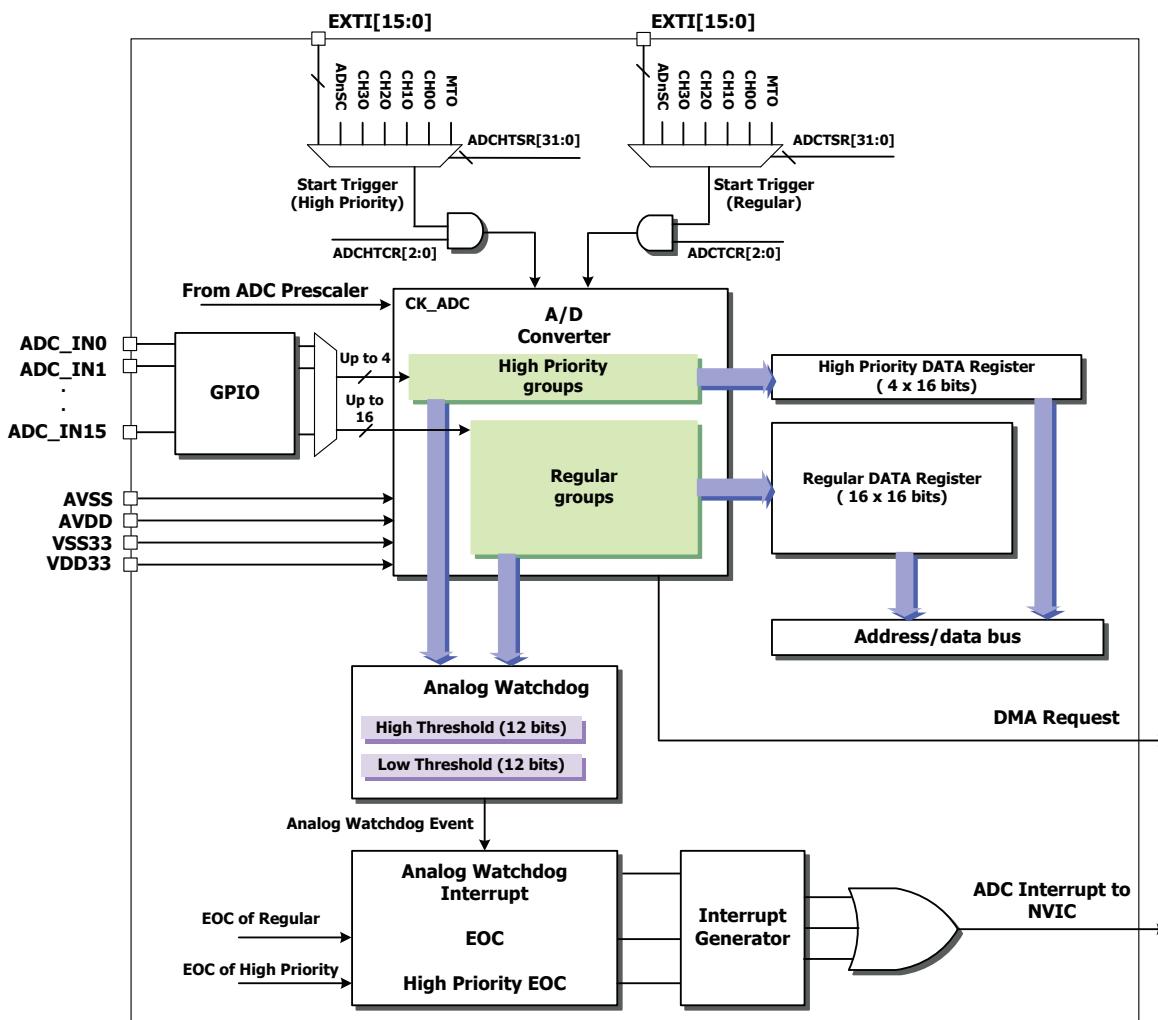


Figure 25. ADC Block Diagram

Features

- 12-bit SAR ADC engine
- Up to 1 MSPS conversion rate
 - 1 μ s at 56 MHz, 1.17 μ s at 72 MHz
- 16 external analog input channels
- 2 internal analog input channels for reference voltage measurement
- Separately programmable sampling time for each channel
- Three conversion modes
 - One shot conversion mode
 - Continuous conversion mode
 - Discontinuous conversion mode.
- Two level conversion priority
 - Regular – can still be interrupted by a high priority conversion
 - High priority
- Up to 16 dedicated sequencer and data registers for regular conversion
- Up to 4 dedicated sequencer and data registers for high priority conversion
- Data alignment adjustment and offset cancellation
 - Right/left alignment
 - Signed/unsigned
 - 16 offset registers for each channel
- Analog watchdog for predefined voltage range monitor
 - Lower/upper threshold register
 - Interrupt generation
- Various trigger start sources for both regular and high priority conversion modes
 - Software trigger
 - EXTI - external interrupt input pin
 - GPTM0 / GPTM1 trigger
 - MCTM0 / MCTM1 trigger
 - BFTM0 / BFTM1 trigger
- Multiple generated interrupts
 - End of single conversion
 - End of subgroup conversion
 - End of cycle conversion
 - Analog Watchdog
 - Data register overwriting
- PDMA request when end of conversion occurs

Functional Descriptions

ADC Clock Setup

The ADC clock, CK_ADC is provided by the Clock Controller which is synchronous with the APB clock, known as PCLK. Refer to the Clock Control Unit chapter for more details. Notes that the ADC requires at least two ADC clock cycles to switch between its power-on and power off conditions (ADEN bit = '0').

Regular and High Priority Channel Selection

The A/D converter has 16 multiplexed channels and after conversion organises the conversion results into two groups: a regular group and a high priority group. A regular group can organise a conversion sequence which can be implemented on channels arranged in a specific conversion sequence length from 1 to 16. For example, conversion can be carried out with the following channel sequence: CH2, CH4, CH7, CH5, CH6, CH3, CH1 and CH0 one after another.

A regular group is composed of up to 16 conversions. The selected channels of the regular group conversion can be specified in the ADCLST0~ADCLST3 registers. The total conversion sequence length is setup using the ADSEQL[3:0] bits in the ADCCONV register.

A high priority group is composed of up to 4 conversions. The sequence length and the selected channels of the high priority conversion can be specified in the ADCHLST register. The total conversion sequence length of the high priority group can be setup in the ADHSEQL[1:0] bits in the ADCHCONV register.

Modifying the ADCCONV or ADCHCONV register during a conversion process will reset the current conversion, after which a new start pulse is required to restart a new conversion.

Conversion Modes

The A/D has three operating conversion modes. The conversion modes are One Shot Conversion Mode, Continuous Conversion Mode, and Discontinuous Conversion mode. Details are provided later.

One Shot Conversion Mode

In the one shot conversion mode, the ADC will perform conversion cycles on the channels specified in the A/D conversion list registers ADCLSTn or ADCHLST with a specific sequence when an A/D converter event occurs. When the A/D conversion mode field AD(H)MODE [1:0] is set to 0x0, the A/D converter will operate in the One Shot Conversion Mode. This mode can be started by a software trigger, an external EXTI event or a TM event determined by the Trigger Control Register, ADCTCR or ADCHTCR, and the Trigger Source Register ADCTS or ADCHTS.

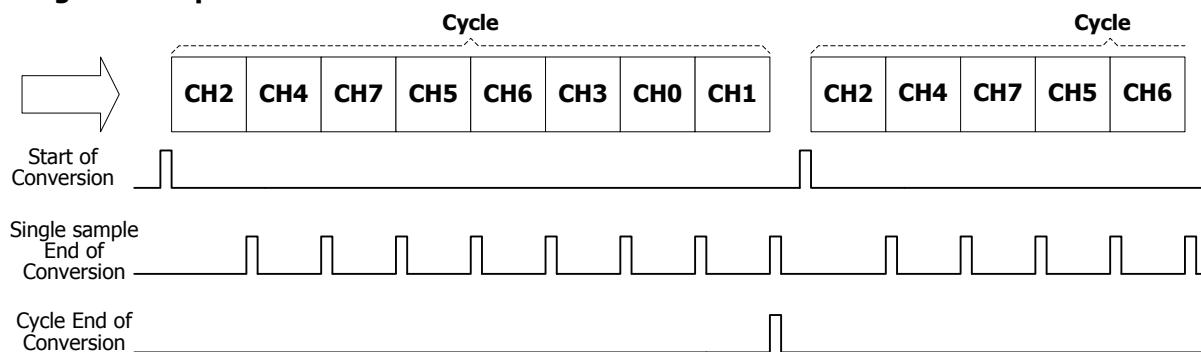
Regular Conversion

- The converted data will be stored in the 16-bit ADCDRy (y = 0~15) register.
- The ADC regular single sample end of conversion event raw status flag, ADIRAWS, in the ADCIRAW register will be set when the single sample conversion has finished.
- An interrupt will be generated after a single sample end of conversion if the ADIES bit in the ADCIER register is enabled.
- An interrupt will be generated after a regular group cycle end of conversion if the ADIEC bit in the ADCIER register is enabled.

High Priority Conversion

- The converted data will be stored in the 16-bit ADCHDR_y ($y = 0\sim 3$) registers
- The ADC high priority single sample end of conversion event raw status flag, ADIRAWHS, in the ADCIRAW register, will be set when the conversion has finished.
- An interrupt will be produced if the ADIEHS bit in the ADCIER register is enabled.
- An interrupt will be generated after a high priority group cycle end of conversion if the ADIEHC bit in the ADCIER register is enabled.

Regular Group (ex: Sequence Length=8)



High Priority Group (ex: Sequence Length=4)

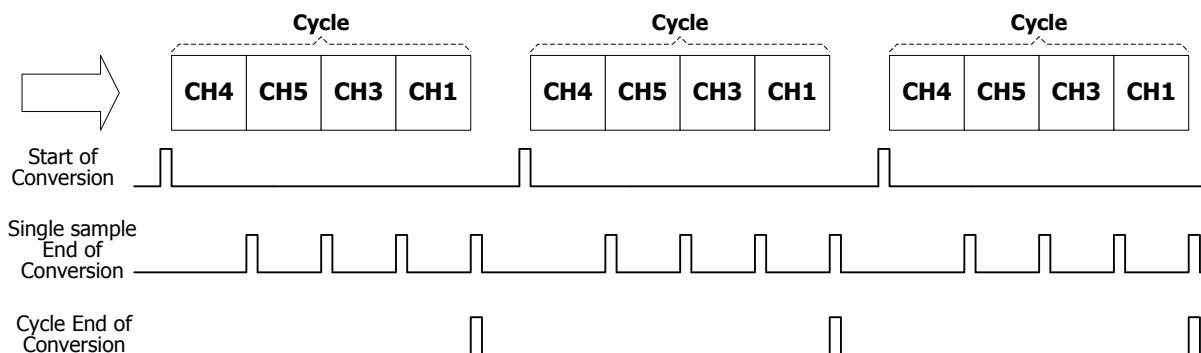


Figure 26. One Shot Conversion Mode

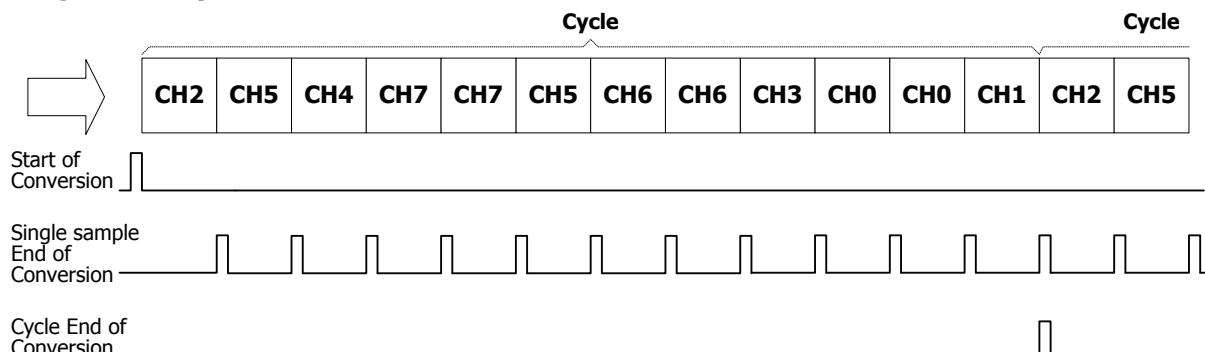
Continuous Conversion Mode

In the Continuous Conversion Mode, repeated conversion cycles will start automatically without requiring additional A/D start trigger signals after a channel group conversion has completed. When the A/D conversion mode field AD(H)MODE [1:0] is set to 0x2, the A/D converter will operate in the Continuous Conversion Mode. A conversion cycle can be started by a software trigger, an external EXTI event or a TM event determined by the Trigger Control Register, ADCTCR or ADCHTCR, and the Trigger Source Register ADCTS or ADCHTSR.

After each conversion

- The converted data will be stored in the 16-bit ADCDR_y ($y = 0\sim15$) or ADCHDR_y ($y = 0\sim3$) registers.
- The ADC regular group or high priority group cycle end of conversion event raw status flags, ADIRAWC or ADIRAWHC, in the ADCIRAW register will be set when the conversion cycle is finished.
- An interrupt will be generated after an end of conversion if the ADIEC or ADIEHC bit in the ADCIER register is enabled.

Regular Group (ex: Sequence Length=12)



High Priority Group (ex: Sequence Length=3)

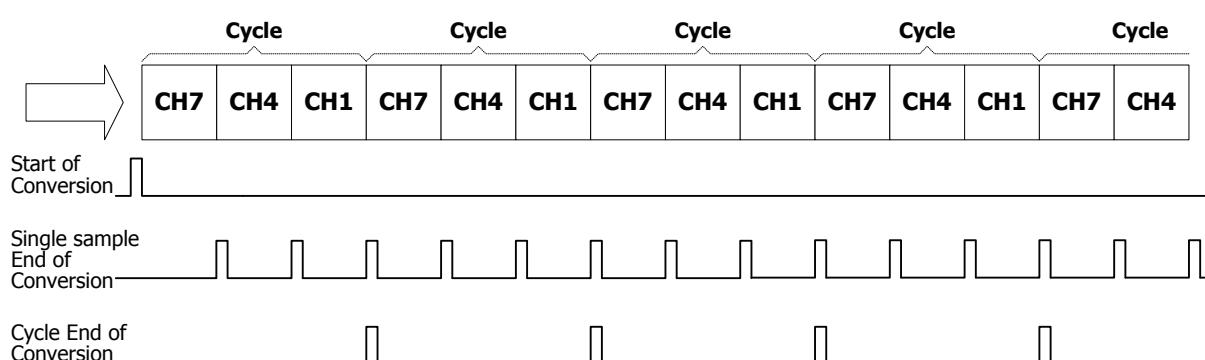


Figure 27. Continuous Conversion Mode

Discontinuous Conversion Mode

Regular group

The A/D converter will operate in the Discontinuous Conversion Mode for regular groups when the A/D conversion mode bit field ADMODE [1:0] in the ADCCONV register is set to 0x3. The regular group to be converted can have up to 16 channels and can be arranged in a specific sequence by configuring the ADCLSTn registers where n ranges from 0 to 3. This mode is provided to convert data for a regular group with a short sequence, named as the A/D regular conversion subgroup, each time a trigger event occurs. The subgroup length is defined in the ADSUBL [3:0] field to specify the subgroup length. In the Discontinuous Conversion Mode the A/D converter can be started by a software trigger, an external EXTI event or a TM event for regular groups determined by the Trigger Control Register ADCTCR and the Trigger Source Register ADCTS.R.

In the Discontinuous Conversion Mode, the A/D Converter will start to convert the next n conversions where the number n is the subgroup length defined by the ADSUBL field. When a trigger event occurs, the channels to be converted with a specific sequence are specified in the ADCLSTn registers. After n conversions have completed, the regular subgroup EOC interrupt raw flag, ADIRAWG, in the ADCIRAW register will be asserted. The A/D converter will now not continue with the next n conversions until the next trigger event occurs. The conversion cycle will end after all the regular group channels, of which the total number is defined by the ADSEQL[3:0] bits in the ADCCONV register, have finished their conversion, at which point the regular cycle EOC interrupt raw flag, ADIRAWC, in the ADCIRAW register will be asserted. If a new trigger event occurs after all the subgroup channels have all been converted, i.e., a complete conversion cycle has been finished, the conversion will restart from the first subgroup.

Examples:

A/D subgroup length = 3 (ADSUBL=2) and sequence length = 8 (ADSEQL=7), channels to be converted = 2, 4, 7, 5, 6, 3, 0 and 1 - specific converting sequence as defined in the ADCLSTn registers,

- Trigger 1: subgroup channels to be converted are CH2, CH4 and CH7 with the ADIRAWG flag being asserted after subgroup EOC.
- Trigger 2: subgroup channels to be converted are CH5, CH6 and CH3 with the ADIRAWG flag being asserted after subgroup EOC.
- Trigger 3: subgroup channels to be converted are CH0 and CH1 with the ADIRAWG flag being asserted after subgroup EOC. Also a cycle end of conversion (EOC) interrupt raw flag ADIRAWC will be asserted.
- Trigger 4: subgroup channels to be converted are CH2, CH4 and CH7 with the ADIRAWG flag being asserted - conversion sequence restarts from the beginning.

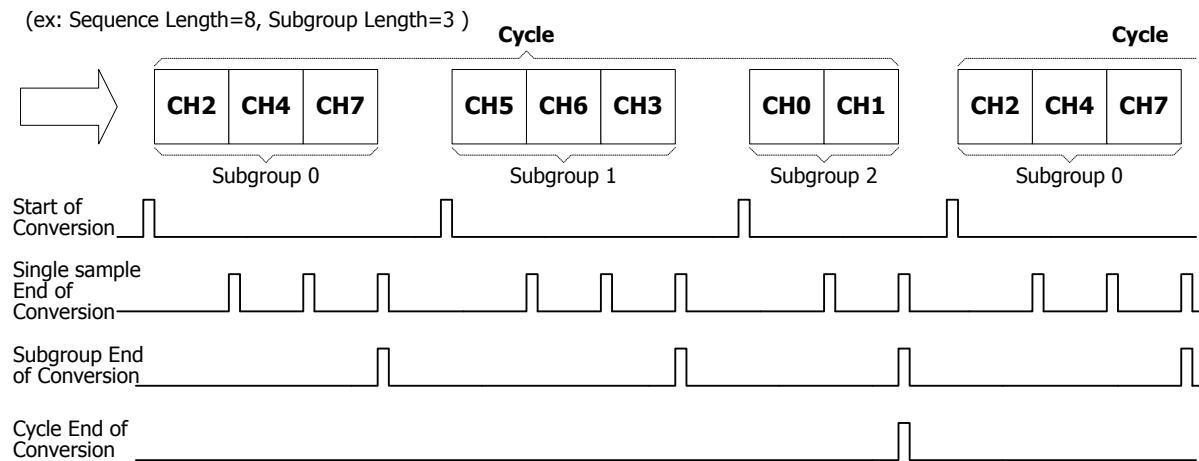


Figure 28. Regular Group Discontinuous Conversion Mode

High priority group

The A/D converter will operate in the Discontinuous Conversion Mode for the high priority group when the A/D high priority conversion mode bit field, ADHMODE [1:0], in the ADCHCONV register is set to 0x3. The high priority group to be converted can be up to 4 channels and can be arranged in a specific sequence by configuring the ADCHLST register. This mode is provided to convert data for the high priority group with a short sequence, named as the A/D high priority conversion subgroup, each time a trigger event occurs. The subgroup length is defined in the ADHSUBL [1:0] field to specify the high priority subgroup length. In the Discontinuous Conversion Mode the A/D converter can be started by a software trigger, an external EXTI event or a TM event for high priority group determined by the high priority Trigger Control Register ADCHTCR and the Trigger Source Register ADCHTSR.

In the Discontinuous Conversion Mode, the A/D Converter will start to convert the next n conversions when a trigger event occurs. Here the number n is the subgroup length defined by the ADHSUBL field. The channels to be converted with a specific sequence are specified in the ADCHLST register. After n conversions have finished, the high priority subgroup EOC interrupt raw flag ADIRAWHG in the ADCIRAW register will be asserted. The A/D converter will then not execute any further n conversions until the next trigger event occurs. The conversion cycle will finish after all the high priority group channels, of which the total number is defined by the ADHSEQ[1:0] bits in the ADCHCONV register, have finished conversion. The high priority cycle EOC interrupt raw flag, ADIRAWHC, in the ADCIRAW register will also be asserted. If a new trigger event occurs after all the subgroup channels have been converted, i.e., a complete conversion cycle has finished, the conversion will restart from the first subgroup.

Example:

A/D subgroup length = 2 (ADHSUBL=1) and sequence length = 3 (ADHSEQL=2), channels to be converted = 4, 7 and 1 (specific converting sequence defined in ADCHLST registers).

- Trigger 1: subgroup channels to be converted are CH4 and CH7 with the ADIRAWHG flag being asserted after subgroup EOC.
- Trigger 2: subgroup channel to be converted is CH1 with the ADIRAWHG flag being asserted after subgroup EOC. A Cycle end of conversion (EOC) interrupt raw flag, ADIRAWHC, will also be asserted.
- Trigger 3: subgroup channels to be converted are CH4 and CH7 with the ADIRAWHG flag being asserted after subgroup EOC - conversion sequence restarts from the beginning.

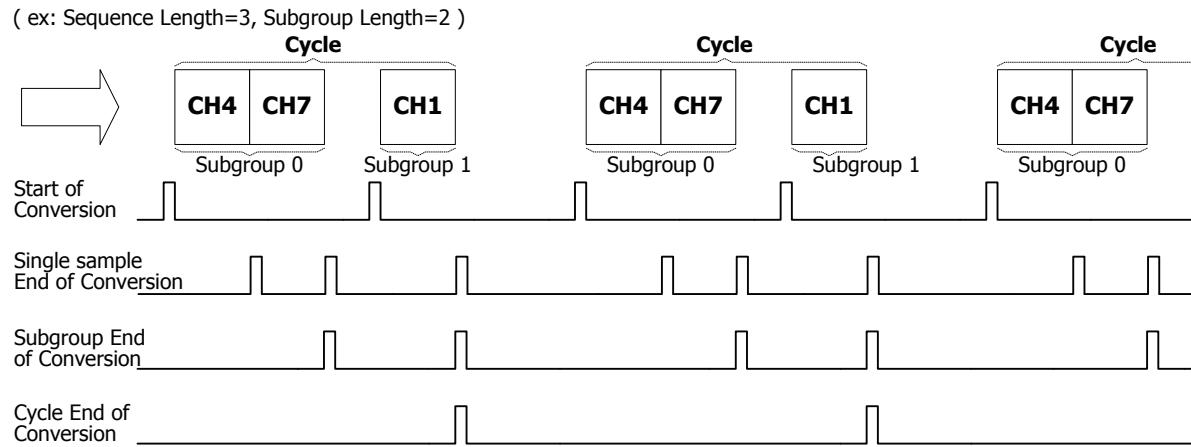


Figure 29. High Priority Group Discontinuous Conversion Mode

Start Conversion on External Event

Data conversion can be initiated by a software trigger, a General-Purpose Timer Module (GPTM) event, a Motor Control Timer Module (MCTM) event, a Basic Function Timer Module (BFTM) event or an external trigger. Each trigger source can be enabled by setting the corresponding enable control bit in the ADCTCR or ADCHTCR register and then selected by configuring the associated selection bits in the ADCTSR or ADCHTSR register to start a group channel conversion.

An A/D converter conversion can be started by setting the software trigger bit, ADSC or ADHSC, in the ADCTSR or ADCHTSR register for the regular or high priority group channel when the software trigger enable bit, ADSW or ADHSW, in the ADCTCR or ADCHTCR register is set to 1. After the A/D converter starts converting the analog data, the corresponding enable bit, ADSC or ADHSC, will be cleared to 0 automatically.

The A/D converter can also be triggered to start a regular or high priority channel conversion by a TM event. The TM events include a GPTM or MCTM master trigger output MTO, four GPTM or MCTM channel outputs CH0~CH3 and a BFTM trigger output. If the corresponding TM trigger enable bit is set to 1 and the trigger output or the TM channel event is selected via the relevant TM event selection bits, the A/D converter will start a conversion when a rising edge of the selected trigger event occurs.

In addition to the internal trigger sources, the A/D converter can be triggered to start a conversion by an external trigger event. The external trigger event is derived from the external lines EXTIn. If the external trigger enable bit, ADEXTI or ADHEXTI, is set to 1 and the corresponding EXTI line is selected by configuring the ADEXTIS or ADHEXTIS bit for regular or high priority group, the A/D converter will start a conversion when an EXTI line rising edge occurs.

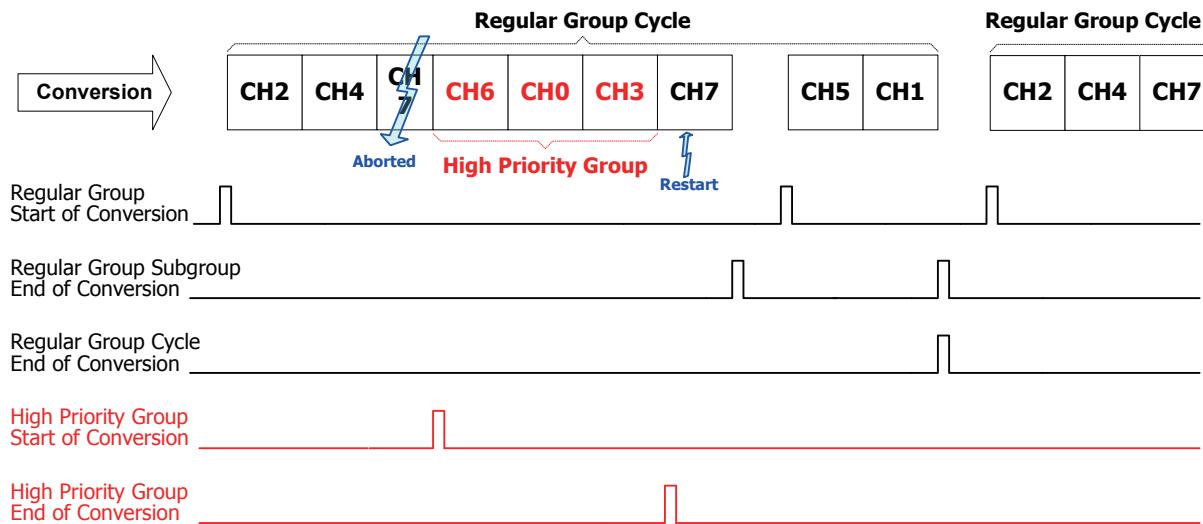
High Priority Group Management

The high priority channels have a higher priority than the regular A/D conversion channels. If, during a regular conversion process, a high priority channel trigger event occurs, then the current regular channel conversion will be aborted and the high priority channel conversion will be initiated.

The high priority channel length to be converted depends upon the high priority group conversion mode as the high priority start trigger occurs. When a high priority start trigger occurs, the high priority channel length to be converted is defined by the ADHSQL field for the one shot conversion mode. For the discontinuous conversion mode, the length to be converted is the high priority subgroup length defined by ADHSUBL field. If the high priority group is configured to be operated in the continuous conversion mode, the high priority conversion will keep converting each channel in the high priority group repeatedly after a high priority start trigger occurs until the high priority conversion mode has been changed.

When the high priority conversion has finished, the regular group conversion will then restart from the aborted channel location. Note that no matter what conversion mode the regular group operates in, the high priority conversion will always interrupt the current regular group conversion when a high priority start trigger occurs regardless of the high priority group conversion mode.

- ◆ Regular Group : Sequence Length=5, Subgroup Length=3, discontinuous conversion mode
- ◆ **High Priority Group** : Sequence Length=3, one shot conversion mode



- ◆ Regular Group : Sequence Length=5, Subgroup Length=3, discontinuous conversion mode
- ◆ **High Priority Group** : Sequence Length=3, Subgroup Length=2, discontinuous conversion mode

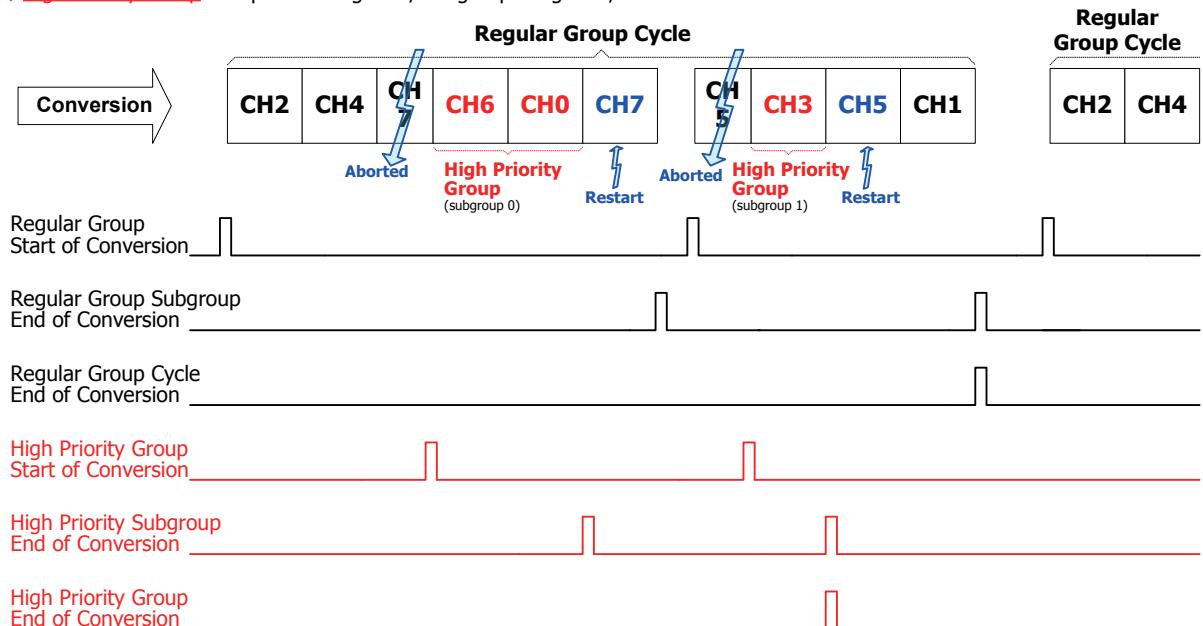


Figure 30. High Priority Channel Management

Sampling Time Setup

Each conversion channel can be sampled with a different sampling time. By modifying the ADSTn [7:0] bits in the ADCSTRn (n = 0~15) registers, the sampling time of the analog input signal can be determined.

The total conversion time (T_{conv}) is calculated using the following formula:

$$T_{\text{conv}} = T_{\text{Sampling}} + T_{\text{Latency}}$$

Where the minimum sampling time $T_{\text{Sampling}} = 1.5$ cycles (when ADST [7:0] = 0) and the minimum channel conversion latency $T_{\text{Latency}} = 12.5$ cycles.

Example:

With the A/D Converter clock $CK_{\text{ADC}} = 14$ MHz and a sampling time =1.5 cycles:

$$T_{\text{conv}} = 1.5 + 12.5 = 14 \text{ cycles} = 1 \mu\text{s}$$

Data Format and Alignment

The A/D Conversion result can have different output data formats, selected by the configuring the ADOFE and ADAL bits in the ADCOFRn (n = 0~15) registers, which is shown in Table 27.

Each channel has a dedicated offset subtraction function whose offset value can be defined by the user and written into the ADCOFRn (n = 0~15) register. The original A/D conversion data written in the data register will always be an unsigned number between 0x0FFF and 0x0000 in which only twelve bits are significant. If the ADOFEn bit in the ADCOFRn (n = 0~15) register is set to 1 then the offset subtraction is enabled. The significant conversion data in the ADCDRy (y = 0~15) or ADCHDRy (y = 0~3) registers has a thirteen bit format where the *most significant bit* (MSB) of the data stream is the sign bit

Table 27. Data format in ADCDRy[15:0] (y = 0~15) and ADCHDRy[15:0] (y = 0~3)

ADOFE	ADAL	Description	Data Format
0	0	Right aligned and unsigned	"0_0_0_0_d11_d10_d9_d8_d7_d6_d5_d4_d3_d2_d1_d0"
0	1	Left aligned and unsigned	"d11_d10_d9_d8_d7_d6_d5_d4_d3_d2_d1_d0_0_0_0"
1	0	Right aligned and signed after offset subtraction	"0_0_0_Sign bit_d11_d10_d9_d8_d7_d6_d5_d4_d3_d2_d1_d0_0_0_0"
1	1	Left aligned and signed after offset subtraction	"Sign bit_d11_d10_d9_d8_d7_d6_d5_d4_d3_d2_d1_d0_0_0_0"

Analog Watchdog

The A/D converter includes a watchdog function to monitor the converted data. There are two kinds of thresholds for the watchdog monitor function, known as the watchdog upper threshold and watchdog lower threshold, which are specified in the Watchdog Upper and Lower Threshold Registers respectively. The watchdog monitor function is enabled by setting the watchdog upper and lower threshold monitor function enable bits, ADWUE and ADWLE, in the watchdog control register ADCWCR. The channel to be monitored can be specified by configuring the ADWCH and ADWALL bits. When the converted data is less or higher than the lower or upper threshold, as defined in the ADCLTR or ADCUTR registers respectively, the watchdog lower or upper threshold interrupt raw flags, ADIRAWL or ADIRAWU, in the ADCIRAW register, will be asserted if the watchdog lower or upper threshold monitor function is enabled. If the lower or upper threshold interrupt raw flag is asserted and the corresponding interrupt is enabled by setting the ADIEL or ADIEU bits in the ADCIER register, a A/D watchdog lower or upper threshold interrupt will be generated.

Interrupts

When an A/D conversion is completed, an End of Conversion EOC event will occur. There are three kinds of EOC events which are known as single sample EOC, subgroup EOC and cycle EOC for both regular and high priority groups. A single sample EOC event will occur and the single sample EOC interrupt raw flag, ADIRAWS or ADIRAWHS, in the ADCIRAW register, will be asserted when a single channel conversion has completed. A subgroup EOC event will occur and the subgroup EOC interrupt raw flag, ADIRAWG or ADIRAWHG, in the ADCIRAW register, will be asserted when a subgroup conversion has completed. A cycle EOC event will occur and the cycle EOC interrupt raw flag, ADIRAWC or ADIRAWHC, in the ADCIRAW register, will be asserted when a cycle conversion is finished. When a single sample EOC, a subgroup EOC or a cycle EOC raw flag is asserted and the corresponding interrupt enable bits, ADIEC, ADIEG, ADIES, ADIEHC, ADIEHG or ADIEHS, in the ADCIER register, is set to 1, the associated interrupt will be generated.

After a conversion has completed, the 12-bit digital data will be stored in the associated ADCDRy or ADCHDRy register and the value of the data valid flag, ADVLDy or ADHVLDy, will be changed from low to high. The converted data should be read by the application program, after which the data valid flag, ADVLDy or ADHVLDy, will be automatically changed from high to low. Otherwise, a data overwrite event will occur and the data overwrite interrupt raw flag, ADIRAWO or ADIRAWHO, in the ADCIRAW register will be asserted. When the related data overwrite raw flag is asserted, the data overwrite interrupt will be generated if the interrupt enable bit, ADIEO or ADIEHO, in the ADCIER register is set to 1.

If the A/D watchdog monitor function is enabled and the data after a channel conversion is less than the lower threshold or higher than the upper threshold, the watchdog lower or upper threshold interrupt raw flag, ADIRAWL or ADIRAWU, in the ADCIRAW register will be asserted. When the ADIRAWL or ADIRAWU flag is asserted and the corresponding interrupt enable bit, ADIEL or ADIEU, in the ADCIER register, is set then a watchdog lower or upper threshold interrupt will be generated.

The A/D Converter interrupt clear bits are used to clear the associated A/D converter interrupt raw and interrupt status bits. Writing a 1 into the specific A/D converter interrupt clear bit in the A/D converter interrupt clear register, ADCICLR, will clear the corresponding A/D converter interrupt raw and interrupt status bits. These bits are automatically cleared to 0 by hardware after being set to 1.

PDMA Request

The converted channel value will be stored in the corresponding data register. The A/D Converter can inform the MCU using the A/D Converter corresponding EOC interrupt if new conversion data is already stored in the ADC(H)DRn register. Users also can determine the PDMA request is asserted by setting the ADDMAC, ADDMAG, ADDMAS, ADDMAHC, ADDMAHG or ADDMAHS bit in the ADCDMAR register. A PDMA request will be automatically generated at the end of each A/D conversion. A detailed description is provided in the ADCDMAR register description section. .

Register Map

The following table shows the A/D Converter registers and reset values.

Table 28. ADC Register Map

Register	Offset	Description	Reset Value
ADC Base Address = 0x4001_0000			
ADCRST	0x004	ADC Reset Register	0x0000_0000
ADCCONV	0x008	ADC Regular Conversion Mode Register	0x0000_0000
ADCHCONV	0x00C	ADC High Priority Conversion Mode Register	0x0000_0000
ADCLST0	0x010	ADC Regular Conversion List Register 0	0x0000_0000
ADCLST1	0x014	ADC Regular Conversion List Register 1	0x0000_0000
ADCLST2	0x018	ADC Regular Conversion List Register 2	0x0000_0000
ADCLST3	0x01C	ADC Regular Conversion List Register 3	0x0000_0000
ADCHLST	0x020	ADC High Priority Conversion List Register	0x0000_0000
ADCOFR0	0x030	ADC Input 0 Offset Register	0x0000_0000
ADCOFR1	0x034	ADC Input 1 Offset Register	0x0000_0000
ADCOFR2	0x038	ADC Input 2 Offset Register	0x0000_0000
ADCOFR3	0x03C	ADC Input 3 Offset Register	0x0000_0000
ADCOFR4	0x040	ADC Input 4 Offset Register	0x0000_0000
ADCOFR5	0x044	ADC Input 5 Offset Register	0x0000_0000
ADCOFR6	0x048	ADC Input 6 Offset Register	0x0000_0000
ADCOFR7	0x04C	ADC Input 7 Offset Register	0x0000_0000
ADCOFR8	0x050	ADC Input 8 Offset Register	0x0000_0000
ADCOFR9	0x054	ADC Input 9 Offset Register	0x0000_0000
ADCOFR10	0x058	ADC Input 10 Offset Register	0x0000_0000
ADCOFR11	0x05C	ADC Input 11 Offset Register	0x0000_0000
ADCOFR12	0x060	ADC Input 12 Offset Register	0x0000_0000
ADCOFR13	0x064	ADC Input 13 Offset Register	0x0000_0000
ADCOFR14	0x068	ADC Input 14 Offset Register	0x0000_0000
ADCOFR15	0x06C	ADC Input 15 Offset Register	0x0000_0000
ADCSTR0	0x070	ADC Input 0 Sampling Time Register	0x0000_0000
ADCSTR1	0x074	ADC Input 1 Sampling Time Register	0x0000_0000
ADCSTR2	0x078	ADC Input 2 Sampling Time Register	0x0000_0000
ADCSTR3	0x07C	ADC Input 3 Sampling Time Register	0x0000_0000
ADCSTR4	0x080	ADC Input 4 Sampling Time Register	0x0000_0000
ADCSTR5	0x084	ADC Input 5 Sampling Time Register	0x0000_0000
ADCSTR6	0x088	ADC Input 6 Sampling Time Register	0x0000_0000

Register	Offset	Description	Reset Value
ADCSTR7	0x08C	ADC Input 7 Sampling Time Register	0x0000_0000
ADCSTR8	0x090	ADC Input 8 Sampling Time Register	0x0000_0000
ADCSTR9	0x094	ADC Input 9 Sampling Time Register	0x0000_0000
ADCSTR10	0x098	ADC Input 10 Sampling Time Register	0x0000_0000
ADCSTR11	0x09C	ADC Input 11 Sampling Time Register	0x0000_0000
ADCSTR12	0x0A0	ADC Input 12 Sampling Time Register	0x0000_0000
ADCSTR13	0x0A4	ADC Input 13 Sampling Time Register	0x0000_0000
ADCSTR14	0x0A8	ADC Input 14 Sampling Time Register	0x0000_0000
ADCSTR15	0x0AC	ADC Input 15 Sampling Time Register	0x0000_0000
ADCDR0	0x0B0	ADC Regular Conversion Data Register 0	0x0000_0000
ADCDR1	0x0B4	ADC Regular Conversion Data Register 1	0x0000_0000
ADCDR2	0x0B8	ADC Regular Conversion Data Register 2	0x0000_0000
ADCDR3	0x0BC	ADC Regular Conversion Data Register 3	0x0000_0000
ADCDR4	0x0C0	ADC Regular Conversion Data Register 4	0x0000_0000
ADCDR5	0x0C4	ADC Regular Conversion Data Register 5	0x0000_0000
ADCDR6	0x0C8	ADC Regular Conversion Data Register 6	0x0000_0000
ADCDR7	0x0CC	ADC Regular Conversion Data Register 7	0x0000_0000
ADCDR8	0x0D0	ADC Regular Conversion Data Register 8	0x0000_0000
ADCDR9	0x0D4	ADC Regular Conversion Data Register 9	0x0000_0000
ADCDR10	0x0D8	ADC Regular Conversion Data Register 10	0x0000_0000
ADCDR11	0x0DC	ADC Regular Conversion Data Register 11	0x0000_0000
ADCDR12	0x0E0	ADC Regular Conversion Data Register 12	0x0000_0000
ADCDR13	0x0E4	ADC Regular Conversion Data Register 13	0x0000_0000
ADCDR14	0x0E8	ADC Regular Conversion Data Register 14	0x0000_0000
ADCDR15	0x0EC	ADC Regular Conversion Data Register 15	0x0000_0000
ADCHDR0	0x0F0	ADC High Priority Conversion Data Register 0	0x0000_0000
ADCHDR1	0x0F4	ADC High Priority Conversion Data Register 1	0x0000_0000
ADCHDR2	0x0F8	ADC High Priority Conversion Data Register 2	0x0000_0000
ADCHDR3	0x0FC	ADC High Priority Conversion Data Register 3	0x0000_0000
ADCTCR	0x100	ADC Regular Trigger Control Register	0x0000_0000
ADCTS	0x104	ADC Regular Trigger Source Register	0x0000_0000
ADCHTCR	0x110	ADC High Priority Trigger Control Register	0x0000_0000
ADCHTSR	0x114	ADC High Priority Trigger Source Register	0x0000_0000
ADCWCR	0x120	ADC Watchdog Control Register	0x0000_0000
ADCLTR	0x124	ADC Watchdog Lower Threshold Register	0x0000_0000
ADCUTR	0x128	ADC Watchdog Upper Threshold Register	0x0000_0000
ADCIER	0x130	ADC Interrupt Enable Register	0x0000_0000
ADCIRAW	0x134	ADC Interrupt Raw Status Register	0x0000_0000
ADCISR	0x138	ADC Interrupt Status Register	0x0000_0000
ADCICLR	0x13C	ADC Interrupt Clear Register	0x0000_0000
ADCDMAR	0x140	ADC DMA Request Register	0x0000_0000

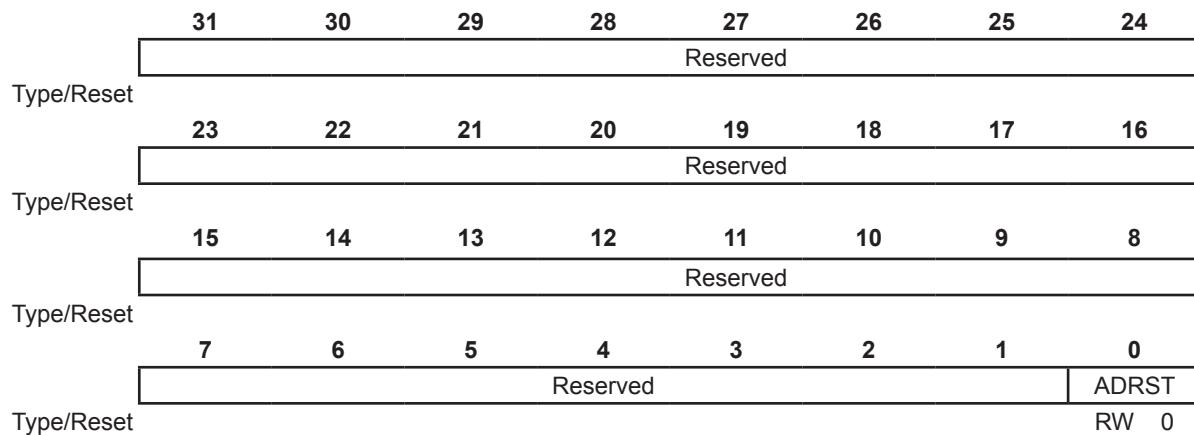
Register Descriptions

ADC Reset Register – ADCRST

ADC software reset register.

Offset: 0x004

Reset value: 0x0000_0000



Bits	Field	Descriptions
[0]	ADRST	ADC Software Reset 0: No effect 1: Reset A/D converter except for the A/D Converter registers.

ADC Regular Conversion Mode Register – ADCCONV

This register specifies the mode setting, queue length, and subgroup length of the ADC regular conversion mode. Note that once the content of ADCCONV is changed, the regular conversion in progress will be aborted and the ADC will be reset. The program will have to wait for at least one ADCLK before issuing the next command.

Offset: 0x008

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Reserved								
Type/Reset	23	22	21	20	19	18	17	16
	Reserved				ADSUBL			
Type/Reset					RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
Type/Reset	Reserved				ADSEQL			
					RW 0	RW 0	RW 0	RW 0
Type/Reset	7	6	5	4	3	2	1	0
	Reserved						ADMODE	
							RW 0	RW 0

Bits	Field	Descriptions
[19:16]	ADSUBL	ADC Regular Conversion Subgroup Length ADSUBL specifies the conversion channel length of each subgroup for the regular discontinuous mode. Length of each subgroup = ADSUBL [3:0]+1. If (ADSEQL [3:0]+1) is not a multiple of (ADSUBL [3:0] + 1), the last subgroup will be shorter than others.
[11:8]	ADSEQL	ADC Regular Conversion Length 0x00: Implement a conversion on the specified channel only (specified by ADSEQ0 in ADCLST0 register). Others: Length of list queue = ADSEQL [3:0] + 1.
[1:0]	ADMODE	ADC Regular Conversion Mode

ADMODE [1:0]	Mode	Descriptions
00	One shot mode	After each trigger, the conversion loops once.
01	Reserved	
10	Continuous mode	After trigger, the conversion loops for the whole sequence continuously until the conversion mode is changed.
11	Discontinuous mode	After each trigger, implement a conversion on the current subgroup. When the last subgroup is finished, the loop restarts from the first subgroup.

ADC High Priority Conversion Mode Register – ADCHCONV

This register specifies the mode setup, queue length, and subgroup length of the ADC high priority conversion mode. Note that once the contents of ADCHCONV have changed, the high priority conversion in progress will be aborted and the ADC will be reset. The program will have to wait for at least one ADCLK before issuing the next command.

Offset: 0x00C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Reserved								
Type/Reset	23	22	21	20	19	18	17	16
	Reserved						ADHSUBL	
Type/Reset	RW	0	RW	0				
	15	14	13	12	11	10	9	8
Type/Reset	Reserved						ADHSEQL	
	RW	0	RW	0				
Type/Reset	7	6	5	4	3	2	1	0
	Reserved						ADHMODE	
	RW	0	RW	0				

Bits	Field	Descriptions															
[17:16]	ADHSUBL	ADC High Priority Conversion Subgroup Length ADHSUBL specifies the conversion channel length of each subgroup for the high priority discontinuous mode. Length of each subgroup = ADHSUBL [1:0] + 1. If (ADHSEQL [1:0] + 1) is not a multiple of (ADHSUBL [1:0] + 1), the last subgroup will be shorter than others.															
[9:8]	ADHSEQL	ADC High Priority Conversion Length 0x00: Implement a conversion on the specified channel only (specified by HSEQ0 in ADCHLST). Others: Length of list queue = ADHSEQL [1:0] + 1.															
[1:0]	ADHMODE	ADC High Priority Conversion Mode <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>ADHMODE [1:0]</th> <th>Mode</th> <th>Descriptions</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>One shot mode</td> <td>After each trigger, the conversion loops once.</td> </tr> <tr> <td>01</td> <td>Reserved</td> <td></td> </tr> <tr> <td>10</td> <td>Continuous mode</td> <td>After a trigger, the conversion loops for the whole sequence continuously until the conversion mode is changed.</td> </tr> <tr> <td>11</td> <td>Discontinuous mode</td> <td>After each trigger, implement a conversion on the current subgroup. When the last subgroup is finished, the loop restarts from the first subgroup.</td> </tr> </tbody> </table>	ADHMODE [1:0]	Mode	Descriptions	00	One shot mode	After each trigger, the conversion loops once.	01	Reserved		10	Continuous mode	After a trigger, the conversion loops for the whole sequence continuously until the conversion mode is changed.	11	Discontinuous mode	After each trigger, implement a conversion on the current subgroup. When the last subgroup is finished, the loop restarts from the first subgroup.
ADHMODE [1:0]	Mode	Descriptions															
00	One shot mode	After each trigger, the conversion loops once.															
01	Reserved																
10	Continuous mode	After a trigger, the conversion loops for the whole sequence continuously until the conversion mode is changed.															
11	Discontinuous mode	After each trigger, implement a conversion on the current subgroup. When the last subgroup is finished, the loop restarts from the first subgroup.															

ADC Regular Conversion List Register 0 – ADCLST0

This register specifies the conversion sequence order No.0 ~ No.3 of the ADC regular group.

Offset: 0x010

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Type/Reset		Reserved		ADSEQ3				
	23	22	21	20	19	18	17	16
Type/Reset		Reserved		ADSEQ2				
	15	14	13	12	11	10	9	8
Type/Reset		Reserved		ADSEQ1				
	7	6	5	4	3	2	1	0
Type/Reset		Reserved		ADSEQ0				
				RW	0	RW	0	RW

Bits	Field	Descriptions
[28:24]	ADSEQ3	ADC Regular Conversion Sequence Select 3 Select the ADC input channel of 3rd sequence in ADC regular conversion mode. 0x0: ADC_IN0 0x1: ADC_IN1 0x2: ADC_IN2 0x3: ADC_IN3 0x4: ADC_IN4 0x5: ADC_IN5 0x6: ADC_IN6 0x7: ADC_IN7 0x8: ADC_IN8 0x9: ADC_IN9 0xA: ADC_IN10 0xB: ADC_IN11 0xC: ADC_IN12 0xD: ADC_IN13 0xE: ADC_IN14 0xF: ADC_IN15 0x10: Analog ground, AVSS (VREF-) 0x11: Analog power, AVDD (VREF+) 0x12 ~ 0x1F: Invalid setting. These values must not be selected as they may cause ADC instability.
[20:16]	ADSEQ2	ADC Regular Conversion Sequence Select 2
[12:8]	ADSEQ1	ADC Regular Conversion Sequence Select 1
[4:0]	ADSEQ0	ADC Regular Conversion Sequence Select 0

ADC Regular Conversion List Register 1 – ADCLST1

This register specifies the conversion sequence order No.4 ~ No.7 of the ADC regular group.

Offset: 0x014

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24		
Type/Reset		Reserved				ADSEQ7				
	23	22	21	20	19	18	17	16		
Type/Reset		Reserved				ADSEQ6				
	15	14	13	12	11	10	9	8		
Type/Reset		Reserved				ADSEQ5				
	7	6	5	4	3	2	1	0		
Type/Reset		Reserved				ADSEQ4				

Bits	Field	Descriptions
[28:24]	ADSEQ7	ADC Regular Conversion Sequence Select 7 Select the ADC input channel of 7th sequence in ADC regular conversion mode. 0x0: ADC_IN0 0x1: ADC_IN1 0x2: ADC_IN2 0x3: ADC_IN3 0x4: ADC_IN4 0x5: ADC_IN5 0x6: ADC_IN6 0x7: ADC_IN7 0x8: ADC_IN8 0x9: ADC_IN9 0xA: ADC_IN10 0xB: ADC_IN11 0xC: ADC_IN12 0xD: ADC_IN13 0xE: ADC_IN14 0xF: ADC_IN15 0x10: Analog ground, AVSS (VREF-) 0x11: Analog power, AVDD (VREF+) 0x12 ~ 0x1F: Invalid setting. These values must not be selected as they may cause ADC instability.
[20:16]	ADSEQ6	ADC Regular Conversion Sequence Select 6
[12:8]	ADSEQ5	ADC Regular Conversion Sequence Select 5
[4:0]	ADSEQ4	ADC Regular Conversion Sequence Select 4

ADC Regular Conversion List Register 2 – ADCLST2

This register specifies the conversion sequence order No.8 ~ No.11 of the ADC regular group.

Offset: 0x018

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24		
Type/Reset		Reserved				ADSEQ11				
	23	22	21	20	19	18	17	16		
Type/Reset		Reserved				ADSEQ10				
	15	14	13	12	11	10	9	8		
Type/Reset		Reserved				ADSEQ9				
	7	6	5	4	3	2	1	0		
Type/Reset		Reserved				ADSEQ8				

Bits	Field	Descriptions
[28:24]	ADSEQ11	ADC Regular Conversion Sequence Select 11 Select ADC input channel of 11th sequence in the ADC regular conversion mode. 0x0: ADC_IN0 0x1: ADC_IN1 0x2: ADC_IN2 0x3: ADC_IN3 0x4: ADC_IN4 0x5: ADC_IN5 0x6: ADC_IN6 0x7: ADC_IN7 0x8: ADC_IN8 0x9: ADC_IN9 0xA: ADC_IN10 0xB: ADC_IN11 0xC: ADC_IN12 0xD: ADC_IN13 0xE: ADC_IN14 0xF: ADC_IN15 0x10: Analog ground, AVSS (VREF-) 0x11: Analog power, AVDD (VREF+) 0x12 ~ 0x1F: Invalid setting. These values must not be selected as they may cause ADC instability.
[20:16]	ADSEQ10	ADC Regular Conversion Sequence Select 10
[12:8]	ADSEQ9	ADC Regular Conversion Sequence Select 9
[4:0]	ADSEQ8	ADC Regular Conversion Sequence Select 8

ADC Regular Conversion List Register 3 – ADCLST3

This register specifies the conversion sequence order No.12 ~ No.15 of the ADC regular group.

Offset: 0x01C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24		
Type/Reset		Reserved				ADSEQ15				
	23	22	21	20	19	18	17	16		
Type/Reset		Reserved				ADSEQ14				
	15	14	13	12	11	10	9	8		
Type/Reset		Reserved				ADSEQ13				
	7	6	5	4	3	2	1	0		
Type/Reset		Reserved				ADSEQ12				

Bits	Field	Descriptions
[28:24]	ADSEQ15	ADC Regular Conversion Sequence Select 15 Select the ADC input channel of 15th sequence in ADC regular conversion mode. 0x0: ADC_IN0 0x1: ADC_IN1 0x2: ADC_IN2 0x3: ADC_IN3 0x4: ADC_IN4 0x5: ADC_IN5 0x6: ADC_IN6 0x7: ADC_IN7 0x8: ADC_IN8 0x9: ADC_IN9 0xA: ADC_IN10 0xB: ADC_IN11 0xC: ADC_IN12 0xD: ADC_IN13 0xE: ADC_IN14 0xF: ADC_IN15 0x10: Analog ground, AVSS (VREF-) 0x11: Analog power, AVDD (VREF+) 0x12 ~ 0x1F: Invalid setting. These values must not be selected as they may cause ADC instability
[20:16]	ADSEQ14	ADC Regular Conversion Sequence Select 14
[12:8]	ADSEQ13	ADC Regular Conversion Sequence Select 13
[4:0]	ADSEQ12	ADC Regular Conversion Sequence Select 12

ADC High Priority Conversion List Register – ADCHLST

This register specifies the conversion sequence order No.0 ~ No.3 of the ADC high priority group.

Offset: 0x020

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24		
Type/Reset		Reserved				ADHSEQ3				
	23	22	21	20	19	18	17	16		
Type/Reset		Reserved				ADHSEQ2				
	15	14	13	12	11	10	9	8		
Type/Reset		Reserved				ADHSEQ1				
	7	6	5	4	3	2	1	0		
Type/Reset		Reserved				ADHSEQ0				

Bits	Field	Descriptions
[28:24]	ADHSEQ3	ADC High Priority Conversion Sequence Select 3 Select the ADC input channel of 3rd sequence in ADC high priority conversion mode. 0x0: ADC_IN0 0x1: ADC_IN1 0x2: ADC_IN2 0x3: ADC_IN3 0x4: ADC_IN4 0x5: ADC_IN5 0x6: ADC_IN6 0x7: ADC_IN7 0x8: ADC_IN8 0x9: ADC_IN9 0xA: ADC_IN10 0xB: ADC_IN11 0xC: ADC_IN12 0xD: ADC_IN13 0xE: ADC_IN14 0xF: ADC_IN15 0x10: Analog ground, AVSS (VREF-) 0x11: Analog power, AVDD (VREF+) 0x12 ~ 0x1F: Invalid setting. Don't set these value, it maybe cause the ADC operation become abnormally.
[20:16]	ADHSEQ2	ADC High Priority Conversion Sequence Select 2
[12:8]	ADHSEQ1	ADC High Priority Conversion Sequence Select 1
[4:0]	ADHSEQ0	ADC High Priority Conversion Sequence Select 0

ADC Input Offset Register n – ADCOFRn, n = 0 ~ 15

This register specifies the ADC input channel n offset together with the offset cancellation function enable control.

Offset: 0x030 ~ 0x06C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24	
Type/Reset	Reserved								
	23	22	21	20	19	18	17	16	
Type/Reset	Reserved								
	15	14	13	12	11	10	9	8	
Type/Reset	ADOFEn	ADALn	Reserved			ADOFn			
	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	
	7	6	5	4	3	2	1	0	
Type/Reset	ADOFn								
	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	

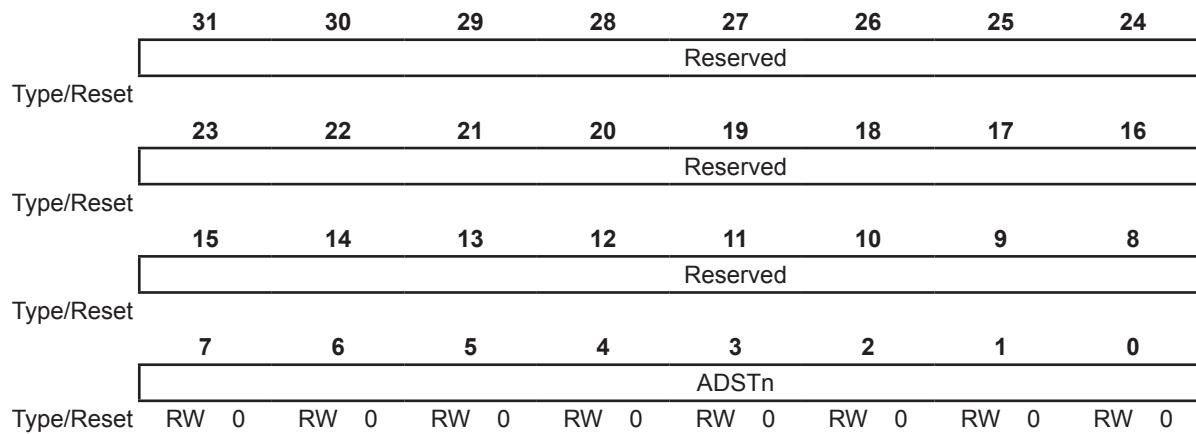
Bits	Field	Descriptions
[15]	ADOFEn	ADC Input Channel n Offset Cancellation Enable (n = 0 ~ 15) 0: ADC_INn offset cancellation is disabled. 1: ADC_INn offset cancellation is enabled.
[14]	ADALn	ADC Input Channel n Data Alignment (n = 0 ~ 15) 0: Right aligned 1: Left aligned
[11:0]	ADOFn	ADC Input Channel n Offset Value (n = 0 ~ 15) The data values read from ADC data registers (ADCDR) which are the raw data from the ADC conversion engine minus this offset on Channel n (ADC_INn) after format transfer.

ADC Input Sampling Time Register n – ADCSTRn, n = 0 ~ 15

This register specifies the sampling time of ADC channel n.

Offset: 0x070 ~ 0x0AC

Reset value: 0x0000_0000



Bits	Field	Descriptions
[7:0]	ADSTn	ADC Input Channel n Sampling Time (n = 0 ~ 15) Sampling time = (STn [7:0] + 1.5) ADC clocks.

ADC Regular Conversion Data Register y – ADCDRy, y = 0 ~ 15

This register specifies the regular conversion data of ADC SEQy.

Offset: 0x0B0 ~ 0x0EC

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Type/Reset	ADVLDy				Reserved			
	RC	0						
	23	22	21	20	19	18	17	16
Type/Reset					Reserved			
	15	14	13	12	11	10	9	8
Type/Reset	RO	0	RO	0	RO	0	RO	0
	7	6	5	4	3	2	1	0
Type/Reset	RO	0	RO	0	RO	0	RO	0
					ADDy			
Type/Reset	RO	0	RO	0	RO	0	RO	0
					ADDy			
Type/Reset	RO	0	RO	0	RO	0	RO	0

Bits	Field	Descriptions
[31]	ADVLDy	ADC Regular Conversion Data of SEQy Valid Bit (y = 0 ~ 15) 0: Data is invalid or has been read 1: New data is valid
[15:0]	ADDy	ADC Regular Conversion Data of SEQy (y = 0 ~ 15) The regular conversion result of SEQy in ADCLST register

ADC High Priority Conversion Data Register y – ADCHDRy, y = 0 ~ 3

This register specifies the regular conversion data of ADC HSEQy.

Offset: 0x0F0 ~ 0x0FC

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Type/Reset	ADHVLDy				Reserved			
	RC	0						
Type/Reset	23	22	21	20	19	18	17	16
					Reserved			
Type/Reset	15	14	13	12	11	10	9	8
					ADHDy			
Type/Reset	RO	0	RO	0	RO	0	RO	0
	7	6	5	4	3	2	1	0
Type/Reset	RO	0	RO	0	RO	0	RO	0
					ADHDy			
Type/Reset	RO	0	RO	0	RO	0	RO	0

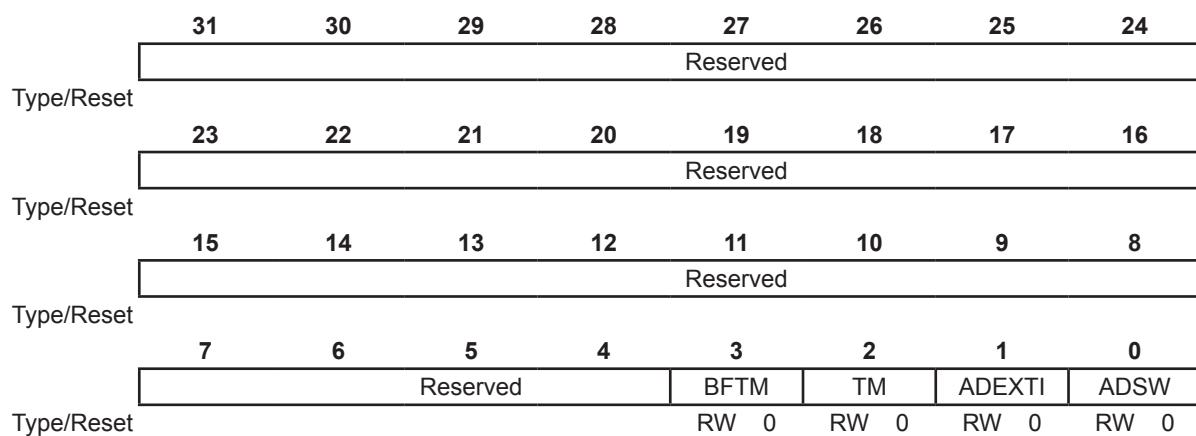
Bits	Field	Descriptions
[31]	ADHVLDy	ADC High Priority Conversion Data of HSEQy Valid Bit (y = 0 ~ 3) 0: Data is invalid or has been read 1: New data is valid
[15:0]	ADHDy	ADC High Priority Conversion Data of HSEQy (y = 0 ~ 3) The regular conversion result of HSEQn in the ADCHLST register

ADC Regular Trigger Control Register – ADCTCR

This register contains the ADC start conversion trigger enable bits of the regular conversion.

Offset: 0x100

Reset value: 0x0000_0000



Bits	Field	Descriptions
[3]	BFTM	ADC Regular Conversion Trigger by BFTM Event 0: Disable regular conversion trigger by BFTM function 1: Enable regular conversion trigger by BFTM function
[2]	TM	ADC Regular Conversion Trigger by GPTM or MCTM Event 0: Disable regular conversion trigger by GPTM or MCTM function 1: Enable regular conversion trigger by GPTM or MCTM function
[1]	ADEXTI	ADC Regular Conversion Trigger by EXTI Event 0: Disable regular conversion trigger by EXTI function 1: Enable regular conversion trigger by EXTI function
[0]	ADSW	ADC Regular Conversion Trigger by Software 0: Disable regular conversion trigger by software function 1: Enable regular conversion trigger by software function

ADC Regular Trigger Source Register – ADCTSR

This register contains the trigger source selection and the software trigger bit of the regular conversion.

Offset: 0x104

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Type/Reset	Reserved							TME
	23	22	21	20	19	18	17	16
Type/Reset	Reserved							TMS
	15	14	13	12	11	10	9	8
Type/Reset	Reserved							ADEXTIS
	7	6	5	4	3	2	1	0
Type/Reset	Reserved							ADSC
								RW 0

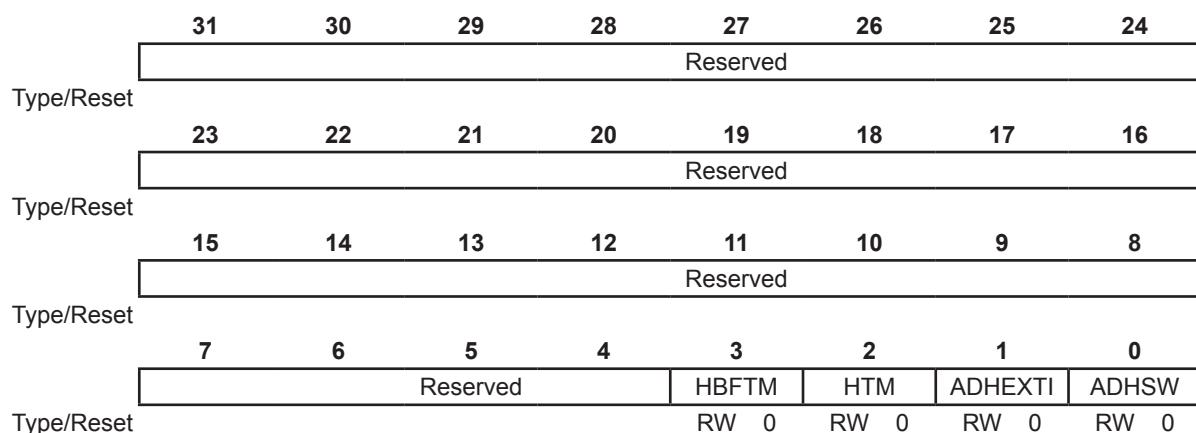
Bits	Field	Descriptions
[26:24]	TME	GPTM or MCTM Trigger Event Selection of the ADC Regular Conversion 000: GPTM or MCTM MTO event 001: GPTM or MCTM CH0O event 010: GPTM or MCTM CH1O event 011: GPTM or MCTM CH2O event 100: GPTM or MCTM CH3O event Others: Reserved - must not be used, or results will be unpredictable
[19]	BFTMS	BFTM Trigger Timer Selection of ADC Regular Conversion 0: BFTM0 1: BFTM1
[18:16]	TMS	GPTM or MCTM Trigger Timer Selection of ADC Regular Conversion 000: MCTM0 001: MCTM1 010: GPTM0 011: GPTM1 Others: Reserved - must not be used, or results will be unpredictable
[11:8]	ADEXTIS	EXTI Trigger Source Selection of ADC Regular Conversion 0x00: EXTI line 0 0x01: EXTI line 1 ... 0x0F: EXTI line 15
[0]	ADSC	ADC Regular Conversion Software Trigger Bit 0: Reset 1: Start regular conversion immediately Set by software to start regular conversion manually. Cleared by hardware after conversion starts.

ADC High Priority Trigger Control Register – ADCHTCR

This register contains the ADC start conversion trigger enable bits of the high priority conversion.

Offset: 0x110

Reset value: 0x0000_0000



Bits	Field	Descriptions
[3]	HBFTM	ADC High Priority Conversion Trigger by BFTM Event 0: Disable high priority conversion trigger by BFTM function 1: Enable high priority conversion trigger by BFTM function
[2]	HTM	ADC High Priority Conversion Trigger by GPTM or MCTM Event 0: Disable high priority conversion trigger by GPTM or MCTM function 1: Enable high priority conversion trigger by GPTM or MCTM function
[1]	ADHEXTI	ADC High Priority Conversion Trigger by EXTI Event 0: Disable high priority conversion trigger by EXTI function 1: Enable high priority conversion trigger by EXTI function
[0]	ADHSW	ADC High Priority Conversion Trigger by Software 0: Disable high priority conversion trigger by software function 1: Enable high priority conversion trigger by software function

ADC High Priority Trigger Source Register – ADCHTSR

This register contains the trigger source selection and the software trigger bit of the high priority conversion.

Offset: 0x114

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Type/Reset	Reserved							
						RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
Type/Reset	Reserved							
					HBFTMS	HTMS		
						RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
Type/Reset	Reserved							
						RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
Type/Reset	Reserved							
							ADHSC	
								RW 0

Bits	Field	Descriptions
[26:24]	HTME	GPTM or MCTM Trigger Event Selection of ADC High Priority Conversion 000: GPTM or MCTM MTO event 001: GPTM or MCTM CH0O event 010: GPTM or MCTM CH1O event 011: GPTM or MCTM CH2O event 100: GPTM or MCTM CH3O event Others: Reserved - must not be used, or results will be unpredictable
[19]	HBFTMS	BFTM Trigger Timer Selection of ADC High Priority Conversion 0: BFTM0 1: BFTM1
[18:16]	HTMS	GPTM or MCTM Trigger Timer Selection of ADC High Priority Conversion 000: MCTM0 001: MCTM1 010: GPTM0 011: GPTM1 Others: Reserved - must not be used, or results will be unpredictable
[11:9]	ADHEXTIS	EXTI Trigger Source Selection of ADC High Priority Conversion 0x00: EXTI line 0 0x01: EXTI line 1 ... 0x0F: EXTI line 15
[0]	ADHSC	ADC High Priority Conversion Software Trigger Bit 0: Reset 1: Start high priority conversion immediately Set by software to start high priority conversion manually. Cleared by hardware after conversion starts.

ADC Watchdog Control Register – ADCWCR

This register provides the control bits and status of the ADC watchdog function.

Offset: 0x120

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24	
Type/Reset				Reserved	ADUCH				
					RO 0	RO 0	RO 0	RO 0	
	23	22	21	20	19	18	17	16	
Type/Reset				Reserved	ADLCH				
					RO 0	RO 0	RO 0	RO 0	
	15	14	13	12	11	10	9	8	
Type/Reset				Reserved	ADWCH				
					RW 0	RW 0	RW 0	RW 0	
	7	6	5	4	3	2	1	0	
Type/Reset				Reserved	ADWALL	ADWUE	ADWLE		
					RW 0	RW 0	RW 0		

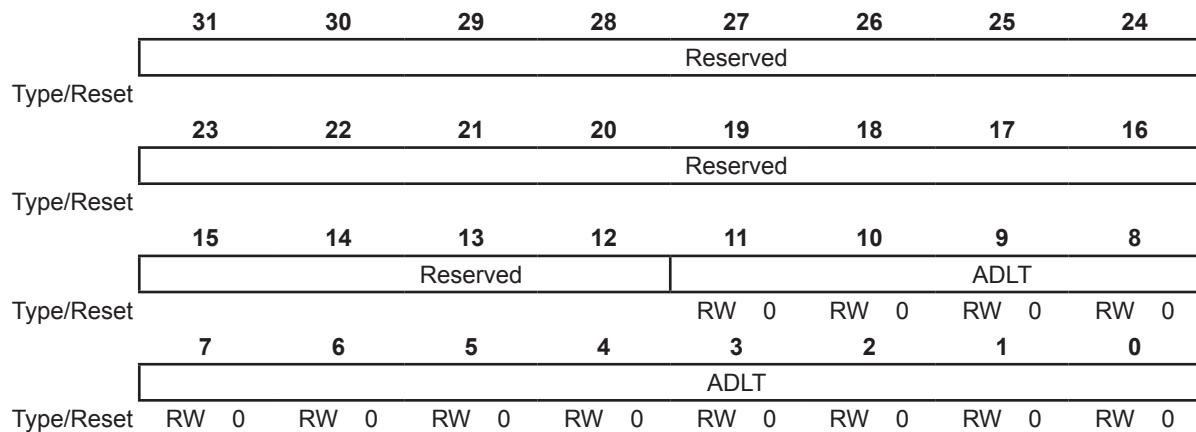
Bits	Field	Descriptions
[27:24]	ADUCH	Upper Threshold Channel Status 0000: ADC_IN0 is higher then ADCWUTR 0001: ADC_IN1 is higher then ADCWUTR ... 1111: ADC_IN15 is higher then ADCWUTR Others: Reserved
[19:16]	ADLCH	Lower Threshold Channel Status 0000: ADC_IN0 is lower then ADCWLTR 0001: ADC_IN1 is lower then ADCWLTR ... 1111: ADC_IN15 is lower then ADCWLTR Others: Reserved
[11:8]	ADWCH	ADC Watchdog Specific Channel Selection 0000: ADC_IN0 is monitored 0001: ADC_IN1 is monitored ... 1111: ADC_IN15 is monitored Others: Reserved
[2]	ADWALL	ADC Watchdog Specific/All Channel Setting 0: Only the channel which specified by the ASWCH field is monitored 1: All channels are monitored
[1]	ADWUE	ADC Watchdog Upper Threshold Enable Bit 0: Disable upper threshold function 1: Enable upper threshold function
[0]	ADWLE	ADC Watchdog Lower Threshold Enable Bit 0: Disable lower threshold function 1: Enable lower threshold function

ADC Watchdog Lower Threshold Register – ADCLTR

This register specifies the lower threshold of the ADC watchdog function.

Offset: 0x124

Reset value: 0x0000_0000



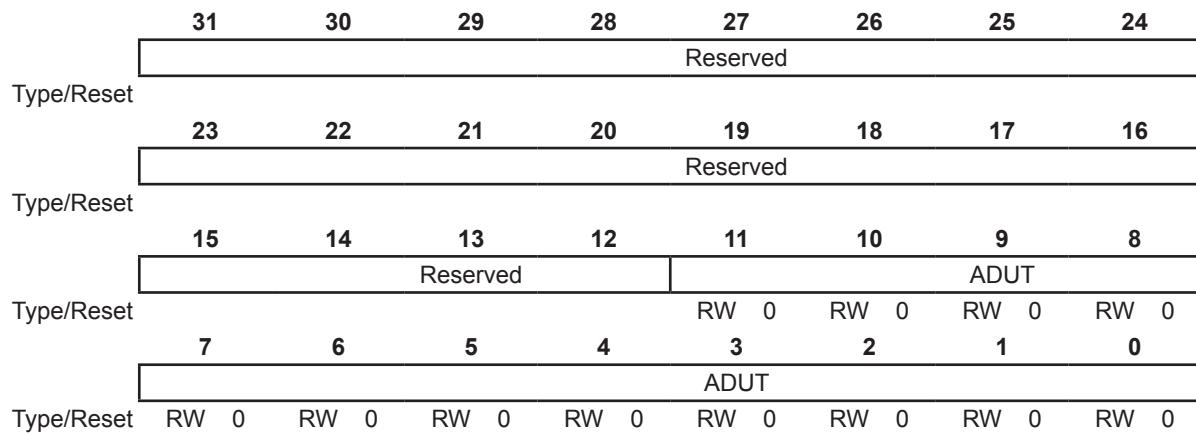
Bits	Field	Descriptions
[11:0]	ADLT	ADC Watchdog Lower Threshold Value Specify lower threshold of ADC result data.

ADC Watchdog Upper Threshold Register – ADCUTR

This register specifies the upper threshold of the ADC watchdog function.

Offset: 0x128

Reset value: 0x0000_0000



Bits	Field	Descriptions
[11:0]	ADUT.	ADC Watchdog Upper Threshold Value Specify upper threshold of ADC result data.

ADC Interrupt Enable Register – ADCIER

This register contains the ADC interrupt enable bits.

Offset: 0x130

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Type/Reset	Reserved					ADIEHO	ADIEO	
	23	22	21	20	19	18	17	16
Type/Reset	Reserved					ADIEU	ADIEL	
	15	14	13	12	11	10	9	8
Type/Reset	Reserved					ADIEHC	ADIEHG	ADIEHS
	7	6	5	4	3	2	1	0
Type/Reset	Reserved					ADIEC	ADIEG	ADIES
						RW 0	RW 0	RW 0

Bits	Field	Descriptions
[25]	ADIEHO	ADC High Priority Data Register Overwrite Interrupt Enable 0: ADC high priority data register overwrite interrupt is disabled 1: ADC high priority data register overwrite interrupt is enabled
[24]	ADIEO	ADC Regular Data Register Overwrite Interrupt Enable 0: ADC regular data register overwrite interrupt is disabled 1: ADC regular data register overwrite interrupt is enabled
[17]	ADIEU	ADC Watchdog Upper Threshold Interrupt Enable 0: ADC watchdog upper threshold interrupt is disabled 1: ADC watchdog upper threshold interrupt is enabled
[16]	ADIEL	ADC Watchdog Lower Threshold Interrupt Enable 0: ADC watchdog lower threshold interrupt is disabled 1: ADC watchdog lower threshold interrupt is enabled
[10]	ADIEHC	ADC High Priority Cycle EOC Interrupt Enable 0: ADC high priority cycle end of conversion interrupt is disabled 1: ADC high priority cycle end of conversion interrupt is enabled
[9]	ADIEHG	ADC High Priority Subgroup EOC Interrupt Enable 0: ADC high priority subgroup end of conversion interrupt is disabled 1: ADC high priority subgroup end of conversion interrupt is enabled
[8]	ADIEHS	ADC High Priority Single EOC Interrupt Enable 0: ADC high priority single end of conversion interrupt is disabled 1: ADC high priority single end of conversion interrupt is enabled
[2]	ADIEC	ADC Regular Cycle EOC Interrupt Enable 0: ADC regular cycle end of conversion interrupt is disabled 1: ADC regular cycle end of conversion interrupt is enabled
[1]	ADIEG	ADC Regular Subgroup EOC Interrupt Enable 0: ADC regular subgroup end of conversion interrupt is disabled 1: ADC regular subgroup end of conversion interrupt is enabled
[0]	ADIES	ADC Regular Single EOC Interrupt Enable 0: ADC regular single end of conversion interrupt is disabled 1: ADC regular single end of conversion interrupt is enabled

ADC Interrupt Raw Status Register – ADCIRAW

This register contains the ADC interrupt raw status bits.

Offset: 0x134

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Type/Reset				Reserved				
						ADIRAWHO	ADIRAWO	
	23	22	21	20	19	18	17	16
Type/Reset				Reserved				
						ADIRAWU	ADIRAWL	
	15	14	13	12	11	10	9	8
Type/Reset				Reserved			ADIRAWHC	ADIRAWHG
							ADIRAWHS	
	7	6	5	4	3	2	1	0
Type/Reset				Reserved			ADIRAWC	ADIRAWG
							ADIRAWS	
						RO 0	RO 0	RO 0

Bits	Field	Descriptions
[25]	ADIRAWHO	ADC High Priority Data Register Overwrite Interrupt Raw Status 0: ADC high priority data register overwrite interrupt has not occurred 1: ADC high priority data register overwrite interrupt has occurred
[24]	ADIRAWO	ADC Regular Data Register Overwrite Interrupt Raw Status 0: ADC regular data register overwrite interrupt has not occurred 1: ADC regular data register overwrite interrupt has occurred
[17]	ADIRAWU	ADC Watchdog Upper Threshold Interrupt Raw Status 0: ADC watchdog upper threshold interrupt has not occurred 1: ADC watchdog upper threshold interrupt has occurred
[16]	ADIRAWL	ADC Watchdog Lower Threshold Interrupt Raw Status 0: ADC watchdog lower threshold interrupt has not occurred 1: ADC watchdog lower threshold interrupt has occurred
[10]	ADIRAWHC	ADC High Priority Cycle EOC Interrupt Raw Status 0: ADC high priority cycle end of conversion interrupt has not occurred 1: ADC high priority cycle end of conversion interrupt has occurred
[9]	ADIRAWHG	ADC High Priority Subgroup EOC Interrupt Raw Status 0: ADC high priority subgroup end of conversion interrupt has not occurred 1: ADC high priority subgroup end of conversion interrupt has occurred
[8]	ADIRAWHS	ADC High Priority Single EOC Interrupt Raw Status 0: ADC high priority single end of conversion interrupt has not occurred 1: ADC high priority single end of conversion interrupt has occurred
[2]	ADIRAWC	ADC Regular Cycle EOC Interrupt Raw Status 0: ADC regular cycle end of conversion interrupt has not occurred 1: ADC regular cycle end of conversion interrupt has occurred
[1]	ADIRAWG	ADC Regular Subgroup EOC Interrupt Raw Status 0: ADC regular subgroup end of conversion interrupt has not occurred 1: ADC regular subgroup end of conversion interrupt has occurred
[0]	ADIRAWS	ADC Regular Single EOC Interrupt Raw Status 0: ADC regular single end of conversion interrupt has not occurred 1: ADC regular single end of conversion interrupt has occurred

ADC Interrupt Status Register – ADCISR

This register contains the ADC interrupt status bits. The corresponding status will be set to 1 if the associated interrupt event occurs and the related enable bit is set to 1.

Offset: 0x138

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Type/Reset				Reserved				
						ADISHO	ADISO	
	23	22	21	20	19	18	17	16
Type/Reset				Reserved				
						ADISU	ADISL	
	15	14	13	12	11	10	9	8
Type/Reset				Reserved			ADISHC	ADISHG
							ADISHS	
						RO 0	RO 0	RO 0
Type/Reset	7	6	5	4	3	2	1	0
				Reserved			ADISC	ADISG
							ADISS	
						RO 0	RO 0	RO 0

Bits	Field	Descriptions
[25]	ADISHO	ADC High Priority Data Register Overwrite Interrupt Status 0: ADC high priority data register overwrite interrupt has not occurred 1: ADC high priority data register overwrite interrupt has occurred
[24]	ADISO	ADC Regular Data Register Overwrite Interrupt Status 0: ADC regular data register overwrite interrupt has not occurred 1: ADC regular data register overwrite interrupt has occurred
[17]	ADISU	ADC Watchdog Upper Threshold Interrupt Status 0: ADC watchdog upper threshold interrupt has not occurred 1: ADC watchdog upper threshold interrupt has occurred
[16]	ADISL	ADC Watchdog Lower Threshold Interrupt Status 0: ADC watchdog lower threshold interrupt has not occurred 1: ADC watchdog lower threshold interrupt has occurred
[10]	ADISHC	ADC High Priority Cycle EOC Interrupt Status 0: ADC high priority cycle end of conversion interrupt has not occurred 1: ADC high priority cycle end of conversion interrupt has occurred
[9]	ADISHG	ADC High Priority Subgroup EOC Interrupt Status 0: ADC high priority subgroup end of conversion interrupt has not occurred 1: ADC high priority subgroup end of conversion interrupt has occurred
[8]	ADISHS	ADC High Priority Single EOC Interrupt Status 0: ADC high priority single end of conversion interrupt has not occurred 1: ADC high priority single end of conversion interrupt has occurred
[2]	ADISC	ADC Regular Cycle EOC Interrupt Status 0: ADC regular cycle end of conversion interrupt has not occurred 1: ADC regular cycle end of conversion interrupt has occurred
[1]	ADISG	ADC Regular Subgroup EOC Interrupt Status 0: ADC regular subgroup end of conversion interrupt has not occurred 1: ADC regular subgroup end of conversion interrupt has occurred
[0]	ADISS	ADC Regular Single EOC Interrupt Status 0: ADC regular single end of conversion interrupt has not occurred 1: ADC regular single end of conversion interrupt has occurred

ADC Interrupt Clear Register – ADCICLR

This register provides the clear bits used to clear the interrupt raw and interrupt status of the ADC. These bits are set to 1 by software to clear the interrupt status and automatically cleared to 0 by hardware after being set to 1.

Offset: 0x13C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Type/Reset				Reserved				
	23	22	21	20	19	18	17	16
Type/Reset				Reserved				
	15	14	13	12	11	10	9	8
Type/Reset				Reserved				
	7	6	5	4	3	2	1	0
Type/Reset				Reserved				
						ADICLRC	ADICLRG	ADICLRS
						WO 0	WO 0	WO 0

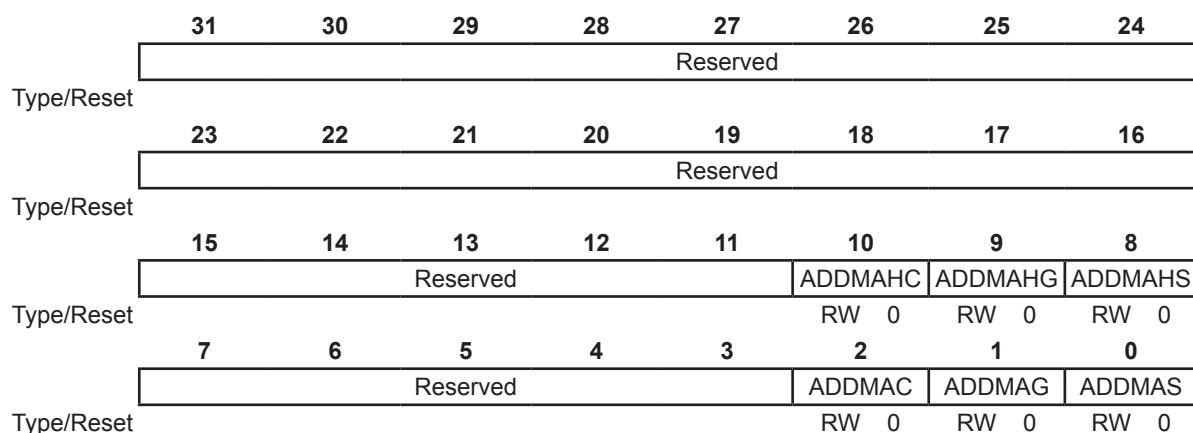
Bits	Field	Descriptions
[25]	ADICLRO	ADC High Priority Data Register Overwrite Interrupt Status Clear Bit 0: No effect 1: Clear ADIEHO
[24]	ADICLRO	ADC Regular Data Register Overwrite Interrupt Status Clear Bit 0: No effect 1: Clear ADIEO
[17]	ADICLRU	ADC Watchdog Upper Threshold Interrupt Status Clear Bit 0: No effect 1: Clear ADIEU
[16]	ADICLRL	ADC Watchdog Lower Threshold Interrupt Status Clear Bit 0: No effect 1: Clear ADIEL
[10]	ADICLRHC	ADC High Priority Cycle EOC Interrupt Status Clear Bit 0: No effect 1: Clear ADIEHC
[9]	ADICLRHG	ADC High Priority Subgroup EOC Interrupt Status Clear Bit 0: No effect 1: Clear ADIEHG
[8]	ADICLRHS	ADC High Priority Single EOC Interrupt Status Clear Bit 0: No effect 1: Clear ADIEHS
[2]	ADICLRC	ADC Regular Cycle EOC Interrupt Status Clear Bit 0: No effect 1: Clear ADIEC
[1]	ADICLRG	ADC Regular Subgroup EOC Interrupt Status Clear Bit 0: No effect 1: Clear ADIEG
[0]	ADICLRS	ADC Regular Single EOC Interrupt Status Clear Bit 0: No effect 1: Clear ADIES

ADC DMA Request Register – ADCDMAR

This register contains the ADC DMA request enable bits.

Offset: 0x140

Reset value: 0x0000_0000



Bits	Field	Descriptions
[10]	ADDMAHC	ADC High Priority Cycle EOC DMA Request Enable Bit 0: ADC high priority cycle end of conversion DMA request is disabled 1: ADC high priority cycle end of conversion DMA request is enabled
[9]	ADDMAHG	ADC High Priority Subgroup EOC DMA Request Enable Bit 0: ADC high priority subgroup end of conversion DMA request is disabled 1: ADC high priority subgroup end of conversion DMA request is enabled
[8]	ADDMAHS	ADC High Priority Single EOC DMA Request Enable Bit 0: ADC high priority single end of conversion DMA request is disabled 1: ADC high priority single end of conversion DMA request is enabled
[2]	ADDMAC	ADC Regular Cycle EOC DMA Request Enable Bit 0: ADC regular cycle end of conversion DMA request is disabled 1: ADC regular cycle end of conversion DMA request is enabled
[1]	ADDMAHG	ADC Regular Subgroup EOC DMA Request Enable Bit 0: ADC regular subgroup end of conversion DMA request is disabled 1: ADC regular subgroup end of conversion DMA request is enabled
[0]	ADDMAS	ADC Regular Single EOC DMA Request Enable Bit 0: ADC regular single end of conversion DMA request is disabled 1: ADC regular single end of conversion DMA request is enabled

13 Operational Amplifier/Comparator (OPA/CMP)

Introduction

Two Operational Amplifiers/Comparators, OPA/CMP, are implemented within the devices. They can be configured either as Operational Amplifiers or Analog Comparators. When configured as a comparators, they are capable of asserting interrupts to the NVIC.

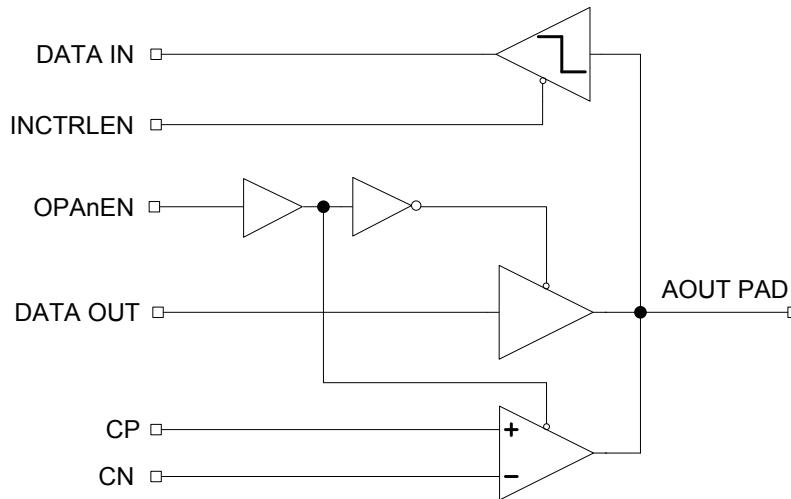


Figure 31. Simplified Block Diagram of OPA/CMP with Digital I/O

Features

- Operational Amplifier or Comparator function determined by software
- Supply Voltage Range: 2.7 V ~ 3.6 V
- Typical Operating Current: 230 μ A (@V_{DD} = 3.3 V and Room Temperature = 25°C)
- Power Down Supply Current (OPAnEN = 0 and AnOFM = 0): < 0.1 μ A
- Comparator Offset (After Calibration): < \pm 1 mV
- Comparator Response Time: < 2 μ s (@ overdrive voltage = 10 mV)

Functional Descriptions

Function Diagram

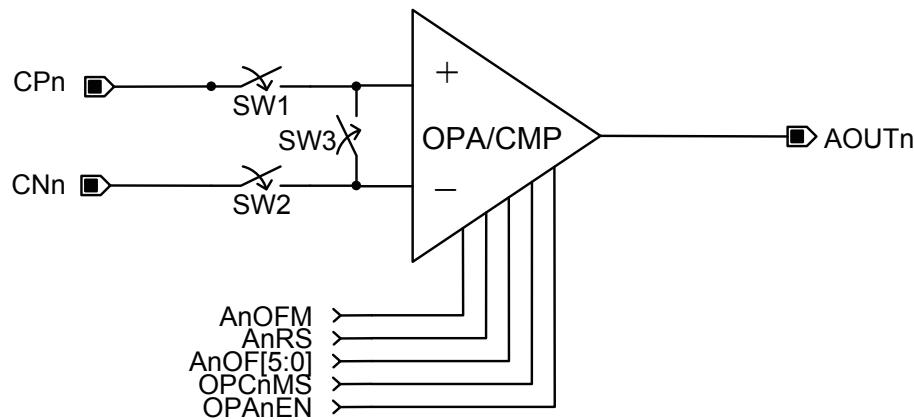


Figure 32. OPA/CMP Functional Diagram

Table 29. OPA/CMP Functional Signal Definition

AnOFM	AnRS	SW1	SW2	SW3
0	X	ON	ON	OFF
1	0	OFF	ON	ON
1	1	ON	OFF	ON

Interrupts and Status

The analog comparator can be generated an interrupt when its output waveform generates a rising or falling edge and its corresponding interrupt enables control bit is also set.

For example, when a comparator output rising edge occurs, the comparator rising edge raw flag CRnRAW in the Comparator Raw Status Register CMPRSRn will be set. If the comparator output rising edge interrupt enable control bit CRnIEN in the Comparator Interrupt Enable Register CMPIERn is enabled, the comparator output rising edge masked interrupt status bit CRnIS in the Comparator Masked Interrupt Status Register CMPISRn, will be set when the comparator output rising edge occurs. An interrupt will then be generated and sent to the NVIC unit. Writing “1” into the comparator output rising edge interrupt clear bit CRnICLR in the Comparator Interrupt Clear Register CMPICLRn will clear the CRnIS and CRnRAW status bits. The comparator output falling edge interrupt also has the same corresponding interrupt setting.

Offset Cancellation Procedures

The device provides an offset cancellation function. Users can cancel the input voltage offset by using a specific procedure by configuring the corresponding registers. The offset cancellation procedure is shown in the following steps.

Cancellation procedure

1. Set the AnOFM bit in the OPACRn register to 1 to enter the offset cancellation mode.
2. Configure the AnRS bit in the OPACRn register to select whether the reference voltage input comes from the comparator negative or positive input pin. If the AnRS bit is set to 1, the reference voltage input will come from the comparator positive input pin. Otherwise, the reference voltage input will come from the comparator negative input pin when the AnRS bit is cleared to 0.
3. Specify the OFVCRn register with a value of 0x00 to start the cancellation procedure.
4. If the CMPnS bit in the OPACRn register is equal to 0, then increase the OFVCRn register content, AnOF, by 1 and check whether the CMPnS bit state has changed from 0 to 1. If not, then keep increasing the register content until the CMPnS bit state changes from 0 to 1.
5. When the CMPnS bit changes to 1, then the AnOF data which is equal to N or (N-1) is the specific value written into the OFVCRn register to cancel the comparator input offset voltage.

Note that the reference input voltage must be in the range from ($V_{DDA}-1.2V$) to ($V_{SSA}+0.5V$) to obtain a more accurate cancellation result.

Register Map

The following table shows the OPA/CMP registers and reset values.

Table 30. OPA/CMP Register Map

Register	Offset	Description	Reset Value
OPACMP Base Address = 0x4001_8000			
OPACR0	0x000	Operational Amplifier Control Register 0	0x0000_0000
OFVCR0	0x004	Comparator Input Offset Voltage Cancellation Register 0	0x0000_0000
CMPIER0	0x008	Comparator Interrupt Enable Register 0	0x0000_0000
CMPRSR0	0x00C	Comparator Raw Status Register 0	0x0000_0000
CMPISR0	0x010	Comparator Masked Interrupt Status Register 0	0x0000_0000
CMPICLR0	0x014	Comparator Interrupt Clear Register 0	NA
OPACR1	0x100	Operational Amplifier Control Register 1	0x0000_0000
OFVCR1	0x104	Comparator Input Offset Voltage Cancellation Register 1	0x0000_0000
CMPIER1	0x108	Comparator Interrupt Enable Register 1	0x0000_0000
CMPRSR1	0x10C	Comparator Raw Status Register 1	0x0000_0000
CMPISR1	0x110	Comparator Masked Interrupt Status Register 1	0x0000_0000
CMPICLR1	0x114	Comparator Interrupt Clear Register 1	NA

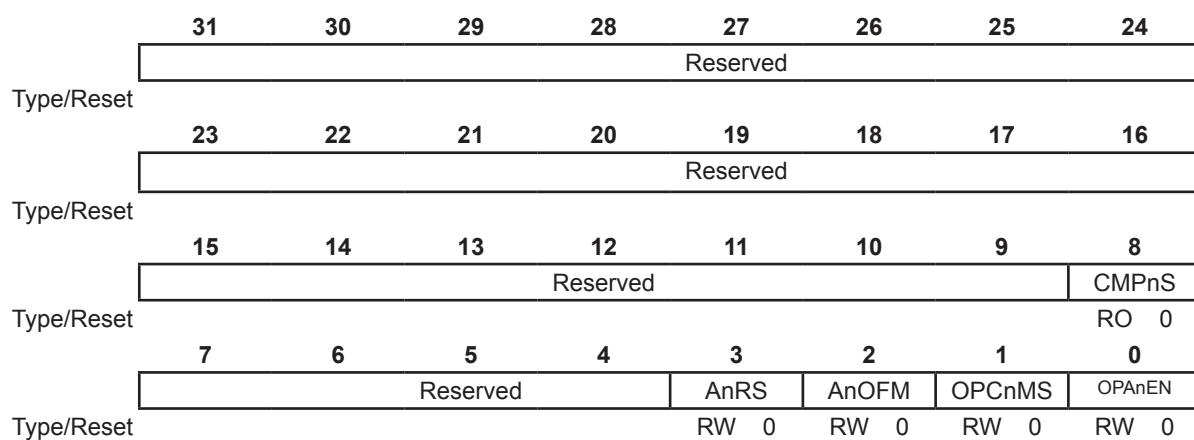
Register Descriptions

Operational Amplifier Control Register n – OPACRn, n = 0 or 1

This register contains the OPA/CMP enable control, the OPA/CMP mode selection, input offset cancellation control bits and the comparator digital output status.

Offset: 0x000 (0), 0x100 (1)

Reset value: 0x0000_0000



Bits	Field	Descriptions
[8]	CMPnS	Comparator Digital Output Status This bit is read only and has the same polarity as Comparator output. It can be used for software monitor the Comparator output in the input offset voltage cancellation mode.
[3]	AnRS	Operational Amplifier Input Offset Voltage Cancellation Reference Voltage Selection 0: Comparator negative input is selected as the reference input 1: Comparator positive input is selected as the reference input
[2]	AnOFM	Operational Amplifier / Comparator Mode or Input Offset Voltage Cancellation Mode Selection 0: Operational Amplifier / Comparator mode 1: Input offset voltage cancellation mode
[1]	OPCnMS	Operational Amplifier or Comparator Mode Selection 0: Operational Amplifier mode 1: Comparator mode
[0]	OPAnEN	Operational Amplifier / Comparator Enable or Power Down Control Bit 0: Disable Operational Amplifier / Comparator (entering the power down mode) 1: Enable Operational Amplifier / Comparator

Comparator Input Offset Voltage Cancellation Register n – OFVCRn, n=0 or 1

The register is used to cancel the comparator n input offset voltage.

Offset: 0x004 (0), 0x104 (1)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24		
Type/Reset	Reserved									
	23	22	21	20	19	18	17	16		
Type/Reset	Reserved									
	15	14	13	12	11	10	9	8		
Type/Reset	Reserved									
	7	6	5	4	3	2	1	0		
Type/Reset	Reserved		RW	0	RW	0	RW	0	RW	0
	AnOF									

Bits	Field	Descriptions
[5:0]	AnOF	Operational Amplifier / Comparator Input Offset Voltage Cancellation Control Bit 000000: Minumun ... 100000: Center ... 111111: Maxumun

Comparator Interrupt Enable Register n – CMPIERn, n = 0 or 1

Comparator n Interrupt Mask Enable Register.

Offset: 0x008 (0), 0x108 (1)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24	
Type/Reset	Reserved								
	23	22	21	20	19	18	17	16	
Type/Reset	Reserved								
	15	14	13	12	11	10	9	8	
Type/Reset	Reserved								
	7	6	5	4	3	2	1	0	
Type/Reset	Reserved						CRnIEN	CFnIEN	
							RW 0	RW 0	

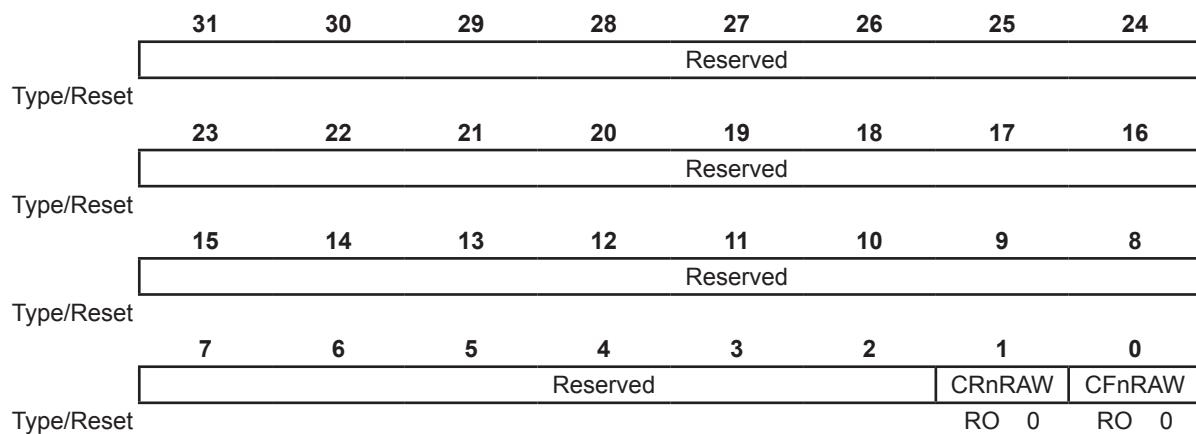
Bits	Field	Descriptions
[1]	CRnIEN	Comparator Output Rising Edge Interrupt Enable Control Bit 0: Comparator output rising edge interrupt is disabled. 1: Comparator output rising edge interrupt is enabled.
[0]	CFnIEN	Comparator Output Falling Edge Interrupt Enable Control Bit 0: Comparator output falling edge interrupt is disabled. 1: Comparator output falling edge interrupt is enabled.

Comparator Raw Status Register n – CMPSR_n, n = 0 or 1

This register contains the comparator n output transition event raw status.

Offset: 0x00C (0), 0x10C (1)

Reset value: 0x0000_0000



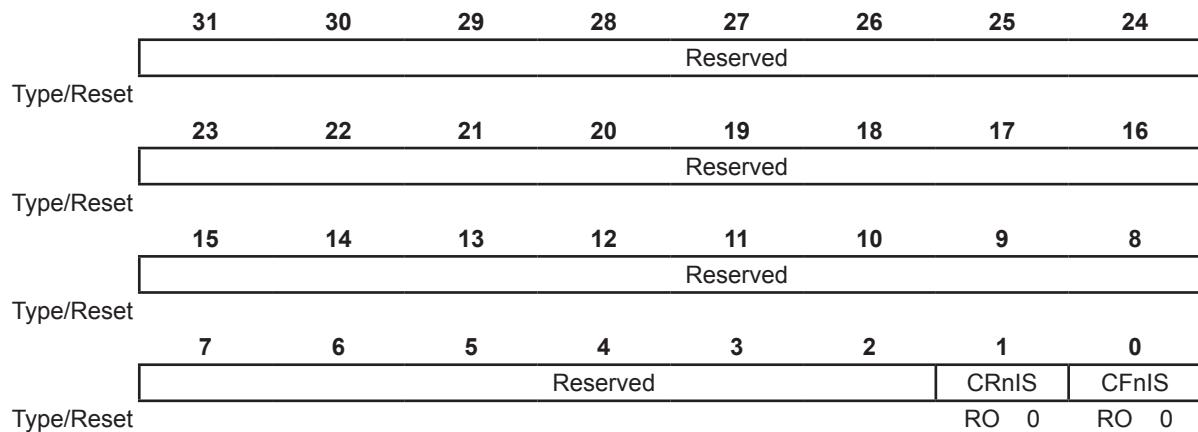
Bits	Field	Descriptions
[1]	CRnRAW	<p>Comparator Output Rising Edge Raw Flag Bit.</p> <p>0: No Comparator output rising edge is occurs.</p> <p>1: Comparator output rising edge is occurs.</p> <p>This bit can be cleared by writing “1” into the CRnICLR bit in the CMPICLR_n register via the application software.</p>
[0]	CFnRAW	<p>Comparator Output Falling Edge Interrupt Raw Flag Bit.</p> <p>0: No Comparator output falling edge is occurs.</p> <p>1: Comparator output falling edge is occurs.</p> <p>This bit can be cleared by writing “1” into the CFnICLR bit in the CMPICLR_n register via the application software.</p>

Comparator Interrupt Status Register n – CMPISRn, n = 0 or 1

This register contains the comparator n transition event masked interrupt status.

Offset: 0x010 (0), 0x110 (1)

Reset value: 0x0000_0000



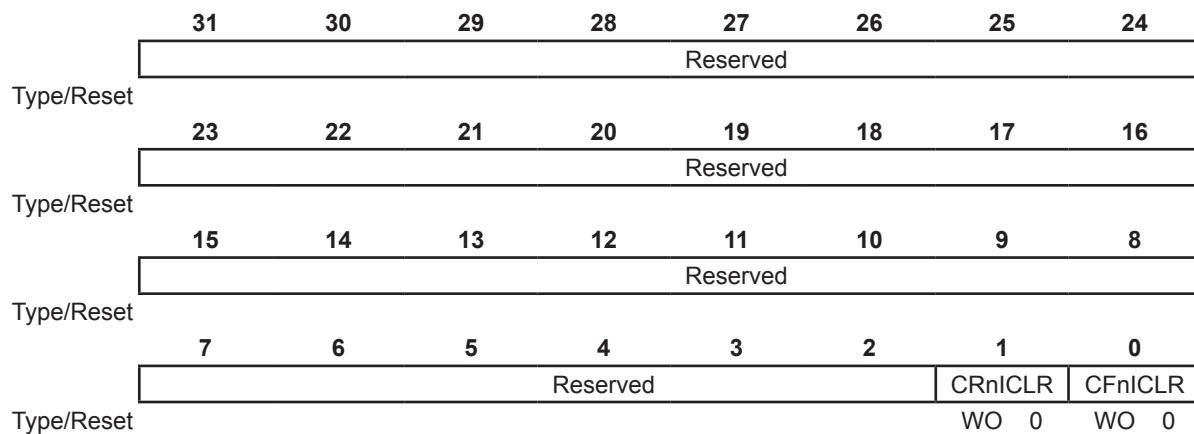
Bits	Field	Descriptions
[1]	CRnIS	Comparator Output Rising Edge Masked Interrupt Flag 0: No Comparator output rising edge occurs or the Comparator output rising edge interrupt is disabled. 1: Comparator output rising edge occurs and the Comparator output rising edge interrupt is enabled.
[0]	CFnIS	Comparator Output Falling Edge Masked Interrupt Bit 0: No Comparator output falling edge occurs or the Comparator output falling edge interrupt is disabled. 1: Comparator output falling edge occurs and the Comparator output falling edge interrupt is enabled.

Comparator Interrupt Clear Register n – CMPICLRn, n = 0 or 1

The register provides the interrupt status clear bits used to indicate the comparator n output transition interrupt raw and masked status. These bits are set to 1 by software to clear the associated interrupt raw and masked status bits and cleared to 0 by hardware automatically after being set to 1.

Offset: 0x014 (0), 0x114 (1)

Reset value: 0x0000_0000



Bits	Field	Descriptions
[1]	CRnICLR	Comparator Output Rising Edge Interrupt status Clear Control 0: No effect 1: Comparator output rising edge interrupt raw status and masked status is cleared.
[0]	CFnICLR	Comparator Output Falling Edge Interrupt status Clear Control Bit 0: No effect 1: Comparator output falling edge interrupt raw status and masked status is cleared.

14

General-Purpose Timers (GPTM)

Introduction

The General-Purpose Timer consists of one 16-bit up/down-counter, four 16-bit Capture/Compare Registers (CCRs), one 16-bit Counter-Reload Register (CRR) and several control/status registers. It can be used for a variety of purposes including general timer, input signal pulse width measurement or output waveform generation such as single pulse generation or PWM output. The GPTM supports an encoder interface using a quadrature decoder with two inputs.

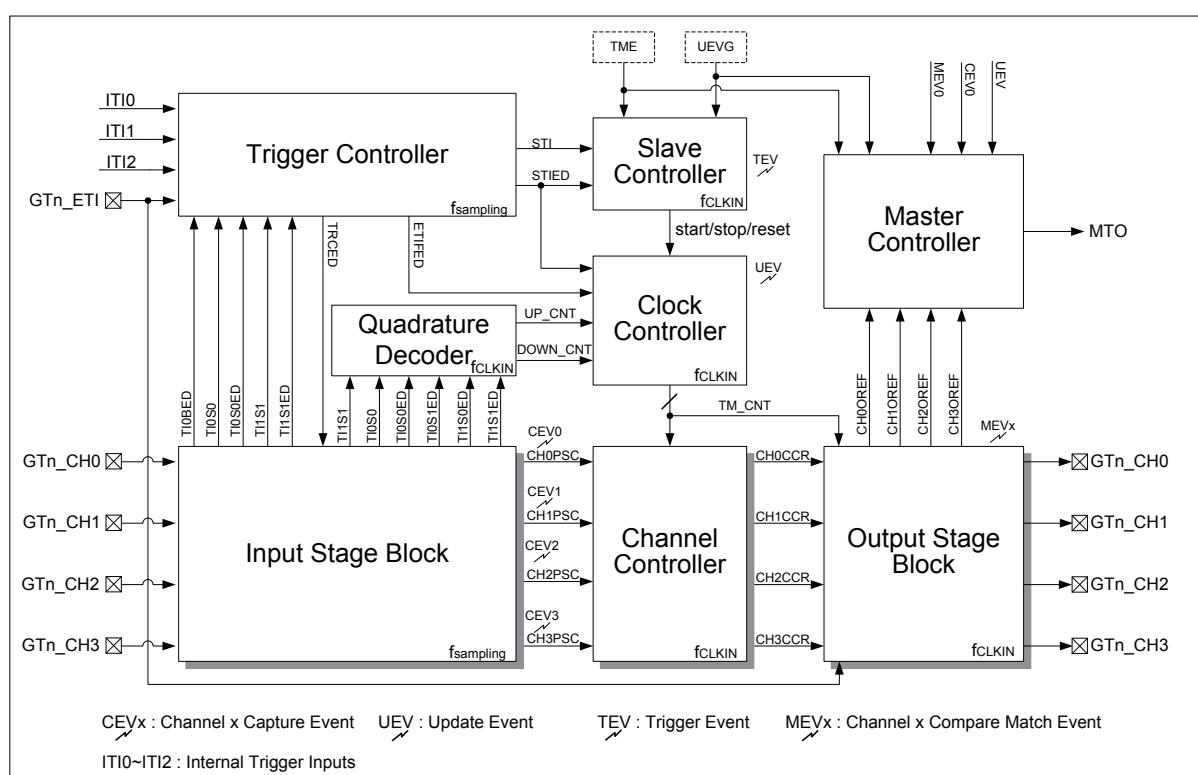


Figure 33. GPTM Block Diagram

Features

- 16-bit up/down auto-reload counter
- 16-bit programmable prescaler that allows division of the counter clock frequency by any factor between 1 and 65536
- Up to 4 independent channels for:
 - Input Capture function
 - Compare Match Output
 - Generation of PWM waveform - Edge and Center-aligned Mode
 - Single Pulse Mode Output
- Encoder interface controller with two inputs using quadrature decoder
- Synchronization circuit to control the timer with external signals and to interconnect several timers together
- Interrupt/PDMA generation with the following events:
 - Update event
 - Trigger event
 - Input capture event
 - Output compare match event
- GPTM Master/Slave mode controller

Functional Descriptions

Counter Mode

Up-Counting

In this mode the counter counts continuously from 0 to the counter-reload value, which is defined in the CRR register, in a count-up direction. Once the counter reaches the counter-reload value, the Timer Module generates an overflow event and the counter restarts to count once again from 0. This action will continue repeatedly. The counting direction bit DIR in the CNTCFR register should be set to 0 for the up-counting mode.

When the update event is generated by setting the UEVG bit in the EVGR register to 1, the counter value will also be initialized to 0.

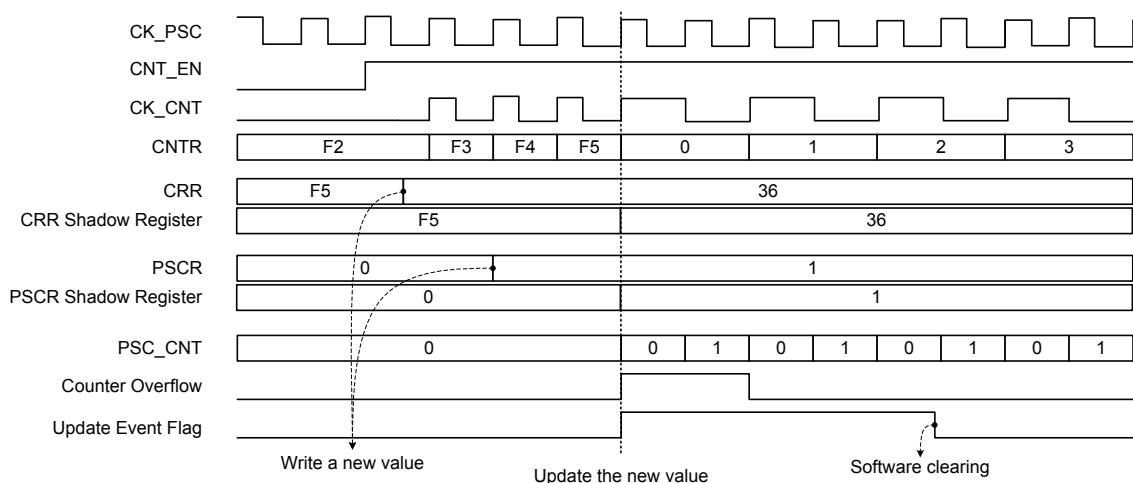


Figure 34. Up-counting Example

Down-Counting

In this mode the counter counts continuously from the counter-reload value, which is defined in the CRR register, to 0 in a count-down direction. Once the counter reaches 0, the Timer module generates an underflow event and the counter restarts to count once again from the counter-reload value. This action will continue repeatedly. The counting direction bit DIR in the CNTCFR register should be set to 1 for the down-counting mode.

When the update event is set by the UEVG bit in the EVGR register, the counter value will also be initialized to the counter-reload value.

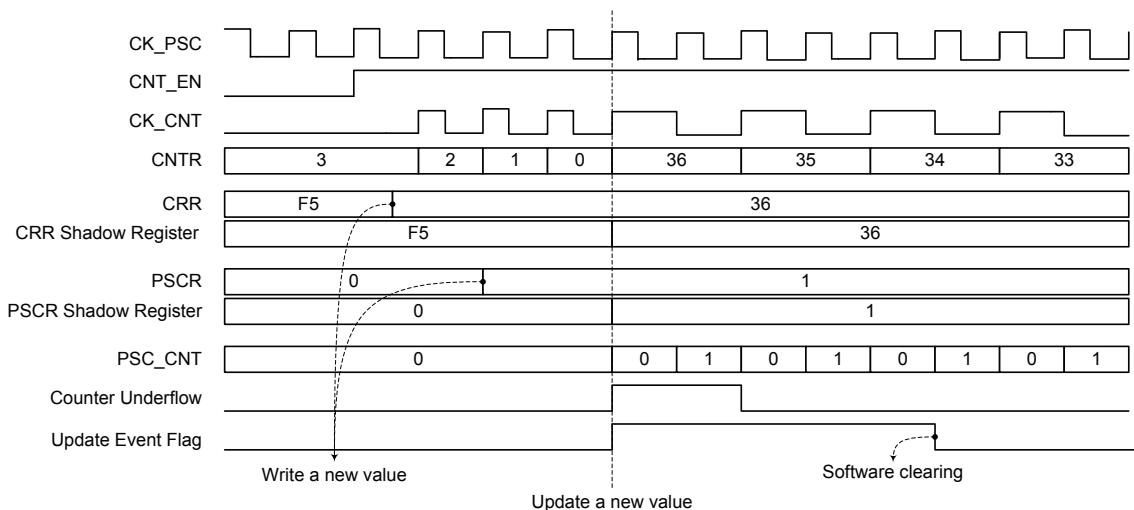


Figure 35. Down-counting Example

Center-Align Counting

In the center-aligned counting mode, the counter counts up from 0 to the counter-reload value and then counts down to 0 alternatively. The Timer module generates an overflow event when the counter counts to the counter-reload value in the up-counting mode and generates an underflow event when the counter counts to 0 in the down-counting mode. The counting direction bit DIR in the CNTCFR register is read-only and indicates the counting direction when in the center-align mode. The counting direction is updated by hardware automatically.

Setting the UEVG bit in the EVGR register will initialize the counter value to 0 irrespective of whether the counter is counting up or down in the center-align counting mode.

The UEVIF bit in the INTSR register can be set to 1 when an overflow or underflow event or both of them occur according to the CMSEL field setting in the CNTCFR register.

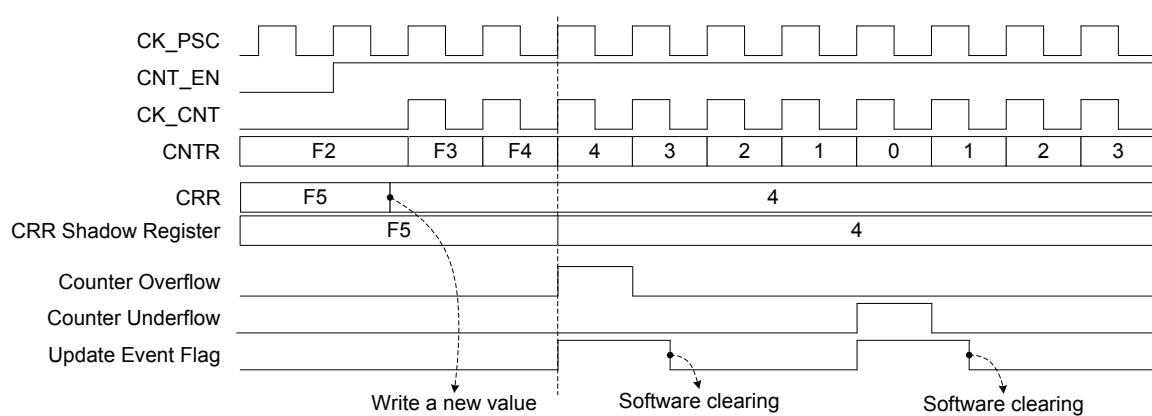


Figure 36. Center-aligned Counting Example

Clock Controller

The following describes the Timer Module clock controller which determines the clock source of the internal prescaler counter.

Internal APB clock f_{CLKIN}

The default internal clock source is the APB clock f_{CLKIN} used to drive the counter prescaler when the slave mode is disabled. If the slave mode controller is enabled by setting SMSEL field in the MDCFR register to an available value including 0x1, 0x2, 0x3 and 0x7, the prescaler is clocked by other clock sources selected by the TRSEL field in the TRCFR register and described as follows. When the slave mode selection bits SMSEL are set to 0x4, 0x5 or 0x6, the internal APB clock f_{CLKIN} is the counter prescaler driving clock source.

Quadrature Decoder

To select Quadrature Decoder mode the SMSEL field should be set to 0x1, 0x2 or 0x3 in the MDCFR register. The Quadrature Decoder function uses two input states of the GTn_CH0 and GTn_CH1 pins to generate the clock pulse to drive the counter prescaler. The counting direction bit DIR is modified by hardware automatically at each transition on the input source signal. The input source signal can be derived from the GTn_CH0 pin only, the GTn_CH1 pin only or both GTn_CH0 and GTn_CH1 pins.

STIED

The counter prescaler can count during each rising edge of the STI signal. This mode can be selected by setting the SMSEL field to 0x7 in the MDCFR register. Here the counter will act as an event counter. The input event, known as STI here, can be selected by setting the TRSEL field to an available value except the value of 0x0. When the STI signal is selected as the clock source, the internal edge detection circuitry will generate a clock pulse during each STI signal rising edge to drive the counter prescaler. It is important to note that if the TRSEL field is set to 0x0 to select the software UEVG bit as the trigger source, then when the SMSEL field is set to 0x7, the counter will be updated instead of counting.

ETIFED

The counter prescaler can be driven to count during each rising edge on the external pin GTn_ETI. This mode can be selected by setting the ECME bit in the TRCFR register to 1. The other way to select the ETIF signal as the clock source is to set the SMSEL field to 0x7 and the TRSEL field to 0x3 respectively. Note that the ETIF signal is derived from the GTn_ETI pin sampled by a digital filter. When the clock source is selected to come from the ETIF signal, the Trigger Controller including the edge detection circuitry will generate a clock pulse during each ETIF signal rising edge to clock the counter prescaler.

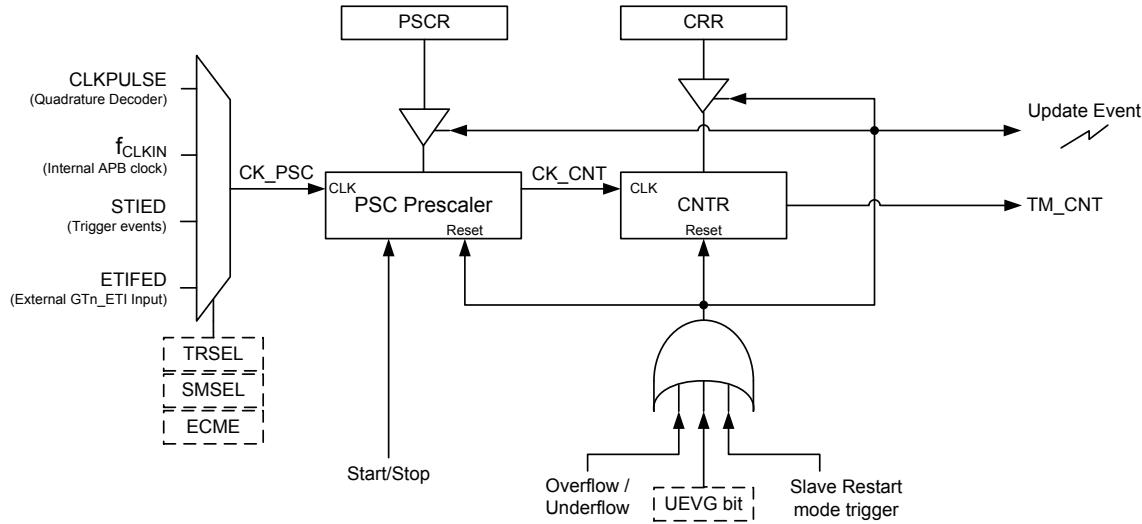


Figure 37. GPTM Clock Selection Source

Trigger Controller

The trigger controller is used to select the trigger source and setup the trigger level or edge trigger condition. The active polarity of the external trigger input signal GTn_ETI can be configured by the External Trigger Polarity control bit ETIPOL in the GPTM Trigger Configuration Register TRCFR. The frequency of the external trigger input can be divided by configuring the related bits, named as External Trigger Prescaler control bits ETIPSC, in the TRCFR register. The trigger signal can also be filtered by configuring the External Trigger Filter ETF selection bits in the TRCFR register if a filtered signal is necessary for specific applications. For the internal trigger input, it can be selected by the Trigger Selection bits TRSEL in the TRCFR register. For all the trigger sources except the UEVG bit software trigger, the internal edge detection circuitry will generate a clock pulse at each trigger signal rising edge to stimulate some GPTM functions which are triggered by a trigger signal rising edge.

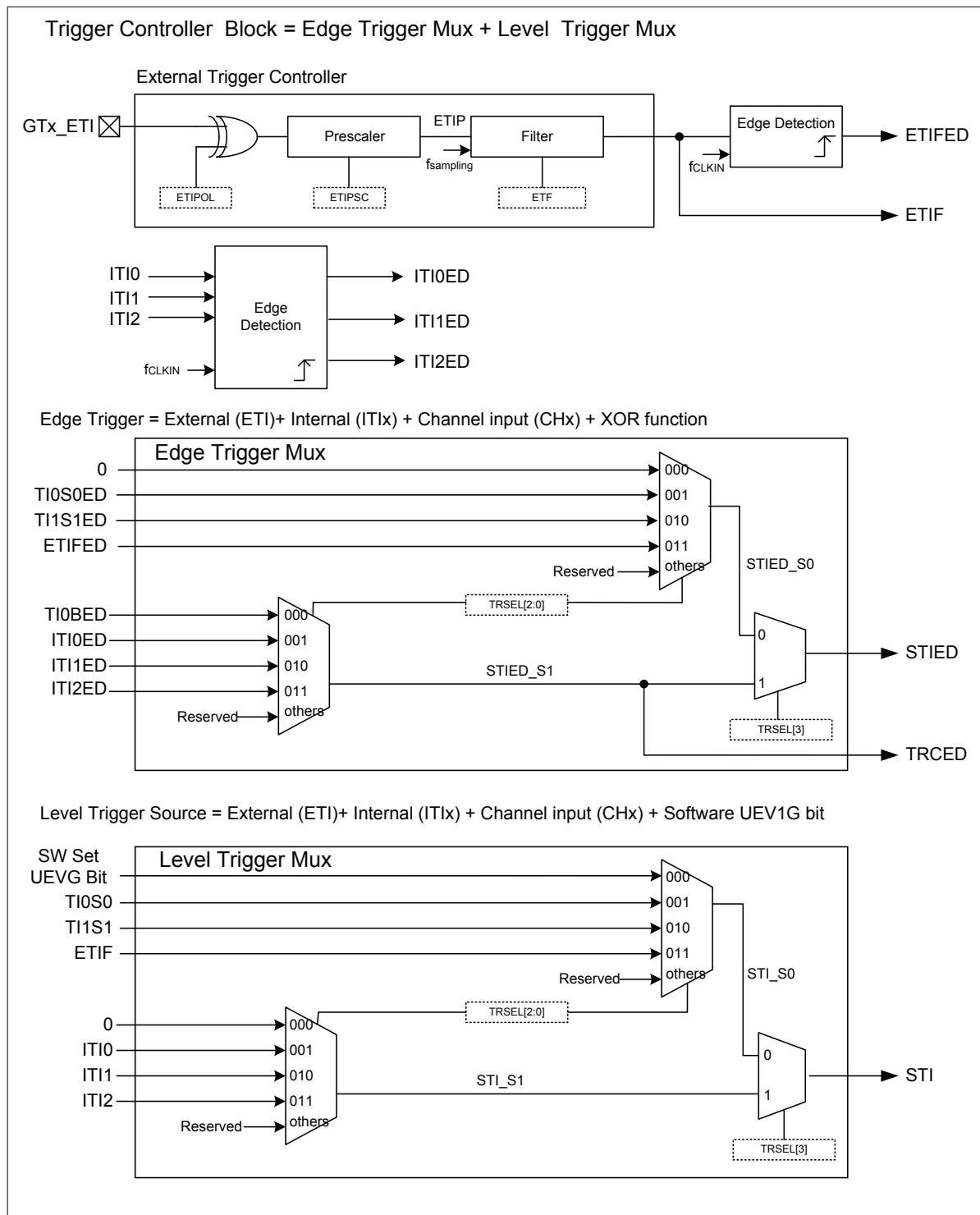


Figure 38. Trigger Control Block

Slave Controller

The GPTM can be synchronized with an external trigger in several modes including the Restart mode, the Pause mode and the Trigger mode which is selected by the SMSEL field in the MDCFR register. The trigger input of these modes comes from the STI signal which is selected by the TRSEL field in the TRCFR register. The operation modes in the Slave Controller are described in the accompanying sections.

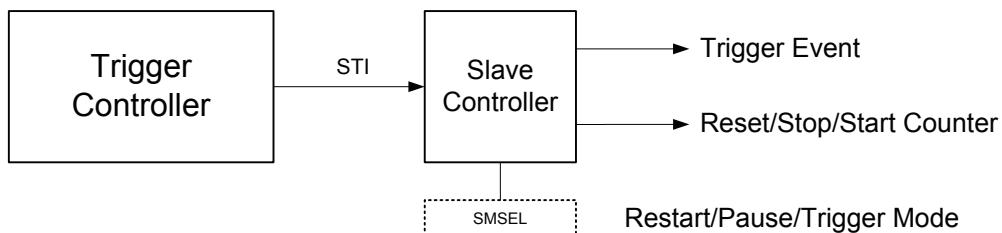


Figure 39. Slave Controller Diagram

Restart Mode

The counter and its prescaler can be reinitialized in response to a rising edge of the STI signal. When a STI rising edge occurs, the update event software generation bit named UEVG will automatically be asserted by hardware and the trigger event flag will also be set. Then the counter and prescaler will be reinitialized. Although the UEVG bit is set to 1 by hardware, the update event does not really occur. It depends upon whether the update event disable control bit UEVDIS is set to 1 or not. If the UEVDIS is set to 1 to disable the update event to occur, there will no update event be generated, however the counter and prescaler are still reinitialized when the STI rising edge occurs. If the UEVDIS bit in the CNTCFR register is cleared to enable the update event to occur, an update event will be generated together with the STI rising edge, then all the preloaded registers will be updated.

Timer Counter Reload Register CRR = 32

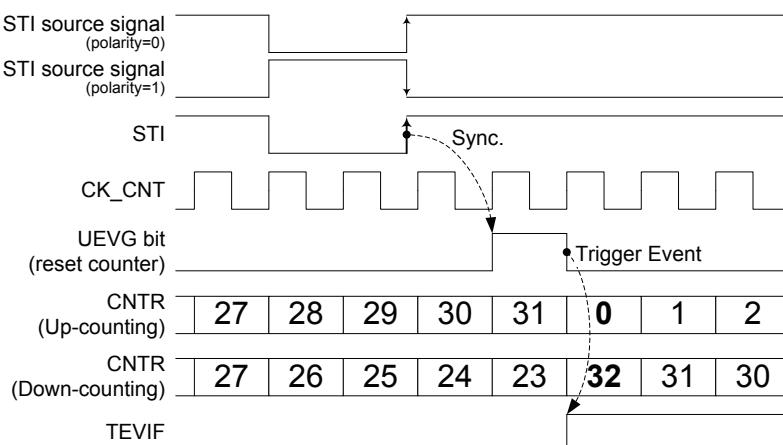


Figure 40. GPTM in Restart Mode

Pause Mode

In the Pause Mode, the selected STI input signal level is used to control the counter start/stop operation. The counter starts to count when the selected STI signal is at a high level and stops counting when the STI signal is changed to a low level, here the counter will maintain its present value and will not be reset. Since the Pause function depends upon the STI level to control the counter stop/start operation, the selected STI trigger signal can not be derived from the TI0BED signal.

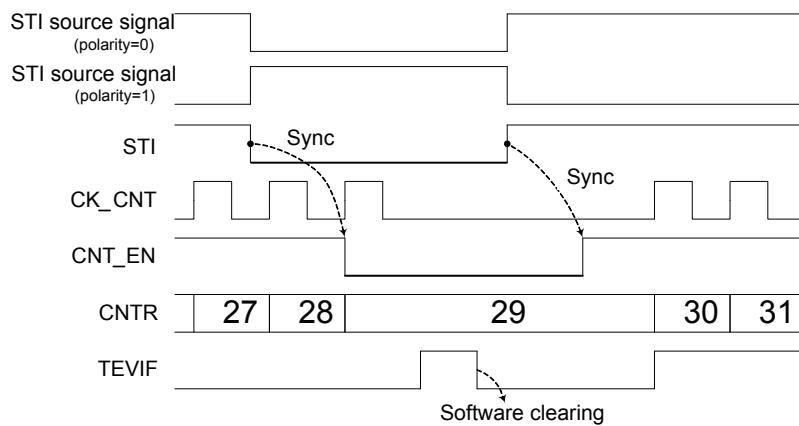


Figure 41. GPTM in Pause Mode

Trigger Mode

After the counter is disabled to count, the counter can resume counting when a STI rising edge signal occurs. When an STI rising edge occurs, the counter will start to count from the current value in the counter. Note that if the STI signal is selected to be derived from the UEVG bit software trigger, the counter will not resume counting. When software triggering using the UEVG bit is selected as the STI source signal, there will be no clock pulse generated which can be used to make the counter resume counting. Note that the STI signal is only used to enable the counter to resume counting and has no effect on controlling the counter to stop counting.

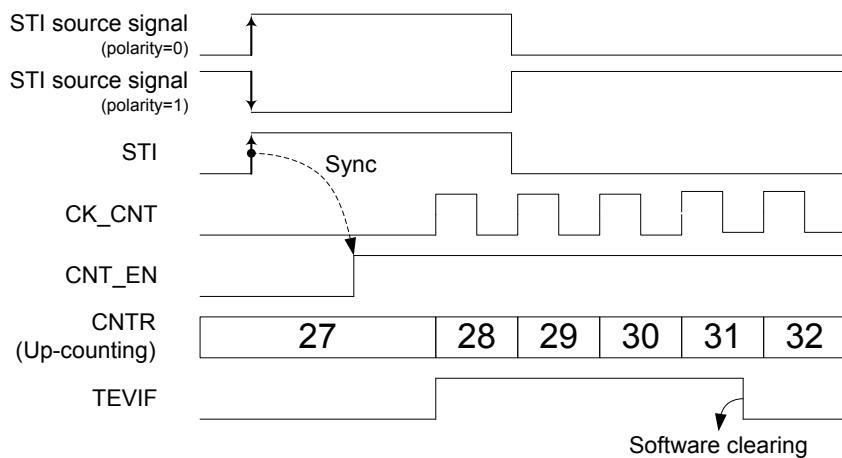


Figure 42. GPTM in Trigger Mode

Master Controller

The GPTMs and MCTMs can be linked together internally for timer synchronization or chaining. When one GPTM is configured to be in the Master Mode, the GPTM Master Controller will generate a Master Trigger Output (MTO) signal which includes a reset, a start, a stop signal or a clock source which is selected by the MMSEL field in the MDCFR register to trigger or drive another GPTM or MCTM, if exists, which is configured in the Slave Mode.

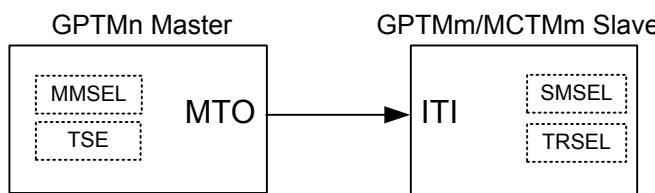


Figure 43. Master GPTMn and Slave GPTMm/MCTMm Connection

The Master Mode Selection bits, MMSEL, in the MDCFR register are used to select the MTO source for synchronizing another slave GPTM or MCTM if exists.

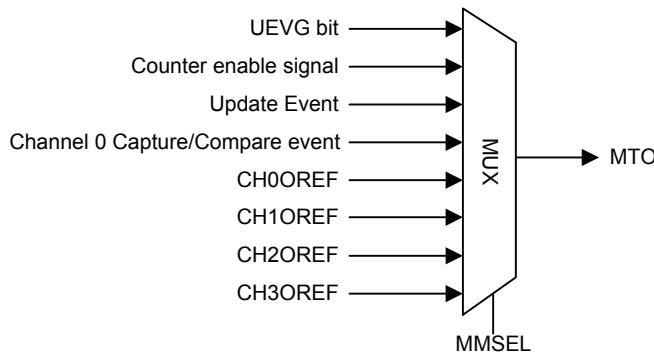


Figure 44. MTO Selection

For example, setting the MMSEL field to 0x5 is to select the CH1OREF signal as the MTO signal to synchronize another slave GPTM or MCTM. For a more detailed description, refer to the related MMSEL field definitions in the MDCFR register.

Channel Controller

The GPTM has four independent channels which can be used as capture inputs or compare match outputs. Each capture input or compare match output channel is composed of a preload register and a shadow register. Data access of the APB bus is always through the read/write preload register.

When used in the input capture mode, the counter value is captured into the CHxCCR shadow register first and then transferred into the CHxCCR preload register when the capture event occurs.

When used in the compare match output mode, the contents of the CHxCCR preload register is copied into the associated shadow register; the counter value is then compared with the register value.

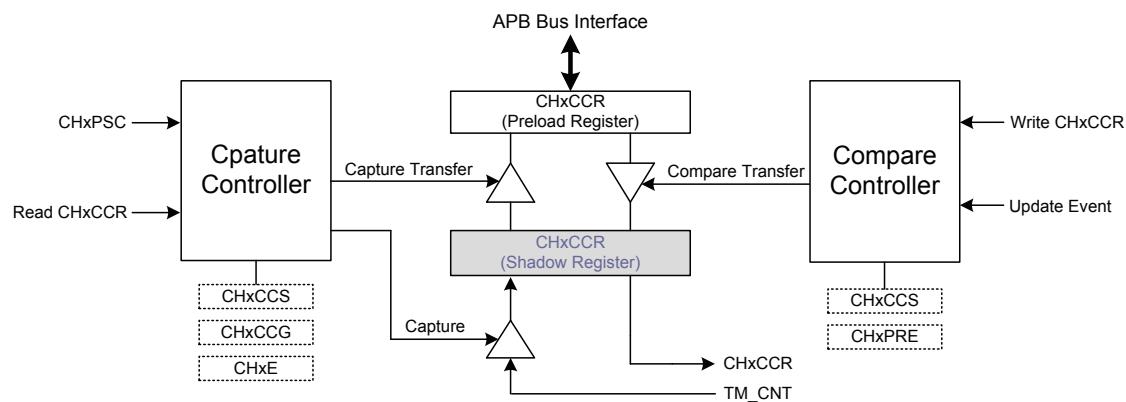


Figure 45. Capture/Compare Block Diagram

Capture Counter Value Transferred to CHxCCR

When the channel is used as a capture input, the counter value is captured into the Channel Capture/Compare Register (CHxCCR) when an effective input signal transition occurs. Once the capture event occurs, the CHxCCIF flag in the INTSR register is set accordingly. If the CHxCCIF bit is already set, i.e., the flag has not yet been cleared by software, and another capture event on this channel occurs, the corresponding channel Over-Capture flag, named CHxOCF, will be set.

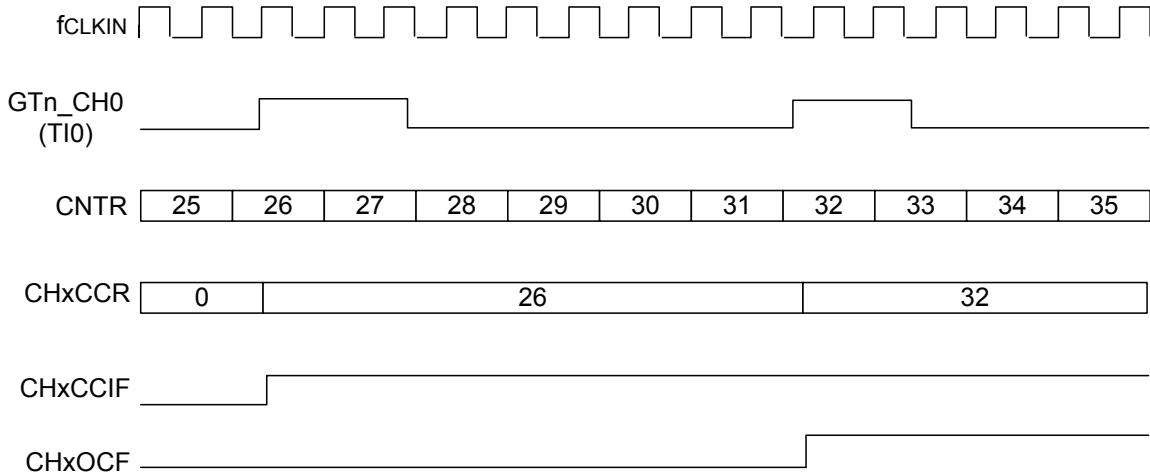


Figure 46. Input Capture Mode

Pulse Width Measurement

The input capture mode can be also used for pulse width measurement from signals on the GTn_CHx pins (TIx). The following example shows how to configure the GPTM operated in the input capture mode to measure the high pulse width and the input period on the GTn_CH0 pin using channel 0 and channel 1. The basic steps are shown as follows.

- Configure the capture channel 0 (CH0CCS = 0x1) to select the TI0 signal as the capture input.
- Configure the CH0P bit to 0 to choose the rising edge of the TI0 input as the active polarity.
- Configure the capture channel 1 (CH1CCS = 0x2) to select the TI0 signal as the capture input.
- Configure the CH1P bit to 1 to choose the falling edge of the TI0 input as the active polarity.
- Configure the TRSEL bits to 0x0001 to select TI0S0 as the trigger input.
- Configure the Slave controller to operate in the Restart mode by setting the SMSEL field in the MDCFTR register to 0x4
- Enable the input capture mode by setting the CH0E and CH1E bits in the CHCTR register to 1.

As the following diagram shows, the high pulse width on the GTn_CH0 pin will be captured into the CH1CCR register while the input period will be captured into the CH0CCR register after input capture operation.

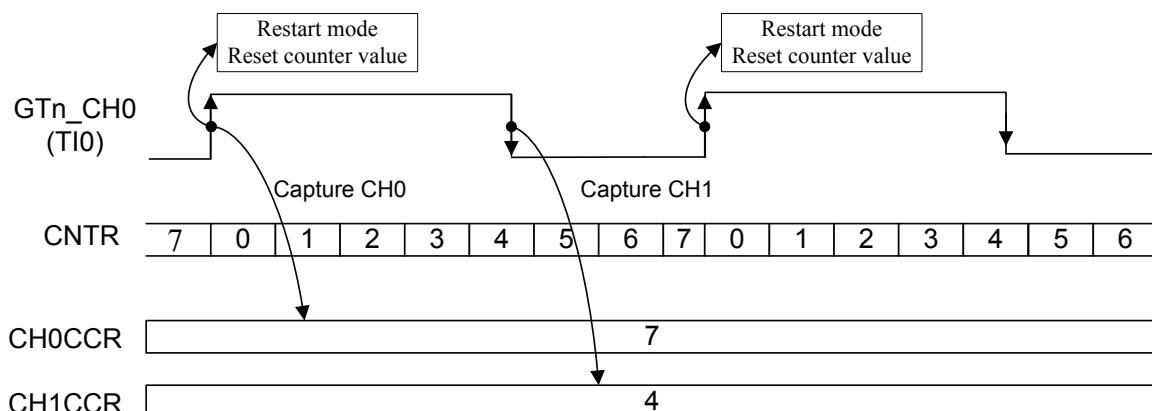


Figure 47. PWM Pulse Width Measurement Example

Input Stage

The input stage consists of a digital filter, a channel polarity selection, edge detection and a channel prescaler. The channel 0 input signal (TI0) can be chosen to come from the GTn_CH0 signal or the Exclusive-OR function of the GTn_CH0, GTn_CH1 and GTn_CH2 signals. The channel input signal (TIx) is sampled by a digital filter to generate a filtered input signal TIxF. Then the channel polarity and the edge detection block can generate a TIxS0ED or TIxS1ED signal for the input capture function. The effective input event number can be set by the channel input prescaler register (CHxPSC).

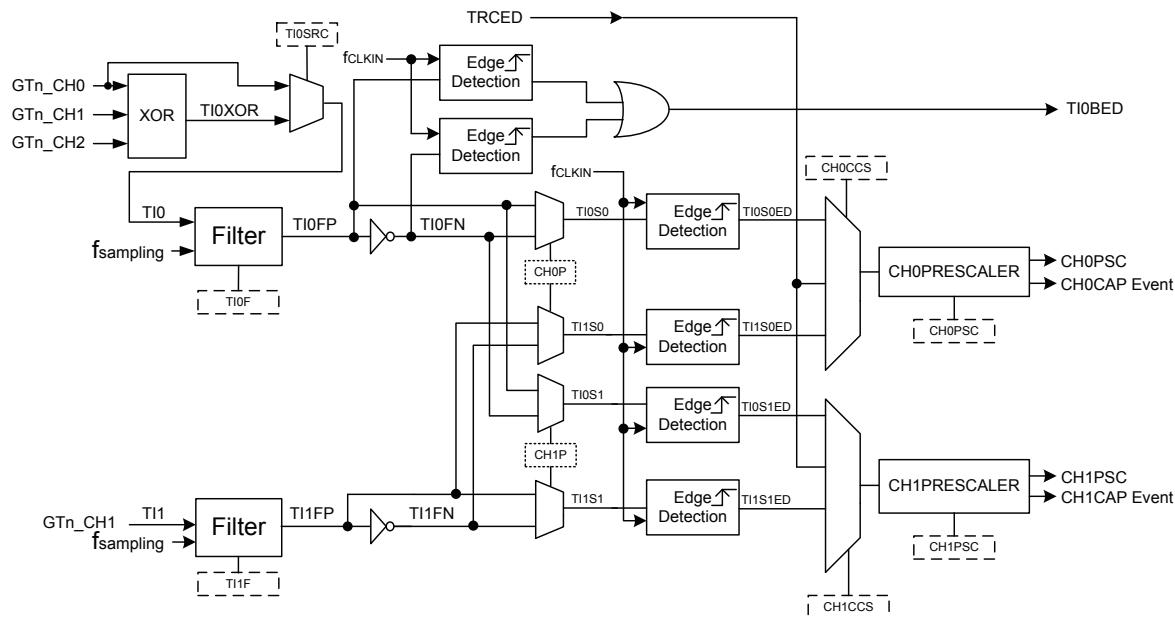


Figure 48. Channel 0 and Channel 1 Input Stage

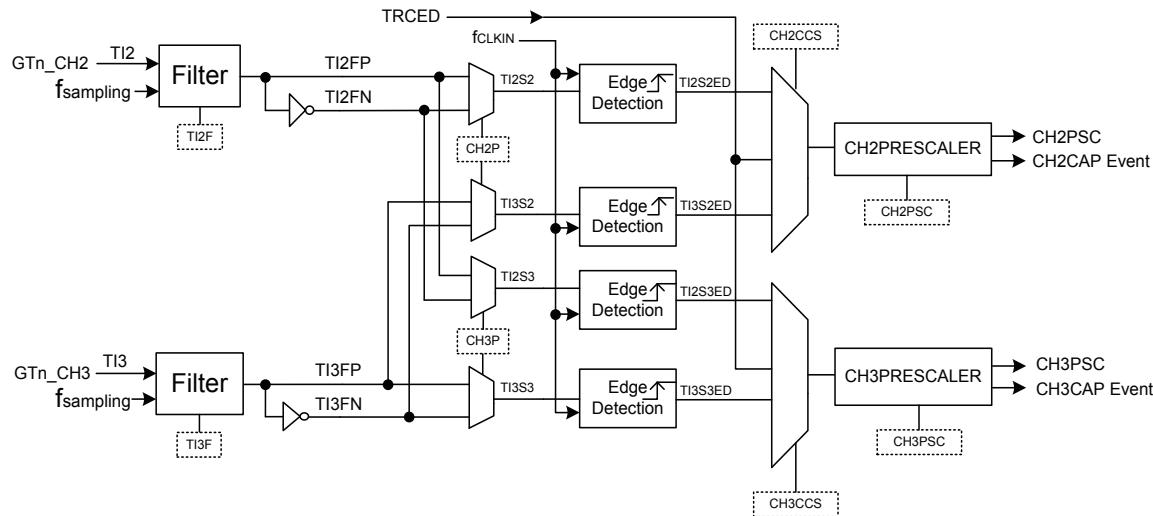


Figure 49. Channel 2 and Channel 3 Input Stage

Output Stage

The GPTM has four channels for compare match, single pulse or PWM output function. The channel output GTn_CHx is controlled by the REFxCE, CHxOM, CHxP and CHxE bits in the corresponding CHxOCFR, CHPOLR and CHCTR registers.

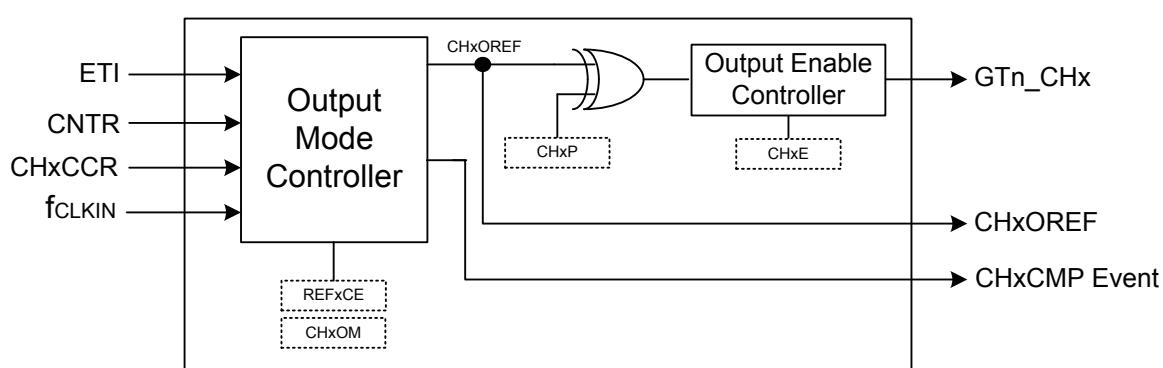


Figure 50. Output Stage Block Diagram

Channel Output Reference Signal

When the GPTM is used in the compare match output mode, the CHxOREF signal (Channel x Output Reference signal) is defined by setting the CHxOM bits. The CHxOREF signal has several types of output function. These include, keeping the original level by setting the CHxOM field to 0x00, set to 0 by setting the CHxOM field to 0x01, set to 1 by setting the CHxOM field to 0x02 or signal toggle by setting the CHxOM field to 0x03 when the counter value matches the content of the CHxCCR register.

The PWM mode 1 and PWM mode 2 outputs are also another kind of CHxOREF output which is setup by setting the CHxOM field to 0x06/0x07. In these modes, the CHxOREF signal level is changed according to the counting direction and the relationship between the counter value and the CHxCCR content. With regard to a more detailed description refer to the relative bit definition.

Another special function of the CHxOREF signal is a forced output which can be achieved by setting the CHxOM field to 0x04/0x05. Here the output can be forced to an inactive/active level irrespective of the comparison condition between the counter and the CHxCCR values.

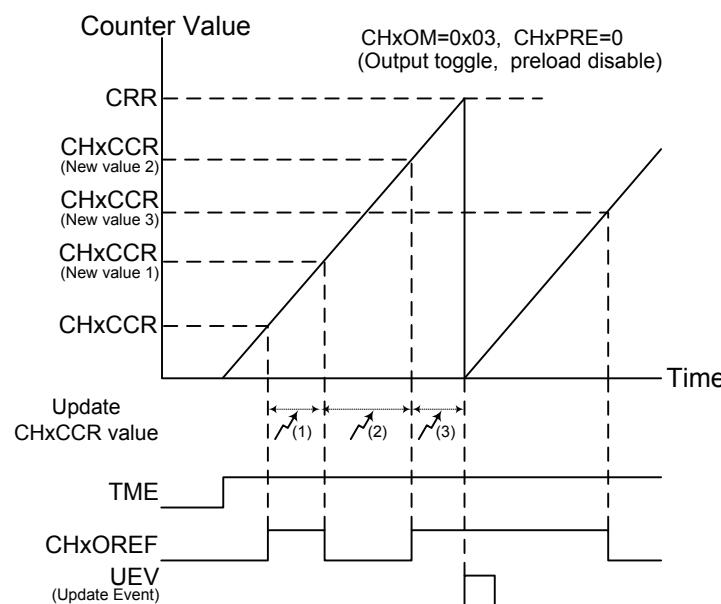


Figure 51. Toggle Mode Channel Output Reference Signal (CHxPRE = 0)

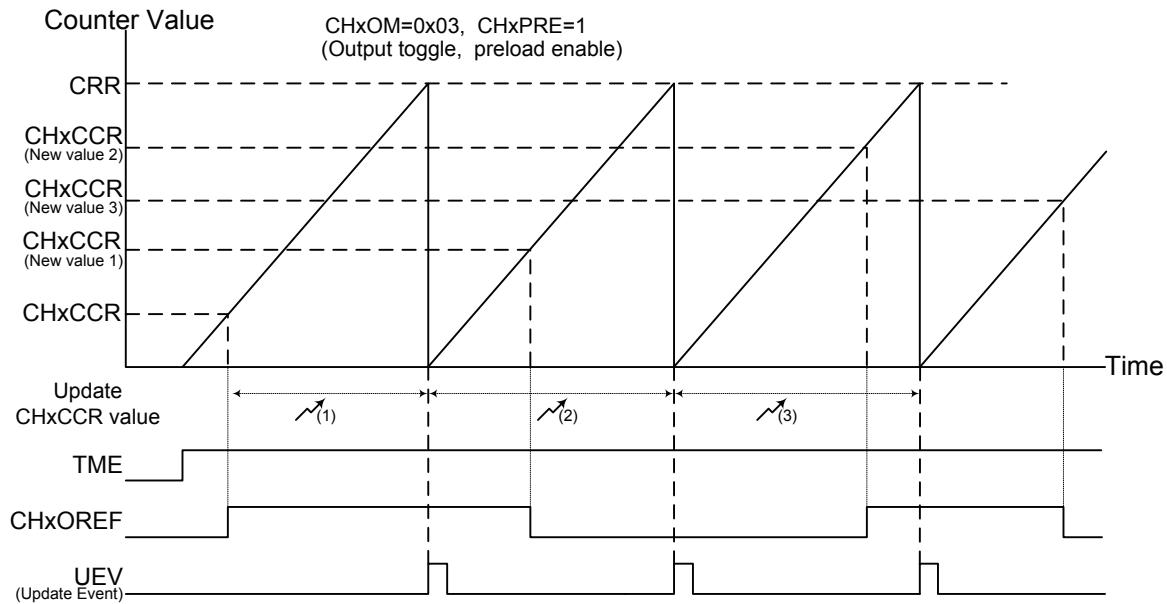


Figure 52. Toggle Mode Channel Output Reference Signal (CHxPRE = 1)

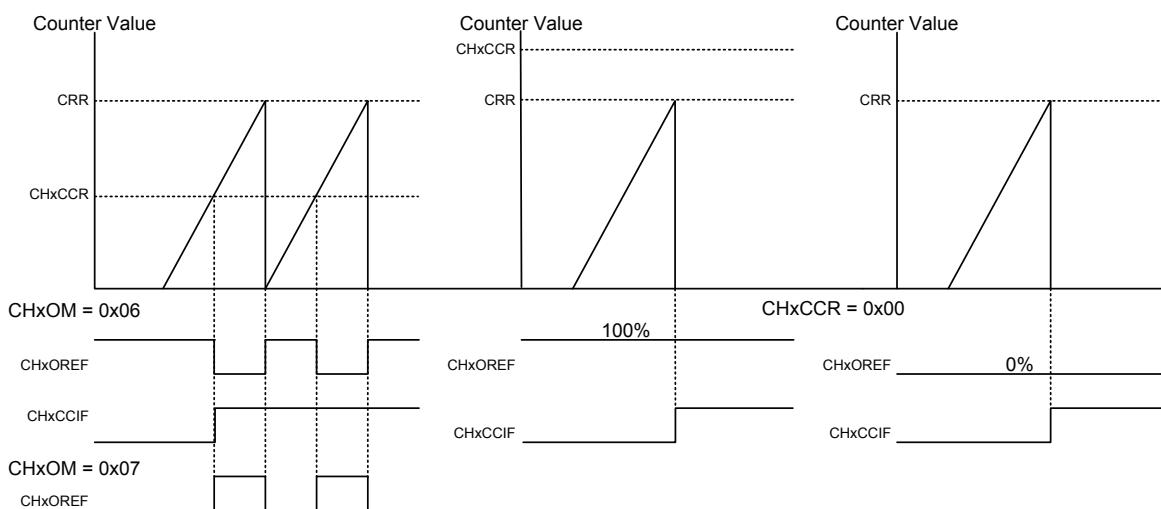


Figure 53. PWM Mode Channel Output Reference Signal and Counter in Up-counting Mode

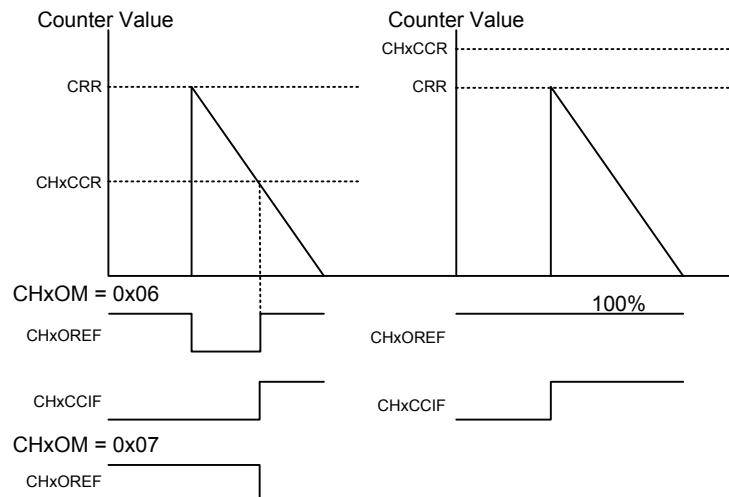


Figure 54. PWM Mode Channel Output Reference Signal and Counter in Down-counting Mode

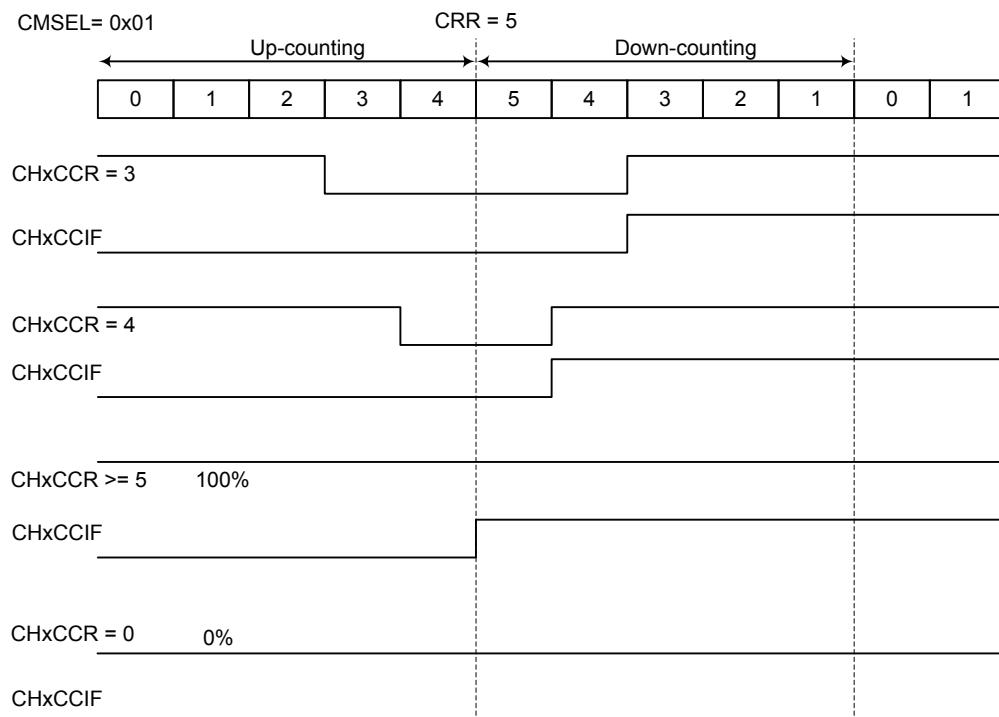


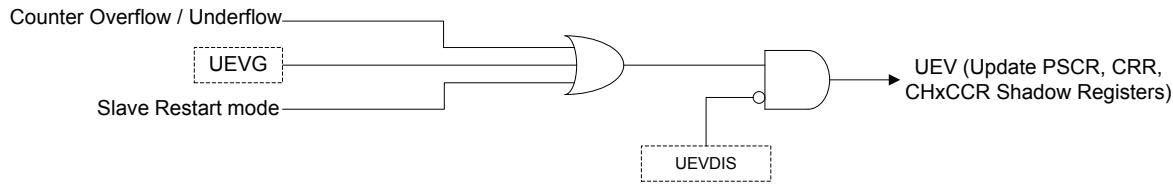
Figure 55. PWM Mode Channel Output Reference Signal and Counter in Centre-align Mode

Update Management

The Update event is used to update the CRR, the PSCR and the CHxCCR values from the actual registers to the corresponding shadow registers. An update event occurs when the counter overflows or underflows, the software update control bit is triggered or an update event from the slave controller is generated.

The UEVDIS bit in the CNTCFR register can determine whether the update event occurs or not. When the update event occurs, the corresponding update event interrupt will be generated depending upon whether the update event interrupt generation function is enabled or not by configuring the UGDIS bit in the CNTCFR register. For more detail description, refer to the UEVDIS and UGDIS bit definition in the CNTCFR register

Update Event Management



Update Event Interrupt Management

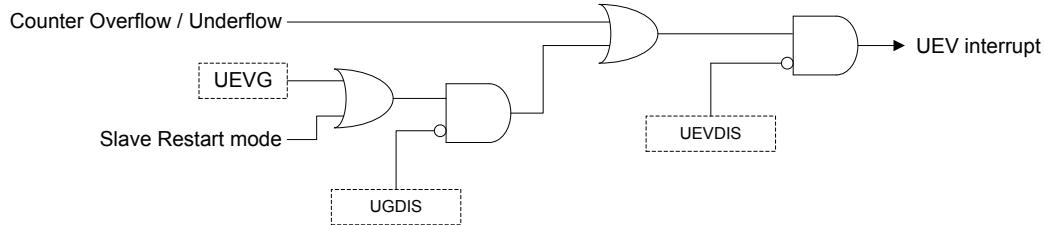


Figure 56. Update Event Setting Diagram

Quadrature Decoder

The Quadrature Decoder function uses two quadrantal inputs TI0 and TI1 derived from the GTn_CH0 and GTn_CH1 pins respectively to interact to generate the counter value. The DIR bit is modified by hardware automatically during each input source transition. The input source can be either TI0 only, TI1 only or both TI0 and TI1, the selection made by setting the SMSEL field to 0x01, 0x02 or 0x03. The mechanism for changing the counter direction is shown in the following table. The Quadrature decoder can be regarded as an external clock with a directional selection. This means that the counter counts continuously in the interval between 0 and the counter-reload value. Therefore, users must configure the CRR register before the counter starts to count.

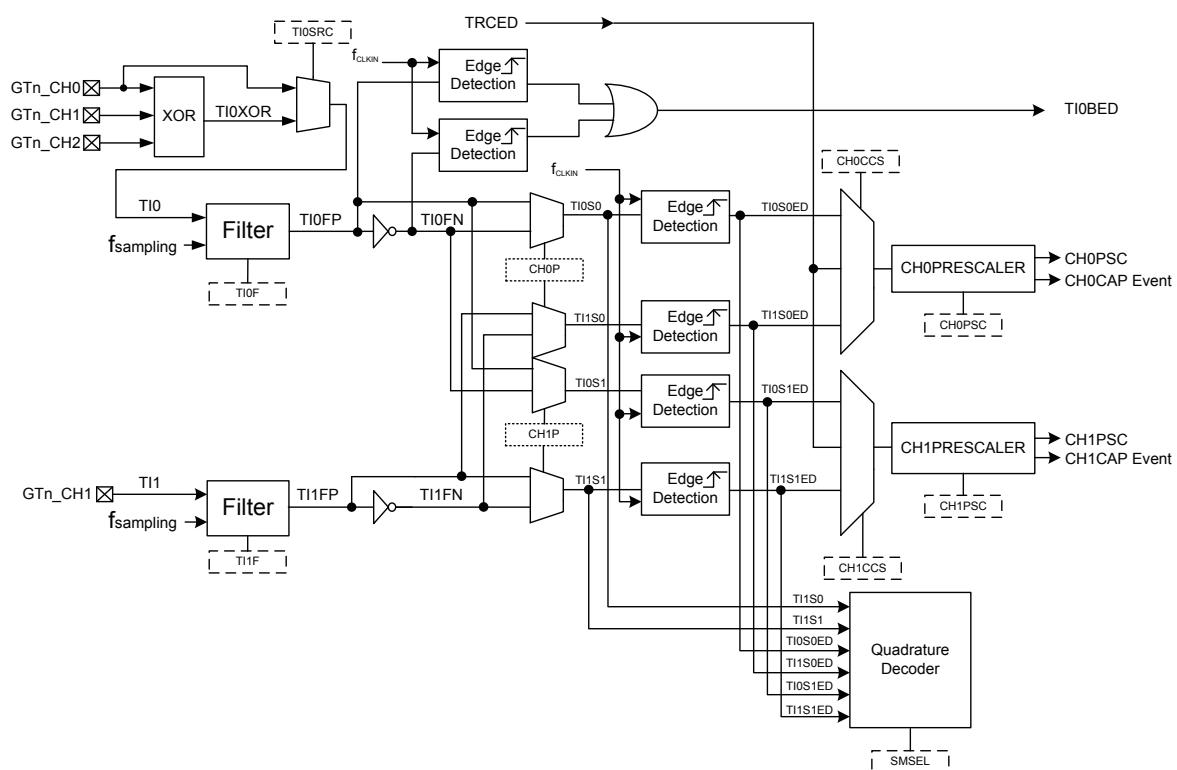


Figure 57. Input Stage and Quadrature Decoder Block Diagram

Table 31. Counting Direction and Encoding Signals

Counting mode	Level	TI0S0		TI1S1	
		Rising	Falling	Rising	Falling
Counting on TI0 only (SMSEL = 0x01)	TI1S1 = High	Down	Up	—	—
	TI1S1 = Low	Up	Down	—	—
Counting on TI1 only (SMSEL = 0x02)	TI0S0 = High	—	—	Up	Down
	TI0S0 = Low	—	—	Down	Up
Counting on TI0 and TI1 (SMSEL = 0x03)	TI1S1 = High	Down	Up	X	X
	TI1S1 = Low	Up	Down	X	X
	TI0S0 = High	X	X	Up	Down
	TI0S0 = Low	X	X	Down	Up

Note: "—" → means "no counting"; "X" → impossible

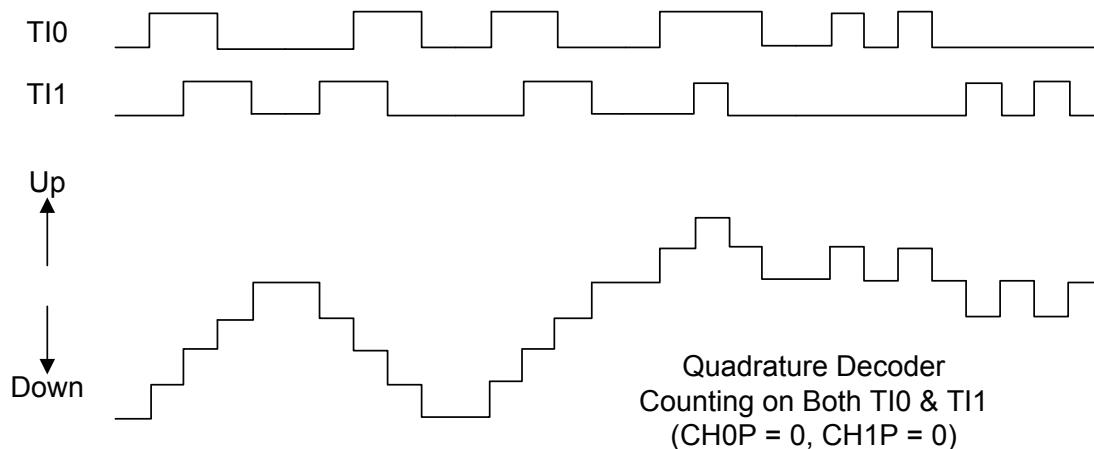


Figure 58. Both TI0 and TI1 Quadrature Decoder Counting

Digital Filter

The digital filters are embedded in the input stage and clock controller block for the GTn_CH0 ~ GTn_CH3 and GTn_ETI pins respectively. The digital filter in the GPTM is an N-event counter where N refers to how many valid transitions are necessary to output a filtered signal. The N value can be 0, 2, 4, 5, 6 or 8 according to the user selection for each filter.

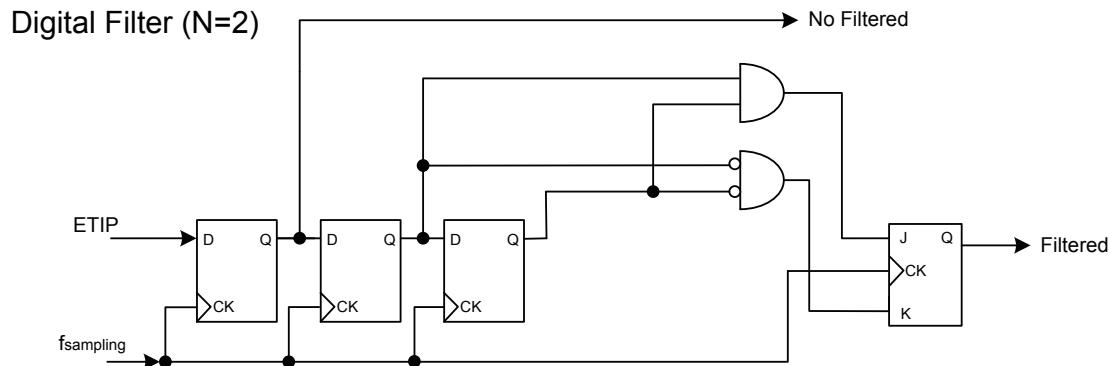


Figure 59. GTn_ETI Pin Digital Filter Diagram with N = 2

Clearing the CHxOREF when ETIF is high

The CHxOREF signal can be forced to 0 when the ETIF signal is derived from the external GTn_ETI pin and when it is set to a high level by setting the REFxCE bit to 1 in the CHxOCFR register. The CHxOREF signal will not return to its active level until the next update event occurs.

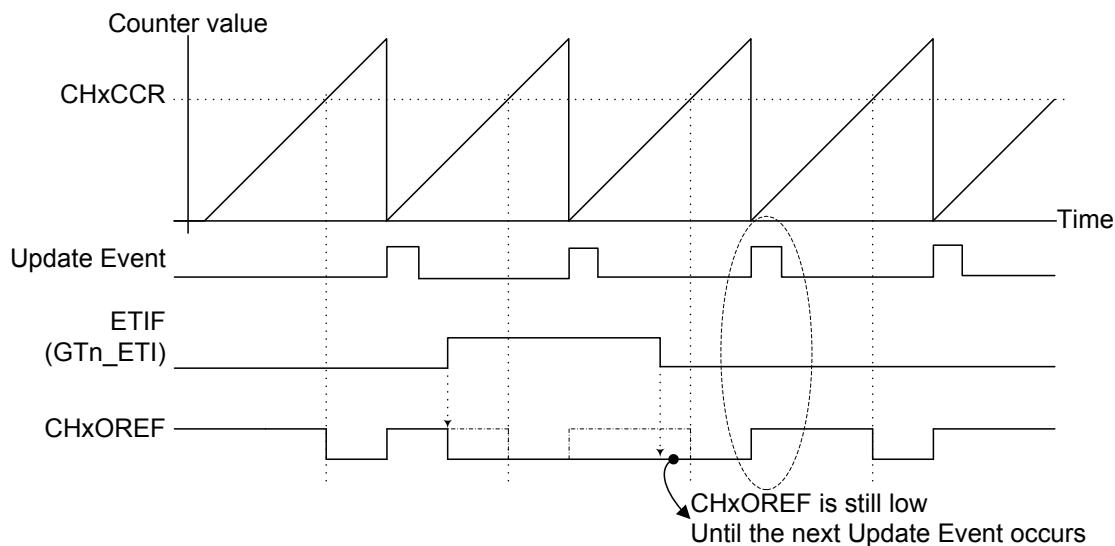


Figure 60. Clearing CHxOREF by ETIF

Single Pulse Mode

Once the timer is set to operate in the single pulse mode, it is not necessary to set the timer enable bit TME in the CTR register to 1 to enable the counter. The trigger to generate a pulse can be sourced from the STI signal rising edge or by setting the TME bit to 1 using software. Setting the TME bit to 1 or a trigger from the STI signal rising edge can generate a pulse and then keep the TME bit at a high state until the update event occurs or the TME bit is written to 0 by software. If the TME bit is cleared to 0 using software, the counter will be stopped and its value held. If the TME bit is automatically cleared to 0 by a hardware update event, the counter will be reinitialized.

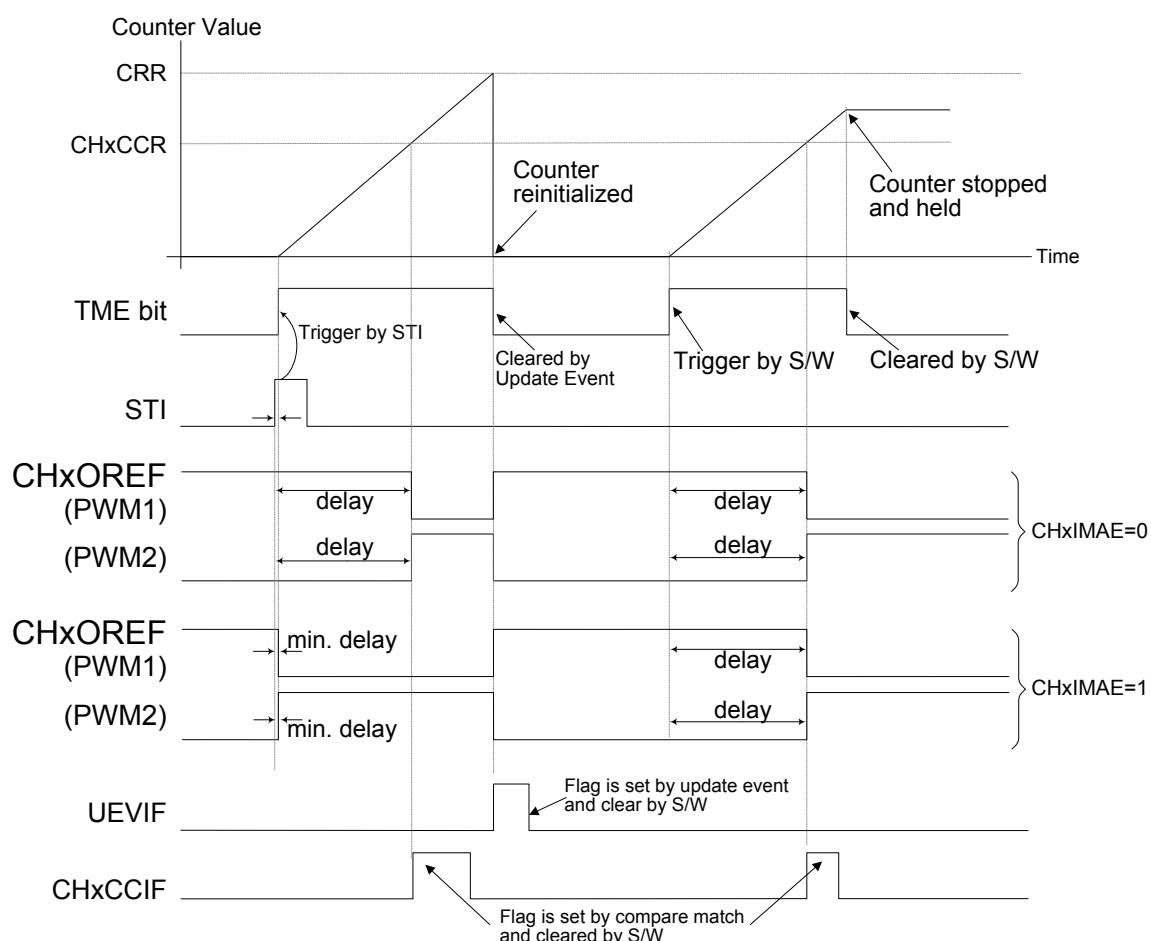


Figure 61. Single Pulse Mode

In the Single Pulse mode, the STI active edge which sets the TME bit to 1 will enable the counter. However, there exist several clock delays to perform the comparison result between the counter value and the CHxCCR value. In order to reduce the delay to a minimum value, the user can set the CHxIMAE bit in each CHxOCFR register. After a STI rising edge trigger occurs in the single pulse mode, the CHxOREF signal will immediately be forced to the state which the CHxOREF signal will change to as the compare match event occurs without taking the comparison result into account. The CHxIMAE bit is available only when the output channel is configured to operate in the PWM1 or PWM2 output mode and the trigger source is derived from the STI signal.

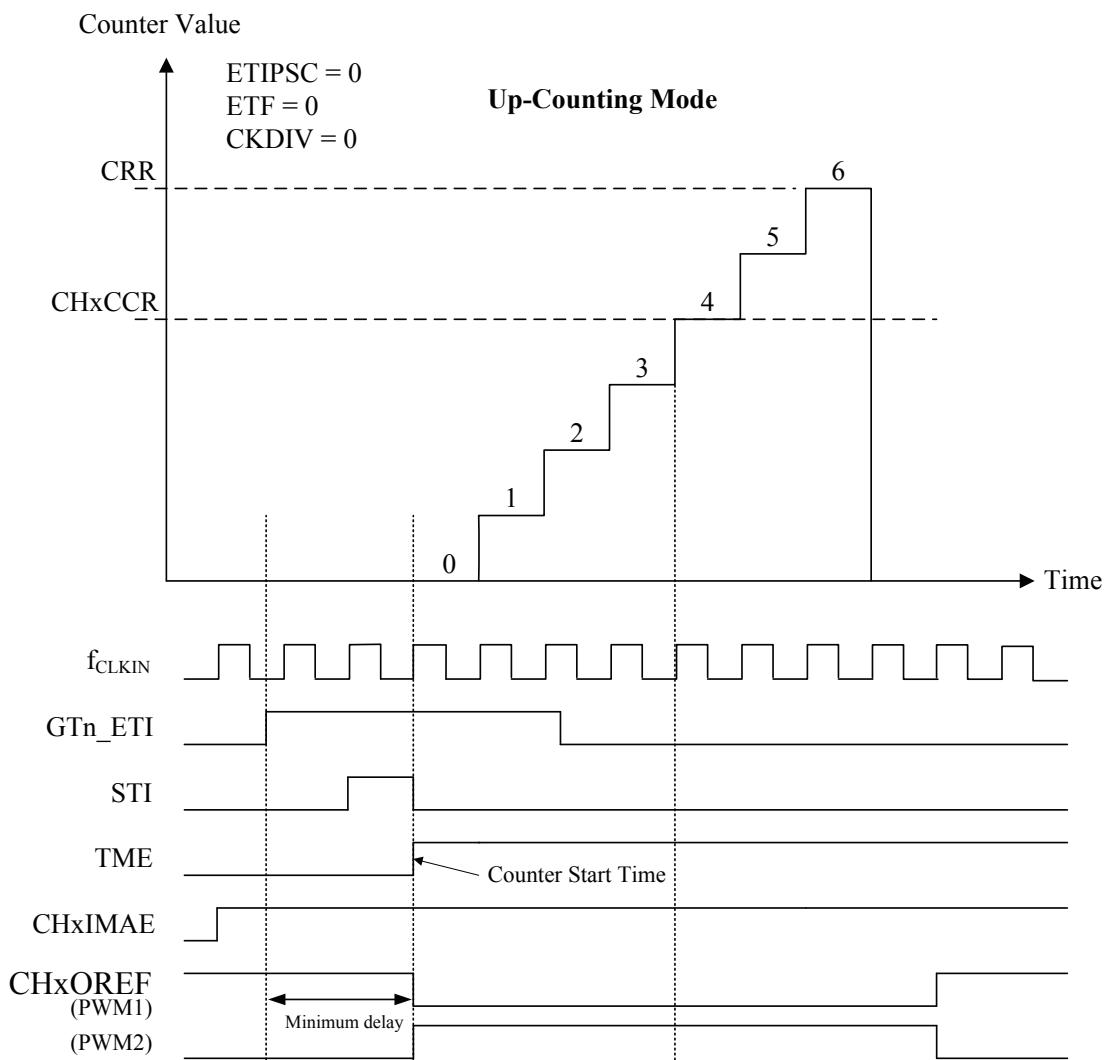


Figure 62. Immediate Active Mode Minimum Delay

Asymmetric PWM Mode

Asymmetric PWM mode allows two center-aligned PWM signals to be generated with a programmable phase shift. While the PWM frequency is determined by the value of the CRR register, the duty cycle and the phase-shift are determined by the CHxCCR and CHxACR register. When the counter is counting up, the PWM using the value in CHxCCR as up-count compare value. When the counter is into counting down stage, the PWM using the value in CHxACR as down-count compare value. The Figure 63 is shown an example for asymmetric PWM mode in center-aligned counting mode.

Note: Asymmetric PWM mode can only be operated in center-aligned counting mode.

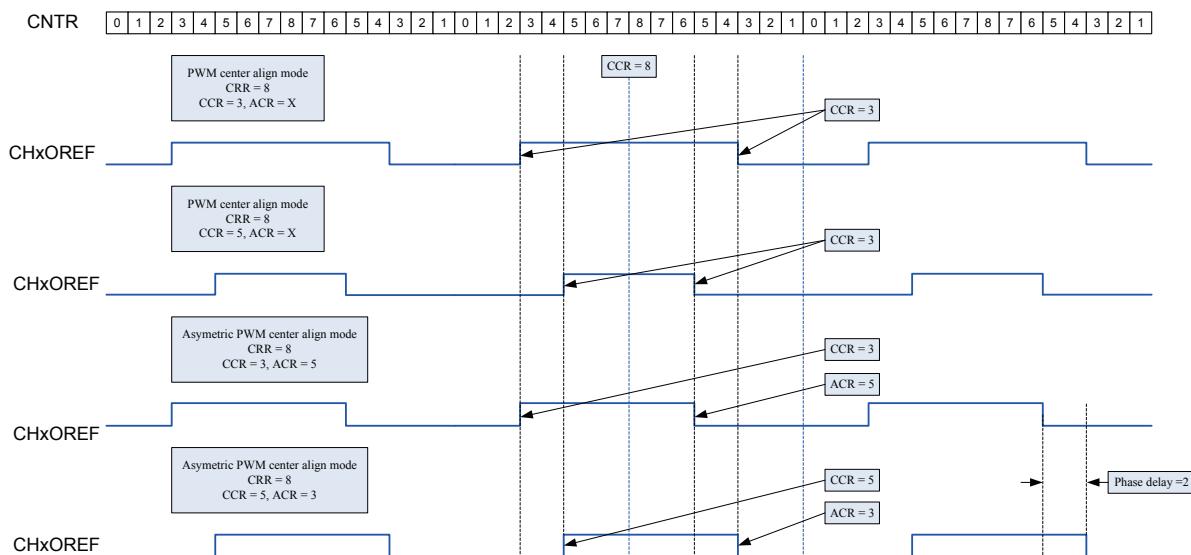


Figure 63. Asymmetric PWM mode versus center align counting mode

Timer Interconnection

The timers can be internally connected together for timer chaining or synchronization. This can be implemented by configuring one timer to operate in the Master mode while configuring another timer to be in the Slave mode. The following figures present several examples of trigger selection for the master and slave modes.

Using one timer to enable/disable another timer start or stop counting

- Configure GPTM0 as the master mode to send its channel 0 Output Reference signal CH0OREF as a trigger output (MMSEL = 0x04).
- Configure GPTM0 CH0OREF waveform.
- Configure GPTM1 to receive its input trigger source from the GPTM0 trigger output (TRSEL = 0x09).
- Configure GPTM1 to operate in the pause mode (SMSEL = 0x05).
- Enable GPTM1 by writing ‘1’ to the TME bit.
- Enable GPTM0 by writing ‘1’ to the TME bit.

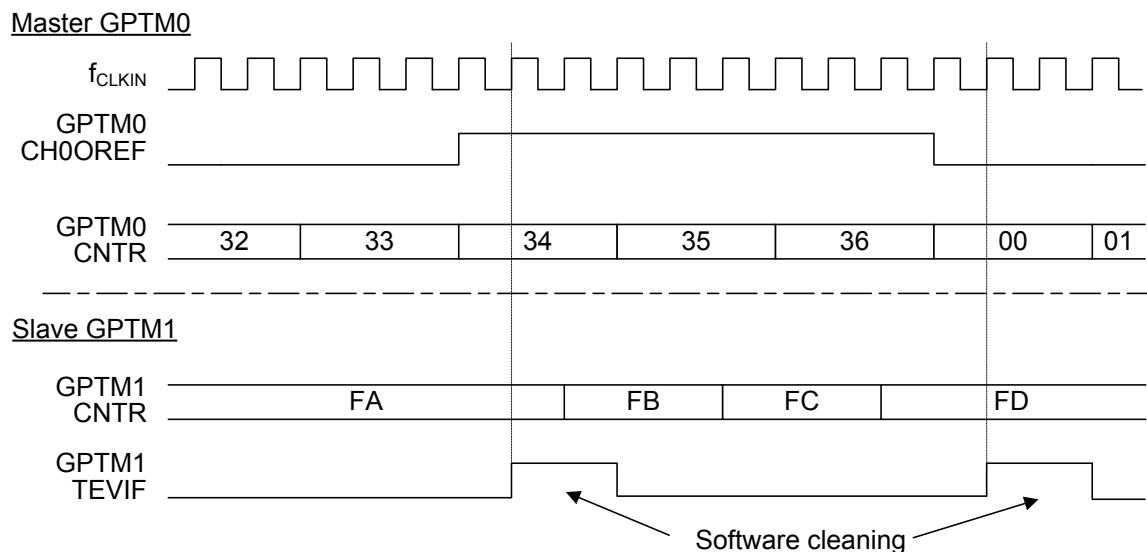


Figure 64. Pausing GPTM1 using the GPTM0 CH0OREF Signal

Using one timer to trigger another timer start counting

- Configure GPTM0 to operate in the master mode to send its Update Event UEV as the trigger output (MMSEL = 0x02).
- Configure the GPTM0 period by setting the CRR register.
- Configure GPTM1 to get the input trigger source from the GPTM0 trigger output (TRSEL = 0x09).
- Configure GPTM1 to be in the slave trigger mode (SMSEL = 0x06).
- Start GPTM0 by writing ‘1’ to the TME bit.

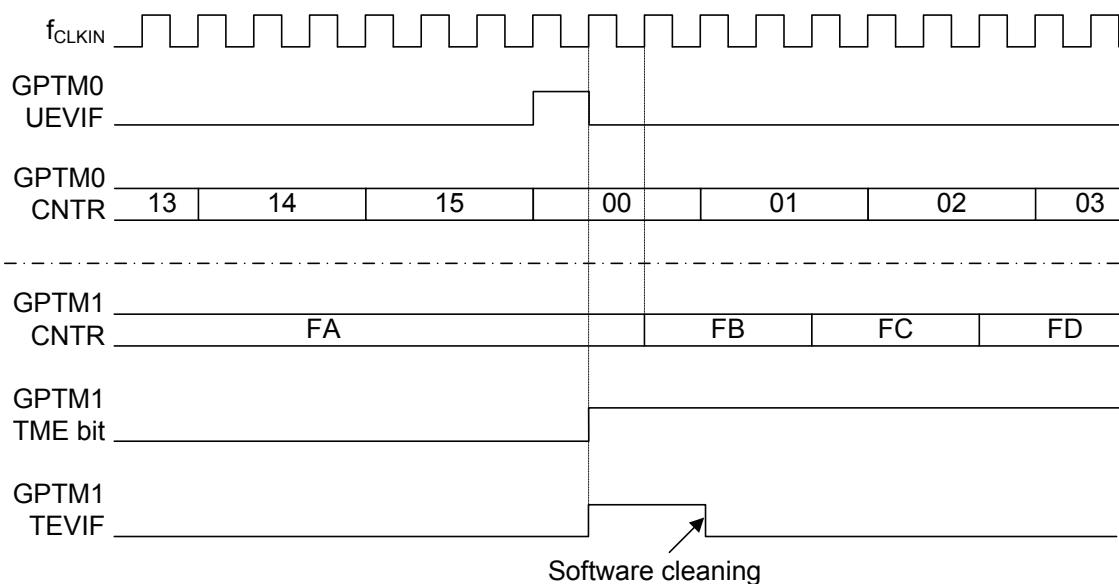
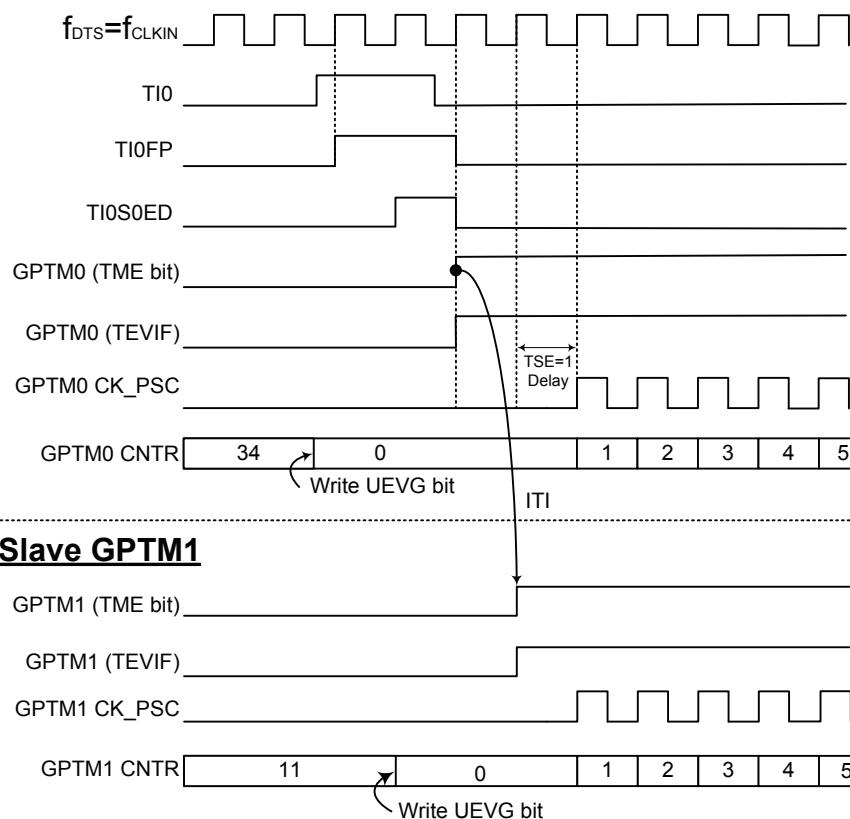


Figure 65. Triggering GPTM1 with GPTM0 Update Event

Starting two timers synchronously in response to an external trigger

- Configure GPTM0 to operate in the master mode to send its enable signal as a trigger output (MMSEL = 0x01).
- Configure GPTM0 slave mode to receive its input trigger source from GTn_CH0 pin (TRSEL = 0x01).
- Configure GPTM0 to be in the slave trigger mode (SMSEL = 0x06).
- Enable the GPTM0 master timer synchronization function by setting the TSE bit in the MDCFR register to 1 to synchronize the slave timer.
- Configure GPTM1 to receive its input trigger source from the GPTM0 trigger output (TRSEL = 0x09).
- Configure GPTM1 to be in the slave trigger mode (SMSEL = 0x06).

Master GPTM0



Slave GPTM1

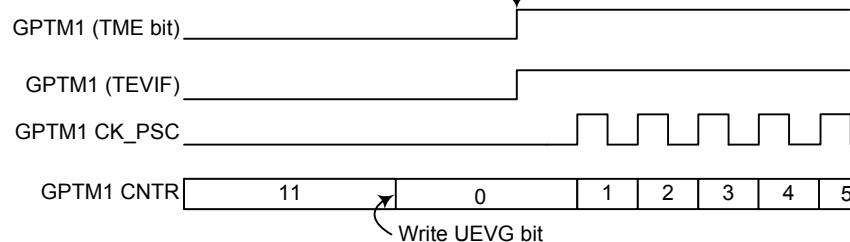


Figure 66. Trigger GPTM0 and GPTM1 with the GPTM0 CH0 Input

Trigger ADC Start

To interconnect with the Analog-to-Digital Converter, the GPTM can output the MTO signal or the channel output GTn_CHx (x = 0 ~ 3) signal to be used as the Analog-to-Digital Converter input trigger signal.

PDMA Request

The GPTM supports the interface for PDMA data transfer. There are certain events which can generate the PDMA requests if the corresponding enable control bits are set to 1 to enable the PDMA access. These events are the GPTM update events, trigger events and channel capture/compare events. When the PDMA request is generated from the GPTM channel, it can be derived from the channel capture/compare event or the GPTM update event selected by the channel PDMA selection bit, CHCCDS, for all channels. For more detailed PDMA configuring information, refer to the corresponding section in the PDMA chapter.

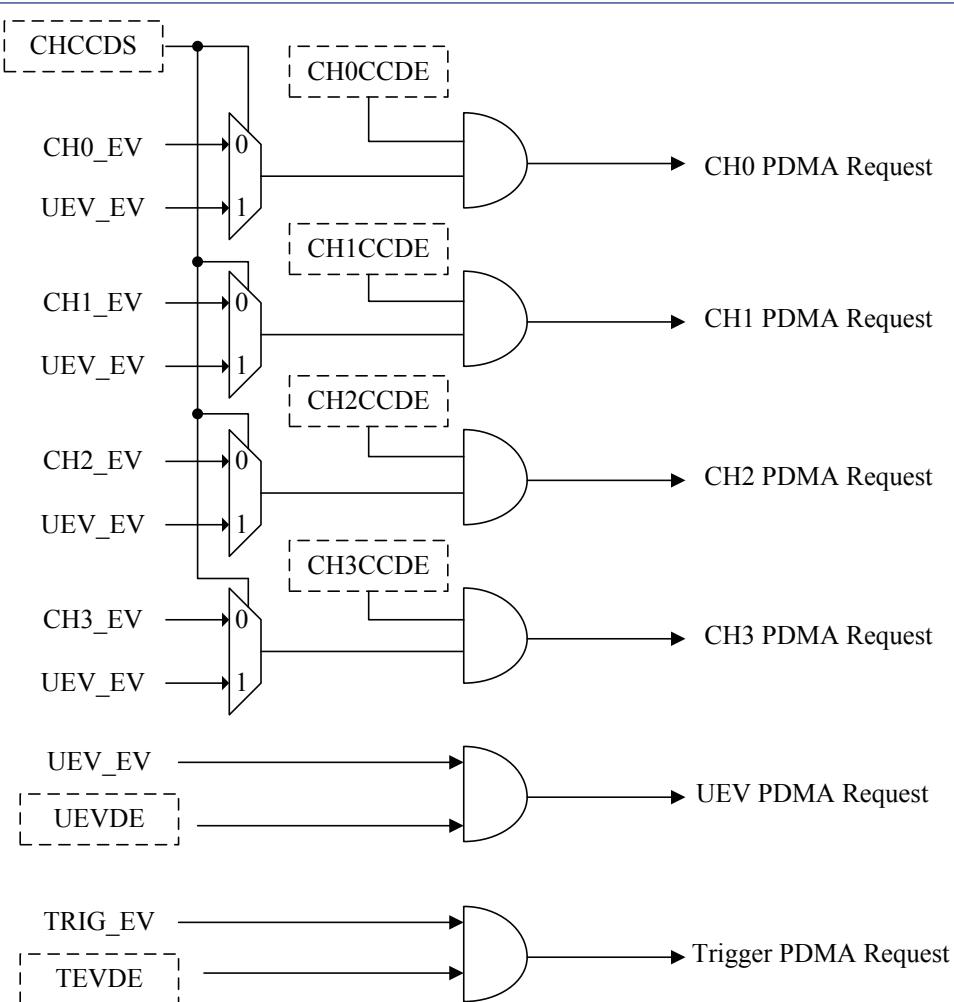


Figure 67. GPTM PDMA Mapping Diagram

Register Map

The following table shows the GPTM registers and reset values.

Table 32. GPTM Register Map

Register	Offset	Description	Reset Value
GPTM0 Base Address = 0x4006_E000			
GPTM1 Base Address = 0x4006_F000			
CNTCFR	0x000	Timer Counter Configuration Register	0x0000_0000
MDCFR	0x004	Timer Mode Configuration Register	0x0000_0000
TRCFR	0x008	Timer Trigger Configuration Register	0x0000_0000
CTR	0x010	Timer Control Register	0x0000_0000
CH0ICFR	0x020	Channel 0 Input Configuration Register	0x0000_0000
CH1ICFR	0x024	Channel 1 Input Configuration Register	0x0000_0000
CH2ICFR	0x028	Channel 2 Input Configuration Register	0x0000_0000
CH3ICFR	0x02C	Channel 3 Input Configuration Register	0x0000_0000
CH0OCFR	0x040	Channel 0 Output Configuration Register	0x0000_0000
CH1OCFR	0x044	Channel 1 Output Configuration Register	0x0000_0000
CH2OCFR	0x048	Channel 2 Output Configuration Register	0x0000_0000
CH3OCFR	0x04C	Channel 3 Output Configuration Register	0x0000_0000
CHCTR	0x050	Channel Control Register	0x0000_0000
CHPOLR	0x054	Channel Polarity Configuration Register	0x0000_0000
DICTR	0x074	Timer PDMA / Interrupt Control Register	0x0000_0000
EVGR	0x078	Timer Event Generator Register	0x0000_0000
INTSR	0x07C	Timer Interrupt Status Register	0x0000_0000
CNTR	0x080	Timer Counter Register	0x0000_0000
PSCR	0x084	Timer Prescaler Register	0x0000_0000
CRR	0x088	Timer Counter Reload Register	0x0000_FFFF
CH0CCR	0x090	Channel 0 Capture/Compare Register	0x0000_0000
CH1CCR	0x094	Channel 1 Capture/Compare Register	0x0000_0000
CH2CCR	0x098	Channel 2 Capture/Compare Register	0x0000_0000
CH3CCR	0x09C	Channel 3 Capture/Compare Register	0x0000_0000
CH0ACR	0x0A0	Channel 0 Asymmetric Compare Register	0x0000_0000
CH1ACR	0x0A4	Channel 1 Asymmetric Compare Register	0x0000_0000
CH2ACR	0x0A8	Channel 2 Asymmetric Compare Register	0x0000_0000
CH3ACR	0x0AC	Channel 3 Asymmetric Compare Register	0x0000_0000

Register Descriptions

Timer Counter Configuration Register – CNTCFR

This register specifies the GPTM counter configuration.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Type/Reset	Reserved							
	23	22	21	20	19	18	17	16
Type/Reset	Reserved							
	15	14	13	12	11	10	9	8
Type/Reset	Reserved							
	7	6	5	4	3	2	1	0
Type/Reset	Reserved							
							UGDIS	UEVDIS

Bits	Field	Descriptions
[24]	DIR	Counting Direction 0: Count-up 1: Count-down Note: This bit is read only when the Timer is configured to be in the Center-aligned mode or when used as a Quadrature decoder.
[17:16]	CMSEL	Counter Mode Selection 00: Edge aligned mode. Normal up-counting and down-counting available for this mode. Counting direction is defined by the DIR bit. 01: Center aligned mode 1. The counter counts up and down alternatively. The compare match interrupt flag is set during the count-down period. 10: Center aligned mode 2. The counter counts up and down alternatively. The compare match interrupt flag is set during the count-up period. 11: Center aligned mode 3. The counter counts up and down alternatively. The compare match interrupt flag is set during the count-up and count-down period.
[9:8]	CKDIV	Clock Division These two bits define the frequency ratio between the timer clock (f_{CLKIN}) and the dead-time clock (f_{DTS}). The dead-time clock is also used for digital filter sampling clock. 00: $f_{DTS} = f_{CLKIN}$ 01: $f_{DTS} = f_{CLKIN} / 2$ 10: $f_{DTS} = f_{CLKIN} / 4$ 11: Reserved

Bits	Field	Descriptions
[1]	UGDIS	Update event interrupt generation disable control 0: Any of the following events will generate an update PDMA request or interrupt - Counter overflow/underflow - Setting the UEVG bit - Update generation through the slave mode 1: Only counter overflow/underflow generates an update PDMA request or interrupt
[0]	UEVDIS	Update event Disable control 0: Enable the update event request by one of following events: - Counter overflow/underflow - Setting the UEVG bit - Update generation through the slave mode 1: Disable the update event (However the counter and the prescaler are reinitialized if the UEVG bit is set or if a hardware restart is received from the slave mode)

Timer Mode Configuration Register – MDCFR

This register specifies the GPTM master and slave mode selection and single pulse mode.

Offset: 0x004

Reset value: 0x0000_0000

Type/Reset	31	30	29	28	27	26	25	24
	Reserved					SPMSET		
								RW 0
Type/Reset	23	22	21	20	19	18	17	16
	Reserved					MMSEL		
								RW 0 RW 0 RW 0
Type/Reset	15	14	13	12	11	10	9	8
	Reserved					SMSEL		
								RW 0 RW 0 RW 0
Type/Reset	7	6	5	4	3	2	1	0
	Reserved					TSE		
								RW 0

Bits	Field	Descriptions
[24]	SPMSET	Single Pulse Mode Setting 0: Counter counts normally irrespective of whether the update event occurred or not. 1: Counter stops counting at the next update event and then the TME bit is cleared by hardware.

Bits	Field	Descriptions	
[18:16]	MMSEL	Master Mode Selection Master mode selection is used to select the MTO signal source which is used to synchronize the other slave timer.	
MMSEL [2:0]			
		Mode	Descriptions
	000	Reset Mode	The MTO in the Reset mode is an output derived from one of the following cases: Software setting UEVG bit The STI trigger input signal which will be output on the MTO signal line when the Timer is used in the slave Restart mode
	001	Enable Mode	The Counter Enable signal is used as the trigger output.
	010	Update Mode	The update event is used as the trigger output according to one of the following cases when the UEVDIS bit is cleared to 0: Counter overflow / underflow Software setting UEVG Slave trigger input when used in slave restart mode
	011	Capture/ Compare Mode	When a Channel 0 capture or compare match event occurs, it will generate a positive pulse used as the master trigger output.
	100	Compare Mode 0	The Channel 0 Output reference signal named CH0OREF is used as the trigger output.
	101	Compare Mode 1	The Channel 1 Output reference signal named CH1OREF is used as the trigger output.
	110	Compare Mode 2	The Channel 2 Output reference signal named CH2OREF is used as the trigger output.
	111	Compare Mode 3	The Channel 3 Output reference signal named CH3OREF is used as the trigger output.

Bits	Field	Descriptions		
[10:8]	SMSEL	Slave Mode Selection		
		SMSEL [2:0]	Mode	Descriptions
		000	Disable mode	The prescaler is clocked directly by the internal clock.
		001	Quadrature Decoder mode 1	The counter uses the clock pulse generated from the interaction between the TI0 and TI1 signals to drive the counter prescaler. A transition of the TI0 edge is used in this mode depending upon the TI1 level.
		010	Quadrature Decoder mode 2	The counter uses the clock pulse generated from the interaction between the TI0 and TI1 signals to drive the counter prescaler. A transition of the TI1 edge is used in this mode depending upon the TI0 level.
		011	Quadrature Decoder mode 3	The counter uses the clock pulse generated from the interaction between the TI0 and TI1 signals to drive the counter prescaler. A transition of one channel edge is used in the quadrature decoder mode 3 depending upon the other channel level.
		100	Restart Mode	The counter value restarts from 0 or the CRR shadow register value depending upon the counter mode on the rising edge of the STI signal. The registers will also be updated.
		101	Pause Mode	The counter starts to count when the selected trigger input STI is high. The counter stops counting on the instant, not being reset, when the STI signal changes its state to a low level. Both the counter start and stop control are determined by the STI signal.
		110	Trigger Mode	The counter starts to count from the original value in the counter on the rising edge of the selected trigger input STI. Only the counter start control is determined by the STI signal.
		111	STIED	The rising edge of the selected trigger signal STI will clock the counter.
[0]	TSE	Timer Synchronization Enable		
		0: No action 1: Master timer (current timer) will generate a delay to synchronize its slave timer through the MTO signal.		

Timer Trigger Configuration Register – TRCFR

This register specifies the GPTM external clock setting and the trigger source selection.

Offset: 0x008

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Type/Reset	Reserved							
	23	22	21	20	19	18	17	16
Type/Reset	Reserved							
	15	14	13	12	11	10	9	8
Type/Reset	Reserved		ETIPSC		ETF			
	7	6	5	4	3	2	1	0
Type/Reset	Reserved				TRSEL			

Bits	Field	Descriptions
[24]	ECME	External Clock Mode Enable 0: External clock mode is disabled 1: External clock mode is enabled If the ECME bit is set to 1 and the timer is configured to be in the STI trigger slave mode in which the trigger source is derived from the GTn_ETI pin, the external clock input on the GTn_ETI pin is used.
[16]	ETIPOL	External Trigger Polarity 0: GTn_ETI active at high level or rising edge 1: GTn_ETI active at low level or falling edge
[13:12]	ETIPSC	External Trigger Prescaler A prescaler can be enabled to reduce the ETIP frequency. 00: Prescaler OFF 01: ETIP frequency divided by 2 10: ETIP frequency divided by 4 11: ETIP frequency divided by 8

Bits	Field	Descriptions
[11:8]	ETF	<p>External Trigger Filter</p> <p>These bits define the frequency divided ratio that is used to sample the GTn_ETI signal. The digital filter in the GPTM is an N-event counter where N means how many valid transitions are necessary to output a filtered signal.</p> <ul style="list-style-type: none"> 0000: No filter, the sampling clock is f_{DTS} 0001: $f_{SAMPLING} = f_{CLKIN}$, N = 2 0010: $f_{SAMPLING} = f_{CLKIN}$, N = 4 0011: $f_{SAMPLING} = f_{CLKIN}$, N = 8 0100: $f_{SAMPLING} = f_{DTS} / 2$, N = 6 0101: $f_{SAMPLING} = f_{DTS} / 2$, N = 8 0110: $f_{SAMPLING} = f_{DTS} / 4$, N = 6 0111: $f_{SAMPLING} = f_{DTS} / 4$, N = 8 1000: $f_{SAMPLING} = f_{DTS} / 8$, N = 6 1001: $f_{SAMPLING} = f_{DTS} / 8$, N = 8 1010: $f_{SAMPLING} = f_{DTS} / 16$, N = 5 1011: $f_{SAMPLING} = f_{DTS} / 16$, N = 6 1100: $f_{SAMPLING} = f_{DTS} / 16$, N = 8 1101: $f_{SAMPLING} = f_{DTS} / 32$, N = 5 1110: $f_{SAMPLING} = f_{DTS} / 32$, N = 6 1111: $f_{SAMPLING} = f_{DTS} / 32$, N = 8
[3:0]	TRSEL	<p>Trigger Source Selection</p> <p>These bits are used to select the trigger input (STI) for counter synchronizing.</p> <ul style="list-style-type: none"> 0000: Software Trigger by setting the UEVG bit 0001: Filtered input of channel 0 (TI0S0) 0010: Filtered input of channel 1 (TI1S1) 0011: External Trigger input (ETIF) 1000: Channel 0 Edge Detector (TI0BED) 1001: Internal Timing Module Trigger 0 (ITI0) 1010: Internal Timing Module Trigger 1 (ITI1) 1011: Internal Timing Module Trigger 2 (ITI2) Others: Default 0 <p>Note: These bits must be updated only when they are not in use, i.e. the slave mode is disabled by setting the SMSEL field to 0x00.</p>

Table 33. GPTM Internal Trigger Connection

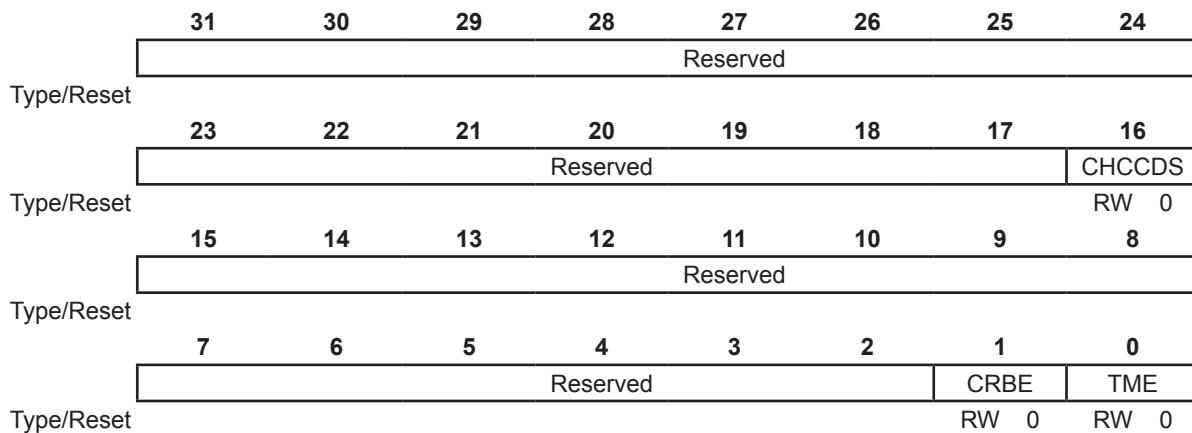
Slave Timing Module	ITI0	ITI1	ITI2
GPTM0	GPTM1	MCTM0	MCTM1
GPTM1	GPTM0	MCTM0	MCTM1

Timer Counter Register – CTR

This register specifies the timer enable bit (TME), CRR buffer enable bit (CRBE) and Channel PDMA selection bit (CHCCDS).

Offset: 0x010

Reset value: 0x0000_0000



Bits	Field	Descriptions
[16]	CHCCDS	Channel PDMA event selection 0: Channel PDMA request derived from the channel capture/compare event. 1: Channel PDMA request derived from the Update event.
[1]	CRBE	Counter-Reload register Buffer Enable 0: Counter reload register can be updated immediately 1: Counter reload register can not be updated until the update event occurs
[0]	TME	Timer Enable bit 0: GPTM off 1: GPTM on - GPTM functions normally When the TME bit is cleared to 0, the counter is stopped and the GPTM consumes no power in any operation mode except for the single pulse mode and the slave trigger mode. In these two modes the TME bit can automatically be set to 1 by hardware which permits all the GPTM registers to function normally.

Channel 0 Input Configuration Register – CH0ICFR

This register specifies the channel 0 input mode configuration.

Offset: 0x020

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Type/Reset	TI0SRC	Reserved						
	RW 0							
	23	22	21	20	19	18	17	16
Type/Reset	Reserved				CH0PSC		CH0CCS	
	15	14	13	12	11	10	9	8
Type/Reset	Reserved							
	7	6	5	4	3	2	1	0
Type/Reset	Reserved				TI0F			

Bits	Field	Descriptions
[31]	TI0SRC	Channel 0 Input Source TI0 Selection 0: The GTn_CH0 pin is connected to channel 0 input TI0 1: The XOR operation output of the GTn_CH0, GTn_CH1, and GTn_CH2 pins are connected to the channel 0 input TI0
[19:18]	CH0PSC	Channel 0 Capture Input Source Prescaler Setting These bits define the effective events of the channel 0 capture input. Note that the prescaler is reset once the Channel 0 Capture/Compare Enable bit, CH0E, in the Channel Control register named CHCTR is cleared to 0. 00: No prescaler, channel 0 capture input signal is chosen for each active event 01: Channel 0 Capture input signal is chosen for every 2 events 10: Channel 0 Capture input signal is chosen for every 4 events 11: Channel 0 Capture input signal is chosen for every 8 events
[17:16]	CH0CCS	Channel 0 Capture/Compare Selection 00: Channel 0 is configured as an output 01: Channel 0 is configured as an input derived from the TI0 signal 10: Channel 0 is configured as an input derived from the TI1 signal 11: Channel 0 is configured as an input which comes from the TRCED signal derived from the Trigger Controller Note: The CH0CCS field can be accessed only when the CH0E bit is cleared to 0.

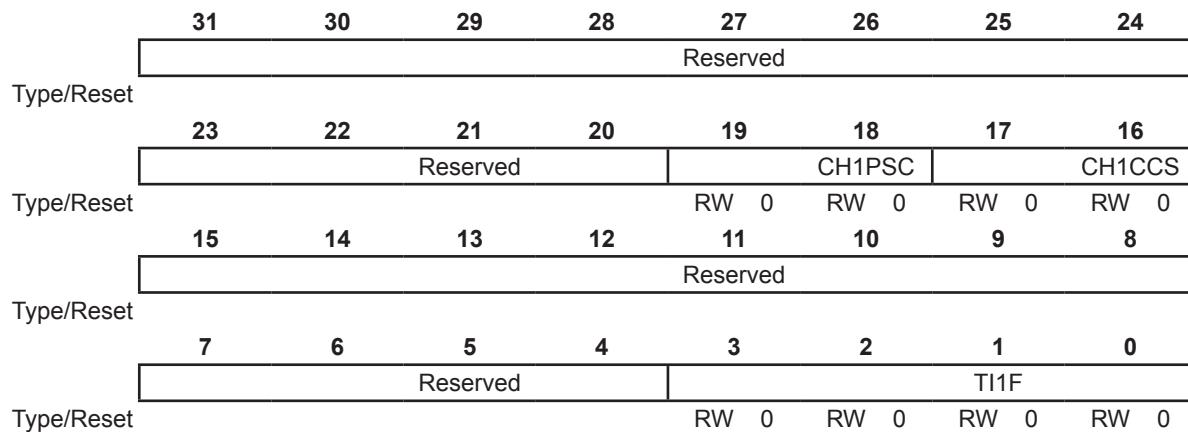
Bits	Field	Descriptions
[3:0]	TIOF	<p>Channel 0 Input Source TIO Filter Setting</p> <p>These bits define the frequency divided ratio used to sample the TIO signal. The Digital filter in the GPTM is an N-event counter where N is defined as how many valid transitions are necessary to output a filtered signal.</p> <ul style="list-style-type: none"> 0000: No filter, the sampling clock is f_{DTS}. 0001: $f_{SAMPLING} = f_{CLKIN}$, $N = 2$ 0010: $f_{SAMPLING} = f_{CLKIN}$, $N = 4$ 0011: $f_{SAMPLING} = f_{CLKIN}$, $N = 8$ 0100: $f_{SAMPLING} = f_{DTS} / 2$, $N = 6$ 0101: $f_{SAMPLING} = f_{DTS} / 2$, $N = 8$ 0110: $f_{SAMPLING} = f_{DTS} / 4$, $N = 6$ 0111: $f_{SAMPLING} = f_{DTS} / 4$, $N = 8$ 1000: $f_{SAMPLING} = f_{DTS} / 8$, $N = 6$ 1001: $f_{SAMPLING} = f_{DTS} / 8$, $N = 8$ 1010: $f_{SAMPLING} = f_{DTS} / 16$, $N = 5$ 1011: $f_{SAMPLING} = f_{DTS} / 16$, $N = 6$ 1100: $f_{SAMPLING} = f_{DTS} / 16$, $N = 8$ 1101: $f_{SAMPLING} = f_{DTS} / 32$, $N = 5$ 1110: $f_{SAMPLING} = f_{DTS} / 32$, $N = 6$ 1111: $f_{SAMPLING} = f_{DTS} / 32$, $N = 8$

Channel 1 Input Configuration Register – CH1ICFR

This register specifies the channel 1 input mode configuration.

Offset: 0x024

Reset value: 0x0000_0000



Bits	Field	Descriptions
[19:18]	CH1PSC	<p>Channel 1 Capture Input Source Prescaler Setting</p> <p>These bits define the effective events of the channel 1 capture input. Note that the prescaler is reset once the Channel 1 Capture/Compare Enable bit, CH1E, in the Channel Control register named CHCTR is cleared to 0.</p> <ul style="list-style-type: none"> 00: No prescaler, channel 1 capture input signal is chosen for each active event 01: Channel 1 Capture input signal is chosen for every 2 events 10: Channel 1 Capture input signal is chosen for every 4 events 11: Channel 1 Capture input signal is chosen for every 8 events
[17:16]	CH1CCS	<p>Channel 1 Capture/Compare Selection</p> <ul style="list-style-type: none"> 00: Channel 1 is configured as an output 01: Channel 1 is configured as an input derived from the TI1 signal 10: Channel 1 is configured as an input derived from the TI0 signal 11: Channel 1 is configured as an input which comes from the TRCED signal derived from the Trigger Controller <p>Note: The CH1CCS field can be accessed only when the CH1E bit is cleared to 0.</p>

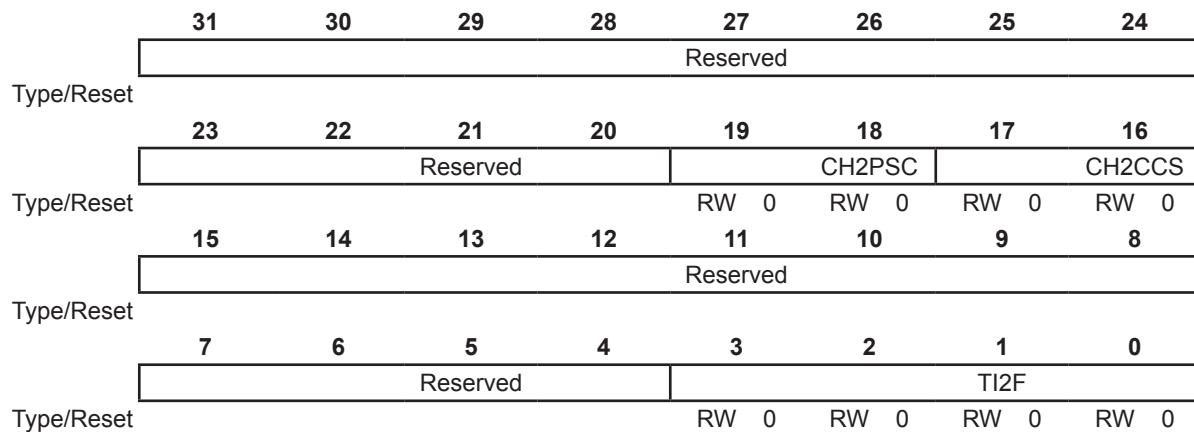
Bits	Field	Descriptions
[3:0]	TI1F	<p>Channel 1 Input Source TI1 Filter Setting</p> <p>These bits define the frequency divided ratio used to sample the TI1 signal. The Digital filter in the GPTM is an N-event counter where N is defined as how many valid transitions are necessary to output a filtered signal.</p> <ul style="list-style-type: none"> 0000: No filter, the sampling clock is f_{DTS}. 0001: $f_{SAMPLING} = f_{CLKIN}$, N = 2 0010: $f_{SAMPLING} = f_{CLKIN}$, N = 4 0011: $f_{SAMPLING} = f_{CLKIN}$, N = 8 0100: $f_{SAMPLING} = f_{DTS} / 2$, N = 6 0101: $f_{SAMPLING} = f_{DTS} / 2$, N = 8 0110: $f_{SAMPLING} = f_{DTS} / 4$, N = 6 0111: $f_{SAMPLING} = f_{DTS} / 4$, N = 8 1000: $f_{SAMPLING} = f_{DTS} / 8$, N = 6 1001: $f_{SAMPLING} = f_{DTS} / 8$, N = 8 1010: $f_{SAMPLING} = f_{DTS} / 16$, N = 5 1011: $f_{SAMPLING} = f_{DTS} / 16$, N = 6 1100: $f_{SAMPLING} = f_{DTS} / 16$, N = 8 1101: $f_{SAMPLING} = f_{DTS} / 32$, N = 5 1110: $f_{SAMPLING} = f_{DTS} / 32$, N = 6 1111: $f_{SAMPLING} = f_{DTS} / 32$, N = 8

Channel 2 Input Configuration Register – CH2ICFR

This register specifies the channel 2 input mode configuration.

Offset: 0x028

Reset value: 0x0000_0000



Bits	Field	Descriptions
[19:18]	CH2PSC	<p>Channel 2 Capture Input Source Prescaler Setting</p> <p>These bits define the effective events of the channel 2 capture input. Note that the prescaler is reset once the Channel 2 Capture/Compare Enable bit, CH2E, in the Channel Control register named CHCTR is cleared to 0.</p> <ul style="list-style-type: none"> 00: No prescaler, channel 2 capture input signal is chosen for each active event 01: Channel 2 Capture input signal is chosen for every 2 events 10: Channel 2 Capture input signal is chosen for every 4 events 11: Channel 2 Capture input signal is chosen for every 8 events
[17:16]	CH2CCS	<p>Channel 2 Capture/Compare Selection</p> <ul style="list-style-type: none"> 00: Channel 2 is configured as an output 01: Channel 2 is configured as an input derived from the TI2 signal 10: Channel 2 is configured as an input derived from the TI3 signal 11: Channel 2 is configured as an input which comes from the TRCED signal derived from the Trigger Controller <p>Note: The CH2CCS field can be accessed only when the CH2E bit is cleared to 0</p>

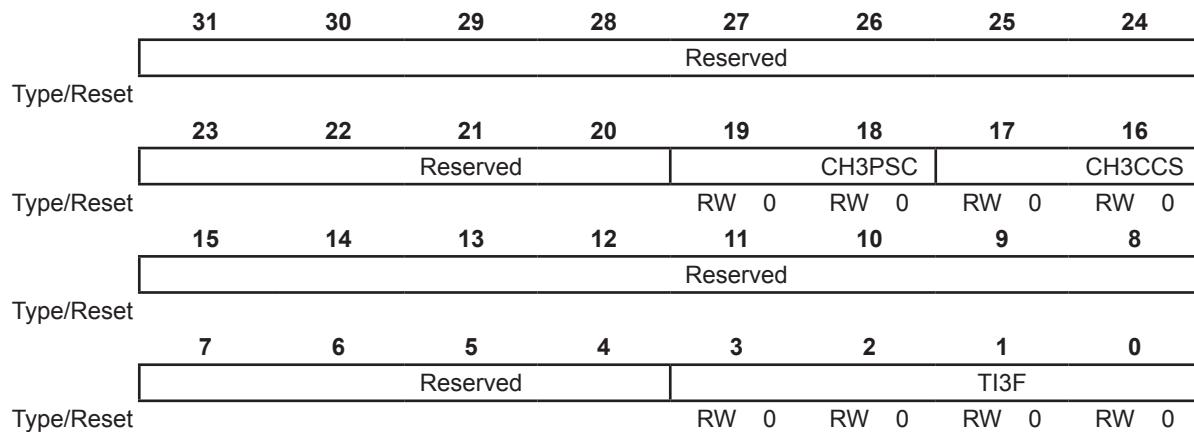
Bits	Field	Descriptions
[3:0]	TI2F	<p>Channel 2 Input Source TI2 Filter Setting</p> <p>These bits define the frequency divided ratio used to sample the TI2 signal. The Digital filter in the GPTM is an N-event counter where N is defined as how many valid transitions are necessary to output a filtered signal.</p> <ul style="list-style-type: none"> 0000: No filter, the sampling clock is f_{DTS}. 0001: $f_{SAMPLING} = f_{CLKIN}$, $N = 2$ 0010: $f_{SAMPLING} = f_{CLKIN}$, $N = 4$ 0011: $f_{SAMPLING} = f_{CLKIN}$, $N = 8$ 0100: $f_{SAMPLING} = f_{DTS} / 2$, $N = 6$ 0101: $f_{SAMPLING} = f_{DTS} / 2$, $N = 8$ 0110: $f_{SAMPLING} = f_{DTS} / 4$, $N = 6$ 0111: $f_{SAMPLING} = f_{DTS} / 4$, $N = 8$ 1000: $f_{SAMPLING} = f_{DTS} / 8$, $N = 6$ 1001: $f_{SAMPLING} = f_{DTS} / 8$, $N = 8$ 1010: $f_{SAMPLING} = f_{DTS} / 16$, $N = 5$ 1011: $f_{SAMPLING} = f_{DTS} / 16$, $N = 6$ 1100: $f_{SAMPLING} = f_{DTS} / 16$, $N = 8$ 1101: $f_{SAMPLING} = f_{DTS} / 32$, $N = 5$ 1110: $f_{SAMPLING} = f_{DTS} / 32$, $N = 6$ 1111: $f_{SAMPLING} = f_{DTS} / 32$, $N = 8$

Channel 3 Input Configuration Register – CH3ICFR

This register specifies the channel 3 input mode configuration.

Offset: 0x02C

Reset value: 0x0000_0000



Bits	Field	Descriptions
[19:18]	CH3PSC	<p>Channel 3 Capture Input Source Prescaler Setting</p> <p>These bits define the effective events of the channel 3 capture input. Note that the prescaler is reset once the Channel 3 Capture/Compare Enable bit, CH3E, in the Channel Control register named CHCTR is cleared to 0.</p> <ul style="list-style-type: none"> 00: No prescaler, channel 3 capture input signal is chosen for each active event 01: Channel 3 Capture input signal is chosen for every 2 events 10: Channel 3 Capture input signal is chosen for every 4 events 11: Channel 3 Capture input signal is chosen for every 8 events
[17:16]	CH3CCS	<p>Channel 3 Capture/Compare Selection</p> <ul style="list-style-type: none"> 00: Channel 3 is configured as an output 01: Channel 3 is configured as an input derived from the TI3 signal 10: Channel 3 is configured as an input derived from the TI2 signal 11: Channel 3 is configured as an input which comes from the TRCED signal derived from the Trigger Controller <p>Note: The CH3CCS field can be accessed only when the CH3E bit is cleared to 0</p>

Bits	Field	Descriptions
[3:0]	TI3F	<p>Channel 3 Input Source TI3 Filter Setting</p> <p>These bits define the frequency divided ratio used to sample the TI3 signal. The Digital filter in the GPTM is an N-event counter where N is defined as how many valid transitions are necessary to output a filtered signal.</p> <ul style="list-style-type: none"> 0000: No filter, the sampling clock is f_{DTS}. 0001: $f_{SAMPLING} = f_{CLKIN}$, N = 2 0010: $f_{SAMPLING} = f_{CLKIN}$, N = 4 0011: $f_{SAMPLING} = f_{CLKIN}$, N = 8 0100: $f_{SAMPLING} = f_{DTS} / 2$, N = 6 0101: $f_{SAMPLING} = f_{DTS} / 2$, N = 8 0110: $f_{SAMPLING} = f_{DTS} / 4$, N = 6 0111: $f_{SAMPLING} = f_{DTS} / 4$, N = 8 1000: $f_{SAMPLING} = f_{DTS} / 8$, N = 6 1001: $f_{SAMPLING} = f_{DTS} / 8$, N = 8 1010: $f_{SAMPLING} = f_{DTS} / 16$, N = 5 1011: $f_{SAMPLING} = f_{DTS} / 16$, N = 6 1100: $f_{SAMPLING} = f_{DTS} / 16$, N = 8 1101: $f_{SAMPLING} = f_{DTS} / 32$, N = 5 1110: $f_{SAMPLING} = f_{DTS} / 32$, N = 6 1111: $f_{SAMPLING} = f_{DTS} / 32$, N = 8

Channel 0 Output Configuration Register – CH0OCFR

This register specifies the channel 0 output mode configuration.

Offset: 0x040

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24	
Type/Reset	Reserved								
	23	22	21	20	19	18	17	16	
Type/Reset	Reserved								
	15	14	13	12	11	10	9	8	
Type/Reset	Reserved							CH0OM[3]	
	7	6	5	4	3	2	1	0	
Type/Reset	Reserved	CH0IMAE	CH0PRE	REF0CE	CH0OM[2:0]				
	RW	0	RW	0	RW	0	RW	0	

Bits	Field	Descriptions
[5]	CH0IMAE	<p>Channel 0 Immediate Active Enable</p> <p>0: No action 1: Single pulse Immediate Active Mode is enabled</p> <p>The CH0OREF will be forced to the compare matched level immediately after an available trigger event occurs irrespective of the result of the comparison between the CNTR and the CH0CCR values.</p> <p>The effective duration ends automatically at the next overflow or underflow event.</p> <p>Note: The CH0IMAE bit is available only if the channel 0 is configured to be operated in the PWM mode 1 or the PWM mode 2.</p>
[4]	CH0PRE	<p>Channel 0 Capture/Compare Register (CH0CCR) Preload Enable</p> <p>0: CH0CCR preload function is disabled. The CH0CCR register can be immediately assigned a new value when the CH0PRE bit is cleared to 0 and the updated CH0CCR value is used immediately.</p> <p>1: CH0CCR preload function is enabled. The new CH0CCR value will not be transferred to its shadow register until the update event occurs.</p>
[3]	REF0CE	<p>Channel 0 Reference Output Clear Enable</p> <p>0: CH0OREF performed normally and is not affected by the ETIF signal 1: CH0OREF is forced to 0 on the high level of the ETIF signal derived from the GTn_ETI pin</p>

Bits	Field	Descriptions
[8][2:0]	CH0OM[3:0]	<p>Channel 0 Output Mode Setting</p> <p>These bits define the functional types of the output reference signal CH0OREF.</p> <ul style="list-style-type: none"> 0000: No Change 0001: Output 0 on compare match 0010: Output 1 on compare match 0011: Output toggles on compare match 0100: Force inactive – CH0OREF is forced to 0 0101: Force active – CH0OREF is forced to 1 0110: PWM mode 1 <ul style="list-style-type: none"> - During up-counting, channel 0 has an active level when CNTR < CH0CCR or otherwise has an inactive level. - During down-counting, channel 0 has an inactive level when CNTR > CH0CCR or otherwise has an active level. 0111: PWM mode 2 <ul style="list-style-type: none"> - During up-counting, channel 0 has an inactive level when CNTR < CH0CCR or otherwise has an active level. - During down-counting, channel 0 has an active level when CNTR > CH0CCR or otherwise has an inactive level. 1110: Asymmetric PWM mode 1 <ul style="list-style-type: none"> - During up-counting, channel 0 has an active level when CNTR < CH0CCR or otherwise has an inactive level. - During down-counting, channel 0 has an inactive level when CNTR > CH0ACR or otherwise has an active level. 1111: Asymmetric PWM mode 2 <ul style="list-style-type: none"> - During up-counting, channel 0 has an inactive level when CNTR < CH0CCR or otherwise has an active level. - During down-counting, channel 0 has an active level when CNTR > CH0ACR or otherwise has an inactive level

Note: When channel 0 is used as asymmetric PWM output mode, the Counter Mode. Selection bit in Counter Configuration Register must be configured as Center-aligned Counting mode (CMSEL = 01/02/03).

Channel 1 Output Configuration Register – CH1OCFR

This register specifies the channel 1 output mode configuration.

Offset: 0x044

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24	
Type/Reset	Reserved								
	23	22	21	20	19	18	17	16	
Type/Reset	Reserved								
	15	14	13	12	11	10	9	8	
Type/Reset	Reserved								CH1OM[3]
	7	6	5	4	3	2	1	0	
Type/Reset	Reserved		RW 0						
	CH1OM[2:0]								

Bits	Field	Descriptions
[5]	CH1IMAE	<p>Channel 1 Immediate Active Enable</p> <p>0: No action 1: Single pulse Immediate Active Mode is enabled</p> <p>The CH1OREF will be forced to the compare matched level immediately after an available trigger event occurs irrespective of the result of the comparison between the CNTR and the CH1CCR values.</p> <p>The effective duration ends automatically at the next overflow or underflow event.</p> <p>Note: The CH1IMAE bit is available only if the channel 1 is configured to be operated in the PWM mode 1 or the PWM mode 2.</p>
[4]	CH1PRE	<p>Channel 1 Capture/Compare Register (CH1CCR) Preload Enable</p> <p>0: CH1CCR preload function is disabled. The CH1CCR register can be immediately assigned a new value when the CH1PRE bit is cleared to 0 and the updated CH1CCR value is used immediately.</p> <p>1: CH1CCR preload function is enabled The new CH1CCR value will not be transferred to its shadow register until the update event occurs.</p>
[3]	REF1CE	<p>Channel 1 Reference Output Clear Enable</p> <p>0: CH1OREF performed normally and is not affected by the ETIF signal 1: CH1OREF is forced to 0 on the high level of the ETIF signal derived from the GTn_ETI pin</p>

Bits	Field	Descriptions
[8][2:0]	CH1OM[3:0]	<p>Channel 1 Output Mode Setting</p> <p>These bits define the functional types of the output reference signal CH1OREF.</p> <ul style="list-style-type: none"> 0000: No Change 0001: Output 0 on compare match 0010: Output 1 on compare match 0011: Output toggles on compare match 0100: Force inactive – CH1OREF is forced to 0 0101: Force active – CH1OREF is forced to 1 0110: PWM mode 1 <ul style="list-style-type: none"> - During up-counting, channel 1 has an active level when CNTR < CH1CCR or otherwise has an inactive level. - During down-counting, channel 1 has an inactive level when CNTR > CH1CCR or otherwise has an active level. 0111: PWM mode 2 <ul style="list-style-type: none"> - During up-counting, channel 1 has an inactive level when CNTR < CH1CCR or otherwise has an active level. - During down-counting, channel 1 has an active level when CNTR > CH1CCR or otherwise has an inactive level. 1110: Asymmetric PWM mode 1 <ul style="list-style-type: none"> - During up-counting, channel 1 has an active level when CNTR < CH1CCR or otherwise has an inactive level. - During down-counting, channel 1 has an inactive level when CNTR > CH1ACR or otherwise has an active level. 1111: Asymmetric PWM mode 2 <ul style="list-style-type: none"> - During up-counting, channel 1 has an inactive level when CNTR < CH1CCR or otherwise has an active level. - During down-counting, channel 1 has an active level when CNTR > CH1ACR or otherwise has an inactive level

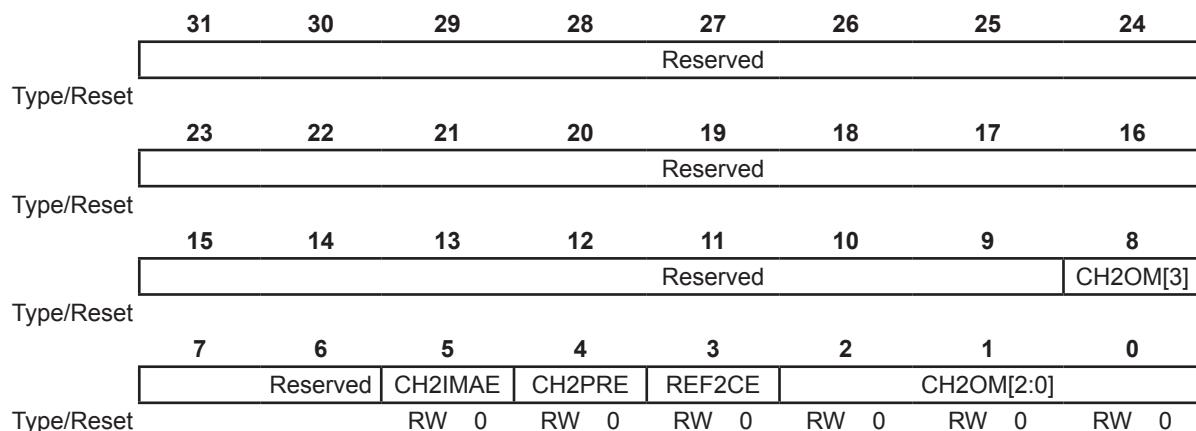
Note: When channel 1 is used as asymmetric PWM output mode, the Counter Mode Selection bit in Counter Configuration Register must be configured as Center-aligned Counting mode (CMSEL = 01/02/03).

Channel 2 Output Configuration Register – CH2OCFR

This register specifies the channel 2 output mode configuration.

Offset: 0x048

Reset value: 0x0000_0000



Bits	Field	Descriptions
[5]	CH2IMAE	<p>Channel 2 Immediate Active Enable</p> <p>0: No action 1: Single pulse Immediate Active Mode is enabled</p> <p>The CH2OREF will be forced to the compare matched level immediately after an available trigger event occurs irrespective of the result of the comparison between the CNTR and the CH2CCR values.</p> <p>The effective duration ends automatically at the next overflow or underflow event.</p> <p>Note: The CH2IMAE bit is available only if the channel 2 is configured to be operated in the PWM mode 1 or the PWM mode 2.</p>
[4]	CH2PRE	<p>Channel 2 Capture/Compare Register (CH2CCR) Preload Enable</p> <p>0: CH2CCR preload function is disabled. The CH2CCR register can be immediately assigned a new value when the CH2PRE bit is cleared to 0 and the updated CH2CCR value is used immediately.</p> <p>1: CH2CCR preload function is enabled The new CH2CCR value will not be transferred to its shadow register until the update event occurs.</p>
[3]	REF2CE	<p>Channel 2 Reference Output Clear Enable</p> <p>0: CH2OREF performed normally and is not affected by the ETIF signal 1: CH2OREF is forced to 0 on the high level of the ETIF signal derived from the GTn_ETI pin</p>

Bits	Field	Descriptions
[8][2:0]	CH2OM[3:0]	<p>Channel 2 Output Mode Setting</p> <p>These bits define the functional types of the output reference signal CH2OREF.</p> <ul style="list-style-type: none"> 0000: No Change 0001: Output 0 on compare match 0010: Output 1 on compare match 0011: Output toggles on compare match 0100: Force inactive – CH2OREF is forced to 0 0101: Force active – CH2OREF is forced to 1 0110: PWM mode 1 <ul style="list-style-type: none"> - During up-counting, channel 2 has an active level when CNTR < CH2CCR or otherwise has an inactive level. - During down-counting, channel 2 has an inactive level when CNTR > CH2CCR or otherwise has an active level. 0111: PWM mode 2 <ul style="list-style-type: none"> - During up-counting, channel 2 has an inactive level when CNTR < CH2CCR or otherwise has an active level. - During down-counting, channel 2 has an active level when CNTR > CH2CCR or otherwise has an inactive level. 1110: Asymmetric PWM mode 1 <ul style="list-style-type: none"> - During up-counting, channel 2 has an active level when CNTR < CH2CCR or otherwise has an inactive level. - During down-counting, channel 2 has an inactive level when CNTR > CH2ACR or otherwise has an active level. 1111: Asymmetric PWM mode 2 <ul style="list-style-type: none"> - During up-counting, channel 2 has an inactive level when CNTR < CH2CCR or otherwise has an active level. - During down-counting, channel 2 has an active level when CNTR > CH2ACR or otherwise has an inactive level

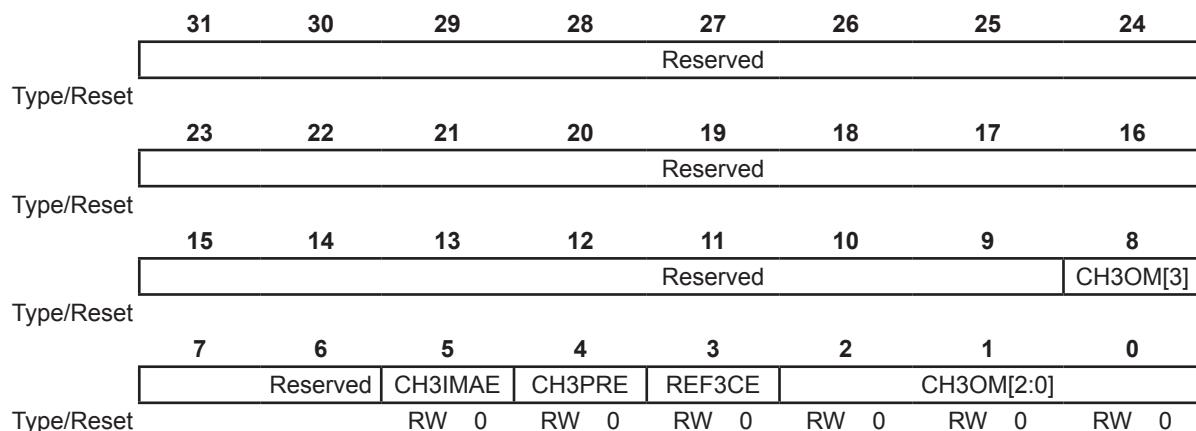
Note: When channel 2 is used as asymmetric PWM output mode, the Counter Mode. Selection bit in Counter Configuration Register must be configured as Center-aligned Counting mode (CMSEL = 01/02/03).

Channel 3 Output Configuration Register – CH3OCFR

This register specifies the channel 3 output mode configuration.

Offset: 0x04C

Reset value: 0x0000_0000



Bits	Field	Descriptions
[5]	CH3IMAE	<p>Channel 3 Immediate Active Enable</p> <p>0: No action 1: Single pulse Immediate Active Mode is enabled</p> <p>The CH3OREF will be forced to the compare matched level immediately after an available trigger event occurs irrespective of the result of the comparison between the CNTR and the CH3CCR values.</p> <p>The effective duration ends automatically at the next overflow or underflow event.</p> <p>Note: The CH3IMAE bit is available only if the channel 3 is configured to be operated in the PWM mode 1 or the PWM mode 2.</p>
[4]	CH3PRE	<p>Channel 3 Capture/Compare Register (CH3CCR) Preload Enable</p> <p>0: CH3CCR preload function is disabled. The CH3CCR register can be immediately assigned a new value when the CH3PRE bit is cleared to 0 and the updated CH3CCR value is used immediately.</p> <p>1: CH3CCR preload function is enabled The new CH3CCR value will not be transferred to its shadow register until the update event occurs.</p>
[3]	REF3CE	<p>Channel 3 Reference Output Clear Enable</p> <p>0: CH3OREF performed normally and is not affected by the ETIF signal 1: CH3OREF is forced to 0 on the high level of the ETIF signal derived from the GTn_ETI pin</p>

Bits	Field	Descriptions
[8][2:0]	CH3OM[3:0]	<p>Channel 3 Output Mode Setting</p> <p>These bits define the functional types of the output reference signal CH3OREF</p> <ul style="list-style-type: none"> 0000: No Change 0001: Output 0 on compare match 0010: Output 1 on compare match 0011: Output toggles on compare match 0100: Force inactive – CH3OREF is forced to 0 0101: Force active – CH3OREF is forced to 1 0110: PWM mode 1 <ul style="list-style-type: none"> - During up-counting, channel 3 has an active level when CNTR < CH3CCR or otherwise has an inactive level. - During down-counting, channel 3 has an inactive level when CNTR > CH3CCR or otherwise has an active level. 0111: PWM mode 2 <ul style="list-style-type: none"> - During up-counting, channel 3 has an inactive level when CNTR < CH3CCR or otherwise has an active level. - During down-counting, channel 3 has an active level when CNTR > CH3CCR or otherwise has an inactive level 1110: Asymmetric PWM mode 1 <ul style="list-style-type: none"> - During up-counting, channel 3 has an active level when CNTR < CH3CCR or otherwise has an inactive level. - During down-counting, channel 3 has an inactive level when CNTR > CH3ACR or otherwise has an active level. 1111: Asymmetric PWM mode 2 <ul style="list-style-type: none"> - During up-counting, channel 3 has an inactive level when CNTR < CH3CCR or otherwise has an active level. - During down-counting, channel 3 has an active level when CNTR > CH3ACR or otherwise has an inactive level

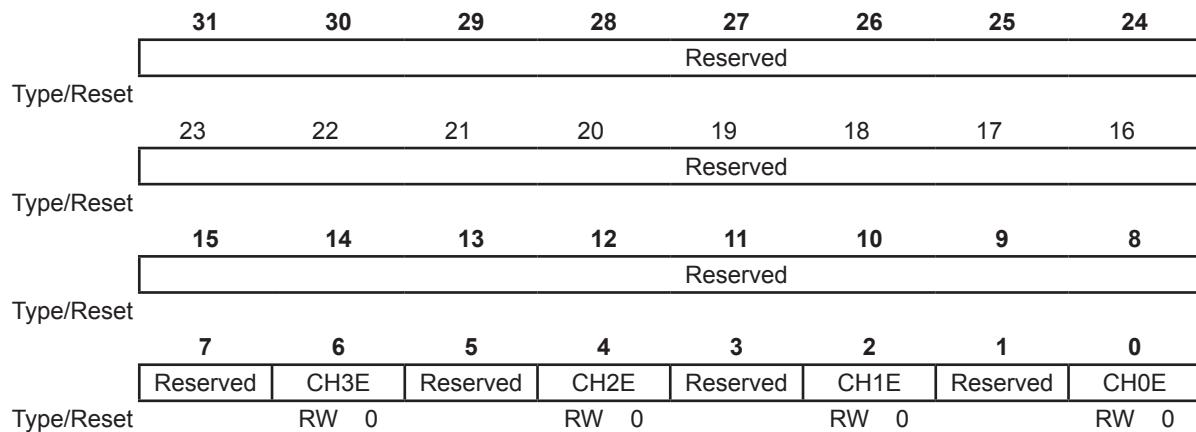
Note: When channel 3 is used as asymmetric PWM output mode, the Counter Mode Selection bit in Counter Configuration Register must be configured as Center-aligned Counting mode (CMSEL = 01/02/03).

Channel Control Register – CHCTR

This register contains the channel capture input or compare output function enable control bits.

Offset: 0x050

Reset value: 0x0000_0000



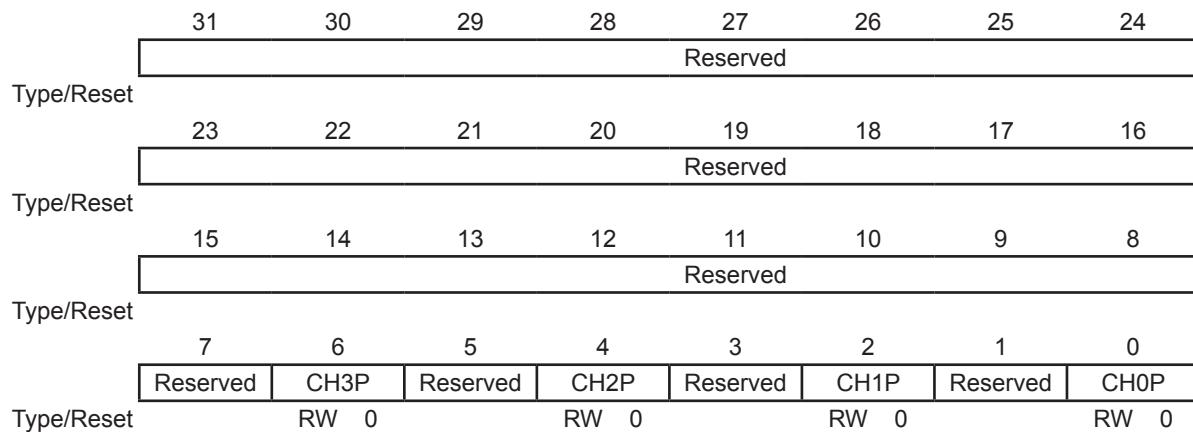
Bits	Field	Descriptions
[6]	CH3E	Channel 3 Capture/Compare Enable - Channel 3 is configured as an input (CH3CCS = 0x01/0x02/0x03) 0: Input Capture Mode disabled 1: Input Capture Mode enabled - Channel 3 is configured as an output (CH3CCS = 0x00) 0: Off –Channel 3 output signal CH3O is not active 1: On –Channel 3 output signal CH3O generated on the corresponding output pin
[4]	CH2E	Channel 2 Capture/Compare Enable - Channel 2 is configured as an input (CH2CCS = 0x01/0x02/0x03) 0: Input Capture Mode disabled 1: Input Capture Mode enabled - Channel 2 is configured as an output (CH2CCS = 0x00) 0: Off –Channel 2 output signal CH2O is not active 1: On –Channel 2 output signal CH2O generated on the corresponding output pin
[2]	CH1E	Channel 1 Capture/Compare Enable - Channel 1 is configured as an input (CH1CCS = 0x01/0x02/0x03) 0: Input Capture Mode disabled 1: Input Capture Mode enabled - Channel 1 is configured as an output (CH1CCS = 0x00) 0: Off –Channel 1 output signal CH1O is not active 1: On –Channel 1 output signal CH1O generated on the corresponding output pin
[0]	CH0E	Channel 0 Capture/Compare Enable - Channel 0 is configured as an input (CH0CCS = 0x01/0x02/0x03) 0: Input Capture Mode disabled 1: Input Capture Mode enabled - Channel 0 is configured as an output (CH0CCS = 0x00) 0: Off –Channel 0 output signal CH0O is not active 1: On –Channel 0 output signal CH0O generated on the corresponding output pin

Channel Polarity Configuration Register – CHPOLR

This register contains the channel capture input or compare output polarity control.

Offset: 0x054

Reset value: 0x0000_0000



Bits	Field	Descriptions
[6]	CH3P	Channel 3 Capture/Compare Polarity - When Channel 3 is configured as an input 0: capture event occurs on a Channel 3 rising edge 1: capture event occurs on a Channel 3 falling edge - When Channel 3 is configured as an output (CH3CCS = 0x00) 0: Channel 3 Output active high 1: Channel 3 Output active low
[4]	CH2P	Channel 2 Capture/Compare Polarity - When Channel 2 is configured as an input 0: capture event occurs on a Channel 2 rising edge 1: capture event occurs on a Channel 2 falling edge - When Channel 2 is configured as an output (CH2CCS = 0x00) 0: Channel 2 Output active high 1: Channel 2 Output active low
[2]	CH1P	Channel 1 Capture/Compare Polarity - When Channel 1 is configured as an input 0: capture event occurs on a Channel 1 rising edge 1: capture event occurs on a Channel 1 falling edge - When Channel 1 is configured as an output (CH1CCS = 0x00) 0: Channel 1 Output active high 1: Channel 1 Output active low
[0]	CH0P	Channel 0 Capture/Compare Polarity - When Channel 0 is configured as an input 0: capture event occurs on a Channel 0 rising edge 1: capture event occurs on a Channel 0 falling edge - When Channel 0 is configured as an output (CH0CCS = 0x00) 0: Channel 0 Output active high 1: Channel 0 Output active low

Timer PDMA/Interrupt Control Register – DICTR

This register contains the timer PDMA and interrupt enable control bits.

Offset: 0x074

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Type/Reset	Reserved					TEVDE	Reserved	UEVDE
						RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
Type/Reset	Reserved					CH3CCDE	CH2CCDE	CH1CCDE
						RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
Type/Reset	Reserved					TEVIE	Reserved	UEVIE
						RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
Type/Reset	Reserved					CH3CCIE	CH2CCIE	CH1CCIE
						RW 0	RW 0	RW 0
	CH0CCIE					RW 0	RW 0	RW 0

Bits	Field	Descriptions
[26]	TEVDE	Trigger event PDMA Request Enable 0: Trigger PDMA request disabled 1: Trigger PDMA request enabled
[24]	UEVDE	Update event PDMA Request Enable 0: Update event PDMA request disabled 1: Update event PDMA request enabled
[19]	CH3CCDE	Channel 3 Capture/Compare PDMA Request Enable 0: Channel 3 PDMA request disabled 1: Channel 3 PDMA request enabled
[18]	CH2CCDE	Channel 2 Capture/Compare PDMA Request Enable 0: Channel 2 PDMA request disabled 1: Channel 2 PDMA request enabled
[17]	CH1CCDE	Channel 1 Capture/Compare PDMA Request Enable 0: Channel 1 PDMA request disabled 1: Channel 1 PDMA request enabled
[16]	CH0CCDE	Channel 0 Capture/Compare PDMA Request Enable 0: Channel 0 PDMA request disabled 1: Channel 0 PDMA request enabled
[10]	TEVIE	Trigger event Interrupt Enable 0: Trigger event interrupt disabled 1: Trigger event interrupt enabled

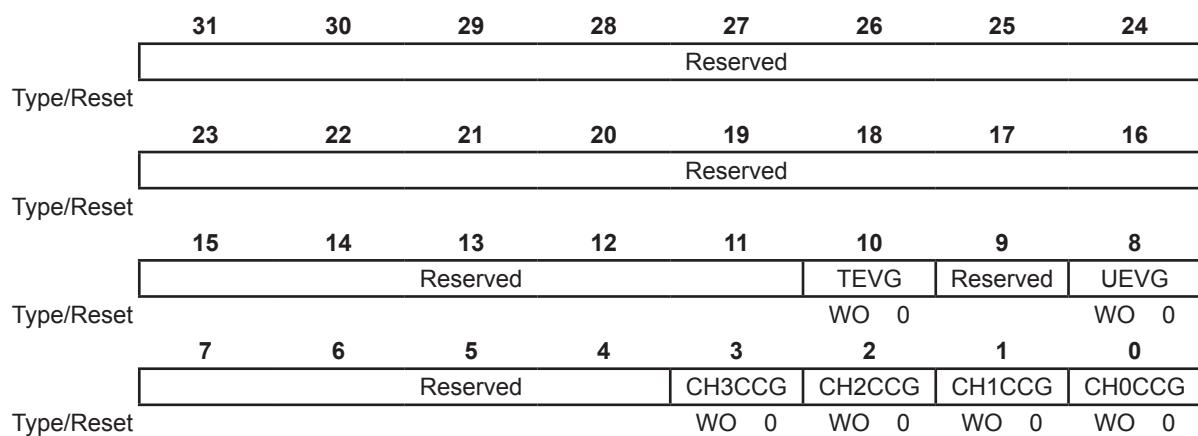
Bits	Field	Descriptions
[8]	UEVIE	Update event Interrupt Enable 0: Update event interrupt disabled 1: Update event interrupt enabled
[3]	CH3CCIE	Channel 3 Capture/Compare Interrupt Enable 0: Channel 3 interrupt disabled 1: Channel 3 interrupt enabled
[2]	CH2CCIE	Channel 2 Capture/Compare Interrupt Enable 0: Channel 2 interrupt disabled 1: Channel 2 interrupt enabled
[1]	CH1CCIE	Channel 1 Capture/Compare Interrupt Enable 0: Channel 1 interrupt disabled 1: Channel 1 interrupt enabled
[0]	CH0CCIE	Channel 0 Capture/Compare Interrupt Enable 0: Channel 0 interrupt disabled 1: Channel 0 interrupt enabled

Timer Event Generator Register – EVGR

This register contains the software event generation bits.

Offset: 0x078

Reset value: 0x0000_0000



Bits	Field	Descriptions
[10]	TEVG	<p>Trigger Event Generation</p> <p>The trigger event TEV can be generated by setting this bit. It is cleared by hardware automatically.</p> <p>0: No action 1: TEVIF flag is set</p>
[8]	UEVG	<p>Update Event Generation</p> <p>The update event UEV can be generated by setting this bit. It is cleared by hardware automatically.</p> <p>0: No action 1: Reinitialize the counter</p> <p>The counter value returns to 0 or the CRR preload value, depending on the counter mode in which the current timer is being used. An update operation of any related registers will also be performed. For more detail descriptions, refer to the corresponding section.</p>

Bits	Field	Descriptions
[3]	CH3CCG	<p>Channel 3 Capture/Compare Generation</p> <p>A Channel 3 capture/compare event can be generated by setting this bit. It is cleared by hardware automatically.</p> <ul style="list-style-type: none"> 0: No action 1: Capture/compare event is generated on channel 3 <p>If Channel 3 is configured as an input, the counter value is captured into the CH3CCR register and then the CH3CCIF bit is set. If Channel 3 is configured as an output, the CH3CCIF bit is set.</p>
[2]	CH2CCG	<p>Channel 2 Capture/Compare Generation</p> <p>A Channel 2 capture/compare event can be generated by setting this bit. It is cleared by hardware automatically.</p> <ul style="list-style-type: none"> 0: No action 1: Capture/compare event is generated on channel 2 <p>If Channel 2 is configured as an input, the counter value is captured into the CH2CCR register and then the CH2CCIF bit is set. If Channel 2 is configured as an output, the CH2CCIF bit is set.</p>
[1]	CH1CCG	<p>Channel 1 Capture/Compare Generation</p> <p>A Channel 1 capture/compare event can be generated by setting this bit. It is cleared by hardware automatically.</p> <ul style="list-style-type: none"> 0: No action 1: Capture/compare event is generated on channel 1 <p>If Channel 1 is configured as an input, the counter value is captured into the CH1CCR register and then the CH1CCIF bit is set. If Channel 1 is configured as an output, the CH1CCIF bit is set.</p>
[0]	CH0CCG	<p>Channel 0 Capture/Compare Generation</p> <p>A Channel 0 capture/compare event can be generated by setting this bit. It is cleared by hardware automatically.</p> <ul style="list-style-type: none"> 0: No action 1: Capture/compare event is generated on channel 0 <p>If Channel 0 is configured as an input, the counter value is captured into the CH0CCR register and then the CH0CCIF bit is set. If Channel 0 is configured as an output, the CH0CCIF bit is set.</p>

Timer Interrupt Status Register – INTSR

This register stores the timer interrupt status.

Offset: 0x07C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24	
	Reserved								
Type/Reset									
	23	22	21	20	19	18	17	16	
	Reserved								
Type/Reset									
	15	14	13	12	11	10	9	8	
	Reserved						TEVIF	Reserved	
Type/Reset							RW 0	RW 0	
	7	6	5	4	3	2	1	0	
Type/Reset	CH3OCF	CH2OCF	CH1OCF	CH0OCF	CH3CCIF	CH2CCIF	CH1CCIF	CH0CCIF	
	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	

Bits	Field	Descriptions
[10]	TEVIF	Trigger Event Interrupt Flag This flag is set by hardware on a trigger event and is cleared by software. 0: No trigger event occurs 1: Trigger event occurs
[8]	UEVIF	Update Event Interrupt Flag. This bit is set by hardware on an update event and is cleared by software. 0: No update event occurs 1: Update event occurs Note: The update event is derived from the following conditions: - The counter overflows or underflows - The UEVG bit is asserted - A restart trigger event occurs from the slave trigger input
[7]	CH3OCF	Channel 3 Over-Capture Flag This flag is set by hardware and cleared by software. 0: No over-capture event is detected 1: Capture event occurs again when the CH3CCIF bit is already set and it is not yet cleared by software
[6]	CH2OCF	Channel 2 Over-Capture Flag This flag is set by hardware and cleared by software. 0: No over-capture event is detected 1: Capture event occurs again when the CH2CCIF bit is already set and it is not cleared yet by software
[5]	CH1OCF	Channel 1 Over-Capture Flag This flag is set by hardware and cleared by software. 0: No over-capture event is detected 1: Capture event occurs again when the CH1CCIF bit is already set and it is not cleared yet by software.

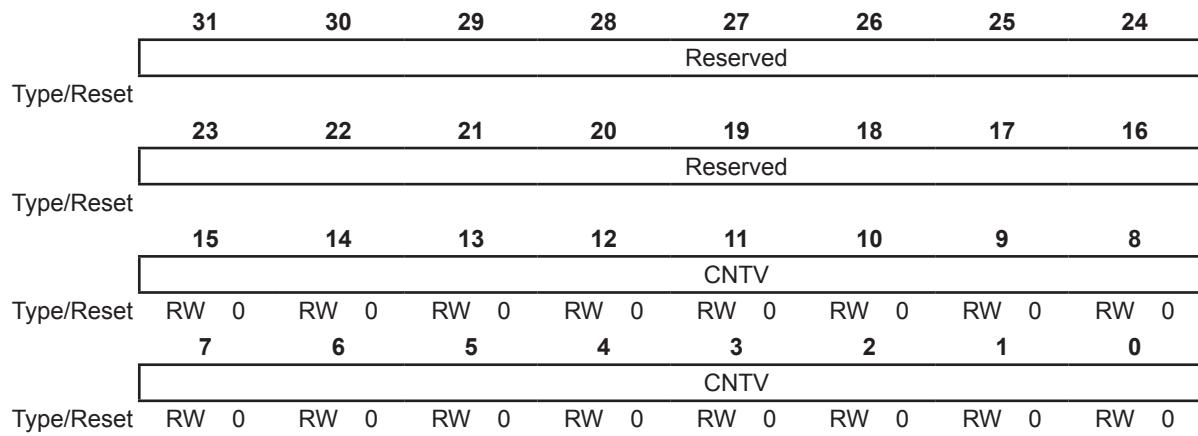
Bits	Field	Descriptions
[4]	CH0OCF	<p>Channel 0 Over-Capture Flag</p> <p>This flag is set by hardware and cleared by software.</p> <ul style="list-style-type: none"> 0: No over-capture event is detected 1: Capture event occurs again when the CH0CCIFbit is already set and it is not yet cleared by software.
[3]	CH3CCIF	<p>Channel 3 Capture/Compare Interrupt Flag</p> <ul style="list-style-type: none"> - Channel 3 is configured as an output: <ul style="list-style-type: none"> 0: No match event occurs 1: The contents of the counter CNTR have matched the contents of the CH3CCR register. <p>This flag is set by hardware when the counter value matches the CH3CCR value except in the center-aligned mode. It is cleared by software.</p> - Channel 3 is configured as an input: <ul style="list-style-type: none"> 0: No input capture occurs 1: Input capture occurs <p>This bit is set by hardware on a capture event. It is cleared by software or by reading the CH3CCR register.</p>
[2]	CH2CCIF	<p>Channel 2 Capture/Compare Interrupt Flag</p> <ul style="list-style-type: none"> - Channel 2 is configured as an output: <ul style="list-style-type: none"> 0: No match event occurs 1: The contents of the counter CNTR have matched the contents of the CH2CCR register <p>This flag is set by hardware when the counter value matches the CH2CCR value except in the center-aligned mode. It is cleared by software.</p> - Channel 2 is configured as an input: <ul style="list-style-type: none"> 0: No input capture occurs 1: Input capture occurs. <p>This bit is set by hardware on a capture event. It is cleared by software or by reading the CH2CCR register.</p>
[1]	CH1CCIF	<p>Channel 1 Capture/Compare Interrupt Flag</p> <p>Channel 1 is configured as an output:</p> <ul style="list-style-type: none"> 0: No match event occurs 1: The contents of the counter CNTR have matched the contents of the CH1CCR register <p>This flag is set by hardware when the counter value matches the CH1CCR value except in the center-aligned mode. It is cleared by software.</p> <ul style="list-style-type: none"> - Channel 1 is configured as an input: <ul style="list-style-type: none"> 0: No input capture occurs 1: Input capture occurs <p>This bit is set by hardware on a capture event. It is cleared by software or by reading the CH1CCR register.</p>
[0]	CH0CCIF	<p>Channel 0 Capture/Compare Interrupt Flag</p> <ul style="list-style-type: none"> - Channel 0 is configured as an output: <ul style="list-style-type: none"> 0: No match event occurs 1: The contents of the counter CNTR have matched the content of the CH0CCR register <p>This flag is set by hardware when the counter value matches the CH0CCR value except in the center-aligned mode. It is cleared by software.</p> - Channel 0 is configured as an input: <ul style="list-style-type: none"> 0: No input capture occurs 1: Input capture occurs <p>This bit is set by hardware on a capture event. It is cleared by software or by reading the CH0CCR register.</p>

Timer Counter Register – CNTR

This register stores the timer counter value.

Offset: 0x080

Reset value: 0x0000_0000



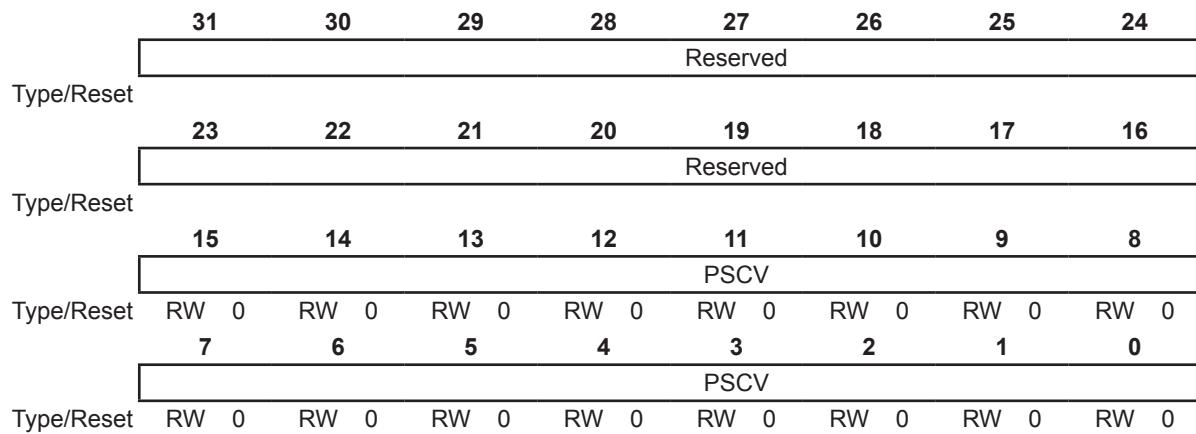
Bits	Field	Descriptions
[15:0]	CNTV	Counter Value.

Timer Prescaler Register – PSCR

This register specifies the timer prescaler value to generate the counter clock.

Offset: 0x084

Reset value: 0x0000_0000



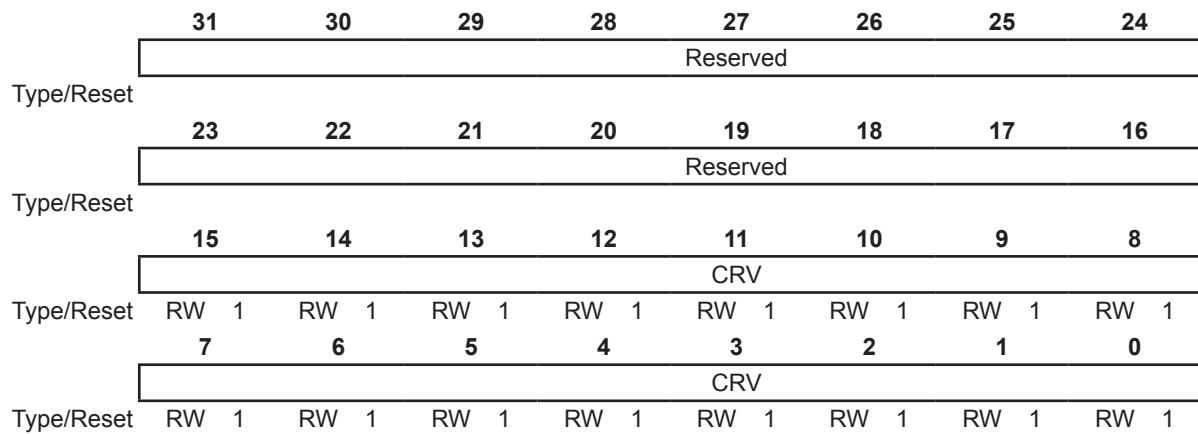
Bits	Field	Descriptions
[15:0]	PSCV	<p>Prescaler Value</p> <p>These bits are used to specify the prescaler value to generate the counter clock frequency f_{CK_CNT}.</p> $f_{CK_CNT} = \frac{f_{CK_PSC}}{PSCV[15:0] + 1}$, where the f_{CK_PSC} is the prescaler clock source.

Timer Counter Reload Register – CRR

This register specifies the timer counter reload value.

Offset: 0x088

Reset value: 0x0000_FFFF



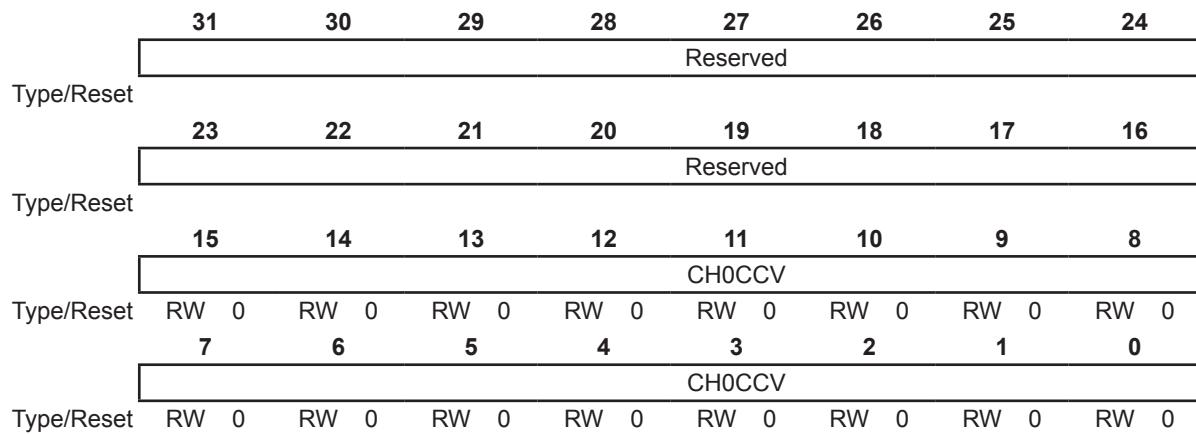
Bits	Field	Descriptions
[15:0]	CRV	Counter Reload Value The CRV is the reload value which is loaded into the actual counter register.

Channel 0 Capture/Compare Register – CH0CCR

This register specifies the timer channel 0 capture/compare value.

Offset: 0x090

Reset value: 0x0000_0000



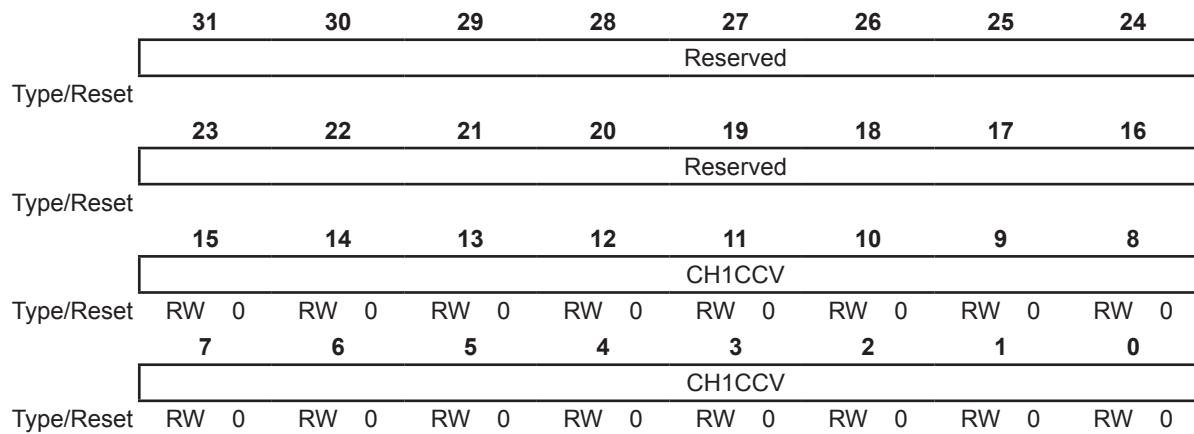
Bits	Field	Descriptions
[15:0]	CH0CCV	<p>Channel 0 Capture/Compare Value</p> <ul style="list-style-type: none"> - When Channel 0 is configured as an output The CH0CCR value is compared with the counter value and the comparison result is used to trigger the CH0OREF output signal. - When Channel 0 is configured as an input The CH0CCR register stores the counter value captured by the last channel 0 capture event.

Channel 1 Capture/Compare Register – CH1CCR

This register specifies the timer channel 1 capture/compare value.

Offset: 0x094

Reset value: 0x0000_0000



Bits	Field	Descriptions
[15:0]	CH1CCV	<p>Channel 1 Capture/Compare Value</p> <ul style="list-style-type: none"> - When Channel 1 is configured as an output The CH1CCR value is compared with the counter value and the comparison result is used to trigger the CH1OREF output signal. - When Channel 1 is configured as an input The CH1CCR register stores the counter value captured by the last channel 1 capture event.

Channel 2 Capture/Compare Register – CH2CCR

This register specifies the timer channel 2 capture/compare value.

Offset: 0x098

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Type/Reset	Reserved							
	23	22	21	20	19	18	17	16
Type/Reset	Reserved							
	15	14	13	12	11	10	9	8
Type/Reset	CH2CCV							
	RW	0	RW	0	RW	0	RW	0
Type/Reset	7	6	5	4	3	2	1	0
	CH2CCV							
Type/Reset	RW	0	RW	0	RW	0	RW	0

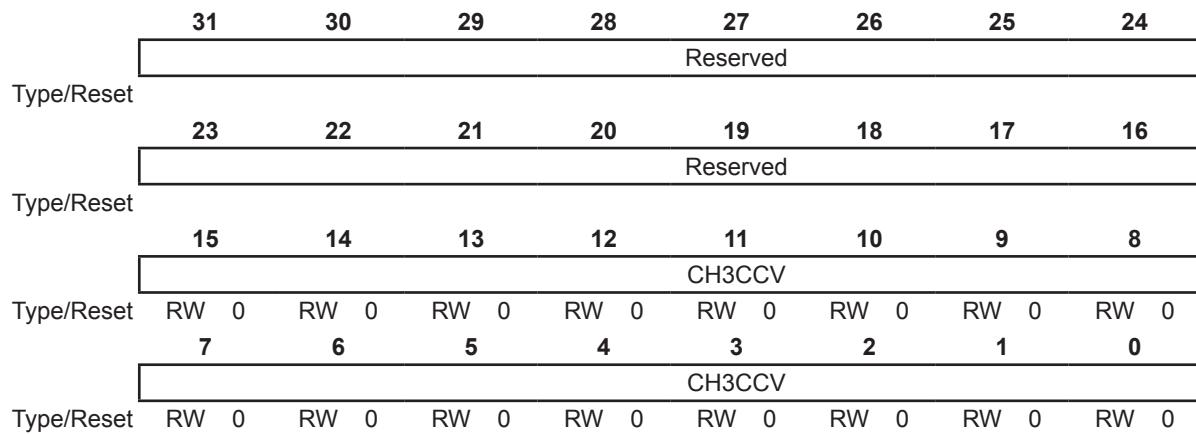
Bits	Field	Descriptions
[15:0]	CH2CCV	<p>Channel 2 Capture/Compare Value</p> <ul style="list-style-type: none"> - When Channel 2 is configured as an output The CH2CCR value is compared with the counter value and the comparison result is used to trigger the CH2OREF output signal. - When Channel 2 is configured as an input The CH2CCR register stores the counter value captured by the last channel 2 capture event.

Channel 3 Capture/Compare Register – CH3CCR

This register specifies the timer channel 3 capture/compare value.

Offset: 0x09C

Reset value: 0x0000_0000



Bits	Field	Descriptions
[15:0]	CH3CCV	<p>Channel 3 Capture/Compare Value</p> <ul style="list-style-type: none"> - When Channel 3 is configured as an output The CH3CCR value is compared with the counter value and the comparison result is used to trigger the CH3OREF output signal. - When Channel 3 is configured as an input The CH3CCR register stores the counter value captured by the last channel 3 capture event.

Channel 0 Asymmetric Compare Register – CH0ACR

This register specifies the timer channel 0 asymmetric compare value.

Offset: 0x0A0

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Reserved								
Type/Reset	23	22	21	20	19	18	17	16
Reserved								
Type/Reset	15	14	13	12	11	10	9	8
CH0ACV								
Type/Reset	RW	0	RW	0	RW	0	RW	0
	7	6	5	4	3	2	1	0
CH0ACV								
Type/Reset	RW	0	RW	0	RW	0	RW	0

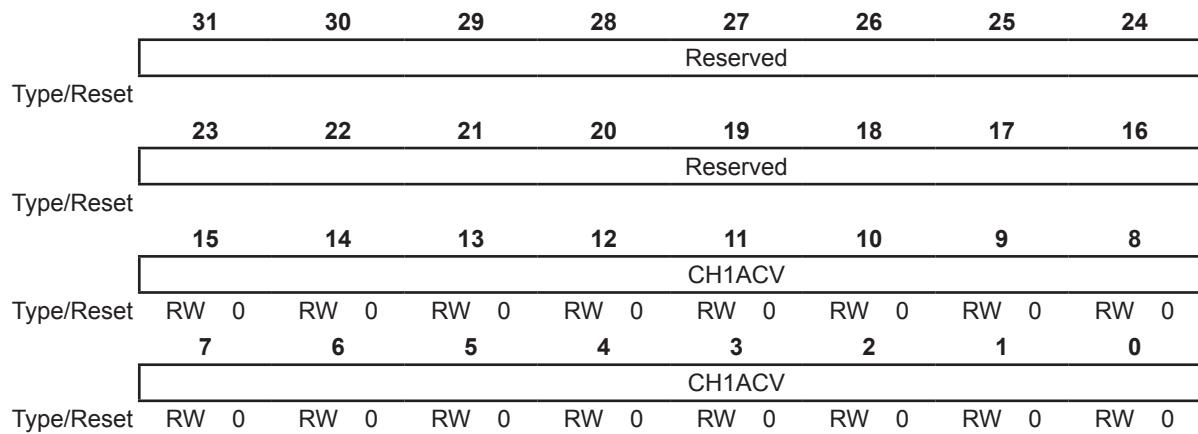
Bits	Field	Descriptions
[15:0]	CH0ACV	Channel 0 Asymmetric Compare Value When channel 0 is configured as asymmetric PWM mode and the counter is counting down, the value written is this register will be compared to the counter.

Channel 1 Asymmetric Compare Register – CH1ACR

This register specifies the timer channel 1 asymmetric compare value.

Offset: 0x0A4

Reset value: 0x0000_0000



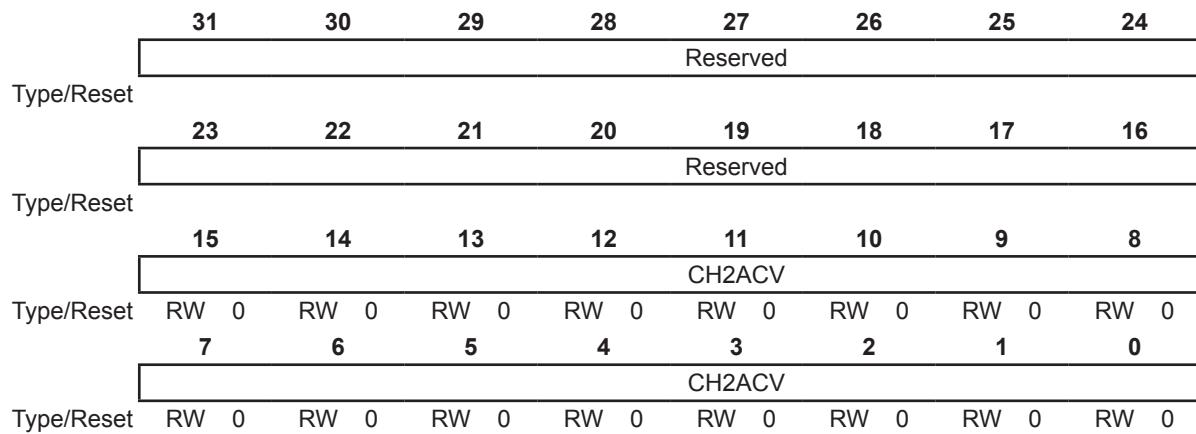
Bits	Field	Descriptions
[15:0]	CH1ACV	Channel 1 Asymmetric Compare Value When channel 1 is configured as asymmetric PWM mode and the counter is counting down, the value written is this register will be compared to the counter.

Channel 2 Asymmetric Compare Register – CH2ACR

This register specifies the timer channel 2 asymmetric compare value.

Offset: 0x0A8

Reset value: 0x0000_0000



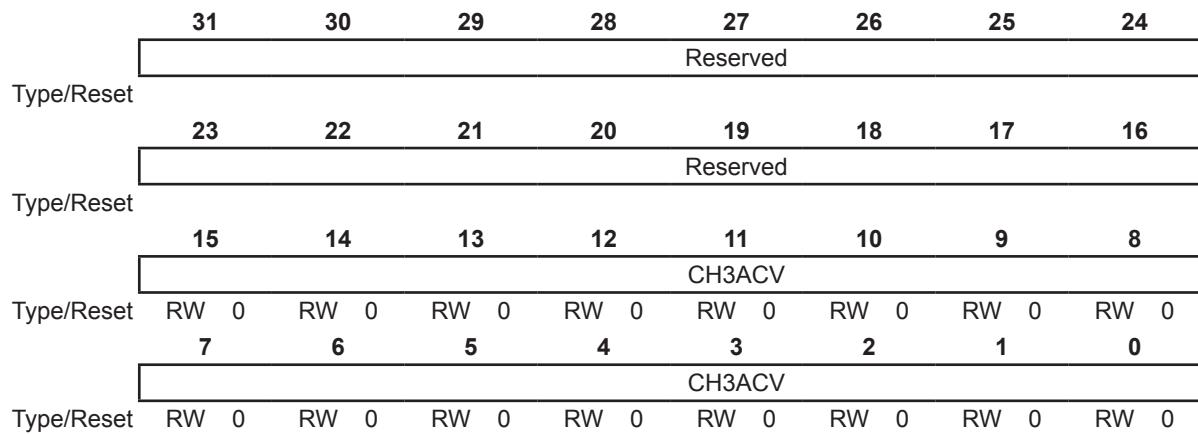
Bits	Field	Descriptions
[15:0]	CH2ACV	Channel 2 Asymmetric Compare Value When channel 2 is configured as asymmetric PWM mode and the counter is counting down, the value written is this register will be compared to the counter.

Channel 3 Asymmetric Compare Register – CH3ACR

This register specifies the timer channel 3 asymmetric compare value.

Offset: 0x0AC

Reset value: 0x0000_0000



Bits	Field	Descriptions
[15:0]	CH3ACV	Channel 3 Asymmetric Compare Value When channel 3 is configured as asymmetric PWM mode and the counter is counting down, the value written is this register will be compared to the counter.

15 Basic Function Timer (BFTM)

Introduction

The Basic Function Timer Module, BFTM, is a 32-bit up-counting counter designed to measure time intervals, generate one shot pulses or generate repetitive interrupts. The BFTM can operate in two modes which are repetitive and one shot modes. The repetitive mode restarts the counter at each compare match event which is generated by the internal comparator. The BFTM also supports a one shot mode which will force the counter to stop counting when a compare match occurs.

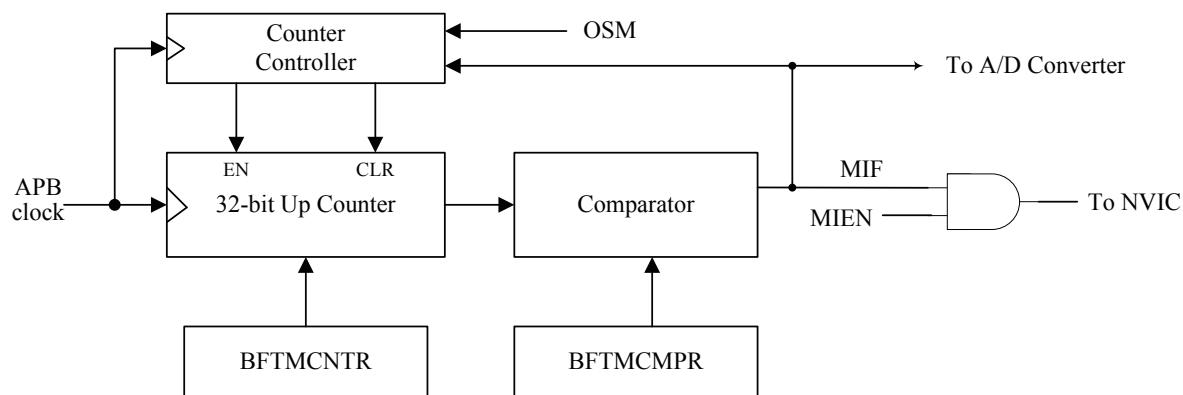


Figure 68. BFTM Block Diagram

Features

- 32-bit up-counting counter
- Compare Match function
- Includes debug mode
- Clock source: APB clock
- Counter value can be R/W on the fly
- One shot mode: counter stops counting when compare match occurs
- Repetitive mode: counter restarts when compare match occurs
- Compare Match interrupt enable/disable control

Functional Descriptions

The BFTM is a 32-bit up-counting counter which is driven by the APB clock, PCLK. The counter value can be changed or read at any time even when the timer is counting. The BFTM supports two operating modes known as the repetitive mode and one shot mode allowing the measurement of time intervals or the generation of periodic time durations.

Repetitive Mode

The BFTM counts up from zero to a specific compare value which is pre-defined by the BFTMnCMPR register. When the BFTM operates in the repetitive mode and the counter reaches a value equal to the specific compare value in the BFTMnCMPR register, the timer will generate a compare match event signal, MIFn. When this occurs, the counter will be reset to 0 and resume its counting operation. When the MIFn signal is generated, a BFTM compare match interrupt will also be generated periodically if the compare match interrupt is enabled by setting the corresponding interrupt control bit, MIENn, to 1. The counter value will remain unchanged and the counter will stop counting if it is disabled by clearing the CENn bit to 0.

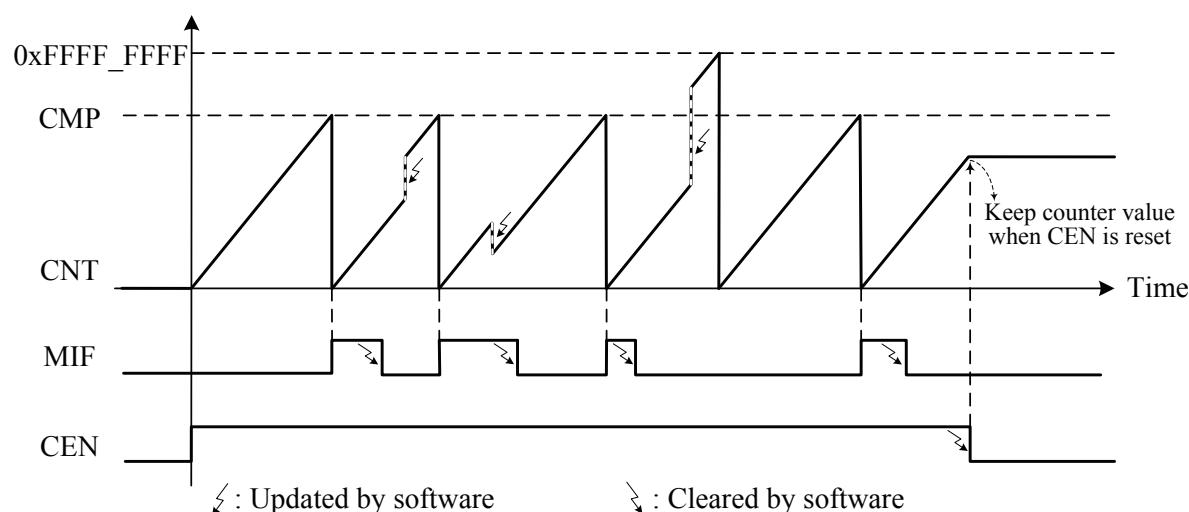


Figure 69. BFTM – Repetitive Mode

One Shot Mode

By setting the OSM_n bit in BFTMnCR register to 1, the BFTM will operate in the one shot mode. The BFTM starts to count when the CEN_n bit is set to 1 by the application program. The counter value will remain unchanged if the CEN_n bit is cleared to 0 by the application program. However, the counter value will be reset to 0 and stop counting when the CEN_n bit is cleared automatically to 0 by the internal hardware when a counter compare match event occurs.

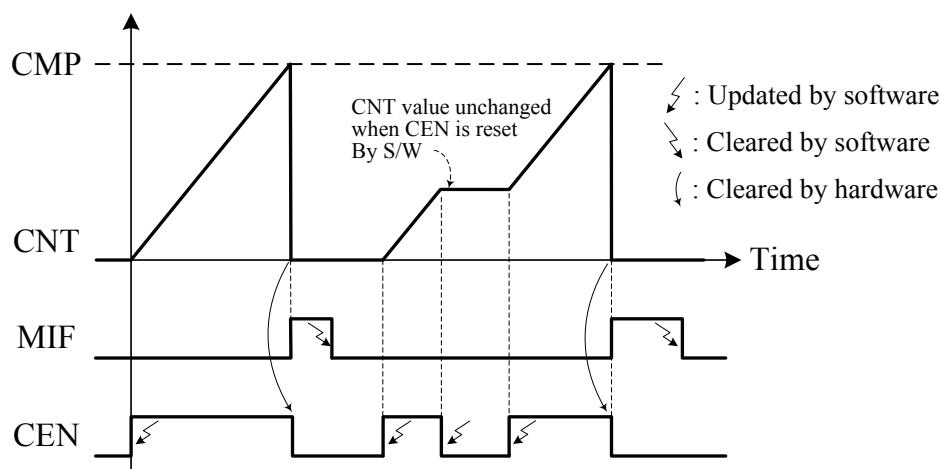


Figure 70. BFTM – One Shot Mode

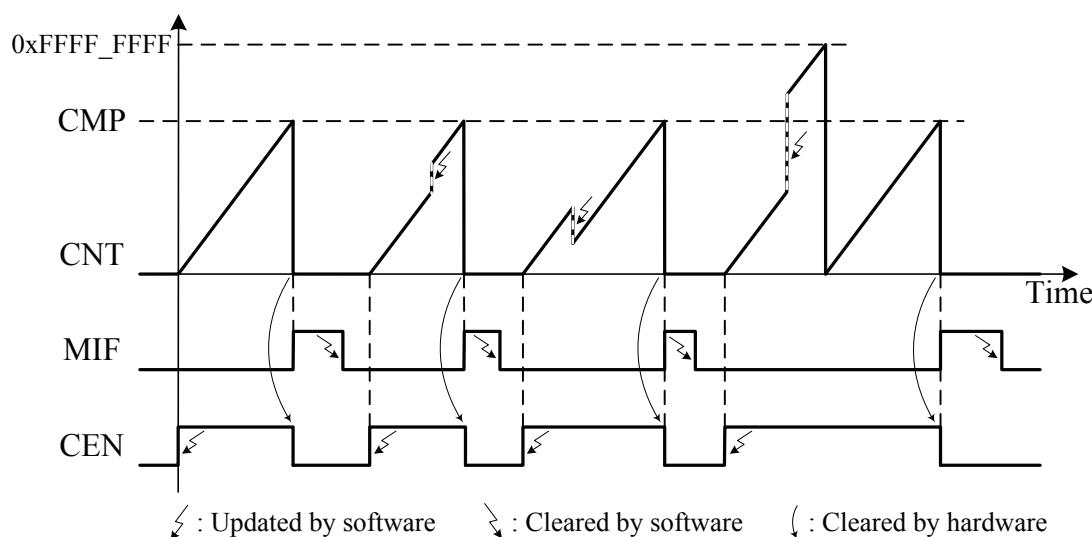


Figure 71. BFTM – One Shot Mode Counter Updating

Trigger ADC Start

When a BFTM compare match event occurs, a compare match interrupt flag, MIF_n, will be generated which can be used as an A/D Converter input trigger source.

Register Map

The following table shows the BFTM registers and their reset values.

Table 34. BFTM Register Map

Register	Offset	Description	Reset Value
BFTM0 Base Address = 0x4007_6000			
BFTM1 Base Address = 0x4007_7000			
BFTMnCR	0x000	BFTMn Control Register	0x0000_0000
BFTMnSR	0x004	BFTMn Status Register	0x0000_0000
BFTMnCNTR	0x008	BFTMn Counter Value Register	0x0000_0000
BFTMnCMPR	0x00C	BFTMn Compare Value Register	0xFFFF_FFFF

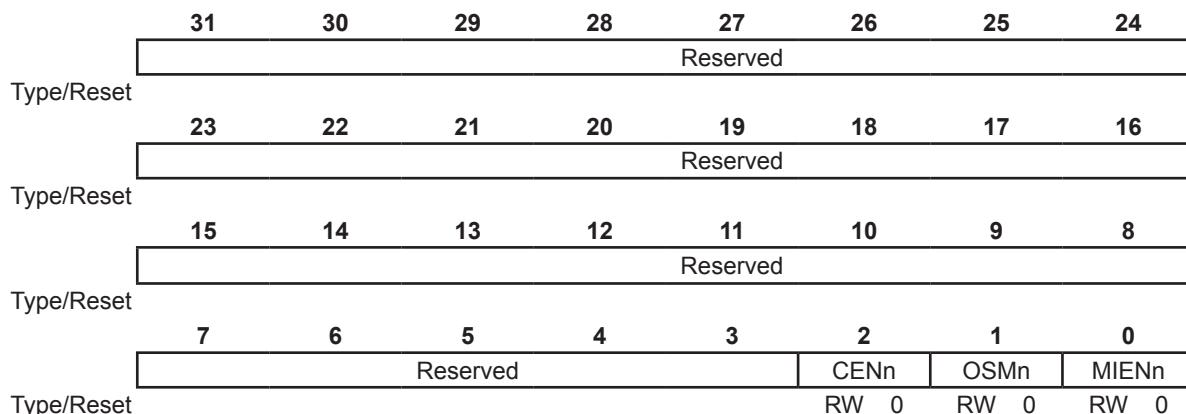
Register Descriptions

BFTMn Control Register – BFTMnCR, n=0~1

This register specifies the overall BFTMn control bits.

Offset: 0x000

Reset value: 0x0000_0000



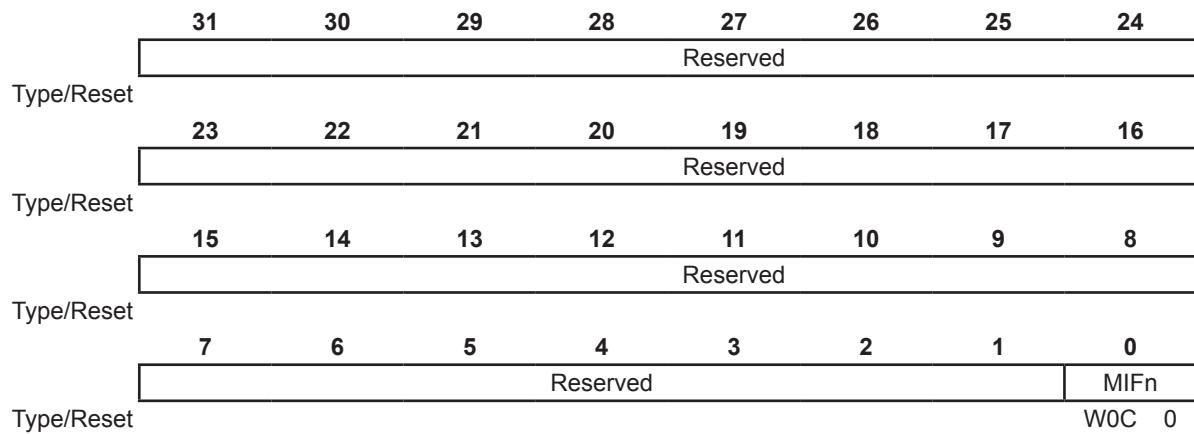
Bits	Field	Descriptions
[2]	CENn	BFTMn Counter Enable Control 0: BFTM is disabled 1: BFTM is enabled When this bit is set to 1, the BFTM counter will start to count. The counter will stop counting and the counter value will remain unchanged when the CENn bit is cleared to 0 by the application program regardless of whether it is in the repetitive or one shot mode. However, in the one shot mode, the counter will stop counting and be reset to 0 when the CENn bit is cleared to 0 by the timer hardware circuitry which results from a compare match event.
[1]	OSMn	BFTMn One Shot Mode Selection 0: Counter operates in repetitive mode 1: Counter operates in one shot mode
[0]	MIENn	BFTM n Compare Match Interrupt Enable Control 0: Compare Match Interrupt is disabled 1: Compare Match Interrupt is enabled

BFTMn Status Register – BFTMnSR, n=0~1

This register specifies the BFTMn status.

Offset: 0x004

Reset value: 0x0000_0004



Bits	Field	Descriptions
[0]	MIFn	<p>BFTMn Compare Match Interrupt Flag</p> <p>0: No compare match event occurs</p> <p>1: Compare match event occurs</p> <p>When the counter value, CNTn, is equal to the compare register value, CMPn, a compare match event will occur and the corresponding interrupt flag, MIFn will be set. The MIFn bit is cleared to 0 by writing a data "0".</p>

BFTMn Counter Register – BFTMnCNTR, n=0~1

This register specifies the BFTMn counter value.

Offset: 0x008

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
CNTn								
Type/Reset	RW 0							
23 22 21 20 19 18 17 16								
CNTn								
Type/Reset	RW 0							
15 14 13 12 11 10 9 8								
CNTn								
Type/Reset	RW 0							
7 6 5 4 3 2 1 0								
CNTn								
Type/Reset	RW 0							

Bits	Field	Descriptions
[31:0]	CNTn	BFTMn Counter Register A 32-bit BFTMn counter value is stored in this field which can be read or written on-the-fly.

BFTMn Compare Value Register – BFTMnCMPR, n=0~1

The register specifies the BFTMn compare value.

Offset: 0x00C

Reset value: 0xFFFF_FFFF

	31	30	29	28	27	26	25	24
CMPn								
Type/Reset	RW 1							
23 22 21 20 19 18 17 16								
CMPn								
Type/Reset	RW 1							
15 14 13 12 11 10 9 8								
CMPn								
Type/Reset	RW 1							
7 6 5 4 3 2 1 0								
CMPn								
Type/Reset	RW 1							

Bits	Field	Descriptions
[31:0]	CMPn	<p>BFTMn Compare Value Register</p> <p>This register specifies a 32-bit BFTMn compare value which is used for comparison with the BFTMn counter value.</p>

16 Motor Control Timer (MCTM)

Introduction

The Motor Control Timer consists of one 16-bit up/down-counter, four 16-bit Capture/Compare Registers (CCRs), one 16-bit Counter-Reload Register (CRR), one 8-bit Repetition Counter (REPR) and several control/status registers. It can be used for a variety of purposes which include general time measurement, input signal pulse width measurement, output waveform generation for signals such as single pulse generation or PWM generation, including dead time insertion. The MCTM supports an encoder interface using a quadrature decoder with two inputs.

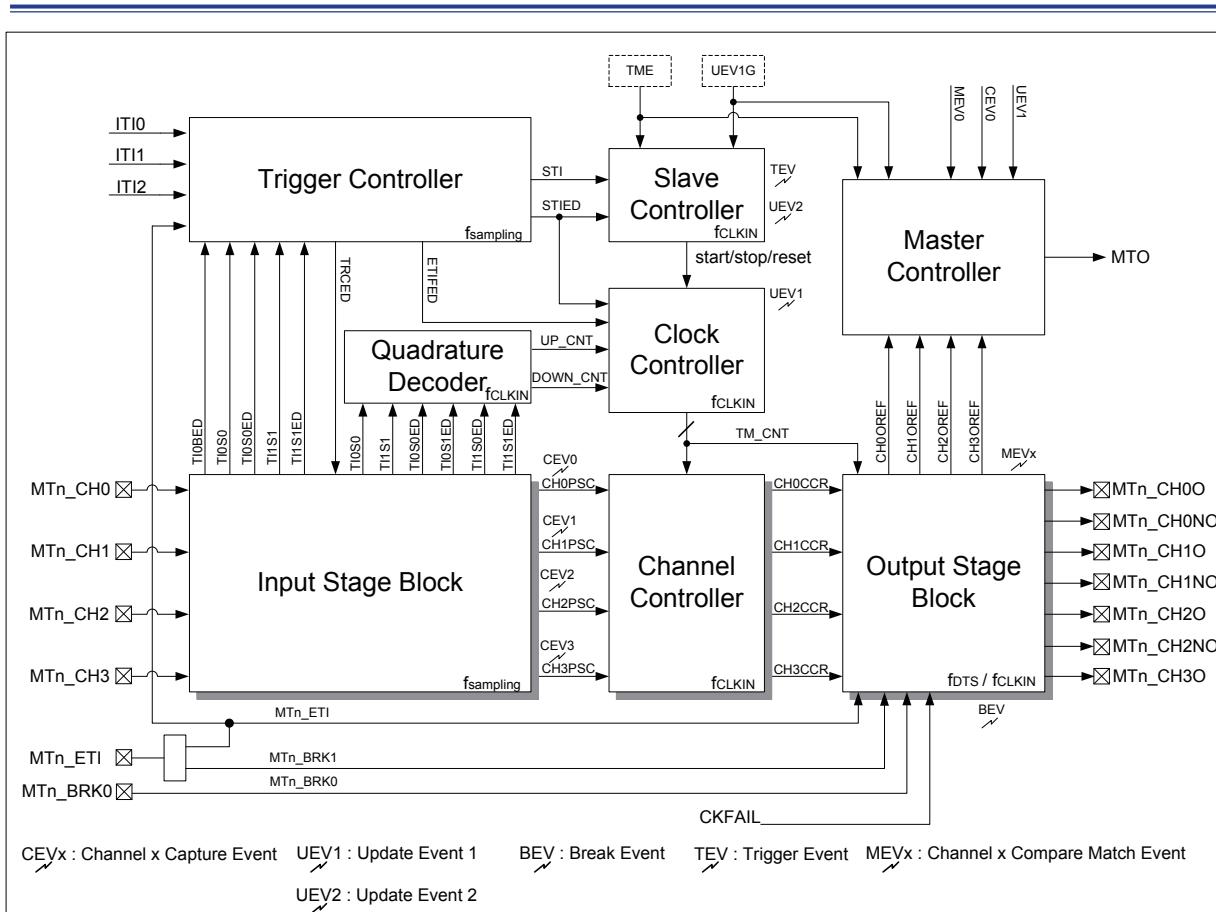


Figure 72. MCTM Block Diagram

Features

- 16-bit up/down auto-reload counter.
- 16-bit programmable prescaler that allows division the counter clock frequency by any factor between 1 and 65536.
- Up to 4 independent channels for:
 - Input Capture function
 - Compare Match Output
 - PWM waveform Generation - Edge and Center-aligned Counting Mode
 - Single Pulse Mode Output
- Complementary Outputs with programmable dead-time insertion
- Encoder interface controller with two inputs using quadrature decoder
- Repetition counter updates timer registers only after a given number of counter cycles.
- Synchronization circuit controls the timer with external signals and can interconnect several timers together.
- Interrupt/PDMA generation on the following events:
 - Update event 1
 - Update event 2
 - Trigger event
 - Input capture event
 - Output compare match
 - Break event - only interrupt
- MCTM Master/Slave mode controller
- Supports 3-phase motor control and hall sensor interface
- Maximum 2 Break input signals to assert the timer output signals in reset state or in a known state

Functional Descriptions

Counter Mode

Up-Counting

In this mode the counter counts continuously from 0 to the counter-reload value, which is defined in the CRR register, in a count-up direction. Once the counter reaches the counter-reload value, the Timer Module generates an overflow event and the counter restarts to count once again from 0. This action will continue repeatedly. The counting direction bit DIR in the CNTCFR register should be set to 0 for the up-counting mode.

When an update event 1 is generated by setting the UEV1G bit in the EVGR register to 1, the counter value will also be initialised to 0.

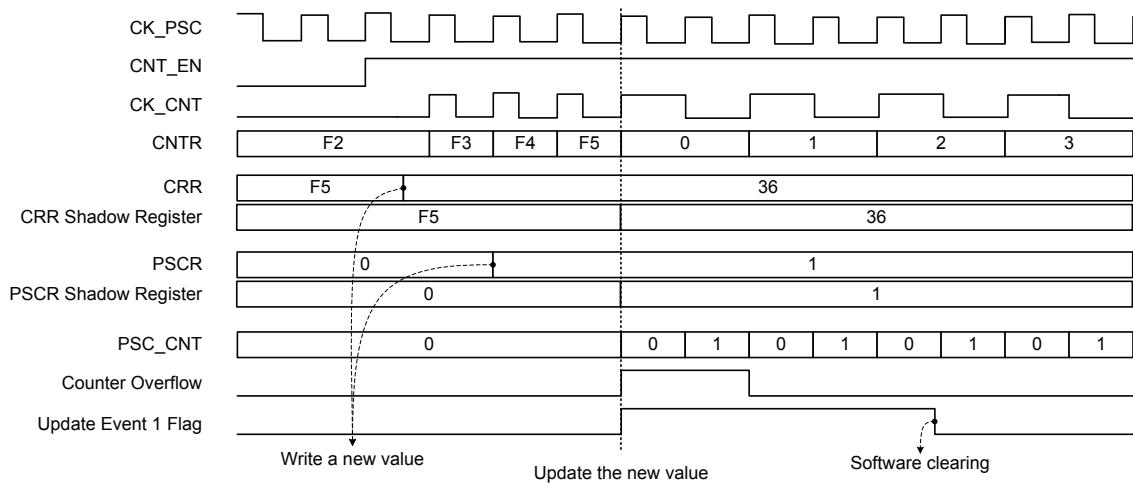


Figure 73. Up-counting Example

Down-Counting

In this mode the counter counts continuously from the counter-reload value, which is defined in the CRR register, to 0 in a count-down direction. Once the counter reaches 0, the Timer module generates an underflow event and the counter restarts to count once again from the counter-reload value. This action will continue repeatedly. The counting direction bit DIR in the CNTCFR register should be set to 1 for the down-counting mode.

When an update event 1 is generated by setting the UEV1G bit in the EVGR register to 1, the counter value will also be initialised to the counter-reload value.

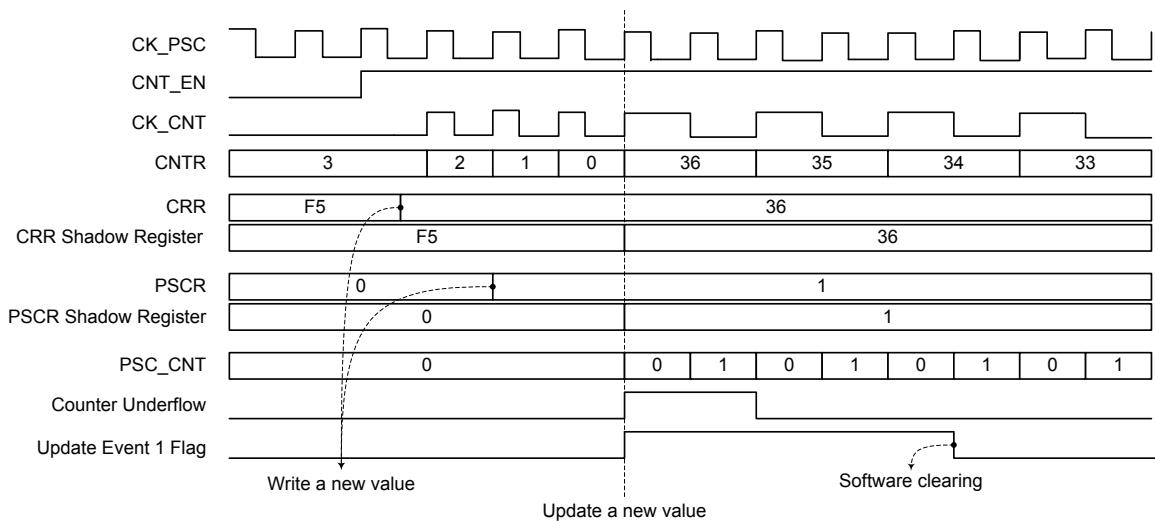


Figure 74. Down-counting Example

Center-aligned Counting

In the center-aligned counting mode, the counter counts up from 0 to the counter-reload value and then counts down to 0 alternatively. The Timer Module generates an overflow event when the counter counts to the counter-reload value in the up-counting mode and generates an underflow event when the counter counts to 0 in the down-counting mode. The counting direction bit DIR in the CNTCFR register is read-only and indicates the count direction when in the center-aligned counting mode. The count direction is updated by hardware automatically.

Setting the UEV1G bit in the EVGR register will initialise the counter value to 0 irrespective of whether the counter is counting up or down in the center-aligned counting mode.

The UEV1IF bit in the INTSR register can be set to 1 according to the CMSEL field setting in the CNTCFR register. When CMSEL=0x01, an underflow event will set the UEV1IF bit to 1. When CMSEL=0x10, an overflow event will set the UEV1IF bit to 1. When CMSEL=0x11, either underflow or overflow event will set the UEV1IF bit to 1.

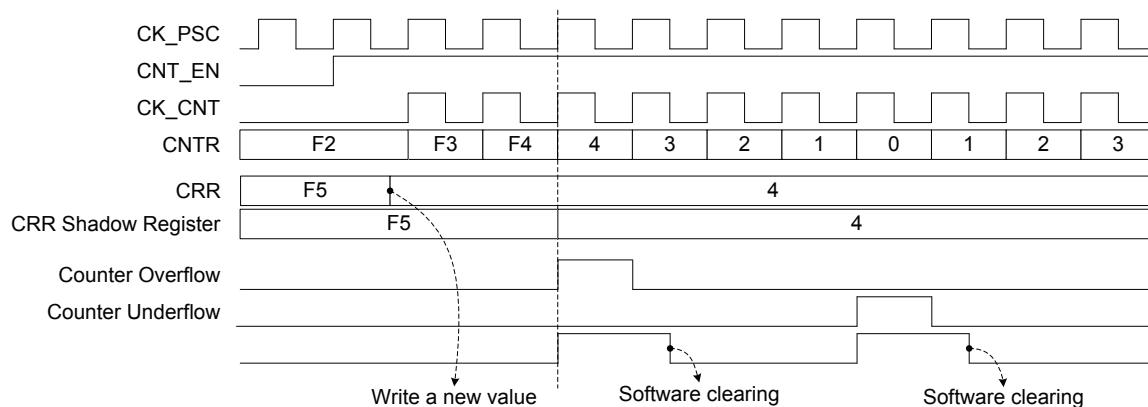


Figure 75. Center-aligned Counting Example

Repetition Down-counter Operation

The update event 1 is usually generated at each overflow or underflow event occurrence. However, when the repetition operation is active by assigning a non-zero value into the REPR register, the update event is only generated if the REPR counter has reached zero. The REPR value is decreased when the following conditions occur:

- At each counter overflow in the up-counting mode
- At each counter underflow in the down-counting mode
- At each counter overflow and at each counter underflow in the center-aligned counting mode

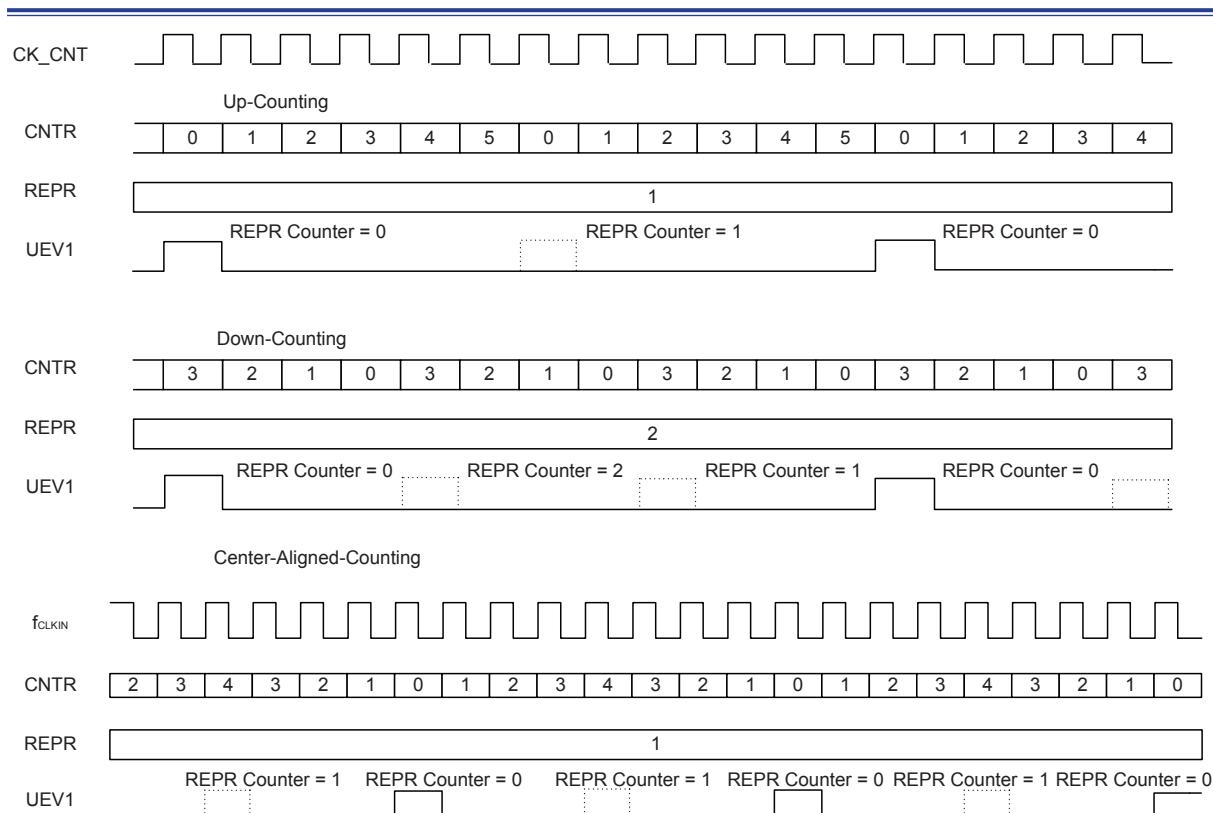


Figure 76. Update Event Dependent Repetition Mechanism Example

Clock Controller

The following describes the Timer Module clock controller which determines the internal prescaler counter clock source.

Internal APB clock f_{CLKIN}

The default internal clock source is the APB clock f_{CLKIN} which is used to drive the counter prescaler when the slave mode is disabled. When the slave mode selection bits SMSEL are set to 0x4, 0x5 or 0x6, the internal APB clock f_{CLKIN} is the counter prescaler driving clock source.

Quadrature Decoder

To select the Quadrature Decoder mode the SMSEL field should be set to 0x1, 0x2 or 0x3 in the MDCFR register. The Quadrature Decoder function uses the two input conditions of the MTn_CH0 and MTn_CH1 pins to generate the clock pulses to drive the counter prescaler. The counting direction bit DIR is modified by hardware automatically at each transition on the input source signal.

STIED

The counter prescaler can count during each rising edge of the STI signal. This mode can be selected by setting the SMSEL field to 0x7 in the MDCFR register. Here the counter will act as an event counter. The input event, known as STI here, can be selected by setting the TRSEL field to an available value except the value of 0x0. When the STI signal is selected as the clock source, the internal edge detection circuitry will generate a clock pulse during each STI signal rising edge to drive the counter prescaler. It is important to note that if the TRSEL field is set to 0x0 to select the software UEV1G bit as the trigger source, then when the SMSEL field is set to 0x7, the counter will be updated instead of counting.

ETIFED

The counter prescaler can be driven to count during each rising edge on ETIF. This mode can be selected by setting the ECME bit in the TRCFR register to 1. The other way to select the ETIF signal as the clock source is to set the SMSEL field to 0x7 and the TRSEL field to 0x3 respectively. When the clock source is selected to come from the ETIF signal, the Trigger Controller including the edge detection circuitry will generate a clock pulse during each ETIF signal rising edge to clock the counter prescaler.

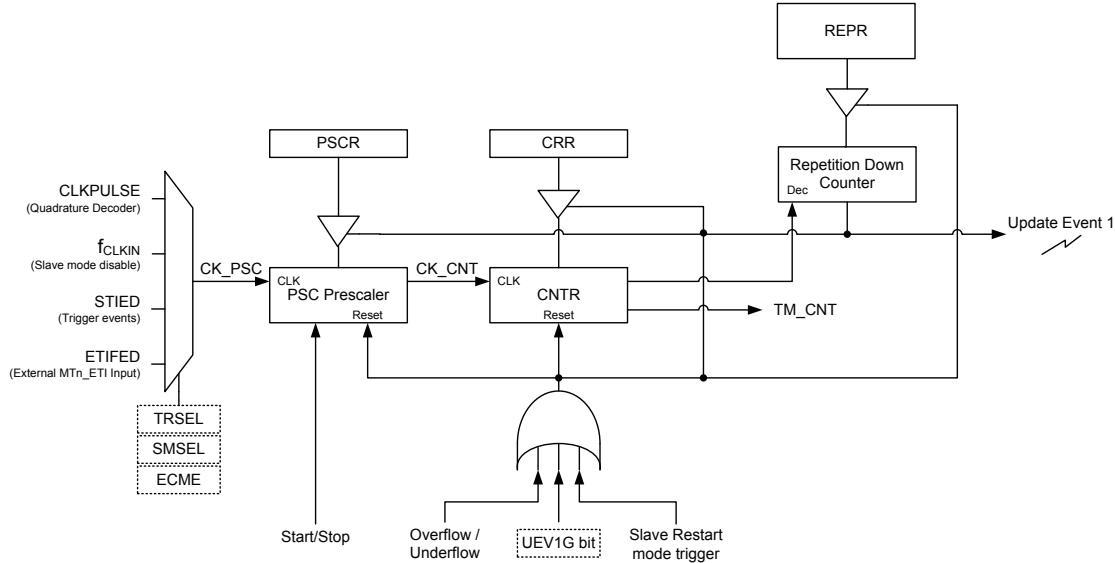
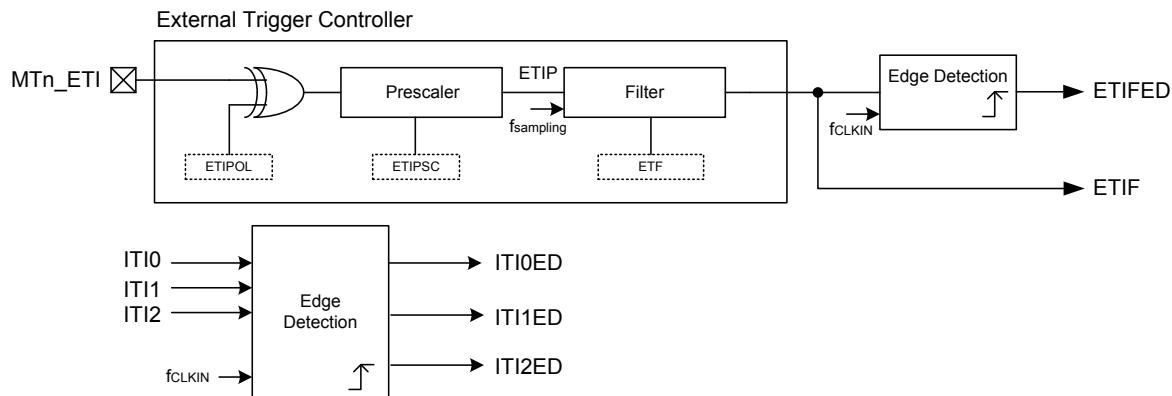


Figure 77. MCTM Clock Selection Source

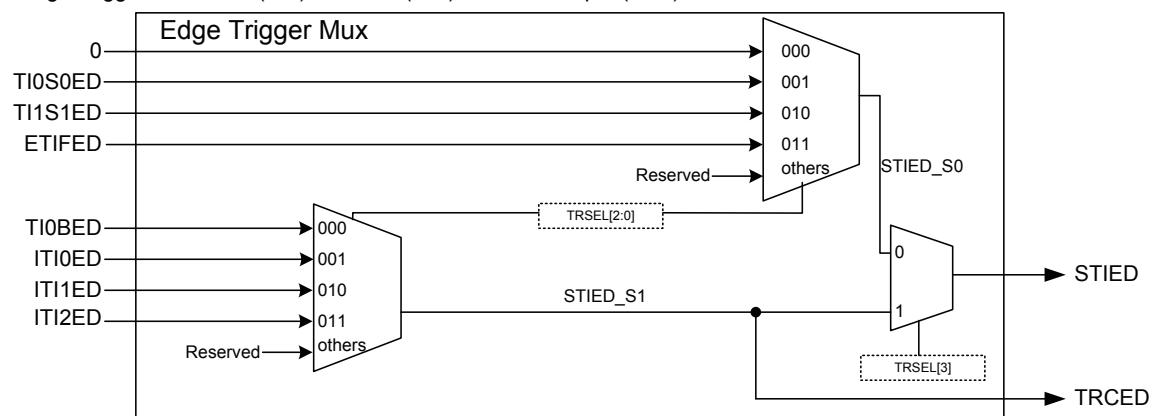
Trigger Controller

The trigger controller is used to select the trigger source and setup the trigger level and edge trigger conditions. The active polarity of the external trigger input signal MT_n_ETI can be configured by the External Trigger Polarity control bit, ETIPOL, in the MCTM Trigger Configuration Register TRCFR. The frequency of the external trigger input can be divided by configuring the related bits, which are the External Trigger Prescaler control bits, ETIPSC, in the TRCFR register. The trigger signal can also be filtered by configuring the External Trigger Filter ETF selection bits in the TRCFR register if a filtered signal is necessary for specific applications. For the internal trigger input, it can be selected by the Trigger Selection bits, TRSEL, in the TRCFR register. For all the trigger sources except the UEV1G bit software trigger, the internal edge detection circuitry will generate a clock pulse at each trigger signal rising edge to activate some MCTM functions which are triggered by a trigger signal rising edge.

Trigger Controller Block = Edge Trigger Mux + Level Trigger Mux



Edge Trigger = External (ETI)+ Internal (ITIx) + Channel input (CHn) + XOR function



Level Trigger Source = External (ETI)+ Internal (ITIx) + Channel input (CHn) + Software UEV1G bit

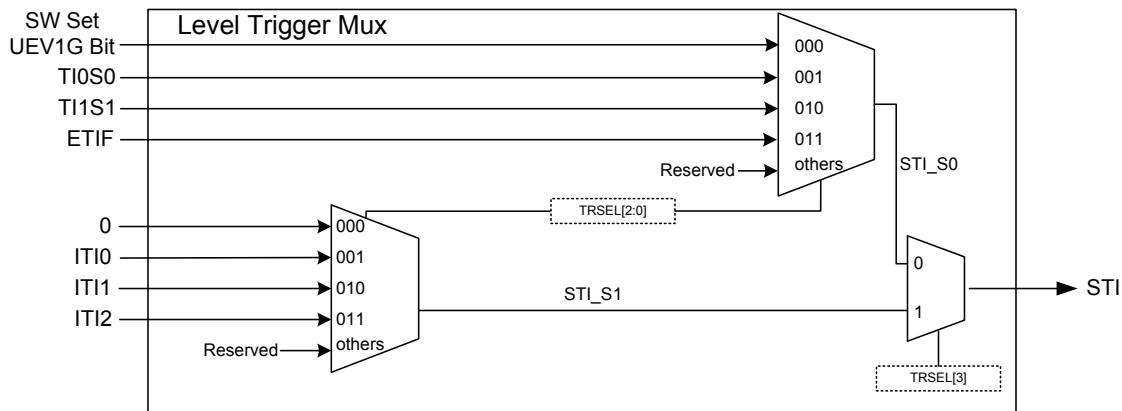


Figure 78. Trigger Control Block

Slave Controller

The MCTM can be synchronised with an internal/external trigger in several modes including the Restart mode, the Pause mode and the Trigger mode which are selected by the SMSEL field in the MDCFR register. The trigger input of these modes comes from the STI signal which is selected by the TRSEL field in the TRCFR register. The operation modes in the Slave Controller are described in the accompanying sections.

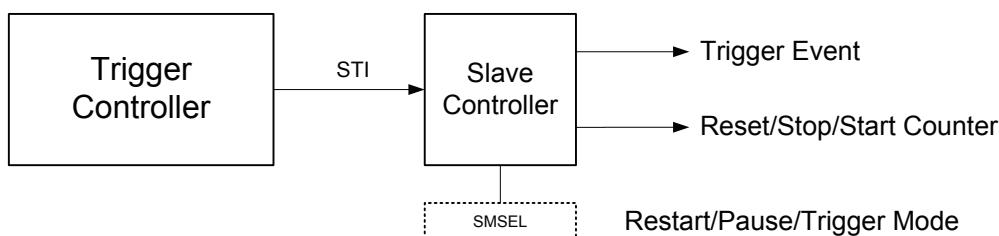


Figure 79. Slave Controller Diagram

Restart Mode

The counter and its prescaler can be reinitialised in response to an STI signal rising edge. If the UEV1DIS bit is set to 1 to disable the update event, then no update event will be generated, however the counter and prescaler are still reinitialised when an STI rising edge occurs. If the UEV1DIS bit in the CNTCFR register is cleared to enable the update event, then an update event will be generated together with the STI rising edge and all the preloaded registers will be updated.

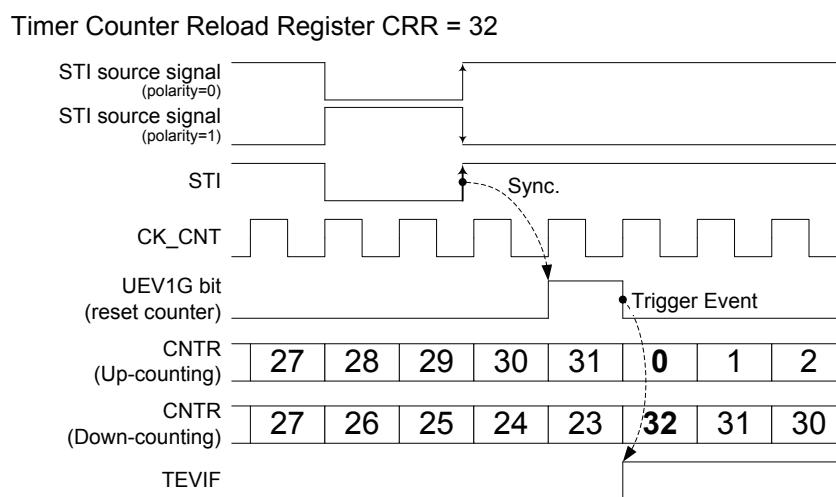


Figure 80. MCTM in Restart Mode

Pause Mode

In the Pause Mode, the selected STI input signal level is used to control the counter start/stop operation. The counter starts to count when the selected STI signal is at a high level and stops counting when the STI signal is changed to a low level. When the counter stops, it will maintain its present value and not be reset. Since the Pause function depends upon the STI level to control the counter stop/start operation, the selected STI trigger signal can not be derived from the TI0BED signal.

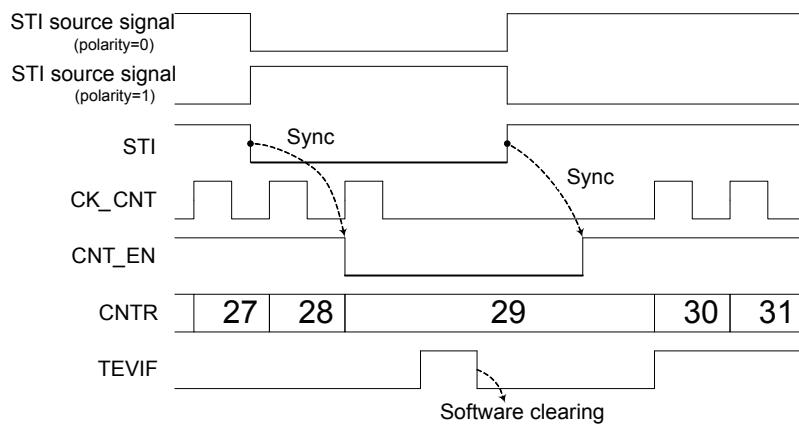


Figure 81. MCTM in Pause Mode

Trigger Mode

After the counter is disabled to count, the counter can resume counting when an STI rising edge signal occurs. When an STI rising edge occurs, the counter will start to count from the current value in the counter. Note that if the STI signal is selected to be sourced from the UEV1G bit software trigger, the counter will not resume counting. When software triggering using the UEV1G bit is selected as the STI source signal, there will be no clock pulse generated which can be used to make the counter resume counting. Note that the STI signal is only used to enable the counter to resume counting and has no effect to stop counting.

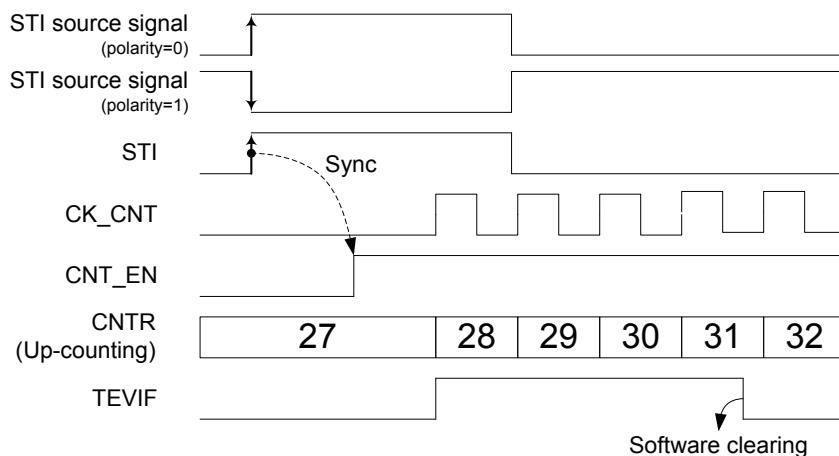


Figure 82. MCTM in Trigger Mode

Master Controller

The MCTMs and GPTMs can be linked together internally for timer synchronisation or chaining. When one MCTM is configured to be in the Master Mode, the MCTM Master Controller will generate a Master Trigger Output (MTO) signal which can reset, start, stop the Slave counter or be a clock source of the Slave Counter. This can be selected by the MMSEL field in the MDCFR register to trigger or drive another MCTM or GPTM which should be configured in the Slave Mode.

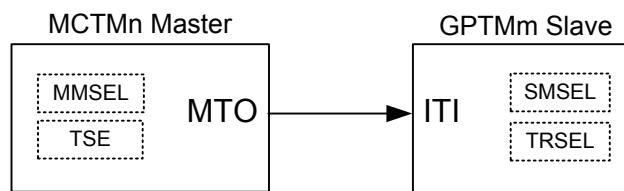


Figure 83. Master MCTMn and Slave GPTM Connection

The Master Mode Selection bits, MMSEL, in the MDCFR register are used to select the MTO source for synchronising another slave MCTM or GPTM.

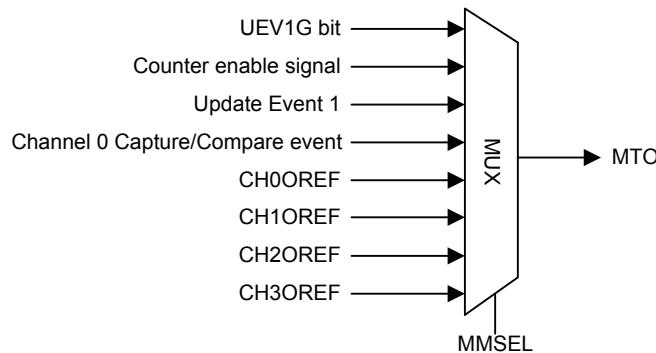


Figure 84. MTO selection

For example, setting the MMSEL field to 0x5 is to select the CH1OREF signal as the MTO signal to synchronise another slave MCTM or GPTM. For a more detailed description, refer to the related MMSEL field definitions in the MDCFR register.

Channel Controller

The MCTM has four independent channels which can be used as capture inputs or compare match outputs. Each capture input or compare match output channel is composed of a preload register and a shadow register. Data access of the APB bus is always implemented through the read/write preload register.

When used in the input capture mode, the counter value is captured into the CH_xCCR shadow register first and then transferred into the CH_xCCR preload register when the capture event occurs.

When used in the compare match output mode, the contents of the CH_xCCR preload register is copied into the associated shadow register, the counter value is then compared with the register value.

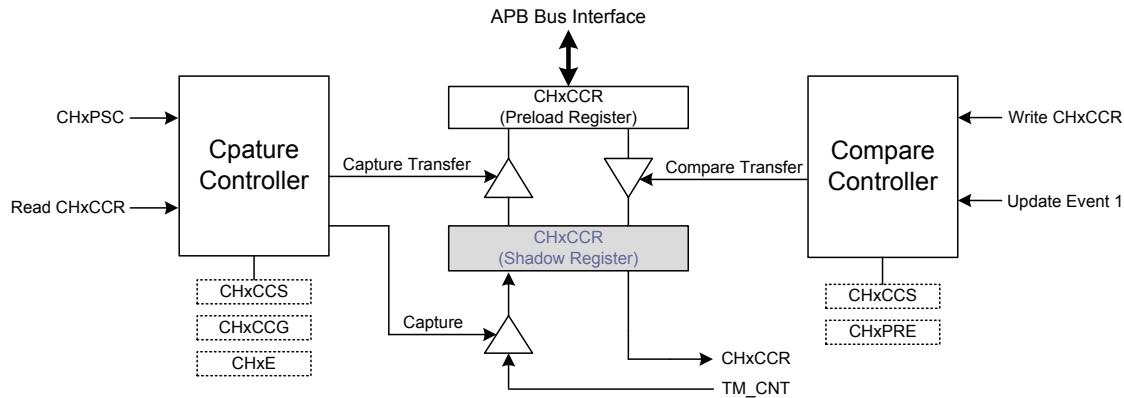


Figure 85. Capture/Compare Block Diagram

Capture Counter Value Transferred to CHxCCR

When the channel is used as a capture input, the counter value is captured into the Channel Capture/Compare Register (CHxCCR) when an effective input signal transition occurs. Once the capture event occurs, the CHxCCIF flag in the INTSR register is set accordingly. If the CHxCCIF bit is already set, i.e., the flag has not yet been cleared by software, and another capture event on this channel occurs, the corresponding channel Over-Capture flag, named CHxOCF, will be set.

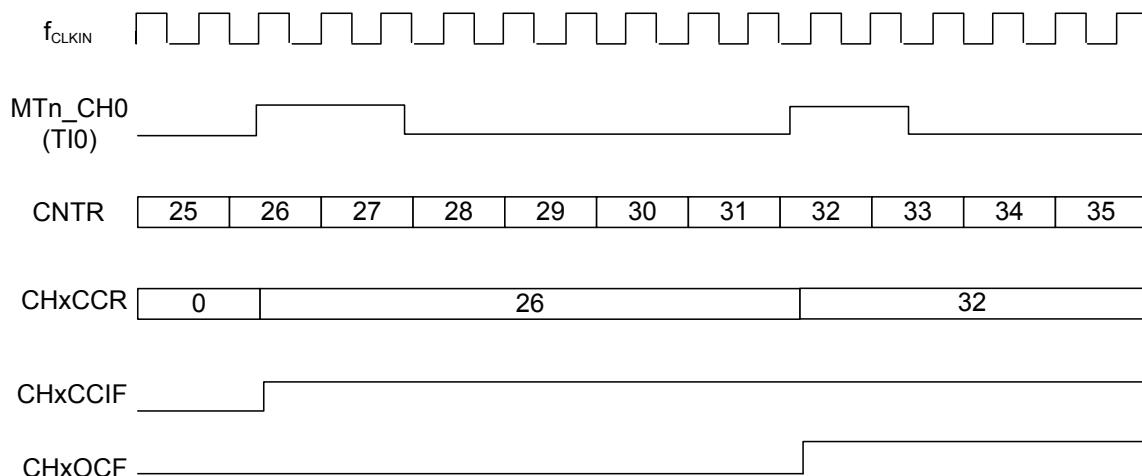


Figure 86. Input Capture Mode

Pulse Width Measurement

The input capture mode can be also used for pulse width measurement from signals on the MTn_CHx pins, TIx. The following example shows how to configure the MCTM when operated in the input capture mode to measure the high pulse width and the input period on the MTn_CH0 pin using channel 0 and channel 1. The basic steps are shown as follows.

- Configure the capture channel 0 (CH0CCS = 0x1) to select the TI0 signal as the capture input.
- Configure the CH0P bit to 0 to choose the rising edge of the TI0 input as the active polarity.
- Configure the capture channel 1 (CH1CCS = 0x2) to select the TI0 signal as the capture input.
- Set the CH1P bit to 1 to choose the falling edge of the TI0 input as the active polarity.
- Setup the TRSEL bits to 0x0001 to select TI0S0 as the trigger input.
- Configure the Slave controller to operate in the Restart mode by setting the SMSEL field in the MDCFR register to 0x4
- Enable the input capture mode by setting the CH0E and CH1E bits in the CHCTR register to 1.

As the following diagram shows, the high pulse width on the MTn_CH0 pin will be captured into the CH1CCR register while the input period will be captured into the CH0CCR register after an input capture operation.

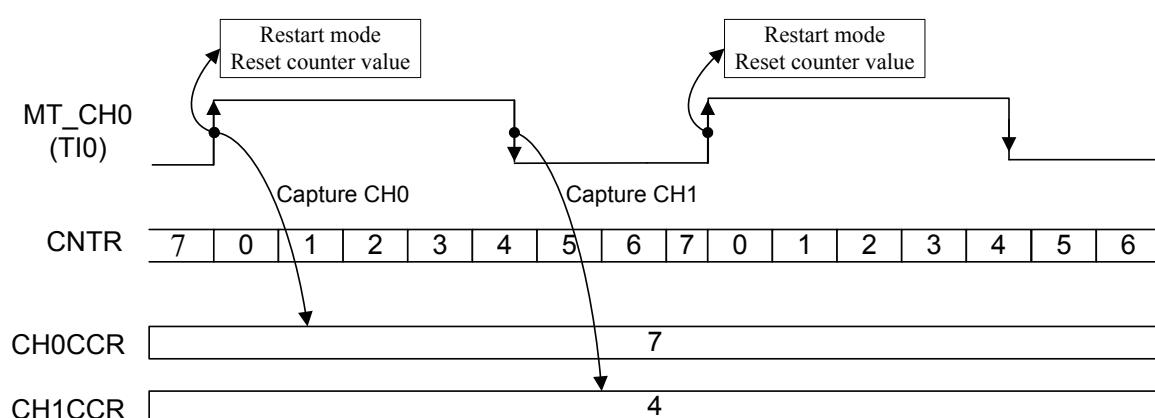


Figure 87. PWM Pulse Width Measurement Example

Input Stage

The input stage consists of a digital filter, a channel polarity selection, edge detection and a channel prescaler. The channel 0 input signal, TI0, can be chosen to come from the MTn_CH0 signal or the Exclusive-OR function of the MTn_CH0, MTn_CH1 and MTn_CH2 signals. The channel input signal, TIx, is sampled by a digital filter to generate a filtered input signal TIxFP. Then the channel polarity and the edge detection block can generate a TIxSxED signal for the input capture function. The effective input event number can be set by the channel input prescaler register CHxPSC.

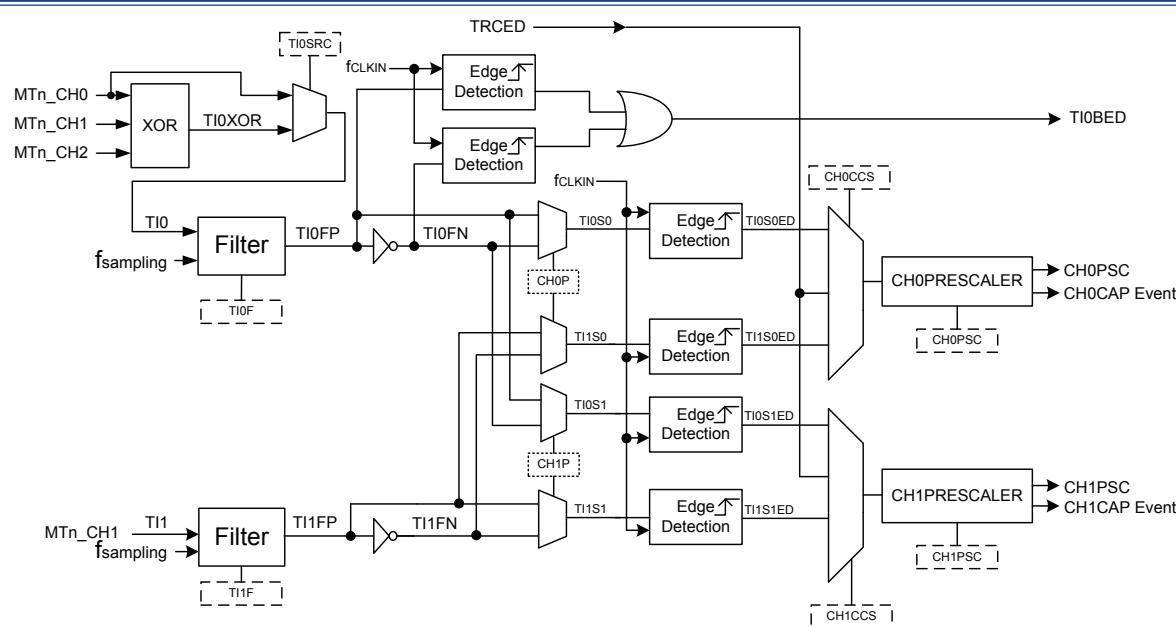


Figure 88. Channel 0 and Channel 1 Input Stage

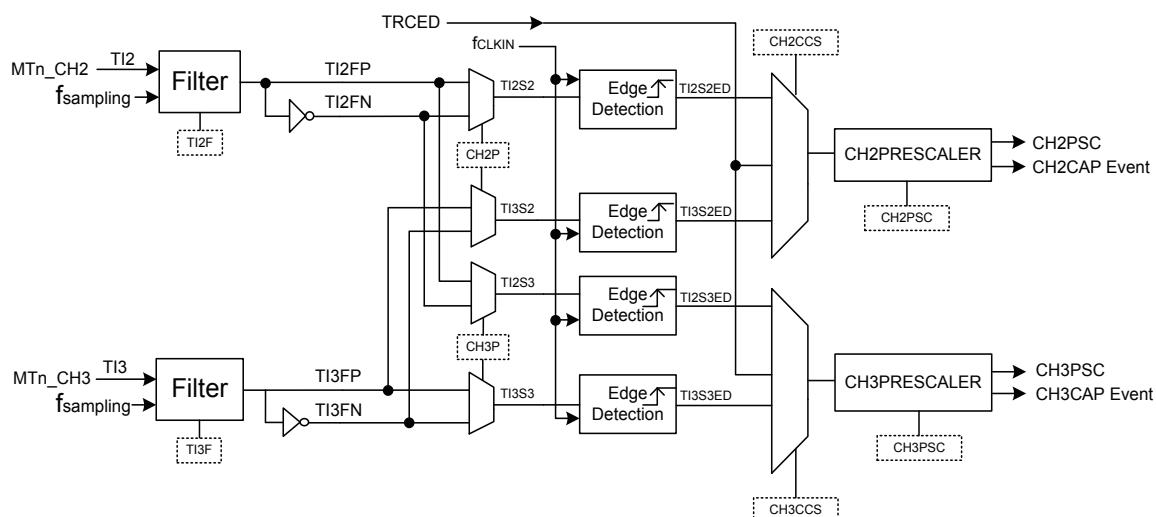


Figure 89. Channel 2 and Channel 3 Input Stage

Output Stage

The MCTM supports complementary outputs for channels 0, 1 and 2 with dead time insertion. The MCTM channel 3 output function is almost the same as that of GPTM channel 3 except for the break function.

The channel outputs, CHxO and CHxNO, are referenced to the CHxOREF signal. These channel outputs generate a wide variety of wide waveforms according to the configuration values of corresponding control bits, as shown by the dashed box in the diagram.

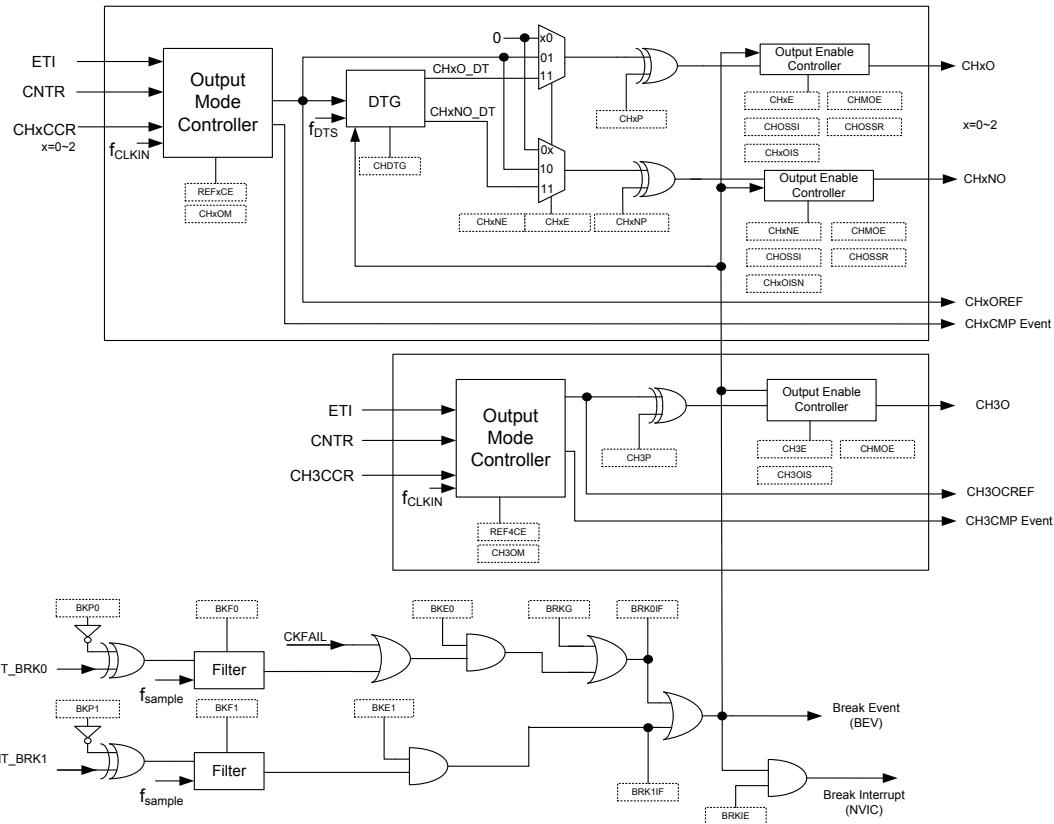


Figure 90. Output Stage Block Diagram

Channel Output Reference Signal

When the MCTM is used in the compare match output mode, the CHxOREF signal (Channel x Output Reference signal) is defined by the CHxOM bit setup. The CHxOREF signal has several types of output function which defines what happens to the output when the counter value matches the contents of the CHxCCR register. In addition to the low, high and toggle CHxOREF output types, there are also PWM mode 1 and PWM mode 2 outputs. In these modes, the CHxOREF signal level is changed according to the count direction and the relationship between the counter value and the CHxCCR content. There are also two modes which will force the output into an inactive or active state irrespective of the CHxCCR content or counter values. With regard to a more detailed description refer to the relative bit definition.

The accompanying table shows a summary of the output type setup.

Table 35. Compare Match Output Setup

CHxOM value	Compare Match Level
0x00	No change
0x01	Clear Output to 0
0x02	Set Output to 1
0x03	Toggle Output
0x04	Force Inactive Level
0x05	Force Active Level
0x06	PWM Mode 1
0x07	PWM Mode 2

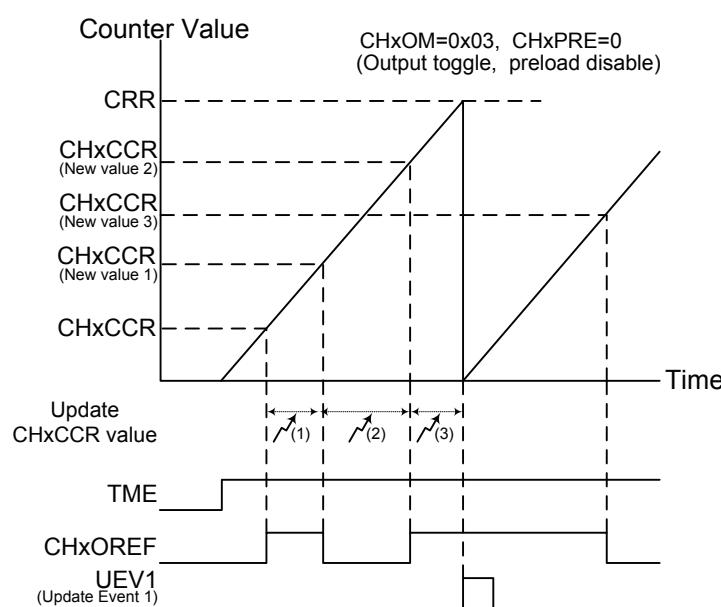


Figure 91. Toggle Mode Channel Output Reference Signal - CHxPRE = 0

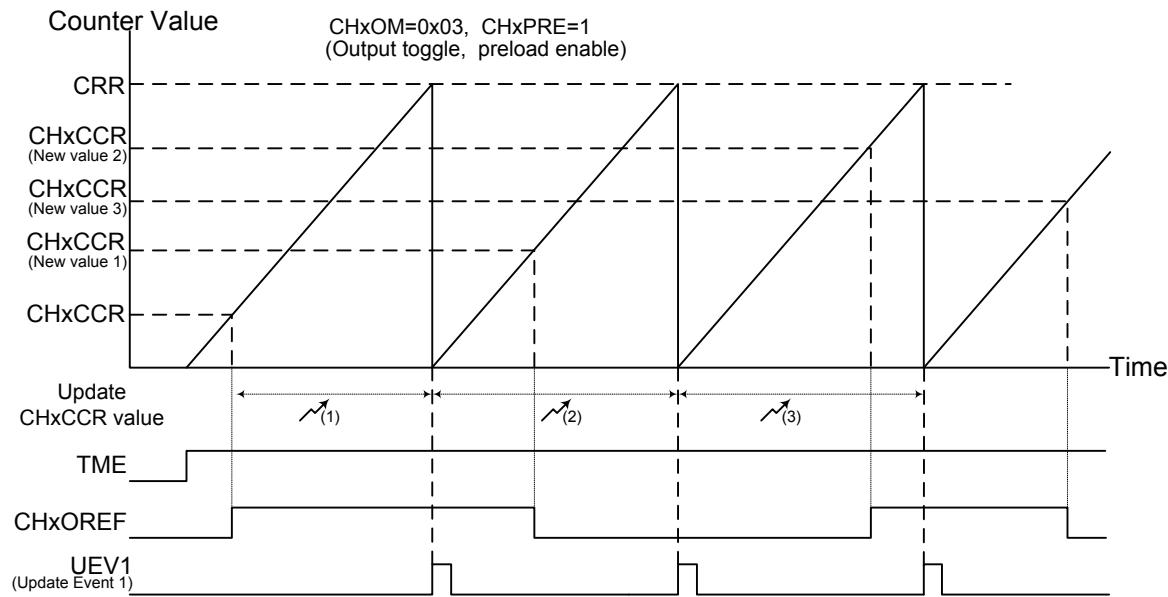


Figure 92. Toggle Mode Channel Output Reference Signal - CHxPRE = 1

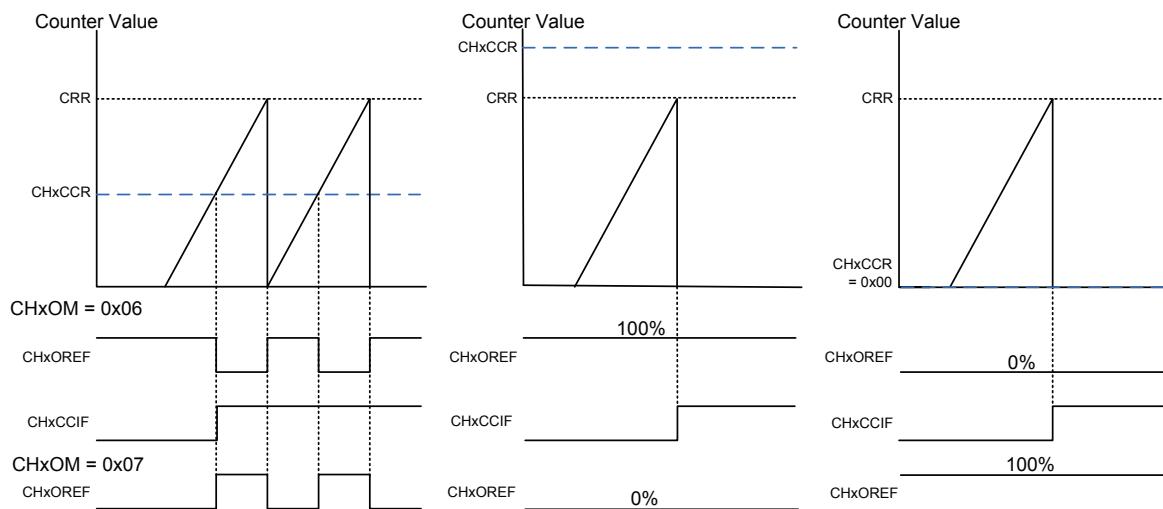


Figure 93. PWM Mode Channel Output Reference Signal and Counter in Up-counting Mode

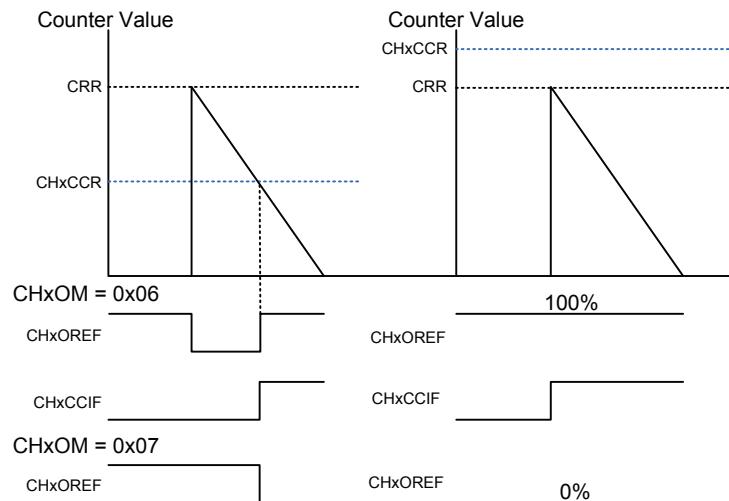


Figure 94. PWM Mode Channel Output Reference Signal and Counter in Down-counting Mode

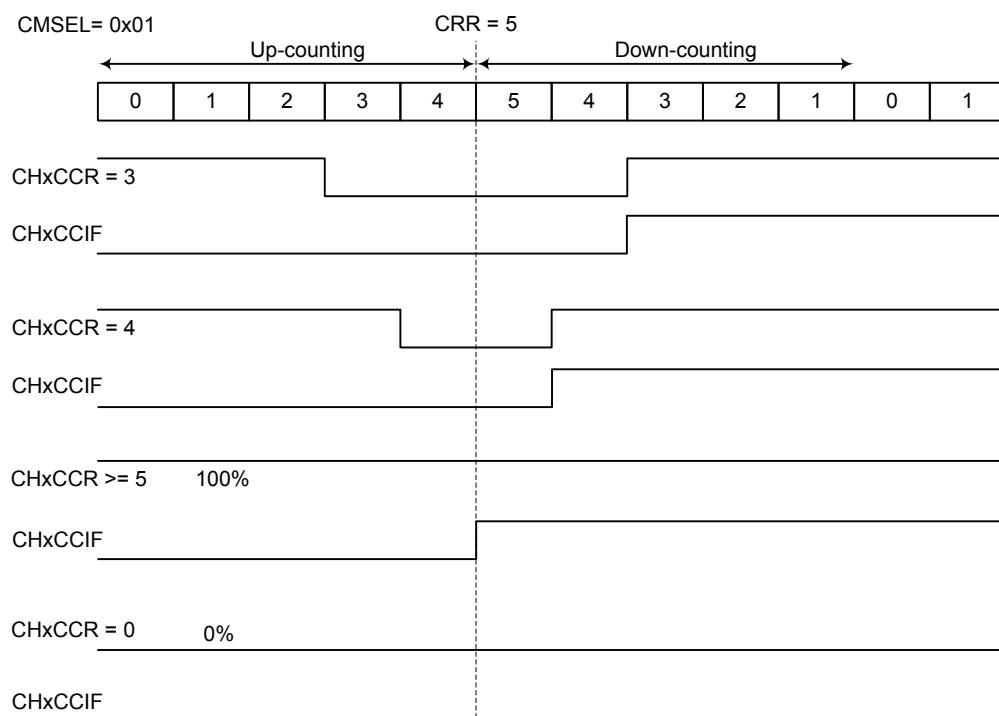


Figure 95. PWM Mode 1 Channel Output Reference Signal and Counter in Centre-aligned Counting Mode

Dead Time Generator

An 8-bit dead time generator function is included for channels 0~2. The dead time insertion is enabled by setting both the CHxE and CHxNE bits. The relationship between the CHxO and CHxNO signals with respect to the CHxOREF signal is as follows:

- The CHxO signal is the same as the CHxOREF signal except for the rising edge which is delayed with a dead time relative to the reference signal rising edge.
- The CHxNO is the opposite of the CHxOREF signal except for the rising edge which is delayed with a dead time relative to the reference signal falling edge.

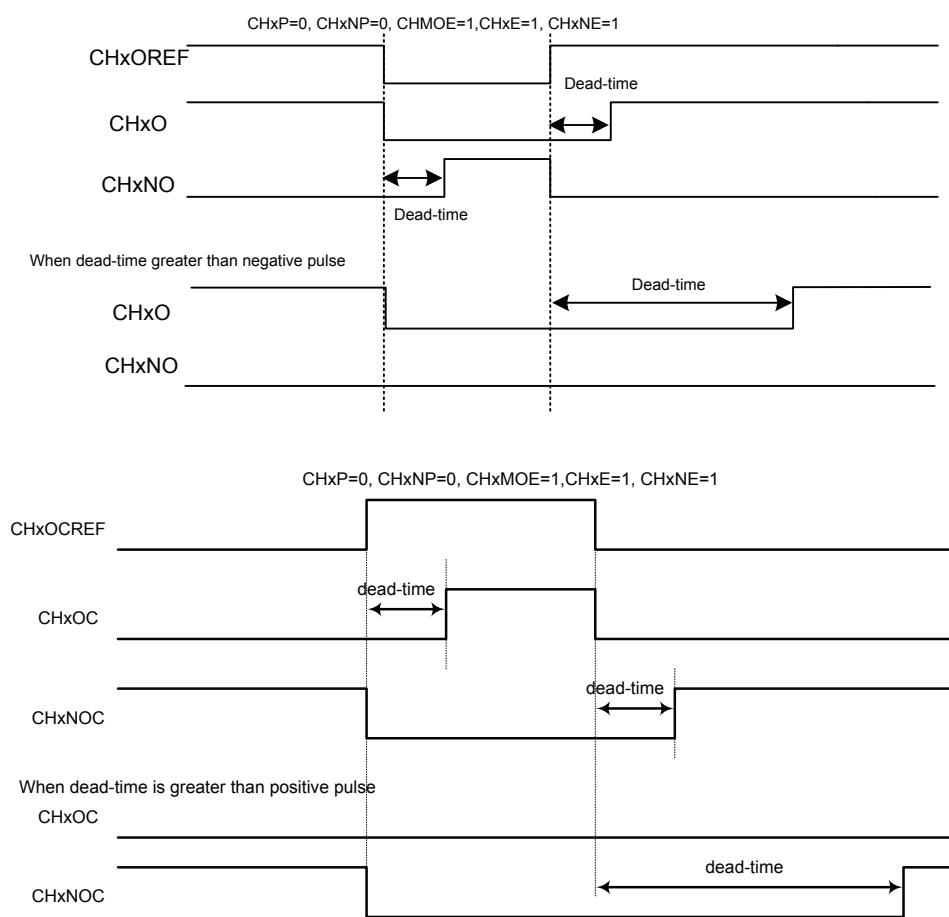


Figure 96. Dead-time Insertion Performed for Complementary Outputs

If the delay is greater than the width of the active output of CHxO or CHxNO, then the corresponding PWM pulses will not be generated.

Break Function

The MCTM includes break function and maximum two input signals for MCTM break. The MT_BRK0 is default function and from external MTn_BRK pin. But the second break signal MT_BRK1 is share with the MT_ETI pin and default is disabled. It can set the BRK1SEL bit in CHBRKCTR register to select the MT_ETI pin for extra break signal MT_BRK1. The detail block diagram is shown as below figure.

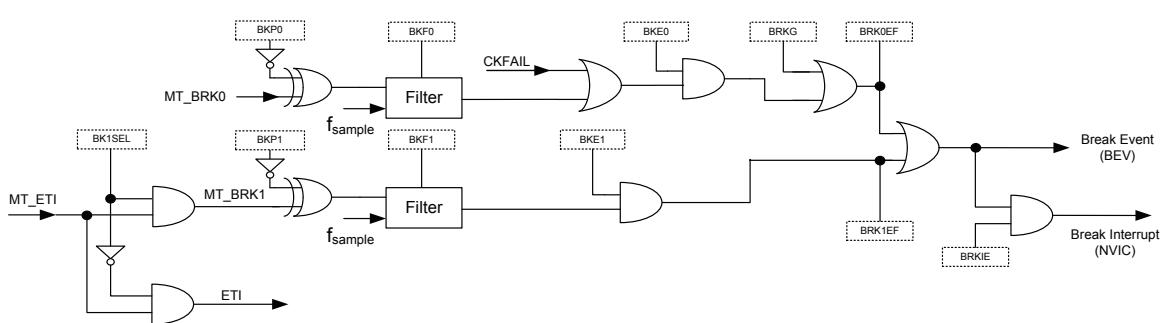


Figure 97. Break signal bolck diagram for MCTM

When the MT_BRK input has an active level or the Clock Monitor Circuitry detects a clock failure event, a break event will be generated if the break function is enabled. Meanwhile, each channel output will be forced to a reset state, an inactive or idle state. Moreover, a break event can also be generated by the software asserting the BRKG bit in the EVGR register even if the break function is disabled.

The MT_BRK input signal can be enabled by by setting the BKE bit in the CHBRKCTR register. The break input polarity can be selected by setting the BKP bit in CHBRKCTR register. The BKE and BKP bits can be modified at the same time.

The digital filters are embedded in the input stage and clock controller block for the break signal. The input filter of the MT_BRK signal can be enabled by by setting the BKF bits in the CHBRKCTR register. The digital filter is an N-event counter where N refers to how many valid transitions are necessary to output a filtered signal.

Digital Filter (N=2)

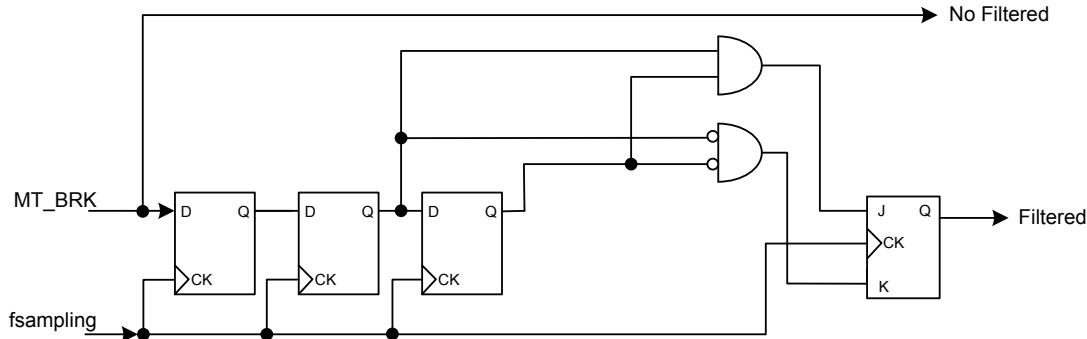


Figure 98. MT_BRK Pin Digital Filter Diagram with N = 2

When using the break function, the channel output enable signals and output levels are changed depending on several control bits which include the CHMOE, CHOSSI, CHOSSR, CHxOIS and CHxOISN bits. Once a break event occurs, the output enable bit CHMOE will be cleared asynchronously. The break interrupt flag, BRKIF, will be set and then an interrupt will be generated if the break function interrupt is enabled by setting the BRKIE bit to 1. The channel output behavior is as described below:

- If complementary outputs are used, the channel outputs a level signal first which can be selected to be either a disable or inactive level, selected by configuring the CHOSSI bit in the CHBRKCTR register. After the dead-time duration, the outputs will be changed to the idle state. The idle state is determined by the CHxOIS/CHxOISN bits in the CHBRKCFR register.
- If complementary outputs are not used (Channel 3), the channel will output an idle state. The main output enable control bit, CHMOE can not be set until the break event is cleared.

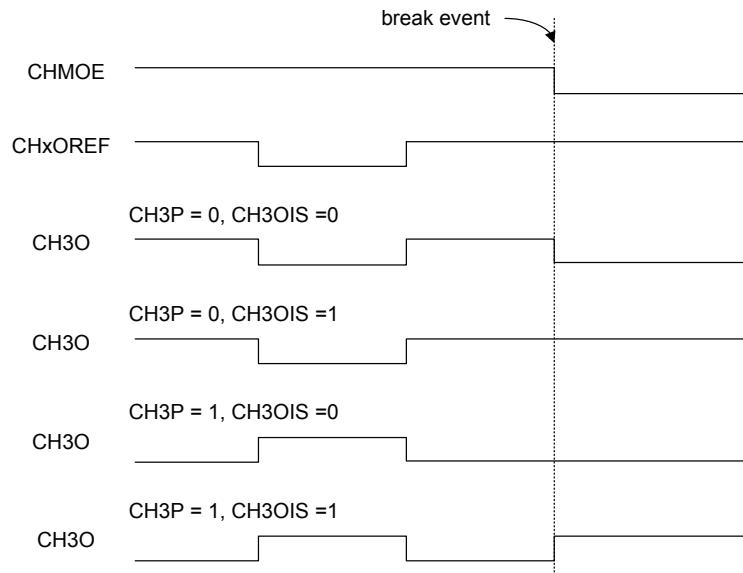


Figure 99. Channel 3 Output with a Break Event Occurrence

The accompanying diagram shows that the complementary output states when a break event occurs where the complementary outputs are enabled by setting both the CHxE and CHxNE bits to 1.

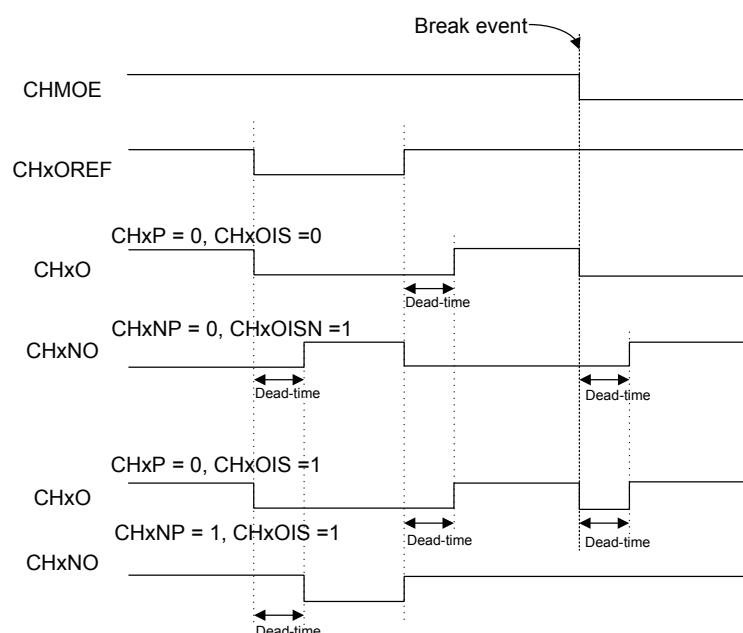


Figure 100. Channel 0 ~ 2 Complementary Outputs with a Break Event Occurrence

The accompanying diagram shows the output states in the case of the output being enabled by setting the CHxE bit to 1 and the complementary output being disabled by clearing the CHxNE to 0 when a break event occurs.

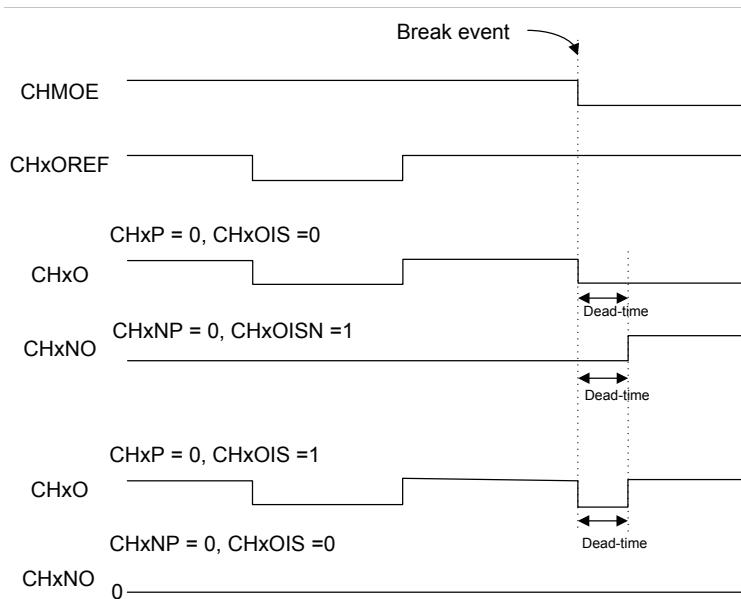


Figure 101. Channel 0 ~ 2 Only One Output Enabled when Fault Event Occurs

The CHxO and CHxNO complementary outputs should not be set to an active level at the same time. The hardware will protect the MCTM circuitry to force only one channel output to be in the active state.

Example: Both CHxOIS and CHxOISN are set to active levels after a break event; only the CHxO waveform is generated.

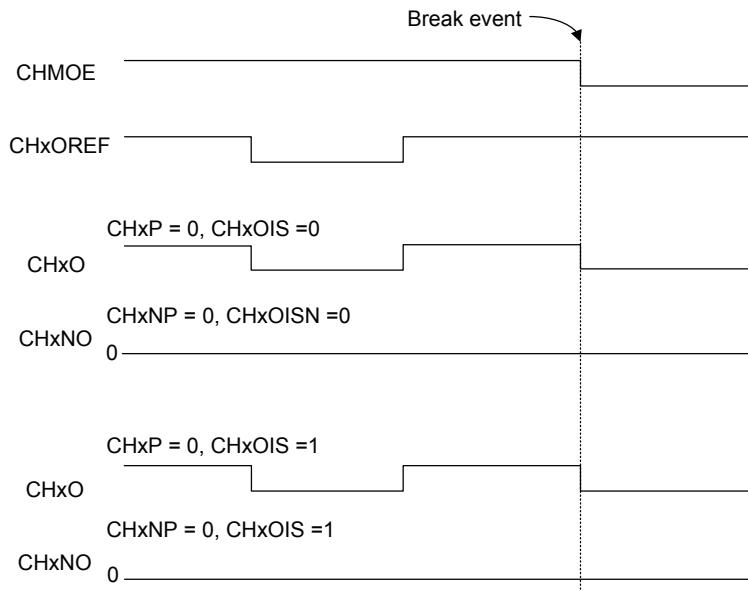


Figure 102. Hardware Protection When Both CHxO and CHxNO Are in Active Condition

CHMOE can be set automatically by update event 1 if the automatic output enable function is enabled by setting the CHAOE bit in the CHBRKCTR register to 1.

Channel Complementary Output with Break Function

The Channel complementary outputs, CHxO and CHxNO, are enabled by a combination of the CHxE, CHxNE, CHMOE, CHOSSR, CHOSSI control bits.

Table 36. Output Control Bits for Complementary Output with a Break Event Occurrence

Control bit					Output status	
CHMOE	CHOSSI	CHOSSR	CHxE	CHxNE	MT_CHx Pin output state	MT_CHxN Pin output state
1 (Run)	x	0	0	0	Output disabled - floating - not driven by the timer MT_CHx ^(Note 1) = floating MT_CHx_OEN ^(Note 2) = 1	Output disabled - floating - not driven by the timer MT_CHxN = floating MT_CHxN_OEN = 1
		0	0	1	Output disable - floating - not driven by the timer MT_CHx_OEN = 1	Output enabled MT_CHxN = CHx_OREF xor CHxNP MT_CHxN_OEN = 0
		0	1	0	Output enabled MT_CHx = CHx_OREF xor CHxP MT_CHx_OEN = 0	Output disabled - floating - not driven by the timer MT_CHxN = floating MT_CHxN_OEN = 1
		0	1	1	Output enabled MT_CHx = CHx_OREF xor CHxP + dead-time MT_CHx_OEN = 0	Output enabled MT_CHxN = not CHx_OREF xor CHxNP + dead-time MT_CHxN_OEN = 0
		1	0	0	Output disabled - floating - not driven by the timer MT_CHx = floating MT_CHx_OEN = 1	Output disabled floating - not driven by the timer MT_CHxN = floating MT_CHxN_OEN = 1
		1	0	1	Off-State MT_CHx = CHxP MT_CHx_OEN = 0	Output enabled MT_CHxN = CHx_OREF xor CHxNP MT_CHxN_OEN = 0
		1	1	0	Output enabled MT_CHx = CHx_OCREF xor CHxP MT_CHx_OEN = 0	Off-State MT_CHxN = CHxNP MT_CHxN_OEN = 0
		1	1	1	Output enabled MT_CHx = CHx_OREF xor CHxP + dead-time MT_CHx_OEN = 0	Output enabled MT_CHxN = not CHx_OREF xor CHxNP + dead-time MT_CHxN_OEN = 0
0 (Idle)	x	0	0	0	Before dead-time: Output disabled - floating MT_CHx = floating, MT_CHxN = floating MT_CHx_OEN = 1, MT_CHxN_OEN = 1	
		0	0	1		
		0	1	0		
		0	1	1		
		1	0	0		
		1	0	1	Before dead-time: Off state MT_CHx = CHxP, MT_CHxN = CHxNP MT_CHx_OEN = 0, MT_CHxN_OEN = 0	
		1	0	0		
		1	1	1		
		1	1	1	After dead-time: Output enabled MT_CHx = CHxOIS, MT_CHxN = CHxOISN MT_CHx_OEN = 0, MT_CHxN_OEN = 0	

Note: 1. The MT_CHx pin is the MCTM I/O Pin.

2. The MT_CHx_OEN and MT_CHxN_OEN signals are the MCTM I/O pin output enable combinational logic control signals which are active low.

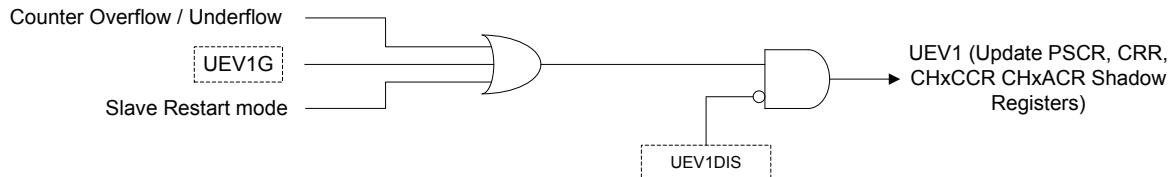
Update Management

The update events are categorised into two different types which are the update event 1, UEV1, and update event 2, UEV2. The update event 1 is used to update the CRR, the PSCR and the CHxCCR values from the actual registers to the corresponding shadow registers. An update event 1 occurs when the counter overflows or underflows, the UEV1G bit is set or the slave restart mode is triggered. The update event 2 is used to update the CHxE, CHxNE and CHxOM control bits. An update event 2 is generated when a rising edge on the STI occurs or the corresponding software update control bit is set.

Update Event 1

The UEV1DIS bit in the CNTCFR register can determine whether an update event 1 occurs or not. When the update event 1 occurs, the corresponding update event interrupt will be generated depending upon whether the update event 1 interrupt generation function is enabled or not by configuring the UGDIS bit in the CNTCFR register. For a more detailed description, refer to the UEV1DIS and UGDIS bit definition in the CNTCFR register.

Update Event 1 Management



Update Event 1 Interrupt Management

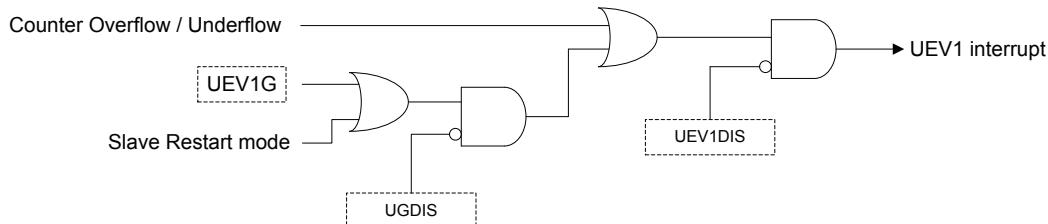


Figure 103. Update Event 1 Setup Diagram

Update Event 2

The CHxE, CHxNE, CHxOM control bits for the complementary outputs can be preloaded by setting the COMPRE bit in the CTR register. Here the shadow bits of the CHxE, CHxNE, CHxOM bits will be updated when an update event 2 occurs.

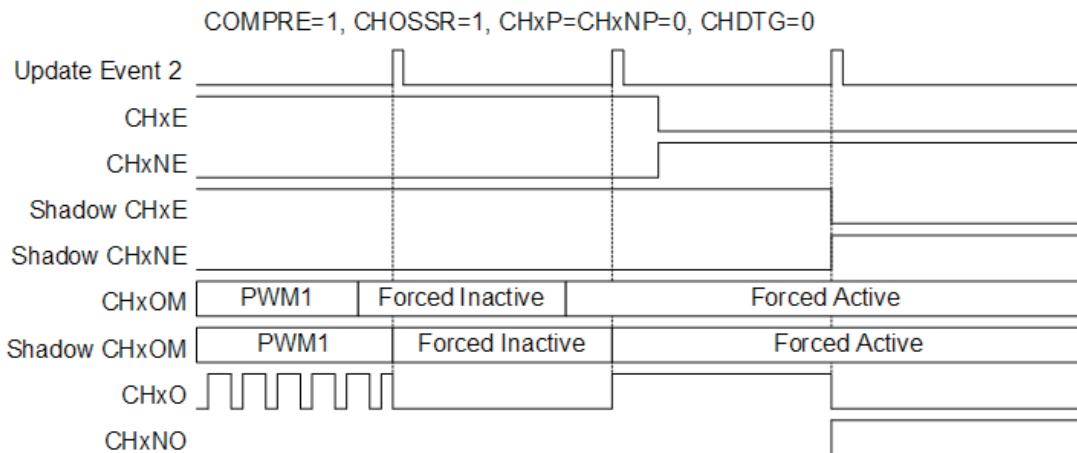


Figure 104. CHxE, CHxNE and CHxOM Updated by Update Event 2

An update event 2 can be generated by setting the software update bit, UEV2G, in the EVGR register or by the rising edge of the STI signal if the COMUS bit is set in the CTR register.

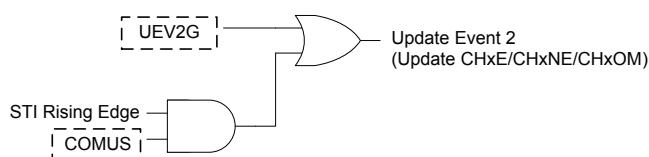


Figure 105. Update Event 2 Setup Diagram

Quadrature Decoder

The Quadrature Decoder function uses two quadrantal inputs TI0 and TI1 derived from the MTx_CH0 and MTx_CH1 pins respectively which interact to generate the counter value. The DIR bit is modified by hardware automatically during each input source transition. The counter is counting on TI0 edges only, TI1 edges only or both TI0 and TI1 edges. The selection is made by setting the SMSEL field to 0x01, 0x02 or 0x03. The mechanism for changing the counter direction is shown in the following table. The Quadrature decoder can be regarded as an external clock with a directional selection. This means that the counter counts continuously in the interval between 0 and the counter-reload value. The application program must therefore configure the CRR register before the counter starts to count.

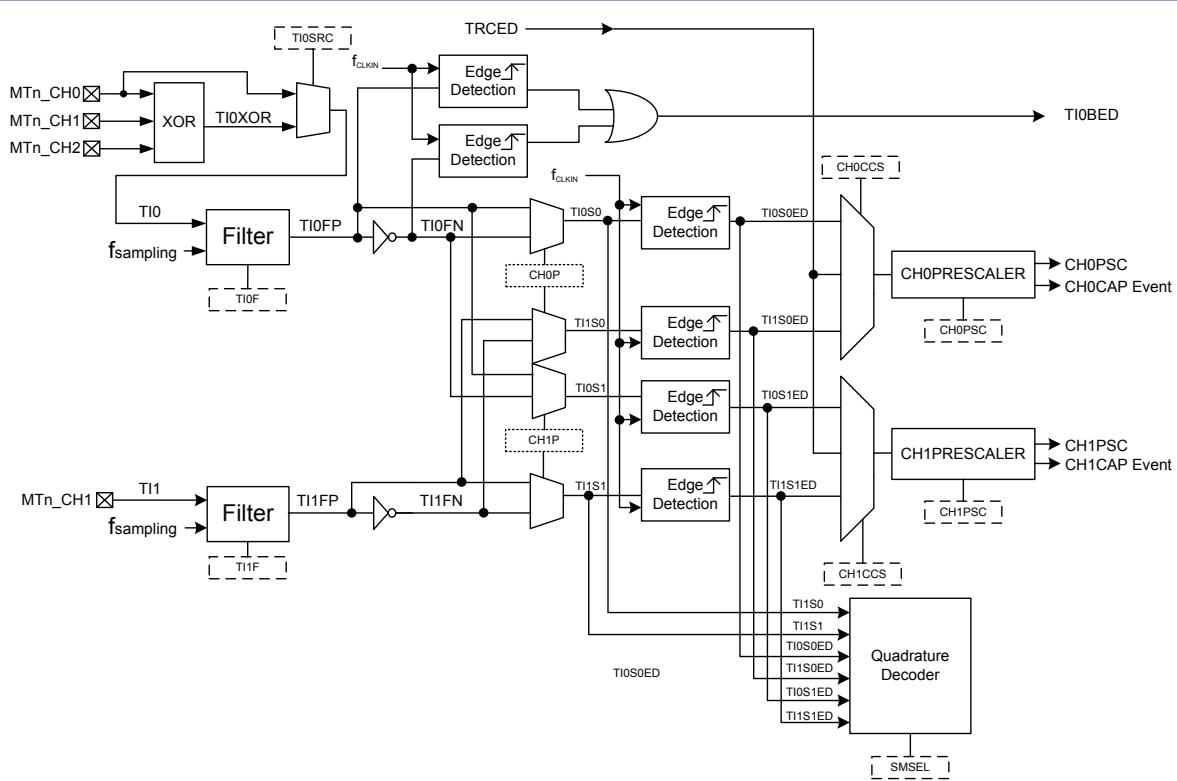


Figure 106. Input Stage and Quadrature Decoder Block Diagram

Table 37. Counting Direction and Encoding Signals

Counting mode	Level	TI0S0		TI1S1	
		Rising	Falling	Rising	Falling
Counting on TI0 only (SMSEL = 0x01)	TI1S1 = High	Down	Up	—	—
	TI1S1 = Low	Up	Down	—	—
Counting on TI1 only (SMSEL = 0x02)	TI0S0 = High	—	—	Up	Down
	TI0S0 = Low	—	—	Down	Up
Counting on TI0 and TI1 (SMSEL = 0x03)	TI1S1 = High	Down	Up	X	X
	TI1S1 = Low	Up	Down	X	X
	TI0S0 = High	X	X	Up	Down
	TI0S0 = Low	X	X	Down	Up

Note: "—" → means "no counting"; "X" → impossible

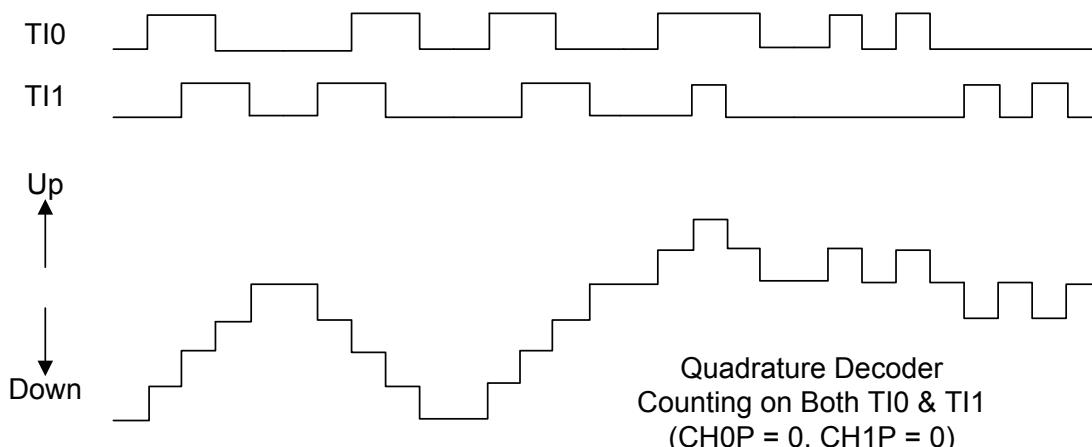


Figure 107. Both TI0 and TI1 Quadrature Decoder Counting

Digital Filter

The digital filters are embedded in the input stage and clock controller block for the MTn_CH0 ~ MTn_CH3 and MTn_ETI pins. The digital filter in the MCTM is an N-event counter where N refers to how many valid transitions are necessary to output a filtered signal. The N value can be 0, 2, 4, 5, 6 or 8 according to the selection for each filter.

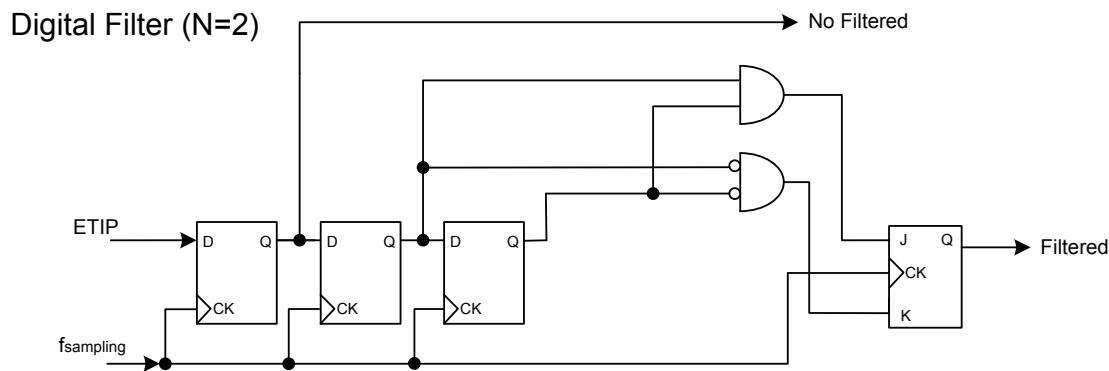


Figure 108. MTn_ETI Pin Digital Filter Diagram with N = 2

Clearing CHxOREF when ETIF is high

The CHxOREF signal can be forced to 0 when the ETIF signal is set to a high level by setting the REFxCE bit to 1 in the CHxOCFR register. The CHxOREF signal will not return to its active level until the next update event 1 occurs.

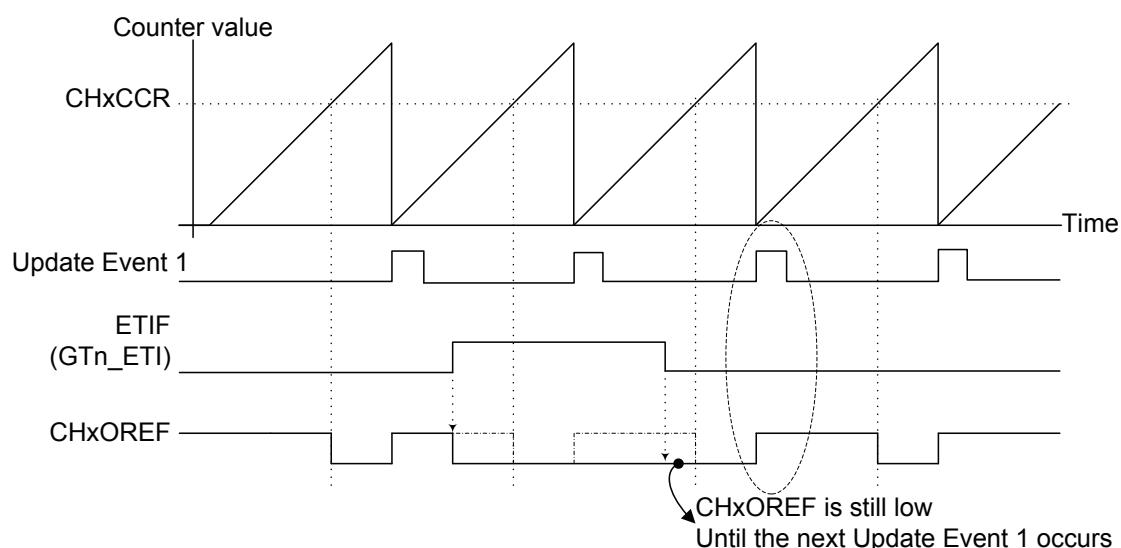


Figure 109. Clearing CHxOREF by ETIF

Single Pulse Mode

Once the timer is set to operate in the single pulse mode, it is not necessary to set the timer enable bit TME in the CTR register to 1 to enable the counter. The trigger to generate a pulse can be sourced from the STI signal rising edge or by setting the TME bit to 1 using software. Setting the TME bit to 1 or a trigger from the STI signal rising edge can generate a pulse and then keep the TME bit at a high state until the update event 1 occurs or the TME bit is cleared to 0 by software. If the TME bit is cleared to 0 using software, the counter will be stopped and its value held. If the TME bit is automatically cleared to 0 by a hardware update event 1, the counter will be reinitialised.

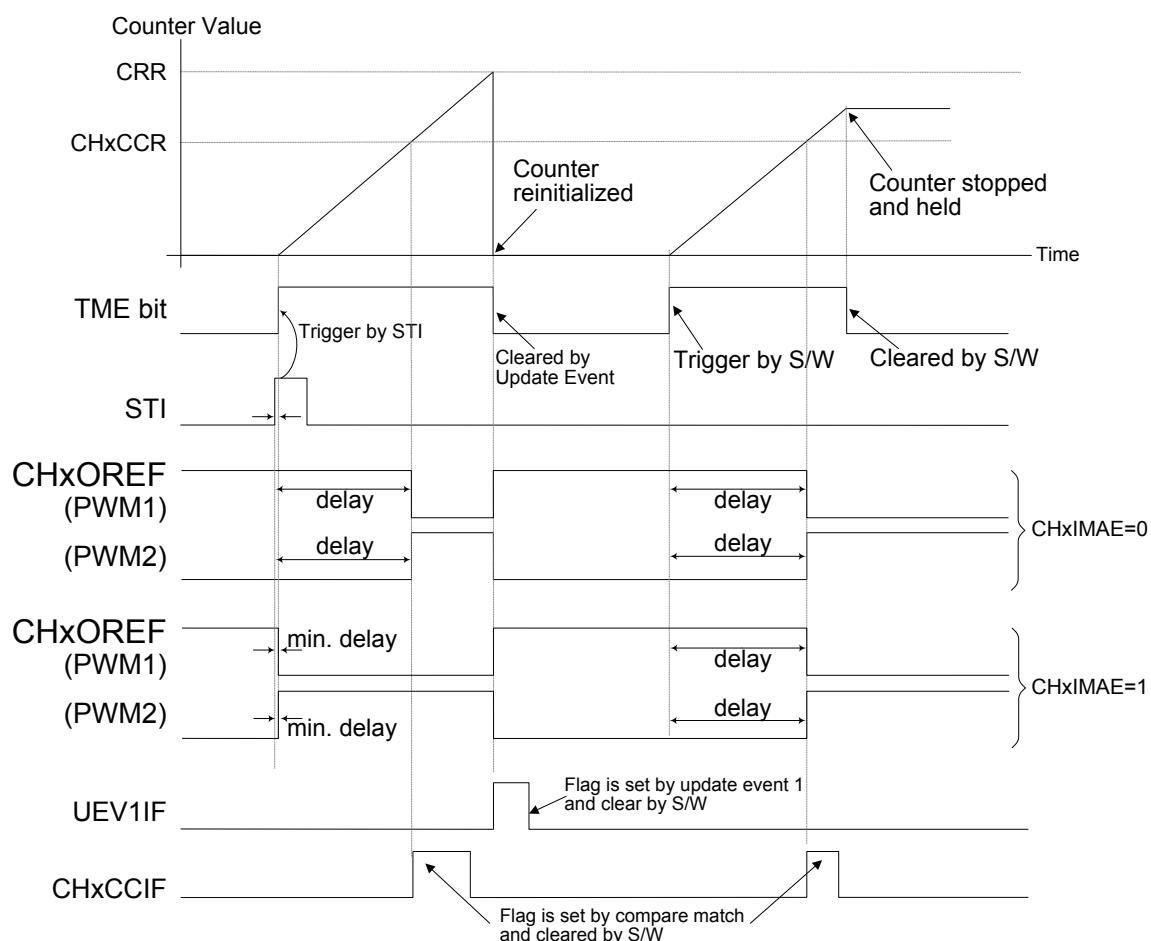


Figure 110. Single Pulse Mode

In the Single Pulse mode, the STI active edge which sets the TME bit to 1 will enable the counter. However, there exist several clock delays to perform the comparison result between the counter value and the CHxCCR value. In order to reduce the delay to a minimum value, users can set the CHxIMAE bit in each CHxOCFR register. After a STI rising edge trigger occurs in the single pulse mode, the CHxOREF signal will immediately be forced to the state to which the CHxOREF signal will change to as the compare match event occurs without taking the comparison result into account. The CHxIMAE bit is available only when the output channel is configured to operate in the PWM1 or PWM2 output mode and the trigger source is derived from the STI signal.

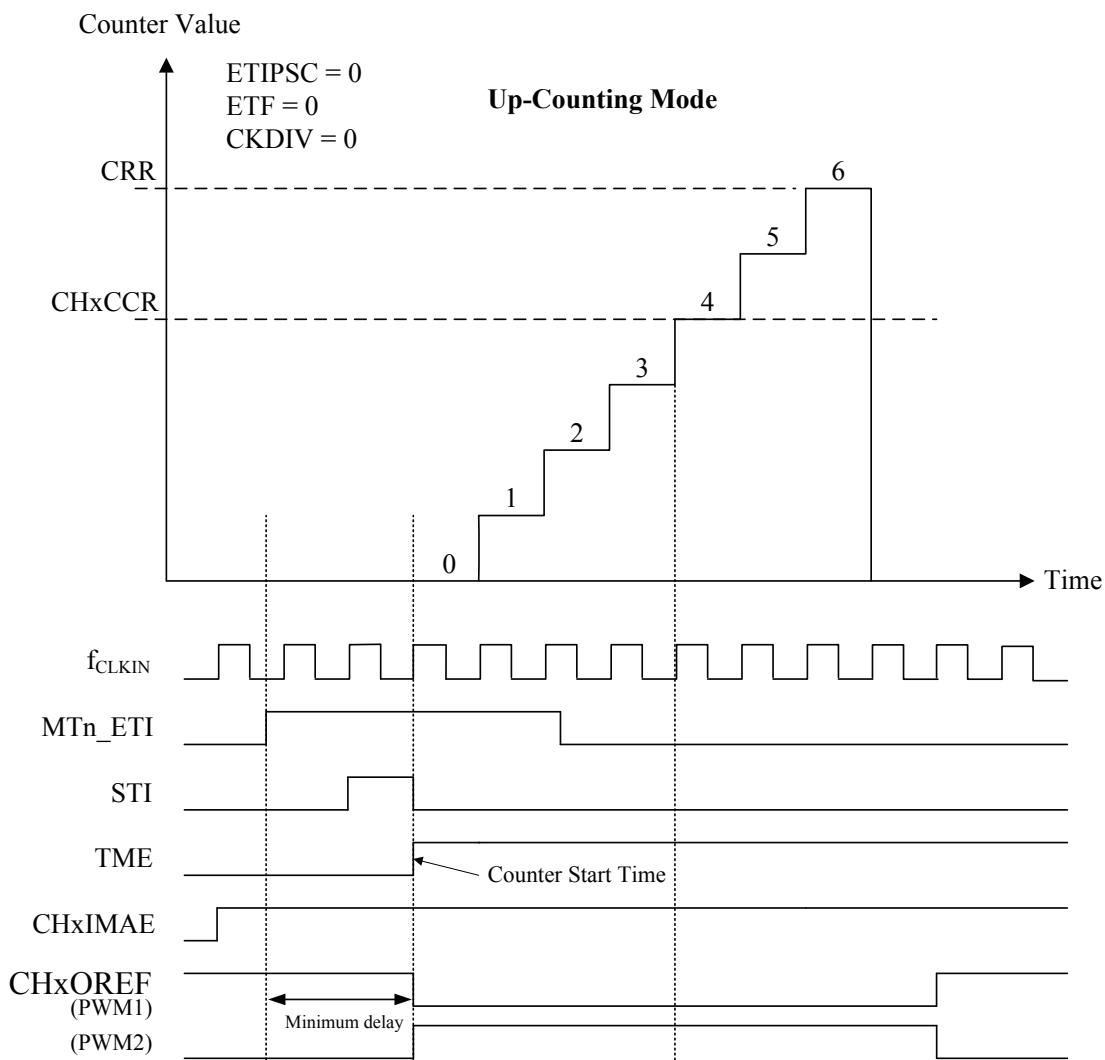


Figure 111. Immediate Active Mode Minimum Delay

Asymmetric PWM Mode

Asymmetric PWM mode allows two center-aligned PWM signals to be generated with a programmable phase shift. While the PWM frequency is determined by the value of the MCTMx_CRR register, the duty cycle and the phase-shift are determined by the CHxCCR and CHxACR register. When the counter is counting up, the PWM using the value in CHxCCR as up-count compare value. When the counter is into counting down stage then using the value in CHxACR as down-count compare value. The Figure 112 is shown a example for asymmetric PWM mode in Center-aligned Counting mode.

Note: Asymmetric PWM mode can only be operated in Center-aligned Counting mode.

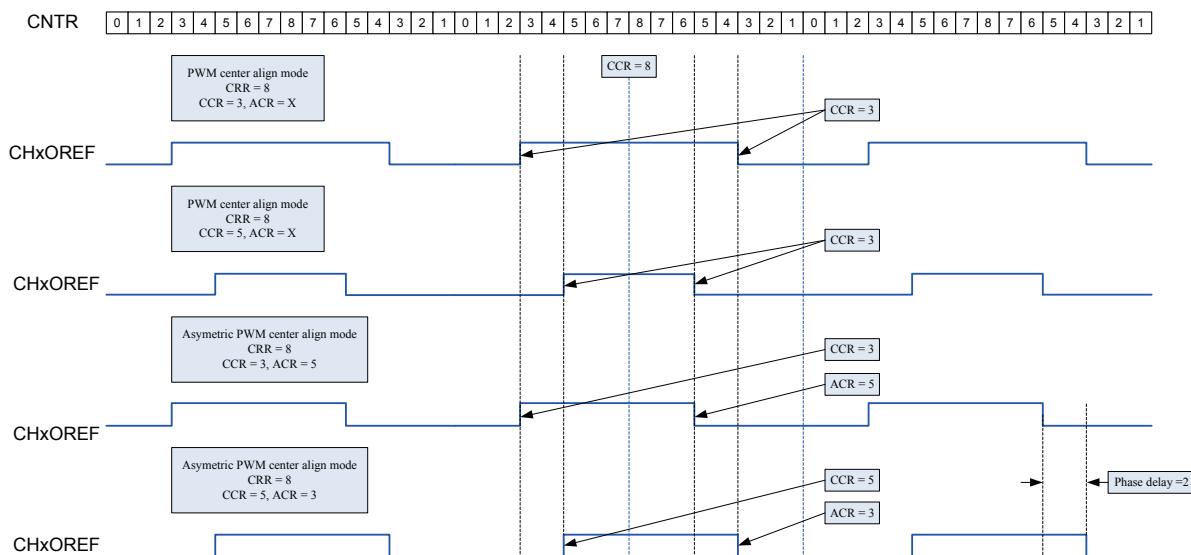


Figure 112. Asymmetric PWM mode versus Center-aligned Counting mode

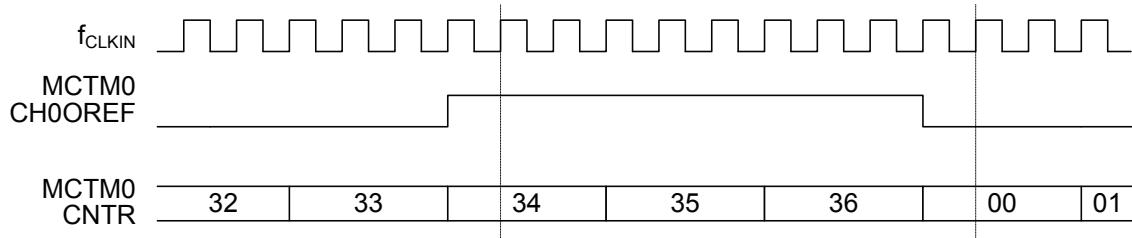
Time Interconnection

The timers can be internally connected together for timer chaining or synchronization. This can be implemented by configuring one timer to operate in the Master mode while configuring another timer to be in the Slave mode. The following figures present several examples of trigger selection for the master and slave modes.

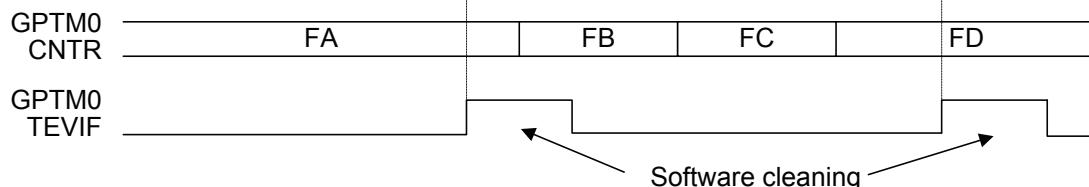
Using one timer to trigger another timer to start or stop counting

- Configure MCTM0 to be in the master mode and to send its channel 0 Output Reference signal CH0OREF as a trigger output (MMSEL = 0x04).
- Configure the MCTM0 CH0OREF waveform.
- Configure the GPTM0 to receive its input trigger source from the MCTM0 trigger output (TRSEL = 0x0A).
- Configure GPTM0 to operate in the pause mode (SMSEL = 0x05).
- Enable GPTM0 by writing "1" to the TME bit.
- Enable MCTM0 by writing "1" to the TME bit.

Master MCTM0



Slave GPTM0



Software cleaning

Figure 113. Pausing GPTM0 using the MCTM0 CH0OREF Signal

Using one timer to trigger another timer to start counting

- Configure MCTM0 to operate in the master mode and to send its Update Event UEV as the trigger output (MMSEL = 0x02).
- Configure the MCTM0 period by setting the CHxCRR register.
- Configure GPTM0 to get the input trigger source from the MCTM0 trigger output (TRSEL = 0x0A).
- Configure GPTM0 to be in the slave trigger mode (SMSEL = 0x06).
- Start MCTM0 by writing ‘1’ to the TME bit.

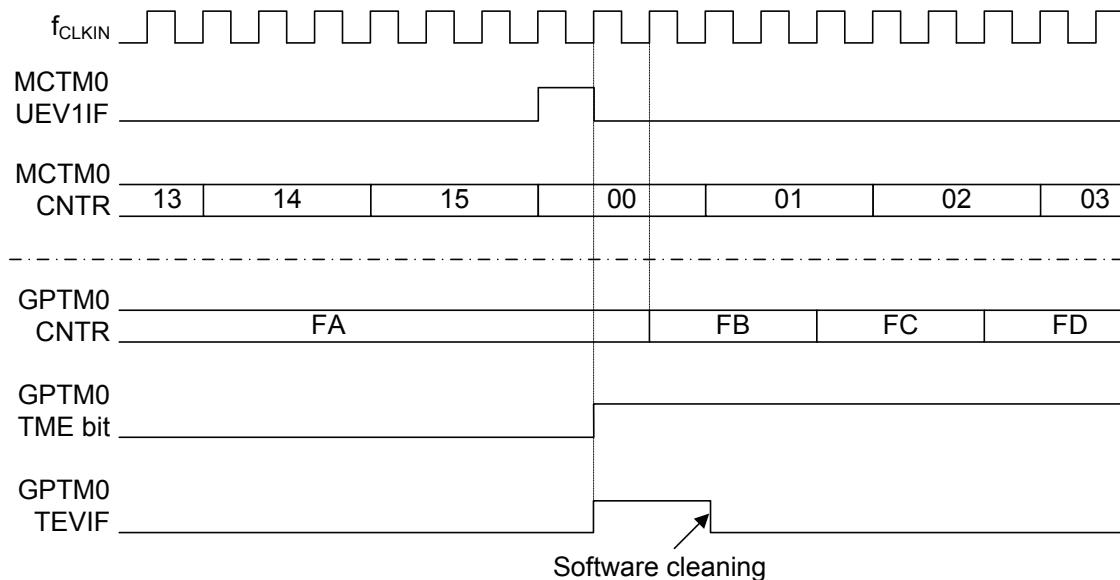
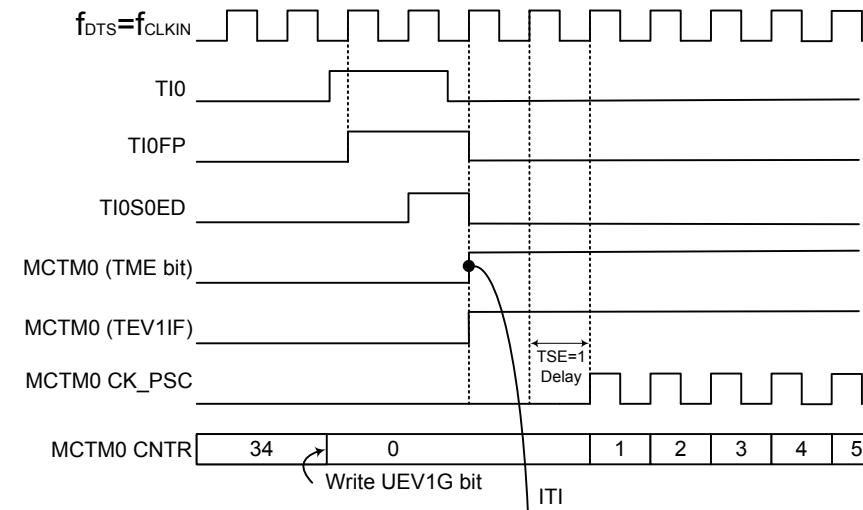


Figure 114. Triggering GPTM0 with MCTM0 Update Event 1

Starting two timers synchronously in response to an external trigger

- Configure MCTM0 to operate in the master mode to send its enable signal as a trigger output (MMSEL = 0x01).
- Configure MCTM0 slave mode to receive its input trigger source from MTn_CH0 pin (TRSEL = 0x01).
- Configure MCTM0 to be in the slave trigger mode (SMSEL = 0x06).
- Enable the MCTM0 master timer synchronisation function by setting the TSE bit in the MDCFR register to 1 to synchronise the slave timer.
- Configure GPTM0 to receive its input trigger source from the MCTM0 trigger output (TRSEL = 0x0A).
- Configure GPTM0 to be in the slave trigger mode (SMSEL = 0x06).

Master MCTM0



Slave GPTM0



Figure 115. Trigger MCTM0 and GPTM0 with the MCTM0 CH0 Input

Using one timer as a hall sensor interface to trigger another timer with update event 2

GPTM0

- Configure channel 0 to choose an input XOR function (TI0SRC = 1)
- Configure channel 0 to be in the input capture mode and TRCED as capture source (CH0CCS= 0x03) and Enable channel 0 (CH0E=1)
- Configure the UEVG bit as the source of MTO (MMSEL= 0x00)
- Configure TI0BED to be connected to STI (TRSEL = 0x08)
- Configure the counter to be in the slave restart mode (SMSEL = 0x04)
- Enable GPTM0 (TME=1)

MCTM0

- Select GPTM0 MTO to be the STI source of MCTM (TRSEL = 0x0A)
- Enable the CHxE, CHxNE and CHxOM preload function (COMPRE = 1)
- Select the rising edge on STI to generate an update event 2 (COMUS = 1)
- Enable the update event 2 interrupt (UEV2IE = 1)
- In the update event 2 ISR: write CHxE, CHxNE and CHxOM register for the next step

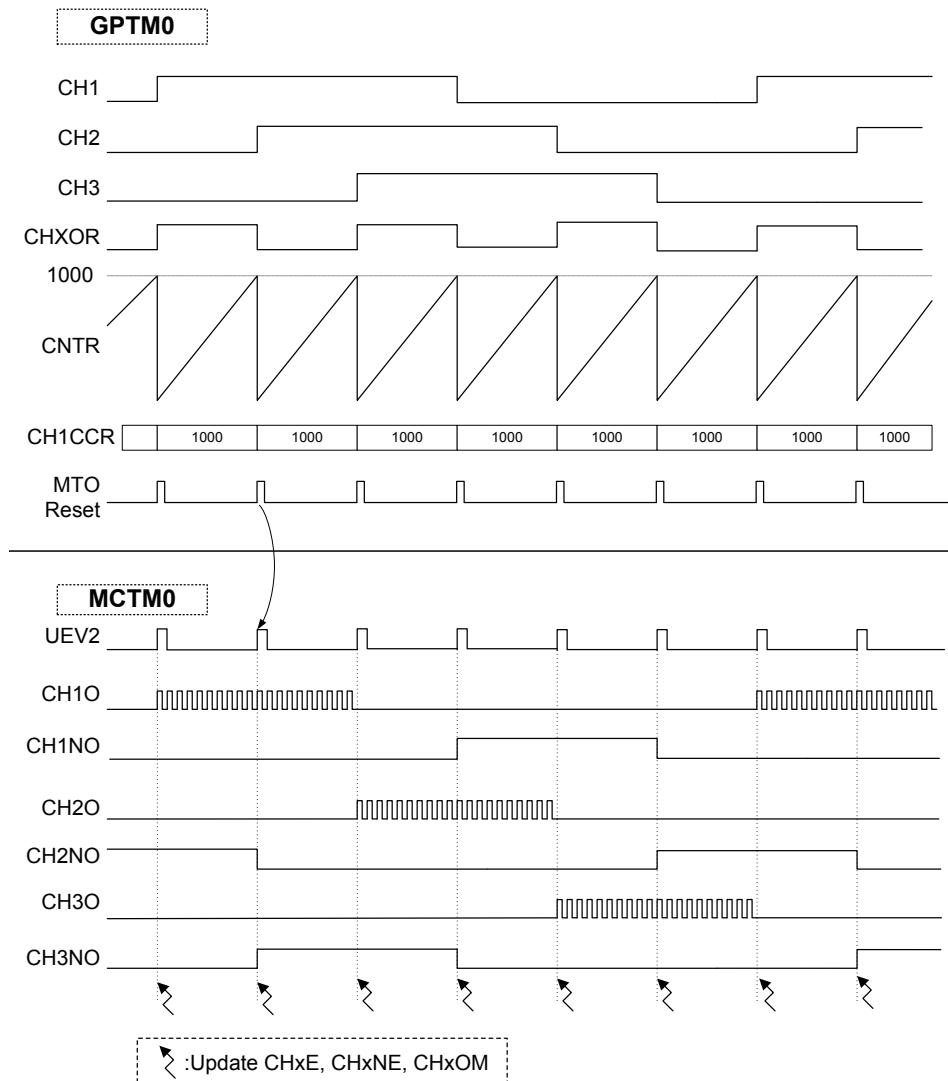


Figure 116. CH1XOR Input as Hall Sensor Interface

Trigger ADC Start

To interconnect to the Analog-to-Digital Converter, the MCTM can output the MTO signal or the channel output MTn_CHx (x = 0 ~ 3) signal to be used as an Analog-to-Digital Converter input trigger signal.

Lock Level Table

In addition to the break input and output management, a write protection has been internally implemented in the break circuitry to safeguard the application. Users can choose one protection level selected by the LOCKLV bits to protect the relative control bits of the registers. The LOCKLV bits can only be written once after an MCTM or system reset. Then the protected bits will be locked and can not be changed anymore except by the MCTM reset or when the system is reset.

Table 38. Lock Level Table

Lock Configuration	Protected Bits					
Lock Level 1 (LOCKLV = "01")	CHDTG	CHxOIS	CHxOISN	BKE	BKP	CHAOE
Lock Level 2 (LOCKLV = "10")	CHDTG	CHxOIS	CHxOISN	BKE	BKP	CHAOE
	CHxP	CHxNP	CHOSSI	CHOSSR	MCTMEN ⁽¹⁾	CKMEN ⁽²⁾
Lock Level 3 (LOCKLV = "11")	CHDTG	CHxOIS	CHxOISN	BKE	BKP	CHAOE
	CHxP	CHxNP	CHOSSI	CHOSSR	MCTMEN ⁽¹⁾	CKMEN ⁽²⁾
	CHxPRE	CHxOM				

- (1) The MCTMEN bit of the APBCCR1 register is located in the CKCU unit and use to control the clock source of the MCTM unit.
- (2) The CKMEN bit of the GCCR register is located in the CKCU unit and use to monitor the high speed external clock (HSE) source. If the CKMEN bit is enabled and when hardware detects HSE clock stuck at low/high state, internal hardware will automatically switch the system clock to internal high speed RC clock (HSI) to protect the system safty.
- (3) When the MCTMEN and CKMEN control bits of the CKCU lock protection mode is enabled in the MCTM unit, the bits will be allowed to enable only and inhibited to disable again.

PDMA Request

The MCTM has a PDMA data transfer interface. There are certain events which can generate PDMA requests if the corresponding enable control bits are set to 1 to enable the PDMA access. These events are the MCTM update events, trigger event and channel capture/compare events. When the PDMA request is generated from the MCTM channel, it can be derived from the channel capture/compare event or the MCTM update event 1 selected by the channel PDMA selection bit, CHCCDS, for all channels. For more detailed PDMA configuring information, refer to the corresponding section in the PDMA chapter.

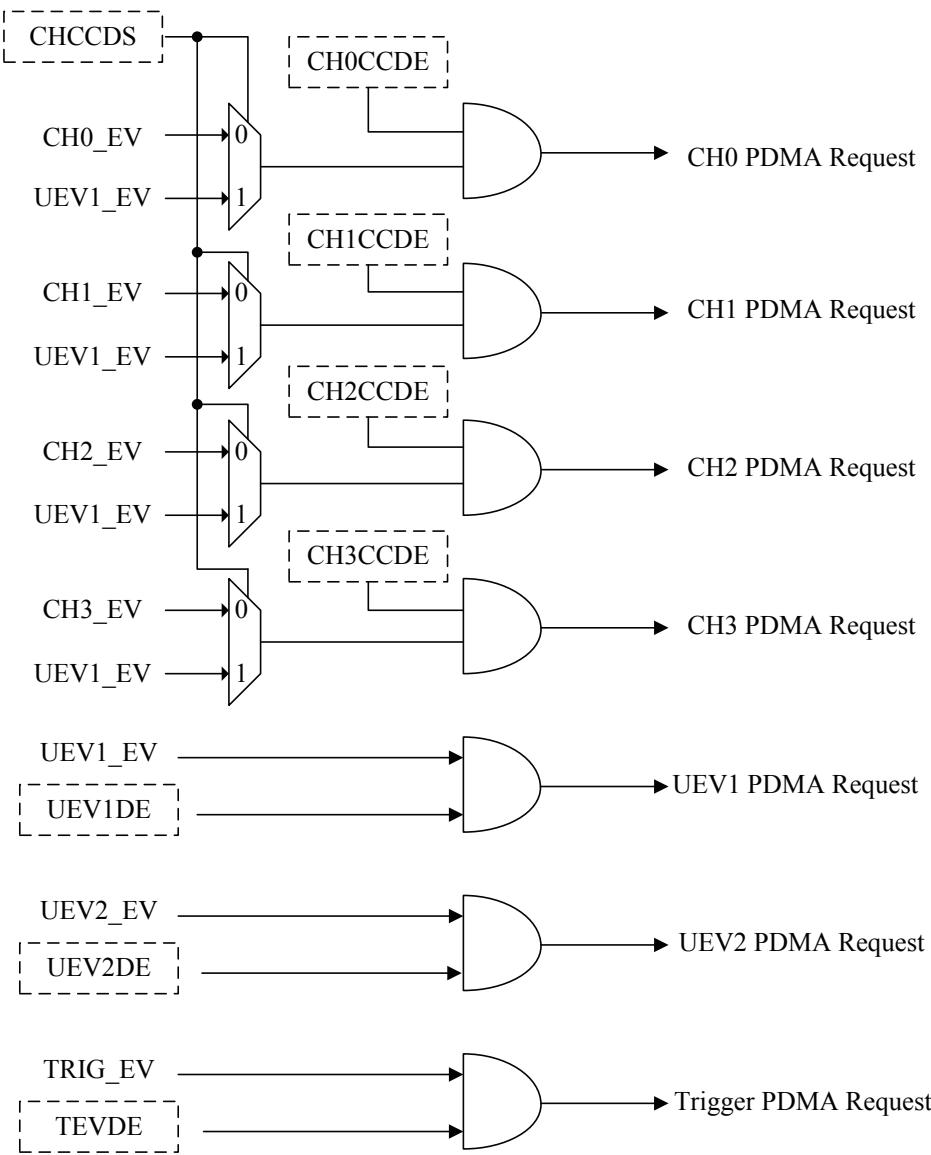


Figure 117. MCTM PDMA Mapping Diagram

Register Map

The following table shows the MCTM registers and reset values.

Table 39. MCTM Register Map

Register	Offset	Description	Reset Value
MCTM0 Base Address = 0x4002_C000			
MCTM1 Base Address = 0x4002_D000			
CNTCFR	0x000	Timer Counter Configuration Register	0x0000_0000
MDCFR	0x004	Timer Mode Configuration Register	0x0000_0000
TRCFR	0x008	Timer Trigger Configuration Register	0x0000_0000
CTR	0x010	Timer Control Register	0x0000_0000
CH0ICFR	0x020	Channel 0 Input Configuration Register	0x0000_0000
CH1ICFR	0x024	Channel 1 Input Configuration Register	0x0000_0000
CH2ICFR	0x028	Channel 2 Input Configuration Register	0x0000_0000
CH3ICFR	0x02C	Channel 3 Input Configuration Register	0x0000_0000
CH0OCFR	0x040	Channel 0 Output Configuration Register	0x0000_0000
CH1OCFR	0x044	Channel 1 Output Configuration Register	0x0000_0000
CH2OCFR	0x048	Channel 2 Output Configuration Register	0x0000_0000
CH3OCFR	0x04C	Channel 3 Output Configuration Register	0x0000_0000
CHCTR	0x050	Channel Control Register	0x0000_0000
CHPOLR	0x054	Channel Polarity Configuration Register	0x0000_0000
CHBRKCFR	0x06C	Channel Break Configuration Register	0x0000_0000
CHBRKCTR	0x070	Channel Break Control Register	0x0000_0000
DICTR	0x074	Timer PDMA/Interrupt Control Register	0x0000_0000
EVGR	0x078	Timer Event Generator Register	0x0000_0000
INTSR	0x07C	Timer Interrupt Status Register	0x0000_0000
CNTR	0x080	Timer Counter Register	0x0000_0000
PSCR	0x084	Timer Prescaler Register	0x0000_0000
CRR	0x088	Timer Counter Reload Register	0x0000_FFFF
REPR	0x08C	Timer Repetition Register	0x0000_0000
CH0CCR	0x090	Channel 0 Capture/Compare Register	0x0000_0000
CH1CCR	0x094	Channel 1 Capture/Compare Register	0x0000_0000
CH2CCR	0x098	Channel 2 Capture/Compare Register	0x0000_0000
CH3CCR	0x09C	Channel 3 Capture/Compare Register	0x0000_0000
CH0ACR	0x0A0	Channel 0 Asymmetric Compare Register	0x0000_0000
CH1ACR	0x0A4	Channel 1 Asymmetric Compare Register	0x0000_0000
CH2ACR	0x0A8	Channel 2 Asymmetric Compare Register	0x0000_0000
CH3ACR	0x0AC	Channel 3 Asymmetric Compare Register	0x0000_0000

Register Descriptions

Timer Counter Configuration Register – CNTCFR

This register specifies the MCTM counter configuration.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Type/Reset	Reserved							
	23	22	21	20	19	18	17	16
Type/Reset	Reserved							
	15	14	13	12	11	10	9	8
Type/Reset	Reserved							
	7	6	5	4	3	2	1	0
Type/Reset	Reserved							

Bits	Field	Descriptions
[24]	DIR	<p>Counting Direction</p> <p>0: Count-up 1: Count-down</p> <p>Note: This bit is read only when the Timer is configured to be in the Center-aligned counting mode or when used as a Quadrature decoder</p>
[17:16]	CMSEL	<p>Counter Mode Selection</p> <p>00: Edge-aligned counting mode. Normal up-counting and down-counting available for this mode. Counting direction is defined by the DIR bit.</p> <p>01: Center-aligned counting mode 1. The counter counts up and down alternatively. The compare match interrupt flag is set during the count-down period.</p> <p>10: Center-aligned counting mode 2. The counter counts up and down alternatively. The compare match interrupt flag is set during the count-up period.</p> <p>11: Center-aligned counting mode 3. The counter counts up and down alternatively. The compare match interrupt flag is set during the count-up and count-down period.</p>
[9:8]	CKDIV	<p>Clock Division</p> <p>These two bits define the frequency ratio between the timer clock (f_{CLKIN}) and the dead-time clock (f_{DTS}). The dead-time clock is also used as the digital filter sampling clock.</p> <p>00: $f_{DTS} = f_{CLKIN}$ 01: $f_{DTS} = f_{CLKIN}/2$ 10: $f_{DTS} = f_{CLKIN}/4$ 11: Reserved</p>

Bits	Field	Descriptions
[1]	UGDIS	Update event 1 interrupt generation disable control 0: Any of the following events will generate an update PDMA request or interrupt - Counter overflow/underflow - Setting the UEV1G bit - Update generation through the slave mode 1: Only counter overflow/underflow generates an update PDMA request or interrupt
[0]	UEV1DIS	Update event 1 Disable control 0: Enable the update event 1 request by one of following events - Counter overflow/underflow - Setting the UEV1G bit - Update generation through the slave mode 1: Disable the update event 1 - however the counter and the prescaler are reinitialised if the UEV1G bit is set or if a hardware restart is received from the slave mode

Timer Mode Configuration Register – MDCFR

This register specifies the MCTM master and slave mode selection and single pulse mode.

Offset: 0x004

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Type/Reset	Reserved							SPMSET
	RW 0							
	23	22	21	20	19	18	17	16
Type/Reset	Reserved							MMSEL
	RW 0 RW 0 RW 0							
	15	14	13	12	11	10	9	8
Type/Reset	Reserved							SMSEL
	RW 0 RW 0 RW 0							
	7	6	5	4	3	2	1	0
Type/Reset	Reserved							TSE
	RW 0							

Bits	Field	Descriptions
[24]	SPMSET	<p>Single Pulse Mode Setting</p> <p>0: Counter counts normally irrespective of whether a update event occurred or not</p> <p>1: Counter stops counting at the next update event and then the TME bit is cleared by hardware</p>

Bits	Field	Descriptions	
[18:16]	MMSEL	Master Mode Selection Master mode selection is used to select the MTO signal source which is used to synchronise the other slave timer.	
MMSEL [2:0]	Mode	Descriptions	
000	Reset Mode	The MTO in the Reset mode is an output derived from one of the following cases: 1. Software setting UEV1G bit 2. Slave has trigger input when used in slave restart mode	
001	Enable Mode	The Counter Enable signal is used as the trigger output.	
010	Update Mode	The update event 1 is used as the trigger output according to one of the following cases when the UEV1DIS bit is cleared to 0: 1. Counter overflow/underflow 2. Software setting UEV1G 3. Slave has trigger input when used in slave restart mode	
011	Capture/Compare Mode	When a Channel 0 capture or compare match event occurs, it will generate a positive pulse which is used as the master trigger output.	
100	Compare output 0	The Channel 0 Output reference signal named CH0OREF is used as the trigger output.	
101	Compare output 1	The Channel 1 Output reference signal named CH1OREF is used as the trigger output.	
110	Compare output 2	The Channel 2 Output reference signal named CH2OREF is used as the trigger output.	
111	Compare output 3	The Channel 3 Output reference signal named CH3OREF is used as the trigger output.	

Bits	Field	Descriptions		
[10:8]	SMSEL	Slave Mode Selection		
		SMSEL [2:0]	Mode	Descriptions
		000	Disable mode	The prescaler is clocked directly by the internal clock.
		001	Quadrature Decoder mode 1	The counter uses the clock pulses generated from the interaction between the TI0 and TI1 signals to drive the counter prescaler. A transition of the TI0 edge is used in this mode depending upon the TI1 level.
		010	Quadrature Decoder mode 2	The counter uses the clock pulse generated from the interaction between the TI0 and TI1 signals to drive the counter prescaler. A transition of the TI1 edge is used in this mode depending upon the TI0 level.
		011	Quadrature Decoder mode 3	The counter uses the clock pulse generated from the interaction between the TI0 and TI1 signals to drive the counter prescaler. A transition of one channel edge is used in the quadrature decoder mode 3 depending upon the other channel level.
		100	Restart Mode	The counter value restarts from 0 or the CRR shadow register value depending upon the counter mode on the rising edge of the STI signal. The registers will also be updated.
		101	Pause Mode	The counter starts to count when the selected trigger input STI is high. The counter stops counting on the instant, not being reset, when the STI signal changes its state to a low level. Both the counter start and stop control are determined by the STI signal.
		110	Trigger Mode	The counter starts to count from the original value in the counter on the rising edge of the selected trigger input STI. Only the star of counter is controlled.
		111	STIED	The rising edge of the selected trigger signal STI will clock the counter.
[0]	TSE	Timer Synchronisation Enable		
		0: No action 1: Master timer (current timer) will generate a delay to synchronise its slave timer through the MTO signal.		

Timer Trigger Configuration Register – TRCFR

This register specifies the MCTM external clock setting and the trigger source selection.

Offset: 0x008

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Type/Reset	Reserved							ECME
	23	22	21	20	19	18	17	16
Type/Reset	Reserved							ETIPOL
	15	14	13	12	11	10	9	8
Type/Reset	Reserved		ETIPSC			ETF		
			RW	0	RW	0	RW	0
	7	6	5	4	3	2	1	0
Type/Reset	Reserved				TRSEL			
					RW	0	RW	0
					RW	0	RW	0

Bits	Field	Descriptions
[24]	ECME	External Clock Mode Enable 0: External clock mode is disabled. 1: External clock mode is enabled. The following two setting have the same effect: 1. Setting the ECME bit to 1 2. Setting SMSEL=0x111 with STI connected to ETIF (TRSEL=0x011)
[16]	ETIPOL	External Trigger Polarity 0: MTn_ETI active at high level or rising edge 1: MTn_ETI active at low level or falling edge.
[13:12]	ETIPSC	External Trigger Prescaler A prescaler can be enabled to reduce the ETIP frequency 00: Prescaler OFF 01: ETIP frequency divided by 2 10: ETIP frequency divided by 4 11: ETIP frequency divided by 8

Bits	Field	Descriptions
[11:8]	ETF	<p>External Trigger Filter</p> <p>These bits define the frequency divided ratio that is used to sample the MTn_ETI signal. The digital filter in the MCTM is an N-event counter where N means how many valid transitions are necessary to output a filtered signal.</p> <ul style="list-style-type: none"> 0000: No filter, the sampling clock is f_{DTS}. 0001: $f_{SAMPLING} = f_{CLKIN}$, $N = 2$ 0010: $f_{SAMPLING} = f_{CLKIN}$, $N = 4$ 0011: $f_{SAMPLING} = f_{CLKIN}$, $N = 8$ 0100: $f_{SAMPLING} = f_{DTS}/2$, $N = 6$ 0101: $f_{SAMPLING} = f_{DTS}/2$, $N = 8$ 0110: $f_{SAMPLING} = f_{DTS}/4$, $N = 6$ 0111: $f_{SAMPLING} = f_{DTS}/4$, $N = 8$ 1000: $f_{SAMPLING} = f_{DTS}/8$, $N = 6$ 1001: $f_{SAMPLING} = f_{DTS}/8$, $N = 8$ 1010: $f_{SAMPLING} = f_{DTS}/16$, $N = 5$ 1011: $f_{SAMPLING} = f_{DTS}/16$, $N = 6$ 1100: $f_{SAMPLING} = f_{DTS}/16$, $N = 8$ 1101: $f_{SAMPLING} = f_{DTS}/32$, $N = 5$ 1110: $f_{SAMPLING} = f_{DTS}/32$, $N = 6$ 1111: $f_{SAMPLING} = f_{DTS}/32$, $N = 8$
[3:0]	TRSEL	<p>Trigger Source Selection</p> <p>These bits are used to select the trigger input (STI) for counter synchronising.</p> <ul style="list-style-type: none"> 0000: Software Trigger by setting the UEV1G bit 0001: Channel 0 filtered input – TI0S0 0010: Channel 1 filtered input – TI1S1 0011: External Trigger input – ETIF 1000: Channel 0 Edge Detector – TI0BED 1001: Internal Timing Module Trigger 0 – ITI0 1010: Internal Timing Module Trigger 1 – ITI1 1011: Internal Timing Module Trigger 2 – ITI2 Others: Default 0 <p>Note: These bits must be updated only when they are not in use, i.e. the slave mode is disabled by setting the SMSEL field to 0x00.</p>

Table 40. MCTM Internal Trigger Connection

Slave Timing Module	ITI0	ITI1	ITI2
MCTM0	MCTM1	GPTM0	GPTM1
MCTM1	MCTM0	GPTM0	GPTM1

Timer Counter Register – CTR

This register specifies the timer enable bit (TME), CRR buffer enable bit (CRBE), Capture/compare control bit and Channel PDMA selection bit (CHCCDS).

Offset: 0x010

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24	
Type/Reset	Reserved								
	23	22	21	20	19	18	17	16	
Type/Reset	Reserved							CHCCDS	
	15	14	13	12	11	10	9	8	
Type/Reset	Reserved					COMUS	COMPRE		
	7	6	5	4	3	2	1	0	
Type/Reset	Reserved					CRBE	TME		

Bits	Field	Descriptions
[16]	CHCCDS	Channel Capture/Compare PDMA Selection 0: Channel PDMA request derived from the channel capture/compare event. 1: Channel PDMA request derived from the update event 1.
[9]	COMUS	Capture/Compare Control Update Selection 0: Updated by setting the UEV2G bit only 1: Updated by setting the UEV2G bit or when a STI signal rising edge occurs This bit is only available when the capture/compare preload function is enabled by setting the COMPRE bit to 1.
[8]	COMPRE	Capture/Compare Preloaded Enable Control 0: CHxE, CHxNE and CHxOM bits are not preloaded 1: CHxE, CHxNE and CHxOM bits are preloaded If this bit is set to 1, the corresponding capture/compare control bits including the CHxE, CHxNE and CHxOM bits will be updated when the update event 2 occurs.
[1]	CRBE	Counter-Reload register Buffer Enable 0: Counter reload register can be updated immediately 1: Counter reload register can not be updated until the update event occurs
[0]	TME	Timer Enable bit 0: MCTM off 1: MCTM on - MCTM functions normally When the TME bit is cleared to 0, the counter is stopped and the MCTM consumes no power in any operational mode except for the single pulse mode and the slave trigger mode. In these two modes the TME bit can automatically be set to 1 by hardware which permits all the MCTM registers to function normally.

Channel 0 Input Configuration Register – CH0ICFR

This register specifies the channel 0 input mode configuration.

Offset: 0x020

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Type/Reset	TI0SRC	Reserved						
	RW 0							
	23	22	21	20	19	18	17	16
Type/Reset	Reserved				CH0PSC		CH0CCS	
	15	14	13	12	11	10	9	8
Type/Reset	Reserved							
	7	6	5	4	3	2	1	0
Type/Reset	Reserved				TI0F			

Bits	Field	Descriptions
[31]	TI0SRC	Channel 0 Input Source TI0 Selection 0: The MTn_CH0 pin is connected to the channel 0 input TI0 1: The XOR operation output of the MTn_CH0, MTn_CH1, and MTn_CH2 pins are connected to the channel 0 input TI0
[19:18]	CH0PSC	Channel 0 Capture Input Source Prescaler Setting These bits define the effective events of the channel 0 capture input. Note that the prescaler is reset once the Channel 0 Capture/Compare Enable bit, CH0E, in the Channel Control register named CHCTR is cleared to 0. 00: No prescaler, channel 0 capture input signal is chosen for each active event 01: Channel 0 Capture input signal is chosen for every 2 events 10: Channel 0 Capture input signal is chosen for every 4 events 11: Channel 0 Capture input signal is chosen for every 8 events
[17:16]	CH0CCS	Channel 0 Capture/Compare Selection 00: Channel 0 is configured as an output 01: Channel 0 is configured as an input derived from the TI0 signal 10: Channel 0 is configured as an input derived from the TI1 signal 11: Channel 0 is configured as an input which comes from the TRCED signal derived from the Trigger Controller Note: The CH0CCS field can be accessed only when the CH0E bit is cleared to 0.

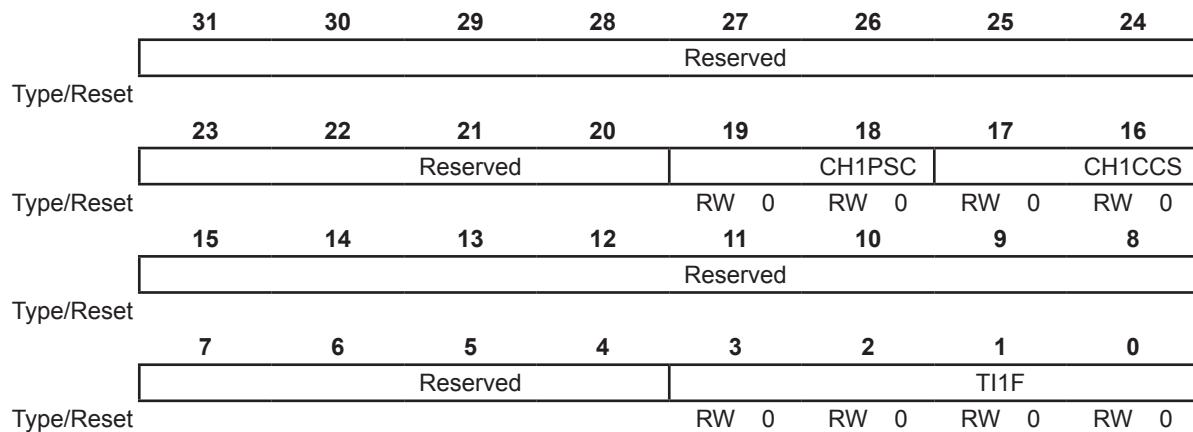
Bits	Field	Descriptions
[3:0]	TIOF	<p>Channel 0 Input Source TIO Filter Setting</p> <p>These bits define the frequency divided ratio used to sample the TIO signal. The Digital filter in the MCTM is an N-event counter where N is defined as how many valid transitions are necessary to output a filtered signal.</p> <ul style="list-style-type: none"> 0000: No filter, the sampling clock is f_{DTS}. 0001: $f_{SAMPLING} = f_{CLKIN}$, $N = 2$ 0010: $f_{SAMPLING} = f_{CLKIN}$, $N = 4$ 0011: $f_{SAMPLING} = f_{CLKIN}$, $N = 8$ 0100: $f_{SAMPLING} = f_{DTS}/2$, $N = 6$ 0101: $f_{SAMPLING} = f_{DTS}/2$, $N = 8$ 0110: $f_{SAMPLING} = f_{DTS}/4$, $N = 6$ 0111: $f_{SAMPLING} = f_{DTS}/4$, $N = 8$ 1000: $f_{SAMPLING} = f_{DTS}/8$, $N = 6$ 1001: $f_{SAMPLING} = f_{DTS}/8$, $N = 8$ 1010: $f_{SAMPLING} = f_{DTS}/16$, $N = 5$ 1011: $f_{SAMPLING} = f_{DTS}/16$, $N = 6$ 1100: $f_{SAMPLING} = f_{DTS}/16$, $N = 8$ 1101: $f_{SAMPLING} = f_{DTS}/32$, $N = 5$ 1110: $f_{SAMPLING} = f_{DTS}/32$, $N = 6$ 1111: $f_{SAMPLING} = f_{DTS}/32$, $N = 8$

Channel 1 Input Configuration Register – CH1ICFR

This register specifies the channel 1 input mode configuration.

Offset: 0x024

Reset value: 0x0000_0000



Bits	Field	Descriptions
[19:18]	CH1PSC	<p>Channel 1 Capture Input Source Prescaler Setting</p> <p>These bits define the effective events of the channel 1 capture input. Note that the prescaler is reset once the Channel 1 Capture/Compare Enable bit, CH1E, in the Channel Control register named CHCTR is cleared to 0.</p> <ul style="list-style-type: none"> 00: No prescaler, channel 1 capture input signal is chosen for each active event 01: Channel 1 Capture input signal is chosen for every 2 events 10: Channel 1 Capture input signal is chosen for every 4 events 11: Channel 1 Capture input signal is chosen for every 8 events
[17:16]	CH1CCS	<p>Channel 1 Capture/Compare Selection</p> <ul style="list-style-type: none"> 00: Channel 1 is configured as an output 01: Channel 1 is configured as an input derived from the TI1 signal 10: Channel 1 is configured as an input derived from the TI0 signal 11: Channel 1 is configured as an input which comes from the TRCED signal derived from the Trigger Controller <p>Note: The CH1CCS field can be accessed only when the CH1E bit is cleared to 0.</p>

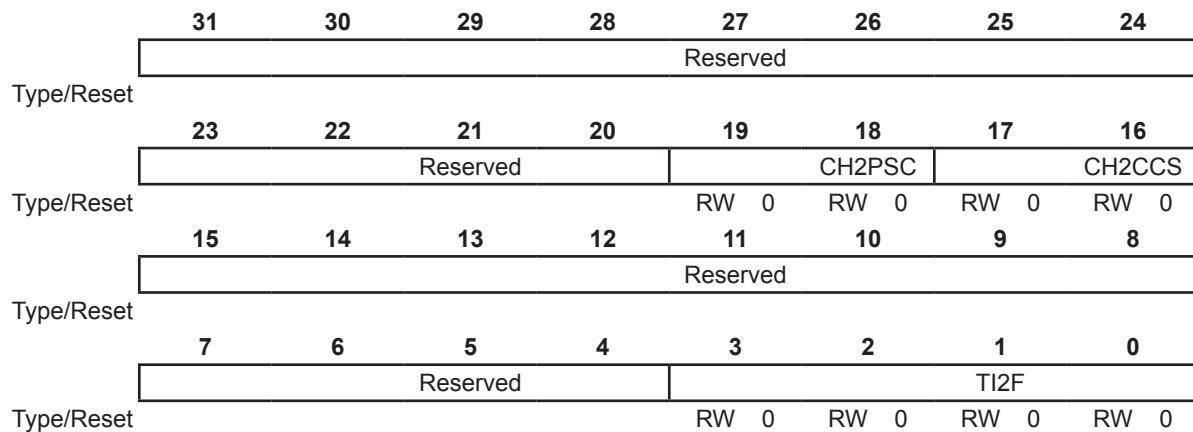
Bits	Field	Descriptions
[3:0]	TI1F	<p>Channel 1 Input Source TI1 Filter Setting</p> <p>These bits define the frequency divide ratio used to sample the TI1 signal. The Digital filter in the MCTM is an N-event counter where N is defined as how many valid transitions are necessary to output a filtered signal</p> <p>0000: No filter, the sampling clock is f_{DTS}.</p> <p>0001: $f_{SAMPLING} = f_{CLKIN}$, N = 2</p> <p>0010: $f_{SAMPLING} = f_{CLKIN}$, N = 4</p> <p>0011: $f_{SAMPLING} = f_{CLKIN}$, N = 8</p> <p>0100: $f_{SAMPLING} = f_{DTS}/2$, N = 6</p> <p>0101: $f_{SAMPLING} = f_{DTS}/2$, N = 8</p> <p>0110: $f_{SAMPLING} = f_{DTS}/4$, N = 6</p> <p>0111: $f_{SAMPLING} = f_{DTS}/4$, N = 8</p> <p>1000: $f_{SAMPLING} = f_{DTS}/8$, N = 6</p> <p>1001: $f_{SAMPLING} = f_{DTS}/8$, N = 8</p> <p>1010: $f_{SAMPLING} = f_{DTS}/16$, N = 5</p> <p>1011: $f_{SAMPLING} = f_{DTS}/16$, N = 6</p> <p>1100: $f_{SAMPLING} = f_{DTS}/16$, N = 8</p> <p>1101: $f_{SAMPLING} = f_{DTS}/32$, N = 5</p> <p>1110: $f_{SAMPLING} = f_{DTS}/32$, N = 6</p> <p>1111: $f_{SAMPLING} = f_{DTS}/32$, N = 8</p>

Channel 2 Input Configuration Register – CH2ICFR

This register specifies the channel 2 input mode configuration.

Offset: 0x028

Reset value: 0x0000_0000



Bits	Field	Descriptions
[19:18]	CH2PSC	<p>Channel 2 Capture Input Source Prescaler Setting</p> <p>These bits define the effective events of the channel 2 capture input. Note that the prescaler is reset once the Channel 2 Capture/Compare Enable bit, CH2E, in the Channel Control register named CHCTR is cleared to 0.</p> <ul style="list-style-type: none"> 00: No prescaler, channel 2 capture input signal is chosen for each active event 01: Channel 2 Capture input signal is chosen for every 2 events 10: Channel 2 Capture input signal is chosen for every 4 events 11: Channel 2 Capture input signal is chosen for every 8 events
[17:16]	CH2CCS	<p>Channel 2 Capture/Compare Selection</p> <ul style="list-style-type: none"> 00: Channel 2 is configured as an output 01: Channel 2 is configured as an input derived from the TI2 signal 10: Channel 2 is configured as an input derived from the TI3 signal 11: Channel 2 is configured as an input which comes from the TRCED signal derived from the Trigger Controller <p>Note: The CH2CCS field can be accessed only when the CH2E bit is cleared to 0.</p>

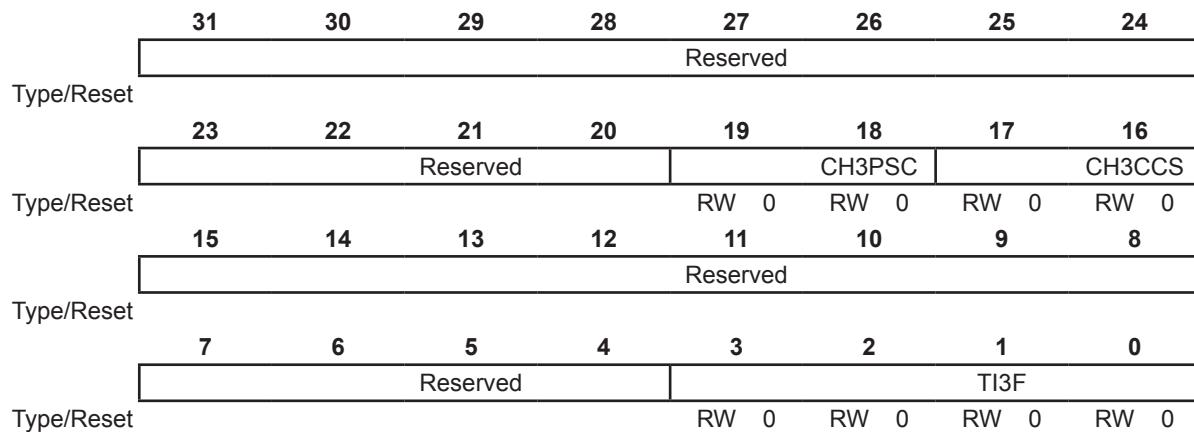
Bits	Field	Descriptions
[3:0]	TI2F	<p>Channel 2 Input Source TI2 Filter Setting</p> <p>These bits define the frequency divide ratio used to sample the TI2 signal. The Digital filter in the MCTM is an N-event counter where N is defined as how many valid transitions are necessary to output a filtered signal.</p> <ul style="list-style-type: none"> 0000: No filter, the sampling clock is f_{DTS}. 0001: $f_{SAMPLING} = f_{CLKIN}$, $N = 2$ 0010: $f_{SAMPLING} = f_{CLKIN}$, $N = 4$ 0011: $f_{SAMPLING} = f_{CLKIN}$, $N = 8$ 0100: $f_{SAMPLING} = f_{DTS} / 2$, $N = 6$ 0101: $f_{SAMPLING} = f_{DTS} / 2$, $N = 8$ 0110: $f_{SAMPLING} = f_{DTS} / 4$, $N = 6$ 0111: $f_{SAMPLING} = f_{DTS} / 4$, $N = 8$ 1000: $f_{SAMPLING} = f_{DTS} / 8$, $N = 6$ 1001: $f_{SAMPLING} = f_{DTS} / 8$, $N = 8$ 1010: $f_{SAMPLING} = f_{DTS} / 16$, $N = 5$ 1011: $f_{SAMPLING} = f_{DTS} / 16$, $N = 6$ 1100: $f_{SAMPLING} = f_{DTS} / 16$, $N = 8$ 1101: $f_{SAMPLING} = f_{DTS} / 32$, $N = 5$ 1110: $f_{SAMPLING} = f_{DTS} / 32$, $N = 6$ 1111: $f_{SAMPLING} = f_{DTS} / 32$, $N = 8$

Channel 3 Input Configuration Register – CH3ICFR

This register specifies the channel 3 input mode configuration.

Offset: 0x02C

Reset value: 0x0000_0000



Bits	Field	Descriptions
[19:18]	CH3PSC	<p>Channel 3 Capture Input Source Prescaler Setting</p> <p>These bits define the effective events of the channel 3 capture input. Note that the prescaler is reset once the Channel 3 Capture/Compare Enable bit, CH3E, in the Channel Control register named CHCTR is cleared to 0.</p> <ul style="list-style-type: none"> 00: No prescaler, channel 3 capture input signal is chosen for each active event 01: Channel 3 Capture input signal is chosen for every 2 events 10: Channel 3 Capture input signal is chosen for every 4 events 11: Channel 3 Capture input signal is chosen for every 8 events
[17:16]	CH3CCS	<p>Channel 3 Capture/Compare Selection</p> <ul style="list-style-type: none"> 00: Channel 3 is configured as an output 01: Channel 3 is configured as an input derived from the TI3 signal 10: Channel 3 is configured as an input derived from the TI2 signal 11: Channel 3 is configured as an input which comes from the TRCED signal derived from the Trigger Controller <p>Note: The CH3CCS field can be accessed only when the CH3E bit is cleared to 0.</p>

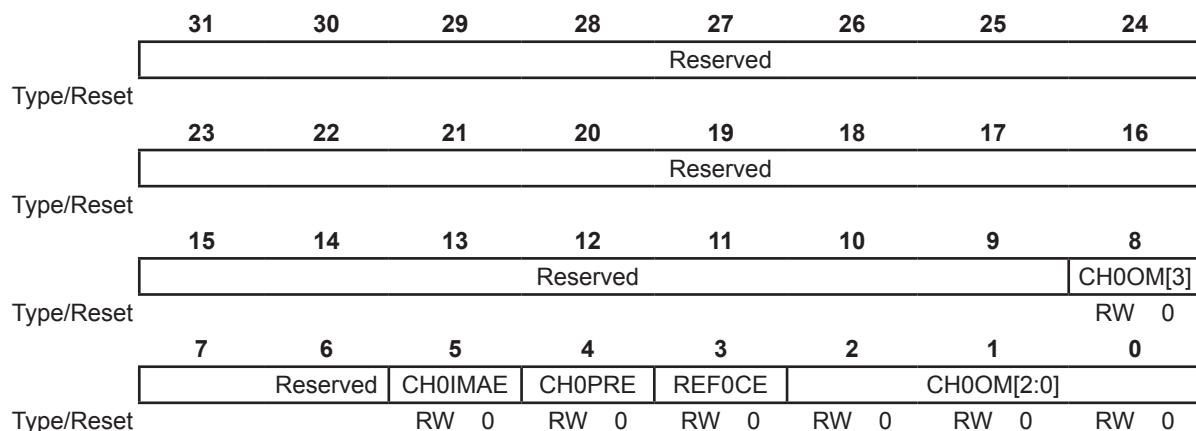
Bits	Field	Descriptions
[3:0]	TI3F	<p>Channel 3 Input Source TI3 Filter Setting</p> <p>These bits define the frequency divide ratio used to sample the TI3 signal. The digital filter in the GPTM is an N-event counter where N is defined as how many valid transitions are necessary to output a filtered signal</p> <ul style="list-style-type: none"> 0000: No filter, the sampling clock is f_{DTS}. 0001: $f_{SAMPLING} = f_{CLKIN}$, $N = 2$ 0010: $f_{SAMPLING} = f_{CLKIN}$, $N = 4$ 0011: $f_{SAMPLING} = f_{CLKIN}$, $N = 8$ 0100: $f_{SAMPLING} = f_{DTS} / 2$, $N = 6$ 0101: $f_{SAMPLING} = f_{DTS} / 2$, $N = 8$ 0110: $f_{SAMPLING} = f_{DTS} / 4$, $N = 6$ 0111: $f_{SAMPLING} = f_{DTS} / 4$, $N = 8$ 1000: $f_{SAMPLING} = f_{DTS} / 8$, $N = 6$ 1001: $f_{SAMPLING} = f_{DTS} / 8$, $N = 8$ 1010: $f_{SAMPLING} = f_{DTS} / 16$, $N = 5$ 1011: $f_{SAMPLING} = f_{DTS} / 16$, $N = 6$ 1100: $f_{SAMPLING} = f_{DTS} / 16$, $N = 8$ 1101: $f_{SAMPLING} = f_{DTS} / 32$, $N = 5$ 1110: $f_{SAMPLING} = f_{DTS} / 32$, $N = 6$ 1111: $f_{SAMPLING} = f_{DTS} / 32$, $N = 8$

Channel 0 Output Configuration Register – CH0OCFR

This register specifies the channel 0 output mode configuration.

Offset: 0x040

Reset value: 0x0000_0000



Bits	Field	Descriptions
[5]	CH0IMAE	<p>Channel 0 Immediate Active Enable</p> <p>0: No action 1: Single pulse Immediate Active Mode is enabled</p> <p>CH0OREF will be forced to the compare matched level immediately after an available trigger event occurs irrespective of the result of the comparison between the CNTR and the CH0CCR values.</p> <p>The effective duration ends automatically at the next overflow or underflow event.</p> <p>Note: The CH0IMAE bit is available only if channel 0 is configured operate in PWM mode 1 or PWM mode 2.</p>
[4]	CH0PRE	<p>Channel 0 Capture/Compare Register (CH0CCR) Preload Enable</p> <p>0: CH0CCR preload function is disabled The CH0CCR register can be immediately assigned a new value when the CH0PRE bit is cleared to 0 and the updated CH0CCR value is used immediately.</p> <p>1: CH0CCR preload function is enabled The new CH0CCR value will not be transferred to its shadow register until an update event 1 occurs.</p>
[3]	REF0CE	<p>Channel 0 Reference Output Clear Enable</p> <p>0: CH0OREF operates normally and is not affected by the ETIF signal 1: CH0OREF is forced to 0 on the high level of the ETIF signal derived from the MTn_ETI pin</p>

Bits	Field	Descriptions
[8][2:0]	CH0OM[3:0]	<p>Channel 0 Output Mode Setting</p> <p>These bits define the functional types of the output reference signal CH0OREF.</p> <ul style="list-style-type: none"> 0000: No Change 0001: Output 0 on compare match 0010: Output 1 on compare match 0011: Output toggles on compare match 0100: Force inactive – CH0OREF is forced to 0 0101: Force active – CH0OREF is forced to 1 0110: PWM mode 1 <ul style="list-style-type: none"> - During up-counting, channel 0 has an active level when CNTR < CH0CCR or otherwise has an inactive level. - During down-counting, channel 0 has an inactive level when CNTR > CH0CCR or otherwise has an active level. 0111: PWM mode 2 <ul style="list-style-type: none"> - During up-counting, channel 0 has an inactive level when CNTR < CH0CCR or otherwise has an active level. - During down-counting, channel 0 has an active level when CNTR > CH0CCR or otherwise has an inactive level. 1110: Asymmetric PWM mode 1 <ul style="list-style-type: none"> - During up-counting, channel 0 has an active level when CNTR < CH0CCR or otherwise has an inactive level. - During down-counting, channel 0 has an inactive level when CNTR > CH0ACR or otherwise has an active level. 1111: Asymmetric PWM mode 2 <ul style="list-style-type: none"> - During up-counting, channel 0 has an inactive level when CNTR < CH0CCR or otherwise has an active level. - During down-counting, channel 0 has an active level when CNTR > CH0ACR or otherwise has an inactive level

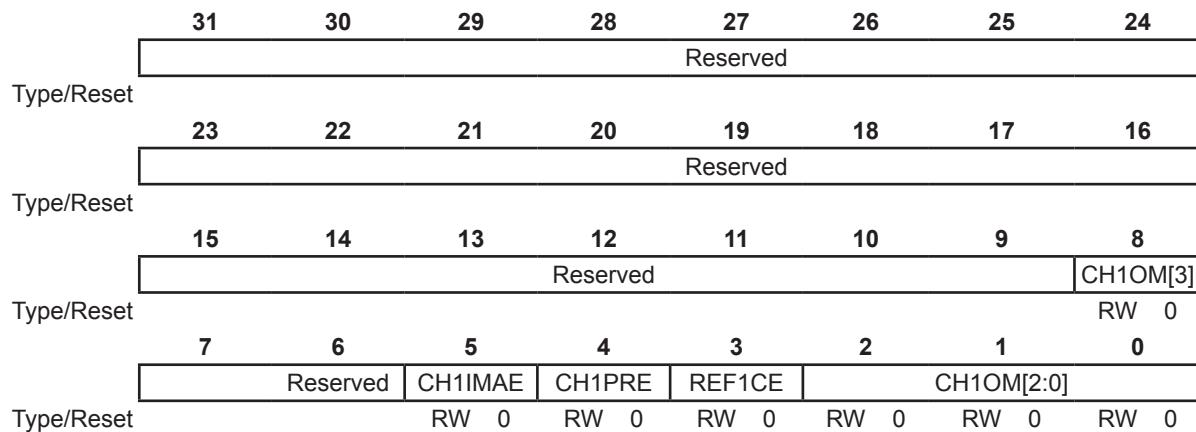
Note: When channel 0 is used as asymmetric PWM output mode, the Counter Mode Selection bit in Counter Configuration Register must be configured as Center-aligned Counting mode (CMSEL = 01/02/03).

Channel 1 Output Configuration Register – CH1OCFR

This register specifies the channel 1 output mode configuration.

Offset: 0x044

Reset value: 0x0000_0000



Bits	Field	Descriptions
[5]	CH1IMAE	<p>Channel 1 Immediate Active Enable</p> <p>0: No action</p> <p>1: Single pulse Immediate Active Mode enabled</p> <p>The CH1OREF will be forced to the compare matched level immediately after an available trigger event occurs irrespective of the result of the comparison between the CNTR and the CH1CCR values.</p> <p>The effective duration ends automatically at the next overflow or underflow event.</p> <p>Note: The CH1IMAE bit is available only if channel 1 is configured to be operated in PWM mode 1 or PWM mode 2.</p>
[4]	CH1PRE	<p>Channel 1 Capture/Compare Register (CH1CCR) Preload Enable</p> <p>0: CH1CCR preload function is disabled.</p> <p>The CH1CCR register can be immediately assigned a new value when the CH1PRE bit is cleared to 0 and the updated CH1CCR value is used immediately.</p> <p>1: CH1CCR preload function is enabled</p> <p>The new CH1CCR value will not be transferred to its shadow register until an update event 1 occurs.</p>
[3]	REF1CE	<p>Channel 1 Reference Output Clear Enable</p> <p>0: CH1OREF performed normally and is not affected by the ETIF signal</p> <p>1: CH1OREF is forced to 0 on the high level of the ETIF signal derived from the MTn_ETI pin.</p>

Bits	Field	Descriptions
[8][2:0]	CH1OM[3:0]	<p>Channel 1 Output Mode Setting</p> <p>These bits define the functional types of the output reference signal CH1OREF.</p> <ul style="list-style-type: none"> 0000: No Change 0001: Output 0 on compare match 0010: Output 1 on compare match 0011: Output toggles on compare match 0100: Force inactive – CH1OREF is forced to 0 0101: Force active – CH1OREF is forced to 1 0110: PWM mode 1 <ul style="list-style-type: none"> - During up-counting, channel 1 has an active level when CNTR < CH1CCR or otherwise has an inactive level. - During down-counting, channel 1 has an inactive level when CNTR > CH1CCR or otherwise has an active level. 0111: PWM mode 2 <ul style="list-style-type: none"> - During up-counting, channel 1 has an inactive level when CNTR < CH1CCR or otherwise has an active level. - During down-counting, channel 1 has an active level when CNTR > CH1CCR or otherwise has an inactive level. 1110: Asymmetric PWM mode 1 <ul style="list-style-type: none"> - During up-counting, channel 1 has an active level when CNTR < CH1CCR or otherwise has an inactive level. - During down-counting, channel 1 has an inactive level when CNTR > CH1ACR or otherwise has an active level. 1111: Asymmetric PWM mode 2 <ul style="list-style-type: none"> - During up-counting, channel 1 has an inactive level when CNTR < CH1CCR or otherwise has an active level. - During down-counting, channel 1 has an active level when CNTR > CH1ACR or otherwise has an inactive level

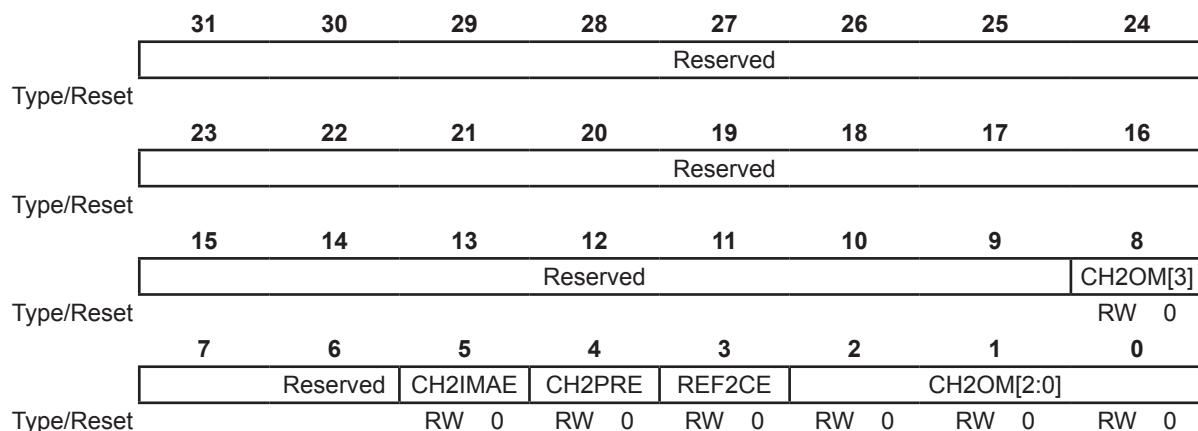
Note: When channel 1 is used as asymmetric PWM output mode, the Counter Mode Selection bit in Counter Configuration Register must be configured as Center-aligned Counting mode (CMSEL = 01/02/03).

Channel 2 Output Configuration Register – CH2OCFR

This register specifies the channel 2 output mode configuration.

Offset: 0x048

Reset value: 0x0000_0000



Bits	Field	Descriptions
[5]	CH2IMAE	<p>Channel 2 Immediate Active Enable</p> <p>0: No action</p> <p>1: Single pulse Immediate Active Mode enabled</p> <p>The CH2OREF will be forced to the compare matched level immediately after an available trigger event occurs irrespective of the result of the comparison between the CNTR and the CH2CCR values.</p> <p>The effective duration ends automatically at the next overflow or underflow event.</p> <p>Note: The CH2IMAE bit is available only if the channel 2 is configured to be operated in PWM mode 1 or PWM mode 2.</p>
[4]	CH2PRE	<p>Channel 2 Capture/Compare Register (CH2CCR) Preload Enable</p> <p>0: CH2CCR preload function is disabled.</p> <p>The CH2CCR register can be immediately assigned a new value when the CH2PRE bit is cleared to 0 and the updated CH2CCR value is used immediately.</p> <p>1: CH2CCR preload function is enabled</p> <p>The new CH2CCR value will not be transferred to its shadow register until an update event 1 occurs.</p>
[3]	CH3OCCE	<p>Channel 2 Reference Output Clear Enable</p> <p>0: CH2OREF operates normally and is not affected by the ETIF signal</p> <p>1: CH2OREF is forced to 0 during a high level of the ETIF signal derived from the MTn_ETI pin</p>

Bits	Field	Descriptions
[8][2:0]	CH2OM[3:0]	<p>Channel 2 Output Mode Setting</p> <p>These bits define the functional types of the output reference signal CH2OREF.</p> <ul style="list-style-type: none"> 0000: No Change 0001: Output 0 on compare match 0010: Output 1 on compare match 0011: Output toggles on compare match 0100: Force inactive – CH2OREF is forced to 0 0101: Force active – CH2OREF is forced to 1 0110: PWM mode 1 <ul style="list-style-type: none"> - During up-counting, channel 2 has an active level when CNTR < CH2CCR or otherwise has an inactive level. - During down-counting, channel 2 has an inactive level when CNTR > CH2CCR or otherwise has an active level. 0111: PWM mode 2 <ul style="list-style-type: none"> - During up-counting, channel 2 has an inactive level when CNTR < CH2CCR or otherwise has an active level. - During down-counting, channel 2 has an active level when CNTR > CH2CCR or otherwise has an inactive level. 1110: Asymmetric PWM mode 1 <ul style="list-style-type: none"> - During up-counting, channel 2 has an active level when CNTR < CH2CCR or otherwise has an inactive level. - During down-counting, channel 2 has an inactive level when CNTR > CH2ACR or otherwise has an active level. 1111: Asymmetric PWM mode 2 <ul style="list-style-type: none"> - During up-counting, channel 2 has an inactive level when CNTR < CH2CCR or otherwise has an active level. - During down-counting, channel 2 has an active level when CNTR > CH2ACR or otherwise has an inactive level

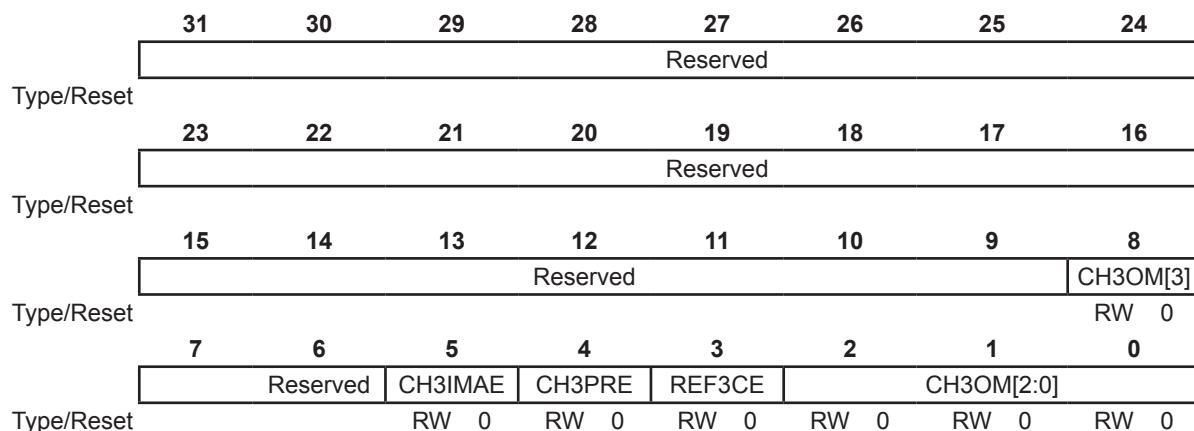
Note: When channel 2 is used as asymmetric PWM output mode, the Counter Mode Selection bit in Counter Configuration Register must be configured as Center-aligned Counting mode (CMSEL = 01/02/03).

Channel 3 Output Configuration Register – CH3OCFR

This register specifies the channel 3 output mode configuration.

Offset: 0x04C

Reset value: 0x0000_0000



Bits	Field	Descriptions
[5]	CH3IMAE	<p>Channel 3 Immediate Active Enable</p> <p>0: No action</p> <p>1: Single pulse Immediate Active Mode enabled</p> <p>The CH3OREF will be forced to the compare matched level immediately after an available trigger event occurs irrespective of the result of the comparison between the CNTR and the CH3CCR values.</p> <p>The effective duration ends automatically at the next overflow or underflow event.</p> <p>Note: The CH3IMAE bit is available only if channel 3 is configured to be operated in PWM mode 1 or PWM mode 2.</p>
[4]	CH3PRE	<p>Channel 3 Capture/Compare Register (CH3CCR) Preload Enable</p> <p>0: CH3CCR preload function is disabled.</p> <p>The CH3CCR register can be immediately assigned a new value when the CH3PRE bit is cleared to 0 and the updated CH3CCR value is used immediately.</p> <p>1: CH3CCR preload function is enabled</p> <p>The new CH3CCR value will not be transferred to its shadow register until an update event 1 occurs.</p>
[3]	REF3CE	<p>Channel 3 Reference Output Clear Enable</p> <p>0: CH3OREF operates normally and is not affected by the ETIF signal</p> <p>1: CH3OREF is forced to 0 during the high level of the ETIF signal derived from the MTn_ETI pin</p>

Bits	Field	Descriptions
[8][2:0]	CH3OM[3:0]	<p>Channel 3 Output Mode Setting</p> <p>These bits define the functional types of the output reference signal CH3OREF</p> <ul style="list-style-type: none"> 0000: No Change 0001: Output 0 on compare match 0010: Output 1 on compare match 0011: Output toggles on compare match 0100: Force inactive – CH3OREF is forced to 0 0101: Force active – CH3OREF is forced to 1 0110: PWM mode 1 <ul style="list-style-type: none"> - During up-counting, channel 3 has an active level when CNTR < CH3CCR or otherwise has an inactive level. - During down-counting, channel 3 has an inactive level when CNTR > CH3CCR or otherwise has an active level. 0111: PWM mode 2 <ul style="list-style-type: none"> - During up-counting, channel 3 has an inactive level when CNTR < CH3CCR or otherwise has an active level. - During down-counting, channel 3 has an active level when CNTR > CH3CCR or otherwise has an inactive level 1110: Asymmetric PWM mode 1 <ul style="list-style-type: none"> - During up-counting, channel 3 has an active level when CNTR < CH3CCR or otherwise has an inactive level. - During down-counting, channel 3 has an inactive level when CNTR > CH3ACR or otherwise has an active level. 1111: Asymmetric PWM mode 2 <ul style="list-style-type: none"> - During up-counting, channel 3 has an inactive level when CNTR < CH3CCR or otherwise has an active level. - During down-counting, channel 3 has an active level when CNTR > CH3ACR or otherwise has an inactive level

Note: When channel 3 is used as asymmetric PWM output mode, the Counter Mode Selection bit in Counter Configuration Register must be configured as Center-aligned Counting mode (CMSEL = 01/02/03).

Channel Control Register – CHCTR

This register contains the channel capture input or compare output function enable control bits.

Offset: 0x050

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24	
Type/Reset	Reserved								
	23	22	21	20	19	18	17	16	
Type/Reset	Reserved								
	15	14	13	12	11	10	9	8	
Type/Reset	Reserved								
	7	6	5	4	3	2	1	0	
Type/Reset	Reserved	RW	0	RW	0	RW	0	RW	0
	CH3E	CH2NE	CH2E	CH1NE	CH1E	CH0NE	CH0E		

Bits	Field	Descriptions
[6]	CH3E	<p>Channel 3 Capture/Compare Enable</p> <ul style="list-style-type: none"> - Channel 3 is configured as an input (CH3CCS = 0x01/0x02/0x03) <ul style="list-style-type: none"> 0: Input Capture Mode disabled 1: Input Capture Mode enabled - Channel 3 is configured as an output (CH3CCS = 0x00) <ul style="list-style-type: none"> 0: Off – Channel 3 output signal CH3O is not active 1: On – Channel 3 output signal CH3O is generated on the corresponding output pin depending on the condition of the CHMOE, CHOSSI, CHOSSR and CH3OIS bits.
[5]	CH2NE	<p>Channel 2 Capture/Compare Complementary Enable</p> <ul style="list-style-type: none"> 0: Off – Channel 2 complementary output CH2NO is not active. The CH2NO level is then determined by the CHMOE, CHOSSI, CHOSSR, CH2OIS, CH2OISN and CH2E bits. 1: On – Channel 2 complementary output CH2NO is generated on the corresponding output pin depending on the condition of the CHMOE, CHOSSI, CHOSSR, CH2OIS, CH2OISN and CH2E bits.
[4]	CH2E	<p>Channel 2 Capture/Compare Enable</p> <ul style="list-style-type: none"> - Channel 2 is configured as an input (CH2CCS = 0x01/0x02/0x03) <ul style="list-style-type: none"> 0: Input Capture Mode disabled 1: Input Capture Mode enabled - Channel 2 is configured as an output (CH2CCS = 0x00) <ul style="list-style-type: none"> 0: Off – Channel 2 output signal CH2O is not active. The CH2O level is then determined by the condition of the CHMOE, CHOSSI, CHOSSR, CH2OIS, CH2OISN and CH2NE bits. 1: On – Channel 2 output signal CH2O is generated on the corresponding output pin determined by the condition of the CHMOE, CHOSSI, CHOSSR, CH2OIS, CH2OISN and CH2NE bits.

Bits	Field	Descriptions
[3]	CH1NE	<p>Channel 1 Capture/Compare Complementary Enable</p> <p>0: Off – Channel 1 complementary output CH1NO is not active. The CH1NO level is then determined by the condition of the CHMOE, CHOSSI, CHOSSR, CH1OIS, CH1OISN and CH1E bits.</p> <p>1: On – Channel 1 complementary output CH1NO is generated on the corresponding output pin determined by the condition of the CHMOE, CHOSSI, CHOSSR, CH1OIS, CH1OISN and CH1E bits.</p>
[2]	CH1E	<p>Channel 1 Capture/Compare Enable</p> <ul style="list-style-type: none"> - Channel 1 is configured as an input (CH1CCS = 0x01/0x02/0x03) <ul style="list-style-type: none"> 0: Input Capture Mode disabled 1: Input Capture Mode enabled - Channel 1 is configured as an output (CH1CCS = 0x00) <ul style="list-style-type: none"> 0: Off – Channel 1 output signal CH1O is not active. The CH1O level is then determined by the condition of the CHMOE, CHOSSI, CHOSSR, CH1OIS, CH1OISN and CH1NE bits. 1: On – Channel 1 output signal CH1O is generated on the corresponding output pin depending on the condition of the CHMOE, CHOSSI, CHOSSR, CH1OIS, CH1OISN and CH1NE bits.
[1]	CH0NE	<p>Channel 0 Capture/Compare Complementary Enable</p> <p>0: Off – Channel 0 complementary output CH0NO is not active. The CH0NO level is then determined by the condition of the CHMOE, CHOSSI, CHOSSR, CH0OIS, CH0OISN and CH0E bits.</p> <p>1: On – Channel 0 complementary output CH0NO is generated on the corresponding output pin depending on the condition of the CHMOE, CHOSSI, CHOSSR, CH0OIS, CH0OISN and CH0E bits.</p>
[0]	CH0E	<p>Channel 0 Capture/Compare Enable</p> <ul style="list-style-type: none"> - Channel 0 is configured as an input (CH0CCS = 0x01/0x02/0x03) <ul style="list-style-type: none"> 0: Input Capture Mode disabled 1: Input Capture Mode enabled - Channel 0 is configured as an output (CH0CCS = 0x00) <ul style="list-style-type: none"> 0: Off – Channel 0 output signal CH0O is not active. The CH0O level is then determined by the condition of the CHMOE, CHOSSI, CHOSSR, CH0OIS, CH0OISN and CH0NE bits. 1: On – Channel 0 output signal CH0O is generated on the corresponding output pin determined by the condition of the CHMOE, CHOSSI, CHOSSR, CH0OIS, CH0OISN and CH0NE bits.

Channel Polarity Configuration Register – CHPOLR

This register contains the channel capture input or compare output polarity control.

Offset: 0x054

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24	
Type/Reset	Reserved								
	23	22	21	20	19	18	17	16	
Type/Reset	Reserved								
	15	14	13	12	11	10	9	8	
Type/Reset	Reserved								
	7	6	5	4	3	2	1	0	
Type/Reset	Reserved	RW	0	RW	0	RW	0	RW	0
	CH3P	CH2NP	CH2P	CH1NP	CH1P	CH0NP	CH0P		

Bits	Field	Descriptions
[6]	CH3P	Channel 3 Capture/Compare Polarity - When Channel 3 is configured as an input 0: capture event occurs on a Channel 3 rising edge 1: capture event occurs on a Channel 3 falling edge - When Channel 3 is configured as an output (CH3CCS = 0x00) 0: Channel 3 Output active high 1: Channel 3 Output active low
[5]	CH2NP	Channel 2 Capture/Compare Complementary Polarity 0: Channel 2 Output active high. 1: Channel 2 Output active low
[4]	CH2P	Channel 2 Capture/Compare Polarity - When Channel 2 is configured as an input 0: capture event occurs on a Channel 2 rising edge 1: capture event occurs on a Channel 2 falling edge - When Channel 2 is configured as an output (CH2CCS = 0x00) 0: Channel 2 Output active high 1: Channel 2 Output active low
[3]	CH1NP	Channel 1 Capture/Compare Complementary Polarity 0: Channel 1 Output active high. 1: Channel 1 Output active low.
[2]	CH1P	Channel 1 Capture/Compare Polarity - When Channel 1 is configured as an input 0: capture event occurs on a Channel 1 rising edge 1: capture event occurs on a Channel 1 falling edge - Channel 1 is configured as an output (CH1CCS = 0x00) 0: Channel 1 Output active high 1: Channel 1 Output active low
[1]	CH0NP	Channel 0 Capture/Compare Complementary Polarity 0: Channel 0 Output active high. 1: Channel 0 Output active low.

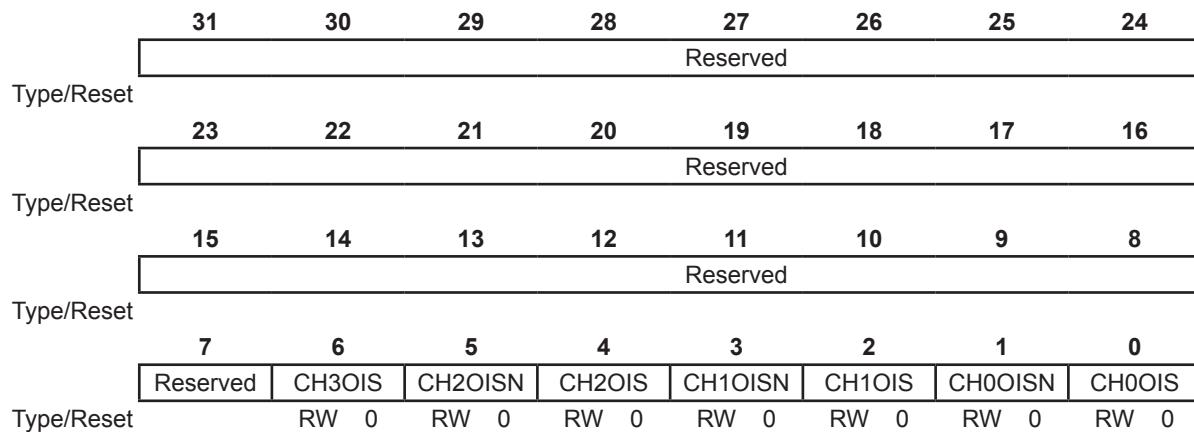
Bits	Field	Descriptions
[0]	CH0P	Channel 0 Capture/Compare Polarity - When Channel 0 is configured as an input 0: capture event occurs on a Channel 0 rising edge 1: capture event occurs on a Channel 0 falling edge - When Channel 0 is configured as an output (CH0CCS = 0x00) 0: Channel 0 Output active high 1: Channel 0 Output active low

Channel Break Configuration Register – CHBRKCFR

This register specifies the channel output idle state when using the break function.

Offset: 0x06C

Reset value: 0x0000_0000



Bits	Field	Descriptions
[6]	CH3OIS	MTx_CH3O Output Idle State 0: Channel 3 output CH3O = 0 when CHMOE = 0. 1: Channel 3 output CH3O = 1 when CHMOE = 0.
[5]	CH2OISN	MTx_CH2NO Output Idle State 0: Channel 2 complementary output CH2NO = 0 after a dead time when CHMOE=0 1: Channel 2 complementary output CH2NO = 1 after a dead time when CHMOE=0
[4]	CH2OIS	MTx_CH2O Output Idle State 0: Channel 2 output CH2O = 0 after a dead time when CHMOE = 0. 1: Channel 2 output CH2O = 1 after a dead time when CHMOE = 0.
[3]	CH1OISN	MTx_CH1NO Output Idle State 0: Channel 1 complementary output CH1NO = 0 after a dead time when CHMOE=0 1: Channel 1 complementary output CH1NO = 1 after a dead time when CHMOE=0
[2]	CH1OIS	MTx_CH1O Output Idle State 0: Channel 1 output CH1O = 0 after a dead time when CHMOE = 0. 1: Channel 1 output CH1O = 1 after a dead time when CHMOE = 0.
[1]	CH0OISN	MTx_CH0NO Output Idle State 0: Channel 0 complementary output CH1NO = 0 after a dead time when CHMOE=0 1: Channel 0 complementary output CH1NO = 1 after a dead time when CHMOE=0
[0]	CH0OIS	MTx_CH0O Output Idle State 0: Channel 0 output CH0O = 0 after a dead time when CHMOE = 0. 1: Channel 0 output CH0O = 1 after a dead time when CHMOE = 0.

Channel Break Control Register – CHBRKCTR

This register specifies the channel break control bits.

Offset: 0x070

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
CHDTG								
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
Reserved CHOSSR CHOSSI GFSEL1 GFSEL0 LOCKLV								
Type/Reset		RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
BKF1 BKF0								
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
Type/Reset	Reserved	BK1SEL	CHAOE	CHMOE	BKP1	BKE1	BKPO	BKE0
	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:24]	CHDTG	Channel Dead Time Duration Definition CHDTG[7:5]=0xx: Channel Dead Time = CHDTG [7:0]×t _{dtg} , with t _{dtg} = t _{DTS} CHDTG[7:5]=10x: Channel Dead Time = (64+CHDTG [5:0])×t _{dtg} , with t _{dtg} = 2×t _{DTS} CHDTG[7:5]=110: Channel Dead Time = (32+CHDTG [4:0])×t _{dtg} , with t _{dtg} = 8×t _{DTS} CHDTG[7:5]=111: Channel Dead Time = (32+CHDTG [4:0])×t _{dtg} , with t _{dtg} = 16×t _{DTS}
[21]	CHOSSR	Channel Off State (CHxE, CHxNE=0) Selection for Normal Run State (CHMOE = 1) 0: When inactive, MTn_CHxO/MTn_CHxNO output disable - not driven by timer 1: When inactive, MTn_CHxO/MTn_CHxNO output enabled with their inactive level
[20]	CHOSSI	Channel Off State Selection for Idle Mode (CHMOE = 0) 0: When inactive, MTn_CHxO/MTn_CHxNO output disable - not driven by timer 1: When inactive, MTn_CHxO/MTn_CHxNO output enabled with their idle level depending upon the condition of the the CHxOIS and CHxOISN bits.
[19]	GFSEL1	Deglitch Filter Selction for Break 1 0: no input deglitch filter 1: 50ns deglitch filter
[18]	GFSEL0	Deglitch Filter Selction for Break 0 0: no input deglitch filter 1: 50ns deglitch filter
[17:16]	LOCKLV	Lock Level Setting These bits offer write protection against software errors. The bits can be written only once after a reset. 00: LOCK OFF. Register write protected function disabled. 01: LOCK Level 1 10: LOCK Level 2 11: LOCK Level 3

Bits	Field	Descriptions
[15:12]	BKF1	<p>Break 1 Input Filter Setting</p> <p>These bits define the frequency ratio used to sample the MT_BRK1 signal. The digital filter in the MCTM is an N-event counter where N is defined as how many valid transitions are necessary to output a filtered signal.</p> <ul style="list-style-type: none"> 0000: No filter – don't need sample clock. 0001: $f_{SAMPLING} = f_{CLKIN}$, N = 2. 0010: $f_{SAMPLING} = f_{CLKIN}$, N = 4. 0011: $f_{SAMPLING} = f_{CLKIN}$, N = 8. 0100: $f_{SAMPLING} = f_{DTS}/2$, N = 6. 0101: $f_{SAMPLING} = f_{DTS}/2$, N = 8. 0110: $f_{SAMPLING} = f_{DTS}/4$, N = 6. 0111: $f_{SAMPLING} = f_{DTS}/4$, N = 8. 1000: $f_{SAMPLING} = f_{DTS}/8$, N = 6. 1001: $f_{SAMPLING} = f_{DTS}/8$, N = 8. 1010: $f_{SAMPLING} = f_{DTS}/16$, N = 5. 1011: $f_{SAMPLING} = f_{DTS}/16$, N = 6. 1100: $f_{SAMPLING} = f_{DTS}/16$, N = 8. 1101: $f_{SAMPLING} = f_{DTS}/32$, N = 5. 1110: $f_{SAMPLING} = f_{DTS}/32$, N = 6. 1111: $f_{SAMPLING} = f_{DTS}/32$, N = 8.
[11:8]	BKF0	<p>Break 0 Input Filter Setting</p> <p>These bits define the frequency ratio used to sample the MT_BRK0 signal. The digital filter in the MCTM is an N-event counter where N is defined as how many valid transitions are necessary to output a filtered signal.</p> <ul style="list-style-type: none"> 0000: No filter – don't need sample clock. 0001: $f_{SAMPLING} = f_{CLKIN}$, N = 2. 0010: $f_{SAMPLING} = f_{CLKIN}$, N = 4. 0011: $f_{SAMPLING} = f_{CLKIN}$, N = 8. 0100: $f_{SAMPLING} = f_{DTS}/2$, N = 6. 0101: $f_{SAMPLING} = f_{DTS}/2$, N = 8. 0110: $f_{SAMPLING} = f_{DTS}/4$, N = 6. 0111: $f_{SAMPLING} = f_{DTS}/4$, N = 8. 1000: $f_{SAMPLING} = f_{DTS}/8$, N = 6. 1001: $f_{SAMPLING} = f_{DTS}/8$, N = 8. 1010: $f_{SAMPLING} = f_{DTS}/16$, N = 5. 1011: $f_{SAMPLING} = f_{DTS}/16$, N = 6. 1100: $f_{SAMPLING} = f_{DTS}/16$, N = 8. 1101: $f_{SAMPLING} = f_{DTS}/32$, N = 5. 1110: $f_{SAMPLING} = f_{DTS}/32$, N = 6. 1111: $f_{SAMPLING} = f_{DTS}/32$, N = 8.
[6]	BK1SEL	<p>Break 1 Selection</p> <ul style="list-style-type: none"> 0: ETI signal is selected for the MT_ETI pin. 1: MT_BRK1 signal is selected for the MT_ETI pin. <p>Note: The Break 1 and ETI signal are share with the same MT_ETI pin. This control bit can switch the pin function for the second break signal of the MCTM.</p>

Bits	Field	Descriptions
[5]	CHAOE	Channel Automatic Output Enable 0: CHMOE can be set only by software. 1: CHMOE can be set by software or automatically by an update event
[4]	CHMOE	Channel Main Output Enable Cleared asynchronously by hardware on a break event occurrence. 0: MTn_CHxO and MTn_CHxNO are disabled or forced to an idle states. 1: MTn_CHxO and MTn_CHxNO are enabled if the enable bits (CHxE, CHxNE) are set.
[3]	BKP1	Break 1 Input Polarity. 0: Break input active low. 1: Break input active high
[2]	BKE1	Break 1 Enable 0: Break inputs disabled 1: Break inputs enabled
[1]	BKP0	Break 0 Input Polarity. 0: Break input active low. 1: Break input active high
[0]	BKE0	Break 0 Enable 0: Break inputs disabled 1: Break inputs enabled

Timer PDMA/Interrupt Control Register – DICTR

This register contains the timer PDAM and interrupt enable control bits.

Offset: 0x074

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Type/Reset			Reserved					TEVDE UEV2DE UEV1DE
						RW 0	RW 0	RW 0
Type/Reset	23	22	21	20	19	18	17	16
		Reserved					CH3CCDE CH2CCDE CH1CCDE CH0CCDE	
						RW 0	RW 0	RW 0
Type/Reset	15	14	13	12	11	10	9	8
		Reserved					BRKIE TEVIE UEV2IE UEV1IE	
						RW 0	RW 0	RW 0
Type/Reset	7	6	5	4	3	2	1	0
		Reserved					CH3CCIE CH2CCIE CH1CCIE CH0CCIE	
						RW 0	RW 0	RW 0

Bits	Field	Descriptions
[26]	TEVDE	Trigger event PDMA Request Enable 0: Trigger PDMA request disabled 1: Trigger PDMA request enabled
[25]	UEV2DE	Update event 2 PDMA Request Enable 0: Update event 2 PDMA request disabled 1: Update event 2 PDMA request enabled
[24]	UEV1DE	Update event 1 DMA Request Enable 0: Update event 1 DMA request disabled 1: Update event 1 DMA request enabled
[19]	CH3CCDE	Channel 3 Capture/Compare PDMA Request Enable 0: Channel 3 PDMA request disabled 1: Channel 3 PDMA request enabled
[18]	CH2CCDE	Channel 2 Capture/Compare PDMA Request Enable 0: Channel 2 PDMA request disabled 1: Channel 2 PDMA request enabled
[17]	CH1CCDE	Channel 1 Capture/Compare PDMA Request Enable 0: Channel 1 PDMA request disabled 1: Channel 1 PDMA request enabled
[16]	CH0CCDE	Channel 0 Capture/Compare PDMA Request Enable 0: Channel 0 PDMA request disabled 1: Channel 0 PDMA request enabled
[11]	BRKIE	Break event Interrupt Enable 0: Break event interrupt disabled 1: Break event interrupt enabled
[10]	TEVIE	Trigger event Interrupt Enable 0: Trigger event interrupt disabled 1: Trigger event interrupt enabled

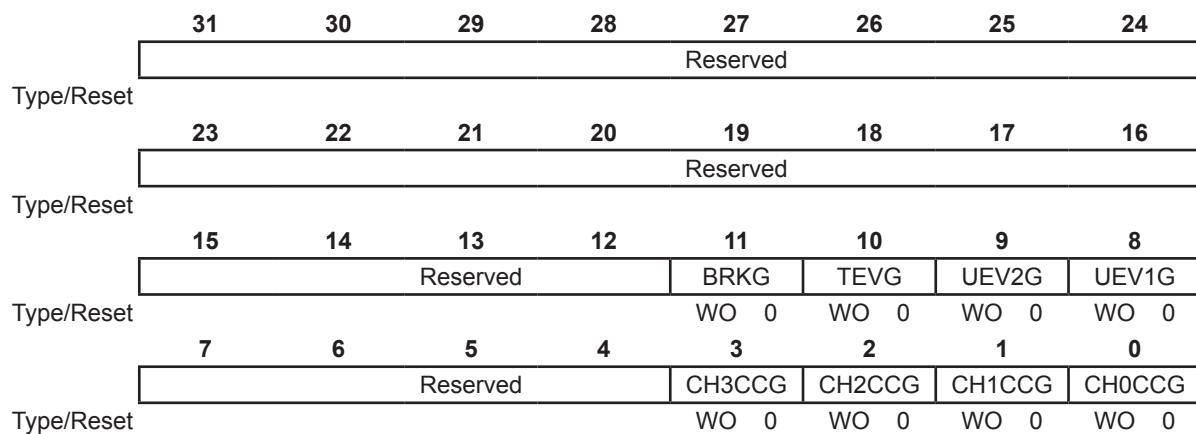
Bits	Field	Descriptions
[9]	UEV2IE	Update event 2 Interrupt Enable 0: Update event 2 interrupt disabled 1: Update event 2 interrupt enabled
[8]	UEV1IE	Update event 1 Interrupt Enable 0: Update event 1 interrupt disabled 1: Update event 1 interrupt enabled
[3]	CH3CCIE	Channel 3 Capture/Compare Interrupt Enable 0: Channel 3 interrupt disabled 1: Channel 3 interrupt enabled
[2]	CH2CCIE	Channel 2 Capture/Compare Interrupt Enable 0: Channel 2 interrupt disabled 1: Channel 2 interrupt enabled
[1]	CH1CCIE	Channel 1 Capture/Compare Interrupt Enable 0: Channel 1 interrupt disabled 1: Channel 1 interrupt enabled
[0]	CH0CCIE	Channel 0 Capture/Compare Interrupt Enable 0: Channel 0 interrupt disabled 1: Channel 0 interrupt enabled

Timer Event Generator Register – EVGR

This register contains the software event generation bits.

Offset: 0x078

Reset value: 0x0000_0000



Bits	Field	Descriptions
[11]	BRKG	<p>Software Break Event Generation</p> <p>The break event BEV can be generated by setting this bit. It is automatically cleared by hardware.</p> <p>0: No action.</p> <p>1: The BRK0IF flag is set and then the CHMOE bit will be cleared.</p>
[10]	TEVG	<p>Trigger Event Generation</p> <p>The trigger event TEV can be generated by setting this bit. It is cleared by hardware automatically.</p> <p>0: No action</p> <p>1: The TEVIF flag is set</p>
[9]	UEV2G	<p>Update Event 2 Generation</p> <p>The update event 2 UEV2 can be generated by setting this bit. It is cleared by hardware automatically.</p> <p>0: No action</p> <p>1: Update the CHxE, CHxNE, and CHxOM bits when COMPRE bit in CTR Register is set to 1.</p>
[8]	UEV1G	<p>Update Event 1 Generation</p> <p>The update event 1 UEV1 can be generated by setting this bit. It is cleared by hardware automatically.</p> <p>0: No action</p> <p>1: Reinitialise the counter</p> <p>The counter value returns to 0 or the CRR preload value, depending on the counter mode in which the current timer is being used. An update operation on any related registers will also be executed. For a more detailed description, refer to the corresponding section.</p>

Bits	Field	Descriptions
[3]	CH3CCG	<p>Channel 3 Capture/Compare Generation</p> <p>A Channel 3 capture/compare event can be generated by setting this bit. It is cleared by hardware automatically.</p> <ul style="list-style-type: none"> 0: No action 1: Capture/compare event is generated on channel 3 <p>If Channel 3 is configured as an input, the counter value is captured into the CH3CCR register and then the CH3CCIF bit is set. If Channel 3 is configured as an output, the CH3CCIF bit is set.</p>
[2]	CH2CCG	<p>Channel 2 Capture/Compare Generation</p> <p>A Channel 2 capture/compare event can be generated by setting this bit. It is cleared by hardware automatically.</p> <ul style="list-style-type: none"> 0: No action 1: Capture/compare event is generated on channel 2 <p>If Channel 2 is configured as an input, the counter value is captured into the CH2CCR register and then the CH2CCIF bit is set. If Channel 2 is configured as an output, the CH2CCIF bit is set.</p>
[1]	CH1CCG	<p>Channel 1 Capture/Compare Generation</p> <p>A Channel 1 capture/compare event can be generated by setting this bit. It is cleared by hardware automatically.</p> <ul style="list-style-type: none"> 0: No action 1: Capture/compare event is generated on channel 1 <p>If Channel 1 is configured as an input, the counter value is captured into the CH1CCR register and then the CH1CCIF bit is set. If Channel 1 is configured as an output, the CH1CCIF bit is set.</p>
[0]	CH0CCG	<p>Channel 0 Capture/Compare Generation</p> <p>A Channel 0 capture/compare event can be generated by setting this bit. It is cleared by hardware automatically.</p> <ul style="list-style-type: none"> 0: No action 1: Capture/compare event is generated on channel 0 <p>If Channel 0 is configured as an input, the counter value is captured into the CH0CCR register and then the CH0CCIF bit is set. If Channel 0 is configured as an output, the CH0CCIF bit is set.</p>

Timer Interrupt Status Register – INTSR

This register stores the timer interrupt status.

Offset: 0x07C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24	
Reserved									
Type/Reset									
	23	22	21	20	19	18	17	16	
Reserved									
Type/Reset									
	15	14	13	12	11	10	9	8	
Reserved									
Type/Reset									
	7	6	5	4	3	2	1	0	
CH3OCF CH2OCF CH1OCF CH0OCF CH3CCIF CH2CCIF CH1CCIF CH0CCIF									
Type/Reset	RW	0	RW	0	RW	0	RW	0	

Bits	Field	Descriptions
[12]	BRK1IF	Break 1 Event Interrupt Flag This flag is set by hardware when a break 1 event occurs and is cleared by software. 0: No break 1 event occurred 1: Break 1 event occurred
[11]	BRK0IF	Break 0 Event Interrupt Flag This flag is set by hardware when a break 0 event occurs and is cleared by software. 0: No break 0 event occurred 1: Break 0 event occurred
[10]	TEVIF	Trigger Event Interrupt Flag This flag is set by hardware when a trigger event occurs and is cleared by software. 0: No trigger event occurred 1: Trigger event occurred
[9]	UEV2IF	Update Event 2 Interrupt Flag This bit is set by hardware when an update event 2 occurs and is cleared by software. 0: No update event 2 occurred 1: Update event 2 occurred
[8]	UEV1IF	Update Event 1 Interrupt Flag This bit is set by hardware when a update event 1 occurs and is cleared by software. 0: No update event 1 occurred 1: Update event 1 occurred Note: The update event 1 is sourced from the following conditions: - A counter overflow or underflow - The UEV1G bit is set with UEVDIS=0 - A STI rising edge is received in slave restart mode with UEVDIS=0
[7]	CH3OCF	Channel 3 Over-capture Flag This flag is set by hardware and cleared by software. 0: No over-capture event is detected 1: Capture event occurs again when the CH3CCIF bit is already set and it is not yet cleared by software.

Bits	Field	Descriptions
[6]	CH2OCF	<p>Channel 2 Over-capture Flag</p> <p>This flag is set by hardware and cleared by software.</p> <ul style="list-style-type: none"> 0: No over-capture event is detected 1: Capture event occurs again when the CH2CCIF bit is already set and it is not cleared yet by software.
[5]	CH1OCF	<p>Channel 1 Over-capture Flag</p> <p>This flag is set by hardware and cleared by software.</p> <ul style="list-style-type: none"> 0: No over-capture event is detected 1: Capture event occurs again when the CH1CCIF bit is already set and it is not cleared yet by software.
[4]	CH0OCF	<p>Channel 0 Over-capture Flag</p> <p>This flag is set by hardware and cleared by software.</p> <ul style="list-style-type: none"> 0: No over-capture event is detected 1: Capture event occurs again when the CH0CCIF bit is already set and it is not yet cleared by software
[3]	CH3CCIF	<p>Channel 3 Capture/Compare Interrupt Flag</p> <ul style="list-style-type: none"> - Channel 3 is configured as an output <ul style="list-style-type: none"> 0: No match event occurred 1: The contents of the counter CNTR have matched the contents of the CH3CCR register. <p>This flag is set by hardware when the counter value matches the CH3CCR value with exception in the center-aligned counting mode. It is cleared by software.</p> - Channel 3 is configured as an input <ul style="list-style-type: none"> 0: No input capture occurred 1: Input capture occurred <p>This bit is set by hardware when a capture event occurs. It is cleared by software or by reading the CH3CCR register.</p>
[2]	CH2CCIF	<p>Channel 2 Capture/Compare Interrupt Flag</p> <ul style="list-style-type: none"> - Channel 2 is configured as an output <ul style="list-style-type: none"> 0: No match event occurred 1: The contents of the counter CNTR have matched the contents of the CH2CCR register <p>This flag is set by hardware when the counter value matches the CH2CCR value with exception in the center-aligned counting mode. It is cleared by software.</p> - Channel 2 is configured as an input <ul style="list-style-type: none"> 0: No input capture occurred 1: Input capture occurred. <p>This bit is set by hardware on a capture event. It is cleared by software or by reading the CH2CCR register.</p>

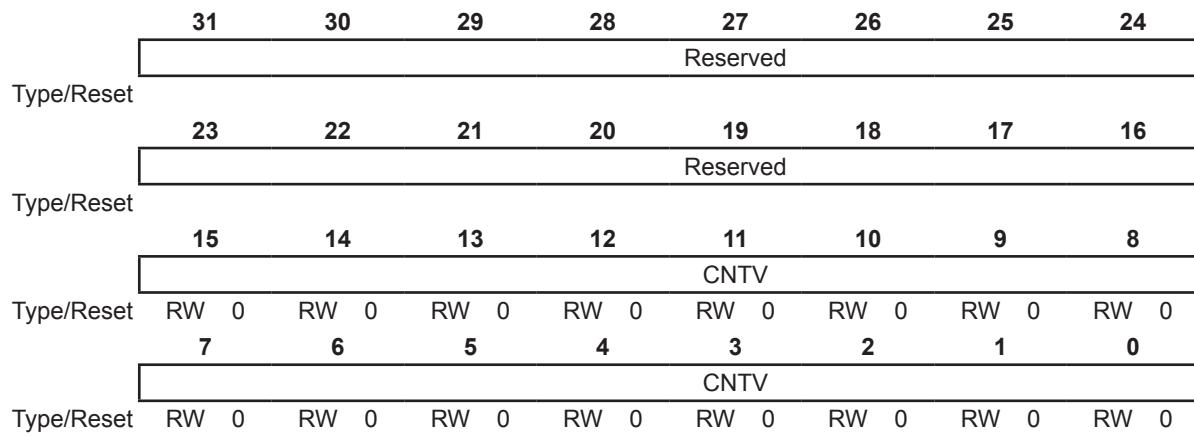
Bits	Field	Descriptions
[1]	CH1CCIF	<p>Channel 1 Capture/Compare Interrupt Flag</p> <ul style="list-style-type: none">- Channel 1 is configured as an output<ul style="list-style-type: none">0: No match event occurred1: The contents of the counter CNTR have matched the contents of the CH1CCR registerThis flag is set by hardware when the counter value matches the CH1CCR value with exception in the center-aligned counting mode. It is cleared by software.- Channel 1 is configured as an input<ul style="list-style-type: none">0: No input capture occurred1: Input capture occurredThis bit is set by hardware on a capture event. It is cleared by software or by reading the CH1CCR register.
[0]	CH0CCIF	<p>Channel 0 Capture/Compare Interrupt Flag</p> <ul style="list-style-type: none">- Channel 0 is configured as an output<ul style="list-style-type: none">0: No match event occurs1: The contents of the counter CNTR have matched the content of the CH0CCR registerThis flag is set by hardware when the counter value matches the CH0CCR value with exception in the center-aligned counting mode. It is cleared by software.- Channel 0 is configured as an input<ul style="list-style-type: none">0: No input capture occurred1: Input capture occurredThis bit is set by hardware on a capture event. It is cleared by software or by reading the CH0CCR register.

Timer Counter Register – CNTR

This register stores the timer counter value.

Offset: 0x080

Reset value: 0x0000_0000



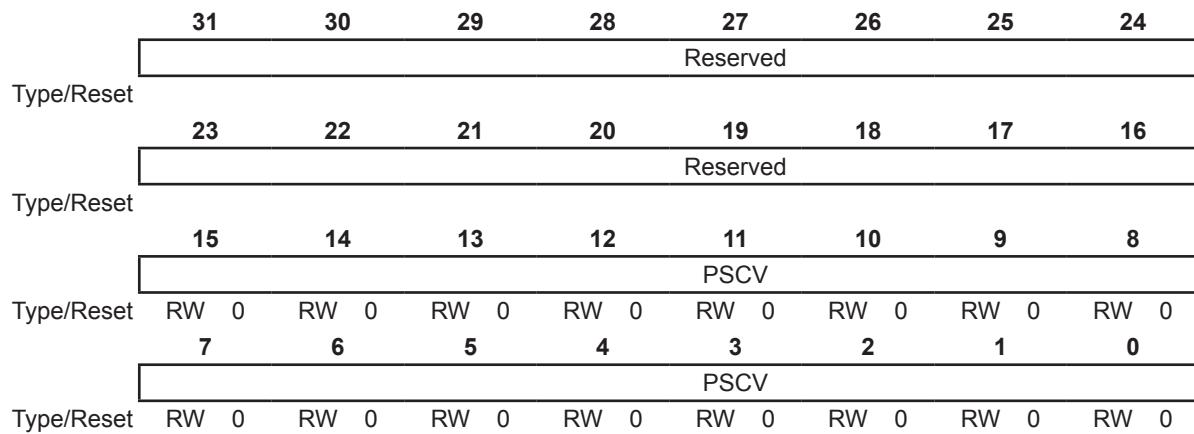
Bits	Field	Descriptions
[15:0]	CNTV	Counter Value.

Timer Prescaler Register – PSCR

This register specifies the timer prescaler value to generate the counter clock.

Offset: 0x084

Reset value: 0x0000_0000



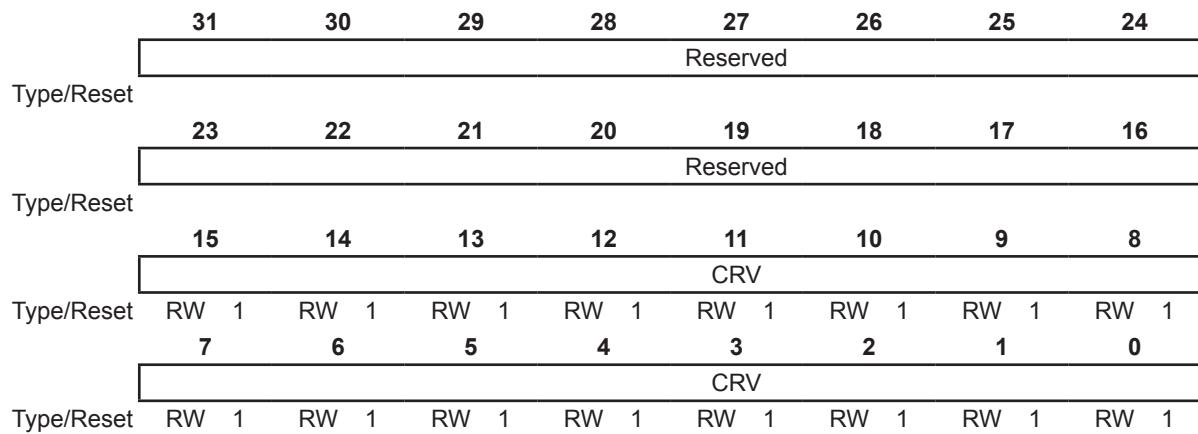
Bits	Field	Descriptions
[15:0]	PSCV	<p>Prescaler Value</p> <p>These bits are used to specify the prescaler value to generate the counter clock frequency f_{CK_CNT}.</p> $f_{CK_CNT} = \frac{f_{CK_PSC}}{PSCV[15:0] + 1}$ <p>where the f_{CK_PSC} is the prescaler clock source.</p>

Timer Counter Reload Register – CRR

This register specifies the timer counter reload value.

Offset: 0x088

Reset value: 0x0000_FFFF



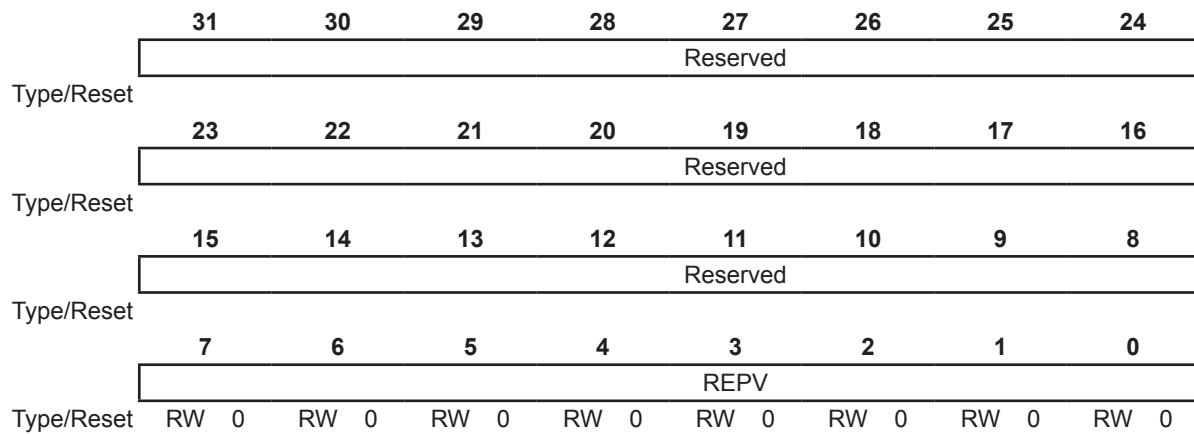
Bits	Field	Descriptions
[15:0]	CRV	Counter Reload Value The CRV is the reload value which is loaded into the actual counter register.

Timer Repetition Register – REPR

This register specifies the timer repetition counter value.

Offset: 0x08C

Reset value: 0x0000_0000



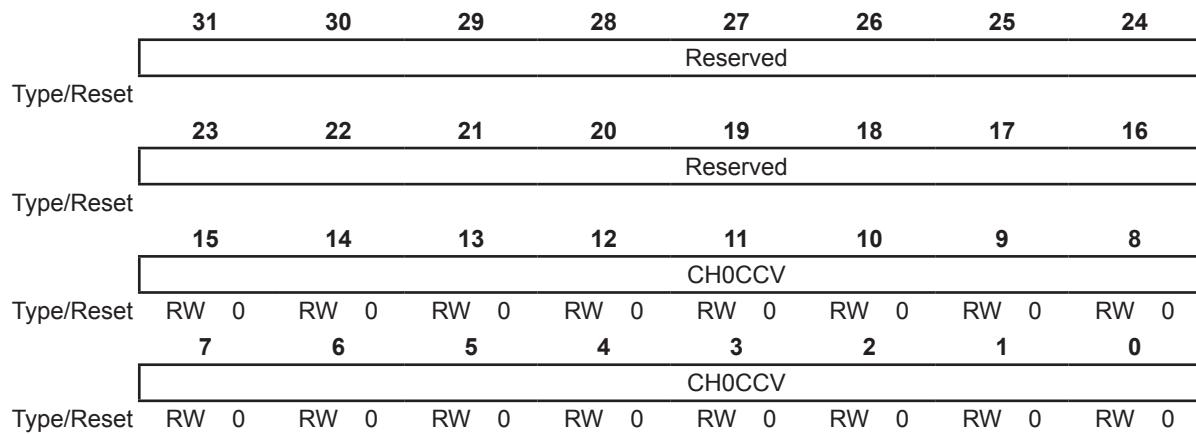
Bits	Field	Descriptions
[7:0]	REPV	Repetition Counter Value. These bits allow the user to specify the update rate of the compare registers.

Channel 0 Capture/Compare Register – CH0CCR

This register specifies the timer channel 0 capture/compare value.

Offset: 0x090

Reset value: 0x0000_0000



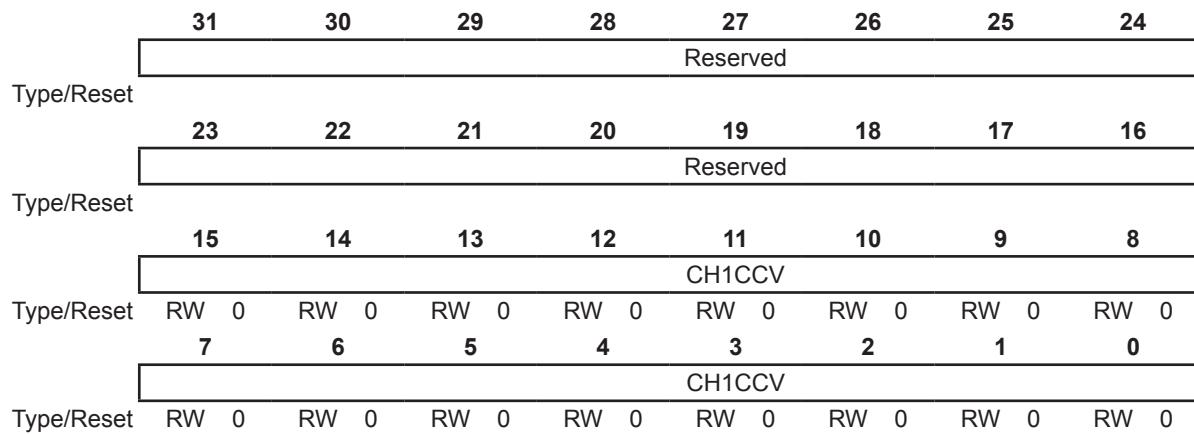
Bits	Field	Descriptions
[15:0]	CH0CCV	<p>Channel 0 Capture/Compare Value</p> <ul style="list-style-type: none"> - When Channel 0 is configured as an output The CH0CCR value is compared with the counter value and the comparison result is used to trigger the CH0OREF output signal. - When Channel 0 is configured as an input The CH0CCR register stores the counter value captured by the last channel 0 capture event.

Channel 1 Capture/Compare Register – CH1CCR

This register specifies the timer channel 1 capture/compare value.

Offset: 0x094

Reset value: 0x0000_0000



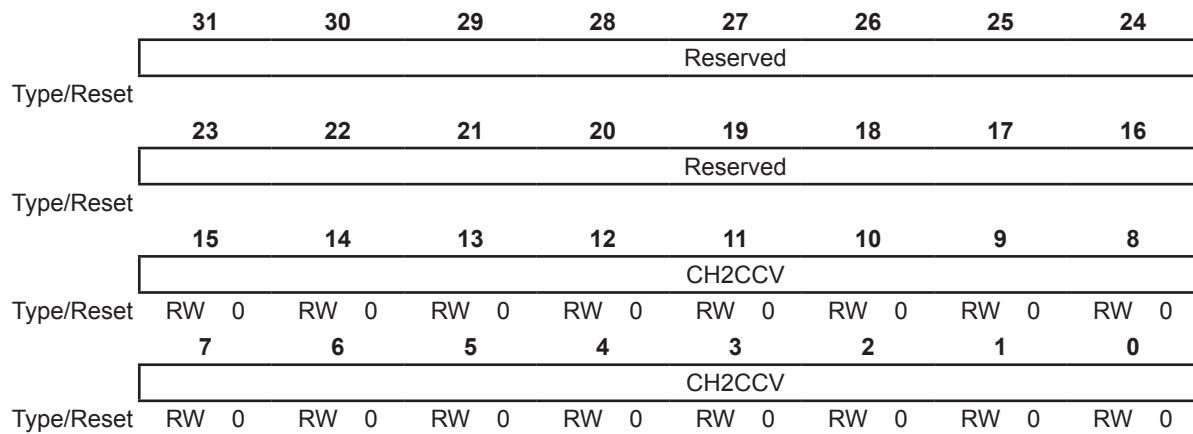
Bits	Field	Descriptions
[15:0]	CH1CCV	<p>Channel 1 Capture/Compare Value</p> <ul style="list-style-type: none"> - When Channel 1 is configured as an output The CH1CCR value is compared with the counter value and the comparison result is used to trigger the CH1OREF output signal. - When Channel 1 is configured as an input The CH1CCR register stores the counter value captured by the last channel 1 capture event.

Channel 2 Capture/Compare Register – CH2CCR

This register specifies the timer channel 2 capture/compare value.

Offset: 0x098

Reset value: 0x0000_0000



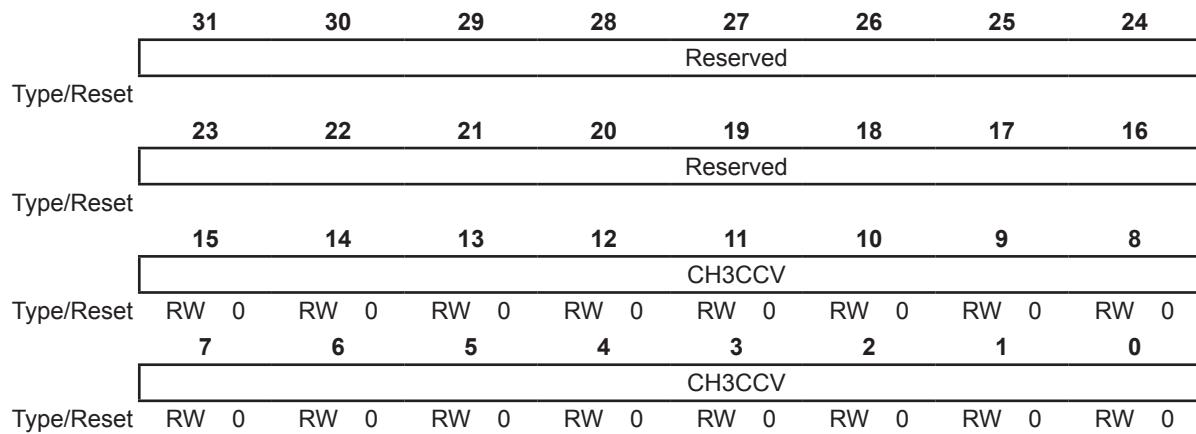
Bits	Field	Descriptions
[15:0]	CH2CCV	<p>Channel 2 Capture/Compare Value</p> <ul style="list-style-type: none"> - When Channel 2 is configured as an output The CH2CCR value is compared with the counter value and the comparison result is used to trigger the CH2OREF output signal. - When Channel 2 is configured as an input The CH2CCR register stores the counter value captured by the last channel 2 capture event.

Channel 3 Capture/Compare Register – CH3CCR

This register specifies the timer channel 3 capture/compare value.

Offset: 0x09C

Reset value: 0x0000_0000



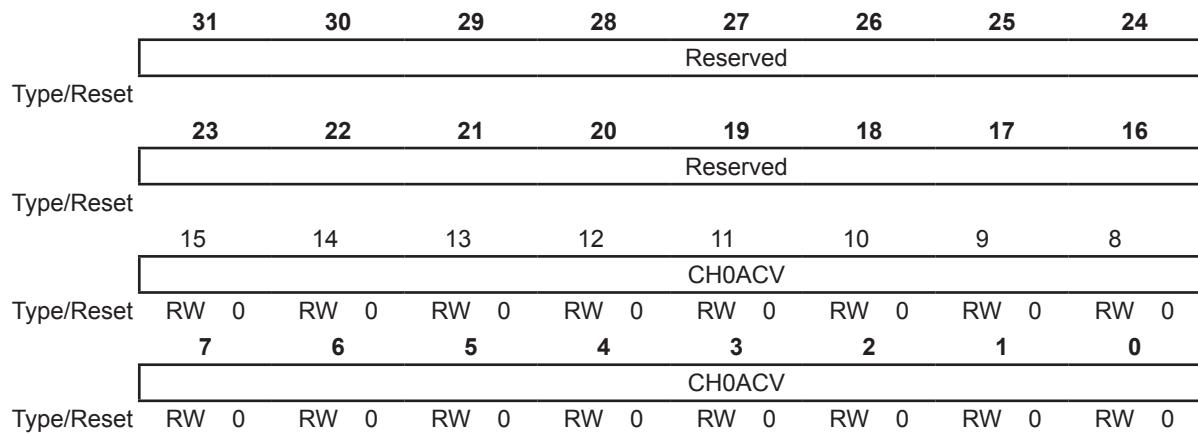
Bits	Field	Descriptions
[15:0]	CH3CCV	<p>Channel 3 Capture/Compare Value</p> <ul style="list-style-type: none"> - When Channel 3 is configured as an output The CH3CCR value is compared with the counter value and the comparison result is used to trigger the CH3OREF output signal. - When Channel 3 is configured as an input The CH3CCR register stores the counter value captured by the last channel 3 capture event.

Channel 0 Asymmetric Compare Register – CH0ACR

This register specifies the timer channel 0 asymmetric compare value.

Offset: 0x0A0

Reset value: 0x0000_0000



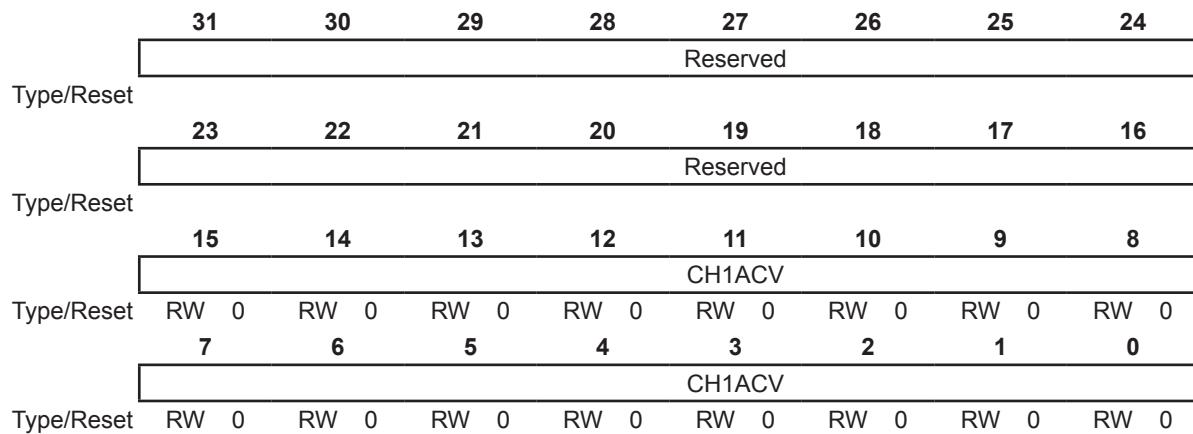
Bits	Field	Descriptions
[15:0]	CH0ACV	Channel 0 Asymmetric Compare Value When channel 0 is configured as asymmetric PWM mode and the counter is counting down, the value written is this register will be compared to the counter.

Channel 1 Asymmetric Compare Register – CH1ACR

This register specifies the timer channel 1 asymmetric compare value.

Offset: 0x0A4

Reset value: 0x0000_0000



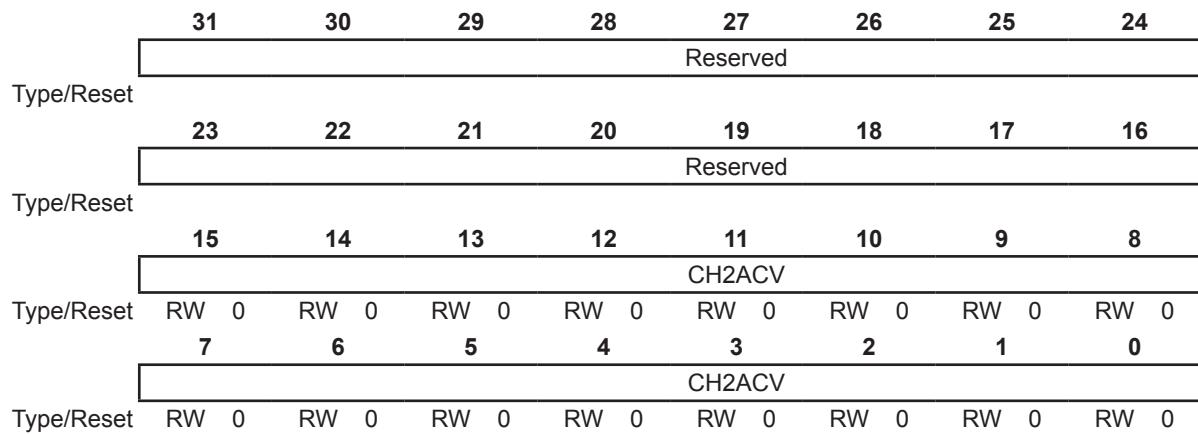
Bits	Field	Descriptions
[15:0]	CH1ACV	<p>Channel 1 Asymmetric Compare Value</p> <p>When channel 1 is configured as asymmetric PWM mode and the counter is counting down, the value written is this register will be compared to the counter.</p>

Channel 2 Asymmetric Compare Register – CH2ACR

This register specifies the timer channel 2 asymmetric compare value.

Offset: 0x0A8

Reset value: 0x0000_0000



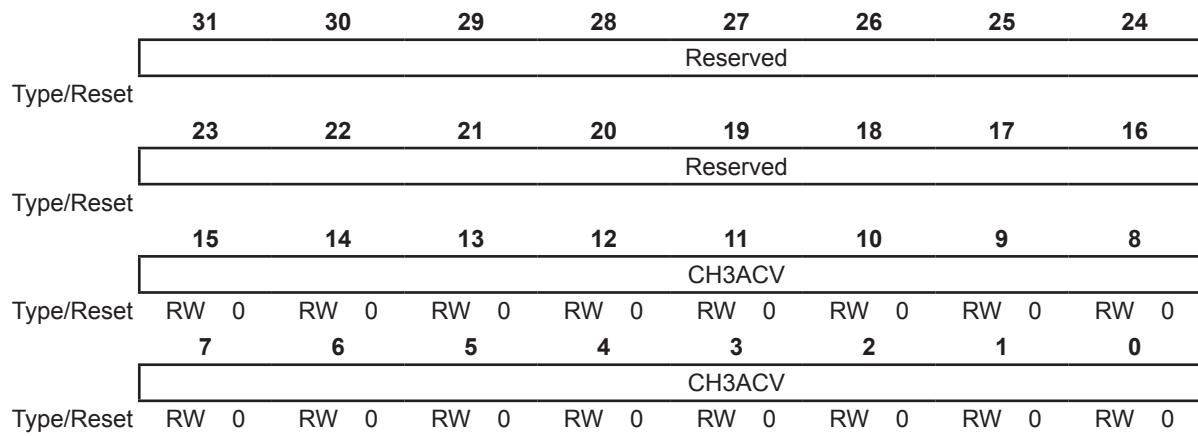
Bits	Field	Descriptions
[15:0]	CH2ACV	Channel 2 Asymmetric Compare Value When channel 2 is configured as asymmetric PWM mode and the counter is counting down, the value written is this register will be compared to the counter.

Channel 3 Asymmetric Compare Register – CH3ACR

This register specifies the timer channel 3 asymmetric compare value.

Offset: 0x0AC

Reset value: 0x0000_0000



Bits	Field	Descriptions
[15:0]	CH3ACV	Channel 3 Asymmetric Compare Value When channel 3 is configured as asymmetric PWM mode and the counter is counting down, the value written is this register will be compared to the counter.

17 Real Time Clock (RTC)

Introduction

The Real Time Clock, RTC, circuitry includes the APB interface, a 32-bit up-counter, a control register, a prescaler, a compare register and a status register. Most of the RTC circuits are located in the Backup Domain, as shown shaded in the accompanying figure, except for the APB interface. The APB interface is located in the VDD18 domain. Therefore, it is necessary to be isolated from the ISO signal that comes from the power control unit when the VDD18 domain is powered off, i.e., when the device enters the Power-Down mode. The RTC counter is used as a wakeup timer to let the system resume from the Power-Down mode. The detailed RTC function will be described in the following sections.

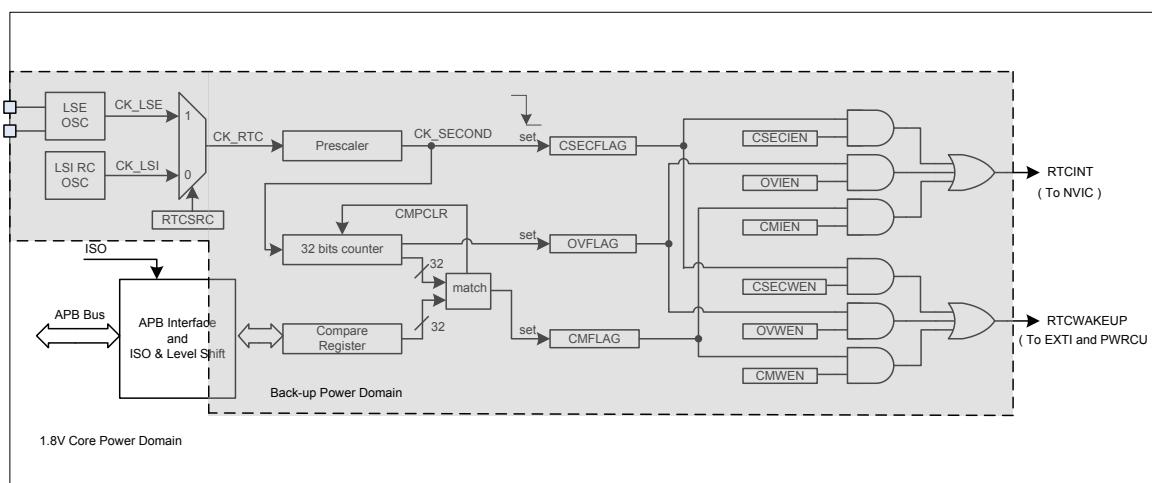


Figure 118. RTC Block Diagram

Features

- 32-bit up counter for counting elapsed time
- Programmable clock prescaler
 - Division factor: 1, 2, 4, 8...,32768
- 32-bit compare register for alarm usage
- RTC clock source
 - LSE oscillator clock
 - LSI oscillator clock
- Three RTC Interrupt/wakeup settings
 - RTC second clock interrupt/wakeup
 - RTC compare match interrupt/wakeup
 - RTC counter overflow interrupt/wakeup
- The RTC interrupt/wakeup event can work together with power management to wake up the chip from power saving mode

Functional Descriptions

RTC Related Register Reset

The RTC registers can only be reset by either a Backup Domain power on reset, PORB, or by a Backup Domain software reset by setting the BAKRST bit in the BAKCR register. Other reset events have no effect to clear the RTC registers.

Reading RTC Register

The RTC control logic and the related registers are powered by the V_{BAK} supply voltage. Therefore, the RTC circuitry remains operational in the Power-Down mode where V_{DD18} is powered off. Only the APB bus, which is located in the V_{DD18} domain, is interconnected to the circuits located in the V_{BAK} domain using level shift circuitry and isolated by the ISO signals when the V_{DD18} supply voltage is powered off. The isolation function must be disabled by setting the BAKISO bit to 1 in the LPCR register as described in the Clock Control Unit before accessing the RTC registers using the APB bus.

Low Speed Clock Configuration

The default RTC clock source, CK_RTC, is derived from the LSI oscillator. The CK_RTC clock can be derived from either the external 32768 Hz crystal oscillator, named the LSE oscillator, or the internal 32K RC oscillator named the LSI oscillator, by setting the RTCSRC bit in the RTCCR register. A prescaler is provided to divide the CK_RTC by a ratio ranged from 2⁰ to 2¹⁵ determined by the RPREG [3:0] field. For instance, setting the prescaler value RPREG [3:0] to 0x0F will generate an exact 1 Hz CK_SECOND clock if the CK_RTC clock frequency is equal to 32,768 Hz. The LSI and LSE oscillators can be enabled by the LSIVEN and LSEEN control bits in the RTCCR register respectively. In addition, the LSE oscillator startup mode can be selected by configuring the LSESM bit in the RTCCR register. This enables the LSE oscillator to have either a shorter startup time or a lower power consumption, both of which are traded off depending upon specific application requirements. An example of the startup time and the power consumption for different startup modes are shown in the accompanying table for reference.

Table 41. LSE Startup Mode Operating Current and Startup Time

Startup mode	LSECM Setting in the RTCCR register	Operating Current	Startup time
Normal startup	0	3µA	Above 200ms
Fast startup	1	8µA	Below 200ms

@ V_{DD} = 3.3 V and LSE clock = 32,768 Hz; these values are only for reference, actual values are dependent on the specification of the external 32.768KHz crystal.

RTC Counter Operation

The RTC provides a 32-bit up-counter which increments at the falling edge of the CK_SECOND clock and whose value can be read from the RTCCNT register asynchronously via the APB bus. A 32-bit compare register, RTCCMP, is provided to store the specific value to be compared with the RTCCNT content. This is used to define a pre-determined time interval. When the RTCCNT register content is equal to the RTCCMP register value, the match flag CMFLAG in the RTCSR register will be set by hardware and an interrupt or wakeup event can be sent according to the corresponding enable bits in the RTCIWEN register. The RTC counter will be either reset to zero or keep counting when the compare match event occurs, dependent upon the CMPCLR bit in the RTCCR register. For example, if the RPREG [3:0] is set to 0x0F, the RTCCMP register content is set to a decimal value of 60 and the CMPCLR bit is set to 1, then the CMFLAG bit will be set every minute. In addition, the OVFLAG bit in the RTCSR register will be set when the RTC counter overflows. A read operation on the RTCSR register clears the status flags including the CSECFLAG, CMFLAG and OVFLAG bits.

Interrupt and Wakeup Control

The falling edge of the CK_SECOND clock causes the CSECFLAG bit in the RTCSR register to be set and generates an interrupt if the corresponding interrupt enable bit, CSECIEN, in the RTCIWEN register is set. The wakeup event can also be generated to wake up the HSI/HSE oscillators, the PLL circuitry, the LDO and the Cortex™ -M3 core if the corresponding wakeup enable bit CSECWEN is set. When the RTC counter overflows or a compare match event occurs, it will generate an interrupt or a wake up event determined by the corresponding interrupt or wakeup enable control bits, OVIEN/OVWEN or CMIEN/CMWEN bits, in the RTCIWEN register. Refer to the related register definitions for more details.

RTCOUT Output Pin Configuration

The following table shows RTCOUT output format according to the mode, polarity, and event selection setting.

Table 42. RTCOUT Output Mode and Active Level Setting

ROWM	ROES	RTCOUT Output Waveform				
0 (Pulse mode)	0 Compare match	RTCCMP		4		
		RTCCNT	3	4	5	
		RTCOUT (ROAP = 0)		T_R		
		RTCOUT (ROAP = 1)				
		ROLF				
	1 Second clock	RTCCMP		X		
		RTCCNT	3	4	5	
		RTCOUT (ROAP = 0)	T_R	T_R	T_R	
		RTCOUT (ROAP = 1)				
		ROLF				
1 (Level mode)	0 Compare match	RTCCMP		4		
		RTCCNT	3	4	5	
		RTCOUT (ROAP = 0)				
		RTCOUT (ROAP = 1)				
		ROLF			\rightarrow	
	1 Second clock	RTCCMP		X		
		RTCCNT	3	4	5	
		RTCOUT (ROAP = 0)				
		RTCOUT (ROAP = 1)				
		ROLF		\rightarrow	\rightarrow	

T_R : RTCOUT output pulse time= $1/f_{CK_RTC}$
 \rightarrow : Clear by software reading ROLF bit

Register Map

The following table shows the RTC registers and reset values. Note all the registers in this unit are located at the V_{BAK} backup power domain.

Table 43. RTC Register Map

Register	Offset	Description	Reset Value
RTC Base Address = 0x4006_A000			
RTCCNT	0x000	RTC Counter Register	0x0000_0000
RTCCMP	0x004	RTC Compare Register	0x0000_0000
RTCCR	0x008	RTC Control Register	0x0000_0F04
RTCSR	0x00C	RTC Status Register	0x0000_0000
RTCIWEN	0x010	RTC Interrupt and Wakeup Enable Register	0x0000_0000

Register Descriptions

RTC Counter Register – RTCCNT

This register defines a 32-bit up counter which is incremented by the CK_SECOND clock.

Address: 0x000

Reset value: 0x0000_0000

RTCCNTV									
Type/Reset	RO 0								
	23	22	21	20	19	18	17	16	
RTCCNTV									
Type/Reset	RO 0								
	15	14	13	12	11	10	9	8	
RTCCNTV									
Type/Reset	RO 0								
	7	6	5	4	3	2	1	0	
RTCCNTV									
Type/Reset	RO 0								

Bits	Field	Descriptions
[31:0]	RTCCNTV	<p>RTC Counter</p> <p>The current value of the RTC counter is returned when reading the RTCCNT register. The RTCCNT register is updated during the falling edge of the CK_SECOND. This register is reset by one of the following conditions:</p> <ul style="list-style-type: none"> Backup Domain software reset - set the BAKRST bit in the BAKCR register Backup Domain power on reset - PORB Compare match (RTCCNT = RTCCMP) when CMPCLR = 1 (in the RTCCR register) RTCEN bit changed from 0 to 1

RTC Compare Register – RTCCMP

This register defines a specific value to be compared with the RTC counter value.

Address: 0x004

Reset value: 0x0000_0000 (Reset by Backup Domain reset only)

	31	30	29	28	27	26	25	24
RTCCMPV								
Type/Reset	RW 0							
23 22 21 20 19 18 17 16								
RTCCMPV								
Type/Reset	RW 0							
15 14 13 12 11 10 9 8								
RTCCMPV								
Type/Reset	RW 0							
7 6 5 4 3 2 1 0								
RTCCMPV								
Type/Reset	RW 0							

Bits	Field	Descriptions
[31:0]	RTCCMPV	<p>RTC Compare Match Value</p> <p>A match condition happens when the value in the RTCCNT register is equal to RTCCMP value. An interrupt can be generated if the CMIEN bit in the RTCIWIN register is set. When the CMPCLR bit in the RTCCR register is set to 0 and a match condition happens, the CMFLAG bit in the RTCSR register is set while the value in the RTCCNT register is not affected and will continue to count until overflow. When the CMPCLR bit is set to 1 and a match condition happens, the CMFLAG bit in the RTCSR register is set and the RTCCNT register will be reset to zero and then the counter continues to count.</p>

RTC Control Register – RTCCR

This register specifies a range of RTC circuitry control bits.

Address: 0x008

Reset value: 0x0000_0F04 (Reset by Backup Domain reset only)

	31	30	29	28	27	26	25	24
Reserved								
Type/Reset	23	22	21	20	19	18	17	16
	Reserved		ROLF	ROAP	ROWM	ROES	ROEN	
Type/Reset			RC 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
Type/Reset	Reserved			RPRE				
	7	6	5	4	3	2	1	0
Type/Reset	Reserved	LSESM	CMPCLR	LSEEN	LSIEN	RTCSR	RTCEN	
		RW 0	RW 0	RW 0	RW 1	RW 0	RW 0	

Bits	Field	Descriptions
[20]	ROLF	RTCOUT Level Mode Flag 0: RTCOUT Output is inactive 1: RTCOUT Output is holding as active level Set by hardware when level mode (ROWM = 1) and a RTCOUT output event occurred. Cleared by software reading this flag. The RTCOUT signal will return to the inactive level after software has read this bit.
[19]	ROAP	RTCOUT Output Active Polarity 0: Active level is high 1: Active level is low
[18]	ROWM	RTCOUT Output Waveform Mode 0: Pulse mode The output pulse duration is one RTC clock (CK_RTC) period. 1: Level mode The RTCOUT signal will remain at an active level until the ROLF bit is cleared by software reading the ROLF bit.
[17]	ROES	RTCOUT Output Event Selection 0: RTC compare match is selected 1: RTC second clock (CK_SECOND) event is selected The ROES bit can be used to select whether the RTCOUT signal is output on the RTCOUT pin when a RTC compare match event or the RTC second clock (CK_SECOND) event occurs.
[16]	ROEN	RTCOUT Output Pin Enable 0: Disable RTCOUT output pin 1: Enable RTCOUT output pin When the ROEN bit is set to 1, the RTCOUT signal will be at an active level once a RTC compare match on the RTC second clock (CK_SECOOD) event occurs. The active polarity and output waveform mode can be configured by the ROAP and ROWM bits respectively. When the ROEN bit is cleared to 0, the RTCOUT pin will be in a floating state.

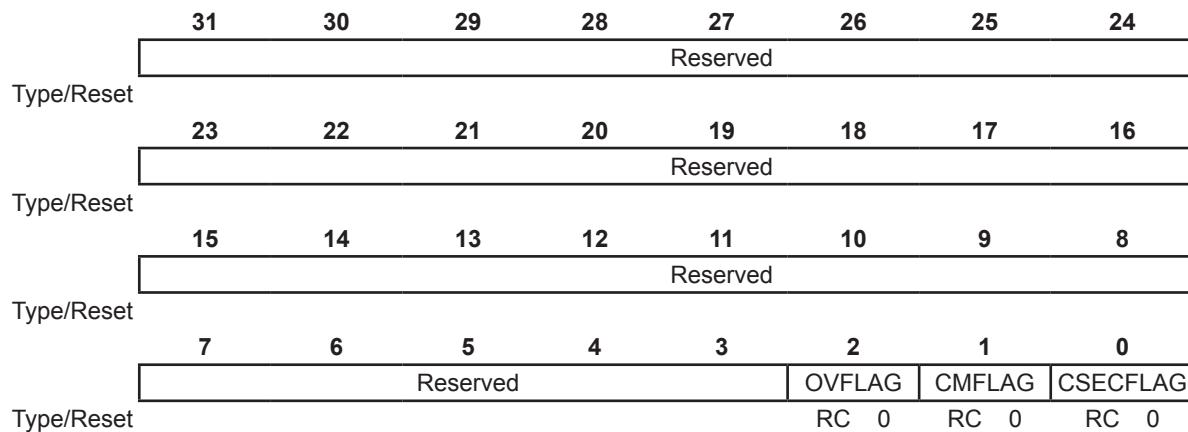
Bits	Field	Descriptions
[11:8]	RPRE	RTC Clock Prescaler Select $CK_{SECOND} = CK_{RTC} / 2^{RPRE}$ b0000: $CK_{SECOND} = CK_{RTC} / 2^0$ b0001: $CK_{SECOND} = CK_{RTC} / 2^1$ b0010: $CK_{SECOND} = CK_{RTC} / 2^2$... b1111: $CK_{SECOND} = CK_{RTC} / 2^{15}$
[5]	LSESM	LSE oscillator Startup Mode 0: Normal startup and requires less operating power 1: Fast startup but requires higher operating current
[4]	CMPCLR	Compare Match Counter Clear 0: 32-bit RTC counter is not affected when compare match condition occurs 1: 32-bit RTC counter is cleared when compare match condition occurs
[3]	LSEEN	LSE oscillator Enable Control 0: LSE oscillator disabled 1: LSE oscillator enabled
[2]	LSIEN	LSI oscillator Enable Control 0: LSI oscillator disabled 1: LSI oscillator enabled The LSIEN bit default value is 1 which means the LSI oscillator is enabled automatically after the Backup Domain powered up. Note: After the backup domain is powered on, the internal LSI RC oscillator will start to oscillate. The frequency range of the LSI oscillator is shown in the LSI oscillator electrical characteristics in the datasheet. The device also provides a production trim value to obtain a more accurate oscillation frequency. The procedure is to disable the LSI oscillator and then enable it again after the backup domain is powered on. After the trimming procedure has completed, the system will automatically load the production trim value to the frequency trimming circuit of the LSI RC oscillator.
[1]	RTCSRC	RTC Clock Source Selection 0: LSI oscillator selected as the RTC clock source 1: LSE oscillator selected as the RTC clock source
[0]	RTCEN	RTC Enable Control 0: RTC is disabled 1: RTC is enabled

RTC Status Register – RTCSR

This register stores the counter flags.

Address: 0x00C

Reset value: 0x0000_0000 (Reset by Backup Domain reset and RTCEN bit change from 1 to 0)



Bits	Field	Descriptions
[2]	OVFLAG	<p>Counter Overflow Flag</p> <p>0: Counter overflow not occurred since the last RTCSR register read operation</p> <p>1: Counter overflow has occurred since the last RTCSR register read operation</p> <p>This bit is set by hardware when the counter value in the RTCCNT register changes from 0xFFFF_FFFF to 0x0000_0000 and cleared by read operation. This bit is suggested to read in the RTC IRQ handler and should be taken care when software polling is used.</p>
[1]	CMFLAG	<p>Compare Match Condition Flag</p> <p>0: Compare match condition not occurred since the last RTCSR register read operation</p> <p>1: Compare match condition has occurred since the last RTCSR register read operation.</p> <p>This bit is set by hardware on the CK_SECOND clock falling edge when the RTCCNT register value is equal to the RTCCMP register content. It is cleared by software reading this bit. This bit is suggested for access in the corresponding RTC interrupt routine – do not use software polling during software free running.</p>
[0]	CSECFLAG	<p>CK_SECOND Occurrence Flag</p> <p>0: CK_SECOND not occurred since the last RTCSR register read operation</p> <p>1: CK_SECOND has occurred since the last RTCSR register read operation</p> <p>This bit is set by hardware on the CK_SECOND clock falling edge. It is cleared by software reading this bit. This bit is suggested for access in the corresponding RTC interrupt routine – do not use software polling during software free running.</p>

RTC Interrupt and Wakeup Enable Register – RTCIWEN

This register contains the interrupt and wakeup enable bits.

Address: 0x010

Reset value: 0x0000_0000 (Reset by Backup Domain reset only)

31	30	29	28	27	26	25	24
Reserved							
Type/Reset							
Reserved							
Type/Reset							
15	14	13	12	11	10	9	8
Reserved					OVWEN	CMWEN	CSECWEN
Type/Reset					RW 0	RW 0	RW 0
7	6	5	4	3	2	1	0
Reserved					OVIEN	CMIEN	CSECIEN
Type/Reset					RW 0	RW 0	RW 0

Bits	Field	Descriptions
[10]	OVWEN	Counter Overflow Wakeup Enable 0: Counter overflow wakeup disabled 1: Counter overflow wakeup enabled
[9]	CMWEN	Compare Match Wakeup Enable 0: Compare match wakeup disabled 1: Compare match wakeup enabled
[8]	CSECWEN	Counter Clock CK_SECOND Wakeup Enable 0: Counter Clock CK_SECOND wakeup disabled 1: Counter Clock CK_SECOND wakeup enabled
[2]	OVIEN	Counter Overflow Interrupt Enable 0: Counter Overflow Interrupt disabled 1: Counter Overflow Interrupt enabled
[1]	CMIEN	Compare Match Interrupt Enable 0: Compare Match Interrupt disabled 1: Compare Match Interrupt enabled
[0]	CSECIEN	Counter Clock CK_SECOND Interrupt Enable 0: Counter Clock CK_SECOND Interrupt disabled 1: Counter Clock CK_SECOND Interrupt enabled

18 Watchdog Timer (WDT)

Introduction

The Watchdog Timer is a hardware timing circuitry that can be used to detect system failures due to software malfunctions. It includes a 12-bit down-counting counter, a prescaler, a WDT counter value register, a WDT delta value register, interrupt related circuits, WDT operation control circuitry and the WDT protection mechanism. The Watchdog Timer can be operated in an interrupt mode or a reset mode. The Watchdog Timer will generate an interrupt or a reset when the counter counts down and reaches a zero value. If the software does not reload the counter value before the Watchdog Timer underflow occurs, an interrupt or a reset will be generated when the counter underflows. In addition, an interrupt or reset is also generated if the software reloads the counter when the counter value is greater than or equal to the WDT delta value. That means the counter must be reloaded within a limited timing window using a specific method. The Watchdog Timer counter can be stopped while the processor is in the debug mode. The register write protection function can be enabled to prevent it from changing the configuration of the Watchdog Timer unexpectedly.

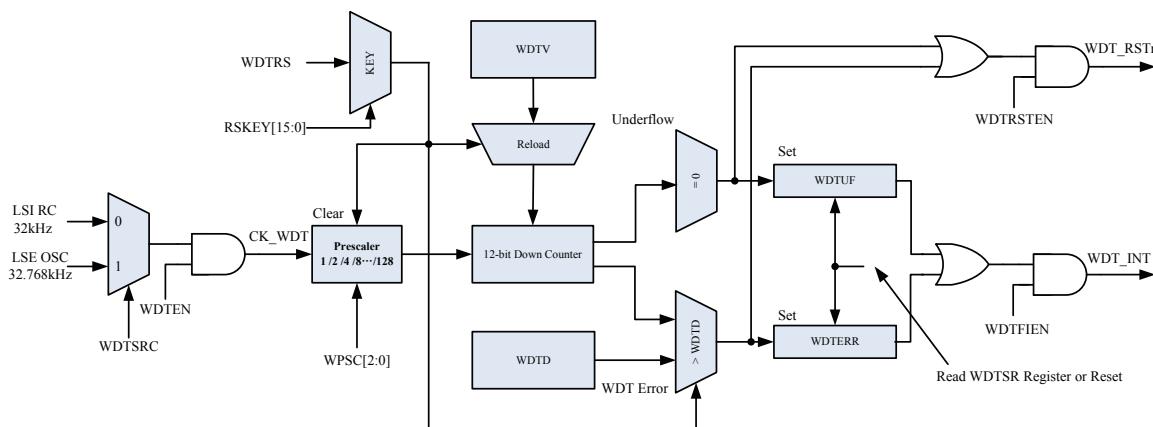


Figure 119. Watchdog Timer Block Diagram

Features

- Clock source from either internal 32kHz RC oscillator (LSI) or 32,768 Hz oscillator (LSE)
- Individually select to keep running or freeze when entering sleep or deep sleep mode 1
- 12-bit down counter with 3-bit prescaler
- Provides reset or interrupt signals to the system
- Limited reload window setting to prevent unsuitable Watchdog timer reload
- Watchdog Timer can be selected to be stopped or not while the processor is in the debug state
- Reload lock key to prevent unexpected operation
- Write protection function of configuration register (counter value, interrupt enable, reset enable, delta value, and prescaler)

Functional Descriptions

The Watchdog timer consists of a 7-stage prescaler and a 12-bit down-counter. The largest time-out period is about 16 seconds using the maximum prescaler value of (1/128).

The configurations of the counter reload value, the interrupt enable, the reset enable, the Delta value, and the prescaler selection in the WDTMR0 and WDTMR1 registers must be set properly before the Watchdog Timer starts to count. In order to prevent an unexpected write operation to those configurations, a register write protection function should be enabled by writing any value except the value 0x35CA to the PROTECT[15:0] bits in the WDTPR register. The value 0x35CA can be written into the PROTECT[15:0] bits to disable the register write protection function before accessing the configuration register. The read operation of the PROTECT[0] bit can obtain the enable/disable status of the register write protection function.

During normal operation, the Watchdog Timer counter should be reloaded before the counter underflows to avoid generating an interrupt or a reset. The 12-bit down counter can be reloaded with the Watchdog Timer Counter Value (WDTV) by setting WDTRS to 1 together with correct lock key 0x5FA0 specified in the WDTCR register.

If a software deadlock situation occurs in a task or a subroutine is contained within a WDT reload operation, then the reload operation will continue to function and a Watchdog Timer underflow reset or interrupt will not be generated. This will result in the software deadlock remaining undetected. To prevent this situation, the reload operation is designated to be executed when the WDT counter value is less than the WDT delta value, WDTD. A reload operation is only executed when the WDT counter value is greater than or equal to the WDT delta value which will then cause a Watchdog Timer error which generates an interrupt or reset depending on the related setting. With a proper WDT delta value being specified, if a software deadlock occurs in a task or if a subroutine is contained within a WDT reload operation, the WDT reload operation will not be executed and a WDT error interrupt or a WDT error reset will be generated to obtain CPU attention. However, the delta value feature described can be disabled by programming the WDTD to have a value greater than or equal to the WDTV value.

The WDTERR and the WDTUF flags in the WDTSTS register will be set respectively when the Watchdog Timer underflows or the Watchdog Timer error occurs. A system reset or the read operation of WDTSTS register clears the WDTERR and the WDTUF flags.

When the system enters the Sleep or Deep sleep mode 1, the Watchdog timer counter will either continue to count or stop depending on the WDTSHLT bits in the WDTMR0 register. The Watchdog stops counting when the WDTSHLT bits are set in the Sleep mode. The count value is retained so that it continues counting after the system is woken up from the Sleep mode. A Watchdog reset or interrupt will occur any time when the Watchdog timer is running and when it has an operating clock source. If a Watchdog interrupt occurs in the Sleep or Deep Sleep mode 1, it will wake up the device.

When the processor enters the debug mode, the Watchdog Timer counter will either continue to count or stop, depending on the DB_WDT bit configuration in the MCDBGCR register in the Clock Control Unit.

The Watchdog timer should be used in the following manners:

- Set the Watchdog timer reload value (WDTV) and reset/interrupt in WDTMR0 register.
- Set the Watchdog timer delta value (WDTD) and prescaler in WDTMR1 register.
- Start the Watchdog timer by writing WDTCR register with WDTRS = 1 and RSKEY = 0x5FA0.
- Write WDTPR register to lock all Watchdog Timer registers except WDTCR and WDTPR.
- The Watchdog Timer counter should be reloaded again within the delta value (WDTD).

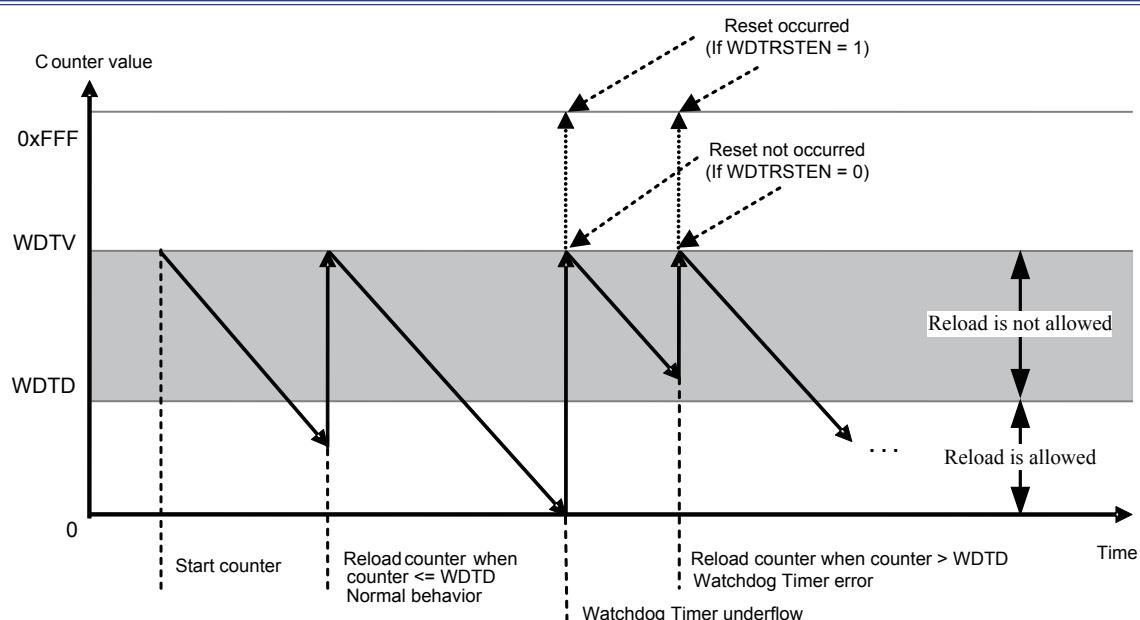


Figure 120. Watchdog Timer Behavior

Register Map

The following table shows the Watchdog Timer registers and reset values.

Table 44. WDT Register Map

Register	Offset	Description	Reset Value
Watchdog Timer Base Address = 0x4006_8000			
WDTCSR	0x000	Watchdog Timer Control Register	0x0000_0000
WDTMR0	0x004	Watchdog Timer Mode Register 0	0x0000_0FFF
WDTMR1	0x008	Watchdog Timer Mode Register 1	0x0000_7FFF
WDTSR	0x00C	Watchdog Timer Status Register	0x0000_0000
WDTPR	0x010	Watchdog Timer Protection Register	0x0000_0000
WDTCR	0x014	Watchdog Timer Counter Register	0x0000_0FFF
WDTCSR	0x018	Watchdog Timer Clock Selection Register	0x0000_0000

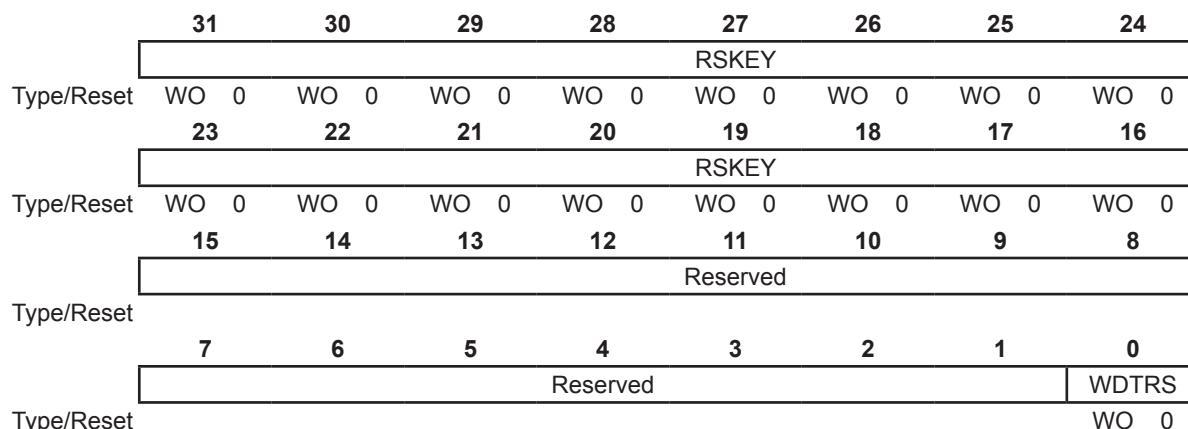
Register Descriptions

Watchdog Timer Control Register – WDTCSR

This register is used to reload Watchdog Timer.

Offset: 0x000

Reset value: 0x0000_0000



Bits	Field	Descriptions
[31:16]	RSKEY	Watchdog Timer Reload Lock Key The RSKEY [15:0] bits should be written with a value of 0x5FA0 to enable the WDT reload operation function. Writing any other value except 0x5FA0 in this field will abort the write operation.
[0]	WDTRS	Watchdog Timer Reload 0: No effect 1: Reload Watchdog Timer. This bit is used to reload the Watchdog Timer Counter with a WDTV value stored in the WDTMR0 register. It is set to 1 by software and cleared to 0 by hardware automatically.

Watchdog Timer Mode Register 0 – WDTMR0

This register specifies the Watchdog Timer counter reload value, interrupt enable and reset enable control.

Offset: 0x004

Reset value: 0x0000_0FFF

	31	30	29	28	27	26	25	24	
Type/Reset	Reserved								
	23	22	21	20	19	18	17	16	
Type/Reset	Reserved								
	15	14	13	12	11	10	9	8	
Type/Reset	WDTSHLT	WDTRSTEN	WDTFIEN	WDTV					
	RW 0	RW 0	RW 0	RW 0	RW 1	RW 1	RW 1	RW 1	
Type/Reset	7	6	5	4	3	2	1	0	
	WDTV								
Type/Reset	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	

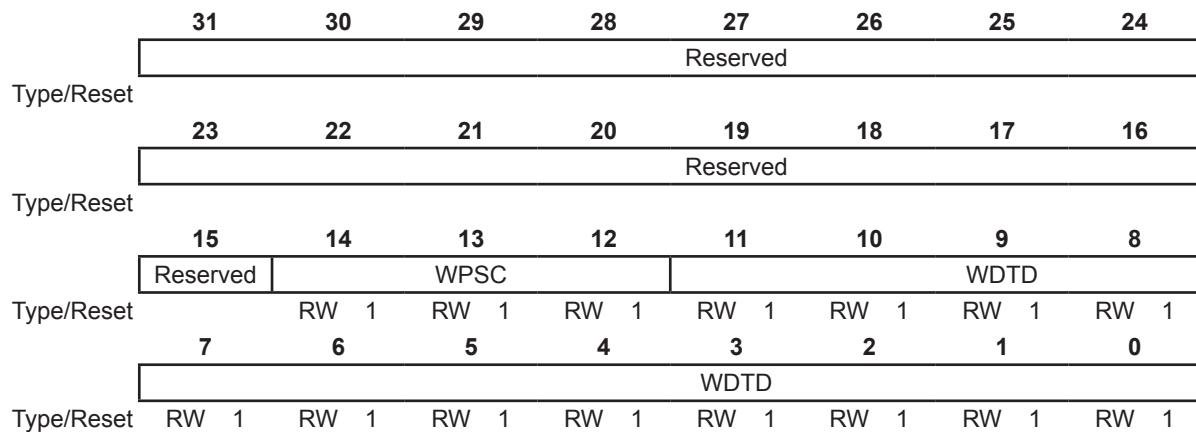
Bits	Field	Descriptions
[16]	WDTEN	Watchdog Timer Running Enable 0: Watchdog timer is disabled 1: Watchdog timer is enabled to run. When the Watchdog timer is disabled, the counter will be reset to its hardware default condition. When the WDTEN bit is set, the Watchdog timer will be reloaded with the WDTV value and count down.
[15:14]	WDTSHLT	Watchdog Timer Sleep Halt 00: The Watchdog runs when the system is in the Sleep mode or Deep Sleep mode 1 01: The Watchdog runs when the system is in the Sleep mode and halts in Deep Sleep mode 1 10 or 11: The Watchdog halts when the system is in the Sleep mode and Deep Sleep mode 1 Note that the Watchdog timer always halts when the system is in Deep Sleep mode 2. If a Watchdog interrupt occurs in Sleep or Deep Sleep mode 1, it will wake up the device. The Watchdog stops counting when the WDTSHLT bits are set in the Sleep mode. The count value is retained so that it continues counting after the system wakes up from the Sleep mode.
[13]	WDTRSTEN	Watchdog Timer Reset Enable 0: A Watchdog Timer underflow or error has no effect on the reset of system. 1: A Watchdog Timer underflow or error triggers a Watchdog Timer system reset.
[12]	WDTFIEN	Watchdog Timer Fault Interrupt Enable 0: A Watchdog Timer underflow or error has no effect on interrupt. 1: A Watchdog Timer underflow or error asserts an interrupt.
[11:0]	WDTV	Watchdog Timer Counter Value WDTV defines the value loaded in the 12-bit Watchdog down counter.

Watchdog Timer Mode Register 1 – WDTMR1

This register specifies the Watchdog delta value and the prescaler selection.

Offset: 0x008

Reset value: 0x0000_7FFF



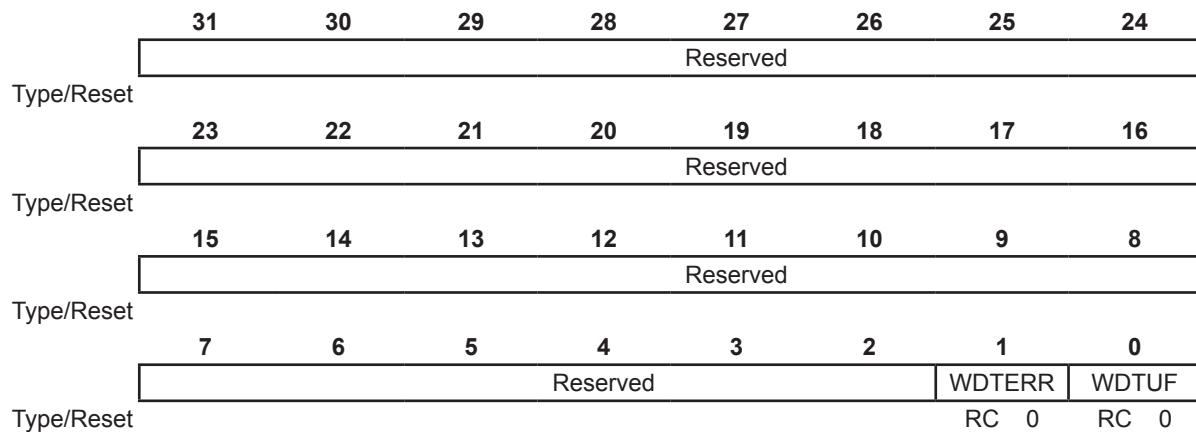
Bits	Field	Descriptions
[14:12]	WPSC	Watchdog Timer Prescaler Selection 000: 1/1 001: 1/2 010: 1/4 011: 1/8 100: 1/16 101: 1/32 110: 1/64 111: 1/128
[11:0]	WDTD	Watchdog Timer Delta Value WDTD is used to define the permitted range to reload the Watchdog Timer. If the Watchdog Timer counter value is less than the WDTD value, writing the WDTCR register with the setting including WDTRS = 1 and RSKEY = 0x5FA0 to execute a WDT reload operation will successfully reload the timer. If the Watchdog Timer value is greater than or equal to the WDTD value, writing the WDTCR register with the setting including WDTRS = 1 and RSKEY = 0x5FA0 to execute a WDT reload operation will cause a Watchdog Timer error. This feature can be disabled by programming the WDTD value to be greater than or equal to the WDTV value.

Watchdog Timer Status Register – WDTSR

This register specifies the Watchdog Timer status.

Offset: 0x00C

Reset value: 0x0000_0000



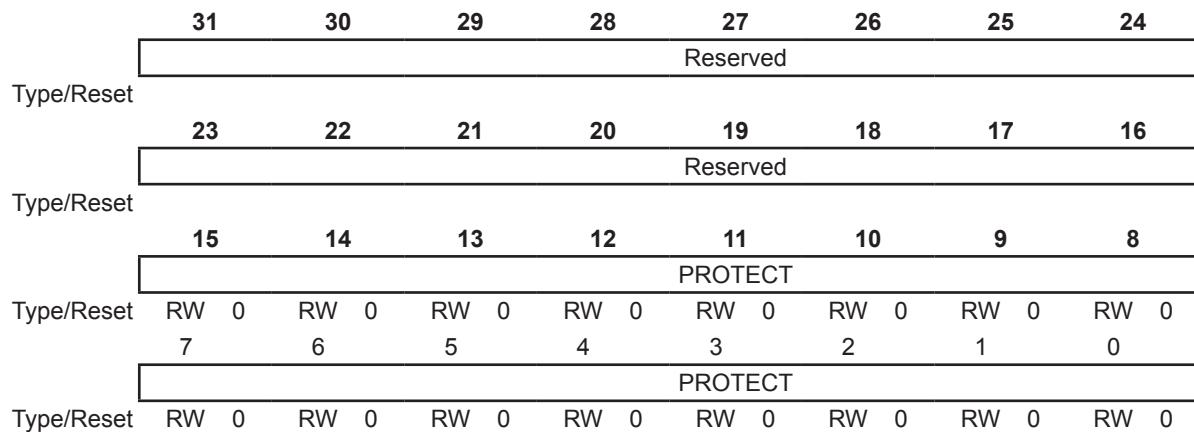
Bits	Field	Descriptions
[1]	WDTERR	<p>Watchdog Timer Error</p> <p>0: No Watchdog timer error occurred since the last read operation on this register</p> <p>1: Watchdog timer error occurred since the last read operation on this register</p> <p>Note: A reload operation will cause a Watchdog Timer error when the Watchdog Timer counter value is greater than or equal to the WDTD value</p>
[0]	WDTUF	<p>Watchdog timer Underflow</p> <p>0: No Watchdog Timer underflow occurred since the last read operation on this register</p> <p>1: Watchdog Timer underflow occurred since the last read operation on this register</p> <p>Note this bit is read clear flag.</p>

Watchdog Timer Protection Register – WDTPR

This register specifies the Watchdog Timer write protection key configuration.

Offset: 0x010

Reset value: 0x0000_0000



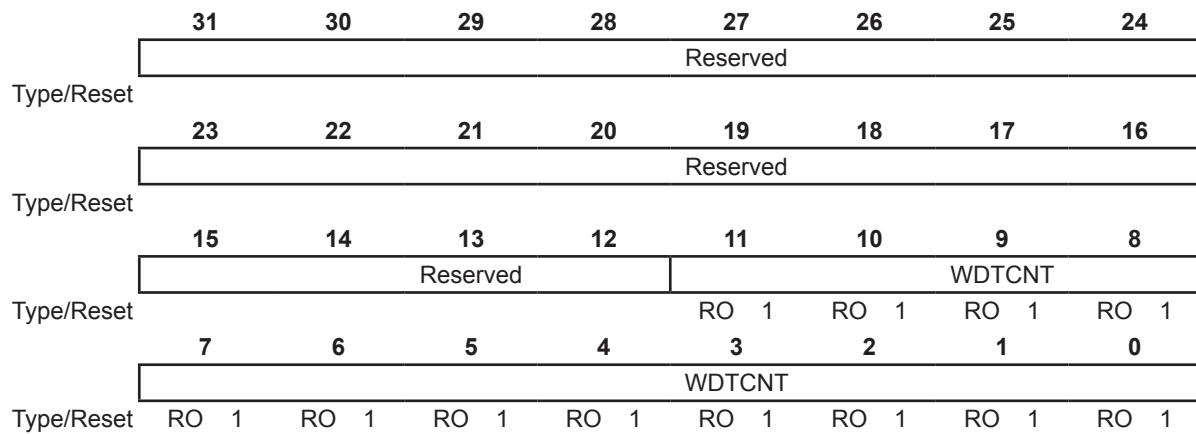
Bits	Field	Descriptions
[15:0]	PROTECT	<p>Watchdog Timer Register Protection</p> <p>For write operation:</p> <ul style="list-style-type: none"> 0x35CA: Disable the Watchdog Timer register write protection Others values: Enable the Watchdog Timer register write protection <p>For read operation:</p> <ul style="list-style-type: none"> 0x0000: Watchdog timer register write protection is disabled 0x0001: Watchdog timer register write protection is enabled <p>This register is used to enable or disable the write protection of WDTMR0 and WDTMR1 registers. Enable write protection will make WDTMR0 and WDTMR1 registers become read only to prevent any unexpected write operation. Read the WDTPR register to indicate if the write protection is enabled or not.</p>

Watchdog Timer Counter Register – WDTCNTR

This register specifies Watchdog Timer counter value configuration.

Offset: 0x014

Reset value: 0x0000_0FFF



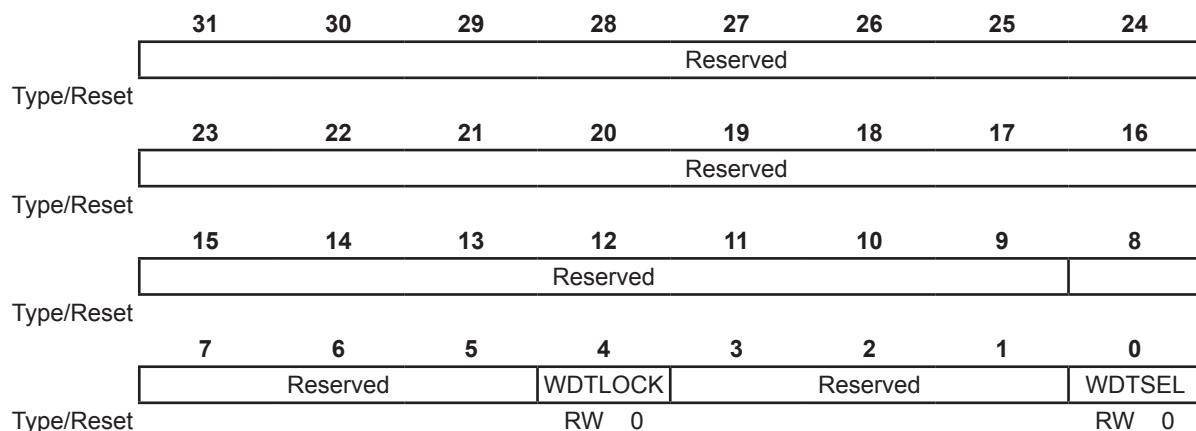
Bits	Field	Descriptions
[15:0]	WDTCNT	<p>Watchdog Timer Counter Value</p> <p>When reading the value of the 12-bit Watchdog timer, the synchronization procedure takes up to some CK_WDT cycles and PCLK cycles, so the value of WDTCNT is older than the actual value of the timer when it's being read by the CPU.</p>

Watchdog Timer Clock Selection Register – WDTCSR

This register specifies Watchdog Timer clock source selection and lock configuration.

Offset: 0x018

Reset value: 0x0000_0FFF



Bits	Field	Descriptions
[4]	WDTLOCK	<p>Watchdog Timer Lock Mode</p> <p>0: This bit is only set to 0 on any reset. It cannot be cleared by software.</p> <p>1: This bit is set once only by software and locks the Watchdog timer function.</p> <p>Software can set this bit to 1 at any time. Once the WDTLOCK bit is set, the function and registers of the Watchdog timer cannot be modified or disabled, including the Watchdog timer clock source, and only waits for a system reset to disable the lock mode.</p>
[0]	WDTSRC	<p>Watchdog Timer Clock Source Selection</p> <p>0: Internal 32kHz RC oscillator clock selected (LSI)</p> <p>1: External 32.768kHz crystal oscillator clock selected (LSE)</p> <p>Select using software to control the Watchdog timer clock source.</p>

19 Inter-Integrated Circuit (I²C)

Introduction

The I²C Module is an internal circuit allowing communication with an external I²C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line, SDA, and a serial clock line, SCL. The I²C module provides three data transfer rates: (1) 100 kHz in the Standard mode, (2) 400 kHz in the Fast mode and (3) 1MHz in the Fast-mode plus. The SCL period generation register is used to setup different kinds of duty cycle implementation for the SCL pulse.

The SDA line which is connected to the whole I²C bus is a bi-directional data line between the master and slave devices used for the transmission and reception of data. The I²C module also has an arbitration detection function to prevent the situation where more than one master attempts to transmit data on the I²C bus at the same time.

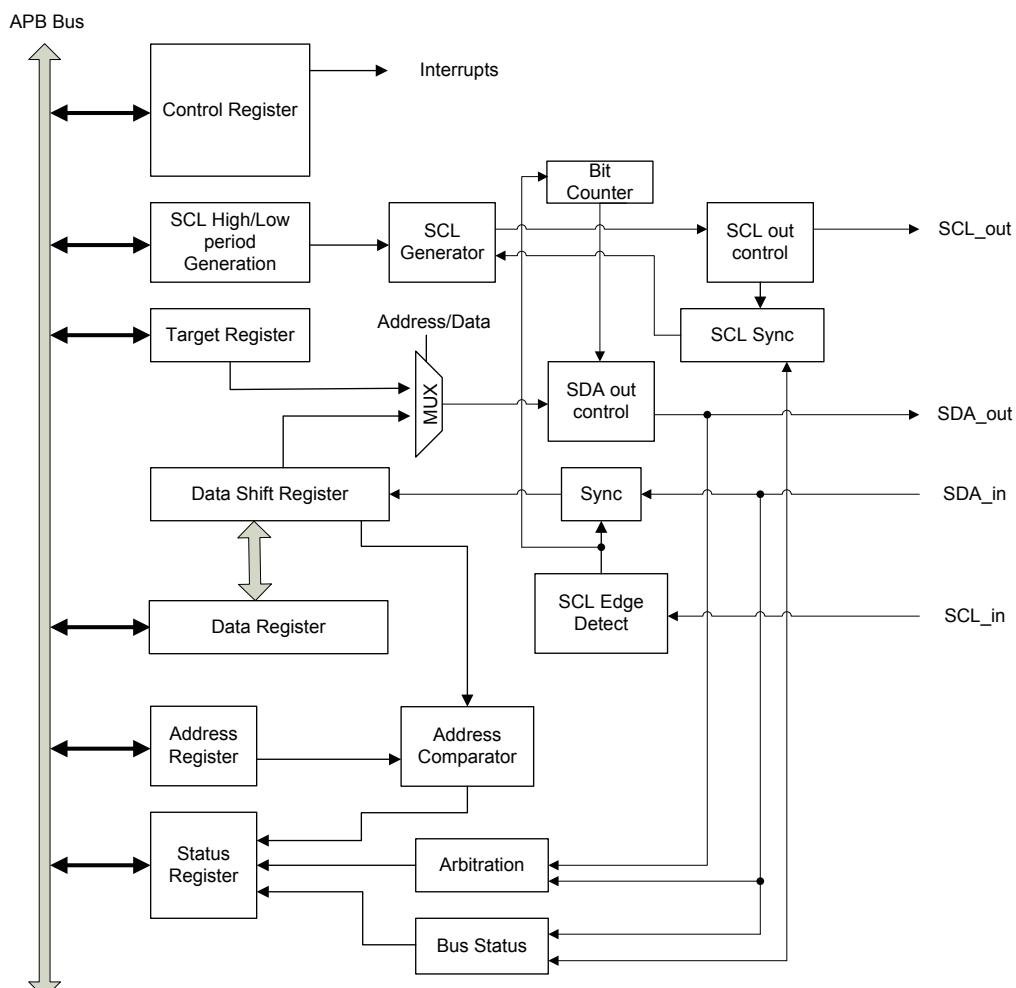


Figure 121. I²C Module Block Diagram

Features

- Two-wire I²C serial interface
 - Serial data line (SDA) and serial clock (SCL)
- Multiple speed modes
 - Standard mode – 100 kHz
 - Fast mode – 400 kHz
 - Fast mode plus – 1 MHz
- Bi-directional data transfer between master and slave
- Multi-master bus – no central master
 - The same interface can act as Master or Slave
- Arbitration among simultaneously transmitting masters without corrupting of serial data on the bus.
- Clock synchronization
 - Allow devices with different bit rates to communicate via one serial bus
- Supports 7-bit and 10-bit addressing mode and general call addressing.
- Multiple slave addresses using address mask function
- Time-out function
- Supports PDMA Interface

Functional Descriptions

Two Wire Serial Interface

The I²C module has two external lines, the serial data SDA and serial clock SCL lines, to carry information between the interconnected devices connected to the bus. The SCL and SDA lines are both bidirectional and must be connected to a pull-high resistor. When the I²C bus is in the free or idle state, both pins are at a high level to perform the required wired-AND function for multiple connected devices.

START and STOP Conditions

A master device can initialize a transfer by sending a START signal and terminate the transfer with a STOP signal. A START signal is usually referred to as the “S” bit, which is defined as a High to Low transition on the SDA line while the SCL line is high. A STOP signal is usually referred to as the “P” bit, which is defined as a Low to High transition on the SDA line while SCL is high.

A repeated START, which is denoted as the “Sr” bit, is functionally identical to the normal START condition. A repeated START signal allows the I²C interface to communicate with another slave device or with the same device but in a different transfer direction without releasing the I²C bus control.

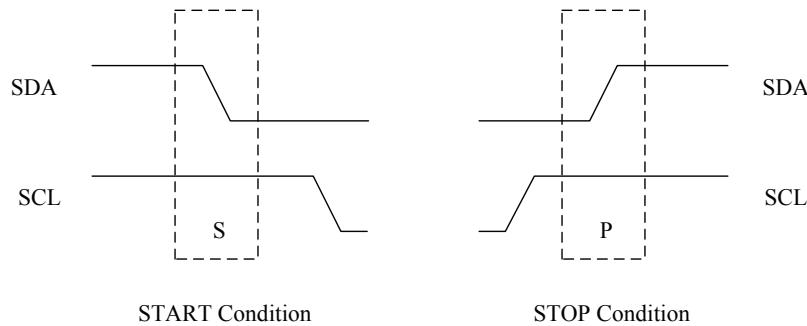


Figure 122. START and STOP Condition

Data Validity

The data on the SDA line must be stable during the high period of the SCL clock. The SDA data state can only be changed when the clock signal on the SCL line is in a low state.

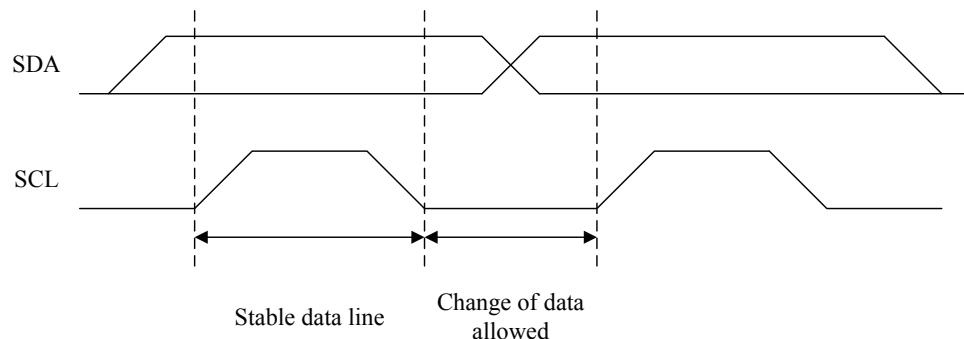


Figure 123. Data Validity

Addressing Format

The I²C interface starts to transfer data after the master device has sent the address to confirm the targeted slave device. The address frame is sent just after the START signal by master device. The addressing mode selection bit named ADRM in the I2CCR register should be defined to choose either the 7-bit or 10-bit addressing mode.

7-bits Address Format

The 7-bit address format is composed of the seven-bit length slave address, which the master device wants to communicate with a R/W bit and an ACK bit. The R/W bit defines the direction of the data transfer.

R/W=0 (Write): The master transmits data to the addressed slave.

R/W=1 (Read): The master receives data from the addressed slave.

The slave address can be assigned through the ADDR field in the I2CADDR register. The slave device sends back the acknowledge bit (ACK) if its slave address matches the transmitted address sent by master.

Note that it is forbidden to own the same address for two slave devices.

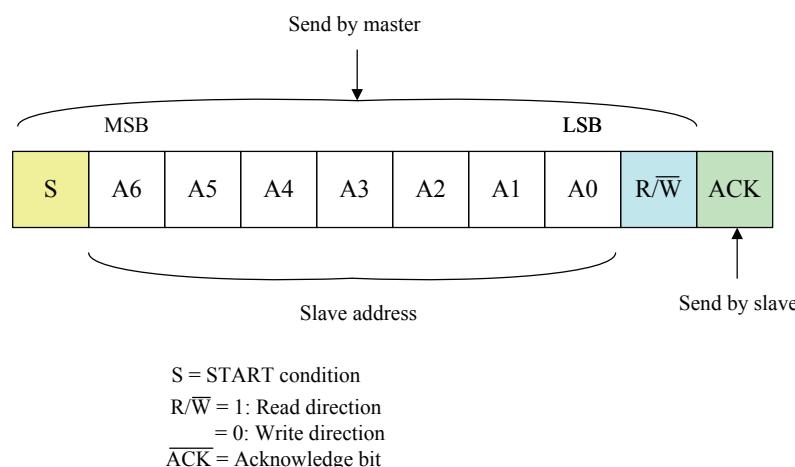


Figure 124. 7-bit Addressing Mode

10-bits Address Format

In order to prevent address clashes, due to the limited range of the 7-bit addresses, a new 10-bit address scheme has been introduced. This enhancement can be mixed with the 7-bit addressing mode which increases the available address range about ten times. For the 10-bit addressing mode, the first two bytes after a START signal include a header byte and an address byte that usually determines which slave will be selected by the master. The header byte is composed of a leading “11110”, 10th and 9th bits of the slave address. The second byte is the remaining 8 bit address of the slave device.

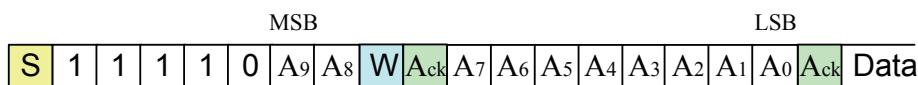


Figure 125. 10-bit Addressing Write Transmit Mode

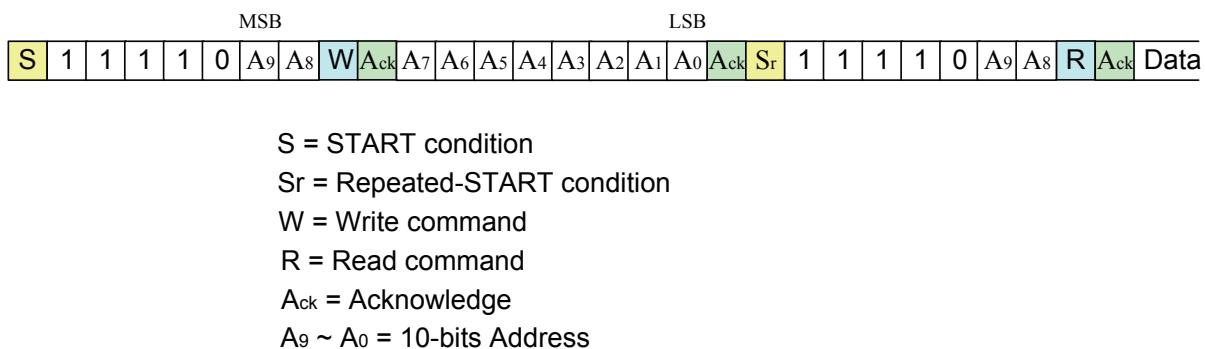


Figure 126. 10-bits Addressing Read Receive Mode

Data Transfer and Acknowledge

Once the slave device address has been matched, the data can be transmitted to or received from the slave device according to the transfer direction specified by the R/W bit. Each byte is followed by an acknowledge bit on the 9th SCL clock.

If the slave device returns a Not Acknowledge (NACK) signal to the master device, the master device can generate a STOP signal to terminate the data transfer or generate a repeated START signal to restart the transfer.

If the master device sends a Not Acknowledge (NACK) signal to the slave device, the slave device should release the SDA line for the master device to generate a STOP signal to terminate the transfer.

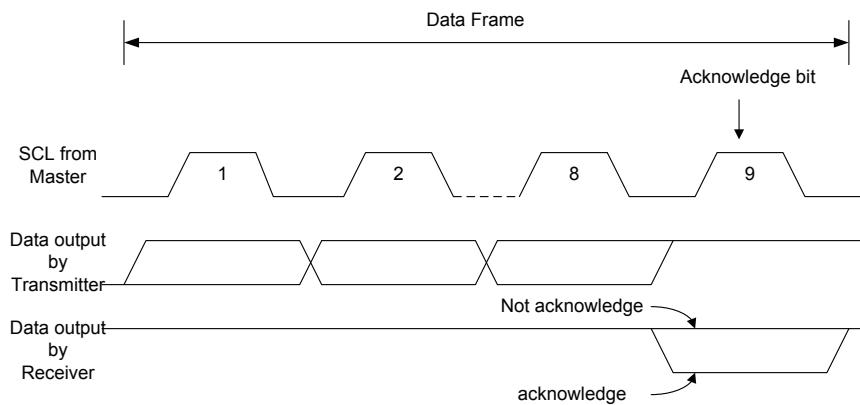


Figure 127. I²C Bus Acknowledge

Clock Synchronization

Only one master device can generate the SCL clock under normal operation. However when there is more than one master trying to generate the SCL clock, the clock should be synchronized so that the data output can be compared. Clock synchronization is performed using the wired-AND connection of the I²C interface to the SCL line.

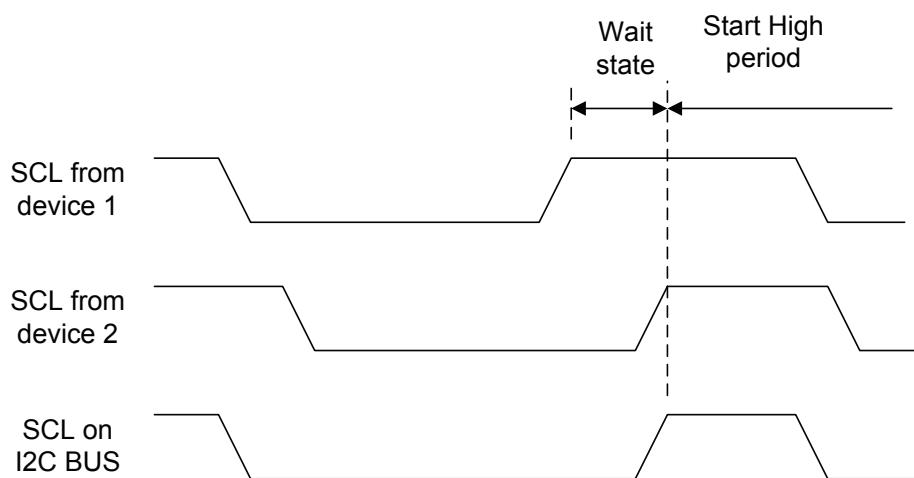


Figure 128. Clock Synchronization during Arbitration

Arbitration

A master may start a transfer only if the I²C bus line is in the free or idle mode. If two or more masters generate a START signal at approximately the same time, an arbitration procedure will occur.

Arbitration takes place on the SDA line and can continue for many bits. The arbitration procedure gives a higher priority to the device that transmits serial data with a binary low bit (logic low). Other master devices which want to transmit binary high bits (logic high) will lose the arbitration. As soon as a master loses the arbitration, the I²C module will set the ARBLOS bit in the I2CSR register and generate an interrupt if the interrupt enable bit, ARBLSIEN, in the I2CIER register is set to 1. Meanwhile, it stops sending data and listens to the bus in order to detect an I²C stop signal. When the stop signal is detected, the master which has lost the arbitration may try to access the bus again.

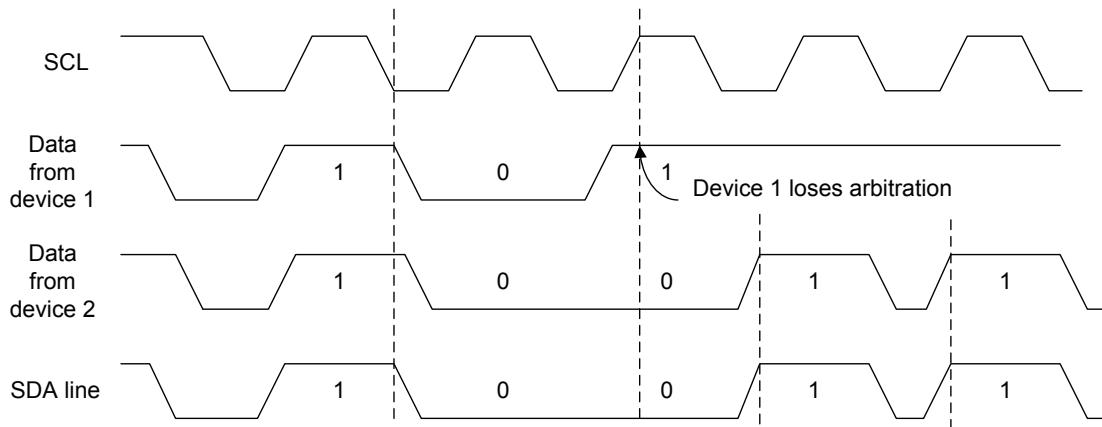


Figure 129. Two Master Arbitration Procedure

General Call Address

The general call addressing function can be used to address all the devices connected to the I²C bus. The master device can activate the general call function by writing a value “00” into the TAR and setting the RWD bit to 0 in the I2CTAR register on the addressing frame.

The device can support the general call addressing function by setting the corresponding enable control bit GCEN to 1. If the GCEN bit is set to 1 to support the general call addressing, the AA bit in the I2CCR register should also be set to 1 to send an acknowledge signal back when the device receives an address frame with a value of 00H. When this condition occurs, the general call flag, GCS, will be set to 1, but the ADRS flag will not be set.

Bus Error

If an unpredictable START or STOP condition occurs when the data is being transferred on the I²C bus, it will be considered as a bus error and the transferring data will be aborted. When a bus error event occurs, the relevant bus error flag BUSERR in the I2CSR register will set to 1 and both the SDA and SCL lines are released. The BUSERR flag should be cleared by writing a 1 to it to initiate the I²C module to an idle state.

Address Mask Enable

The I²C module provides address mask function for user to decide which address bit can be ignored during the comparison with the address frame sent from the master. The ADRS flag will be asserted when the unmasked address bits and the address frame sent from the master are matched. Note that this function is only available in the slave mode.

For instance, the user sets a data transfer with 7-bit addressing mode together with the I2CADDMR register value as 0x05h and the I2CADDR register value as 0x55h, this means if an address which is sent by an I²C master on the bus is equal to 0x50h, 0x51h, 0x54h or 0x55h, the I²C slave address will all be considered to be matched and the ADRS flag in the I2CSR register will be asserted after the address frame.

Address Snoop

The Address Snoop register, I2CADDSSR, is used to monitor the calling address on the I²C bus during the whole data transfer operation no matter if the I²C module operates as a master or a slave device. Note that the I2CADDSSR register is a read only register and each calling address on the I²C bus will be stored in the I2CADDSSR register automatically even if the I²C device is not addressed.

Operation Mode

The I²C module can operate in one of the following modes:

- Master Transmitter
- Master Receiver
- Slave Transmitter
- Slave Receiver

The I²C module operates in the slave mode by default. The interface will switch to the master mode automatically after generating a START signal.

Master Transmitter Mode

Start condition

Users write the target slave device address and communication direction into the I2CTAR register after setting the I2CEN bit in the I2CCR register. The STA flag in the I2CSR register is set by hardware after a start condition occurs. In order to send the following address frame, the STA flag must be cleared to 0 if it has been set to 1. The STA flag is cleared by reading the I2CSR register.

Address Frame

The ADRS flag in the I2CSR register will be set after the address frame is sent by the master device and the acknowledge signal from the address matched slave device is received. In order to send the following data frame, the ADRS flag must be cleared to 0 if it has been set to 1. The ADRS bit is cleared by reading the I2CSR register.

Data Frame

The data to be transmitted to the slave device must be transferred to the I2CDR register.

The TXDE bit in the I2CSR register is set to indicate that the I2CDR register is empty, which results in the SCL line being held at a logic low state. New data must then be transferred to the I2CDR register to continue the data transfer process. Writing a data into the I2CDR register will clear the TXDE flag.

Close / Continue Transmission

After transmitting the last data byte, the STOP bit in the I2CCR register can be set to terminate the transmission or re-assign another slave device by configuring the I2CTAR register to restart a new transfer.

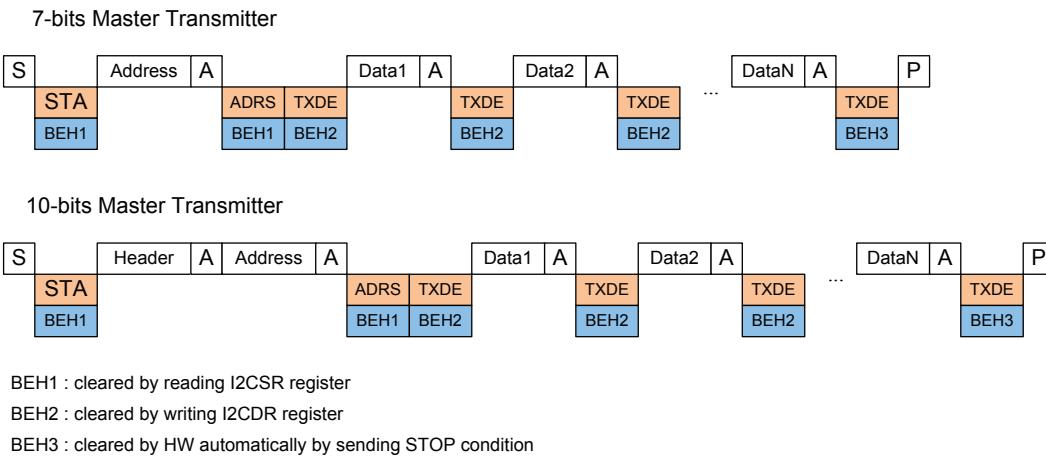


Figure 130. Master Transmitter Timing Diagram

Master Receiver Mode

Start condition

The target slave device address and communication direction must be written into the I2CTAR register. The STA flag in the I2CSR register is set by hardware after a start condition occurs. In order to send the following address frame, the STA flag must be cleared to 0 if it has been set to 1. The STA flag is cleared by reading the I2CSR register.

Address Frame

In the 7-bit addressing mode: The ADRS flag is set after the address frame is sent by the master device and the acknowledge signal from the address matched slave device is received. In order to receive the following data frame, the ADRS bit must be cleared to 0 if it has been set to 1. The ADRS bit is cleared after reading the I2CSR register.

In the 10-bit addressing mode: The ADRS bit in the I2CSR register will be set twice in the 10-bit addressing mode. The first time the ADRS bit is set is when the 10-bit address is sent and the acknowledge signal from the slave device is received. The second time the ADRS bit is set is when the header byte is sent and the slave acknowledge signal is received. In order to receive the following data frame, the ADRS bit must be cleared to 0 if it has been set to 1. The ADRS bit is cleared after reading the I2CSR register. The detailed master receiver mode timing diagram is shown in the following figure.

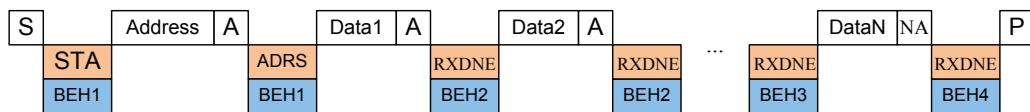
Data Frame

In the master receiver mode, data is transmitted from the slave device. Once a data is received by the master device, the RXDNE flag in the I2CSR register is set but it will not hold the SCL line. However, if the device receives a complete new data byte and the RXDNE flag has already been set to 1, the RXBF bit in the I2CSR register will be set to 1 and the SCL line will be held at a logic low state. When this situation occurs, data from the I2CDR register should be read to continue the data transfer process. The RXDNE flag can be cleared after reading the I2CDR register.

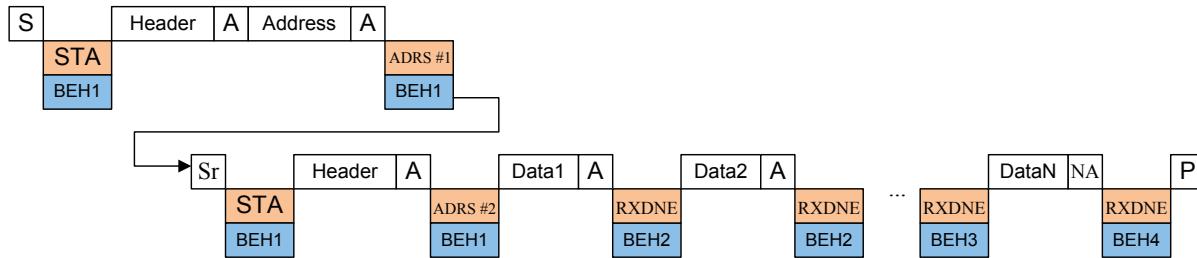
Close / Continue Transmission

The master device needs to reset the AA bit in the I2CCR register to send a NACK signal to the slave device before the last data byte transfer has been completed. After the last data byte has been received from the slave device, the master device will hold the SCL line at a logic low state following after a NACK signal sent by the master device to the slave device. The STOP bit can be set to terminate the data transfer process or re-assign the I2CTAR register to restart a new transfer.

7-bits Master Receiver



10-bits Master Receiver



BEH1 : cleared by reading I2CSR register

BEH2 : cleared by reading I2CDR register

BEH3 : cleared by reading I2CDR register, set AA=0 to send NACK signal

BEH4 : cleared by reading I2CDR register, set STOP=1 to send STOP signal

Figure 131. Master Receiver Timing Diagram

Slave Transmitter Mode

Address Frame

In the 7-bit addressing mode, the ADRS bit in the I2CSR register is set after the slave device receives the calling address which matches with the slave device address. In the 10-bit addressing mode, the ADRS bit is set when the first header byte is matched and the second address byte is matched respectively. After the ADRS bit has been set to 1, it must be cleared to 0 to continue the data transfer process. The ADRS bit is cleared after reading the I2CSR register.

Data Frame

In the Slave transmitter mode, the TXDE bit is set to indicate that the I2CDR is empty, which results in the SCL line being held at a logic low state. New transmission data must then be written into the I2CDR register to continue the data transfer process. Writing a data into the I2CDR register will clear the TXDE bit.

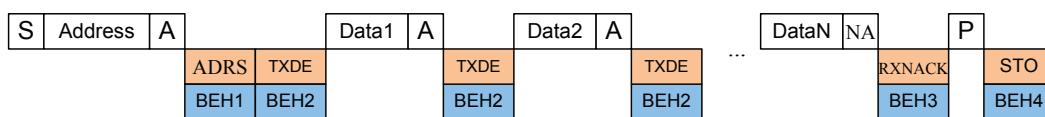
Receive Not-Acknowledge

When the slave device receives a Not-Acknowledge signal, the RXNACK bit in the I2CSR Register is set but it will not hold the SCL line. Writing “1” to RXNACK will clear the RXNACK flag.

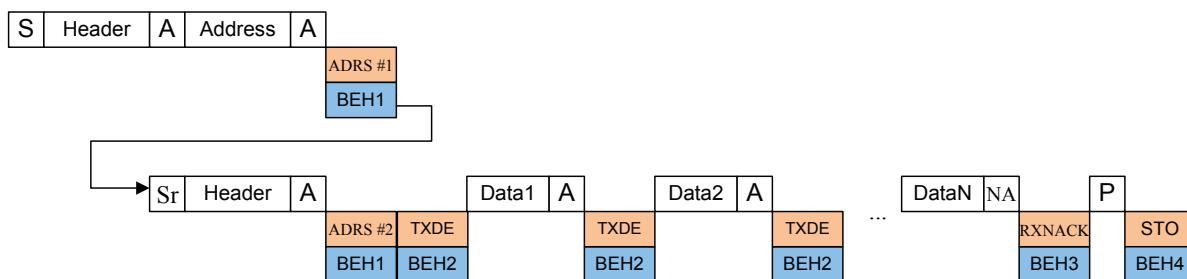
STOP Condition

When the slave device detects a STOP condition, the STO bit in the I2CSR register is set to indicate that the I²C interface transmission is terminated. Reading the I2CSR register can clear the STO flag.

7-bits Slave Transmitter



10-bits Slave Transmitter



BEH1 : cleared by reading I2CSR register

BEH2 : cleared by writing I2CDR register

BEH3 : cleared by writing 1 clear for RXNACK flag, TXDE is not set when NACK is received.

BEH4 : cleared by reading I2CSR register

Figure 132. Slave Transmitter Timing Diagram

Slave Receiver Mode

Address Frame

The ADRS bit in the I2CSR register is set after the slave device receives the calling address which matches with the slave device address. After the ADRS bit has been set to 1, it must be cleared to 0 to continue the data transfer process. The ADRS flag is cleared after reading the I2CSR register.

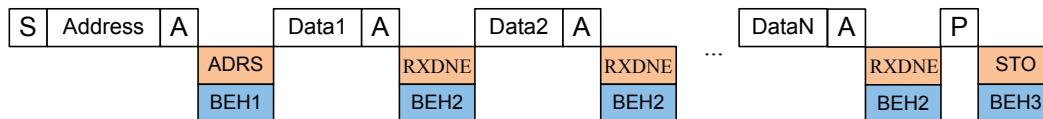
Data Frame

In the slave receiver mode, the data is transmitted from the master device. Once a data byte is received by the slave device, the RXDNE flag in the I2CSR register is set but it will not hold the SCL line. However, if the device receives a complete new data byte and the RXDNE bit has been set to 1, the RXBF bit in the I2CSR register will be set to 1 and the SCL line will be held at a logic low state. When this situation occurs, data from the I2CDR register should be read to continue the data transfer process. The RXDNE flag bit can be cleared after reading the I2CDR register.

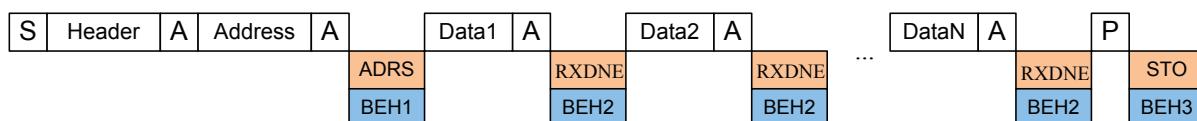
STOP condition

When the slave device detects a STOP condition, the STO flag bit in the I2CSR register is set to indicate that the I²C interface transmission is terminated. Reading the I2CSR register can clear the STO flag bit.

7-bits Slave Receiver



10-bits Slave Receiver



BEH1 : cleared by reading I2CSR register

BEH2 : cleared by reading I2CDR register

BEH3 : cleared by reading I2CSR register

Figure 133. Slave Receiver Timing Diagram

Conditions of Holding SCL Line

The following conditions will cause the SCL line to be held at a logic low state by hardware resulting in all the I²C transfers being stopped. Data transfer will be continued after the creating conditions are eliminated.

Table 45. Conditions of Holding SCL line

Type	Condition	Description	Eliminated
Flag	TXDE	I ² C is used in transmitted mode and I2CDR register needs to have data to transmit. (Note: TXDE won't be assert after receiving a NACK)	Master case: Writing data to I2CDR register Set TAR Set STOP Slave case: Writing data to I2CDR register
	GCS	I ² C is addressed as slave through general call	Reading I2CSR register
	ADRS	Master: I ² C is sent over address frame and is returned an ACK from slave (Note: Reference Fig.11 and Fig.12) Slave: I ² C is addressed as slave device (Note: Reference Fig.13 and Fig.14)	Reading I2CSR register
	STA	Master send START signal	Reading I2CSR register
	RXBF	Received a complete new data and meanwhile the RXDNE flag has been set already before.	Reading I2CDR register
Event	Master receives NACK	No matter in address or data frame, once received a NACK signal will hold SCL line in master mode.	Set TAR Set STOP
	Master send NACK used in received mode	Occurred when receiving the last data byte in Master received mode (Note: Reference Fig.11, and RXNACK flag won't be assert at this case)	Set TAR Set STOP

I²C Timeout Function

In order to reduce the occurrence of I²C lockup problem due to the reception of erroneous clock source, a timeout function is provided. If the I²C bus clock source is not received for a certain timeout period, then a corresponding I²C timeout flag will be asserted. This timeout period is determined by a 16-bit down-counting counter with a programmable preload value. The timeout counter is driven by the I²C timeout clock, f_{I²CTO}, which is specified by the timeout prescaler field in the I2CTOUT register. The TOUT field in the I2CTOUT register is used to define the timeout counter preload value. The timeout function is enabled by setting the ENTOUT bit in the I2CCR register. The timeout counter will start to count down from the preloaded value if the ENTOUT bit is set to 1 and one of the following conditions occurs:

- The I²C master module sends a START signal.
- The I²C slave module detects a START signal.
- The RXBF, TXDE, RXDNE, RXNACK, GCS or ADRS flags are asserted.

The timeout counter will stop counting when the ENTOUT bit is cleared. However, the counter will also stop counting when the conditions, listed as follows occur:

- The I²C slave module is not addressed.
- The I²C slave module detects a STOP signal.
- The I²C master module sends a STOP signal.
- The ARBLOS or BUSERR flags in the I2CSR register are asserted.

If the timeout counter underflows, the corresponding timeout flag, TOUTF, in the I2CSR register will be set to 1 and a timeout interrupt will be generated if the relevant interrupt is enabled.

PDMA Interface

The PDMA interface is integrated in the I²C module. The PDMA function can be enabled by setting the TXDMAE or RXDMAE bit to 1 in the transmitter or receiver mode respectively. When the data register is empty in the transmitter mode and the TXDMAE bit is set to 1, the PMDA function will be activated to move data from a certain memory location into the I²C data register. Similarly, when the data register is not empty in the receiver mode and the RXDMAE bit is set to 1, the PDMA function will also be activated to move data from the I²C data register to a specific memory location.

The DMA NACK control bit, DMANACK, is used to determine whether the NACK signal is sent or not when the I²C module operates in the master receiver mode and the PDMA function is enabled. If the DMANACK bit is set to 1 and the data has all been received and moved using the PDMA interface, a NACK signal will automatically be sent out to properly terminate the data transfer.

For a more detailed description on the PDMA configurations, refer to the PDMA chapter.

Register Map

The following table shows the I²C registers and reset values.

Table 46. I²C Register Map

Register	Offset	Description	Reset Value
I²C0 Base Address = 0x4004_8000			
I²C1 Base Address = 0x4004_9000			
I2CnCR	0x000	I ² Cn Control Register	0x0000_2000
I2CnIER	0x004	I ² Cn Interrupt Enable Register	0x0000_0000
I2CnADDR	0x008	I ² Cn Address Register	0x0000_0000
I2CnSR	0x00C	I ² Cn Status Register	0x0000_0000
I2CnSHPGR	0x010	I ² Cn SCL High Period Generation Register	0x0000_0000
I2CnSLPGR	0x014	I ² Cn SCL Low Period Generation Register	0x0000_0000
I2CnDR	0x018	I ² Cn Data Register	0x0000_0000
I2CnTAR	0x01C	I ² Cn Target Register	0x0000_0000
I2CnADDMR	0x020	I ² Cn Address Mask Register	0x0000_0000
I2CnADDSSR	0x024	I ² Cn Address Snoop Register	0x0000_0000
I2CnTOUT	0x028	I ² Cn Timeout Register	0x0000_0000

Register Descriptions

I²Cn Control Register – I2CnCR, n = 0 or 1

This register specifies the corresponding I²Cn function enable control.

Offset: 0x000

Reset value: 0x0000_2000

	31	30	29	28	27	26	25	24	
Type/Reset	Reserved								
	23	22	21	20	19	18	17	16	
Type/Reset	Reserved								
	15	14	13	12	11	10	9	8	
Type/Reset	RW	0	RW	0	RW	1	RW	0	
	7	6	5	4	3	2	1	0	
Type/Reset	ADRM	Reserved			I2CEN	GCEN	STOP	AA	
	RW	0				RW	0	RW	0

Bits	Field	Descriptions
[14:15]	SEQ_FILTER	SDA or SCL input sequential filter configuration bits 00: Sequential filter disable 01: 1 PCLK glitch filter 10 or 11: 2 PCLK glitch filter Note: This setting would affect the frequency of SCL. Detail is described in I2CSLPG register.
[13]	COMB_FILTER_En	SDA or SCL input combinational filter enable bit 0: Combinational filter Disable 1: Combinational filter Enable
[12]	ENTOUT	I ² C Timeout Function Enable Control 0: Timeout Function disabled 1: Timeout Function enabled This bit is used to enable or disable the I ² C timeout function. When the I2CEN bit is cleared to 0, the ENTOUT bit will be automatically cleared to 0 by hardware. It is recommended that users have to properly configure the PSC and TOUT fields in the I2CnTOUT register before the timeout counter starts to count by setting the ENTOUT bit to 1.
[10]	DMANACK	DMA Mode NACK Control 0: No operation 1: The I ² C master receiver module sends a NACK signal automatically after receiving the last byte from the slave transmitter in the DMA mode When the I2CEN bit is cleared to 0, the DMANACK bit is automatically cleared to 0 by hardware.

Bits	Field	Descriptions
[9]	RXDMAE	DMA Mode RX Request Enable Control 0: RX DMA request disabled 1: RX DMA request enabled If the data register is not empty in the receiver mode and the RXDMAE bit is set to 1, the relevant PDMA channel will be activated to move the data from the data register to a specific location which is defined in the corresponding PDMA register. When the I2CEN bit is cleared to 0, the RXDMAE bit is automatically cleared to 0 by hardware.
[8]	TXDMAE	DMA Mode TX Request Enable Control 0: TX DMA request disabled 1: TX DMA request enabled If the data register is empty in the transmitter mode and the Txdmae bit is set to 1, the relevant PDMA channel will be activated to move the data from a specific location defined in the related PDMA register to the data register. When the I2CEN bit is cleared to 0, the Txdmae bit is automatically cleared to 0 by hardware.
[7]	ADRM	Addressing Mode 0: 7-bit addressing mode 1: 10-bit addressing mode When the I ² C master/slave module operates in the 7-bit addressing mode, it can only send out and respond to a 7-bit address and vice versa. When the I2CEN bit is disabled, the ADRM bit is automatically cleared to 0 by hardware.
[3]	I2CEN	I ² C Interface Enable 0: I ² C interface disabled 1: I ² C interface enabled
[2]	GCEN	General Call Enable 0: General call disabled 1: General call enabled When the device receives the calling address with a value of 0x00 and if both the GCEN and the AA bits are set to 1, then the I ² C interface is addressed as a slave and the GCS bit in the I2CSR register is set to 1. When the I2CEN bit is cleared to 0, the GCEN bit is automatically cleared to 0 by hardware.
[1]	STOP	STOP Condition Control 0: No action 1: Send a STOP condition in master mode This bit is set to 1 by software to generate a STOP condition and automatically cleared to 0 by hardware. The STOP bit is only available for the master device.
[0]	AA	Acknowledge Bit 0: Send a Not Acknowledge (NACK) signal after a byte is received 1: Send an Acknowledge (ACK) signal after a byte is received When the I2CEN bit is cleared to 0, the AA bit is automatically cleared to 0 by hardware.

I²Cn Interrupt Enable Register – I²CnIER, n = 0 or 1

This register specifies the corresponding I²Cn interrupt enable bits.

Offset: 0x004

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Reserved								
Type/Reset	23	22	21	20	19	18	17	16
	Reserved					RXBFIE	TXDEIE	RXDNEIE
Type/Reset	15	14	13	12	11	10	9	8
	Reserved				TOUTIE	BUSERRIE	RXNACKIE	ARBLOSIE
Type/Reset	7	6	5	4	3	2	1	0
	Reserved				GCSIE	ADRSIE	STOIE	STAIE
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[18]	RXBFIE	RX Buffer Full Interrupt Enable Bit 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware.
[17]	TXDEIE	Data Register Empty Interrupt Enable Bit in Transmitter Mode 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware.
[16]	RXDNEIE	Data Register Not Empty Interrupt Enable Bit in Receiver Mode 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware.
[11]	TOUTIE	Timeout Interrupt Enable Bit 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware.
[10]	BUSERRIE	Bus Error Interrupt Enable Bit 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware.
[9]	RXNACKIE	Received Not Acknowledge Interrupt Enable Bit 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware.

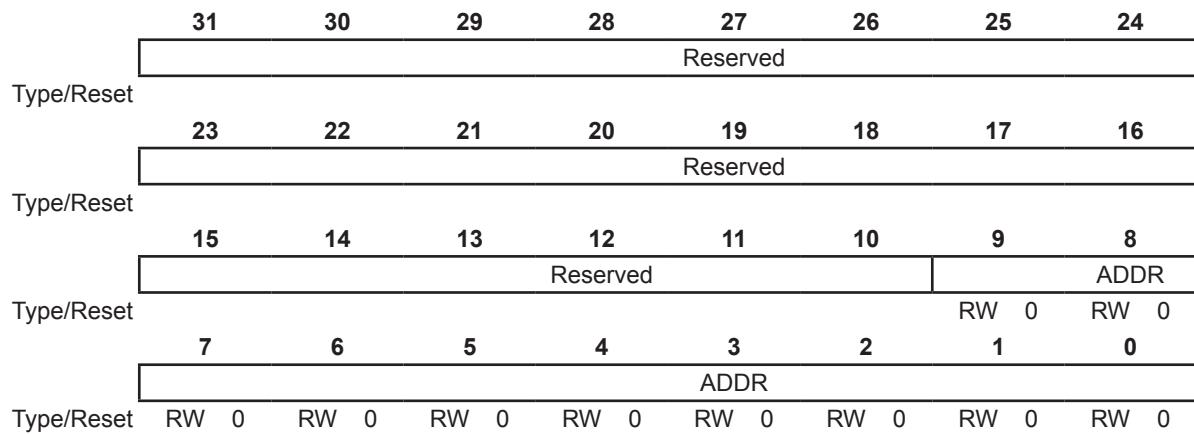
Bits	Field	Descriptions
[8]	ARBLOSIE	Arbitration Loss Interrupt Enable Bit in the I ² C multi-master mode 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware.
[3]	GCSIE	General Call Slave Interrupt Enable Bit 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware.
[2]	ADRSIE	Slave Address Match Interrupt Enable Bit 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware.
[1]	STOIE	STOP Condition Detected Interrupt Enable Bit 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware. The bit is used for the I ² C slave mode only.
[0]	STAIE	START Condition Transmit Interrupt Enable Bit 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware. The bit is used for the I ² C master mode only.

I²Cn Address Register – I²CnADDR, n = 0 or 1

This register specifies the I²Cn device address.

Offset: 0x008

Reset value: 0x0000_0000



Bits	Field	Descriptions
[9:0]	ADDR	Device Address The register indicates the I ² C device address. When the I ² C device is used in the 7-bit addressing mode, only the ADDR[6:0] bits will be compared with the received address sent from the I ² C master device.

I²Cn Status Register – I²CnSR, n = 0 or 1

This register contains the I²Cn operation status.

Offset: 0x00C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Reserved								
Type/Reset								
	23	22	21	20	19	18	17	16
Reserved TXNRX MASTER BUSBUSY RXBF TXDE RXDNE								
Type/Reset RO 0								
	15	14	13	12	11	10	9	8
Reserved TOUTF BUSERR RXNACK ARBLOS								
Type/Reset WC 0 WC 0 WC 0 WC 0 WC 0								
	7	6	5	4	3	2	1	0
Reserved GCS ADRS STO STA								
Type/Reset RC 0 RC 0 RC 0 RC 0 RC 0								

Bits	Field	Descriptions
[21]	TXNRX	Transmitter / Receiver Mode 0: Receiver mode 1: Transmitter mode Read only bit.
[20]	MASTER	Master Mode 0: I ² C is in the slave mode or idle 1: I ² C is in the master mode The I ² C interface is switched as a master device on the I ² C bus when the I2CTAR register is assigned and the I ² C bus is idle. The MASTER bit is cleared by hardware when software disables the I ² C bus by clearing the I2CEN bit to 0 or sends a STOP condition to the I ² C bus or the bus error is detected. This bit is set and cleared by hardware and is a read only bit.
[19]	BUSBUSY	Bus Busy 0: I ² C bus is idle 1: I ² C bus is busy The I ² C interface hardware starts to detect the I ² C bus status if the interface is enabled by setting the I2CEN bit to 1. It is set to 1 when the SDA or SCL signal is detected to have a logic low state and cleared when a STOP condition is detected.
[18]	RXBF	Buffer Full Flag in Receiver Mode 0: Data buffer is not full 1: Data buffer is full This bit is set when the data register I2CDR has already stored a data byte and meanwhile the data shift register also has been received a complete new data byte. The RXBF bit is cleared by software reading the I2CDR register.

Bits	Field	Descriptions
[17]	TXDE	<p>Data Register Empty in Transmitter Mode</p> <ul style="list-style-type: none"> 0: Data register I2CDR not empty 1: Data register I2CDR empty <p>This bit is set when the I2CDR register is empty in the Transmitter mode. Note that the TXDE bit will be set after the address frame is being transmitted to inform that the data to be transmitted should be loaded into the I2CDR register. The TXDE bit is cleared by software writing data to the I2CDR register in both the master and slave mode or cleared automatically by hardware after setting the STOP signal to terminate the data transfer or setting the I2CTAR register to restart a new data transfer in the master mode.</p>
[16]	RXDNE	<p>Data Register Not Empty in Receiver Mode</p> <ul style="list-style-type: none"> 0: Data register I2CDR empty 1: Data register I2CDR not empty <p>This bit is set when the I2CDR register is not empty in the receiver mode. The RXDNE bit is cleared by software reading the data byte from the I2CDR register.</p>
[11]	TOUTF	<p>Timeout Counter Underflow Flag</p> <ul style="list-style-type: none"> 0: No timeout counter underflow occurred 1: Timeout counter underflow occurred <p>Writing “1” to this bit will clear the TOUTF flag.</p>
[10]	BUSERR	<p>Bus Error Flag</p> <ul style="list-style-type: none"> 0: No bus error has occurs 1: Bus error has occurred <p>This bit is set by hardware when the I²C interface detects a misplaced START or STOP condition in a transfer process. Writing a “1” to this bit will clear the BUSERR flag.</p> <p>In Master Mode: Once the Bus Error event occurs, both the SDA and SCL lines are released by hardware and the BUSERR flag is asserted. The application software has to clear the BUSERR flag before the next address byte is transmitted.</p> <p>In Slave Mode: Once a misplaced START or STOP condition has been detected by the slave device, the software must clear the BUSERR flag before the next address byte is received.</p>
[9]	RXNACK	<p>Received Not Acknowledge Flag</p> <ul style="list-style-type: none"> 0: Acknowledge is returned from receiver 1: Not Acknowledge is returned from receiver <p>The RXNACK bit indicates that the not Acknowledge signal is received in master or slave transmitter mode. Writing “1” to this bit will clear the RXNACK flag.</p>
[8]	ARBLOS	<p>Arbitration Loss Flag</p> <ul style="list-style-type: none"> 0: No arbitration loss is detected 1: Bit arbitration loss is detected <p>This bit is set by hardware on the current clock which the I²C interface loses the bus arbitration to another master during the address or data frame transmission. Writing “1” to this bit will clear the ARBLOS flag. Once the ARBLOS flag is asserted by hardware, the ARBLOS flag must be cleared before the next transmission.</p>
[3]	GCS	<p>General Call Slave Flag</p> <ul style="list-style-type: none"> 0: No general call slave occurs 1: I²C interface is addressed by a general call command <p>When the I²C interface receives an address with a value of 0x00 or 0x000 in the 7-bit or 10-bit addressing mode, if both the GCEN and the AA bit are set to 1, then it is switched as a general call slave. This flag is cleared automatically after being read.</p>

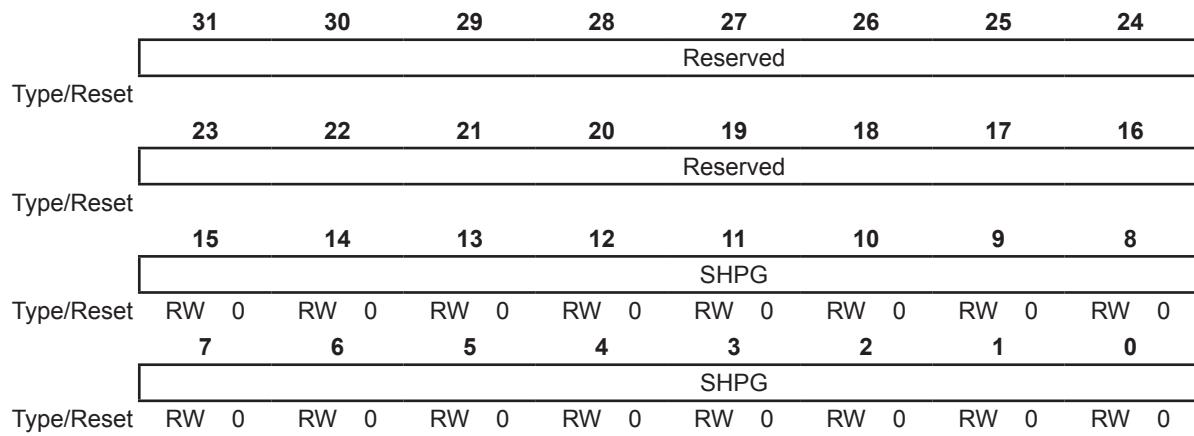
Bits	Field	Descriptions
[2]	ADRS	<p>Address Transmit (master mode) / Address Receive (slave mode) Flag Address Sent in Master Mode</p> <p>0: Address frame has not been transmitted 1: Address frame has been transmitted</p> <p>For the 7-bit addressing mode, this bit is set after the master device receives the address frame acknowledge bit sent from the slave device. For the 10-bit addressing mode, this bit is set after receiving the acknowledge bit of the first header byte and the second address.</p> <p>Address Matched in Slave Mode</p> <p>0: I²C interface is not addressed 1: I²C interface is addressed as slave</p> <p>When the I²C interface has received the calling address that matches the address defined in the I2CADDR register together with the AA bit being set to 1 in the I2CCR register, it will be switched to a slave mode. This flag is cleared automatically after the I2CSR register has been read.</p>
[1]	STO	<p>STOP Condition Detected Flag</p> <p>0: No STOP condition detected 1: STOP condition detected in slave mode</p> <p>This bit is only available for the slave mode and is cleared automatically after the I2CSR register is read.</p>
[0]	STA	<p>START Condition Transmit</p> <p>0: No START condition detected 1: START condition is transmitted in master mode</p> <p>This bit is only available for the master mode and is cleared automatically after the I2CSR register is read.</p>

I²Cn SCL High Period Generation Register – I²CnSHPG, n = 0 or 1

This register specifies the I²Cn SCL clock high period interval.

Offset: 0x010

Reset value: 0x0000_0000



Bits	Field	Descriptions
[15:0]	SHPG	<p>SCL Clock High Period Generation</p> <p>High period duration setting $SCL_{HIGH} = T_{PCLK} \times (SHPG + d)$</p> <p>where T_{PCLK} is the APB bus peripheral clock (PCLK) period, and d value depends on the setting of SEQ_FILTER in the I²C Control Register (I2CCR).</p> <ul style="list-style-type: none"> If SEQ_FILTER=00, d=6 If SEQ_FILTER=01, d=8 If SEQ_FILTER=10 or 11, d=9

I²Cn SCL Low Period Generation Register – I²CnSLPGR, n = 0 or 1

This register specifies the I²Cn SCL clock low period interval.

Offset: 0x014

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Reserved								
Type/Reset	23	22	21	20	19	18	17	16
Reserved								
Type/Reset	15	14	13	12	11	10	9	8
SLPG								
Type/Reset	RW	0	RW	0	RW	0	RW	0
	7	6	5	4	3	2	1	0
Type/Reset	RW	0	RW	0	RW	0	RW	0
SLPG								
Type/Reset	RW	0	RW	0	RW	0	RW	0

Bits	Field	Descriptions
[15:0]	SLPG	<p>SCL Clock Low Period Generation</p> <p>Low period duration setting $SCL_{LOW} = T_{PCLK} \times (SLPG + d)$</p> <p>where T_{PCLK} is the APB bus peripheral clock (PCLK) period, and d value depends on the setting of SEQ_FILTER in the I²C Control Register (I²CCR).</p> <ul style="list-style-type: none"> If SEQ_FILTER=00, d=6 If SEQ_FILTER=01, d=8 If SEQ_FILTER=10 or 11, d=9

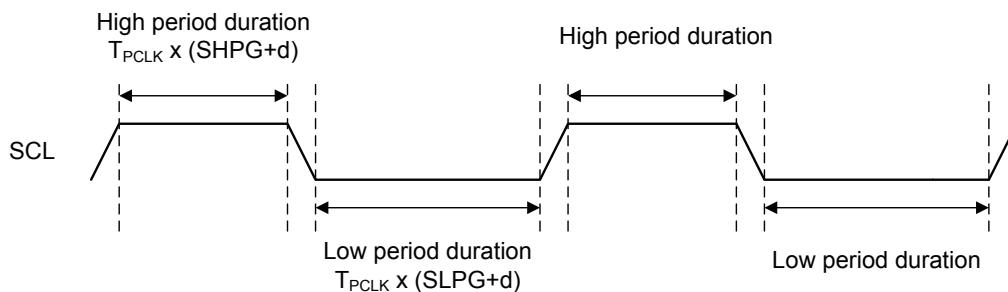


Figure 134. SCL Timing Diagram

Table 47. I²C Clock Setting Example

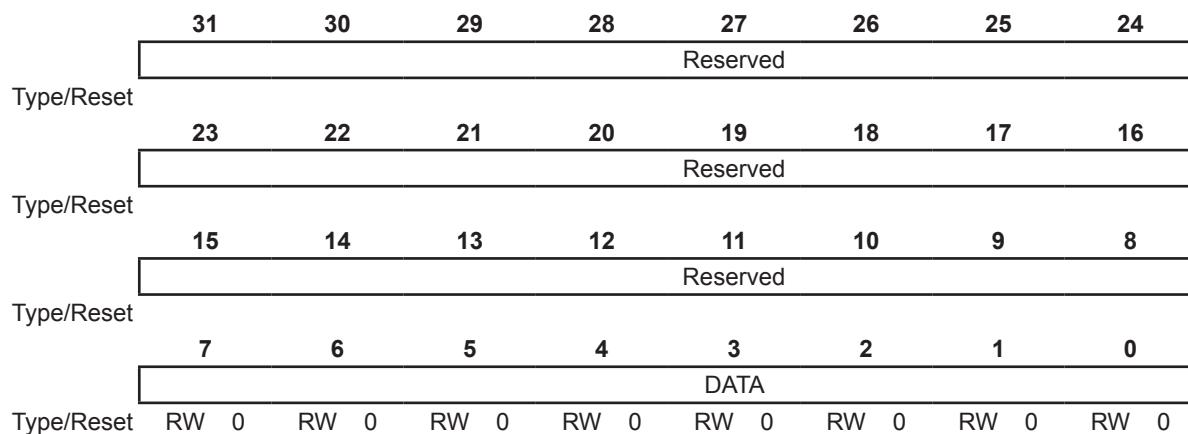
I ² C Clock	$T_{SCL} = T_{PCLK} \times [(SHPG + d) + (SLPG + d)]$ (where d = 6) SHPG + SLPG value at PCLK			
	8MHz	24MHz	48MHz	72MHz
100 kHz (Standard Mode)	68	228	468	708
400 kHz (Fast Mode)	8	48	108	168
1 MHz (Fast Mode Plus)	x	12	36	60

I²Cn Data Register – I²CnDR, n = 0 or 1

This register specifies the data to be transmitted or received by the I²Cn module.

Offset: 0x018

Reset value: 0x0000_0000



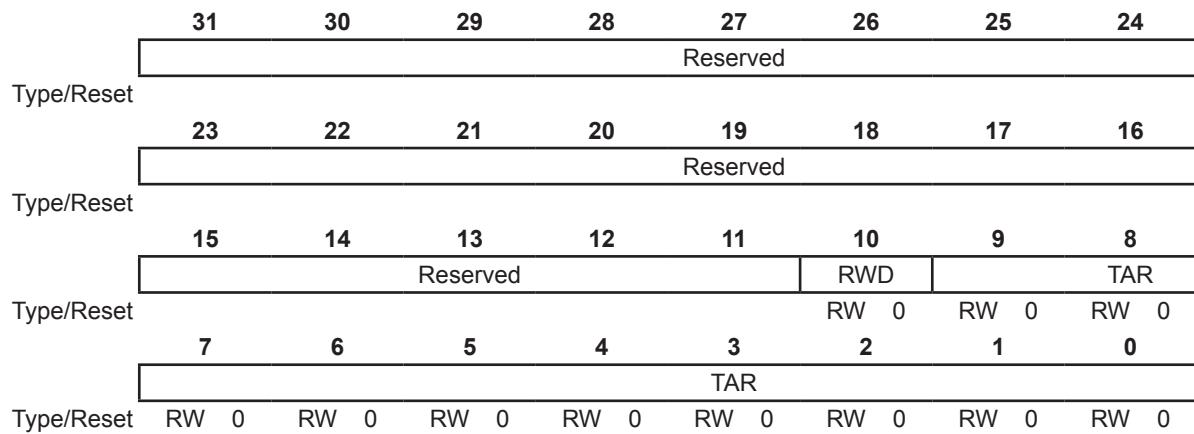
Bits	Field	Descriptions
[7:0]	DATA	<p>I²Cn Data Register</p> <p>For the transmitter mode, a data byte which is transmitted to a slave device can be assigned to these bits. The TXDE flag is cleared if the application software assigns new data to the I²CDR register. For the receiver mode, a data byte is received bit by bit from MSB to LSB through the I²C interface and stored in the data shift register. Once the acknowledge bit is given, the data shift register value is delivered into the I²CDR register if the RXDNE flag is equal to 0.</p>

I²Cn Target Register – I²CnTAR, n = 0 or 1

This register specifies the target device address to be communicated.

Offset: 0x01C

Reset value: 0x0000_0000



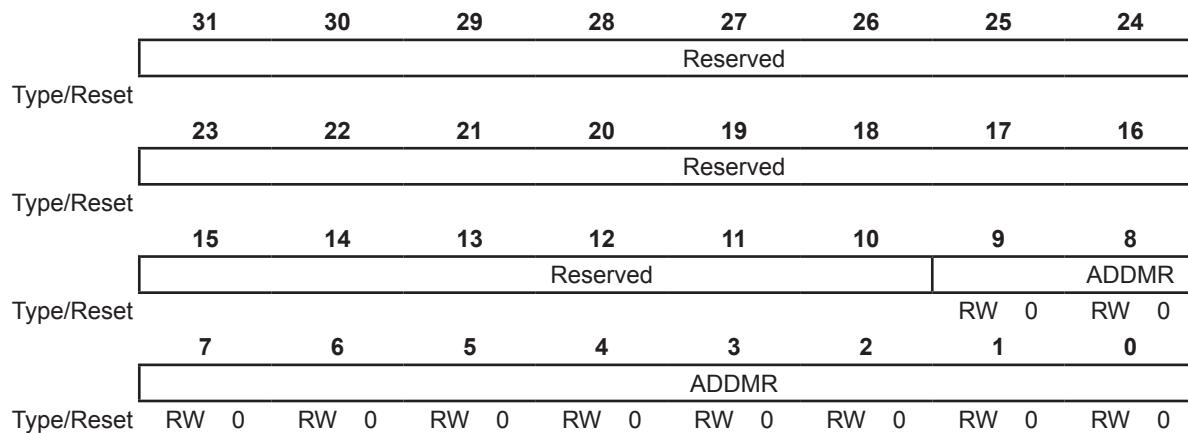
Bits	Field	Descriptions
[10]	RWD	Read or Write Direction 0: Write direction to target slave address 1: Read direction from target slave address If this bit is set to 1 in the 10-bit master receiver mode, the I ² C interface will initiate a byte with a value of 11110XX0b in the first header frame and then continue to deliver a byte with a value of 11110XX1b in the second header frame by hardware automatically.
[9:0]	TAR	Target Slave Address The I ² C interface will assign a START signal and send a target slave address automatically once the data is written to this register. When the system wants to send a repeated START signal to the I ² C bus, the timing is suggested to set the I ² CTAR register after a byte transfer is completed. It is not allowed to set TAR in the address frame. I ² CTAR[9:7] is not available under the 7-bit addressing mode.

I²Cn Address Mask Register – I2CnADDMR, n = 0 or 1

This register specifies which bit of the I²Cn address is masked and not compared with corresponding bit of the received address frame.

Offset: 0x020

Reset value: 0x0000_0000



Bits	Field	Descriptions
[9:0]	ADDMR	<p>Address Mask Control Bit</p> <p>The ADDMR[i] is used to specify whether the ith bit of the ADDR in the I2CnADDR register is masked and is compared with the received address frame or not on the I²Cn bus. The register is only used for the I²Cn slave mode only.</p> <p>0: ith bit of the ADDR is compared with the address frame on the I²Cn bus.</p> <p>1: ith bit of the ADDR is masked and not compared with the address frame on the I²Cn bus.</p>

I²Cn Address Snoop Register – I²CnADDSR, n = 0 or 1

This register is used to indicate the address frame value appeared on the I²Cn bus.

Offset: 0x024

Reset value: 0x0000_0000



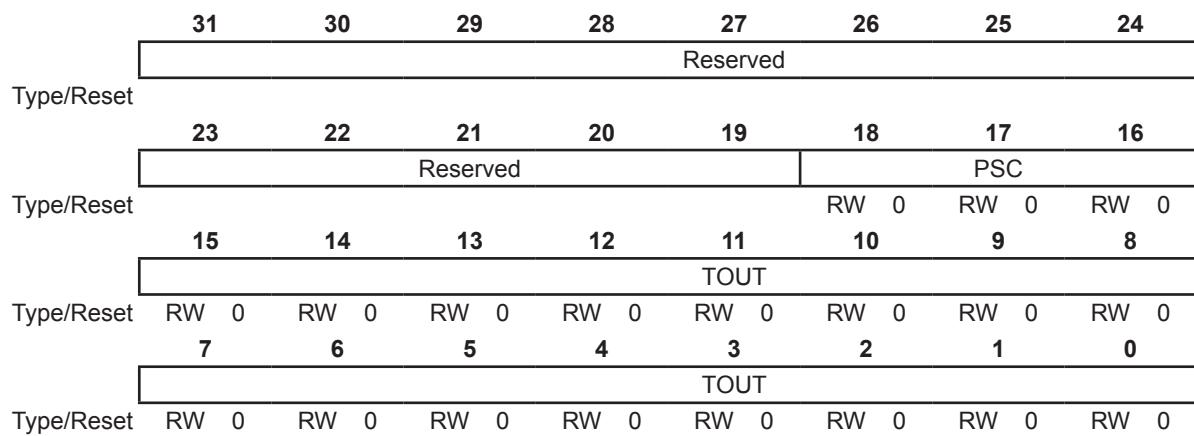
Bits	Field	Descriptions
[9:0]	ADDSR	Address Snoop Once the I2CEN bit is enabled, the calling address value on the I ² Cn bus will automatically be loaded into this ADDSR field.

I²Cn Timeout Register – I²CnTOUT, n = 0 or 1

This register specifies the I²Cn Timeout counter preload value and clock prescaler ratio.

Offset: 0x028

Reset value: 0x0000_0000



Bits	Field	Descriptions
[18:16]	PSC	<p>I²C Time-out Counter Prescaler Selection</p> <p>This PSC field is used to specify the I²C time-out counter clock frequency, f_{I²CTO}. The time-out clock frequency is obtained using the formula:</p> $f_{I^2CTO} = \frac{f_{PCLK}}{2^{PSC}}$ <p>PSC=0 → f_{I²CTO} = f_{PCLK} / 2⁰ = f_{PCLK} PSC=1 → f_{I²CTO} = f_{PCLK} / 2¹ = f_{PCLK} / 2 PSC=2 → f_{I²CTO} = f_{PCLK} / 2² = f_{PCLK} / 4 ... PSC=7 → f_{I²CTO} = f_{PCLK} / 2⁷ = f_{PCLK} / 128</p>
[15:0]	TOUT	<p>I²C Timeout Counter Preload Value</p> <p>The TOUT field is used to define the counter preloaded value</p> <p>The counter value is reloaded as the following conditions occur:</p> <ol style="list-style-type: none"> 1. The RXBF, TXDE, RXDNE, RXNACK, GCS or ADRS flag in the I2CSR register is asserted. 2. The I²C master module sends a START signal. 3. The I²C slave module detects a START signal. <p>The counter stops counting as the following conditions occur:</p> <ol style="list-style-type: none"> 1. The I²C slave device is not addressed. 2. The I²C master module sends a STOP signal. 3. The I²C slave module detects a STOP signal. 4. The ARBLOS or BUSERR flag in the I2CSR register is asserted.

20 Serial Peripheral Interface (SPI)

Introduction

The Serial Peripheral Interface, SPI, provides an SPI protocol data transmit and receive functions in both master or slave mode. The SPI interface uses 4 pins, among which are serial data input and output lines MISO and MOSI, the clock line SCK, and the slave select line SEL. One SPI device acts as a master which controls the data flow using the SEL and SCK signals to indicate the start of the data communication and the data sampling rate. To receive the data bits, the streamlined data bits which ranges from 1 bit to 16 bits specified by the DFL field in the SPIInCR1 register are latched in a specific clock edge and stroed in the data register or in the Rx FIFO. Data transmission is carried in a similar way but with the reverse sequence. The mode fault detection provides a capability for multi-master applications.

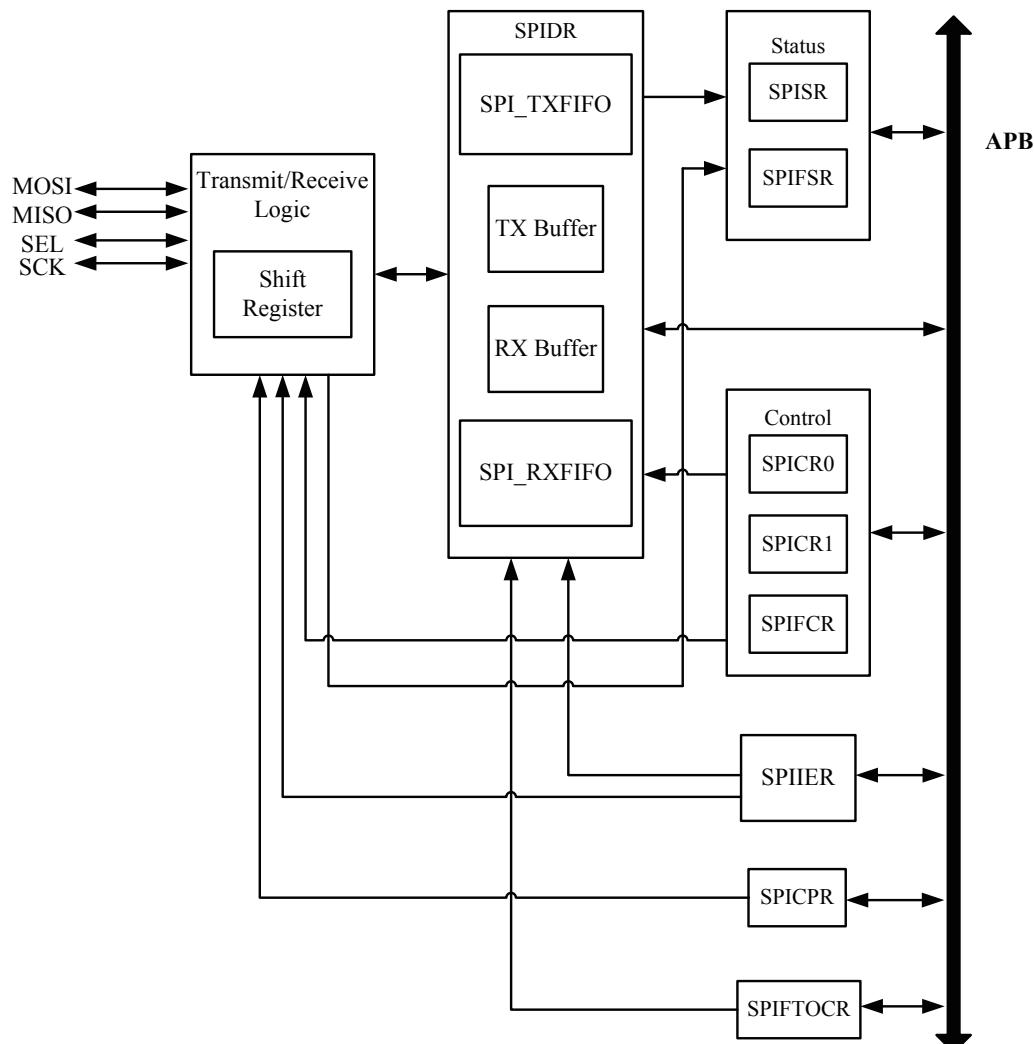


Figure 135. SPI Block Diagram

Features

- Master or slave mode
- Master mode speed up to 36MHz
- Slave mode speed up to 24MHz
- Programmable data frame length up to 16 bits
- FIFO Depth: 8 levels
- MSB or LSB first shift selection
- Programmable slave select high or low active polarity
- Multi-master and multi-slave operation
- Master mode supports the dual output read mode of SPI serial NOR Flash
- Four error flags with individual interrupt
 - Read overrun
 - Write collision
 - Mode fault
 - Slave abort
- Support PDMA interface

Functional Descriptions

Master Mode

Each data frame can range from 1 to 16 bits in data length. The first bit of the transmitted data can be either an MSB or LSB determined by the FIRSTBIT bit in the SPICR1 register. The SPI module is configured as a master or a slave by setting the MODE bit in the SPICR1 register. When the MODE bit is set, the SPI module is configured as a master and will generate the serial clock on the SCK pin. The data stream will transmit data in the shift register to the MOSI pin on the serial clock edge. The SEL pin is active during the full data transmission. When the SELAP bit in the SPICR1 register is set, the SEL pin is active high during the complete data transactions. When the SELM bit in the SPICR1 register is set, the SEL pin will be driven by the hardware automatically and the time interval between the active SEL edge and the first edge of SCK is equal to half a SCK period.

Slave Mode

In the slave mode, the SCK pin acts as an input pin and the serial clock will be derived from the external master device. The SEL pin also acts as an input. When the SELAP bit is cleared to 0, the SEL signal is active low during the full data stream reception. When the SELAP bit is set to 1, the SEL signal will be active high during the full data stream reception.

Note: For the slave mode, the APB clock, known as f_{PCLK} , must be at least 3 times faster than the external SCK clock input frequency.

SPI Serial Frame Format

The SPI interface format is based on the Clock Polarity, CPOL, and the Clock Phase, CPHA, configurations.

- Clock Polarity Bit – CPOL

When the Clock Polarity bit is cleared to 0, the SCK line idle state is LOW. When the Clock Polarity bit is set to 1, the SCK line idle state is HIGH.

- Clock Phase Bit – CPHA

When the Clock Phase bit is cleared to 0, the data is sampled on the first SCK clock transition. When the Clock Phase bit is set to 1, the data is sampled on the second SCK clock transition.

There are four formats contained in the SPI interface. Table 48 shows how to configure these formats by setting the FORMAT field in the SPICR1 register.

Table 48. SPI Interface Format Setup

FORMAT [2:0]	CPOL	CPHA
001	0	0
010	0	1
110	1	0
101	1	1
Others	Reserved	

CPOL = 0, CPHA = 0

In this format, the received data is sampled on the SCK line rising edge while the transmitted data is changed on the SCK line falling edge. In the master mode, the first bit is driven when data is written into the SPIDR Register. In the slave mode, the first bit is driven when the SEL signal goes to an active level. Figure 136 shows the single byte data transfer timing diagram of this format.

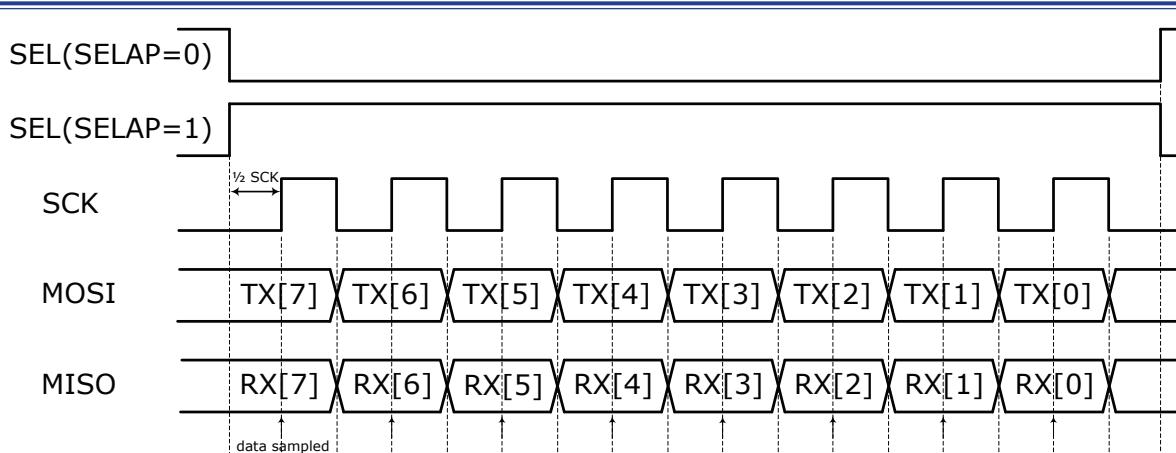


Figure 136. SPI Single Byte Transfer Timing Diagram - CPOL = 0, CPHA = 0

Figure 137 shows the continuous data transfer timing diagram of this format. Note that the SEL signal must change to an inactive level between each data frame.

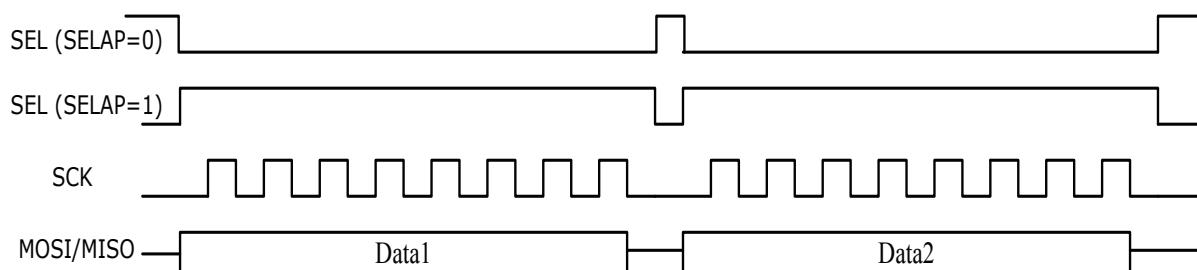


Figure 137. SPI Continuous Data Transfer Timing Diagram - CPOL = 0, CPHA = 0

CPOL = 0, CPHA = 1

In this format, the received data is sampled on the SCK line falling edge while the transmitted data is changed on the SCK line rising edge. In the master mode, the first bit is driven when data is written into the SPIDR register. In the slave mode, the first bit is driven at the first SCK clock rising edge. Figure 138 shows the single data byte transfer timing.

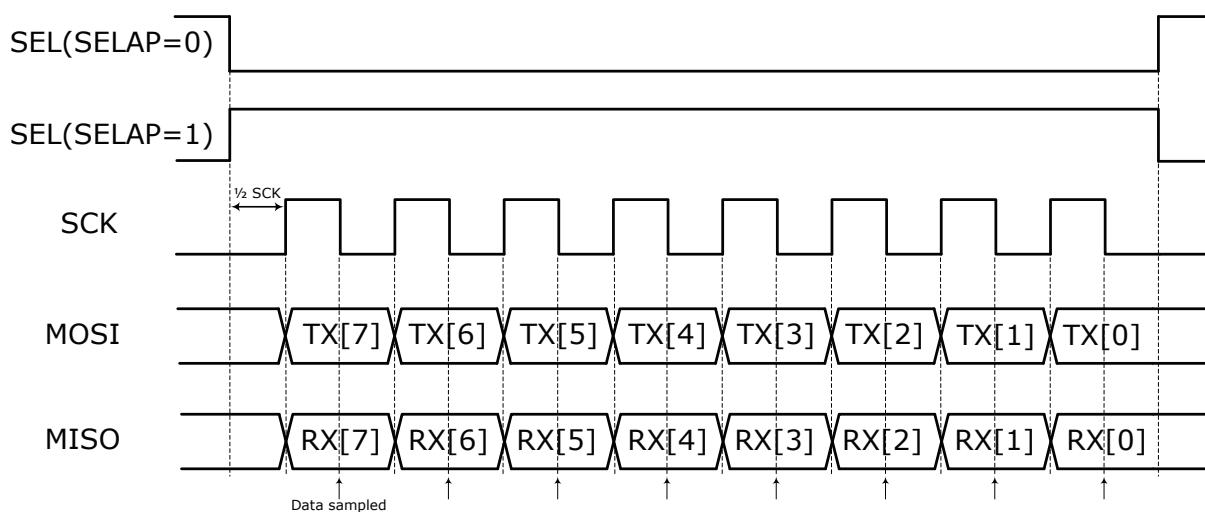


Figure 138. SPI Single Byte Transfer Timing Diagram - CPOL = 0, CPHA = 1

Figure 139 shows the continuous data transfer diagram timing. Note that the SEL signal must remain active until the last data transfer has completed.

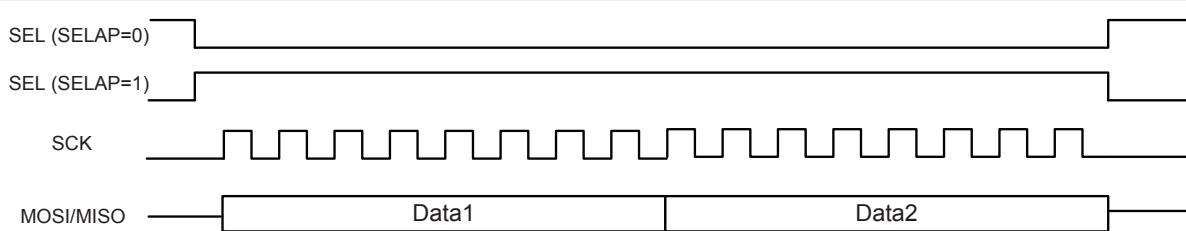


Figure 139. SPI Continuous Transfer Timing Diagram - CPOL = 0, CPHA = 1

CPOL = 1, CPHA = 0

In this format, the received data is sampled on the SCK line falling edge while the transmitted data is changed on the SCK line rising edge. In the master mode, the first bit is driven when data is written into the SPIDR register. In the slave mode, the first bit is driven when the SEL signal changes to an active level. Figure 140 shows the single byte transfer timing of this format.

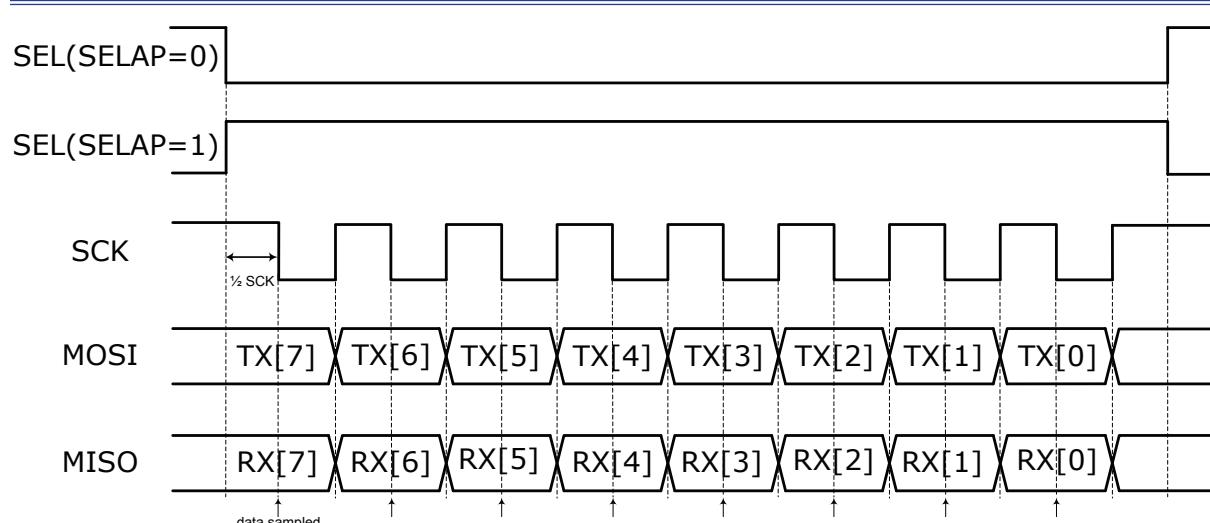


Figure 140. SPI Single Byte Transfer Timing Diagram - CPOL = 1, CPHA = 0

Figure 141 shows the continuous data transfer timing of this format. Note that the SEL signal must change to an inactive level between each data frame.

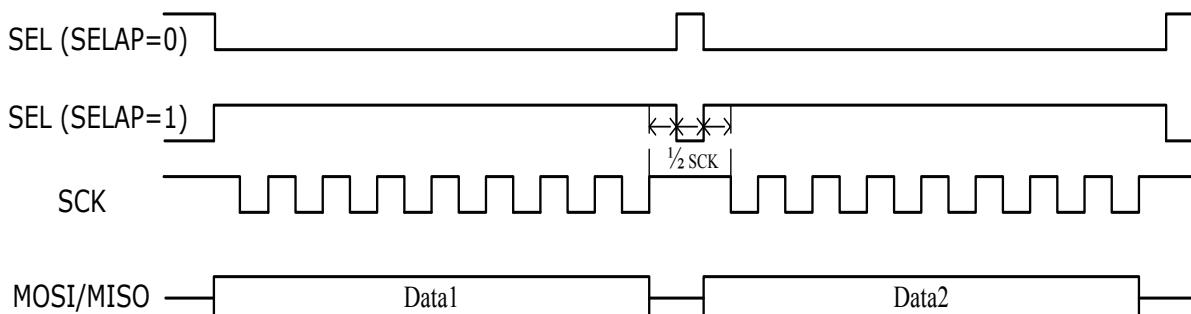


Figure 141. SPI Continuous Transfer Timing Diagram - CPOL = 1, CPHA = 0

CPOL = 1, CPHA = 1

In this format, the received data is sampled on the SCK line rising edge while the transmitted data is changed on the SCK line falling edge. In the master mode, the first bit is driven when data is written into the SPIDR register. In the slave mode, the first bit is driven at the first SCK falling edge. Figure 142 shows the single byte transfer timing of this format.

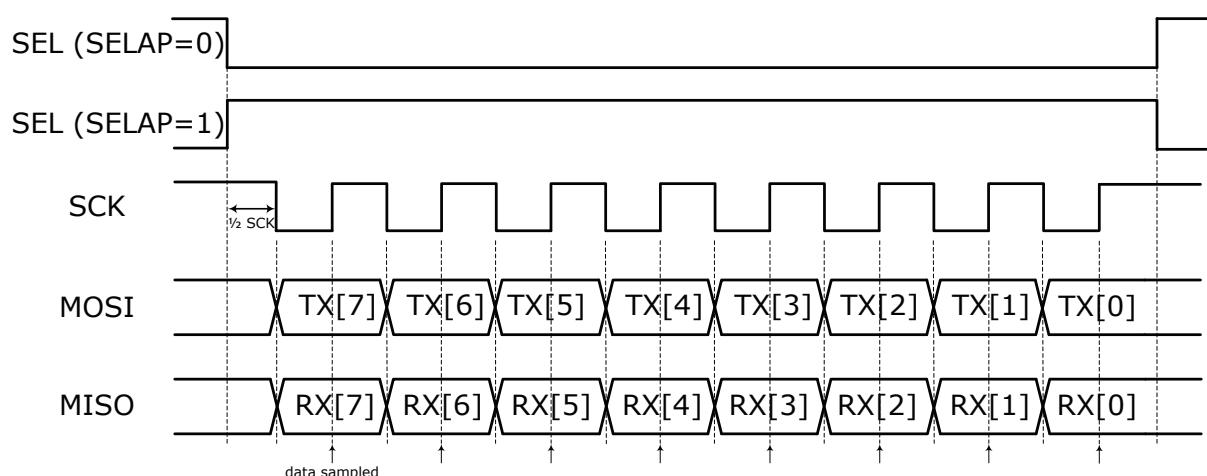


Figure 142. SPI Single Byte Transfer Timing Diagram - CPOL = 1, CPHA = 1

Figure 143 shows the continuous data transfer timing of this format. Note that the SEL signal must remain active until the last data transfer has completed.

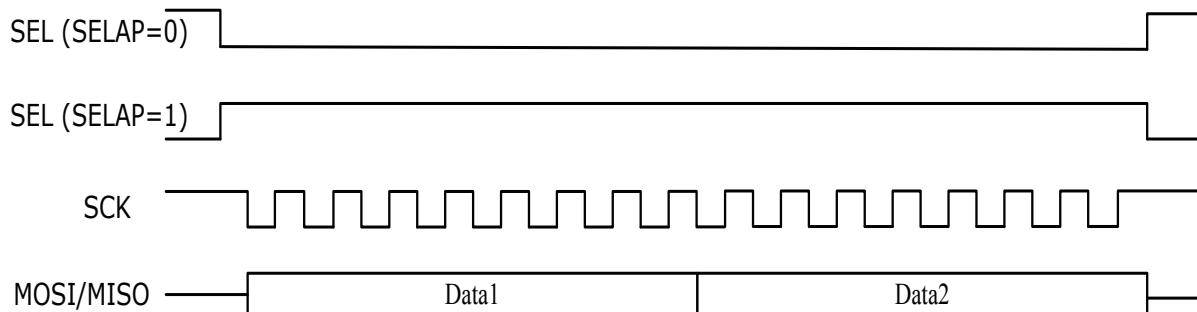


Figure 143. SPI Continuous Transfer Timing Diagram - CPOL = 1, CPHA = 1

Status Flags

Tx Buffer Empty – TXBE

This TXBE flag is set when the Tx buffer is empty in the non-FIFO mode or when the TX FIFO data length is equal to or less than the TX FIFO threshold level as defined by the TXFTLS field in the SPIFCR register in the FIFO mode. The following data to be transmitted can then be loaded into the buffer again. After this, the TXBE flag will be reset when the Tx buffer already contains new data in the non-FIFO mode or the TX FIFO data length is greater than the TX FIFO threshold level determined by the TXFTLS bits in FIFO mode.

Transmission Register Empty – TXE

This TXE flag is set when both the TX buffer and the TX shift registers are empty. It will be reset when the TX buffer or the TX shift register contains new transmitted data.

Rx Buffer Not Empty – RXBNE

This RXBNE flag is set when there is valid received data in the RX Buffer in the non-FIFO mode or the RX FIFO data length is equal to or greater than the RX FIFO threshold level as defined by the RXFTLS field in the SPIFCR register in the SPI FIFO mode. This flag will be automatically cleared by hardware when the received data have been read out from the RX buffer totally in the non-FIFO mode or when the RX FIFO data length is less than the RX FIFO threshold level set in the RXFTLS field.

Time Out Flag – TO

The time out function is only available in the SPI FIFO mode and is disabled by loading a zero value into the TOC field in the Time Out Counter register. The time out counter will start counting if the SPI RX FIFO is not empty, once data is read from the SPIDR register or new data is received, the time out counter will be reset to 0 and count again. When the time out counter value is equal to the value specified by the TOC field in the SPIFTOCR register, the TO flag will be set. The flag is cleared by writing 1 to this bit.

Mode Fault – MF

The mode fault flag can be used to detect SPI bus usage in the SPI multi-master mode. For the multi-master mode, the SPI module is configured as a master device and the SEL signal is setup as an input signal. The mode fault flag is set when the SPI SEL pin is suddenly changed to an active level by another SPI master. This means that another SPI master is requesting to use the SPI bus. Therefore, when an SPI mode fault occurs, it will force the SPI module to operate in the slave mode and also disable all of the SPI interface signals to avoid SPI bus signal collisions. For the same reason, if the SPI master wants to transfer data, it also needs to inform other SPI masters by driving its SEL signal to an active state. The detailed configuration diagram for the SPI multi-master mode is shown in the following figure.

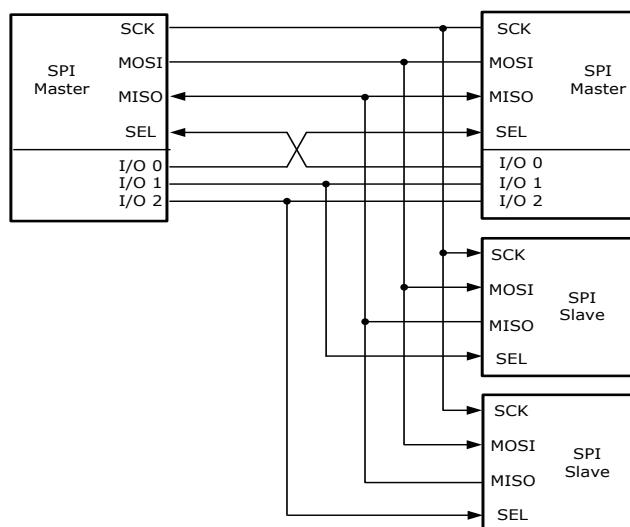


Figure 144. SPI Multi-Master Slave Environment

Table 49. SPI Mode Fault Trigger Conditions

Mode fault	Descriptions
Trigger condition	1. SPI Master mode 2. SELOEN = 0 in the SPICR0 register – SEL pin is configured to be the input mode 3. SEL signal changes to an active level when driven by the external SPI master
SPI behavior	1. Mode fault flag is set. 2. The SPIEN bit in the SPICR0 register is reset. This disables the SPI interface and blocks all output signals from the device. 3. The MODE bit in the SPICR1 register is reset. This forces the device into slave mode.

Table 50. SPI Master Mode SEL Pin Status.

	SEL as Input - SELOEN = 0	SEL as Output - SELOEN = 1	
Multi-master	Support	Not support	
SPI SEL control signal	Use Another GPIO to replace the SEL pin function		
Continuous transfer	Case 1	Case 2	Case 1
	Not supported	Supported	Using hardware control
		Hardware or software control	

Case 1: SEL signal must be inactive between each data transfer.

Case 2: SEL signal will not be active until the last data frame has finished.

Note: When the SPI module is in the slave mode, the SEL signal is always an input and not affected by the SELOEN bit in the SPICR0 register.

Write Collision – WC

The following conditions will assert the Write Collision Flag.

- The FIFOEN bit in the SPIFCR register is cleared

The write collision flag is asserted when new data is written into the SPIDR register while both the TX buffer and the shift register are already full. Any new data written into the TX buffer will be lost.
- The FIFOEN bit in the SPIFCR register is set

The write collision flag is asserted to indicate that new data is written into the SPIDR register while both the TX FIFO and the TX shift register are already full. Any new data written into the TX FIFO will be lost.

Read Overrun – RO

- The FIFOEN bit in the SPIFCR register is cleared

The read overrun flag is asserted to indicate that both the RX shift register and the RX buffer are already full, if one more data is received. This will result in the newly received data not being shifted into the SPI shift register. As a result the latest received data will be lost.
- The FIFOEN bit in the SPIFCR register is set

The read overrun flag is set to indicate that the RX shift register and the RX FIFO are both full, if one more data is received. This means that the latest received data can not be shifted into the SPI shift register. As a result the latest received data will be lost.

Slave Abort – SA

In the SPI slave mode, the slave abort flag is set to indicate that the SEL pin suddenly changed to an inactive state during the reception of a data frame transfer. The data frame length is set by the DFL field in the SPICR1 register.

PDMA Interface

The PDMA interface is integrated in the SPI module. The PDMA function can be enabled by setting the TXDMAE or RXDMAE bit to 1 in the transmitter or receiver mode respectively. When the transmit buffer empty flag, TXBE, is asserted and the TXDMAE bit is set to 1, the PMDA function will be activated to move data from the memory location that users designated into the SPI data register or the TX FIFO until the TXBE flag is cleared to 0. The TXBE flag will be asserted when the transmit buffer is empty in the non-FIFO mode or the data contained in the TX FIFO is equal to or less than the level defined by the TXFTLS field in the FIFO mode.

Similarly, when the receive buffer not empty flag, RXBNE, is asserted and the RXDMAE bit is set to 1, the PDMA function will be activated to move data from the SPI data register or the RX FIFO to the memory location that users designated until the RXBNE flag is cleared to 0. The RXBNE flag will be asserted when the receive buffer is not empty in the non-FIFO mode or the data contained in the RX FIFO is equal to or greater than the level defined by the RXFTLS field in the FIFO mode.

For a mode detailed description on the PDMA configurations, refer to the PDMA chapter.

Register Map

The following table shows the SPI registers and their reset values.

Table 51. SPI Register Map

Register	Offset	Description	Reset Value
SPI0 Base Address = 0x4000_4000			
SPI1 Base Address = 0x4004_4000			
SPICR0	0x000	SPI Control Register 0	0x0000_0000
SPICR1	0x004	SPI Control Register 1	0x0000_0000
SPIIER	0x008	SPI Interrupt Enable Register	0x0000_0000
SPICPR	0x00C	SPI Clock Prescaler Register	0x0000_0000
SPIDR	0x010	SPI Data Register	0x0000_0000
SPISR	0x014	SPI Status Register	0x0000_0003
SPIFCR	0x018	SPI FIFO Control Register	0x0000_0000
SPIFSR	0x01C	SPI FIFO Status Register	0x0000_0000
SPIFTOCR	0x020	SPI FIFO Time Out Counter Register	0x0000_0000

Register Descriptions

SPIn Control Register 0 – SPInCR0, n=0 or 1

This register specifies the SEL control and the SPIn enable bits.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24		
Type/Reset	Reserved									
	23	22	21	20	19	18	17	16		
Type/Reset	Reserved									
	15	14	13	12	11	10	9	8		
Type/Reset	SELHT					GUADT				
	RW	0	RW	0	RW	0	RW	0	RW	0
Type/Reset	7	6	5	4	3	2	1	0		
	GUADTEN	DUALEN	Reserved	SSELCK	SELOEN	RXDMAE	TXDMAE	SPIEN		
Type/Reset	RW	0	RW	0	RW	0	RW	0	RW	0

Bits	Field	Descriptions
[15:12]	SELHT	Chip Select Hold Time 0x0: 1/2 SCK 0x1: 1 SCK 0x2: 3/2 SCK 0x3: 2 SCK ... Note that SELHT is for master mode only.
[11:8]	GUADT	Guard Time 0x0:1 SCK 0x1:2 SCK 0x2: 3 SCK ... Note that GUADT is for master mode only.
[7]	GUADTEN	Guard Time Enable 0: Guard Time is 1/2 SCK 1: When set this bit, Guard time can be controlled by GUADT Note that GUADTEN is for master mode only.
[6]	DUALEN	Dual Port Enable 0: Dual port is disabled 1: Dual port is enabled The control bit is used to support the dual output read mode of the series SPI NOR Flash. When this bit is set and the MOSI signal will change the direction from output to input and receive the series data stream. That means the DUALEN control bit is only for master mode.

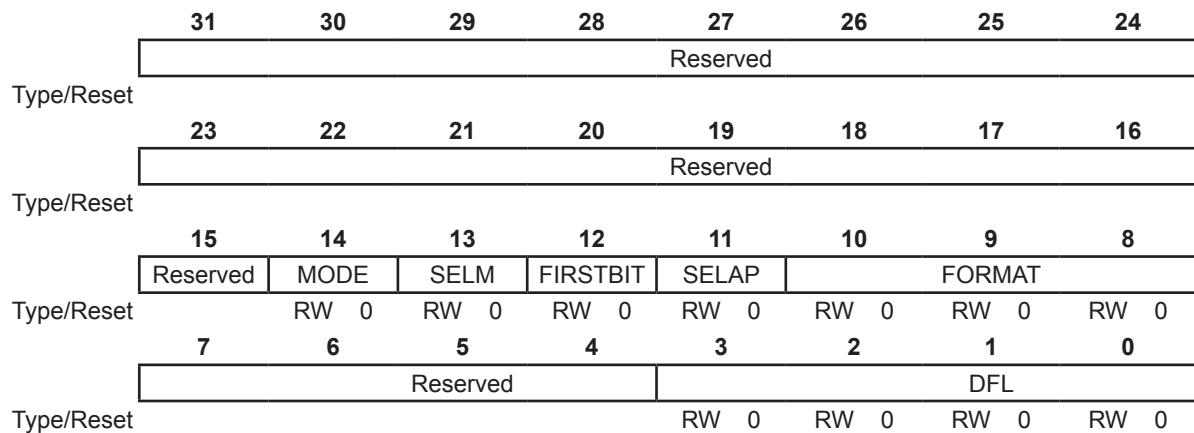
Bits	Field	Descriptions
[4]	SSEL C	<p>Software Slave Select Control</p> <p>0: Set the SEL output to an inactive state 1: Set the SEL output to an active state</p> <p>The application Software can setup the SEL output to an active or inactive state by configuring the SSEL C bit. The active level is configured by the SELAP bit in the SPICR1 register. Note that the SSEL C bit is only available when the SELOEN bit is set to 1 for enabling the SEL output meanwhile the SELM bit is cleared to 0 for controlling the SEL signal by software. Otherwise, the SSEL C bit has no effect.</p>
[3]	SELOEN	<p>Slave Select Output Enable</p> <p>0: Set the SEL signal to the input mode for Multi-master mode 1: Set the SEL signal to the output mode for slave select</p> <p>The SELOEN is only available in the master mode to setup the SEL signal as an input or output signal. When the SEL signal is configured to operate in the output mode, it is used as a slave select signal in either the hardware or software mode according to the SELM bit setting in the SPICR1 register. The SEL signal is used for mode fault detection in the multi-master environment when it is configured to operate in the input mode</p>
[2]	RXDMAE	<p>RX PDMA request enable</p> <p>0: SPI RX path PDMA request disabled. 1: SPI RX path PDMA request enabled.</p>
[1]	TXDMAE	<p>TX PDMA request enable</p> <p>0: SPI TX path PDMA request disabled. 1: SPI TX path PDMA request enabled.</p>
[0]	SPIEN	<p>SPI Enable</p> <p>0: SPI interface is disabled 1: SPI interface is enabled</p>

SPI Control Register 1 – SPInCR1, n=0 or 1

This register specifies the SPIn parameters including the data length, the transfer format, the SEL active polarity/mode, the LSB/MSB control, and the master/slave mode.

Offset: 0x004

Reset value: 0x0000_0000



Bits	Field	Descriptions
[14]	MODE	Master or Slave Mode 0: Slave mode 1: Master mode
[13]	SELM	Slave Select Mode 0: SEL signal is controlled by software – asserted or de-asserted by the SSELC bit 1: SEL signal is controlled by hardware – generated automatically by the SPI hardware Note that SELM bit is available for master mode only - MODE = 1
[12]	FIRSTBIT	LSB or MSB Transmitted First 0: MSB transmitted first 1: LSB transmitted first

Bits	Field	Descriptions																		
[11]	SELAP	Slave Select Active Polarity 0: SEL signal is active low 1: SEL signal is active high																		
[10:8]	FORMAT	SPI Data Transfer Format These three bits are used to determine the data transfer format of the SPI interface <table border="1" data-bbox="493 541 1187 736"> <thead> <tr> <th>FORMAT [2:0]</th><th>CPOL</th><th>CPHA</th></tr> </thead> <tbody> <tr> <td>001</td><td>0</td><td>0</td></tr> <tr> <td>010</td><td>0</td><td>1</td></tr> <tr> <td>110</td><td>1</td><td>0</td></tr> <tr> <td>101</td><td>1</td><td>1</td></tr> <tr> <td>Others</td><td colspan="2">Reserved</td></tr> </tbody> </table> CPOL: Clock Polarity 0: SCK Idle state is low 1: SCK Idle state is high CPHA: Clock Phase 0: Data is captured on the first SCK clock edge 1: Data is captured on the second SCK clock edge	FORMAT [2:0]	CPOL	CPHA	001	0	0	010	0	1	110	1	0	101	1	1	Others	Reserved	
FORMAT [2:0]	CPOL	CPHA																		
001	0	0																		
010	0	1																		
110	1	0																		
101	1	1																		
Others	Reserved																			
[3:0]	DFL	Data Frame Length Selects the data transfer frame from 1 bit to 16 bits. 0x1: 1 bit 0x2: 2 bits ... 0xF: 15 bits 0x0: 16 bits																		

SPI_n Interrupt Enable Register – SPI_nIER, n=0 or 1

This register contains the corresponding SPI_n interrupt enable control bit.

Offset: 0x008

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Reserved								
Type/Reset	23	22	21	20	19	18	17	16
Reserved								
Type/Reset	15	14	13	12	11	10	9	8
Reserved								
Type/Reset	7	6	5	4	3	2	1	0
Type/Reset	TOIEN	SAIEN	MFIEN	ROIEN	WCien	RXBNEIEN	TXEIEN	TXBEIEN
	RW 0	RW 0	RW 0					

Bits	Field	Descriptions
[7]	TOIEN	Time Out Interrupt Enable 0: Disable 1: Enable
[6]	SAIEN	Slave Abort Interrupt Enable 0: Disable 1: Enable
[5]	MFIEN	Mode Fault Interrupt Enable 0: Disable 1: Enable
[4]	ROIEN	Read Overrun Interrupt Enable 0: Disable 1: Enable
[3]	WCien	Write Collision Interrupt Enable 0: Disable 1: Enable
[2]	RXBNEIEN	RX Buffer Not Empty Interrupt Enable 0: Disable 1: Enable Generates an interrupt request when the RXBNE flag is set and when RXBNEIEN is set. In the FIFO mode, the interrupt request being generated depends upon the RX FIFO trigger level setting

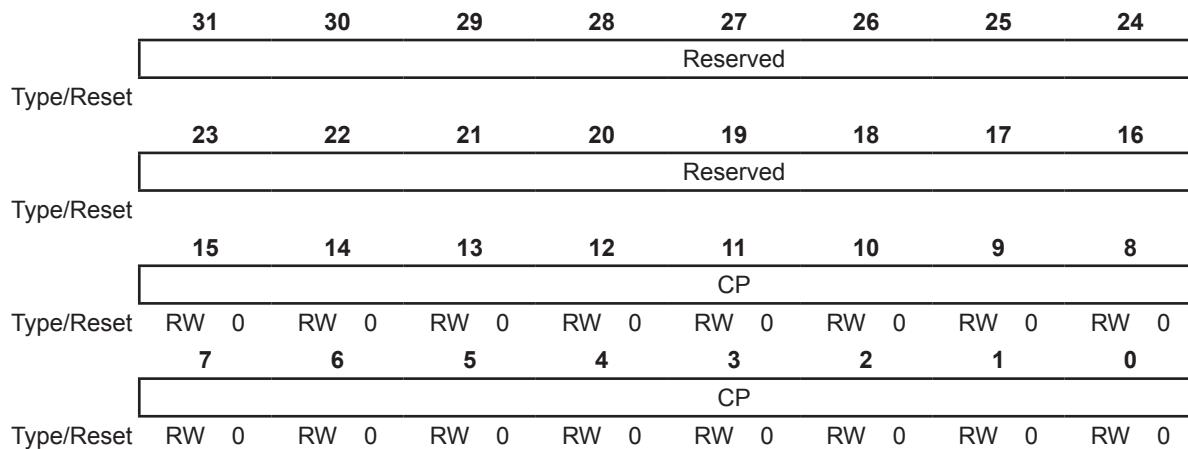
Bits	Field	Descriptions
[1]	TXEIEN	Tx Empty Interrupt Enable 0: Disable 1: Enable The TX register empty interrupt request will be generated when the TXE flag and the TXEIEN bit are set
[0]	TXBEIEN	Tx Buffer Empty Interrupt Enable 0: Disable 1: Enable The TX buffer empty interrupt request will be generated when the TXBE flag and the TXBEIEN bit are set. In the FIFO mode, the interrupt request being generated depends upon the TX FIFO trigger level setting.

SPIn Clock Prescaler Register – SPInCPR, n=0 or 1

This register specifies the SPIn clock prescaler ratio.

Offset: 0x00C

Reset value: 0x0000_0000



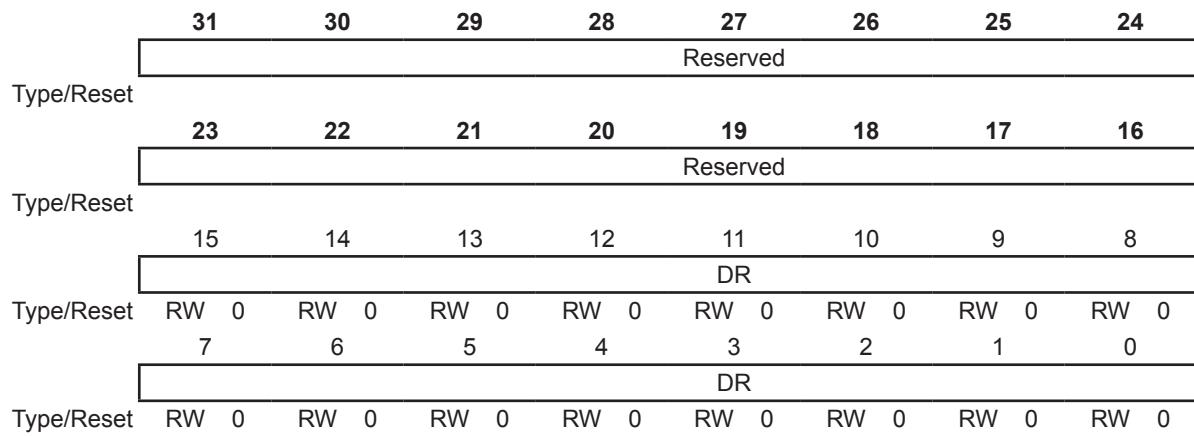
Bits	Field	Descriptions
[15:0]	CP	SPI Clock Prescaler The SPI clock (SCK) is determined by the following equation: $f_{SCK} = f_{PCLK} / (2 * (CP + 1))$, where the CP ranges is from 0 to 65535 Note: For the SPI slave mode, the system clock (f_{PCLK}) must be at least 3 times faster than the external SPI SCK input.

SPIn Data Register – SPInDR, n=0 or 1

This register stores the SPIn received or transmitted Data.

Offset: 0x010

Reset value: 0x0000_0000



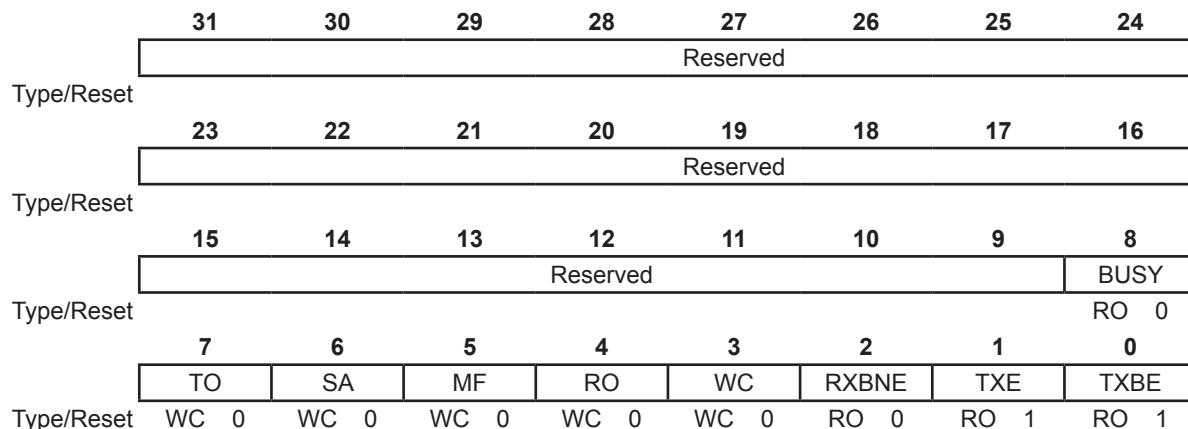
Bits	Field	Descriptions
[15:0]	DR	<p>Data Register</p> <p>The SPI data register is used to store the serial bus transmitted or received data. In the non-FIFO mode, writing data into the SPI data register will also load the data into the data transmission buffer, known as the TX buffer. Reading data from the SPI data register will return the data held in the data received buffer, named RX buffer.</p>

SPI Status Register – SPInSR, n=0 or 1

This register contains the relevant SPI status.

Offset: 0x014

Reset value: 0x0000_0003



Bits	Field	Descriptions
[8]	BUSY	SPI Busy flag 0: SPI not busy 1: SPI busy In the master mode, this flag is reset when the TX buffer and TX shift register are both empty and is set when the TX buffer or the TX shift register are not empty. In the slave mode, this flag is set when SEL changes to an active level and is reset when SEL changes to an inactive level .
[7]	TO	Time Out flag 0: No Rx FIFO time out 1: Rx FIFO time out has occurred. Write 1 to clear it. Once the time out counter value is equal to the TOC field setting in the SPIFTOCR register, the time out flag will be set and an interrupt will be generated if the TOIEN bit in the SPIIER register is enabled. This bit is cleared by writing 1 Note: This Time Out flag function is only available in the SPI FIFO mode.
[6]	SA	Slave Abort flag 0: No slave abort 1: Slave abort has occurred. This bit is set by hardware and cleared by writing 1.
[5]	MF	Mode Fault flag 0: No mode fault 1: Mode fault has occurred This bit is set by hardware and cleared by writing 1.
[4]	RO	Read Overrun flag 0: No read overrun 1: Read overrun has occurred. This bit is set by hardware and cleared by writing 1.

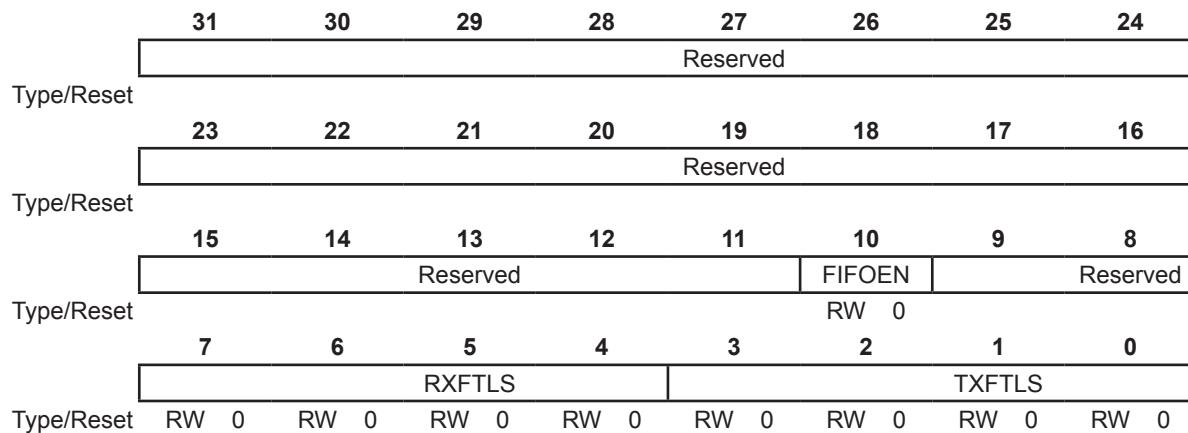
Bits	Field	Descriptions
[3]	WC	<p>Write Collision flag</p> <p>0: No write collision 1: Write collision has occurred.</p> <p>This bit is set by hardware and cleared by writing 1.</p>
[2]	RXBNE	<p>Receive Buffer Not Empty flag</p> <p>0: Rx buffer empty 1: Rx buffer not empty</p> <p>This bit indicates the RX buffer status in the non-FIFO mode. It is also used to indicate if the RX FIFO trigger level has been reached in the FIFO mode. This bit will be cleared when the SPI RX buffer is empty in the non-FIFO mode or if the number of data contained in RX FIFO is less than the trigger level which is specified by the RXFTLS field in the SPIFCR register in the SPI FIFO mode</p>
[1]	TXE	<p>Transmission Register Empty flag</p> <p>0: Tx buffer or Tx shift register is not empty 1: Tx buffer and Tx shift register both are empty</p>
[0]	TXBE	<p>Transmit Buffer Empty flag</p> <p>0: Tx buffer not empty 1: Tx buffer empty</p> <p>In the FIFO mode, this bit indicates that the number of data contained in TX FIFO is equal to or less than the trigger level specified by the TXFTLS field in the SPIFCR register.</p>

SPIn FIFO Control Register – SPInFCR, n=0 or 1

This register contains the related SPIn FIFO control including the FIFO enable control and the FIFO trigger level selections.

Offset: 0x018

Reset value: 0x0000_0000



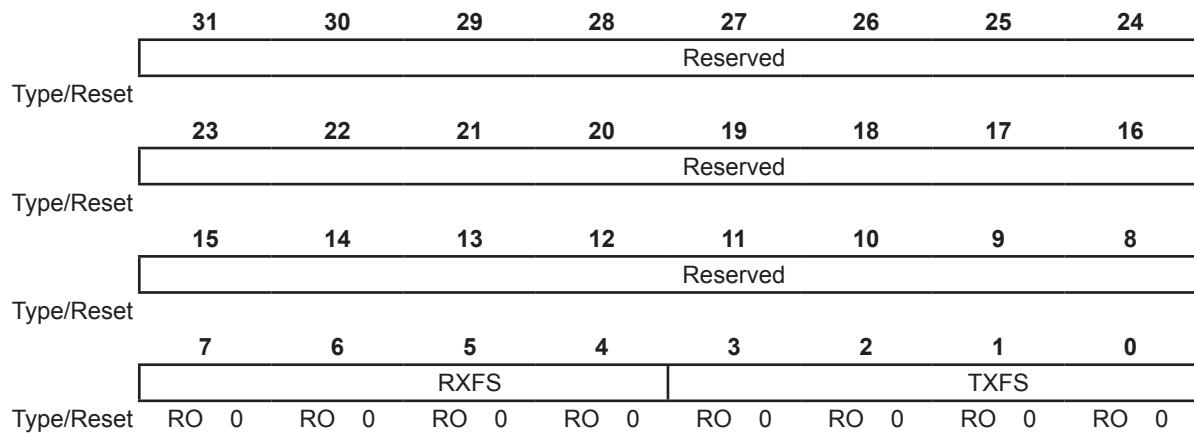
Bits	Field	Descriptions
[10]	FIFOEN	<p>FIFO Enable</p> <p>0: FIFO disable 1: FIFO enable</p> <p>This bit cannot be set or reset when the SPI interface is in transmitting.</p>
[7:4]	RXFTLS	<p>Rx FIFO Trigger Level Select</p> <p>0000: Trigger level is 0 0001: Trigger level is 1 ... 1000: Trigger level is 8 Others: Reserved</p> <p>The RXFTLS field is used to specify the RX FIFO trigger level. When the number of data contained in the RX FIFO is equal to or greater than the trigger level defined by the RXFTLS field, the RXBNE flag will be set</p>
[3:0]	TXFTLS	<p>Tx FIFO Trigger Level Select</p> <p>0000: Trigger level is 0 0001: Trigger level is 1 ... 1000: Trigger level is 8 Others: Reserved</p> <p>The TXFTLS field is used to specify the TX FIFO trigger level. When the number of data contained in the TX FIFO is equal to or less than the trigger level defined by the TXFTLS field, the TXBE flag will be set.</p>

SPIn FIFO Status Register – SPInFSR, n=0 or 1

This register contains the relevant SPIn FIFO status.

Offset: 0x01C

Reset value: 0x0000_0000



Bits	Field	Descriptions
[7:4]	RXFS	Rx FIFO Status 0000: Rx FIFO empty 0001: Rx FIFO contains 1 data ... 1000: Rx FIFO contains 8 data Others: Reserved
[3:0]	TXFS	Tx FIFO Status 0000: Tx FIFO empty 0001: Tx FIFO contains 1 data ... 1000: Tx FIFO contains 8 data Others: Reserved

SPIn FIFO Time Out Counter Register – SPInFTOCR, n=0 or 1

This register stores the SPIn Rx FIFO time out counter value.

Offset: 0x020

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
TOC								
Type/Reset	RW 0							
23 22 21 20 19 18 17 16								
TOC								
Type/Reset	RW 0							
15 14 13 12 11 10 9 8								
TOC								
Type/Reset	RW 0							
7 6 5 4 3 2 1 0								
TOC								
Type/Reset	RW 0							

Bits	Field	Descriptions
[31:0]	TOC	<p>Time Out Counter</p> <p>The time out counter starts to count from 0 after the SPI RX FIFO receives a data, and reset the counter value once the data is read from the SPIDR register by software or another new data is received. If the FIFO does not receive new data or the software does not read data from the SPIDR register, the time out counter value will continuously increase. When the time out counter value is equal to the TOC setting value, the TO flag in the SPIISR register will be set and an interrupt will be generated if the TOIEN bit in the SPIIEN register is set. The time out counter will be stopped when the RX FIFO is empty. The SPI FIFO time out function can be disabled by setting the TOC field to zero. The time out counter is driven by the system APB clock, named f_{PCLK}.</p>

21 Universal Synchronous Asynchronous Receiver Transmitter (USART)

Introduction

The Universal Synchronous Asynchronous Receiver Transceiver, USART, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. The USART is used to translate data between parallel and serial interfaces, and is also commonly used for RS232 standard communication. The USART peripheral function supports a variety of interrupts.

The USART module includes a 16-byte transmitter FIFO, TX_FIFO, and a 16-byte receiver FIFO, RX_FIFO.

Software can detect a USART error status by reading Line Status Register, LSR. The status includes the type and the condition of the transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

The USART includes a programmable baud rate generator which is capable of dividing the CK_AHB to produce a clock for the USART transmitter and receiver.

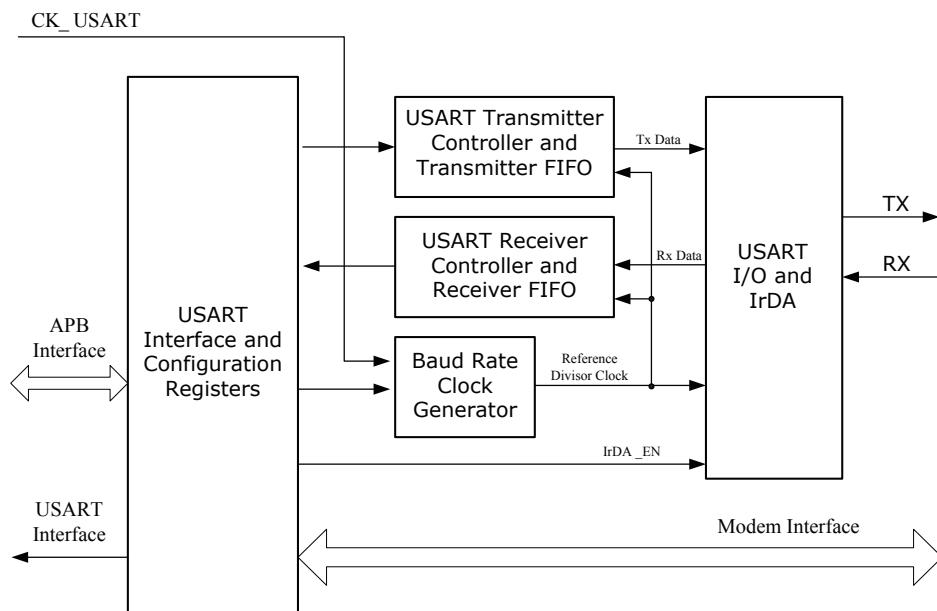


Figure 145. USART Block Diagram

Features

- Supports both asynchronous and clocked synchronous serial communication modes
- Full Duplex Communication Capability
- IrDA SIR encoder and decoder
 - Support of normal 3/16 bit duration and low-power (1.41 ~ 2.23 µs) durations
- Supports RS485 mode with output enable
- Auto hardware flow control mode – RTS, CTS
- Full modem function
- Fully programmable serial communication functions including:
 - Word length: 7, 8, or 9-bit character
 - Parity: Even, odd, or no-parity bit generation and detection
 - Stop bit: 1 or 2 stop bit generation
 - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun, and frame error
- FIFO:
 - Receive FIFO: 16 × 9 bits (max 9 data bits)
 - Transmit FIFO: 16 × 9 bits (max 9 data bits)
- Supports PDMA Interface

Functional Descriptions

Serial Data Format

The USART module performs a parallel-to-serial conversion on data that is read from the Transmitter FIFO and then sends the data with the following format: start bit, 7 ~ 9 LSB first data bits, optional parity bit and finally 1 ~ 2 stop bits. The start bit has the opposite polarity of the data line idle state. The stop bit is the same as the data line idle state and provides a delay before the next start situation. The start and stop bits are both used for data synchronization during the asynchronous data transmission.

The USART module also performs a serial-to-parallel conversion on the data that is read from the Receiver FIFO. It will first check the Parity bit and will then look for a Stop bit. If the Stop bit is not found, the USART module will consider the entire word transmission to have failed and respond with a Framing Error.

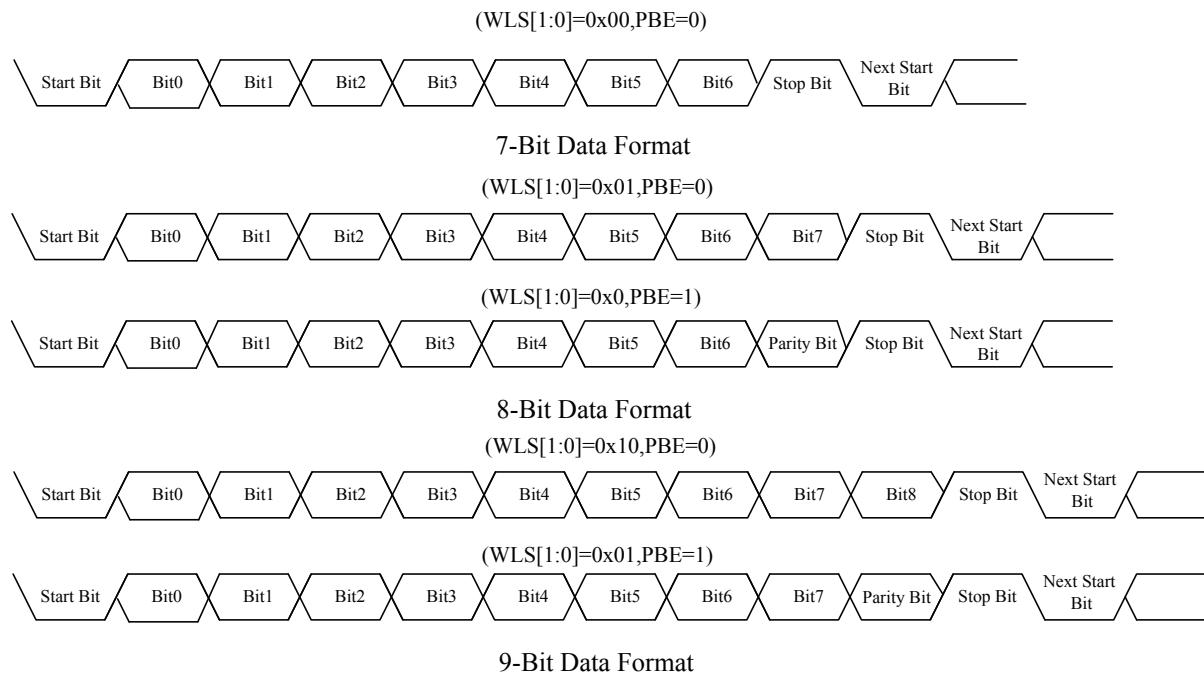


Figure 146. USART Serial Data Format

Baud Rate Generation

The baud rate for the USART receiver and transmitter are both set with the same values. The baud-rate divisor, BRD, has the following relationship with the USART clock which is known as CK_USART.

$$\text{Baud Rate Clock} = \text{CK_USART} / \text{BRD}$$

Where CK_USART clock is the system clock connected to the USART module while the BRD range is from 16 to 65535.

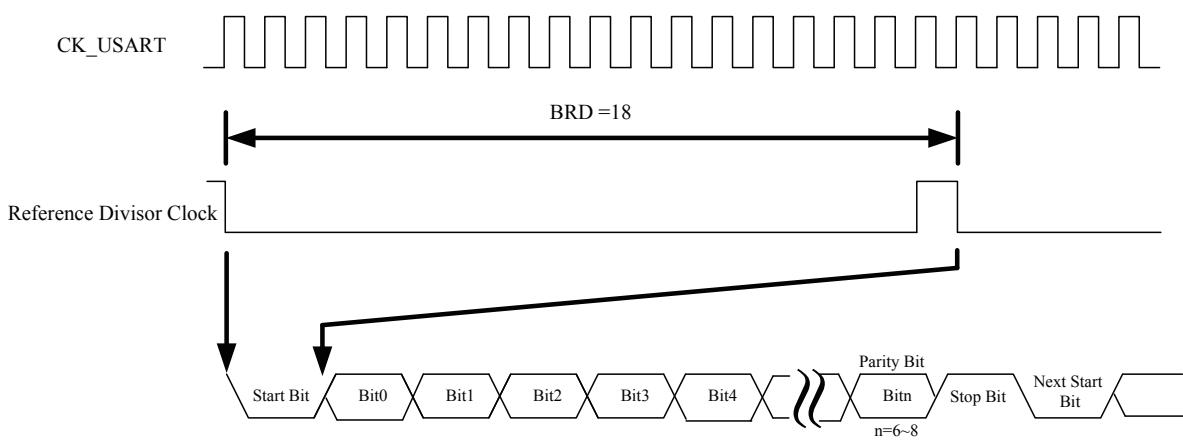


Figure 147. USART Clock CK_USART and Data Frame Timing

Table 52. Baud Rate Error calculation – CK_USART = 72 MHz.

Baud rate		CK_USART = 72 MHz			
No	Kbps	Actual	BRD/16	BRD	Error rate
1	2.4	2.4	1875	30000	0%
2	9.6	9.6	468.75	7500	0%
3	19.2	19.2	234.375	3750	0%
4	57.6	57.6	78.125	1250	0%
5	115.2	115.2	39.0625	625	0%
6	230.4	230.769	19.5	312	0.16%
7	460.8	461.538	9.75	156	0.16%
8	921.6	923.076	4.875	78	0.16%
9	2250	2250	2	32	0%
10	4500	4500	1	16	0%

IrDA

The USART IrDA mode is provided half-duplex point-to-point wireless communication.

The USART module include an integrated modulator and demodulator which allow a wireless communication using infrared transceivers. The transmitter specifies a data ‘0’ as a ‘low’ pulse and a data ‘1’ as a ‘low’ level while the Receiver specifies a data ‘0’ as a ‘low’ pulse and a data ‘1’ as ‘high’ level in the IrDA mode. The IrDA mode provides two operation modes, one is the normal mode, and the other is the low-power mode.

For the IrDA normal mode, the width of each transmitted pulse generated by the transmitter modulator is specified as 3/16th of the baud rate clock period. The receiver pulse width for the IrDA receiver demodulator is based on the IrDA receive debounce filter which is implement using an 8-bit down-counting counter. The debounce filter counter value is specified by the IrDAPSC field in the IrDACR register. When a falling edge is detected on the UR_RX pin, the debounce filter counter starts to count down, driven by the CK_USART clock. If a rising edge is detected on the UR_RX pin, the counter stops counting and is reloaded with the IrDAPSC value. When a low pulse falling edge on the UR_RX pin is detected and then before the debounce filter has counted down to zero, a rising edge is also detected, then this low pulse will be considered as glitch noise and will be discarded. If a low pulse falling edge appears on the UR_RX pin but no rising edge is detected before the debounce counter reaches 0, then the input on the USART receiver pin is regarded as a valid data “0” for this bit duration. The IrDAPSC value must be set to be greater than or equal to 0x01, then the IrDA receiver demodulation operation can function properly. The IrDAPSC value can be adjusted to meet the USART baud rate setting to filter the IrDA received glitch noise of which the width is smaller than the prescaler setting duration.

In the IrDA low-power mode, the transmitted IrDA pulse width generated by the transmitter modulator is not kept at 3/16 of the baud rate clock period. Instead, the pulse width is fixed and is calculated by the following formula. The transmitted pulse width can be adjusted by the IrDAPSC field to meet the minimum pulse width specification of the external IrDA Receiver device.

$$T_{\text{IrDA_L}} = 3 \times \text{IrDAPSC} / \text{CK_USART}$$

Note: $T_{\text{IrDA_L}}$ is transmitted pulse width in the low power mode.

The IrDAPSC filed in the IrDACR prescaler value in the IrDA Control Register IrDACR.

The debounce behavior in the IrDA low-power receiving mode is similar to the IrDA normal mode. For glitch detection, the low pulse of which the pulse width is shorter than $1 \times (\text{IrDAPSC} / \text{CK_USART})$ should be discarded in the IrDA receiver demodulation. A valid low data is accepted if its low pulse width is greater than $2 \times (\text{IrDAPSC} / \text{CK_USART})$ duration.

The IrDA physical layer specification specifies a minimum delay with a value of 10 ms between the transmission and reception and this IrDA receiver set-up time should be managed by the software.

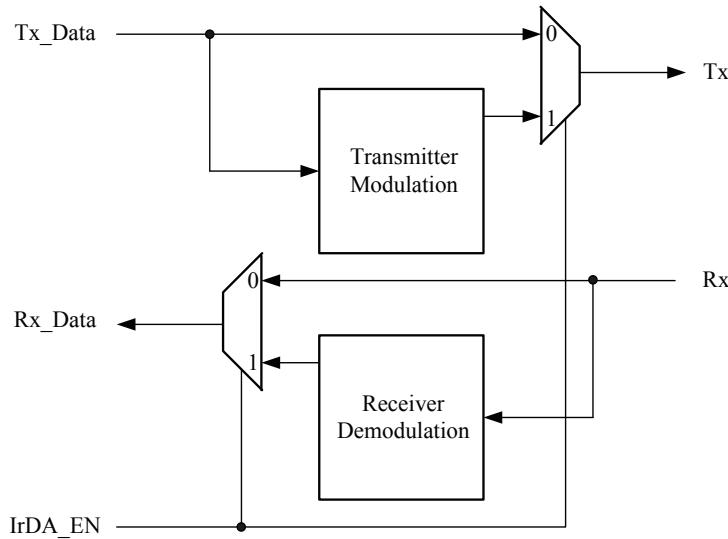


Figure 148. USART I/O and IrDA Block Diagram

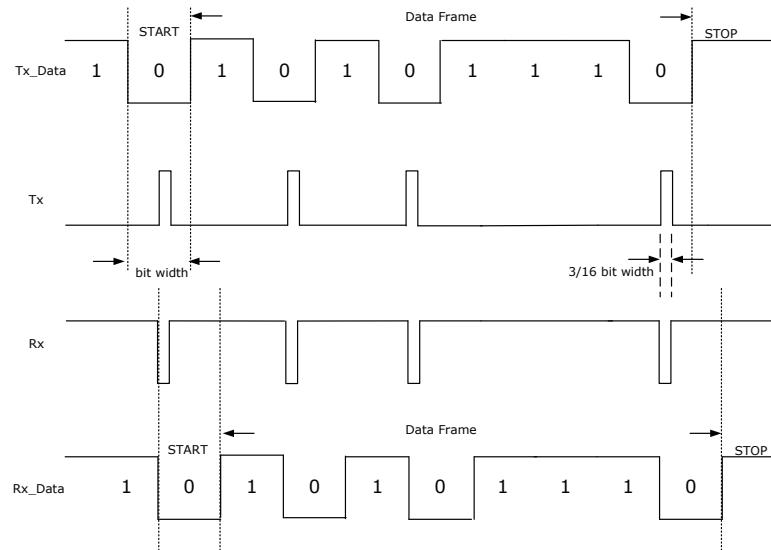


Figure 149. IrDA Modulation and Demodulation

RS485 Mode

The data on RS485 interface is transmitted over a 2-wire twisted pair bus. The RS485 transceiver interprets the voltage levels of the differential signals with respect to a third common voltage. Without this common reference, the transceiver may interpret the differential signals incorrectly. This enhances the noise rejection capabilities of the RS485 interface. The UR_RTS pin is used to control the external RS485 transceiver whose polarity can be selected by configuring the TXENP bit in the RS485 Control Register, named RS485CR, when the USART module operates in the RS485 mode.

RS485 Auto Direction Mode – AUD

When the RS485 interface is configured as a master transmitter, it will operate in the Auto Direction Mode, AUD. In the AUD mode the polarity of the UR_RTS pin is configurable according to the TXENP bit in the RS485 Control Register in the RS485 mode. This pin can be used to control the external RS485 transceiver to enable the transmitter.

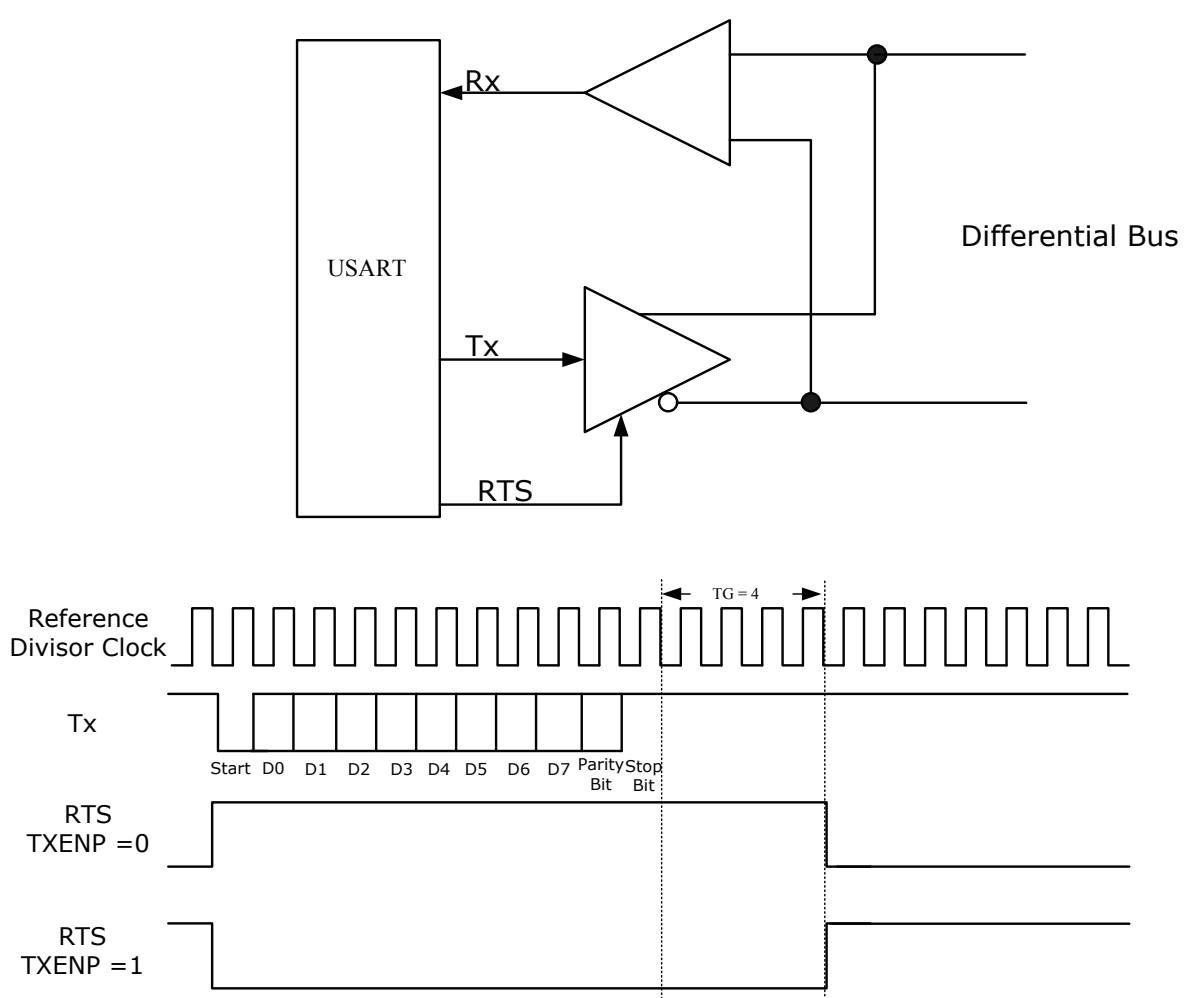


Figure 150. RS485 Interface and Waveform

RS485 Normal Multi-drop Operation Mode (NMM)

When the RS485 interface is configured as an addressable slave, it will operate in the Normal Multi-drop Operation Mode, NMM. This mode is enabled when the RSNMM field is set in the RS485CR register. Regardless of the URRXEN value in the FCR register, all the received data with a parity bit “0” will be ignored until the first address byte is detected with a parity bit “1” and then the received address byte will be stored in the RXFIFO. Once the first address data is detected and stored in the RXFIFO, the RSADDEF flag in the LSR register will be set and generate an interrupt if the RLSIE bit in the IER register is set to 1. Application software can determine whether the receiver is enabled or disabled to accept the following data by configuring the URRXEN bit. When the receiver is enabled by setting the URRXEN bit to 1, all received data will be stored in the RXFIFO. Otherwise, all received data will be ignored if the receiver is disabled by clearing the URRXEN bit to 0.

RS485 Auto Address Detection Operation Mode (AAD)

Except in the Normal Multi-drop Operation Mode, the RS485 interface can operate in the Auto Address Detection Operation Mode, AAD, when it is configured as an addressable slave. This mode is enabled by setting the RSAAD filed to 1 in the RS485CR register. The receiver will detect the address frame with a parity bit “1” and then compare the received address data with the ADDMATCH field value which is a programmable 8-bit address value specified in the RS485CR register. If the address data matches the ADDMATCH value, it will be stored in the RXFIFO and the URRXEN bit will be automatically set. When the receiver is enabled, all received data will be stored in the RXFIFO until the next address frame does not match the ADDMATCH value and then the receiver will be automatically disabled. After the receiver is enabled, software can disable the receiver by setting the URRXEN bit to ‘0’.

Synchronous Mode

The data is transmitted in a full-duplex style in the USART Synchronous Master Mode, i.e., data transmission and reception both occur at the same time and only support master mode. The USART UR_CTS/SCK pin is the synchronous USART transmitter clock output. In this mode, no clock pulses will be sent to the UR_CTS pin during the start bit, parity bit and stop bit duration. The CPS bit in the Synchronous Control Register, SYNCR, can be used to determine whether data is captured on the first or the second clock edge. The CPO bit in the SYNCR can be used to configure the clock polarity in the USART Synchronous Mode idle state. Detailed timing information is shown in the accompanying diagram.

In the USART synchronous Mode, the UR_CTS/SCK clock output pin is only used to transmit the data to slave device. If the transmission data register TBR, is written with valid data, the USART synchronous mode will automatically transmit this data with the corresponding clock output and the USART receiver will also receive data on the UR_RX pin. Otherwise the receiver will not obtain synchronous data if no data is transmitted.

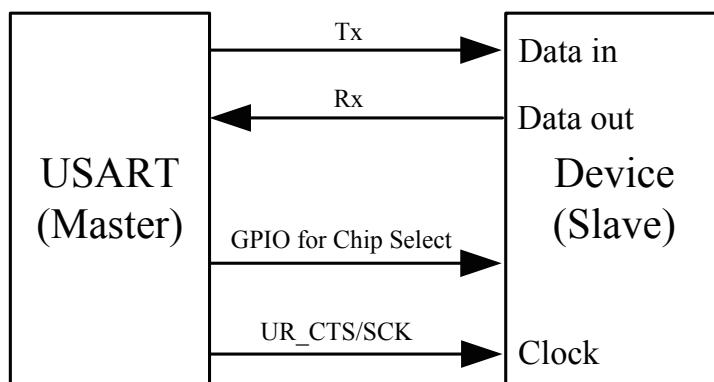


Figure 151. USART Synchronous Transmission Example

Note: The USART supports the synchronous master mode only: it cannot receive or send data related to an input clock. The USART clock is always an output.

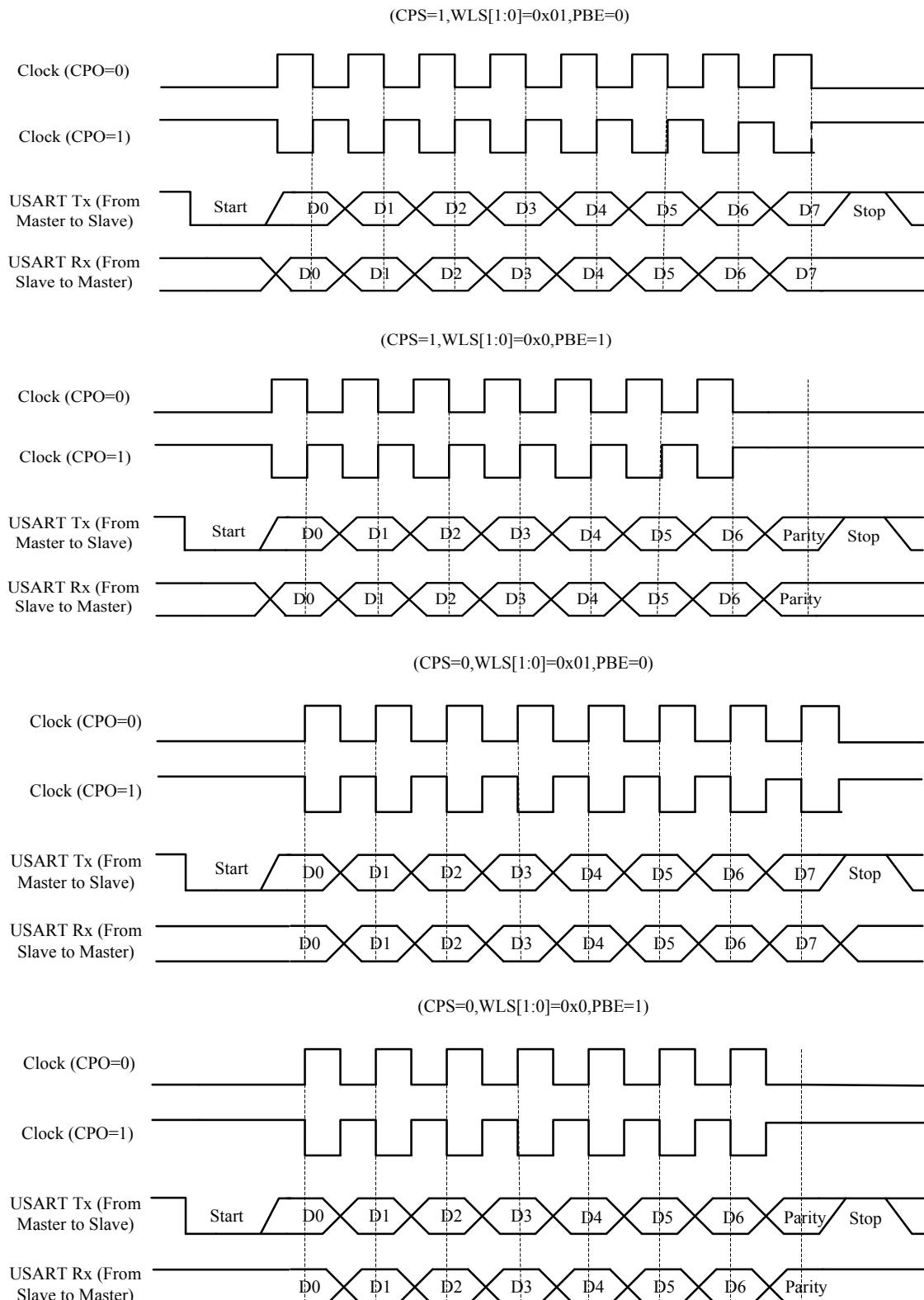


Figure 152. 8-bit Format USART Synchronous Waveform

Hardware Flow Control

The RS485 interface supports the hardware flow control function which is enabled by setting the HFCEN bit in the MODCR register to 1. The hardware flow control function is categorized into two types. One is the RTS flow control function and the other is the CTS flow control function.

RTS Flow Control

In the RTS flow control, the UR_RTS pin is active with a logic low state when the RX FIFO is empty. It means that the receiver is ready to receive a new data. When the RX FIFO reaches the trigger level which is specified by configuring the RFTL field in the FCR register, the UR_RTS pin is inactive with a logic high state. Figure 153 shows the example of RTS flow control.

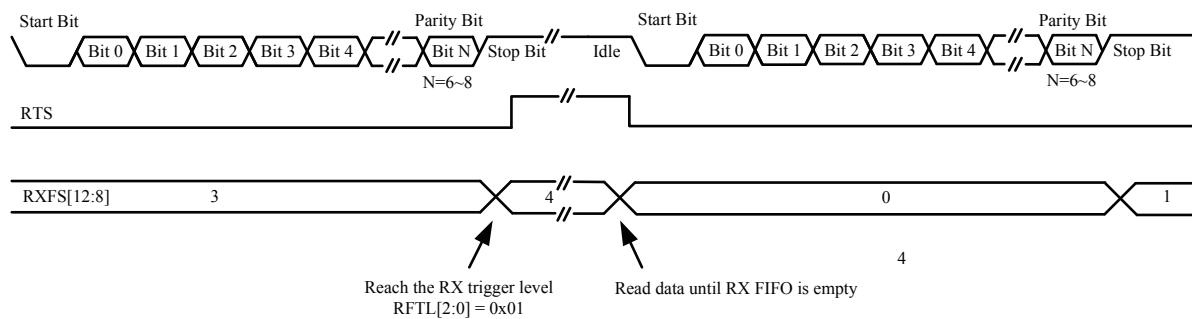


Figure 153. USART RTS Flow Control

CTS Flow Control

If the hard flow control function is enabled, the URTXEN bit in the FCR register is controlled by the UR_CTS input signal. If the UR_CTS pin is forced to a logic low state, the URTXEN bit will automatically be set to 1 to enable the data transmission. However, if the UR_CTS pin is forced to a logic high state, the URTXEN bit will be cleared to 0 and then the data transmission will also be disabled.

When the UR_CTS pin is forced to a logic high state during a data transmission, the current data transmission will be continued until the stop bit is completed. The figure 154 shows an example of communication with CTS flow control.

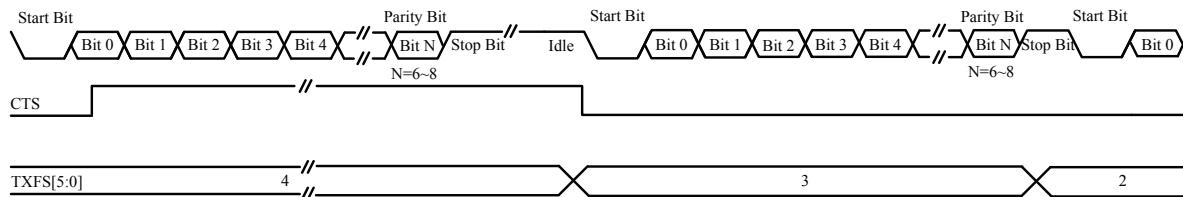


Figure 154. USART CTS flow control

Interrupts and Status

The USART module can generate an interrupt when the following event occurs:

- Receiver Line Status Interrupt (Irpt_RLSI): Occurrence of USART overrun error, parity error, framing error, or break events.
- Receiver FIFO Threshold Level Interrupt (Irpt_RFTLI): When the FIFO received data amount has reached the specified threshold level.
- Receiver FIFO Time-out Interrupt (Irpt_RTOI): When the USART receiver FIFO does not receive a new data package during the specified time-out interval.
- Transmitter FIFO Threshold Level Interrupt (Irpt_TFTLI): When the data to be transmitted in the USART transmitter FIFO is less than the specified threshold level.
- MODEM Status Interrupt (Irpt_MODSI): When the DCD, RI, DSR, or CTS bits states in the MODSR register have changed

PDMA Interface

The PDMA interface is integrated in the USART module. The PDMA function can be enabled by setting the TXDMAEN or RXDMAEN bit in the MDR register to 1 in the transmitter or receiver mode respectively. When the data to be transmitted in the USART transmitter FIFO is less than the TX FIFO threshold level specified by the TFTL field in the FCR register and the TXDMAEN bit is set to 1, the PDMA function will be activated to move data from a certain memory location into the USART TX FIFO.

Similarly, when the received data amount in the receiver FIFO is equal to the RX FIFO threshold level specified by the RFTL field in the FCR register and the RXDMAEN bit is set to 1, the PDMA function will be activated to move data from the USART RX FIFO to a specific memory location.

For a more detailed description on the PDMA configurations, refer to the PDMA chapter.

Register Map

The following table shows the USART registers and reset values.

Table 53. USART Register Map

Register	Offset	Description	Reset Value
USART0 Base Address = 0x4000_0000			
USART1 Base Address = 0x4004_0000			
RBRn	0x000	USARTn Receiver Buffer Register	0x0000_0000
TBRn	0x000	USARTn Transmitter Buffer Register	0x0000_0000
IERN	0x004	USARTn Interrupt Enable Register	0x0000_0000
IIRn	0x008	USARTn Interrupt Identification Register	0x0000_0001
FCRn	0x00C	USARTn FIFO Control Register	0x0000_0001
LCRn	0x010	USARTn Line Control Register	0x0000_0000
MODCRn	0x014	USARTn Modem Control Register	0x0000_0000
LSRn	0x018	USARTn Line Status Register	0x0000_0060
MODSRn	0x01C	USARTn Modem Status Register	0x0000_0000
TPRn	0x020	USARTn Timing Parameter Register	0x0000_0000
MDRn	0x024	USARTn Mode Register	0x0000_0000
IrDACRn	0x028	USARTn IrDA Control Register	0x0000_0000
RS485CRn	0x02C	USARTn RS485 Control Register	0x0000_0000
SYNCRn	0x030	USARTn Synchronous Control Register	0x0000_0000
FSRn	0x034	USARTn FIFO Status Register	0x0000_0000
DLRn	0x038	USARTn Divider Latch Register	0x0000_0010
DEGTSTRn	0x040	USARTn Debug/Test Register	0x0000_0000

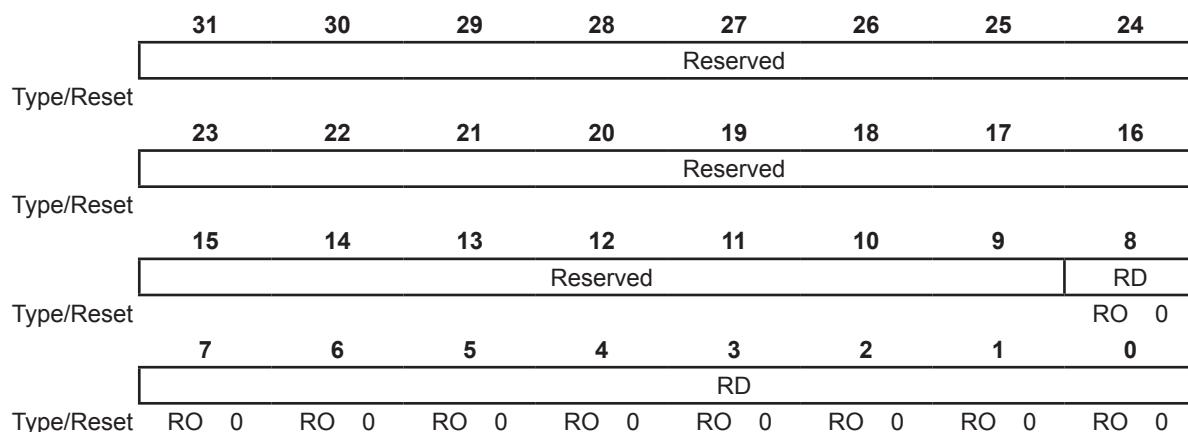
Register Descriptions

USARTn Receiver Buffer Register – RBRn, n = 0 or 1

The register is used to store the USARTn received data.

Offset: 0x000

Reset value: 0x0000_0000



Bits	Field	Descriptions
[8:0]	RD	Reading the data via this receiver buffer register will return the data from the receiver FIFO. The receiver FIFO has a capacity of up to 16×9 bits. By reading this register, the USART will return a 7, 8 and 9-bit received data. The RD field bit 8 is valid for 9-bit mode only and is fixed at 0 for the 8-bit mode. For the 7-bits mode, the receiver buffer register RD[6:0] contain the available bits.

USARTn Transmitter Buffer Register – TBRn, n = 0 or 1

The register is used to specify the USARTn transmitted data.

Offset: 0x000

Reset value: 0x0000_0000



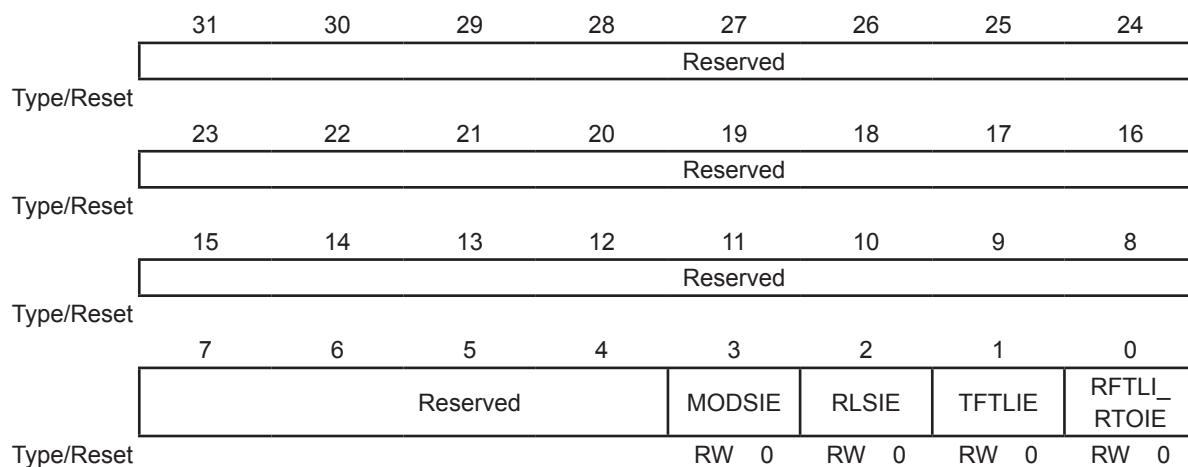
Bits	Field	Descriptions
[8:0]	TD	<p>Writing data to this transmitter buffer register will load data into the transmitter FIFO. The transmitter FIFO has a capacity of up to 16×9 bits.</p> <p>By writing to this register, the USART will send out 7,8 or 9-bit transmitted data. The TD field bit 8 is valid for the 9-bit mode only and will be ignored for the 8-bit mode. For the 7-bit mode, the transmitter buffer register TD [6:0] contains the available bits.</p>

USARTn Interrupt Enable Register – IERn, n = 0 or 1

This register is used to enable or disable the related USARTn interrupt function. The USARTn module generates interrupts to the controller when the corresponding events occur and the corresponding interrupt enable bits are set.

Offset: 0x004

Reset value: 0x0000_0000



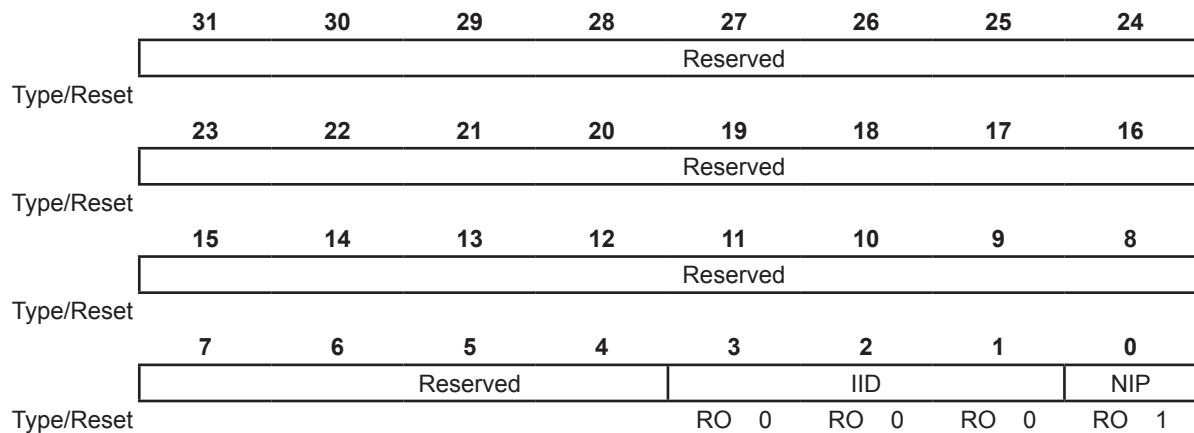
Bits	Field	Descriptions
[3]	MODSIE	MODEM Status Interrupt Enable (Irpt_MODSI) 0: Mask off Irpt_MODSI 1: Enable Irpt_MODSI
[2]	RLSIE	Receive Line Status Interrupt Enable (Irpt_RLSI) 0: Mask off Irpt_RLSI 1: Enable Irpt_RLSI
[1]	TFTLIE	Transmitter FIFO Threshold Level Interrupt (Irpt_TFTLI) Enable 0: Mask off Irpt_TFTLI 1: Enable Irpt_TFTLI
[0]	RFTLI_RTOIE	Receiver FIFO Threshold Level Interrupt Enable (Irpt_RFTLI) or receiver FIFO Time-Out Interrupt Enable (Irpt_RTOI) 0: Mask off Irpt_RFTLI and Irpt_RTOI 1: Enable Irpt_RFTLI or Irpt_RTOI

USARTn Interrupt Identification Register – IIRn, n = 0 or 1

This register is used to identify the interrupt source including the FIFO threshold and USARTn Receiver/Transmitter status.

Offset: 0x008

Reset value: 0x0000_0001



Bits	Field	Descriptions
[3:1]	IID	Interrupt Identification. The detailed interrupt descriptions are shown in the accompanying table. The IID and NIP bits indicate the current USART interrupt request.
[0]	NIP	No Interrupt Pending 1; No pending USART interrupt. 0: Pending USART interrupts.

Table 54. USART Interrupt Control Function

IID & NIP	Priority	Interrupt Type	Interrupt Source	Interrupt Reset control
xxx1	NA	None	None	NA
0110	Highest	Receiver Line Status Interrupt (Irpt_RLSI)	USART occurs overrun error, parity error, framing error, or break events. [note] In RS485 mode, it can indicate the address detection.	Reading the LSR register.
0100	Second	Receiver FIFO Threshold Level Interrupt (Irpt_RFTLI)	Receiver FIFO threshold level is reached	Read the RBR register to decrease the receiver FIFO level to less than the specified threshold.
1100	Second	Receiver FIFO Time-out Interrupt (Irpt_RTOI)	Receiver FIFO is not empty and no activities have occurred in the receiver FIFO during the RTOIC time-out duration	Reading the RBR register
0010	Third	Transmitter FIFO Threshold Level Interrupt (Irpt_TFTLI)	Transmitter FIFO level is less than the transmitter FIFO threshold level which is set by the TFTL field in the FIFO Control Register named FCR.	Writing data into the TBR register.
0000	Fourth	MODEM Status Interrupt (Irpt_MODSI)	The DCDS, RIS, DSRS, or CTSS bits in the MODSR register have changing state.	Reading the MODSR register– optional

USARTn FIFO Control Register – FCRn, n = 0 or 1

This register specifies the USARTn FIFO control and configurations including threshold level and reset function.

Offset: 0x00C

Reset value: 0x0000_0001

	31	30	29	28	27	26	25	24	
Type/Reset	Reserved								
	23	22	21	20	19	18	17	16	
Type/Reset	Reserved								
	15	14	13	12	11	10	9	8	
Type/Reset	Reserved						URRXEN	URTXEN	
	7	6	5	4	3	2	1	0	
Type/Reset	RW 0	RW 0	RW 0	RW 0	Reserved	TFR	RFR	FME	
						WO 0	WO 0	RO 1	

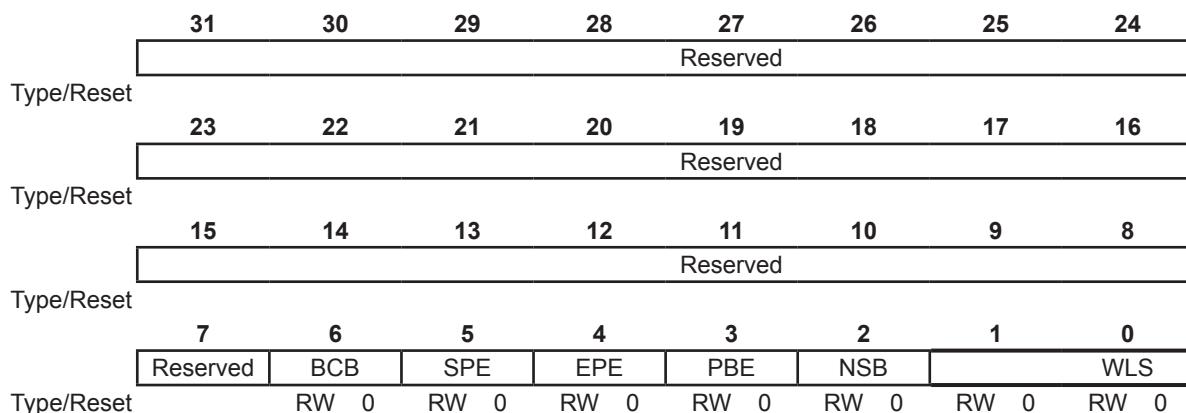
Bits	Field	Descriptions
[9]	URRXEN	USART RX Enable 0: disable 1: enable
[8]	URTXEN	USART TX Enable 0: disable 1: enable
[7:6]	RFTL	RX FIFO Threshold Level Setting The RFTL field defines the RX FIFO trigger level. 00: 1 byte 01: 4bytes 10: 8 bytes 11: 14bytes
[5:4]	TFTL	TX FIFO Threshold Level Setting The TFTL field determines the TX FIFO trigger level. 00: 0 byte 01: 2bytes 10: 4bytes 11: 8 bytes
[2]	TFR	TX FIFO Reset Setting this bit will generate a reset pulse to reset TX FIFO which will empty the TX FIFO. i.e., the TX pointer will be reset to 0, after a reset signal. This bit returns to 0 automatically after the reset pulse is generated.
[1]	RFR	RX FIFO Reset Setting this bit will generate a reset pulse to reset the RX FIFO which will empty the RX FIFO. i.e., the RX pointer will be reset to 0, after a reset signal. This bit returns to 0 automatically after the reset pulse is generated.
[0]	FME	FIFO Mode Enable Because the USART module is always operated in the FIFO mode, writing to this bit will have no effect.

USARTn Line Control Register – LCRn, n = 0 or 1

The line control register specifies the serial parameters such as data length, parity, and stop bit for the USARTn module.

Offset: 0x010

Reset value: 0x0000_0000



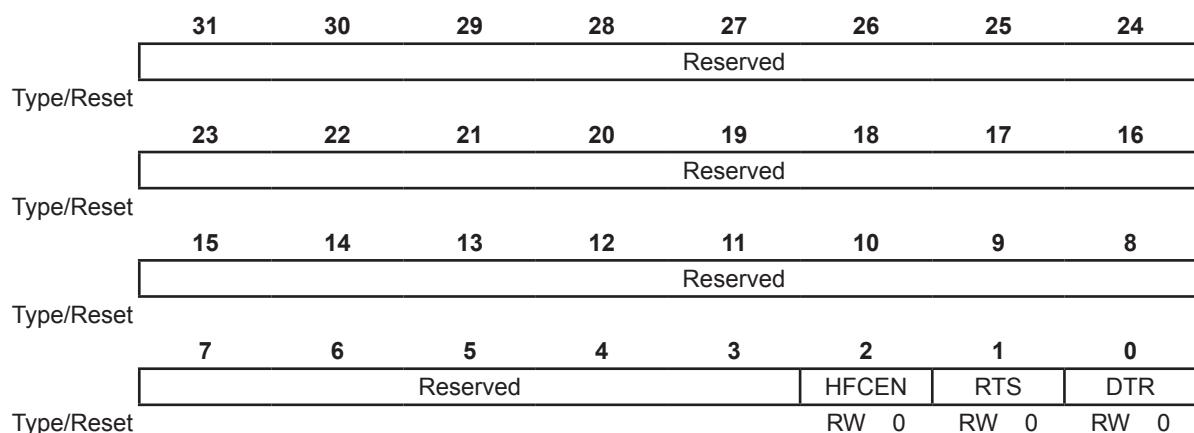
Bits	Field	Descriptions
[6]	BCB	Break Control Bit When this bit is set 1, the serial data output on the UR_TX pin will be forced to the Spacing State (logic 0). This bit acts only on UR_TX output pin and has no effect on the transmitter logic.
[5]	SPE	Stick Parity Enable 0: Disable stick parity 1: Stick Parity bit is transmitted This bit is only available when the PBE bit is set to 1. If both the PBE and SPE bits are set to 1 and the EPE bit is cleared to 0, the transmitted parity bit will be set to 1. However, when the PBE and SPE bits are set to 1 and also the EPE bit is set to 1, the transmitted parity bit will be cleared to 0.
[4]	EPE	Even Parity Enable 0: Odd number of logic 1's are transmitted or checked in the data word and parity bits. 1: Even number of logic 1's are transmitted or checked in the data word and parity bits. This bit is only available when PBE is set to 1.
[3]	PBE	Parity Bit Enable 0: Parity bit is not generated (transmitted data) or checked (receive data) during transfer. 1: Parity bit is generated or checked during transfer. Note: When the WLS field is set to "10" to select the 9-bit data format, writing to the PBE bit has no effect.
[2]	NSB	Number of "STOP bit" 0: One "STOP bit" is generated in the transmitted data 1: Two "STOP bit" is generated when 8- and 9-bit word length is selected.
[1:0]	WLS	Word Length Select 00: 7 bits 01: 8 bits 10: 9 bits 11: Reserved

USARTn Modem Control Register – MODCRn, n = 0 or 1

This register contains a related modem control.

Offset: 0x014

Reset value: 0x0000_0000



Bits	Field	Descriptions
[2]	HFCEN	Hardware Flow Control Function Enable 0: Disabled 1: Enabled
[1]	RTS	RTS - Request-To-Send Signal 0: Drive UR_RTS pin to logic 1 1: Drive UR_RTS pin to logic 0 Note that the RTS bit is used to control the UR_RTS pin status when the HFCEN bit is set.
[0]	DTR	DTR (Data-Terminal-Ready) Signal 0: Drive DTR pin to logic 1 1: Drive DTR pin to logic 0

USARTn Line Status Register – LSRn, n = 0 or 1

This register contains the corresponding USARTn status.

Offset: 0x018

Reset value: 0x0000_0060

	31	30	29	28	27	26	25	24	
Type/Reset	Reserved								
	23	22	21	20	19	18	17	16	
Type/Reset	Reserved								
	15	14	13	12	11	10	9	8	
Type/Reset	Reserved							RSADDEF	
	7	6	5	4	3	2	1	0	
Type/Reset	ERRRX	TXEMPT	TXFEMPT	BII	FEI	PEI	OEI	RFDR	
	RC 0	RO 1	RO 1	RC 0	RC 0	RC 0	RC 0	RO 0	

Bits	Field	Descriptions
[8]	RSADDEF	RS485 Address Detection Flag 0: Address is not detected 1: Address is detected This bit is set to 1 when the receiver detects the address and is cleared to 0 when the LSR register is read. Note: This bit is only used in the RS485 mode by setting the MDR field to "b10".
[7]	ERRRX	RX FIFO Error 0: RX FIFO works normally 1: There is at least one parity error (PE), framing error (FE), or break indication (BI) in the receiver FIFO. The ERRRX bit is cleared when the CPU reads the LSR register and if there are no subsequent errors in the RX FIFO
[6]	TXEMPT	Transmitter Empty 0: Either Transmitter FIFO (TX FIFO) or Transmitter Shift Register (TSR) is not empty. 1: Both the TX FIFO and TSR register are empty.
[5]	TXFEMPT	Transmitter FIFO Empty 0: TX FIFO is not empty. 1: TX FIFO is empty. The TXFEMPT bit is set when the last data package in the TX FIFO is transferred to the Transmitter Shift Register (TSR). This bit is reset when the TBR (or TX FIFO) is loaded with new data. This bit also causes the USART to issue an interrupt (Irpt_TFTLI) to the CPU when the TFTLIE bit in the IER register is set to 1 to enable the relevant interrupt and when the TFTL field in the FCR register is set to the value 0.
[4]	BII	Break Interrupt Indicator This bit is set to 1 whenever the received data input is held in the "spacing state" (logic 0) for longer than a full word transmission time, which is the total time of "start bit" + data bits + "parity" + "stop bits" duration, and is reset whenever the CPU reads the contents of this LSR register.

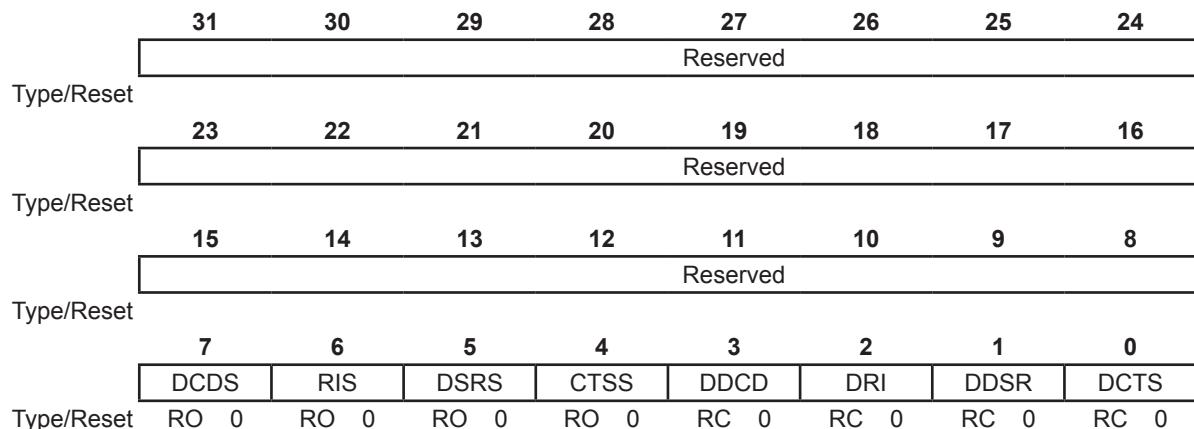
Bits	Field	Descriptions
[3]	FEI	Framing Error Indicator This bit is set 1 whenever the received character does not have a valid "stop bit", which means, the stop bit following the last data bit or parity bit is detected as a logic 0, and is reset whenever the CPU reads the contents of this LSR register.
[2]	PEI	Parity Error Indicator This bit is set to 1 whenever the received character does not have a valid "parity bit" and is reset whenever the CPU reads the contents of this LSR register.
[1]	OEI	Overrun Error Indicator An overrun error will occur only after the RX FIFO is full and when the next character has been completely received in the RX shift register. The character in the shift register is overwritten, when an overrun event occurs, but it is not transferred to the RX FIFO. The OEI bit is used to indicate to the CPU as soon as it happens and is reset whenever the CPU reads the contents of this LSR register.
[0]	RFDR	RX FIFO Data Ready 0: RX FIFO is empty 1: RX FIFO contains at least 1 received data word.

USARTn Modem Status Register – MODSRn, n = 0 or 1

This register contains the USARTn modem status bits.

Offset: 0x01C

Reset value: 0x0000_0000



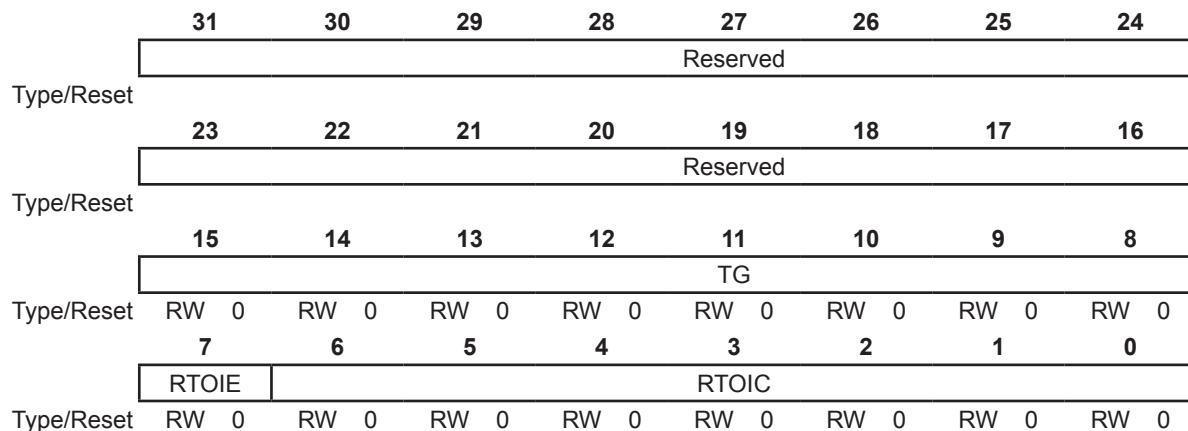
Bits	Field	Descriptions
[7]	DCDS	DCD - Data-Carrier-Detect Status 0: UR_DCD pin is inactive. 1: UR_DCD pin is active and kept at a "0" state.
[6]	RIS	UR_RI Ring-Indicator Status 0: UR_RI pin is inactive 1: UR_RI pin is active and kept at a "0" state
[5]	DSRS	UR_DSR Data-Set-Ready Status 0: UR_DSR pin is inactive 1: UR_DSR pin is active and kept at a "0" state
[4]	CTSS	UR_CTS Clear-To-Send Status 0: UR_CTS pin is inactive 1: UR_CTS pin is active and kept at a "0" state
[3]	DDCD	Detect UR_DCD Status Change This bit is set whenever the UR_DCD input pin status has been changed and will be reset if the CPU reads this MODSR register. When the DDCD bit is set to 1, a modem status interrupt is generated if the MODSIE bit in the IER register is set to 1.
[2]	DRI	Detect UR_RI Status Change This bit is set whenever the UR_RI input pin status has been changed and will be reset if the CPU reads the MODSR register. When the DIR bit is set to 1, a modem status interrupt is generated if the MODSIE bit in the IER register is set to 1.
[1]	DDSR	Detect UR_DSR Status Change This bit is set whenever the UR_DSR input pin status has been changed and will be reset if the CPU reads the MODSR register. When the DDSR bit is set to 1, a modem status interrupt is generated if the MODSIE bit in the IER register is set to 1.
[0]	DCTS	Detect UR_CTS Status Change This bit is set whenever the UR_CTS input pin status has been changed and will be reset if the CPU reads the MODSR register. When the DCTS bit is set to 1, a modem status interrupt is generated if the MODSIE bit in the IER register is set to 1.

USARTn Timing Parameter Register – TPRn, n = 0 or 1

This register contains the USARTn timing parameters including the transmitter time guard parameters and the receiver FIFO time-out value together with the RX FIFO time-out interrupt enable control.

Offset: 0x020

Reset value: 0x0000_0000



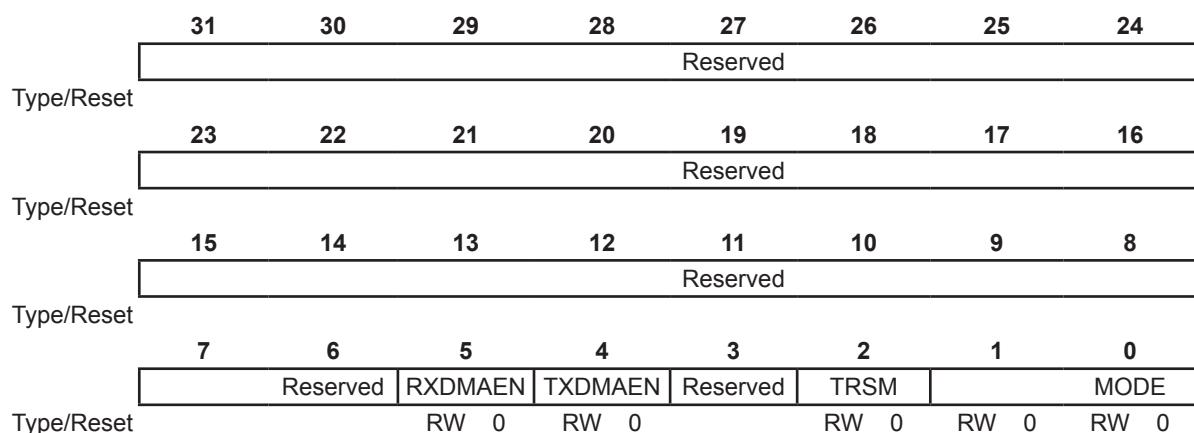
Bits	Field	Descriptions
[15:8]	TG	Transmitter Time Guard The transmitter time guard counter is driven by the baud rate clock. When the TX FIFO transmits data, the counter is reset and then starts to count. Only when the counter content is equal to the TG value, are further word transmission transactions allowed.
[7]	RTOIE	Receiver FIFO Time Out Interrupt Enable The receiver FIFO time-out interrupt is enabled only when the RFTLI_RTOIE bit in the IER register is set to 1.
[6:0]	RTOIC	Receiver FIFO Time-Out Interrupt Compare value The RX FIFO time-out counter, TOUT_CNT, is driven by the baud rate clock. When the RX FIFO receives new data, the counter is reset and then starts to count. Once the time-out counter content is equal to the time-out interrupt compare RTOIC value, a receiver FIFO time-out interrupt, Irpt_RTOI, is generated if the RFTLI_RTOIE bit in the IER register is set to 1. New received data or the empty RX FIFO after being read will clear the RX FIFO time-out counter.

USARTn Mode Register – MDRn, n = 0 or 1

This register specifies the USARTn mode and the data transfer mode selections.

Offset: 0x024

Reset value: 0x0000_0000



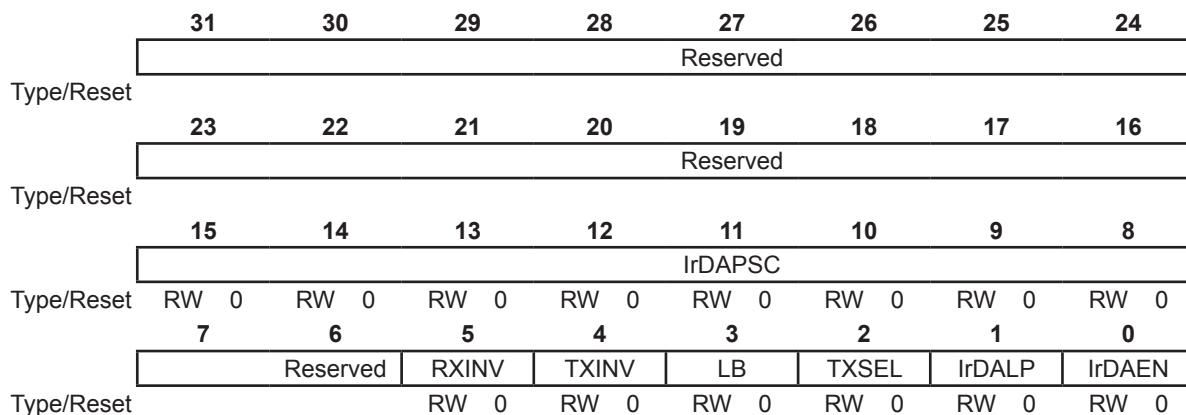
Bits	Field	Descriptions
[5]	RXDMAEN	USART RX DMA Enable 0: Disabled 1: Enabled
[4]	TXDMAEN	USART TX DMA Enable 0: Disabled 1: Enabled
[2]	TRSM	Transfer Mode Selection This bit is used to select the data transfer protocol. 0: LSB first 1: MSB first
[1:0]	MODE	USART Mode Selection. 00: Normal operation 01: IrDA 10: RS485 11: Synchronous

USARTn IrDA Control Register – IrDACPn, n = 0 or 1

This register is the IrDA control register for the USART.

Offset: 0x028

Reset value: 0x0000_0000



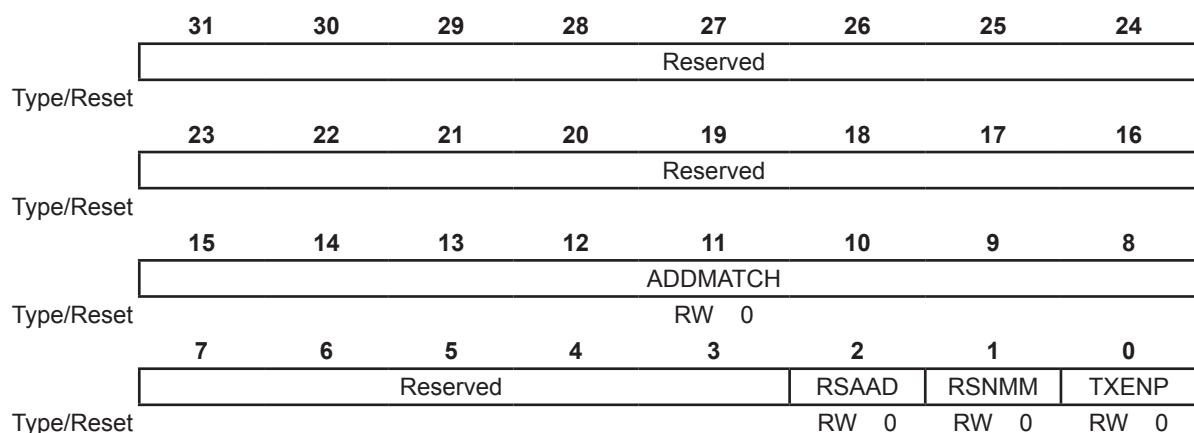
Bits	Field	Descriptions
[15:8]	IrDAPSC	<p>IrDA Prescaler value</p> <p>This field contains the 8-bit debounce prescaler value.</p> <p>The debounce count-down counter is driven by the USART clock, named as CK_USART. The counting period is specified by the IrDAPSC field. The IrDAPSC field must be set to a value equal to or greater than 0x01 to for normal debounce counter operation. If the pulse width is less than the duration specified by the IrDAPSC field, the pulse will be considered as glitch noise and discarded.</p> <ul style="list-style-type: none"> 00000000: Reserved – can not be used. 00000001: CK_USART clock divided by 1 00000010: CK_USART clock divided by 2 00000011: CK_USART clock divided by 3 ...
[5]	RXINV	<p>RX Signal Inverse Control</p> <ul style="list-style-type: none"> 0: No inversion 1: RX input signal is inversed
[4]	TXINV	<p>TX Signal Inverse Control</p> <ul style="list-style-type: none"> 0: No inversion 1: TX output signal is inversed
[3]	LB	<p>IrDA Loop Back Mode</p> <ul style="list-style-type: none"> 0: Disable IrDA loop back mode 1: Enable IrDA loop back mode for self testing.
[2]	TXSEL	<p>Transmit Select</p> <ul style="list-style-type: none"> 0: Enable IrDA receiver 1: Enable IrDA transmitter
[1]	IrDALP	<p>IrDA Low Power Mode</p> <p>Select the IrDA operation mode.</p> <ul style="list-style-type: none"> 0: Normal mode 1: IrDA low power mode
[0]	IrDAEN	<p>IrDA Enable control</p> <ul style="list-style-type: none"> 0: Disable IrDA mode 1: Enable IrDA mode

USARTn RS485 Control Register – RS485CRn, n = 0 or 1

This register contains the USARTn UR_RTS/TXE pin polarity for the RS485 mode.

Offset: 0x02C

Reset value: 0x0000_0000



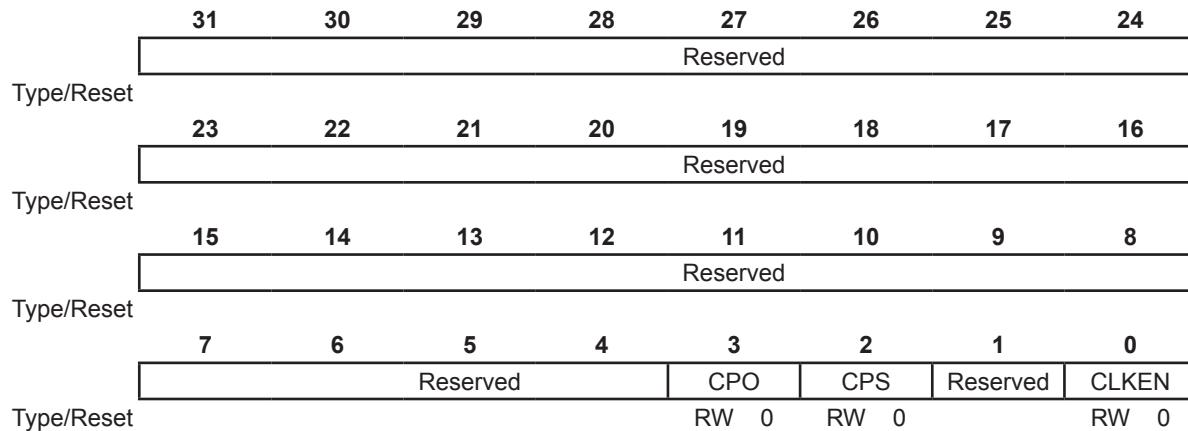
Bits	Field	Descriptions
[15:8]	ADDMATCH	RS485 Auto Address Match value The field contains the address match value for the RS485 auto address detection operation mode.
[2]	RSAAD	RS485 Auto Address Detection Operation Mode Control 0: Disable 1: Enable
[1]	RSNMM	RS485 Normal Multi-drop Operation Mode Control 0: Disable 1: Enable
[0]	TXENP	UR_RTS/TXE Pin Polarity 0: UR_RTS/TXE is active high in the RS485 transmission mode 1: UR_RTS/TXE is active low in the RS485 transmission mode.

USARTn Synchronous Control Register – SYNCR_n, n = 0 or 1

This register is used to control the USARTn synchronous clock pin and the clock polarity together with the clock phase for the synchronous mode.

Offset: 0x030

Reset value: 0x0000_0000



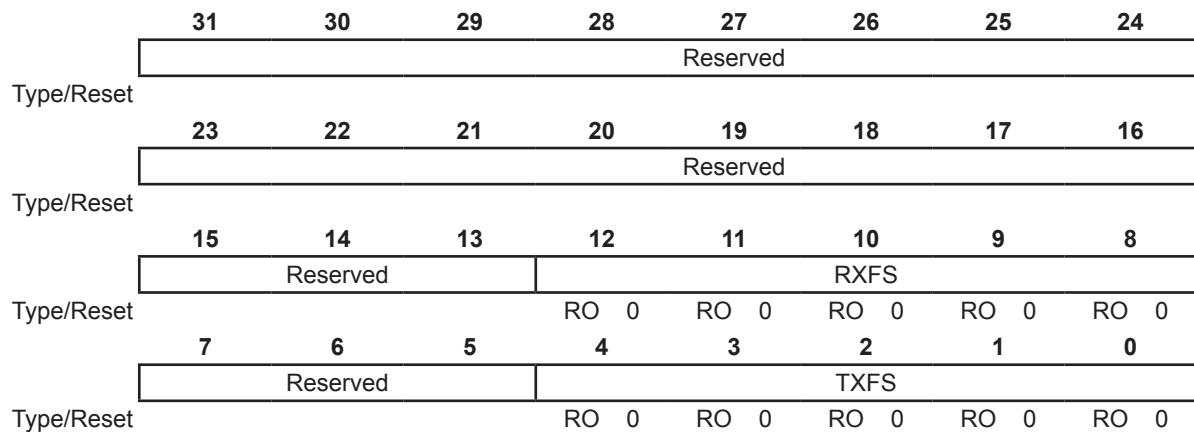
Bits	Field	Descriptions
[3]	CPO	<p>Clock Polarity</p> <p>Selects the polarity of the clock output on the UR_CTS/SCK pin in the synchronous mode. Works in conjunction with the CPS bit to specify the desired clock idle state.</p> <p>0: UR_CTS/SCK pin idle state is low. 1: UR_CTS/SCK pin idle state is high.</p>
[2]	CPS	<p>Clock Phase</p> <p>This bit allows the user to select the phase of the clock output on the UR_CTS/SCK pin in the synchronous mode. Works in conjunction with the CPO bit to determine the data capture edge.</p> <p>0: Data is captured on the first clock edge. 1: Data is captured on the second clock edge.</p>
[0]	CLKEN	<p>Clock Enable</p> <p>Enable/disable the UR_CTS/SCK pin.</p> <p>0: UR_CTS/SCK pin disabled 1: UR_CTS/SCK pin enabled</p>

USARTn FIFO Status Register – FSRn, n = 0 or 1

This register is the USARTn FIFO status register

Offset: 0x034

Reset value: 0x0000_0000



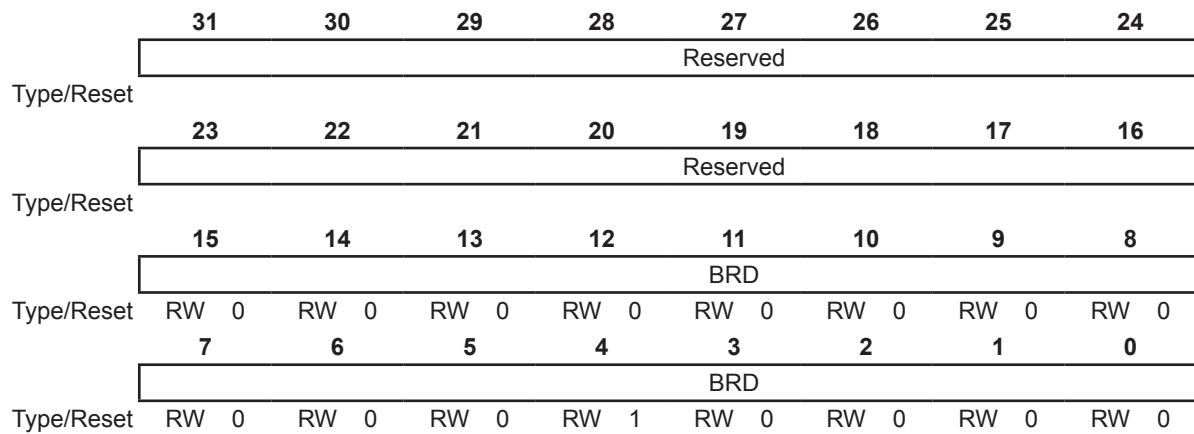
Bits	Field	Descriptions
[12:8]	RXFS	<p>RX FIFO Status</p> <p>The RXFS field shows the current number of data contained in the RX FIFO.</p> <ul style="list-style-type: none"> 00000: Rx FIFO is empty. 00001: Rx FIFO contains 1 data ... 10000: Rx FIFO contains 16 data Others: Reserved
[4:0]	TXFS	<p>TX FIFO Status</p> <p>The TXFS field shows the current number of data contained in the TX FIFO.</p> <ul style="list-style-type: none"> 00000: TX FIFO is empty 00001: TX FIFO contains 1 data ... 10000: TX FIFO contains 16 data Others: Reserved

USARTn Divider Latch Register—DLRn, n = 0 or 1

The register is used to determine the USARTn clock divided ratio to generate the appropriate baud rate.

Offset: 0x038

Reset value: 0x0000_0010



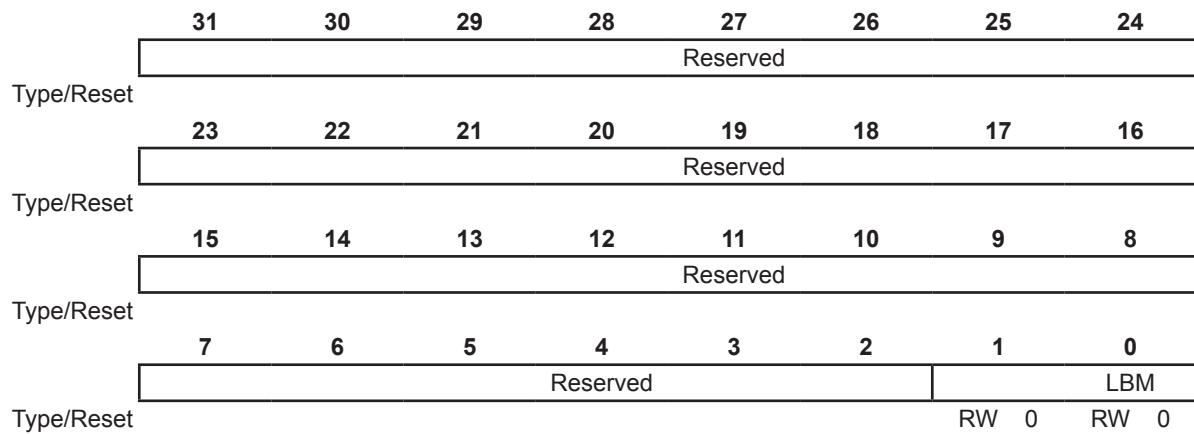
Bits	Field	Descriptions
[15:0]	BRD	<p>Baud Rate Divider</p> <p>The 16 bits define the USART clock divider ratio.</p> <p>Baud Rate = CK_USART / BRD</p> <p>Where the CK_USART clock is the system clock connected to the USART module.</p> <p>The BRD field can be set from 16 to 65535.</p>

USARTn Debug/Test Register – DEGTSTRn, n = 0 or 1

This register controls the USARTn debug mode.

Offset: 0x040

Reset value: 0x0000_0000



Bits	Field	Descriptions
[1:0]	LBM	Loopback Test Mode Select 00: Normal Operation 01: Reserved 10: Automatic Echo Mode 11: Loopback Mode

22 Universal Asynchronous Receiver Transmitter (UART)

Introduction

The Universal Asynchronous Receiver Transceiver, UART, provides a flexible full duplex data exchange with asynchronous transfer. The UART is used to translate data between parallel and serial interfaces, and is also commonly used for RS232 standard communication. The UART peripheral function supports a variety of interrupts.

The UART peripheral supports four-type interrupts as follows:

- Line Status Interrupt
- Transmitter FIFO Empty Interrupt
- Receiver Threshold Level Reaching Interrupt
- Time Out Interrupt

The UART module includes a 16-byte transmitter FIFO, TX_FIFO, and a 16-byte receiver FIFO, RX_FIFO.

Software can detect a UART error status by reading Line Status Register, LSR. The status includes the type and the condition of the transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

The UART includes a programmable baud rate generator which is capable of dividing the CK_AHB to produce a clock for the UART transmitter and receiver.

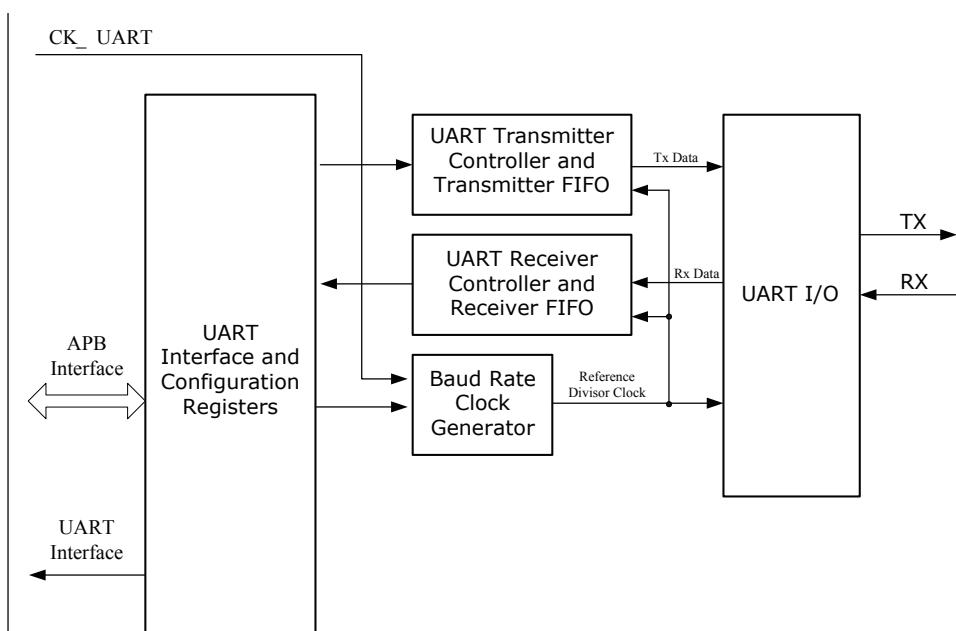


Figure 155. UART Block Diagram

Features

- Asynchronous serial communication mode is supported
- Full Duplex Communication Capability
- Fully programmable serial communication functions including:
 - Word length: 7, 8, or 9-bit character
 - Parity: Even, odd, or no-parity bit generation and detection
 - Stop bit: 1 or 2 stop bit generation
 - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun, and frame error
- FIFO:
 - Receive FIFO: 16×9 bits (max 9 data bits)
 - Transmit FIFO: 16×9 bits (max 9 data bits)

Functional Descriptions

Serial Data Format

The UART module performs a parallel-to-serial conversion on data that is read from the Transmitter FIFO and then sends the data with the following format: start bit, 7 ~ 9 LSB first data bits, optional parity bit and finally 1 ~ 2 stop bits. The start bit has the opposite polarity of the data line idle state. The stop bit is the same as the data line idle state and provides a delay before the next start situation. The start and stop bits are both used for data synchronization during the asynchronous data transmission.

The UART module also performs a serial-to-parallel conversion on the data that is read from the Receiver FIFO. It will first check the Parity bit and will then look for a Stop bit. If the Stop bit is not found, the UART module will consider the entire word transmission to have failed and respond with a Framing Error.

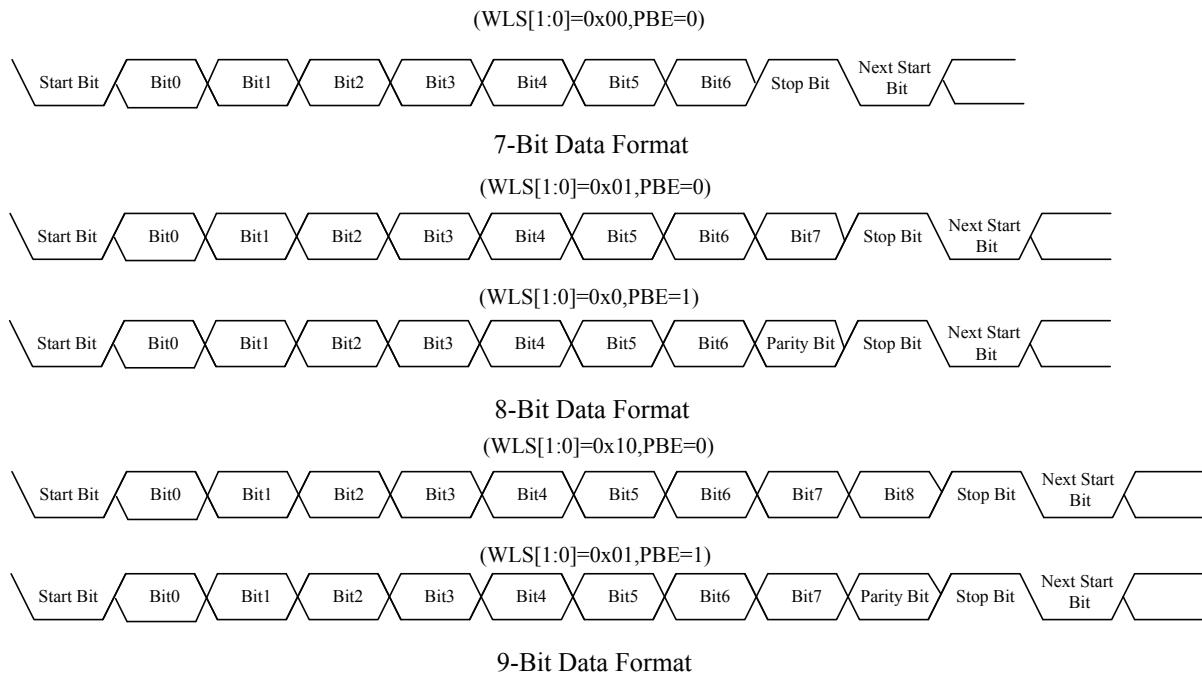


Figure 156. UART Serial Data Format

Baud Rate Generation

The baud rate for the UART receiver and transmitter are both set with the same values. The baud-rate divisor, BRD, has the following relationship with the UART clock which is known as CK_UART.

$$\text{Baud Rate Clock} = \text{CK_UART} / \text{BRD}$$

Where CK_UART clock is the system clock connected to the UART module while the BRD range is from 16 to 65535.

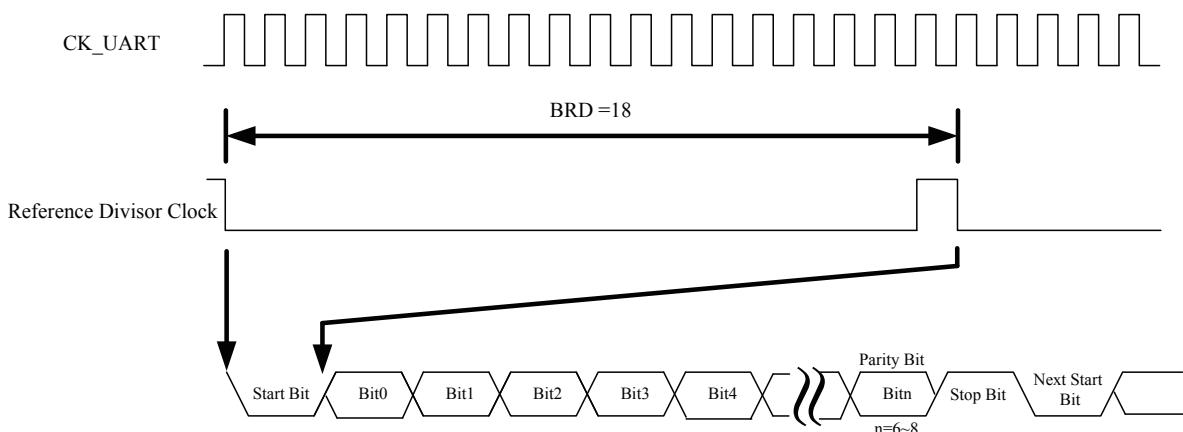


Figure 157. UART Clock CK_UART and Data Frame Timing

Table 55. Baud Rate Error calculation – CK_UART = 72 MHz

Baud rate		CK_UART = 72 MHz			
No	Kbps	Actual	BRD/16	BRD	Error rate
1	2.4	2.4	1875	30000	0%
2	9.6	9.6	468.75	7500	0%
3	19.2	19.2	234.375	3750	0%
4	57.6	57.6	78.125	1250	0%
5	115.2	115.2	39.0625	625	0%
6	230.4	230.769	19.5	312	0.16%
7	460.8	461.538	9.75	156	0.16%
8	921.6	923.076	4.875	78	0.16%
9	2250	2250	2	32	0%
10	4500	4500	1	16	0%

Interrupts and Status

The UART module can generate an interrupt when the following event occurs:

- Receiver Line Status Interrupt (Irpt_RLSI): Occurrence of UART overrun error, parity error, framing error, or break events.
- Receiver FIFO Threshold Level Interrupt (Irpt_RFTLI): When the FIFO received data amount has reached the specified threshold level.
- Receiver FIFO Time-out Interrupt (Irpt_RTOI): When the UART receiver FIFO does not receive a new data package during the specified time-out interval.
- Transmitter FIFO Threshold Level Interrupt (Irpt_TFTLI): When the data to be transmitted in the USART transmitter FIFO is less than the specified threshold level.
- MODEM Status Interrupt (Irpt_MODSI): When the DCD, RI, DSR, or CTS bits states in the MODSR register have changed.

Register Map

The following table shows the UART registers and reset values.

Table 56. UART Register Map

Register	Offset	Description	Reset Value
UART0 Base Address = 0x4000_1000			
UART1 Base Address = 0x4004_1000			
RBRn	0x000	UARTn Receiver Buffer Register	0x0000_0000
TBRn	0x000	UARTn Transmitter Buffer Register	0x0000_0000
IERN	0x004	UARTn Interrupt Enable Register	0x0000_0000
IIRn	0x008	UARTn Interrupt Identification Register	0x0000_0001
FCRn	0x00C	UARTn FIFO Control Register	0x0000_0001
LCRn	0x010	UARTn Line Control Register	0x0000_0000
LSRn	0x018	UARTn Line Status Register	0x0000_0060
TPRn	0x020	UARTn Timing Parameter Register	0x0000_0000
MDRn	0x024	UARTn Mode Register	0x0000_0000
FSRn	0x034	UARTn FIFO Status Register	0x0000_0000
DLRn	0x038	UARTn Divider Latch Register	0x0000_0010
DEGTSTRn	0x040	UARTn Debug/Test Register	0x0000_0000

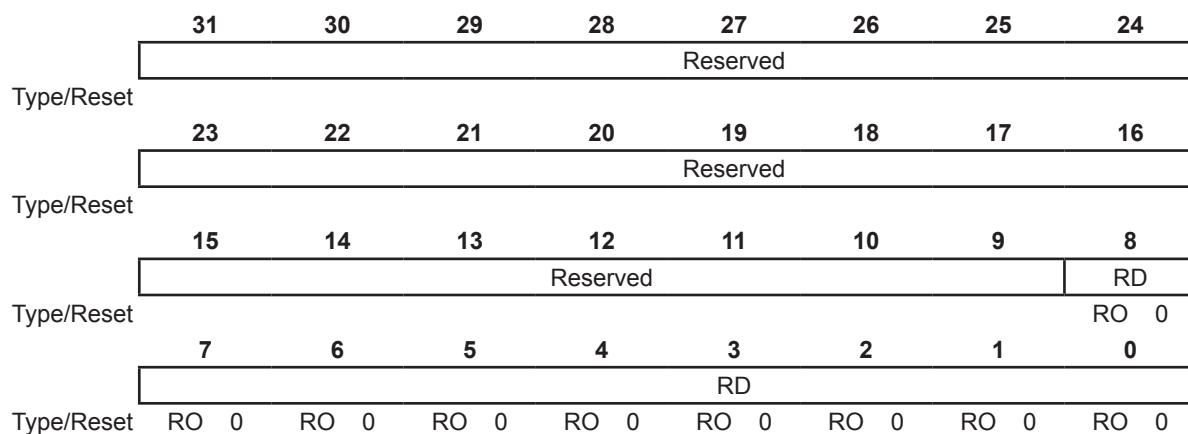
Register Descriptions

UARTn Receiver Buffer Register – RBRn, n = 0 or 1

The register is used to store the UARTn received data.

Offset: 0x000

Reset value: 0x0000_0000



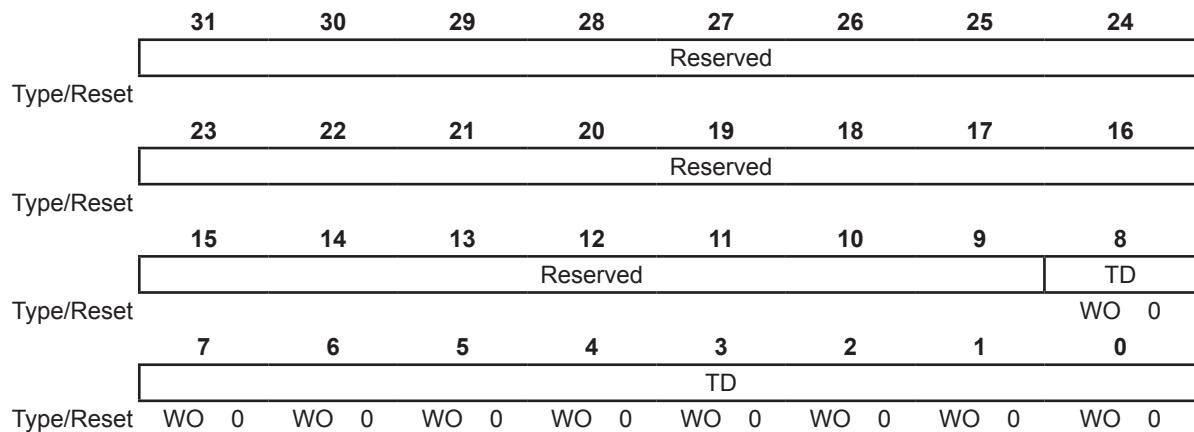
Bits	Field	Descriptions
[8:0]	RD	Reading the data via this receiver buffer register will return the data from the receiver FIFO. The receiver FIFO has a capacity of up to 16×9 bits. By reading this register, the USART will return a 7, 8 and 9-bit received data. The RD field bit 8 is valid for 9-bit mode only and is fixed at 0 for the 8-bit mode. For the 7-bits mode, the receiver buffer register RD[6:0] contain the available bits.

UARTn Transmitter Buffer Register – TBRn, n = 0 or 1

The register is used to specify the UARTn transmitted data.

Offset: 0x000

Reset value: 0x0000_0000



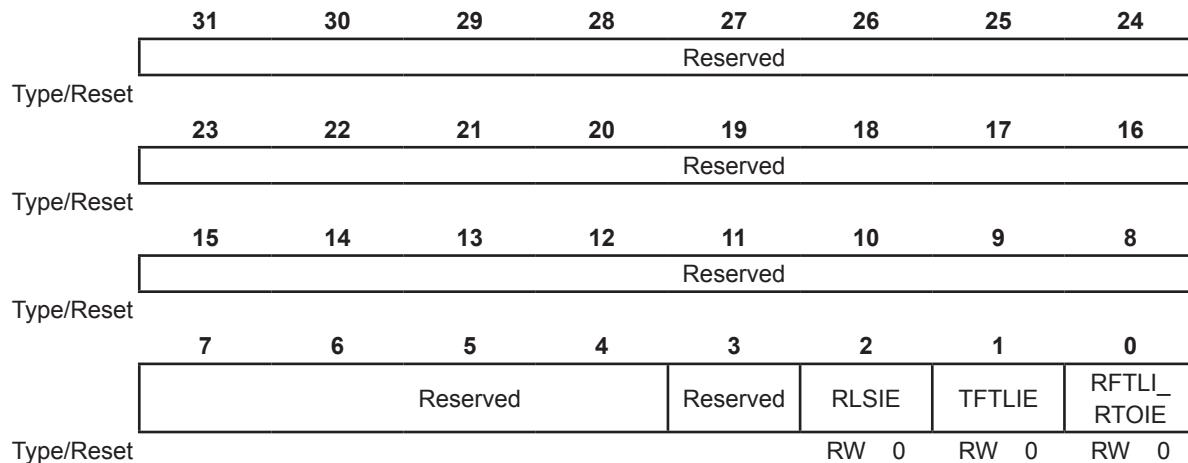
Bits	Field	Descriptions
[8:0]	TD	<p>Writing data to this transmitter buffer register will load data into the transmitter FIFO. The transmitter FIFO has a capacity of up to 16×9 bits.</p> <p>By writing to this register, the USART will send out 7,8 or 9-bit transmitted data. The TD field bit 8 is valid for the 9-bit mode only and will be ignored for the 8-bit mode. For the 7-bit mode, the transmitter buffer register TD [6:0] contains the available bits.</p>

UARTn Interrupt Enable Register – IERn, n = 0 or 1

This register is used to enable or disable the related UARTn interrupt function. The UARTn module generates interrupts to the controller when the corresponding events occur and the corresponding interrupt enable bits are set.

Offset: 0x004

Reset value: 0x0000_0000



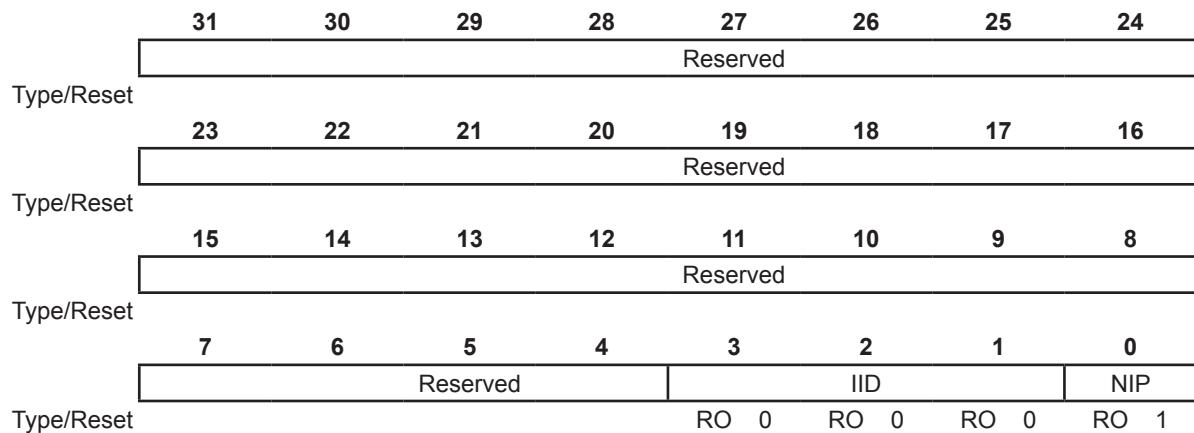
Bits	Field	Descriptions
[2]	RLSIE	Receive Line Status Interrupt Enable (Irpt_RLSI) 0: Mask Irpt_RLSI 1: Enable Irpt_RLSI
[1]	TFTLIE	Transmitter FIFO Threshold Level Interrupt (Irpt_TFTLI) Enable 0: Mask Irpt_TFTLI 1: Enable Irpt_TFTLI
[0]	RFTLI_RTOIE	Receiver FIFO Threshold Level Interrupt Enable (Irpt_RFTLI) or receiver FIFO Time-Out Interrupt Enable (Irpt_RTOI) 0: Mask Irpt_RFTLI and Irpt_RTOI 1: Enable Irpt_RFTLI or Irpt_RTOI

UARTn Interrupt Identification Register – IIRn, n = 0 or 1

This register is used to identify the interrupt source including the FIFO threshold and UARTn Receiver/Transmitter status.

Offset: 0x008

Reset value: 0x0000_0001



Bits	Field	Descriptions
[3:1]	IID	Interrupt Identification The detailed interrupt descriptions are shown in the accompanying table. The IID and NIP bits indicate the current UART interrupt request.
[0]	NIP	No Interrupt Pending 1; No pending URAT interrupt. 0: Pending UART interrupts.

Table 57. UART Interrupt control function

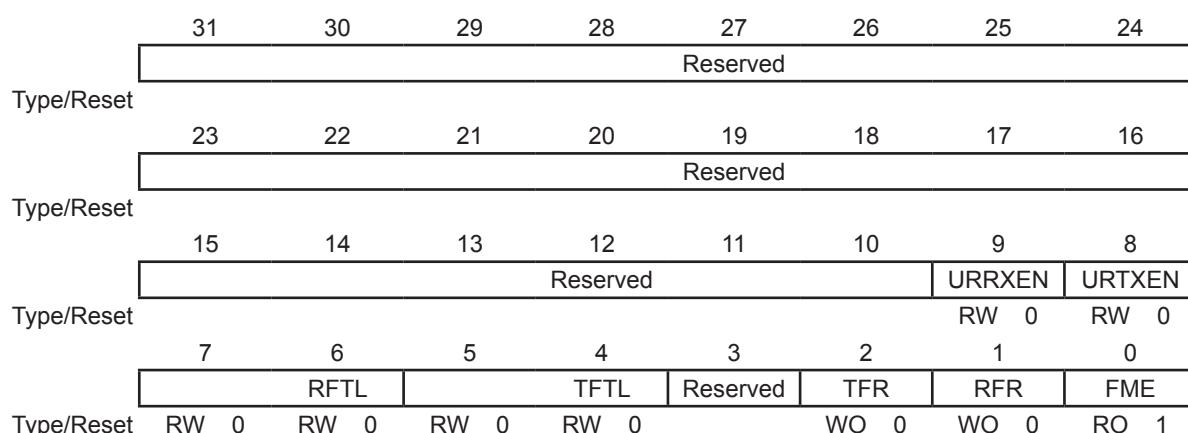
IIR[3:1] & NIP[0]	Priority	Interrupt Type	Interrupt Source	Interrupt Reset control
xxx1	NA	None	None	NA
0110	Highest	Receiver Line Status Interrupt (Irpt_RLSI)	UART occurs overrun error, parity error, framing error, or break events. [note] In RS485 mode, it can indicate the address detection.	Reading the LSR register.
0100	Second	Receiver FIFO Threshold Level Interrupt (Irpt_RFTLI)	Receiver FIFO threshold level is reached	Read the RBR register to decrease the receiver FIFO level to less than the specified threshold.
1100	Second	Receiver FIFO Time-out Interrupt (Irpt_RTOI)	Receiver FIFO is not empty and no activities have occurred in the receiver FIFO during the RTOIC time-out duration	Reading the RBR register
0010	Third	Transmitter FIFO Threshold Level Interrupt (Irpt_TFTLI)	Transmitter FIFO level is less than the transmitter FIFO threshold level which is set by the TFTL field in the FIFO Control Register named FCR.	Writing data into the TBR register.

UARTn FIFO Control Register – FCRn, n = 0 or 1

This register specifies the UARTn FIFO control and configurations including threshold level and reset function.

Offset: 0x00C

Reset value: 0x0000_0001



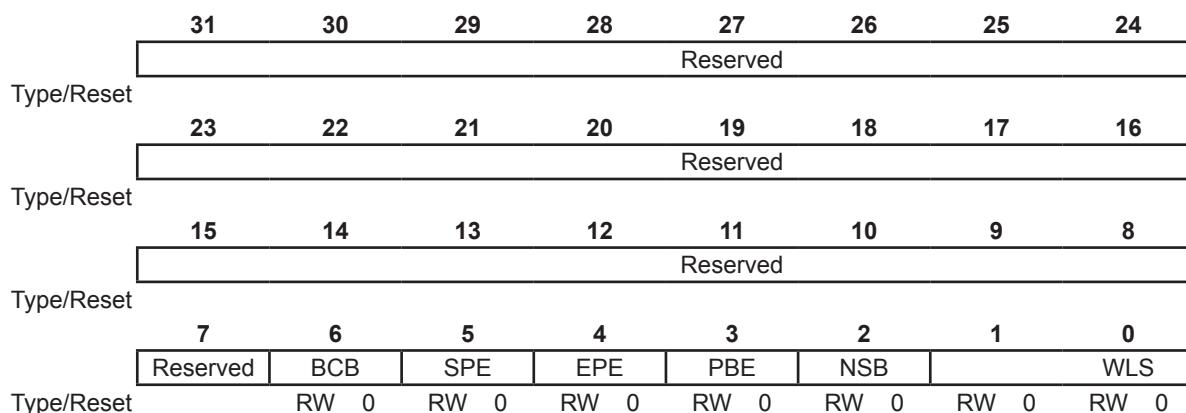
Bits	Field	Descriptions
[9]	URRXEN	UART RX Enable 0: disable 1: enable
[8]	URTXEN	UART TX Enable 0: disable 1: enable
[7:6]	RFTL	RX FIFO Threshold Level Setting The RFTL field defines the RX FIFO trigger level. 00: 1 byte 01: 4bytes 10: 8 bytes 11: 14bytes
[5:4]	TFTL	TX FIFO Threshold Level Setting The TFTL field determines the TX FIFO trigger level. 00: 0 byte 01: 2bytes 10: 4bytes 11: 8 bytes
[2]	TFR	TX FIFO Reset Setting this bit will generate a reset pulse to reset TX FIFO which will empty the TX FIFO. i.e., the TX pointer will be reset to 0, after a reset signal. This bit returns to 0 automatically after the reset pulse is generated.
[1]	RFR	RX FIFO Reset Setting this bit will generate a reset pulse to reset the RX FIFO which will empty the RX FIFO. i.e., the RX pointer will be reset to 0, after a reset signal. This bit returns to 0 automatically after the reset pulse is generated.
[0]	FME	FIFO Mode Enable Because the UART module is always operated in the FIFO mode, writing to this bit will have no effect.

UARTn Line Control Register – LCRn, n = 0 or 1

The line control register specifies the serial parameters such as data length, parity, and stop bit for the UARTn module.

Offset: 0x010

Reset value: 0x0000_0000



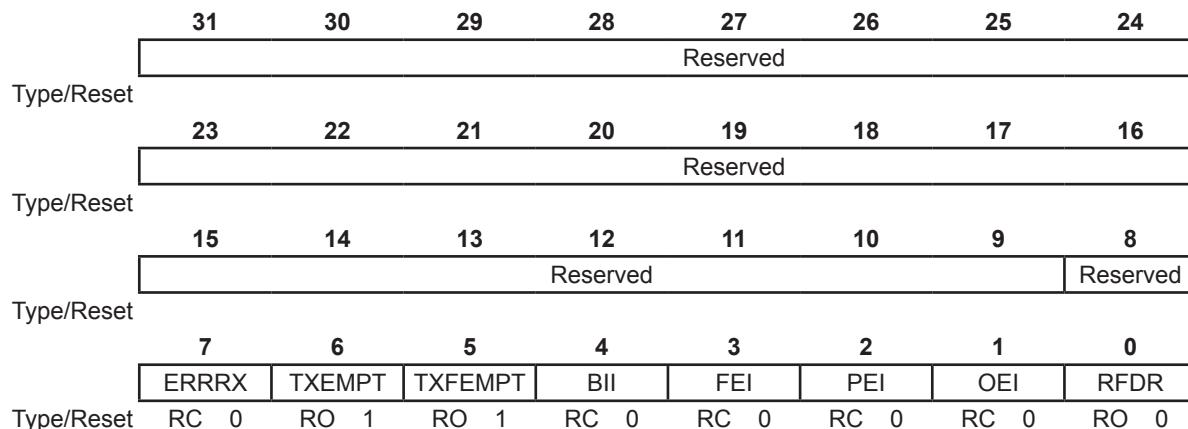
Bits	Field	Descriptions
[6]	BCB	Break Control Bit When this bit is set 1, the serial data output on the UR_TX pin will be forced to the Spacing State (logic 0). This bit acts only on UR_TX output pin and has no effect on the transmitter logic.
[5]	SPE	Stick Parity Enable 0: Disable stick parity 1: Stick Parity bit is transmitted This bit is only available when the PBE bit is set to 1. If both the PBE and SPE bits are set to 1 and the EPE bit is cleared to 0, the transmitted parity bit will be set to 1. However, when the PBE and SPE bits are set to 1 and also the EPE bit is set to 1, the transmitted parity bit will be cleared to 0.
[4]	EPE	Even Parity Enable 0: Odd number of logic 1's are transmitted or checked in the data word and parity bits. 1: Even number of logic 1's are transmitted or checked in the data word and parity bits. This bit is only available when PBE is set to 1.
[3]	PBE	Parity Bit Enable 0: Parity bit is not generated (transmitted data) or checked (receive data) during transfer. 1: Parity bit is generated or checked during transfer. Note: When the WLS field is set to "10" to select the 9-bit data format, writing to the PBE bit has no effect.
[2]	NSB	Number of "STOP bit" 0: One "STOP bit" is generated in the transmitted data 1: Two "STOP bit" is generated when 8- and 9-bit word length is selected.
[1:0]	WLS	Word Length Select 00: 7 bits 01: 8 bits 10: 9 bits 11: Reserved

UARTn Line Status Register – LSRn, n = 0 or 1

This register contains the corresponding UARTn status.

Offset: 0x018

Reset value: 0x0000_0060



Bits	Field	Descriptions
[7]	ERRRX	RS485 Address Detection Flag 0: Address is not detected 1: Address is detected This bit is set to 1 when the receiver detects the address and is cleared to 0 when the LSR register is read. Note: This bit is only used In the RS485 mode by setting the MDR field to "b10".
[6]	TXEMPT	RX FIFO Error 0: RX FIFO works normally 1: There is at least one parity error (PE), framing error (FE), or break indication (BI) in the receiver FIFO. The ERRRX bit is cleared when the CPU reads the LSR register and if there are no subsequent errors in the RX FIFO
[5]	TXFEMPT	Transmitter Empty 0: Either Transmitter FIFO (TX FIFO) or Transmitter Shift Register (TSR) is not empty. 1: Both the TX FIFO and TSR register are empty.

Bits	Field	Descriptions
[4]	BII	<p>Transmitter FIFO Empty</p> <p>0: TX FIFO is not empty. 1: TX FIFO is empty.</p> <p>The TXFEMPT bit is set when the last data package in the TX FIFO is transferred to the Transmitter Shift Register (TSR). This bit is reset when the TBR (or TX FIFO) is loaded with new data. This bit also causes the USART to issue an interrupt (Irpt_TFTLI) to the CPU when the TFTLIE bit in the IER register is set to 1 to enable the relevant interrupt and when the TFTL field in the FCR register is set to the value 0.</p>
[3]	FEI	<p>Break Interrupt Indicator</p> <p>This bit is set to 1 whenever the received data input is held in the "spacing state" (logic 0) for longer than a full word transmission time, which is the total time of "start bit" + data bits + "parity" + "stop bits" duration, and is reset whenever the CPU reads the contents of this LSR register.</p>
[2]	PEI	<p>Framing Error Indicator</p> <p>This bit is set 1 whenever the received character does not have a valid "stop bit", which means, the stop bit following the last data bit or parity bit is detected as a logic 0, and is reset whenever the CPU reads the contents of this LSR register.</p>
[1]	OEI	<p>Parity Error Indicator</p> <p>This bit is set to 1 whenever the received character does not have a valid "parity bit" and is reset whenever the CPU reads the contents of this LSR register.</p>
[0]	RFDR	<p>Overrun Error Indicator</p> <p>An overrun error will occur only after the RX FIFO is full and when the next character has been completely received in the RX shift register. The character in the shift register is overwritten, when an overrun event occurs, but it is not transferred to the RX FIFO. The OEI bit is used to indicate to the CPU as soon as it happens and is reset whenever the CPU reads the contents of this LSR register.</p>

UARTn Timing Parameter Register – TPRn, n = 0 or 1

This register contains the UARTn timing parameters including the transmitter time guard parameters and the receiver FIFO time-out value together with the RX FIFO time-out interrupt enable control.

Offset: 0x020

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24	
Type/Reset	Reserved								
	23	22	21	20	19	18	17	16	
Type/Reset	Reserved								
	15	14	13	12	11	10	9	8	
Type/Reset	RW	0	RW	0	RW	0	RW	0	
	7	6	5	4	3	2	1	0	
Type/Reset	RTOIE	RTOIC							
	RW	0	RW	0	RW	0	RW	0	

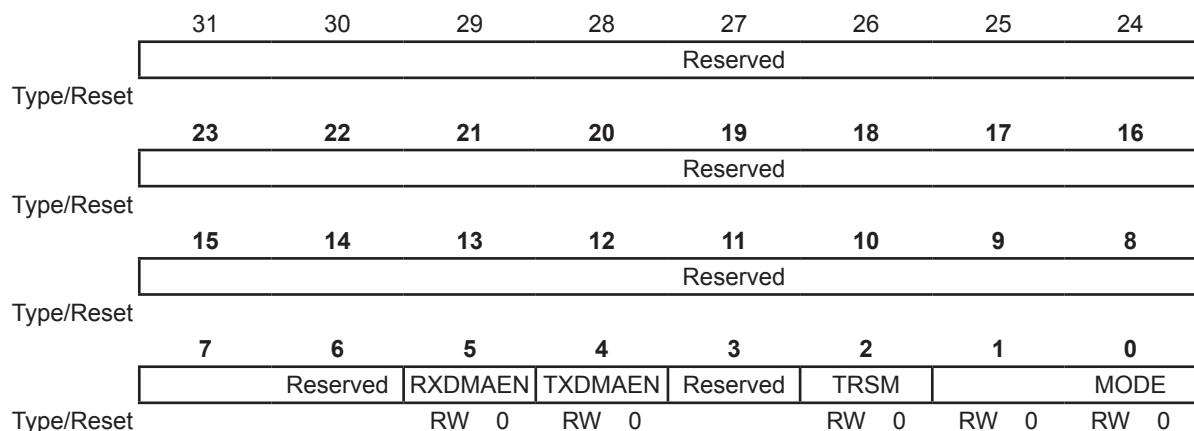
Bits	Field	Descriptions
[15:8]	TG	Transmitter Time Guard The transmitter time guard counter is driven by the baud rate clock. When the TX FIFO transmits data, the counter is reset and then starts to count. Only when the counter content is equal to the TG value, are further word transmission transactions allowed.
[7]	RTOIE	Receiver FIFO Time Out Interrupt Enable The receiver FIFO time-out interrupt is enabled only when the RFTLI_RTOIE bit in the IER register is set to 1.
[6:0]	RTOIC	Receiver FIFO Time-Out Interrupt Compare value The RX FIFO time-out counter, TOUT_CNT, is driven by the baud rate clock. When the RX FIFO receives new data, the counter is reset and then starts to count. Once the time-out counter content is equal to the time-out interrupt compare RTOIC value, a receiver FIFO time-out interrupt, Irpt_RTOI, is generated if the RFTLI_RTOIE bit in the IER register is set to 1. New received data or the empty RX FIFO after being read will clear the RX FIFO time-out counter.

UARTn Mode Register – MDRn, n = 0 or 1

This register specifies the UARTn mode and the data transfer mode selections.

Offset: 0x024

Reset value: 0x0000_0000



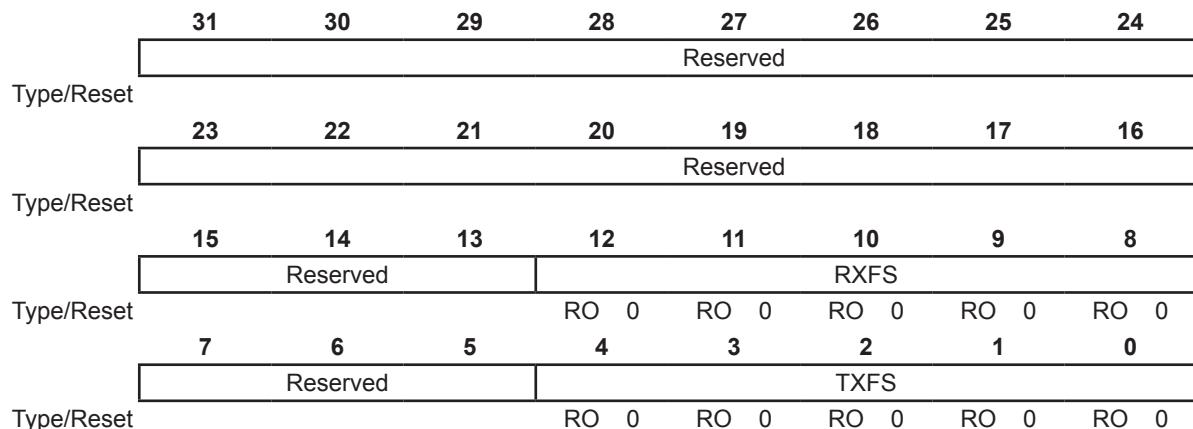
Bits	Field	Descriptions
[5]	RXDMAEN	UART RX DMA Enable 0: Disabled 1: Enabled
[4]	TXDMAEN	UART TX DMA Enable 0: Disabled 1: Enabled
[2]	TRSM	Transfer Mode Selection This bit is used to select the data transfer protocol. 0: LSB first 1: MSB first
[1:0]	MODE	UART Mode Selection. 00: Normal operation 01: IrDA 10: RS485 11: Synchronous

UARTn FIFO Status Register – FSRn, n = 0 or 1

This register is the UART FIFO status register

Offset: 0x034

Reset value: 0x0000_0000



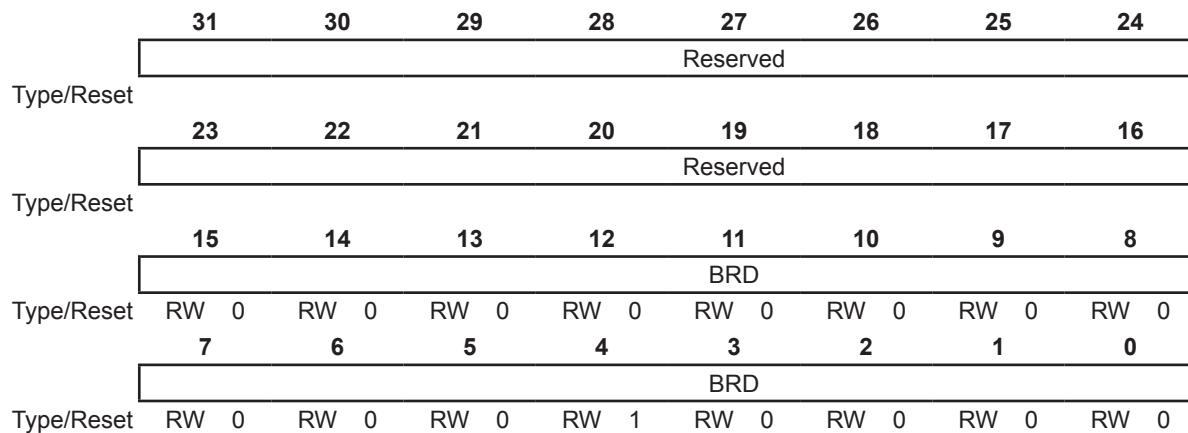
Bits	Field	Descriptions
[12:8]	RXFS	<p>RX FIFO Status</p> <p>The RXFS field shows the current number of data contained in the RX FIFO.</p> <ul style="list-style-type: none"> 00000: Rx FIFO is empty. 00001: Rx FIFO contains 1 data ... 10000: Rx FIFO contains 16 data Others: Reserved
[4:0]	TXFS	<p>TX FIFO Status</p> <p>The TXFS field shows the current number of data contained in the TX FIFO.</p> <ul style="list-style-type: none"> 00000: TX FIFO is empty 00001: TX FIFO contains 1 data ... 10000: TX FIFO contains 16 data Others: Reserved

UARTn Divider Latch Register – DLRn, n = 0 or 1

The register is used to determine the UARTn clock divided ratio to generate the appropriate baud rate.

Offset: 0x038

Reset value: 0x0000_0010



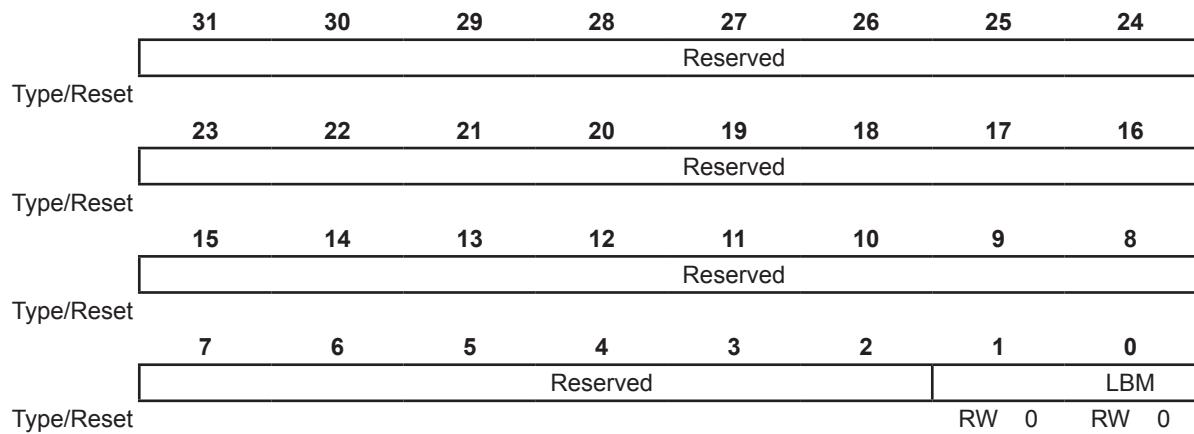
Bits	Field	Descriptions
[15:0]	BRD	Baud Rate Divider The 16 bits define the UART clock divider ratio. Baud Rate = CK_UART / BRD Where the CK_UART clock is the system clock connected to the UART module. The BRD field can be set from 16 to 65535.

UARTn Debug/Test Register – DEGTSTRn, n = 0 or 1

This register controls the UARTn debug mode.

Offset: 0x040

Reset value: 0x0000_0000



Bits	Field	Descriptions
[1:0]	LBM	Loopback Test Mode Select 00: Normal Operation 01: Reserved 10: Automatic Echo Mode 11: Loopback Mode

23 Smart Card Interface (SCI)

Introduction

The Smart Card Interface, SCI, is compatible with the ISO 7816-3 standard. This interface includes functions for card Insertion/Removal detection, SCI data transfer control logic and data buffers, internal Timer Counters and corresponding control logic circuits to perform the required Smart Card operations. The Smart Card interface acts as a Smart Card Reader to facilitate communication with the external Smart Card. The overall functions of the Smart Card interface are controlled by a series of registers including control and status registers together with several corresponding interrupts which are generated to get the attention of the microcontroller for SCI transfer status.

As the complexity of ISO7816-3 standard data protocol does not permit comprehensive specifications to be provided in this datasheet, the reader should therefore consult other external information for a detailed understanding of this standard.

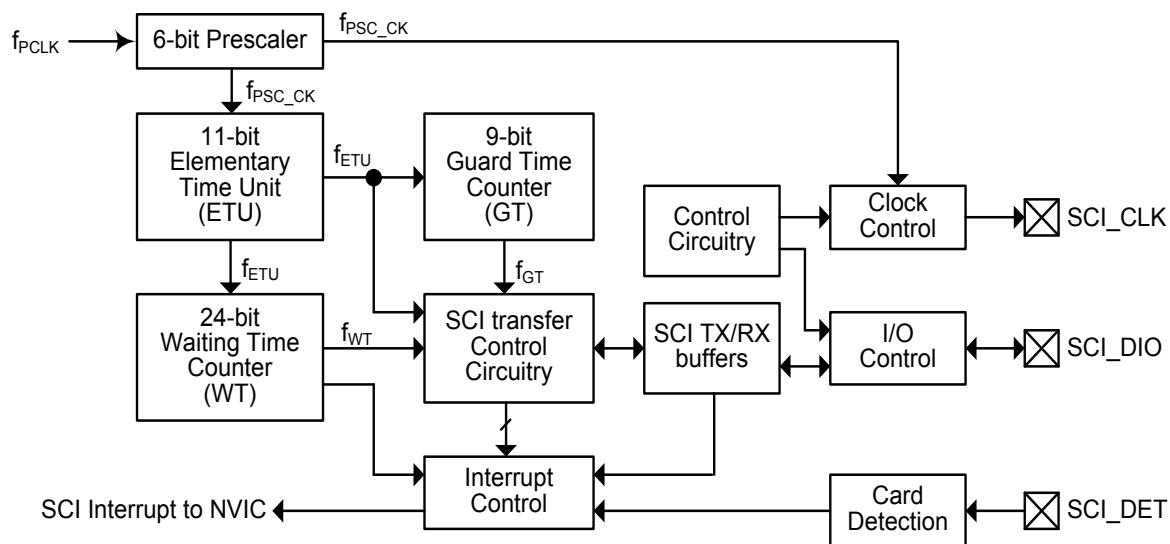


Figure 158. SCI Block Diagram

Features

- Supports ISO 7816-3 standard
- Character Transfer Mode
- 1 transmit buffer and 1 receive buffer
- 11-bit ETU (elementary time unit) counter
- 9-bit guard time counter
- 24-bit general purpose waiting time counter
- Parity generation and checking
- Automatic character repetition on parity error detection in transmission and reception modes
- Supports PDMA access at a transmission or reception completion

Functional Descriptions

To communicate with an external Smart Card, the integrated Smart Card Interface has a series of external pins known as SCI_CLK, SCI_DIO and SCI_DET. The SCI_CLK pin is the clock output signal used to communicate with the external Smart Card together with the serial data pin named SCI_DIO. The operation of the SCI_CLK and SCI_DIO pins can be selected to be the SCI data Transfer Mode which is driven automatically by the SCI control circuits or to be the Manual mode which is controlled by configuring the internal CLK and DIO register bits respectively by the application program. The SCI_DET pin is the external card detection input pin. Insertion or removal of the external Smart Card can be automatically detected and generate an interrupt signal which is sent to the microcontroller if the corresponding interrupt function is enabled.

For proper data transfer, some timing related procedures must be executed before the Smart Card Interface can begin to communicate with the external card. There are three counters named Elementary Time Unit, ETU, Guard Time Counter, GT, and Waiting Time Counter, WT, which are used for the timing related functions in Smart Card Interface data transfer operations.

Elementary Time Unit Counter

The Elementary Time Unit, ETU, is an 11-bit up-counting counter which generates a clock denoted as f_{ETU} to be used as the operating frequency source for the SCI data transmission and reception. The clock source of the ETU comes from the Smart Card clock, named f_{PSC_CK} , which is derived from the 6-bit prescaler. The data transfer of the SCI is a character frame based protocol, which basically consists of a Start bit, 8-bits of data and a Parity bit. The time period, t_{ETU} ($1/f_{ETU}$), generated by the ETU, is the time unit for a character bit. There is a register related to the Elementary Time Unit known as the ETUR register which stores the expected contents of the ETU. Each time the ETUR register is written, the ETU circuitry will reload the new written value and restart counting. The elementary time unit t_{ETU} is obtained from the following formula which defines the bit rate in the ISO 7816-3 standard specification.

$$t_{etu} = t_{ETU} = \frac{F_i}{D_i} \times \frac{1}{f}$$

where:

- t_{etu} is the nominal duration of the data bit on the signal SCI_DIO provided to the card by the interface
- D_i is the bit-rate adjustment factor
- F_i is the clock rate conversion factor
- f is the frequency value of the clock signal SCI_CLK provided to the card by the interface
- D_i is an encoded decimal value based on a 4-bit field, named DI, as represented in the accompanying table.

Table 58. DI Field Based D_i Encoded Decimal Values

DI field	0001	0010	0011	0100	0101	0110	1000	1001
D_i (decimal)	1	2	4	8	16	32	12	20

F_i is an encoded decimal value based on a 4-bit field, named FI, as represented in the following table.

Table 59. FI Field Based F_i Encoded Decimal Values

FI field	0000	0001	0010	0011	0100	0101	0110	1001	1010	1011	1100	1101
F_i (decimal)	372	372	558	744	1116	1488	1860	512	768	1024	1536	2048

The values of FI and DI, as they appear in the preceding tables, will be obtained from the Answer-to-Reset packet sent from the external Smart Card to the Smart Card Interface the first time the external Smart Card is inserted. When the SCI receives the FI and DI information, the F_i and D_i values can be obtained by looking up the preceding two tables. After the F_i and D_i values are obtained, the value which should be written into the ETUR register can be calculated by F_i/D_i . The following table shows the possible ETU values obtained by the F_i/D_i ratio.

Table 60. Possible ETU Values Obtained with the F_i/D_i Ratio

$\frac{F_i}{D_i}$	372	558	774	1116	1488	1860	512	768	1024	1536	2048
1	372	558	744	1116	1488	1860	512	768	1024	1536	2048
2	186	279	372	558	744	930	256	384	512	768	1024
4	93	139.5	186	279	372	465	128	192	256	384	512
8	46.5	69.75	93	139.5	186	232.5	64	96	128	192	256
16	23.25	34.87	46.5	69.75	93	116.2	32	48	64	96	128
32	11.62	17.43	23.25	34.87	46.5	58.13	16	24	32	48	64
12	31	46.5	62	93	124	155	42.66	64	85.33	128	170.6
20	18.6	27.9	37.2	55.8	74.4	93	25.6	38.4	51.2	76.8	102.4

Compensation mode

As the value of the ETUR register is obtained by the above procedure, the calculation results of the value may not be an integer. If the calculation result is not an integer and is less than the integer n but greater than the integer (n-1), either the integer n or (n-1) should be written into the ETUR register depending upon whether the result is closer to integer n or (n-1). The integer n mentioned here is a decimal.

If the calculation result is close to the value of (n-0.5), the compensation mode should be enabled by setting the compensation enable control bit, COMP, in the ETUR register to 1 for successful data transfer. When the result is close to the value of (n-0.5) and the compensation mode is enabled, the value written into the ETUR register should be n. The ETU circuitry will then generate the time unit sequence with n clock cycles and next (n-1) clock cycles alternately and so on. This results in an average time unit of (n-0.5) clock cycles and allows a time granularity down to a half clock cycle. Note that the ETU will reload the ETUR register value and restart counting at the time when the Start bit appears in the SCI data Transfer Mode.

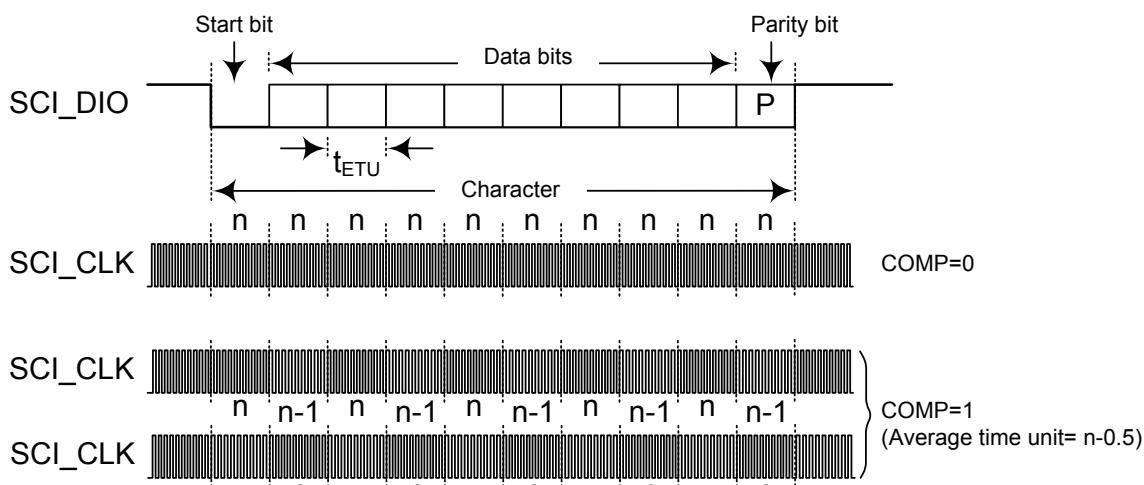


Figure 159. Character Frame and Compensation Mode

Guard Time Counter

The Guard Time Counter, GT, is a 9-bit up-counting counter which generates a minimum time duration known as a character frame, denoted as t_{GT} , between the leading edges of two consecutive characters in the SCI data transfer. The clock source of the guard time counter comes from the ETU, named f_{ETU} in the block diagram. There is a register related to the guard time counter known as the GTR register, which stores the expected value of the guard time counter. The guard time value will be reloaded at the end of the current guard time period. Note that the guard time between the last character received from the Smart Card and the next character transmitted by the SCI circuitry which should be properly managed by the application program. There is no guard time insertion when the first character is transmitted.

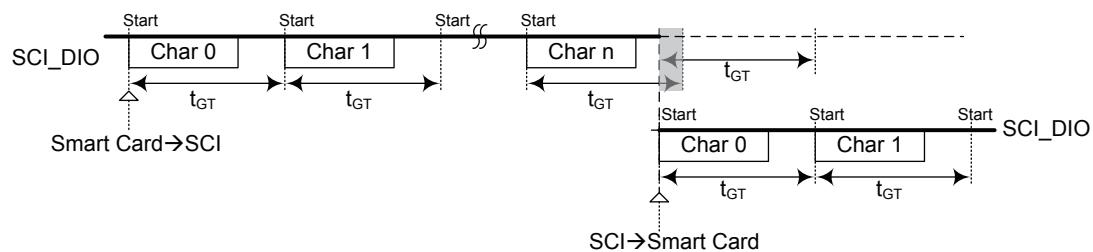


Figure 160. Guard Time Duration

Waiting Time Counter

The Waiting Time counter, WT, is a 24-bit down counting counter which generates a maximum time duration, denoted as t_{WT} , for data transfer. The clock source of the waiting time counter comes from the ETU and is named f_{ETU} .

There is a register for the waiting time counter known as the WTR register which stores the expected waiting time counter value. The waiting time counter can be used in both the SCI data Transfer Mode and manual mode and can reload the value for specific conditions. The function of the waiting time counter is controlled by the WTEN bit in the CR register. When the SCI is configured to be operated in the SCI data Transfer Mode and the waiting time counter is enabled by setting the WTEN bit to 1, the updated WTR register value will be loaded into the waiting time counter when the Start bit is detected. Note that the WTEN bit should not be set to 1 to enable the waiting time counter in the SCI data Transfer Mode until after the external Smart Card is inserted.

If the SCI is configured to operate in the manual mode, the waiting time counter can be used as a general purpose timer and this timer is enabled or disabled by setting or clearing the WTEN bit. The updated WTR register value will not be loaded into the waiting time counter if the waiting time counter is enabled. When the waiting time counter is disabled by setting the WTEN bit to 0 and an updated value is written into the WTR register, the new value will immediately be loaded into the waiting time counter and then the counter will start to count after the WTEN bit is again set to 1.

Software can change the Waiting Time value on-the-fly. For example, in T=1 mode, the value of the Block Waiting Time, t_{BWT} , should be written into the WTR register before the Start bit of the last transmitted character occurs. After the transmission of the last character is completed, software should write the Character Waiting Time value, t_{CWT} , into the WTR register.

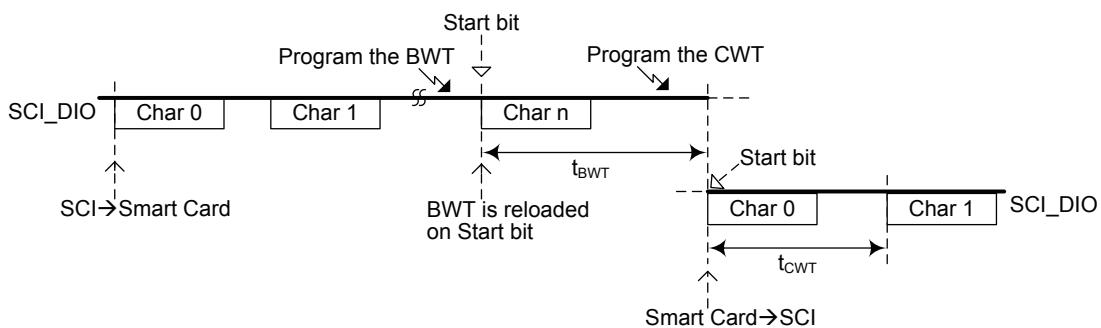


Figure 161. Character and Block Waiting Time Duration – CWT and BWT

Card Clock and Data Selection

The SCI communicates with an external Smart Card using a series of external pins. These are the serial data pin, SCI_DIO, output clock pin, SCI_CLK, and the Card Detection input pin, SCI_DET.

The SCI serial data pin, named SCI_DIO, can be controlled by the SCI hardware circuitry or the software control bits depending upon whether the SCI is operated in the SCI Transfer Mode or in the Manual Mode. The mode selection is determined by the SCIM bit in the CR register. The SCI_DIO pin status is controlled by the CDIO bit in the CCR register when the SCI is configured to operate in the Manual mode by clearing the SCIM bit in the CR register. In the Manual Mode the SCI_DIO pin status is a copy of the CDIO bit. However, when the SCI is configured to operate in the SCI Transfer Mode, the SCI_DIO pin status is determined by the SCI transfer circuitry.

The SCI clock output pin named SCI_CLK can be controlled by the 6-bit SCI prescaler or the software control bits depending upon the condition of the CLKSEL bit in the CCR register. The SCI_CLK pin status is controlled by the CCLK bit in the CCR register when the CLKSEL bit is cleared to 0. The SCI_CLK pin status is a copy of the CCLK bit. However, when the CLKSEL bit is set to 1, the SCI_CLK signal is sourced from the 6-bit prescaler output. The prescaler division ratio is determined by the PSC field in the PSCR register.

Card Detection

When an external Smart Card is inserted, the internal card detector can detect this insertion operation and generate a card insertion interrupt if the corresponding interrupt enable control bit, CARDIRE, in the IER register is set to 1. Similarly, if the card is removed, the internal card detector can also detect the removal and consequently generate a card removal interrupt when the corresponding interrupt function is enabled by setting the control bit, CARDIRE, in the IER register, to 1.

The card detector can support two kinds of card detect switch mechanisms. One is a normally open switch mechanism when the card is not present and the other is a normally closed switch mechanism. After noting which card detect switch mechanism type is used, the card switch selection should be configured by setting the selection bit, DETCNF, in the CR register to correctly detect the card presence. No matter what type of the card switch is selected, by configuring the DETCNF bit, the card Insertion/Removal flag, CPREF, in the SR register will be set to 1 when the card is actually present on the SCI_DET pin. Note that there are no hardware de-bounce circuits in the card detector. Any change of the SCI_DET pin level will cause the CPREF bit to change. The required de-bounce time should be handled by the application program.

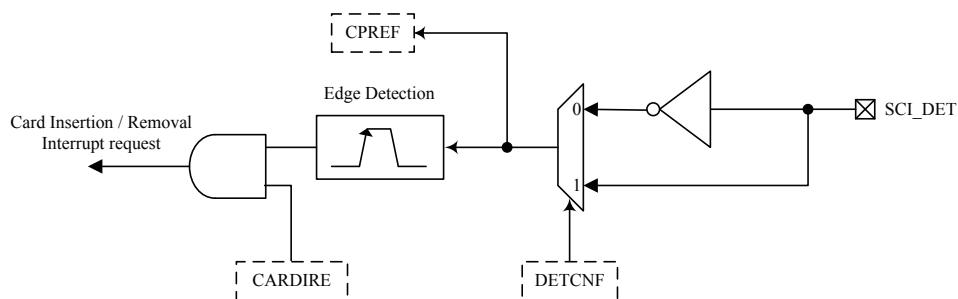


Figure 162. SCI Card Detection Diagram

SCI Data Transfer Mode

The SCI data transfer with the external Smart Card is implemented with two operating modes. One is the SCI mode while the other is the Manual Mode. The data Transfer Mode is selected by the SCI mode selection bit, SCIM, in the CR register. When the SCIM bit is set to 1, the SCI mode is enabled and data will automatically be transferred by the SCI transfer circuitry. Otherwise, data transfer operates in the Manual Mode if the SCIM bit is cleared to 0. The SCI transfer interface is a half-duplex interface and communicates with the external Smart Card via the SCI_CLK and SCI_DIO pins. After a reset condition the SCI transfer interface is in the reception mode but the SCI transfer operation is disabled. When the SCI mode is enabled, data transfer is driven by the SCI transfer circuitry automatically through the SCI_CLK and SCI_DIO pins.

There are two data registers related to data transmission and reception, TXB and RXB, which store the data to be transmitted and received respectively. If a character is written into the TXB register in the SCI Transfer Mode, the SCI transfer interface will automatically switch to the Transmission Mode from the reception mode after a reset. When the SCI transmission or reception has finished, the corresponding request flag, named TXCF or RXCF, in the SR register is set to 1. If the transmit buffer is empty, the transmit buffer empty flag, TXBEF, in the SR register will be set to 1.

Parity Check Function

The SCI transfer interface supports a parity generator and a parity check function. As the parity error occurs during a data transfer, the corresponding request flag, named PARF in the SR register, will be set to 1. Once the PARF bit is set to 1, the parity error pending flag, PARP, in the IPR register will also be set to 1 if the relevant interrupt control bit, PARE, in the IER register is enabled.

If the data transmitted by the SCI is received by the external Smart Card without a parity error, the SCI transmission request flag, TXCF, will be set to 1 and the SCI parity error request flag, PARF, will be cleared to 0. If the data transmitted by the external Smart Card is received by the SCI without a parity error, the SCI reception request flag, RXCF, will be set to 1 and the parity error flag, PARF, will be cleared to 0.

Repetition Function

There is a Character Repetition function supported by the SCI transfer circuitry when a parity error occurs. The Character Repetition function is enabled by setting the CREP bit in the CR register to 1. A repetition function will then be activated when a parity error occurs during a data transfer. The repetition time number can be selected to be 4 or 5 by configuring the RETRY bit in the CR register.

When the CREP bit is set to 1, the character repetition function will be activated. Taking a 4 time repetition as an example, when the CREP bit is set to 1 and the RETRY bit is set to 1, in the Transmission Mode, the SCI will repeatedly transmit the data a maximum of 4 times when an error signal occurs. However, if the SCI is informed that there is still an error signal during the 4 transmissions, the parity error flag PARF will be set to 1 after the same data has been transmitted 4 times but the TXCF flag will not be set. At this time the data in the transmit buffer will be loaded into the transmit shift register and the transmit buffer will be empty which will result in the TXBEF flag being set to 1.

Similarly, when the SCI operates in the reception mode, it will inform the external Smart Card that there is a parity error for a maximum of 4 times if the character repetition function is enabled. If the SCI informs the external Smart Card that there is still an error signal for the 4 receptions, the parity error flag, PARF, will be set to 1 together with the reception request flag, RXCF.

If the CREP bit is cleared to 0, the character repetition function will be disabled. When the SCI operates in the reception mode, both the PARF and RXCF bits will be set to 1 as data with a parity error has been received. If the SCI is informed that there is a parity error in the Transmission Mode, the PARF bit will be set to 1 but the TXCF bit will not be set.

Manual Data Transfer Mode

When the SCIM bit is cleared to 0, data will be transferred in the Manual Mode. In the Manual Mode, the data is controlled by the control bit, CDIO, in the CCR register. The CDIO bit value will be reflected immediately on the SCI_DIO pin in the Manual Mode. Note that in the Manual Mode the character repetition function can not be used as well as the related flags and all the data transfer is handled by the application program. The clock used to drive the external Smart Card that appears on the SCI_CLK pin can be derived from the internal clock source, which is the 6-bit prescaler output, f_{PSC_CK} , or from the control bit, CCLK, in the CCR register. The clock source is selected using the bit, CLKSEL, in the CCR register. When CLKSEL bit is set to 1, the clock used to drive the Smart Card will be sourced from the 6-bit prescaler output, f_{PSC_CK} . If the clock is to be managed manually, the CLKSEL bit should first be cleared to 0 and then the value of the CCLK bit will be present in the SCI_CLK pin.

Data Transfer Direction Convention

If the direction convention used by the Smart Card is the same as the convention used by the SCI, the SCI will generate a reception interrupt if the reception interrupt is enabled without a parity error flag. Otherwise, the SCI will generate a reception interrupt and the parity error flag will be asserted. By checking the parity error flag, the SCI can know if the data direction convention is correct or not.

Interrupt Generator

There are several conditions for the SCI to generate an SCI interrupt. When these conditions are met, an interrupt signal will be generated to obtain the attention of the microcontroller. These conditions are a Smart Card Insertion/Removal, a Waiting Time Counter Underflow, a Parity error, an end of a Character Transmission or Reception and an empty Transmit buffer. When a Smart Card interrupt is generated by any of these conditions, then if the SCI global interrupt and the corresponding SCI interrupt are together enabled, the program will jump to the corresponding interrupt vector where it can be serviced before returning to the main program.

For SCI interrupt events, there are corresponding pending flags which can be masked by the relevant interrupt enable control bit. When the related interrupt enable control is disabled, the corresponding interrupt pending flag will not be affected by the request flag and no interrupt will be generated. If the related interrupt enable control is enabled, the relevant interrupt pending flag will be affected by the request flag and then the interrupt will be generated. The pending flag register, named IPR, is read only and once the pending flag is read by the application program, it will be automatically cleared while the related request flag should be cleared by the application program manually.

For an SCI Interrupt to be serviced, in addition to the bits for the corresponding interrupt enable control in the SCI being set, the SCI global interrupt enable control bit in the NVIC must also be set. If this SCI global interrupt control bit is not set, then no SCI interrupt will be serviced.

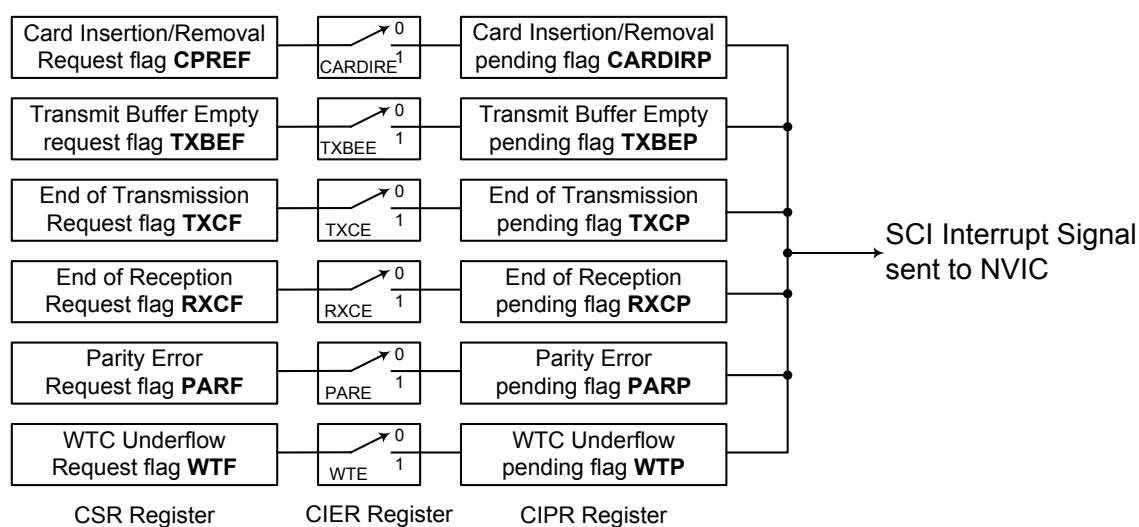


Figure 163. SCI Interrupt Structure

PDMA Interface

The PDMA interface is integrated in the SCI module. The PDMA function can be enabled by setting the TXDMA or RXDMA bit to 1 in the transmitter or receiver mode respectively. When the transmit buffer is empty which results in the transmit buffer empty flag, TXBEF, being asserted and the TXDMA bit is set to 1, the PDMA function will be activated to move data from a certain memory location into the SCI Transmit buffer. Similarly, when the SCI receives a character which results in the character received flag, RXCF, being asserted and the RXDMA bit is set to 1, the PDMA function will be activated to move data from the SCI Receive buffer to a specific memory location.

For a more detailed descriptions on the PDMA configurations, refer to the PDMA chapter.

Register Map

There are several registers associated with the Smart Card function. Some of these registers control the SCI overall function as well as the interrupts, while some of the registers contain the status bits which indicate the Smart Card data transfer situation and error conditions. Also there are two registers for the SCI transmission and reception respectively to store the data received from or to be transmitted to the external Smart Card. The following table shows the SCI register list and reset values.

Table 61. SCI Register Map

Register	Offset	Description	Reset Value
SCI Base Address = 0x4004_3000			
CR	0x000	SCI Control Register	0x0000_0000
SR	0x004	SCI Status Register	0x0000_0080
CCR	0x008	SCI Contact Control Register	0x0000_0008
ETUR	0x00C	SCI Elementary Time Unit Register	0x0000_0174
GTR	0x010	SCI Guard Time Register	0x0000_000C
WTR	0x014	SCI Waiting Time Register	0x0000_2580
IER	0x018	SCI Interrupt Enable Register	0x0000_0000
IPR	0x01C	SCI Interrupt Pending Register	0x0000_0000
TXB	0x020	SCI Transmit Buffer	0x0000_0000
RXB	0x024	SCI Receive Buffer	0x0000_0000
PSCR	0x028	SCI Prescaler Register	0x0000_0000

Register Descriptions

SCI Control Register – CR

This register contains the SCI control bits.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24	
	Reserved								
Type/Reset	23	22	21	20	19	18	17	16	
	Reserved								
Type/Reset	15	14	13	12	11	10	9	8	
	Reserved						RXDMA	TXDMA	
Type/Reset	7	6	5	4	3	2	1	0	
	Reserved	DETCNF	ENSCI	RETRY	SCIM	WTEN	CREP	CONV	
Type/Reset	RW	0	RW	0	RW	0	RW	0	

Bits	Field	Descriptions															
[9]	RXDMA	SCI reception DMA request enable 0: SCI reception DMA request is disabled 1: SCI reception DMA request is enabled															
[8]	TXDMA	SCI transmission DMA request enable control 0: SCI transmission DMA request is disabled 1: SCI transmission DMA request is enabled															
[6]	DETCNF	Card switch type selection 0: Switch is normally opened if no card is present 1: Switch is normally closed if no card is present															
		<table border="1"> <thead> <tr> <th>DETCNT</th> <th>SCI_DET pin</th> <th>STATUS</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1</td> <td>No card insert</td> </tr> <tr> <td>0</td> <td>0</td> <td>Card insert</td> </tr> <tr> <td>1</td> <td>1</td> <td>Card insert</td> </tr> <tr> <td>1</td> <td>0</td> <td>No card insert</td> </tr> </tbody> </table>	DETCNT	SCI_DET pin	STATUS	0	1	No card insert	0	0	Card insert	1	1	Card insert	1	0	No card insert
DETCNT	SCI_DET pin	STATUS															
0	1	No card insert															
0	0	Card insert															
1	1	Card insert															
1	0	No card insert															
		This bit is set and cleared by the application program to configure the card detector switch type.															
[5]	ENSCI	SCI finite state machine enable bit 0: SCI FSM is disabled and forced to its initial state 1: SCI FSM is enabled															
[4]	RETRY	Character transfer repetition time selection for a parity error condition 0: Data transfer 5 times when parity error occurs 1: Data transfer 4 times when parity error occurs															
		The bit is available only when the CREP bit is set to 1. When this bit is set to 1, the data will be transmitted or received 4 times once a parity error occurs. If the bit is cleared to 0, the data will be transferred 5 times if a parity error occurs.															

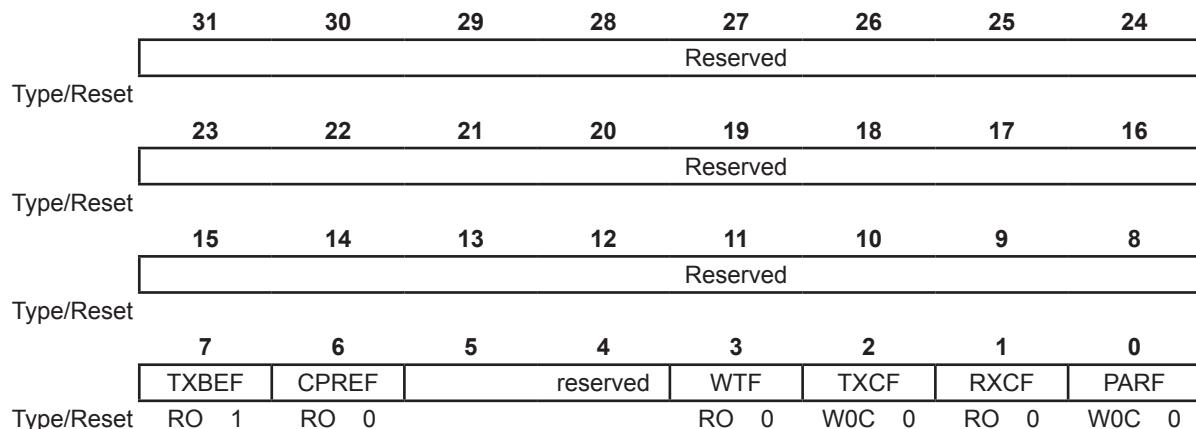
Bits	Field	Descriptions
[3]	SCIM	<p>SCI Mode Selection</p> <p>0: SCI data transfer in manual mode 1: SCI data transfer in SCI mode</p> <p>This bit is set and cleared by the application program to select the SCI data Transfer Mode. If it is cleared to 0, the SCI_DIO pin status is the same as the value of the CDIO bit in the CCR register. If it is set to 1, the SCI_DIO pin is driven by the internal SCI control circuitry. Before the data transfer type is switched from the Manual Mode to the SCI Mode, the CDIO bit must be set to 1 to avoid an SCI malfunction.</p>
[2]	WTEN	<p>Waiting Time Counter enable control</p> <p>0: Waiting Time Counter stops counting 1: Waiting Time Counter starts counting</p> <p>The WTEN bit is set and cleared by the application program. When the WTEN bit is cleared to 0, a write access to the WTR register will load the value into the waiting time counter. If it is set to 1, the waiting time counter is enabled and automatically reloaded with the value at each start bit occurrence.</p>
[1]	CREP	<p>Automatic character repetition enable control for a parity error condition</p> <p>0: No retry on parity error 1: Automatic retry on parity error</p> <p>The CREP bit is set and cleared by the application program. When the CREP bit is cleared to 0, both the RXCF and PARF flags will be set when a parity error occurs in the reception mode after the data is received. However, in the Transmission Mode, the PARF flag will be set but the TXCF flag will not be set when a parity error occurs. If the CREP bit is set to 1, a character transfer will automatically be activated 4 or 5 times depending upon the RETRY bit value. In the Transmission Mode the character will be re-transmitted if the transmitted data has a parity error. Here the parity error flag, PARF, will be set at the end of the 4th or 5th transmission without the TXCF bit being set. In the reception mode if the received data has a parity error, the SCI will inform the external Smart Card for 4 or 5 times and then the PARF and RXCF flags will both be set at the end of the 4th or 5th reception.</p>
[0]	CONV	<p>Data direction convention select</p> <p>0: LSB is transferred first; a data "1" is a logic high level on the SCI_DIO pin and the parity bit is added after the MSB. 1: MSB is transferred first; a data "1" is a logic low level on the SCI_DIO pin and the parity bit is added after the LSB.</p> <p>This bit is set and cleared by the application program to select if the data is transmitted LSB or MSB first. When the data direction convention is the same as the data direction specified by the external Smart Card, only the RXCF flag will be set to 1 without a parity error. Otherwise, both the RXCF and PARF flags will be set to 1 after the data is received.</p>

SCI Status Register – SR

This register contains the SCI status bits.

Offset: 0x004

Reset value: 0x0000_0080



Bits	Field	Descriptions
[7]	TXBEF	Transmit Buffer Empty Request Flag 0: Transmit buffer is not empty 1: Transmit buffer is empty This bit is used to indicate if the transmit buffer is empty and is set or cleared by hardware automatically.
[6]	CPREF	Card Presence Request Flag 0: No card is present 1: A card is present This bit is used to indicate if a card is present and is set or cleared by hardware automatically. The card presence detection function is enabled after the ENSCI bit is set.
[3]	WTF	Waiting Time Counter Underflow Request Flag 0: No Waiting Time Counter underflow 1: The Waiting Time Counter underflows This bit is set and cleared by the application program and indicates if the Waiting Time Counter underflows.
[2]	TXCF	Character Transmission Request Flag. 0: No character transmitted 1: A character has been transmitted This bit is set by hardware and cleared by writing a “0” into it.

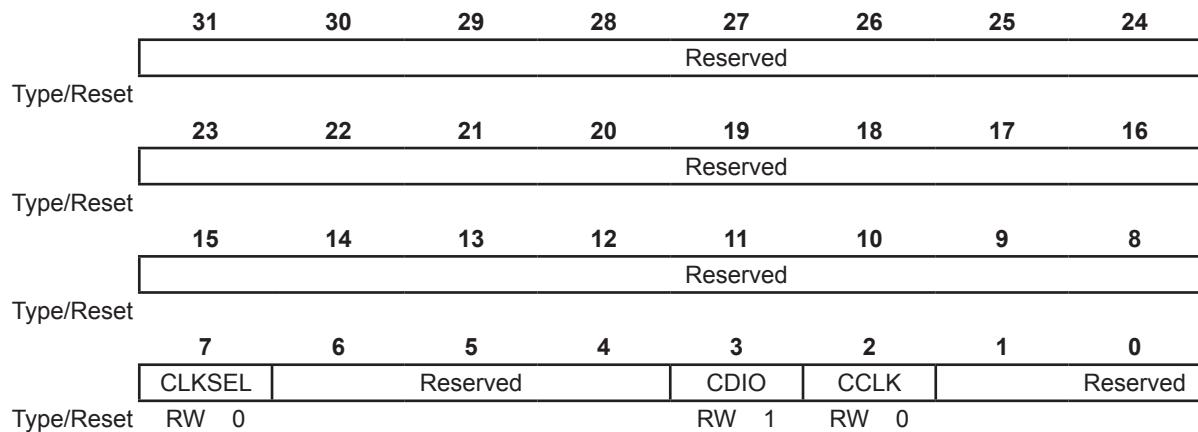
Bits	Field	Descriptions
[1]	RXCF	<p>Character Received Request Flag.</p> <p>0: No character received</p> <p>1: A character has been received</p> <p>This bit is set by hardware and cleared after a read access to the RXB register by the application program. The RXCF bit will be set to 1 when a character is received regardless of the result of the parity check.</p> <p>When the character has been received, the received data stored in the RXB register should be moved to the data memory as specified by the application program. If the contents of the RXB register are not read before the end of the next character to be shifted in, the data stored in the RXB register will be overwritten.</p>
[0]	PARF	<p>Parity Error Request Flag.</p> <p>0: No parity error occurs</p> <p>1: Parity error has occurred</p> <p>This bit is set by hardware and cleared by writing a “0” into it. When a character is received, the parity check circuitry will check that the parity is correct or not. If the result of the parity check is not correct, the parity error request flag, PARF, will be set to 1. Otherwise, the PARF bit will remain zero. In the Transmission Mode when the SCI is informed that there is a parity error in the transmitted character by the external Smart Card, the PARF bit will also be set to 1.</p>

SCI Contact Control Register – CCR

This register specifies the SCI pin setting and clock selection.

Offset: 0x008

Reset value: 0x0000_0008



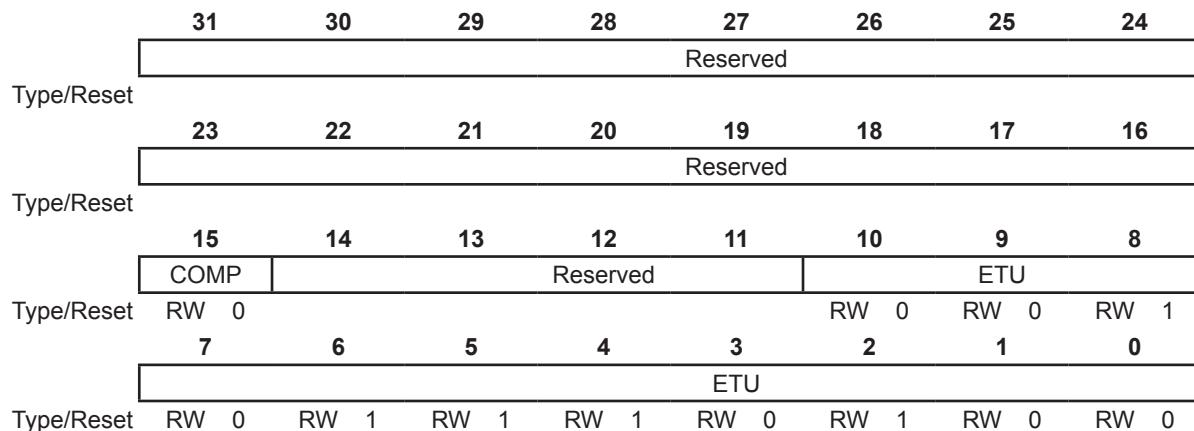
Bits	Field	Descriptions
[7]	CLKSEL	<p>Card Clock Selection</p> <p>0: The CCLK bit content is present on the external SCI_CLK pin.</p> <p>1: The clock output on the external SCI_CLK pin is sourced from the f_{PSC_CK} clock. This bit is used to select the external SCI_CLK pin clock source. It is set and cleared by the application program. It is recommended that to activate the clock at a known level a certain value should be first programmed into the CCLK bit before the CLKSEL bit is switched from 1 to 0.</p>
[3]	CDIO	<p>SCI_DIO pin control</p> <p>0: SCI_DIO pin is logic level 0.</p> <p>1: SCI_DIO pin in open-drain condition condition.</p> <p>This bit is available only when the SCIM bit in the CR register is cleared to 0 to configure the SCI to operate in the Manual Transfer Mode. It is set and cleared by application program to control the external SCI_DIO pin status in the Manual Mode. Reading this bit will return the present status of the SCI_DIO pin.</p>
[2]	CCLK	<p>SCI_CLK pin control.</p> <p>0: SCI_CLK pin is logic level 0</p> <p>1: SCI_CLK pin is logic level 1</p> <p>This bit is available only when the SCIM bit in the CR register is cleared to 0 to configure the SCI to operate in the Manual Transfer Mode. It is set and cleared by application program to control the external SCI_CLK pin status in the Manual Mode. Reading this bit will return the current value in the register and not the present status of the external SCI_CLK pin. To ensure that the clock remains at a known level a certain value should be first programmed into the CCLK bit before the CLKSEL bit is switched from 1 to 0.</p>

SCI Elementary Time Unit Register – ETUR

The register specifies the value determined by the formula described in the ETU section. It also includes the Compensation function enable control bit for the ETU time granularity.

Offset: 0x00C

Reset value: 0x0000_0174



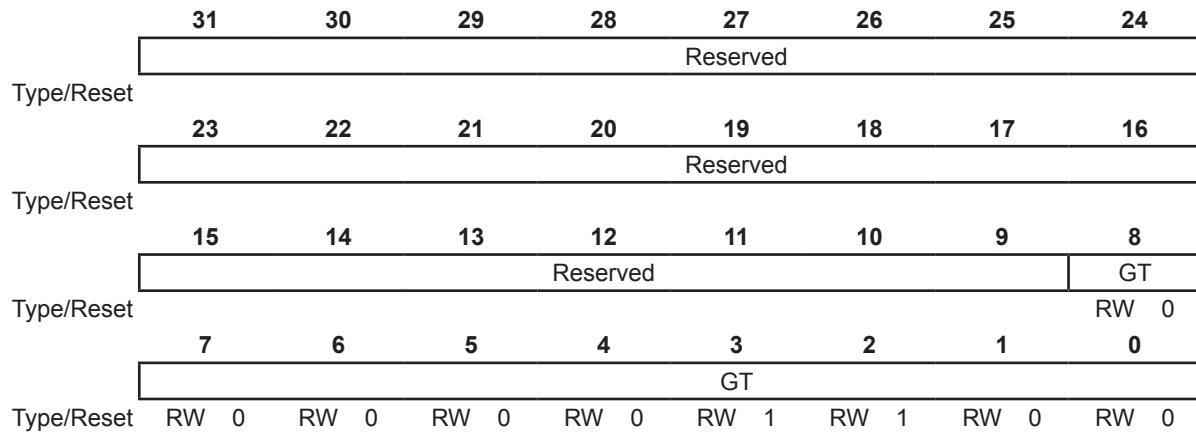
Bits	Field	Descriptions
[15]	COMP	<p>Elementary Time Unit Compensation mode enable control</p> <p>0: Compensation mode is disabled. 1: Compensation mode is enabled.</p> <p>This bit is set and cleared by application program and used to control the ETU compensation function. For more details regarding the compensation function consult the Elementary Time Unit section.</p>
[10:0]	ETU	<p>ETU value for a character data bit</p> <p>This field is configured by the application program to modify the ETU time duration. Note that the value of ETU must be in the range of 0x00C to 0x7FF. To obtain the maximum ETU decimal value of 2048, a 0x000 value should be written into this bit field.</p>

SCI Guard Time Register – GTR

This register specifies the guard time value obtained from the Answer-to-Reset packet described in the Guard Time Counter section.

Offset: 0x010

Reset value: 0x0000_000C



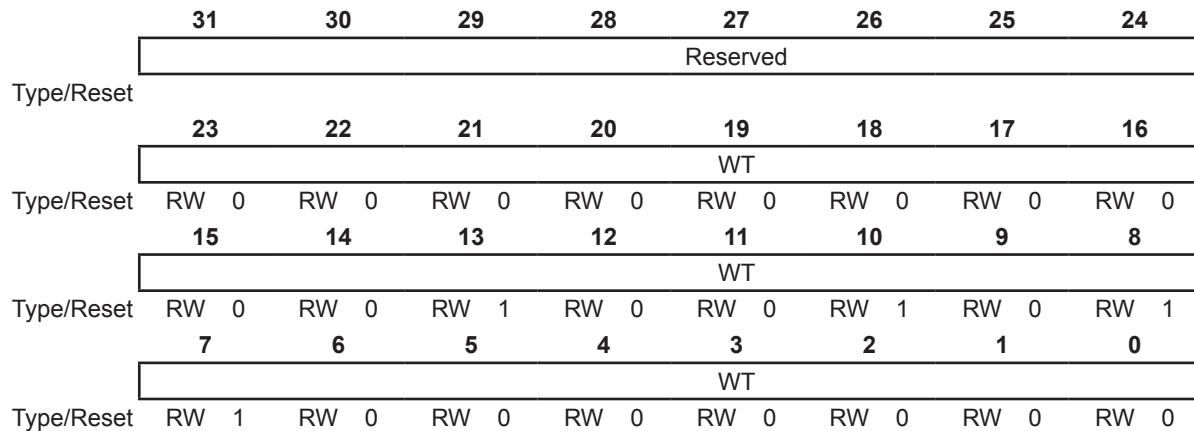
Bits	Field	Descriptions
[8:0]	GT	<p>Character Guard Time value</p> <p>This field is configured by the application program to modify the guard time duration. The updated GT value will be loaded into the GT counter at the end of the current guard time period. Note that the GT value must be in the range from 0x00C to 0x1FF.</p>

SCI Waiting Time Register – WTR

This register specifies the waiting time value obtained from the Answer-to-Reset packet described in the Waiting Time Counter section.

Offset: 0x014

Reset value: 0x0000_2580



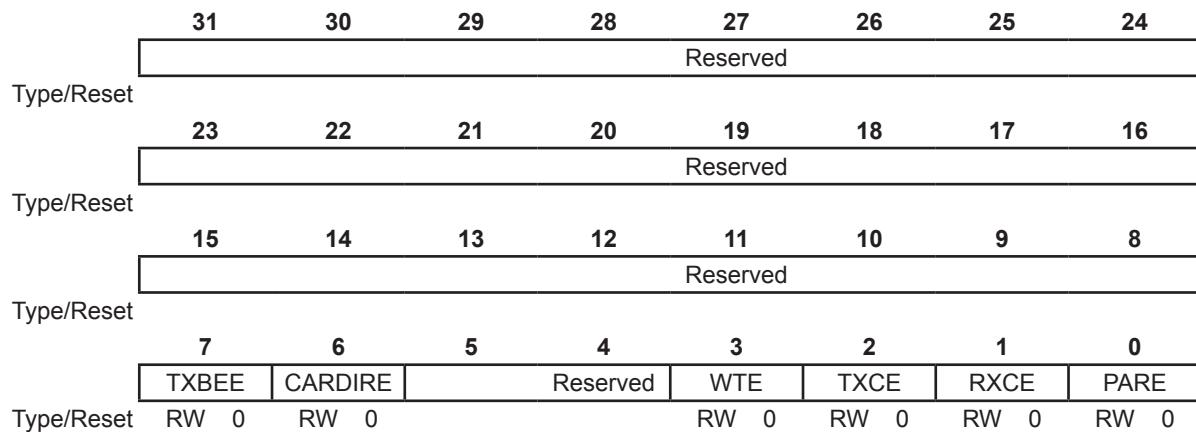
Bits	Field	Descriptions
[23:0]	WT	Character Waiting Time value expressed in ETU (0/16777215). This field is configured by the application program to modify the waiting time duration. The reload conditions of the updated waiting time counter value are described in the waiting time counter section. Refer to the waiting time counter section for more details. Note that the WT value can range from 0x00_0000 to 0xFF_FFFF.

SCI Interrupt Enable Register – IER

This register specifies the interrupt enable control bits for all of the interrupt events in the SCI.

Offset: 0x018

Reset value: 0x0000_0000



Bits	Field	Descriptions
[7]	TXBEE	<p>Transmit buffer empty interrupt enable control</p> <p>0: Disabled 1: Enabled</p> <p>This bit is set and cleared by application program and is used to control the Transmit Buffer Empty interrupt. If this bit is set to 1, the transmit buffer empty interrupt will be generated when the transmit buffer is empty.</p>
[6]	CARDIRE	<p>Card Insertion / Removal interrupt enable control</p> <p>0: Disabled 1: Enabled</p> <p>This bit is set and cleared by application program and is used to control the card insertion/removal interrupt. If this bit is set to 1, the card insertion/removal interrupt will be generated when the external Smart Card is inserted or removed.</p>
[3]	WTE	<p>Waiting Timer Underflow interrupt enable control</p> <p>0: Disabled 1: Enabled</p> <p>This bit is set and cleared by the application program and is used to control the Waiting Timer underflow interrupt. If this bit is set to 1, the waiting time counter underflow interrupt will be generated when the waiting time counter underflows.</p>

Bits	Field	Descriptions
[2]	TXCE	Character Transmission Completion interrupt enable control 0: Disabled 1: Enabled This bit is set and cleared by the application program and is used to control the Character Transmission Completion interrupt. If this bit is set to 1, the Character Transmission Completion interrupt will be generated at the end of the character transmission.
[1]	RXCE	Character Reception Completion interrupt enable control 0: Disabled 1: Enabled This bit is set and cleared by the application program and is used to control the Character Reception Completion interrupt. If this bit is set to 1, the Character Reception Completion interrupt will be generated at the end of the character reception.
[0]	PARE	Parity Error interrupt enable control 0: Disabled 1: Enabled This bit is set and cleared by the application program and is used to control the parity error interrupt. if this bit is set to 1, the Parity Error interrupt will be generated when a parity error occurs.

SCI Interrupt Pending Register – IPR

This register contains the interrupt pending flags for all of the interrupt events in the SCI. These pending flags can be masked by the corresponding interrupt enable control bits.

Offset: 0x01C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24	
Type/Reset	Reserved								
	23	22	21	20	19	18	17	16	
Type/Reset	Reserved								
	15	14	13	12	11	10	9	8	
Type/Reset	Reserved								
	7	6	5	4	3	2	1	0	
Type/Reset	TXBEP	CARDIRP		Reserved	WTP	TXCP	RXCP	PARP	
	RC 0	RC 0			RC 0	RC 0	RC 0	RC 0	

Bits	Field	Descriptions
[7]	TXBEP	<p>Transmit Buffer Empty interrupt pending flag</p> <p>0: No interrupt pending 1: Interrupt pending</p> <p>This bit is set by hardware and cleared by a read access to this register using the application program. This bit is used to indicate if there is a Transmit Buffer Empty interrupt pending or not. If the Transmit Buffer is empty and the corresponding interrupt enable control bit is set to 1, this bit will be set to 1 to indicate that the transmit buffer empty interrupt is pending.</p>
[6]	CARDIRP	<p>Card Insertion/Removal interrupt pending flag</p> <p>0: No interrupt pending 1: Interrupt pending</p> <p>This bit is set by hardware and cleared by a read access to this register using the application program. It is used to indicate if there is an external Smart Card insertion/removal interrupt pending or not. If an external Smart Card is inserted or removed and the corresponding interrupt enable control bit is set to 1, this bit will be set to 1 to indicate that the Card insertion/removal interrupt is pending.</p>
[3]	WTP	<p>Waiting Timer Underflow interrupt pending flag</p> <p>0: No interrupt pending 1: Interrupt pending</p> <p>This bit is set by hardware and cleared by a read access to this register using the application program. It is used to indicate if there is a waiting time counter underflow interrupt pending or not. If the waiting time counter underflows and the corresponding interrupt enable control bit is set to 1, this bit will be set to 1 to indicate that the waiting time counter underflow interrupt is pending.</p>

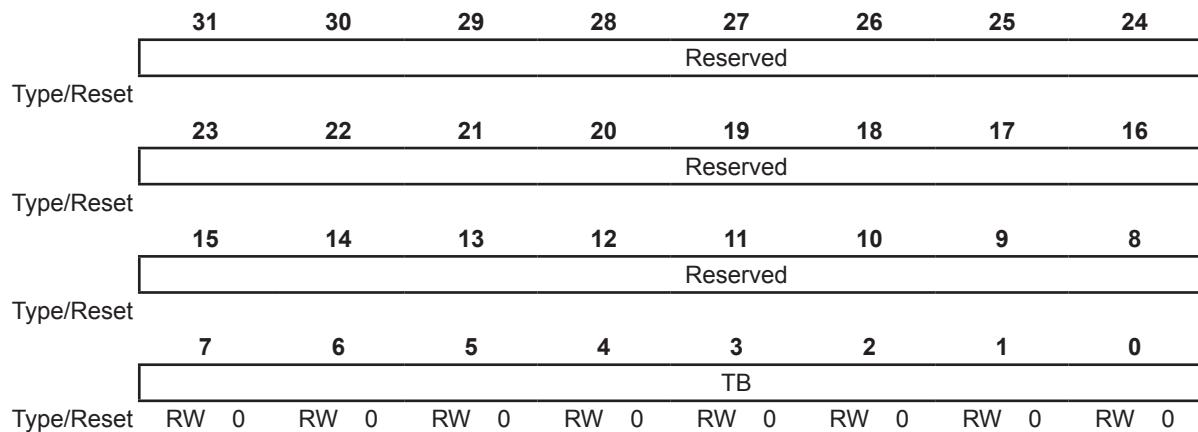
Bits	Field	Descriptions
[2]	TXCP	<p>Character Transmission Completion interrupt pending flag</p> <p>0: No interrupt pending</p> <p>1: Interrupt pending</p> <p>This bit is set by hardware and cleared by a read access to this register using the application program. It is used to indicate if there is a Character Transmission Completion interrupt pending or not. If a character has been transmitted and the related interrupt enable control bit is set to 1, this bit will be set to 1 to indicate that the character transmission completion interrupt is pending.</p>
[1]	RXCP	<p>Character Reception Completion interrupt pending flag</p> <p>0: No interrupt pending</p> <p>1: Interrupt pending</p> <p>This bit is set by hardware and cleared by a read access to this register using the application program. It is used to indicate if there is a Character Reception Completion interrupt pending or not. If a character has been received and the relevant interrupt enable control bit is set to 1, this bit will be set to 1 to indicate that the character reception completion interrupt is pending.</p>
[0]	PARP	<p>Parity Error interrupt pending flag</p> <p>0: No interrupt pending</p> <p>1: Interrupt pending</p> <p>This bit is set by hardware and cleared by a read access to this register using the application program. It is used to indicate if there is a Parity Error interrupt pending or not. If the parity error occurs and its interrupt enable control bit is set to 1, this bit will be set to 1 to indicate that the parity error interrupt is pending.</p>

SCI Transmit Buffer – TXB

This register is used to store the SCI data to be transmitted.

Offset: 0x020

Reset value: 0x0000_0000



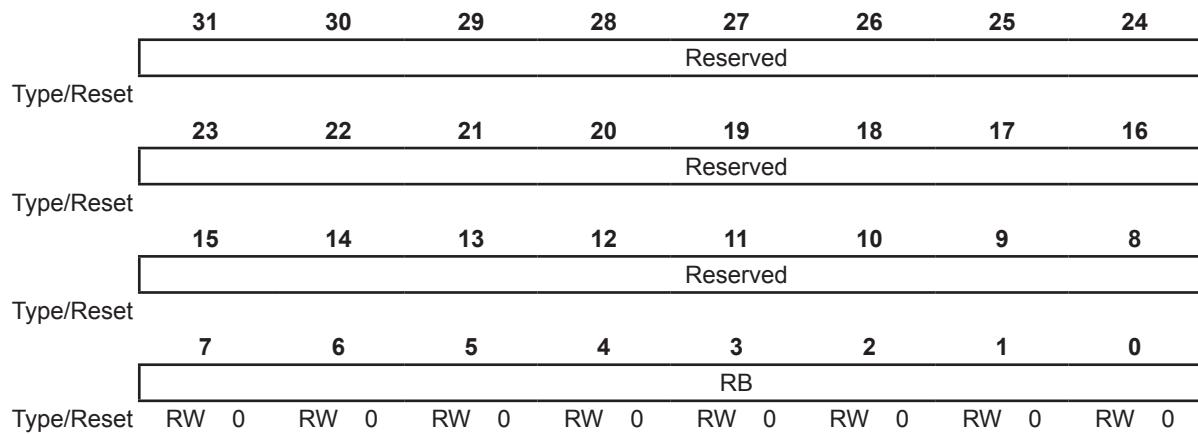
Bits	Field	Descriptions
[7:0]	TB	SCI data byte to be transmitted

SCI Receive Buffer – RXB

This register is used to store the SCI received data.

Offset: 0x024

Reset value: 0x0000_0000

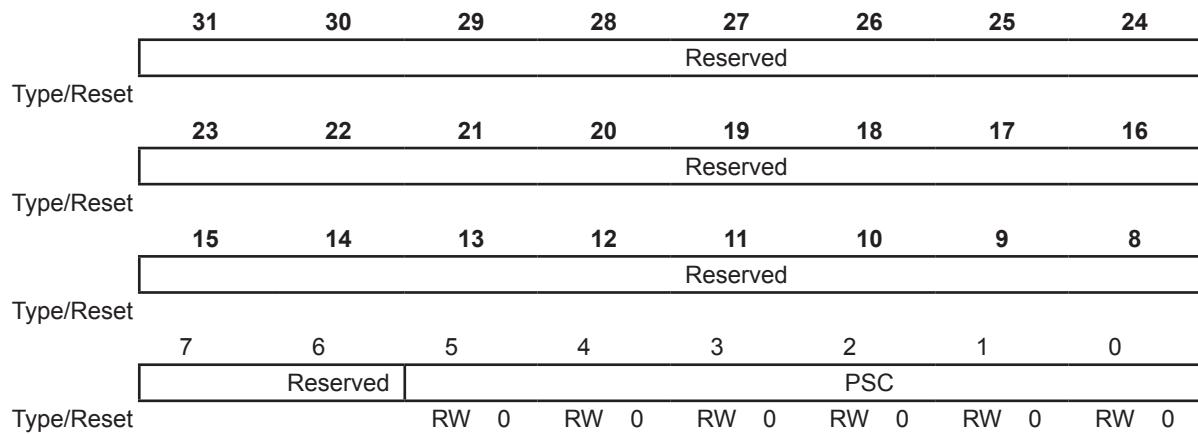


SCI Prescaler Register – PSCR

This register specifies the prescaler division ratio which is used the SCI internal clock.

Offset: 0x028

Reset value: 0x0000_0000



Bits	Field	Descriptions
[5:0]	PSC	SCI prescaler division ratio 0: $f_{PSC_CK} = f_{PCLK}$ 1~63: $f_{PSC_CK} = \frac{f_{PCLK}}{2 \times PSC}$

24 USB Device Controller (USB)

Introduction

The USB device controller is compliant with the USB 2.0 full-speed specification. There is one control endpoint known as Endpoint 0 and seven configurable endpoints (EP1~EP7). A 1024-byte EP-SRAM is used for the endpoint buffers. Each endpoint buffer size is programmable by corresponding registers, which provides maximum flexibility for various applications. The integrated USB full-speed transceiver helps to minimise overall system complexity and cost. The USB also contains the suspend and resume features to meet low-power consumption requirement. The accompanying figure shows the USB block diagram.

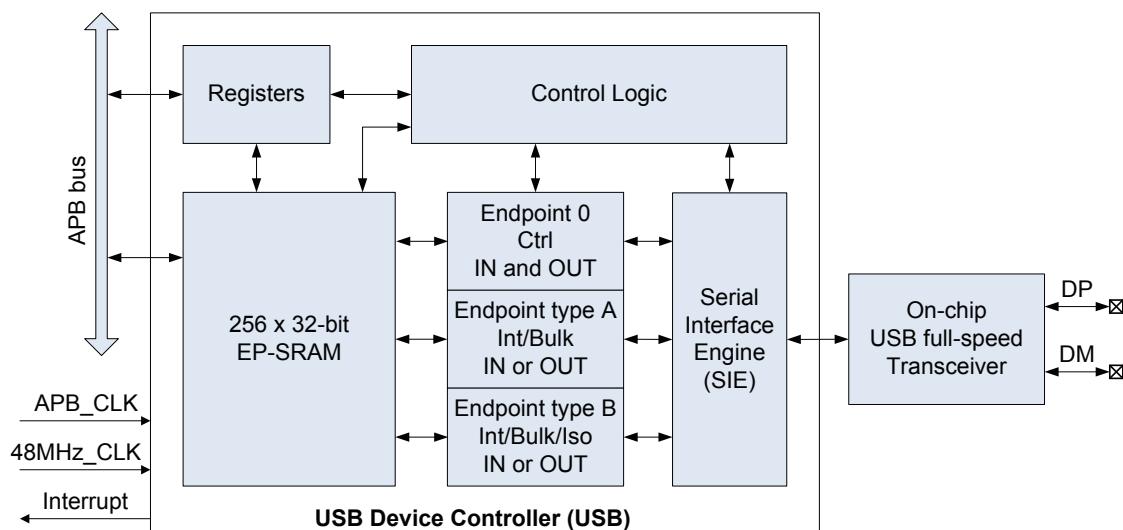


Figure 164. USB Block Diagram

Features

- Complies with USB 2.0 full-speed (12Mbps) specification
- Fully integrated USB full-speed transceiver
- 1 control endpoint (EP0) for control transfer
- 3 single-buffered endpoint (EP1~EP3) for bulk and interrupt transfer
- 4 double-buffered endpoint (EP4~EP7) for bulk, interrupt and isochronous transfer
- 1,024 bytes EP-SRAM used as endpoint data buffers

Functional Descriptions

Endpoints

The USB Endpoint 0 is the only bidirectional endpoint dedicated to USB control transfer. The device also contains seven unidirectional endpoint for other USB transfer types. There are three endpoints (EP1~EP3) which supports a single buffering function which is used for Bulk and Interrupt IN or OUT data transfer. There are four other endpoints (EP4~EP7) which supports single or double buffering functions for Bulk, Interrupt and Isochronous IN or OUT data transfer. The address of the seven unidirectional endpoints (EP1~EP7) can be configured by the application software. The following table lists the endpoint characteristics.

Table 62. Endpoint Characteristics

Endpoint Number	Number Address	Transfer Type	Direction	Buffer Type
0	Fixed	Control	IN and OUT	Single buffering
1~3	Configurable	Interrupt/Bulk	IN or OUT	Single buffering
4~7	Configurable	Interrupt/Bulk/ Isochronous	IN or OUT	Single or Double buffering

EP-SRAM

The USB controller contains a dedicated memory space, EP-SRAM, which is used for the USB endpoint buffers. The EP-SRAM, which is connected to the APB bus, can be accessed by the CPU and PDMA. The EP-SRAM base address is 0x4004_E400 with an offset which ranges from 0x000 to 0x3FF. The EP-SRAM first two words are reserved for Endpoint 0 to temporarily store the 8-byte SETUP data. Therefore the valid start address of the endpoint buffer should start from 0x008 and align to a 4-byte boundary. Each endpoint buffer size is programmable. The following table lists the maximum USB endpoint buffer size which is compliant with USB 2.0 full-speed device specification.

Table 63. USB Data Types and Buffer Size

Transfer Type	Direction	Supported Buffer Size	Bandwidth	CRC	Retrying
Control	Bidirectional	8, 16, 32, 64	Not guaranteed	Yes	Automatic
Bulk	Unidirectional	8, 16, 32, 64	Not guaranteed	Yes	Yes
Interrupt	Unidirectional	≤ 64	Not guaranteed	Yes	Yes
Isochronous	Unidirectional	< 512	Guaranteed	Yes	No

In the following endpoint buffer allocation example, the Endpoint “4” is configured as a double-buffered Bulk IN endpoint while the Endpoint “5” is configured as a double-buffered Bulk OUT endpoint. Each endpoint buffer size is set to 64-bytes.

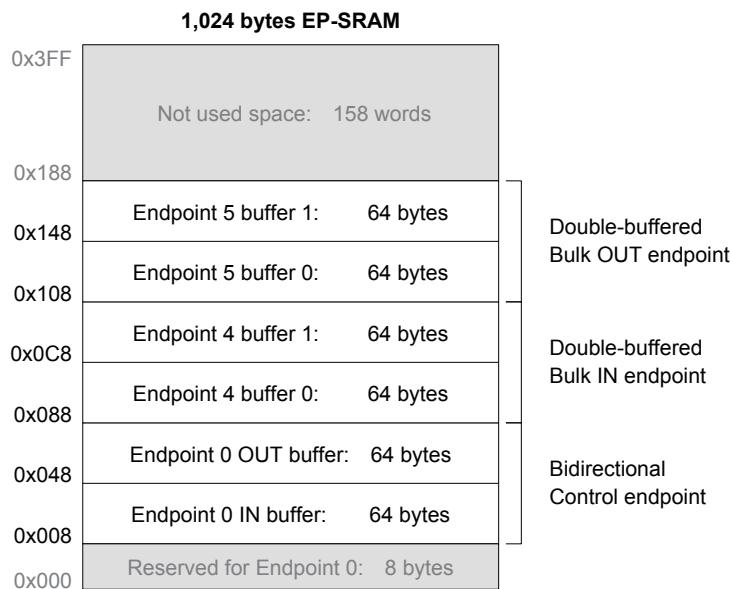


Figure 165. Endpoint Buffer Allocation Example

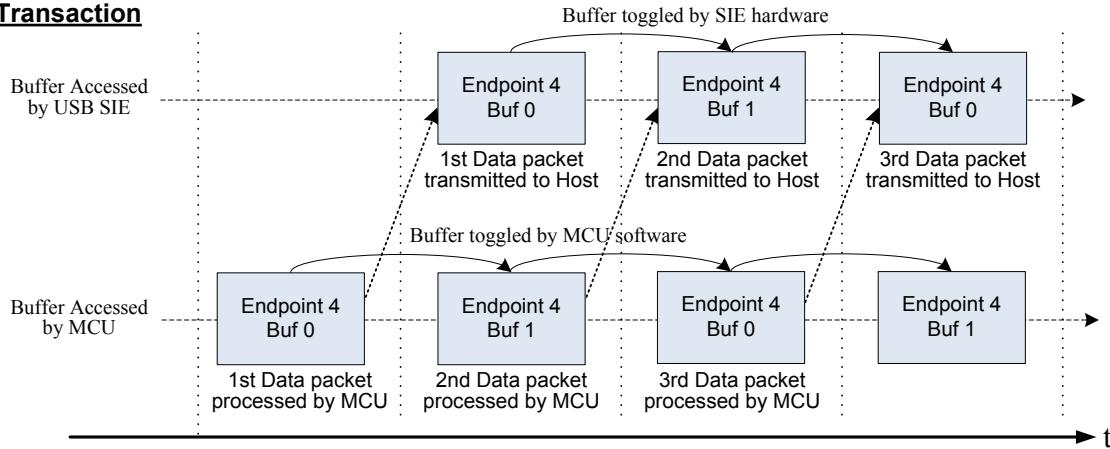
Serial Interface Engine – SIE

The Serial Interface Engine, SIE, which is connected to the USB full-speed transceiver and internal USB control circuitry provides a temporal buffer for the transmitted and received data. The SIE also decodes the SE0 signal, SE1 signal, J-state, K-state, USB RESET event and End of Packet event signals, EOP, when the USB module receives data, transmits data or transmits the resume signal for remote control. The SIE detects the number of SOF packets and generates the SOF interrupt signal to the USB control circuitry which includes data format conversion from parallel to serial or serial to parallel. It also includes, CRC checking and generation, PID decoder, bit-stuffing and debit-stuffing functions.

Double-Buffering

The double buffering function is recommended to be enabled when the corresponding endpoint is specified to be used for Isochronous transfer or high throughput Bulk transfer. The double buffering function stores the preceding data packet sent by the USB host in a single buffer for the MCU to process and the hardware will ensure that it continues to receive the current data packet in the other buffer during a OUT transaction, and vice versa. Using a double buffering function can achieve the highest possible data transfer rate. The details regarding double buffering usage is provided in the corresponding UDBTG and MDBTG control bit description in the USBEPnCSR register where the denotation n ranges from 4 to 7.

IN Transaction



OUT Transaction

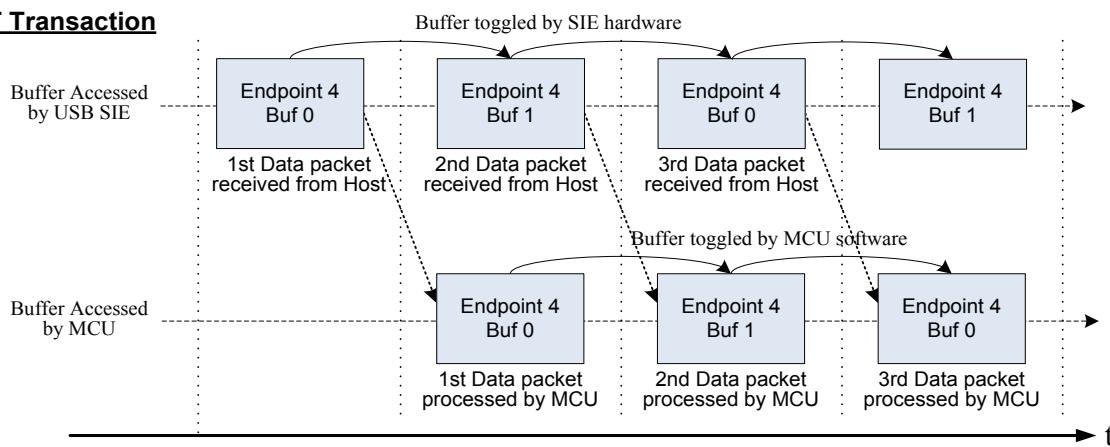


Figure 166. Double-buffering Operation Example

Suspend Mode and Wake-up

According to USB specifications, the device must enter the suspend mode after a 3ms bus idle time. When the USB device enters the suspend mode, the suspend mode current drawn from the USB bus must not be greater than 500 μ A to meet the specification suspend mode current requirements. The USB control circuitry will generate a suspend interrupt if the bus is in the idle state for 3ms. Here the software should set the LPMODE and PDWN bits in the USBCSR register to 1. The LPMODE bit is used to determine whether the USB controller enters the low power mode or not by holding the USB bus in a reset condition while the PDWN bit is used to determine if the integrated USB full-speed transceiver is turned off or not.

There are two ways for the USB host to wake up the USB device, one is to send a USB reset signal, SE0, and the other is to send a USB resume signal known as the K-state. After a wake-up signal, regardless of whether a SE0 signal or a K-state, is detected, the USB device will be woken up.

Remote Wake-up

As the USB device has a remote wake-up function, it can wake up the USB host by sending a resume request signal by setting the GENRSM bit in the USBCSR register to 1. Once the USB host receives the remote wake-up signal from the USB device, it will send a resume signal to the USB device.

Register Map

The following table shows the USB registers and reset values.

Table 64. USB Register map

Register	Offset	Description	Reset Value
USB Base Address = 0x400A_8000			
USBCSR	0x000	USB Control and Status Register	0x0000_00X6
USBIER	0x004	USB Interrupt Enable Register	0x0000_0000
USBISR	0x008	USB Interrupt Status Register	0x0000_0000
USBFCR	0x00C	USB Frame Count Register	0x0000_0000
USBDEVAR	0x010	USB Device Address Register	0x0000_0000
USBEP0CSR	0x014	USB Endpoint 0 Control and Status Register	0x0000_0002
USBEP0IER	0x018	USB Endpoint 0 Interrupt Enable Register	0x0000_0000
USBEP0ISR	0x01C	USB Endpoint 0 Interrupt Status Register	0x0000_0000
USBEP0TCR	0x020	USB Endpoint 0 Transfer Count Register	0x0000_0000
USBEP0CFG	0x024	USB Endpoint 0 Configuration Register	0x8000_0002
USBEP1CSR	0x028	USB Endpoint 1 Control and Status Register	0x0000_0002
USBEP1IER	0x02C	USB Endpoint 1 Interrupt Enable Register	0x0000_0000
USBEP1ISR	0x030	USB Endpoint 1 Interrupt Status Register	0x0000_0000
USBEP1TCR	0x034	USB Endpoint 1 Transfer Count Register	0x0000_0000
USBEP1CFG	0x038	USB Endpoint 1 Configuration Register	0x1000_03FF
USBEP2CSR	0x03C	USB Endpoint 2 Control and Status Register	0x0000_0002
USBEP2IER	0x040	USB Endpoint 2 Interrupt Enable Register	0x0000_0000
USBEP2ISR	0x044	USB Endpoint 2 Interrupt Status Register	0x0000_0000
USBEP2TCR	0x048	USB Endpoint 2 Transfer Count Register	0x0000_0000
USBEP2CFG	0x04C	USB Endpoint 2 Configuration Register	0x1000_03FF
USBEP3CSR	0x050	USB Endpoint 3 Control and Status Register	0x0000_0002

Register	Offset	Description	Reset Value
USBEP3IER	0x054	USB Endpoint 3 Interrupt Enable Register	0x0000_0000
USBEP3ISR	0x058	USB Endpoint 3 Interrupt Status Register	0x0000_0000
USBEP3TCR	0x05C	USB Endpoint 3 Transfer Count Register	0x0000_0000
USBEP3CFG	0x060	USB Endpoint 3 Configuration Register	0x1000_03FF
USBEP4CSR	0x064	USB Endpoint 4 Control and Status Register	0x0000_0002
USBEP4IER	0x068	USB Endpoint 4 Interrupt Enable Register	0x0000_0000
USBEP4ISR	0x06C	USB Endpoint 4 Interrupt Status Register	0x0000_0000
USBEP4TCR	0x070	USB Endpoint 4 Transfer Count Register	0x0000_0000
USBEP4CFG	0x074	USB Endpoint 4 Configuration Register	0x1000_03FF
USBEP5CSR	0x078	USB Endpoint 5 Control and Status Register	0x0000_0002
USBEP5IER	0x07C	USB Endpoint 5 Interrupt Enable Register	0x0000_0000
USBEP5ISR	0x080	USB Endpoint 5 Interrupt Status Register	0x0000_0000
USBEP5TCR	0x084	USB Endpoint 5 Transfer Count Register	0x0000_0000
USBEP5CFG	0x088	USB Endpoint 5 Configuration Register	0x1000_03FF
USBEP6CSR	0x08C	USB Endpoint 6 Control and Status Register	0x0000_0002
USBEP6IER	0x090	USB Endpoint 6 Interrupt Enable Register	0x0000_0000
USBEP6ISR	0x094	USB Endpoint 6 Interrupt Status Register	0x0000_0000
USBEP6TCR	0x098	USB Endpoint 6 Transfer Count Register	0x0000_0000
USBEP6CFG	0x09C	USB Endpoint 6 Configuration Register	0x1000_03FF
USBEP7CSR	0x0A0	USB Endpoint 7 Control and Status Register	0x0000_0002
USBEP7IER	0x0A4	USB Endpoint 7 Interrupt Enable Register	0x0000_0000
USBEP7ISR	0x0A8	USB Endpoint 7 Interrupt Status Register	0x0000_0000
USBEP7TCR	0x0AC	USB Endpoint 7 Transfer Count Register	0x0000_0000
USBEP7CFG	0x0B0	USB Endpoint 7 Configuration Register	0x1000_03FF

Register Descriptions

USB Control and Status Register – USBCSR

This register specifies the USB control bits and USB data line status.

Offset: 0x000

Reset value: 0x0000_00X6

	31	30	29	28	27	26	25	24	
	Reserved								
Type/Reset	23	22	21	20	19	18	17	16	
	Reserved								
Type/Reset	15	14	13	12	11	10	9	8	
	Reserved				DPWKEN	DPPUEN	SRAMRSTC	ADRSET	
Type/Reset					RW 0	RW 0	RW 0	RW 0	
	7	6	5	4	3	2	1	0	
Type/Reset	RXDM	RXDP	GENRSM	Reserved	LPMODE	PDWN	FRES	Reserved	
	RO X	RO X	RW 0		RW 0	RW 1	RW 1		

Bits	Field	Descriptions
[11]	DPWKEN	DP Wake Up Enable 0: Disable DP wake up 1: Enable DP wake up
[10]	DPPUEN	DP Pull Up Enable 0: Disable DP pull up 1: Enable DP pull up
[9]	SRAMRSTC	USB SRAM reset condition 0: Reset USB SRAM when (DP, DM) = (0,0) 1: User can access USB SRAM in spite of (DP, DM) state
[8]	ADRSET	Device Address Setting Control This bit is used to determine when the USB SIE updates the device address with the value of the USBDEVA register. 0: The SIE updates the device address immediately after an address is written into the USBDEVA register. 1: The SIE updates the device address after the USB Host has successfully read the data from the device by the IN operation. This bit is cleared by the SIE after the device address is updated.
[7]	RXDM	Received DM Line Status This bit is used to observe the status of DM data line status at the end of suspend routines to determine whether a wakeup event has occurred.
[6]	RXDP	Received DP Line Status This bit is used to observe the status of DP data line status at the end of suspend routines to determine whether a wakeup event has occurred.

Bits	Field	Descriptions
[5]	GENRSM	<p>Resume Request Generation Control</p> <p>This bit is used to generate a resume request which is sent to the USB host by writing 1 into this bit location. The USB remote wakeup function is always enabled. This bit will be cleared to 0 after a resume signal, sent by the USB host, has been received.</p>
[3]	LPMODE	<p>Low-power Mode Control</p> <p>This bit is used to determine the USB operating mode. Setting this bit will force the USB to enter the low-power mode. When USB bus traffic, known as a wakeup event, is detected by the hardware, this bit should be cleared by software.</p> <p>0: Exit the Low-power mode. 1: Enter the Low-power mode.</p>
[2]	PDWN	<p>Power Down Mode Control</p> <p>This bit is used to switch off the USB bus function. Setting this bit will power down the full-speed USB transceiver. This will disconnect the USB transceiver from the USB bus.</p> <p>0: Exit the Power-Down. 1: Enter the Power-Down mode.</p>
[1]	FRES	<p>Force USB Reset Control</p> <p>This bit is used to reset the USB circuitry. Setting this bit will force the USB into a reset state until the software clears it. A USB reset interrupt will be generated if the corresponding interrupt enable bit in the USBIER register is set to 1. All related USB registers are reset to their default values.</p> <p>0: Release USB reset. 1: Force USB reset.</p>

Table 65. Resume Event Detection

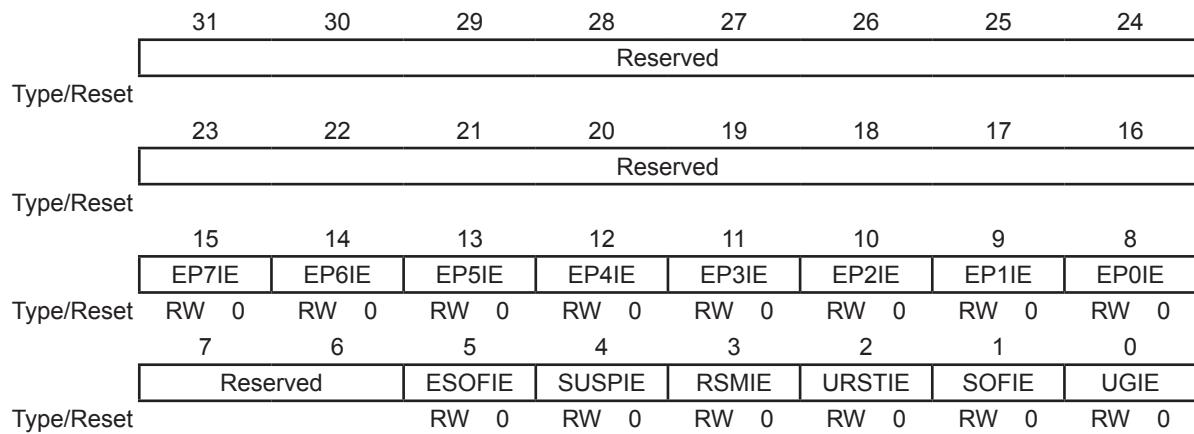
[RXDP, RXDM] Status	Wakeup event	Required resume software action
00	Root reset	None
10	None (noise on bus)	Go back to suspend mode
01	Root resume	None
11	Not allowed (noise on bus)	Go back to suspend mode

USB Interrupt Enable Register – USBIER

This register specifies the USB interrupt enable control.

Offset: 0x004

Reset value: 0x0000_0000



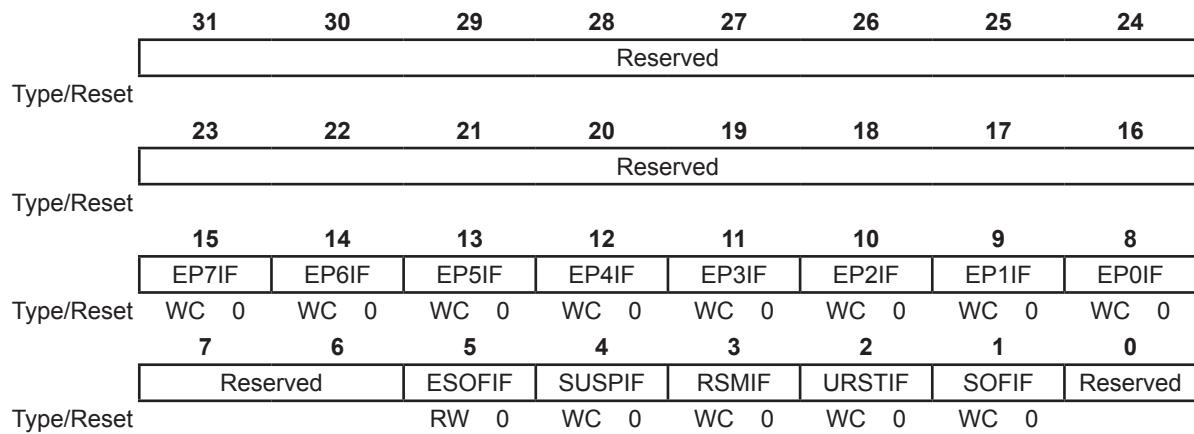
Bits	Field	Descriptions
[15:8]	EPnIE	Endpoint n Interrupt Enable Control (n = 0~7) 0: Disable interrupt 1: Enable interrupt
[5]	ESOFIE	Expected Start Of Frame (ESOF) Interrupt Enable Control 0: Disable ESOF interrupt 1: Enable ESOF interrupt
[4]	SUSPIE	Suspend Interrupt Enable Control 0: Disable suspend interrupt 1: Enable suspend interrupt
[3]	RSMIE	Resume Interrupt Enable Control 0: Disable Resume interrupt 1: Enable Resume interrupt
[2]	URSTIE	USB Reset Interrupt Enable Control 0: Disable USB Reset interrupt 1: Enable USB Reset interrupt
[1]	SOFIE	Start Of Frame (SOF) Interrupt Enable Control 0: Disable SOF interrupt 1: Enable SOF interrupt
[0]	UGIE	USB Global Interrupt Enable Control 0: USB Global interrupt is disabled 1: USB Global interrupt is enabled This bit must be set to 1 to enable the corresponding USB interrupt function, If this bit is cleared to 0, the relevant USB interrupt will not be generated, however, the corresponding interrupt flags still be asserted.

USB Interrupt Status Register – USBISR

This register specifies the USB interrupt status.

Offset: 0x008

Reset value: 0x0000_0000



Bits	Field	Descriptions
[15:8]	EPnIF	<p>Endpoint n Interrupt Flag (n = 0~7)</p> <p>This bit is set by the hardware to indicate the generation of relevant endpoint interrupt. Writing 1 into this bit to clear it. It is important to note that the interrupt flag can only be cleared when the endpoint interrupt status bit in the USBEPIISR register is equal to 0.</p>
[5]	ESOFIF	<p>Expected Start Of Frame Interrupt Flag</p> <p>This bit is set by the hardware when an SOF packet is expected to be received. The USB host sends an SOF (Start Of Frame) packet each millisecond. If the USB device hardware does not receive it properly, an ESOF interrupt will be generated when the ESOFIE bit in the USBIER register is set to 1. If three consecutive ESOF interrupts are generated, which means that the SOF packet has been missed 3 times, the SUSPIF will be set to 1. This bit will be set to 1 when the missing SOF packets occur if the timer is not yet locked.</p> <p>This bit can be read or written. However, only 0 can be written into this bit. Writing 1 has no effect.</p>

Bits	Field	Descriptions
[4]	SUSPIF	<p>Suspend Interrupt Flag</p> <p>This bit is set by the hardware when no data transfer has occurred for 3ms, indicating that a suspend request has been sent from the USB host. The suspend condition check is enabled immediately after a USB reset.</p> <p>This bit is cleared to 0 by writing 1.</p>
[3]	RSMIF	<p>Resume Interrupt Flag</p> <p>This bit is set by the hardware. When this bit is set 1, this means that a device resume has occurred.</p> <p>This bit is cleared to 0 by writing 1.</p>
[2]	URSTIF	<p>USB Reset Interrupt Flag</p> <p>This bit is set by the hardware when the USB reset has been detected. When a USB reset occurs, the internal protocol state machine will be reset and an USB reset interrupt will be generated if the URSTIE bit in the USBIER register is set to 1. Data reception and transmission are disabled until the URSTIF bit is cleared to 0. The USB configuration related registers (USBCSR, USBIER, USBISR, USBFCR and USBDEVAR) will not be reset by a USB reset event except for the USB device address (USBDEVAR), this is to ensure that a USB reset interrupt can be safely executed and any data transactions immediately followed by the USB reset can be completely accessed by the software. Therefore the microcontroller must properly reset these registers. The USB endpoint related registers (USBEPnCSR, USBEPnISR and USBEPnTCR) are also reset by a USB reset event, however, the endpoint configuration (USBEPnCFGGR) and interrupt enable (USBEPnIER) registers are not affected by the USB reset event and will remain unchanged.</p> <p>This bit is cleared to 0 by writing 1.</p>
[1]	SOFIF	<p>SOF Interrupt Flag</p> <p>This bit is set by the hardware when a start-of-frame packet has been received.</p> <p>This bit is cleared to 0 by writing 1.</p>

USB Frame Count Register – USBFCR

This register specifies the lost Start-of-Frame number and the USB frame count.

Offset: 0x00C

Reset value: 0x0000_0000



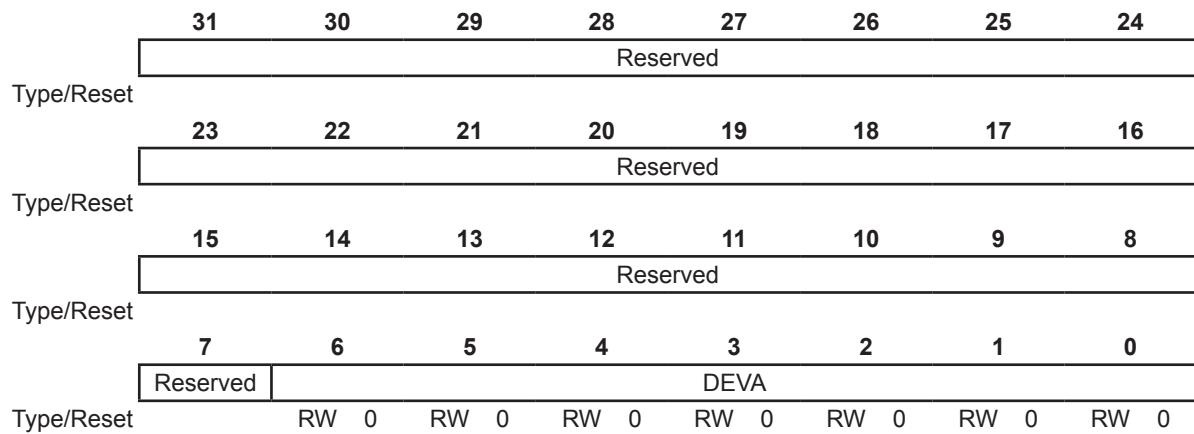
Bits	Field	Descriptions
[18:17]	LSOF	<p>Lost Start-of-Frame number</p> <p>These bits are written and incremented by 1 by the hardware each time the ESOFIF bit is set. It is used to count the number of lost SOF packets. When a SOF packet has been received, these bits are cleared.</p>
[16]	SOFLCK	<p>Start-of-Frame Lock Flag</p> <p>This bit is set by the hardware when a SOF packets have been received before the frame timer times out. Once this flag is set to 1, the frame number which is sent from the USB host will be loaded into the Frame Number field in the USBFCR register. If there no SOF packet has been received during the 1ms frame time duration, this bit will be cleared to 0.</p>
[10:0]	FRNUM	<p>Frame Number</p> <p>This field stores the frame number received from the USB host.</p>

USB Device Address Register – USBDEVA

This register specifies the USB device address.

Offset: 0x010

Reset value: 0x0000_0000



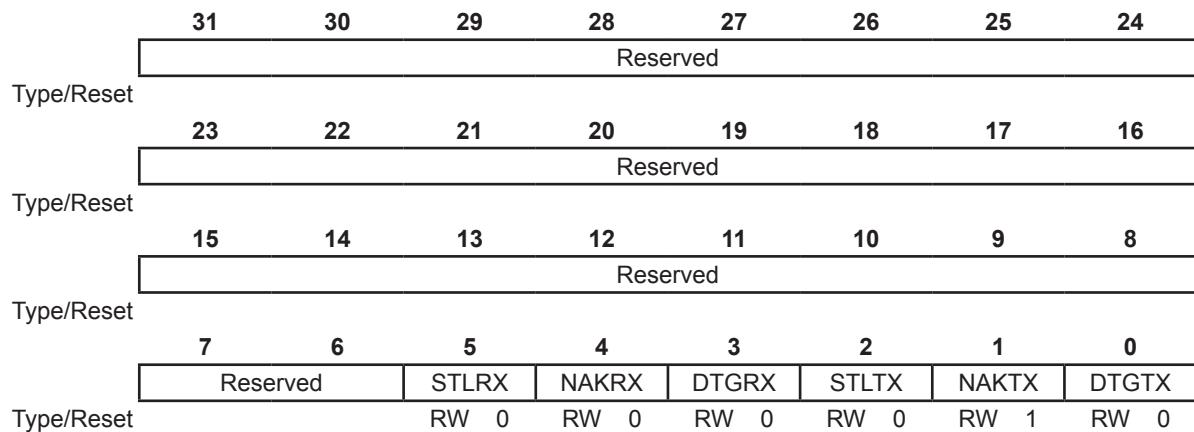
Bits	Field	Descriptions
[6:0]	DEVA	Device Address This field is used to specify the USB device address. This field is cleared when a USB reset event occurs.

USB Endpoint 0 Control and Status Register – USBEP0CSR

This register specifies the Endpoint 0 control and status.

Offset: 0x014

Reset value: 0x0000_0002



Bits	Field	Descriptions
[5]	STLRX	STALL Status for reception (OUT) transfer This bit is set to 1 by the application software and then returns a STALL signal in the handshake phase of an OUT transaction if a functional error is detected. This means that a control request delivered from the USB host is not supported by the USB device. The STALL status is cleared by the hardware circuitry when a SETUP token is received. This bit can be read and written and can only be toggled by writing 1.
[4]	NAKRX	NAK Status for reception (OUT) transfer This bit is toggled from 0 to 1 by the hardware circuitry, which will result in a NAK signal in the handshake phase of an OUT transaction after an ACK signal has been transmitted. This means that the USB device will be temporarily unable to accept data from the USB host. Therefore, more time will be required for the received data to be properly processed. This bit can be read and written and can only be toggled by writing 1.
[3]	DTGRX	Data Toggle Status for reception (OUT) transfer This bit contains the expected value of the data toggle bit (0=DATA0, 1=DTAT1) for the next data packet to be received. When the current valid data packet is received and the corresponding ACK signal is sent to the USB host by the USB device, the hardware circuitry will toggle this bit and the device will be ready to receive the next data packet. For Endpoint 0, the hardware circuitry will toggle this bit to 1 after the SETUP token is received as Endpoint 0 is addressed. This bit can also be toggled by the software to initialise its value for certain applications. This bit can be read and written and can only be toggled by writing 1.

Bits	Field	Descriptions
[2]	STLTX	<p>STALL Status for transmission (IN) transfer</p> <p>This bit is set to 1 by the application software and then returns a STALL signal in response to an IN token if a functional error is detected. This means that the USB device is unable to transmit data. The STALL status is cleared by the hardware circuitry when a SETUP token is received.</p> <p>This bit can be read and written and can only be toggled by writing 1.</p>
[1]	NAKTX	<p>NAK Status for transmission (IN) transfer</p> <p>This bit is toggled from 0 to 1 by the hardware circuitry, which will result in a NAK signal in the handshake phase of an IN transaction after an ACK signal has been received. It indicates that the USB device is temporarily unable to transmit data to the USB host. Therefore, there will be more time for the application software to properly prepare the data to be transmitted.</p> <p>This bit can be read and written and can only be toggled by writing 1.</p>
[0]	DTGTX	<p>Data Toggle Status for transmission (IN) transfer</p> <p>This bit contains the required value of the data toggle bit (0=DATA0, 1=DATA1) for the next data packet to be transmitted. When the current data packet is transmitted by the USB device and the corresponding ACK signal sent by the USB host is received, the hardware circuitry will toggle this bit and the next data packet will be transmitted. For Endpoint 0, the hardware circuitry will toggle this bit to 1 after the SETUP token is received as Endpoint 0 is addressed. This bit can also be toggled by the software to initialise its value for certain applications.</p> <p>This bit can be read and written and can only be toggled by writing 1.</p>

USB Endpoint 0 Interrupt Enable Register – USBEP0IER

This register specifies the Endpoint 0 interrupt control bits.

Offset: 0x018

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Reserved								
Type/Reset	23	22	21	20	19	18	17	16
Reserved								
Type/Reset	15	14	13	12	11	10	9	8
Reserved					ZLRXIE	SDERIE	SDRXIE	STRXIE
Type/Reset	RW	0	RW	0	RW	0	RW	0
	7	6	5	4	3	2	1	0
Type/Reset	RW	0	RW	0	RW	0	RW	0
	UERIE	STLIE	NAKIE	IDTXIE	ITRXIE	ODOVIE	ODRXIE	OTRXIE
	RW	0	RW	0	RW	0	RW	0

Bits	Field	Descriptions
[11]	ZLRXIE	Zero Length Data Received Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt
[10]	SDERIE	SETUP Data Error Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt
[9]	SDRXIE	SETUP Data Received Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt
[8]	STRXIE	SETUP Token Received Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt
[7]	UERIE	USB Error Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt
[6]	STLIE	STALL Transmitted Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt

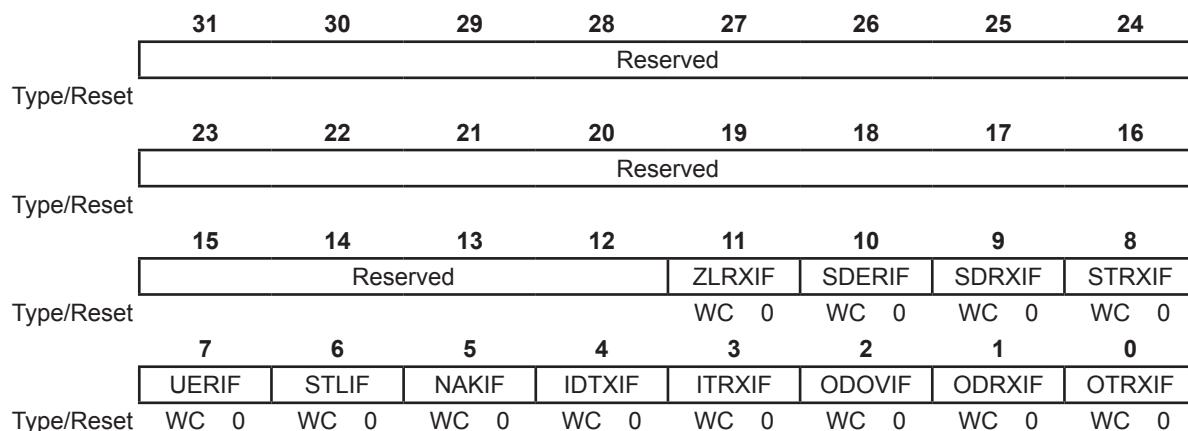
Bits	Field	Descriptions
[5]	NAKIE	NAK Transmitted Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt
[4]	IDTXIE	IN Data Transmitted Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt
[3]	ITRXIE	IN Token Received Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt
[2]	ODOVIE	OUT Data Buffer Overrun Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt
[1]	ODRXIE	OUT Data Received Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt
[0]	OTRXIE	OUT Token Received Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt

USB Endpoint 0 Interrupt Status Register – USBEP0ISR

This register specifies the Endpoint 0 interrupt status.

Offset: 0x01C

Reset value: 0x0000_0000



Bits	Field	Descriptions
[11]	ZLRXIF	Zero Length Data Received Interrupt Flag This bit is set by the hardware when a zero length data packet is received. This bit is cleared by hardware when a SETUP Token is received or by writing 1.
[10]	SDERIF	SETUP Data Error Interrupt Flag This bit is set by the hardware when the SETUP data packet length is not 8 bytes. This bit is cleared by hardware when a SETUP Token is received or by writing 1.
[9]	SDRXIF	SETUP Data Received Interrupt Flag This bit is set by the hardware when a SETUP data packet from the USB host has been received. This bit is cleared by the hardware when a SETUP Token is received or by writing 1. If the received SETUP data is not accessed by the application software before the next SETUP packet is received, the SETUP data buffer will be overwritten.
[8]	STRXIF	SETUP Token Received Interrupt Flag This bit is set by the hardware when a SETUP token is received and is cleared by writing 1.
[7]	UERIF	USB Error Interrupt Flag This bit is set by the hardware when an error occurs during the Endpoint 0 transaction. This bit is cleared by hardware when a SETUP Token is received or by writing 1.

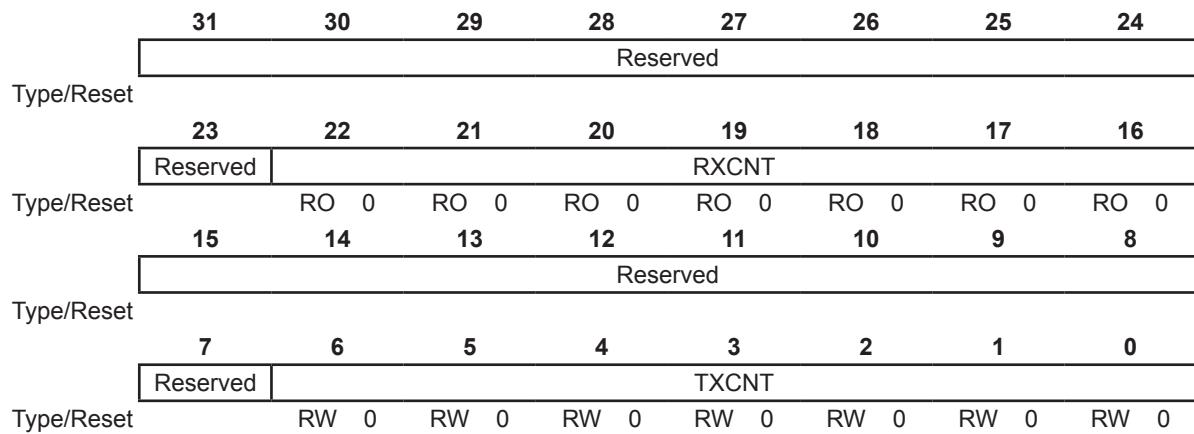
Bits	Field	Descriptions
[6]	STLIF	STALL Transmitted Interrupt Flag This bit is set by the hardware when a STALL signal is sent in response to an IN or OUT transaction. This bit is cleared by hardware when a SETUP Token is received or by writing 1.
[5]	NAKIF	NAK Transmitted Interrupt Flag This bit is set by the hardware when a NAK signal is sent in response to an IN or OUT transaction. This bit is cleared by hardware when a SETUP Token is received or by writing 1.
[4]	IDTXIF	IN Data Transmitted Interrupt Flag This bit is set by the hardware when a data packet is transmitted to and then an ACK signal is received from the USB host. This bit is cleared by hardware when a SETUP Token is received or by writing 1.
[3]	ITRXIF	IN Token Received Interrupt Flag This bit is set by the hardware when the IN token is received from the USB host. This bit is cleared by hardware when a SETUP Token is received or by writing 1.
[2]	ODOVIF	OUT Data Buffer Overrun Interrupt Flag This bit is set by the hardware when the number of received data bytes is larger than the endpoint buffer size. This bit is cleared by hardware when a SETUP Token is received or by writing 1.
[1]	ODRXIF	OUT Data Received Interrupt Flag This bit is set by the hardware when a data packet is successfully received from and then an ACK signal is sent to the USB host. This bit is cleared by hardware when a SETUP Token is received or by writing 1.
[0]	OTRXIF	OUT Token Received Interrupt Flag This bit is set by the hardware when the OUT token is received from the USB host. This bit is cleared by hardware when a SETUP Token is received or by writing 1.

USB Endpoint 0 Transfer Count Register – USBEP0TCR

This register specifies the Endpoint 0 data transfer byte count.

Offset: 0x020

Reset value: 0x0000_0000



Bits	Field	Descriptions
[22:16]	RXCNT	Reception Byte Count The bit field contains the number of data bytes received by Endpoint 0 in the preceding SETUP transaction.
[6:0]	TXCNT	Transmission Byte Count The bit field contains the number of data bytes to be transmitted by Endpoint 0 in the next IN token. If the value of this field is zero, it indicates that a zero length packet will be sent.

USB Endpoint 0 Configuration Register – USBEP0CFGR

This register specifies the Endpoint 0 configurations.

Offset: 0x024

Reset value: 0x8000_0002

	31	30	29	28	27	26	25	24
Type/Reset	EPEN	Reserved			EPADR			
	RO 1				RO 0	RO 0	RO 0	RO 0
	23	22	21	20	19	18	17	16
Type/Reset	Reserved							EPLN
								RW 0
	15	14	13	12	11	10	9	8
Type/Reset	EPLN							EPBUFA
	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
Type/Reset	EPBUFA							
	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 1	RW 0

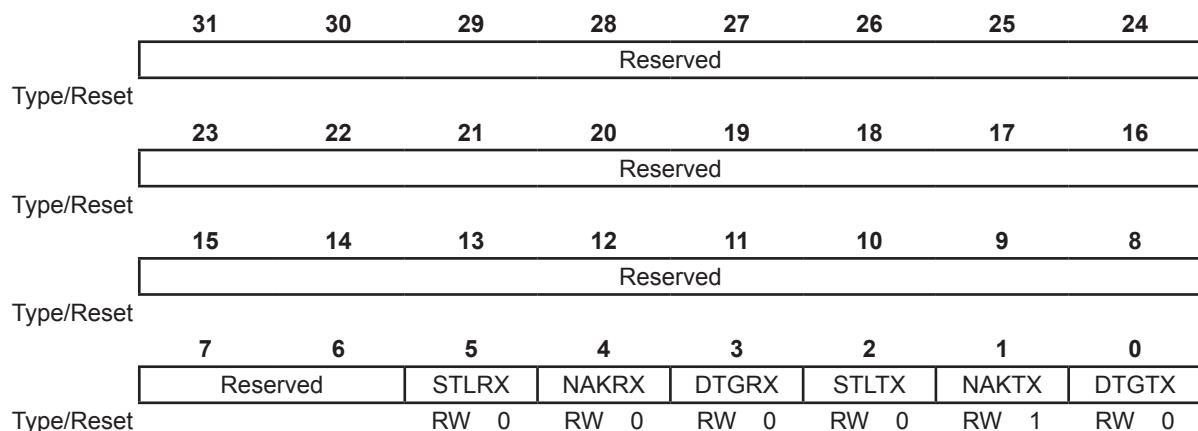
Bits	Field	Descriptions
[31]	EPEN	Endpoint Enable Control This bit is always set to 1 by the hardware circuitry to always enable Endpoint 0.
[27:24]	EPADR	Endpoint Address This field is always set to 0 by the hardware circuitry.
[16:10]	EPLN	Endpoint Buffer Length This field is used to specify the control transfer packet size which can be 8, 16, 32 or 64 bytes as defined in the USB full-speed standard specification.
[9:0]	EPBUFA	Endpoint Buffer Address This field is used to specify the start address of the Endpoint 0 buffer allocated in the EP_SRAM. It starts from 0x008 and should be aligned to 4-byte boundary. Start address of EP0 IN buffer = EPBUFA Start address of EP0 OUT buffer = EPBUFA + EPLN

USB Endpoint 1~3 Control and Status Register – USBE_nCSR, n=1~3

This register specifies the Endpoint 1~3 control and status bit.

Address: 0x028 (n=1), 0x03C (n=2), 0x050 (n=3)

Reset value: 0x0000_0002



Bits	Field	Descriptions
[5]	STLRX	STALL bit for reception transfers This bit is set to 1 by the application software if a functional error has been detected. This bit can be read and written and can only be toggled by writing 1. It can also be toggled by the software to initialise the value under certain conditions.
[4]	NAKRX	NAK bit for reception transfers This bit is toggled from 0 to 1 by the hardware circuitry, which will result in a NAK signal, when a data packet has been received and an ACK signal has been transmitted to the host in the handshake phase of an OUT transaction. It means that the USB device will be temporarily unable to accept data from the USB host until the received data is properly processed. This bit can be read and written and can be only toggled by writing 1.
[3]	DTGRX	Data Toggle bit for reception transfers This bit contains the expected value of the data toggle bit (0=DATA0,1=DATA1) for the next data packet to be received. When the current valid data packet is received and the corresponding ACK signal is sent to the USB host by the USB device, the hardware circuitry will toggle this bit and the device will be ready to receive the next data packet. This bit can be read and written and can only be toggled by writing 1. This bit can also be toggled by the software to initialise its value under certain conditions.

Bits	Field	Descriptions
[2]	STLTX	STALL bit for transmission transfers This bit is set to 1 by the application software if a functional error has been detected. This bit can be read and written and can be only toggled by writing 1. It can also be toggled by the software to initialise its value under certain conditions.
[1]	NAKTX	NAK bit for transmission transfers This bit is toggled from 0 to 1 by the hardware circuitry, which will result in a NAK signal, when a data packet has been transmitted and an ACK signal sent from the host has been received in the handshake phase of an IN transaction. It means that the USB device will be temporarily unable to transmit data packet until the data to be transmitted is appropriately prepared by the application software. This bit can be read and written and can be only toggled by writing 1.
[0]	DTGTX	Data Toggle bit for transmission transfers. This bit contains the required value of the data toggle bit (0=DATA0,1=DATA1) for the next data packet to be transmitted. When the current data packet is transmitted by the USB device and the corresponding ACK signal sent from the USB host is received, the hardware circuitry will toggle this bit and then the next data packet will be transmitted. This bit can be read and written and can only be toggled by writing 1. It can also be toggled by the software to initialise its value under certain conditions.

USB Endpoint 1~3 Interrupt Enable Register – USBEPnIER, n=1~3

This register specifies the Endpoint 1~3 interrupt enable control bits.

Address: 0x02C (n=1), 0x040 (n=2), 0x054 (n=3)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24	
Type/Reset	Reserved								
	23	22	21	20	19	18	17	16	
Type/Reset	Reserved								
	15	14	13	12	11	10	9	8	
Type/Reset	Reserved								
	7	6	5	4	3	2	1	0	
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	
	UERIE	STLIE	NAKIE	IDTXIE	ITRXIE	ODOVIE	ODRXIE	OTRXIE	

Bits	Field	Descriptions
[7]	UERIE	USB Error Interrupt Enable Control 1: Enable interrupt 0: Disable interrupt
[6]	STLIE	STALL Transmitted Interrupt Enable Control 1: Enable interrupt 0: Disable interrupt
[5]	NAKIE	NAK Transmitted Interrupt Enable Control 1: Enable interrupt 0: Disable interrupt
[4]	IDTXIE	IN Data Transmitted Interrupt Enable Control 1: Enable interrupt 0: Disable interrupt
[3]	ITRXIE	IN Token Received Interrupt Enable Control 1: Enable interrupt 0: Disable interrupt
[2]	ODOVIE	OUT Data Buffer Overrun Interrupt Enable Control 1: Enable interrupt 0: Disable interrupt
[1]	ODRXIE	OUT Data Received Interrupt Enable Control 1: Enable interrupt 0: Disable interrupt
[0]	OTRXIE	OUT Token Received Interrupt Enable Control 1: Enable interrupt 0: Disable interrupt

USB Endpoint 1~3 Interrupt Status Register – USBEPnISR, n=1~3

This register specifies the Endpoint 1~3 interrupt status.

Address: 0x030 (n=1), 0x044 (n=2), 0x058 (n=3)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24	
Type/Reset	Reserved								
	23	22	21	20	19	18	17	16	
Type/Reset	Reserved								
	15	14	13	12	11	10	9	8	
Type/Reset	Reserved								
	7	6	5	4	3	2	1	0	
Type/Reset	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	

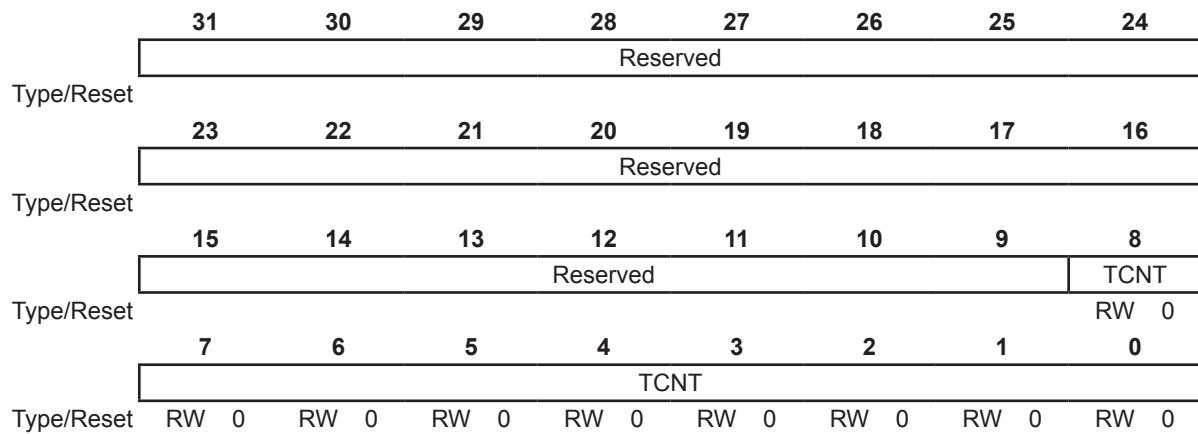
Bits	Field	Descriptions
[7]	UERIF	USB Error Interrupt Flag. This bit is set by the hardware when an error occurs during the transaction. Writing 1 into this status bit will clear it to 0.
[6]	STLIF	STALL Transmitted Interrupt Flag. This bit is set by hardware circuitry when a STALL-token is sent in response to an IN or OUT token and is cleared to 0 by writing 1.
[5]	NAKIF	NAK Transmitted Interrupt Flag. This bit is set by hardware circuitry when a NAK-token is sent in response to an IN or OUT token and is cleared to 0 by writing 1.
[4]	IDTXIF	IN Data Transmitted Interrupt Flag. This bit is set by hardware circuitry when a data packet is successfully transmitted to the host in response to an IN-token and an ACK-token is received. Writing 1 into this status bit will clear it to 0.
[3]	ITRXIF	IN Token Received Interrupt Flag. This bit is set by the hardware circuitry when the endpoint receives an IN token from the host and is cleared to 0 by writing 1.
[2]	ODOVIF	OUT Data Buffer Overrun Interrupt Flag. This bit is set by the hardware circuitry when the received data byte count is larger than the corresponding endpoint OUT data buffer size. Writing 1 into this status bit will clear it to 0.
[1]	ODRXIF	OUT Data Received Interrupt Flag. This bit is set by the hardware circuitry when a data packet is successfully received from the host for an OUT-token and when an endpoint n ACK signal is sent to the host. Writing 1 into this status bit will clear it to 0.
[0]	OTRXIF	OUT Token Received Interrupt Flag. This bit is set by the hardware circuitry when the endpoint receives an OUT token from the host and is cleared to 0 by writing 1.

USB Endpoint 1~3 Transfer Count Register – USBEPnTCR, n=1~3

This register specifies the Endpoint 1~3 transfer byte count.

Address: 0x034 (n=1), 0x048 (n=2), 0x05C (n=3)

Reset value: 0x0000_0000



Bits	Field	Descriptions
[8:0]	TCNT	<p>Transfer Byte Count</p> <p>These bit field contains the number of bytes received by the endpoint n in the preceding OUT transaction or the number of bytes to be transmitted by the endpoint n in the next IN transaction.</p>

USB Endpoint 1~3 Configuration Register – USBE_nCFGR, n=1~3

This register specifies the Endpoint 1~3 configurations.

Address: 0x038 (n=1), 0x04C (n=2), 0x060 (n=3)

Reset value: 0x1000_03FF

	31	30	29	28	27	26	25	24
Type/Reset	EPEN	Reserved	EPTYPE	EPDIR		EPADR		
	RW 0		RW 0	RW 1	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
Type/Reset				Reserved			EPLN	
							RW 0	
	15	14	13	12	11	10	9	8
Type/Reset				EPLN			EPBUFA	
	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 1	RW 1
	7	6	5	4	3	2	1	0
Type/Reset				EPBUFA				
	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1

Bits	Field	Descriptions
[31]	EPEN	Enable Control 0: Disable the endpoint n 1: Enable the endpoint n
[29]	EPTYPE	Transfer Type This bit is set to 0 by the hardware circuitry to specify that the endpoint n transfer type is an Interrupt or Bulk transfer type.
[28]	EPDIR	Transfer Direction 0: OUT 1: IN
[27:24]	EPADR	Endpoint Address The EPADR field value can be assigned by the application software to specify the address of the endpoint n. It is important to note that this EPADR field should not be set to 0, otherwise, the endpoint will be disabled.
[16:10]	EPLN	Buffer Length This field is used to specify the endpoint n data packet size. The field value must be word-aligned to a 4-byte boundary. The maximum size in this field can be 64 bytes which is the maximum payload as defined in the USB full-speed standard specification. Note that the EPLN value should not be assigned to 0 which will result in the endpoint being disabled.
[9:0]	EPBUFA	Endpoint Buffer Address This field is used to specify the endpoint n data buffer start address which ranges from 0x008 to 0x3FC in the EP-SRAM which has a capacity of 1024 bytes and whose field value must be a multiple of 4.

USB Endpoint 4~7 Control and Status Register – USBE_nCSR, n=4~7

This register specifies the Endpoint 4~7 control and status bits.

Address: 0x064 (n=4), 0x078 (n=5), 0x08C (n=6), 0x0A0 (n=7)

Reset value: 0x0000_0002

	31	30	29	28	27	26	25	24	
Type/Reset	Reserved								
	23	22	21	20	19	18	17	16	
Type/Reset	Reserved								
	15	14	13	12	11	10	9	8	
Type/Reset	Reserved								
	7	6	5	4	3	2	1	0	
Type/Reset	UDBTG	MDBTG	STLRX	NAKRX	DTGRX	STLTX	NAKTX	DTGTX	
	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 1	RW 0	

Bits	Field	Descriptions				
[7]	UDBTG	USB Double Buffer Toggle bit The UDBTG and MDBTG bits are used to indicate which data buffer is accessed by the USB SIE hardware and which data buffer is accessed by the MCU software if the double buffering function is enabled. The UDBTG bit will be toggled by the SIE hardware circuitry after the current buffer operation is complete. After the UDBTG bit is toggled by the SIE, a NAK signal will be sent automatically to the USB host by the hardware circuitry. Therefore, the data transfer will be stopped temporarily until the data in the other buffer has been properly setup after which the MDBTG bit is toggled by the MCU application software. The following tables show the double buffering operation and the UDBTG and MDBTG bit status for an IN or OUT transaction.				
		Transaction Type UDBTG MDBTG Buffer read by SIE Buffer written by MCU				
		IN	0	0	None*	EP_BUFO
			0	1	EP_BUFO	EP_BUFI
			1	0	EP_BUFI	EP_BUFO
			1	1	None*	EP_BUFI
		Transaction Type UDBTG MDBTG Buffer written by SIE Buffer read by MCU				
		OUT	0	0	None*	EP_BUFI
			0	1	EP_BUFO	EP_BUFI
			1	0	EP_BUFI	EP_BUFO
			1	1	None*	EP_BUFO

* Means the USB device sends a NAK signal to the USB host using the hardware circuitry.

The UDBTG and MDBTG bits setting procedure for the double buffering function is shown in the following example:

[UDBTG, MDBTG]=[0, 0] → [0, 1] → [1, 1] → [1, 0] → [0, 0] → [0, 1] → [1, 1] → [1, 0]
→...

Bits	Field	Descriptions
[6]	MDBTG	<p>MCU Double Buffer Toggle bit</p> <p>The MDBTG bit is used to indicate which data buffer is accessed by the MCU if the double buffering function is enabled. It can be toggled to switch to the other buffer by the MCU application software after the data in the current buffer accessed by the MCU has been properly setup. The double buffering operation together with the UDBTG and MDBTG bits are shown in the preceding two tables for the UDBTG bit definition</p>
[5]	STLRX	<p>STALL bit for reception transfers</p> <p>This bit is set to 1 by the application software if a functional error has been detected.</p> <p>This bit can be read and written and can only be toggled by writing 1. It can also be toggled by software to initialise its value under certain conditions</p>
[4]	NAKRX	<p>NAK bit for reception transfers</p> <p>This bit is toggled from 0 to 1 by the hardware circuitry, which will result in a NAK signal, when a data packet has been received and an ACK signal has been transmitted to the host in the handshake phase of an OUT transaction addressed to this endpoint. It means that the USB device will be temporarily unable to accept data from the USB host until the received data is properly processed. If the endpoint is defined as an Isochronous transfer type, this bit is not available for use. The hardware will not change the NAKRX bit status after a complete transaction.</p> <p>This bit can be read and written and can be only toggled by writing 1.</p>
[3]	DTGRX	<p>Data Toggle bit for reception transfers</p> <p>If the endpoint is not used for Isochronous transfer, this bit is available for use. This bit contains the expected value of the data toggle bit (0=DATA0,1=DATA1) for the next data packet to be received. When the current valid data packet is received and the corresponding ACK signal is sent to the USB host by the USB device, the hardware circuitry will toggle this bit and the device will be ready to receive the next data packet. If the endpoint is defined as an Isochronous transfer type, this bit is not used since no data toggling is used and only the DATA0 packet will be transferred for normal Isochronous transfers.</p> <p>This bit can be read and written and can only be toggled by writing 1. This bit can also be toggled by the software to initialise its value under certain conditions</p>
[2]	STLTX	<p>STALL bit for transmission transfers</p> <p>This bit is set to 1 by the application software if there is a functional error has been detected.</p> <p>This bit can be read and written and can be only toggled by writing 1. It can be toggled by the software to initialise its value under certain conditions.</p>

Bits	Field	Descriptions
[1]	NAKTX	<p>NAK bit for transmission transfers</p> <p>This bit is toggled from 0 to 1 by the hardware circuitry. This will result in a NAK signal when a data packet has been transmitted and an ACK signal sent from the host has been received in the handshake phase of an IN transaction addressed to this endpoint. It means that the USB device will be temporarily unable to transmit a data packet until the data to be transmitted is properly setup by the application software. If the endpoint is defined as an Isochronous transfer type, then this bit is not available for use. The hardware will not change the NAKTX bit status after a complete transaction.</p> <p>This bit can be read and written and can be only toggled by writing 1. It can also be toggled by the software to initialise its value under certain conditions.</p>
[0]	DTGTX	<p>Data Toggle bit for transmission transfers.</p> <p>If the endpoint is not used for Isochronous transfer, this bit is available for use. This bit contains the required value of the data toggle bit (0=DATA0, 1=DATA1) for the next data packet to be transmitted. When the current data packet is transmitted by the USB device and the corresponding ACK signal sent from the USB host is received, the hardware circuitry will toggle this bit and then the next data packet will be transmitted. If the endpoint is used for Isochronous transfer, this bit is not used since no data toggling is used and only the DATA0 packet will be transferred for normal Isochronous transfer.</p> <p>This bit can be read and written and can only be toggled by writing 1. It can also be toggled by the software to initialise its value under certain conditions.</p>

USB Endpoint 4~7 Interrupt Enable Register – USBEPnIER, n=4~7

This register specifies the Endpoint 4~7 interrupt enable control bits.

Offset: 0x068 (n=4), 0x07C (n=5), 0x090 (n=6), 0x0A4 (n=7)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Reserved								
Type/Reset	23	22	21	20	19	18	17	16
Reserved								
Type/Reset	15	14	13	12	11	10	9	8
Reserved								
Type/Reset	7	6	5	4	3	2	1	0
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	UERIE	STLIE	NAKIE	IDTXIE	ITRXIE	ODOVIE	ODRXIE	OTRXIE

Bits	Field	Descriptions
[7]	UERIE	USB Error Interrupt Enable Control 1: Enable interrupt 0: Disable interrupt
[6]	STLIE	STALL Transmitted Interrupt Enable Control 1: Enable interrupt 0: Disable interrupt
[5]	NAKIE	NAK Transmitted Interrupt Enable Control 1: Enable interrupt 0: Disable interrupt
[4]	IDTXIE	IN Data Transmitted Interrupt Enable Control 1: Enable interrupt 0: Disable interrupt
[3]	ITRXIE	IN Token Received Interrupt Enable Control 1: Enable interrupt 0: Disable interrupt
[2]	ODOVIE	OUT Data Buffer Overrun Interrupt Enable Control 1: Enable interrupt 0: Disable interrupt
[1]	ODRXIE	OUT Data Received Interrupt Enable Control 1: Enable interrupt 0: Disable interrupt
[0]	OTRXIE	OUT Token Received Interrupt Enable Control 1: Enable interrupt 0: Disable interrupt

USB Endpoint 4~7 Interrupt Status Register – USBE_nISR, n=4~7

This register specifies the Endpoint 4~7 interrupt status.

Offset: 0x06C (n=4), 0x080 (n=5), 0x094 (n=6), 0x0A8 (n=7)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24	
Type/Reset	Reserved								
	23	22	21	20	19	18	17	16	
Type/Reset	Reserved								
	15	14	13	12	11	10	9	8	
Type/Reset	Reserved								
	7	6	5	4	3	2	1	0	
Type/Reset	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	
	UERIF	STLIF	NAKIF	IDTXIF	ITRXIF	ODOVIF	ODRXIF	OTRXIF	

Bits	Field	Descriptions
[7]	UERIF	USB Error Interrupt flag This bit is set by the hardware circuitry when an error occurs during the transaction. Writing 1 into this status bit will clear it to 0.
[6]	STLIF	STALL Transmitted Interrupt flag This bit is set by the hardware circuitry when a STALL-token is sent in response to an IN or OUT token and is cleared to 0 by writing 1.
[5]	NAKIF	NAK Transmitted Interrupt flag This bit is set by the hardware circuitry when a NAK-token is sent in response to an IN or OUT token and is cleared to 0 by writing 1.
[4]	IDTXIF	IN Data Transmitted Interrupt flag This bit is set by the hardware circuitry when a data packet is successfully transmitted to the host in response to an IN-token and an ACK-token is received. Writing 1 into this status bit will clear it to 0.
[3]	ITRXIF	IN Token Received Interrupt flag This bit is set by the hardware circuitry when the endpoint receives an IN token from the host and is cleared to 0 by writing 1.
[2]	ODOVIF	OUT Data Buffer Overrun Interrupt flag This bit is set by the hardware circuitry when the received data byte count is larger than the endpoint OUT data buffersize. Writing 1 into this status bit will clear it to 0.
[1]	ODRXIF	OUT Data Received Interrupt flag This bit is set by the hardware circuitry when a data packet is successfully received from the host for an OUT-token and an ACK signal is sent to the host. Writing 1 into this status bit will clear it to 0.
[0]	OTRXIF	OUT Token Received Interrupt flag This bit is set by the hardware circuitry when the endpoint receives an OUT token from the host and is cleared to 0 by writing 1.

USB Endpoint 4~7 Transfer Count Register – USBE_nTCR, n=4~7

This register specifies the Endpoint 4~7 transfer byte count.

Offset: 0x070 (n=4), 0x084 (n=5), 0x098 (n=6), 0x0AC (n=7)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Type/Reset	Reserved							TCNT1
								RW 0 RW 0
	23	22	21	20	19	18	17	16
Type/Reset	TCNT1							
	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
Type/Reset	Reserved							TCNT0
								RW 0 RW 0
	7	6	5	4	3	2	1	0
Type/Reset	TCNT0							
	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[25:16]	TCNT1	<p>Buffer 1 Transfer Byte Count</p> <p>This bit field contains the number of data bytes received by the endpoint n buffer 1 in the preceding OUT transaction or the number of data bytes to be transmitted by the endpoint n buffer1 in the next IN transaction.</p>
[9:0]	TCNT0	<p>Buffer 0 Transfer Byte Count</p> <p>This bit field contains the number of data bytes received by the endpoint n buffer 0 in the preceding OUT transaction or the number of data bytes to be transmitted by the endpoint n buffer 0 in the next IN transaction. Only the TCNT0 field is used for the endpoint data transfer count when the endpoint is configured as a single-buffering transfer type.</p>

USB Endpoint 4~7 Configuration Register - USBE_nCFGR, n=4~7

This register specifies the Endpoint 4~7 configurations.

Offset: 0x074 (n=4), 0x088 (n=5), 0x09C (n=6), 0x0B0 (n=7)

Reset value: 0x1000_03FF

	31	30	29	28	27	26	25	24
Type/Reset	EPEN	Reserved	EPTYPE	EPDIR		EPADR		
	RW 0		RW 0	RW 1	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
Type/Reset	SDBS		Reserved		EPLEN			
	RW 0				RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
Type/Reset			EPLEN			EPBUFA		
	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 1	RW 1
	7	6	5	4	3	2	1	0
Type/Reset			EPBUFA					
	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1

Bits	Field	Descriptions
[31]	EPEN	Enable Control 0: Disable the endpoint n 1: Enable the endpoint n
[29]	EPTYPE	Transfer Type 0: Interrupt or Bulk transfer type 1: Isochronous transfer type
[28]	EPDIR	Transfer Direction 0: OUT 1: IN
[27:24]	EPADR	Endpoint Address The EPADR field can be configured by the application software to specify the address of endpoint n. It is important to note that this EPADR field should not be set to 0, otherwise, the endpoint n will be disabled.
[23]	SDBS	Single-Buffering or Double-Buffering Selection 0: Single-buffering 1: Double-buffering If SDBS bit is set to 1, the endpoint buffer size is twice that of the EPLEN value: - Endpoint Buffer 0 start address is EPBUFA - Endpoint Buffer 1 start address is (EPBUFA + EPLEN)
[19:10]	EPLEN	Buffer Length This field is used to specify the endpoint n data packet size whose field value must be word-aligned to a 4-byte boundary. Note that the endpoint will be disabled if the LEN value is assigned to 0.
[9:0]	EPBUFA	Buffer Address This field is used to specify the endpoint n data buffer start address which ranges from 0x008 to 0x3FC in the EP-SRAM which has a capacity of 1024 bytes where the endpoint transfer data is stored. Note that the buffer start address value must be a multiple of 4.

25 Peripheral Direct Memory Access (PDMA)

Introduction

The Peripheral Direct Memory Access circuitry, PDMA, provides 8 unidirectional channels for dedicated peripherals to implement the peripheral-to-memory and memory-to-peripheral data transfer. The memory-to-memory data transfer such as the FLASH-to-SRAM or SRAM-to-SRAM type is also supported and requested by the application program. Each PDMA channel configuration is independent. The PDMA channel transfer is split into multiple block transactions and the size of a block is equal to the block length multiplied by the data width.

Features

- 8 unidirectional PDMA channels
- Memory-to-peripheral, peripheral-to-memory and memory-to-memory data transfer
- 8-bit, 16-bit and 32-bit width data transfer
- Software and hardware requested data transfer with configurable channel priority
- Linear, circular and non-increment address modes
- 4 transfer event flags - Transfer complete, Half Transfer, Block End and Transfer Error
- Auto-Reload function

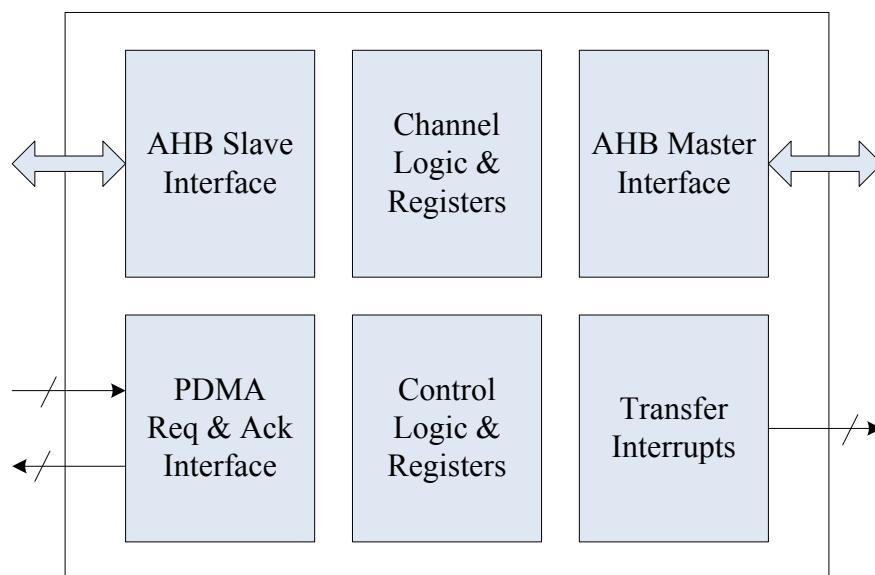


Figure 167. PDMA Block Diagram

Functional Descriptions

AHB Master

The PDMA is an AHB master connected to other AHB peripherals such as the FLASH memory, the SRAM memory and the AHB-to-APB bridges through the bus-matrix. The Cortex-M3 and PDMA can access different AHB slaves at the same time via the bus-matrix.

PDMA Channel

There are 8 unidirectional PDMA channels used to support data transfer between the peripherals and the memory. The configuration and operation of each PDMA channel is independent. For a bidirectional transfer application, two PDMA channels are required. Each PDMA channel is designed to support the dedicated multiple peripherals with the same registers. Therefore, one PDMA channel only can service one peripheral at the same time. The related registers of the PDMA channel are limited to be accessed with 32-bit operations, otherwise a system hard fault event will occur.

PDMA Request Mapping

The multiple requests from the peripherals (ADC, SPI0, I²C, USART and so on) are simply logically ANDed before entering the PDMA, that means that only one request must be enabled at a time in each PDMA channel. Refer to Figure 168: PDMA request mapping architecture and detail peripheral IP requests mapping table is show as the Table 66. The peripheral DMA requests can be independently activated/de-activated by programming the DMA control bit in the registers of the corresponding peripheral.

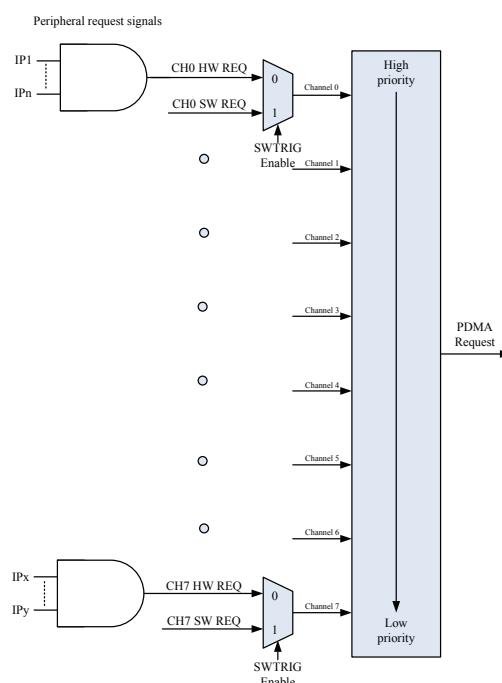


Figure 168. PDMA request mapping architecture

Table 66. PDMA Channel Assignments

IP (x=0, 1)	PDMA Channel Number							
	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7
ADC	ADC							
SPIx	SPI0_RX	SPI0_TX			SPI1_RX	SPI1_TX		
USARTx			USR0_RX	USR0_TX			USR1_TX	USR1_RX
UARTx	UR0_RX	UR0_TX			UR1_RX	UR1_TX		
SCI							SCI_RX	SCI_TX
I2Cx			I2C0_RX		I2C0_TX		I2C1_RX	I2C1_TX
MCTMx	MT0_CH0 MT0_TRIG	MT1_CH0 MT1_CH1 MT1_CH2	MT0_CH3 MT1_UEV1	MT0_CH2 MT1_CH1	MT0_UEV1 MT1_CH3	MT1_UEV2	MT0_UEV2 MT1_TRIG	
GPTMx	GT0_CH1 GT0_CH3	GT0_UEV	GT0_CH2	GT0_CH0 GT0_TRIG	GT1_CH0	GT1_CH1 GT1_UEV	GT1_CH2 GT1_TRIG	GT1_CH3
I ² S			I2S_RX	I2S_TX				

Channel transfer

A PDMA channel transfer is split into multiple block transactions with PDMA arbitration occurring at the end of each block transaction. Although these 8 channel transfers can all be activated, there is only one block transaction being transferred through the bus at a time. The channel transfer sequence depends upon the channel priority setting of each PDMA channel. The total transfer size is calculated from the block transaction count and block size. The block size is equal to the product of the block length and data bit width. For an efficient transfer, it is recommended that the block length is set as a multiple of 4.

Channel Priority

The PDMA provides four priority levels, known as very high, high, medium and low, which can be configured by the application software. The PDMA also provides two methods to determine the channel priority. One is determined by application software configuration and the other is determined by the fixed hardware channel number. The PDMA arbitration processor will first check the software configuring channel priority level used to request the PDMA to provide the data transfer services. If more than one channel has the same priority, the channel with a smaller channel number will have priority over one with a larger channel number after arbitration.

Note that the highest priority channel will not occupy the PDMA service all the time when other lower priority channel requests are pending. The highest priority channel will be skipped for one block transaction time duration after one block transaction is complete. Then a block transaction requested by the second priority channel will be performed. After a block transaction of the second priority channel is complete, the PDMA arbitration processor will re-check all of the requested channel priority with the exception of the second priority channel since the second priority channel will be excluded after the end of a block transaction. Therefore, a block data transaction of the higher priority channel will be serviced and this channel will be excluded from the priority arbitration at the end of the block transaction. The PDMA will keep transferring the data using the method described above until all of the requested channel data transfer is complete. Refer to the accompanying figure for an example which shows the PDMA channel arbitration and scheduling.

Channel 0: priority=very high, block count=2, block length=2
 Channel 1: priority=high, block count=3, block length=4
 Channel 2: priority=low, block count=3, block length=6
 Priority : CH0 > CH1 > CH2

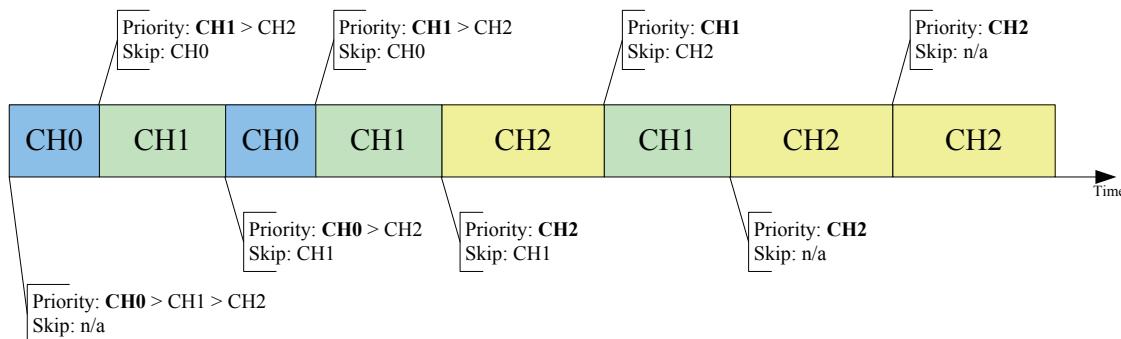


Figure 169. PDMA Channel Arbitration and Scheduling Example

Transfer Request

For a peripheral-to-memory or memory-to-peripheral transfer, one peripheral hardware request will trigger one block transaction of the dedicated PDMA channel. However, a complete data transfer of the relevant dedicated PDMA channel will be triggered when a software request occurs. It is recommended that the PDMA channel is configured to have a lower priority level and a smaller block length which is requested by the software for memory-to-memory data copy applications.

Address Mode

The PDMA provides three kinds of address modes which are the linear address, circular address and fixed address modes. These different address modes are used to support different kinds of source and destination address arrangements. The following table shows the detailed address mode combinations.

Table 67. PDMA Address Modes

Source Address Mode	Destination Address Mode
Linear Increment / Decrement Address	Linear Increment / Decrement Address
Linear Increment / Decrement Address	Circular Increment / Decrement Address
Linear Increment / Decrement Address	Fixed Address
Circular Increment / Decrement Address	Linear Increment / Decrement Address
Circular Increment / Decrement Address	Circular Increment / Decrement Address
Fixed Address	Linear Increment / Decrement Address
Fixed Address	Fixed Address

Linear Address Mode

After data is transferred, the current address will be increased or decreased by 1, 2 or 4 depending upon the data bit width setting.

Circular Address Mode

After data is transferred, the current address will be increased or decreased by 1, 2 or 4 depending upon the data bit width setting. When a block transaction is complete, the current address is loaded with the configured start address.

Fixed Address Mode

After data is transferred, the current address remains unchanged.

Auto-Reload

When the auto-reload control bit, AUTORLn, in the PDMA channel n control register named PDMACHnCR is set, both the channel n current address stored in the PDMACHnCADR register and the channel n current transfer size in the PDMACHnCTSR register will be automatically reloaded with the corresponding start value after the current PDMA channel data transfer has totally completed. The channel n will still be activated and the next relative PDMA request can be serviced without any re-configuration using the application software.

Transfer Interrupt

There are five transfer events during which the interrupts can be asserted for each PDMA channel. These are the block transaction end (BE), half-transfer (HT), transfer complete (TC), transfer error (TE) and global transfer event (GE). Setting the corresponding control bits in the PDMA interrupt enable register named PDMAIER will enable the relevant interrupt events. The global interrupt event, GE, will be generated if any of the four interrupt events including the BE, HT, TC or TE occurs. Clearing the BE, HT, TC or TE event flags will also clear the GE flag. Clearing the GE flag will automatically clear all other event flags. The TE interrupt event will occur when the PDMA accesses a system reserved address space or the PDMA receives a request but when the corresponding transfer size setting is equal to zero.

Register Map

The following table shows the PDMA registers and the reset values.

Table 68. PDMA Register Map

Register	Offset	Description	Reset Value
PDMA Base Address = 0x4009_0000			
PDMA Channel 0 Registers			
PDMACH0CR	0x000	PDMA Channel 0 Control Register	0x0000_0000
PDMACH0SADR	0x004	PDMA Channel 0 Source Address Register	0x0000_0000
PDMACH0DADR	0x008	PDMA Channel 0 Destination Address Register	0x0000_0000
PDMACH0CADR	0x00C	PDMA Channel 0 Current Address Register	0x0000_0000
PDMACH0TSR	0x010	PDMA Channel 0 Transfer Size Register	0x0000_0000
PDMACH0CTSR	0x014	PDMA Channel 0 Current Transfer Size Register	0x0000_0000
PDMA Channel 1 Registers			
PDMACH1CR	0x018	PDMA Channel 1 Control Register	0x0000_0000
PDMACH1SADR	0x01C	PDMA Channel 1 Source Address Register	0x0000_0000
PDMACH1DADR	0x020	PDMA Channel 1 Destination Address Register	0x0000_0000
PDMACH1CADR	0x024	PDMA Channel 1 Current Address Register	0x0000_0000
PDMACH1TSR	0x028	PDMA Channel 1 Transfer Size Register	0x0000_0000
PDMACH1CTSR	0x02C	PDMA Channel 1 Current Transfer Size Register	0x0000_0000
PDMA Channel 2 Registers			
PDMACH2CR	0x030	PDMA Channel 2 Control Register	0x0000_0000
PDMACH2SADR	0x034	PDMA Channel 2 Source Address Register	0x0000_0000
PDMACH2DADR	0x038	PDMA Channel 2 Destination Address Register	0x0000_0000
PDMACH2CADR	0x03C	PDMA Channel 2 Current Address Register	0x0000_0000
PDMACH2TSR	0x040	PDMA Channel 2 Transfer Size Register	0x0000_0000
PDMACH2CTSR	0x044	PDMA Channel 2 Current Transfer Size Register	0x0000_0000
PDMA Channel 3 Registers			
PDMACH3CR	0x048	PDMA Channel 3 Control Register	0x0000_0000
PDMACH3SADR	0x04C	PDMA Channel 3 Source Address Register	0x0000_0000
PDMACH3DADR	0x050	PDMA Channel 3 Destination Address Register	0x0000_0000
PDMACH3CADR	0x054	PDMA Channel 3 Current Address Register	0x0000_0000
PDMACH3TSR	0x058	PDMA Channel 3 Transfer Size Register	0x0000_0000
PDMACH3CTSR	0x05C	PDMA Channel 3 Current Transfer Size Register	0x0000_0000
PDMA Channel 4 Registers			
PDMACH4CR	0x060	PDMA Channel 4 Control Register	0x0000_0000
PDMACH4SADR	0x064	PDMA Channel 4 Source Address Register	0x0000_0000
PDMACH4DADR	0x068	PDMA Channel 4 Destination Address Register	0x0000_0000
PDMACH4CADR	0x06C	PDMA Channel 4 Current Address Register	0x0000_0000
PDMACH4TSR	0x070	PDMA Channel 4 Transfer Size Register	0x0000_0000
PDMACH4CTSR	0x074	PDMA Channel 4 Current Transfer Size Register	0x0000_0000

Register	Offset	Description	Reset Value
PDMA Channel 5 Registers			
PDMACH5CR	0x078	PDMA Channel 5 Control Register	0x0000_0000
PDMACH5SADR	0x07C	PDMA Channel 5 Source Address Register	0x0000_0000
PDMACH5DADR	0x080	PDMA Channel 5 Destination Address Register	0x0000_0000
PDMACH5CADR	0x084	PDMA Channel 5 Current Address Register	0x0000_0000
PDMACH5TSR	0x088	PDMA Channel 5 Transfer Size Register	0x0000_0000
PDMACH5CTSR	0x08C	PDMA Channel 5 Current Transfer Size Register	0x0000_0000
PDMA Channel 6 Registers			
PDMACH6CR	0x090	PDMA Channel 6 Control Register	0x0000_0000
PDMACH6SADR	0x094	PDMA Channel 6 Source Address Register	0x0000_0000
PDMACH6DADR	0x098	PDMA Channel 6 Destination Address Register	0x0000_0000
PDMACH6CADR	0x09C	PDMA Channel 6 Current Address Register	0x0000_0000
PDMACH6TSR	0x0A0	PDMA Channel 6 Transfer Size Register	0x0000_0000
PDMACH6CTSR	0x0A4	PDMA Channel 6 Current Transfer Size Register	0x0000_0000
PDMA Channel 7 Registers			
PDMACH7CR	0x0A8	PDMA Channel 7 Control Register	0x0000_0000
PDMACH7SADR	0x0AC	PDMA Channel 7 Source Address Register	0x0000_0000
PDMACH7DADR	0x0B0	PDMA Channel 7 Destination Address Register	0x0000_0000
PDMACH7CADR	0x0B4	PDMA Channel 7 Current Address Register	0x0000_0000
PDMACH7TSR	0x0B8	PDMA Channel 7 Transfer Size Register	0x0000_0000
PDMACH7CTSR	0x0BC	PDMA Channel 7 Current Transfer Size Register	0x0000_0000
PDMA Global Register			
PDMAISR0	0x120	PDMA Interrupt Status Register 0	0x0000_0000
PDMAISR1	0x124	PDMA Interrupt Status Register 1	0x0000_0000
PDMAISCR0	0x128	PDMA Interrupt Status Clear Register 0	0x0000_0000
PDMAISCR1	0x12C	PDMA Interrupt Status Clear Register 1	0x0000_0000
PDMAIER0	0x130	PDMA Interrupt Enable Register 0	0x0000_0000
PDMAIER1	0x134	PDMA Interrupt Enable Register 1	0x0000_0000

Register Descriptions

PDMA Channel n Control Register – PDMACHnCR, n=0~7

This register is used to specify the PDMA channel n data transfer configuration.

Offset: 0x000 (0), 0x018 (1), 0x030 (2), 0x048 (3), 0x060 (4), 0x078 (5), 0x090 (6), 0x0A8 (7)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24	
Type/Reset	Reserved								
	23	22	21	20	19	18	17	16	
Type/Reset	Reserved								
	15	14	13	12	11	10	9	8	
Type/Reset	Reserved				AUTORLn	FIXAENn	CHnPRI		
	RW	0	RW	0	RW	0	RW	0	
Type/Reset	7	6	5	4	3	2	1	0	
	SRCAMODn	SRCAINCn	DSTAMODn	DSTAINCn	DWIDTHn		SWTRIGN	CHnEN	
Type/Reset	RW	0	RW	0	RW	0	RW	0	

Bits	Field	Descriptions
[11]	AUTORLn	<p>Channel n Auto Reload Enable Control</p> <p>0: Disable Auto Reload function 1: Enable Auto Reload function</p> <p>If this bit is set to 1 to enable the auto-reload function, the PDMACHnCADDR and PDMACHnCTSR registers will be reloaded with the relevant start value and the PDMA channel n will be activated when a transfer is complete. If this bit is cleared to 0, the PDMACHnCADDR and PDMACHnCTSR registers will remain unchanged and the PDMA channel n will be disabled after a transfer completion.</p>
[10]	FIXAENn	<p>Channel n Fixed Address Enable control</p> <p>0: Disable fixed address function in the circular address mode 1: Enable fixed address function in the circular address mode</p> <p>Note that this bit is only available when the source or destination address mode is set to be in the circular address mode. For example, the source address mode is set as in the linear address mode and the destination address mode is set as in the circular mode. If this bit is set to enable the fixed address function, then the source address mode will still be in the linear address but the destination address mode will be in the fixed address mode instead of the circular address mode.</p>
[9:8]	CHnPRI	<p>Channel n Priority</p> <p>00: Low 01: Medium 10: High 11: Very high</p> <p>The CHnPRI field is used to configure the channel priority using the application program. If there are more than one channels which have the same software configured priority level, the channel with the smaller channel number will have priority to transfer one block of data after the arbitration.</p>

Bits	Field	Descriptions
[7]	SRCAMODn	Channel n Source Address Mode selection 0: Linear address mode 1: Circular address mode In the linear address mode, the current source address field value, CSADR, in the PDMACHnCADR register can be incremented or decremented, determined by the SRCAINCn bit value during a complete transfer. In the circular address mode, the CSADR field value can be incremented or decremented which is also determined by the SRCAINCn bit value during a block transfer and will be loaded with the lower 16-bit value of the PDMACHnSADR register when a block transaction has completed.
[6]	SRCAINCn	Channel n Source Address Increment control 0: Increment 1: Decrement This bit is used to determine whether the current source address in the CSADR field is increased or decreased during a complete transfer in the linear address mode or a block transfer in the circular address mode.
[5]	DSTAMODn	Channel n Destination Address Mode selection 0: Linear address mode 1: Circular address mode In linear address mode, the current destination address field value, CDADR, in the PDMACHnCADR register can be incremented or decremented, determined by the DSTAINCn bit value during a complete transfer. In the circular address mode, the CDADR field value can be incremented or decremented which is also determined by the DSTAINCn bit value during a block transfer and will be loaded with the lower 16-bit value of the PDMACHnDADR register when a block transfer has completed.
[4]	DSTAINCn	Channel n Destination Address Increment Control 0: Increment 1: Decrement This bit is used to determine if the current destination address in the CDADR field is increased or decreased during a complete transfer in the linear address mode or a block transfer in the circular address mode.
[3:2]	DWIDTHn	Data Bit Width selection 00: 8-bit 01: 16-bit 10: 32-bit 11: Reserved The field is used to select the data bit width of the corresponding PDMA channel n.
[1]	SWTRIGn	Software Trigger control 0: No operation 1: Software triggered transfer request Setting this bit will generate a memory-to-memory software transfer request on the corresponding PDMA channel n. It is automatically cleared when a transfer has completely finished.
[0]	CHnEN	Channel n Enable control 0: Disable the PDMA channel n 1: Enable the PDMA channel n Setting this bit will enable a software or hardware transfer request on the PDMA channel n. It is automatically cleared by hardware when a transfer has completed with the auto-reload function being disabled. However, if the AUTORLn bit is set to 1 to enable the auto-reload function, this bit will remain high to enable the PDMA channel n function for the next transfer request instead of automatically being cleared by hardware after a transfer has finished.

PDMA Channel n Source Address Register – PDMACHnSADR, n=0~7

This register specifies the source address of the PDMA channel n.

Offset: 0x004 (0), 0x01C (1), 0x034 (2), 0x04C (3), 0x064 (4), 0x07C (5), 0x094 (6), 0x0AC (7)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
SADRn								
Type/Reset	RW 0							
23 22 21 20 19 18 17 16								
SADRn								
Type/Reset	RW 0							
15 14 13 12 11 10 9 8								
SADRn								
Type/Reset	RW 0							
7 6 5 4 3 2 1 0								
SADRn								
Type/Reset	RW 0							

Bits	Field	Descriptions
[31:0]	SADRn	Channel n Source Address The register is used to specify the 32-bit source address of the PDMA channel n.

PDMA Channel n Destination Address Register – PDMACHnDADR, n=0~7

This register specifies the destination address of the PDMA channel n.

Offset: 0x008 (0), 0x020 (1), 0x038 (2), 0x050 (3), 0x068 (4), 0x080 (5), 0x098 (6), 0x0B0 (7)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
DADRn								
Type/Reset	RW 0							
23 22 21 20 19 18 17 16								
DADRn								
Type/Reset	RW 0							
15 14 13 12 11 10 9 8								
DADRn								
Type/Reset	RW 0							
7 6 5 4 3 2 1 0								
DADRn								
Type/Reset	RW 0							

Bits	Field	Descriptions
[31:0]	DADRn	Channel n Destination Address The register is used to specify the 32-bit destination address of the PDMA channel n.

PDMA Channel n Current Address Register – PDMACHnCADR, n=0~7

This register is used to indicate the lower 16-bit of the PDMA channel n current source and destination address.

Offset: 0x00C (0), 0x024 (1), 0x03C (2), 0x054 (3), 0x06C (4), 0x084 (5), 0x09C (6), 0x0B4 (7)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
CSADRn[15:8]								
Type/Reset	RO 0							
23 22 21 20 19 18 17 16								
CSADRn[7:0]								
Type/Reset	RO 0							
15 14 13 12 11 10 9 8								
CDADRN[15:8]								
Type/Reset	RO 0							
7 6 5 4 3 2 1 0								
CDADRN[7:0]								
Type/Reset	RO 0							

Bits	Field	Descriptions
[31:16]	CSADRn	<p>Channel n Current Source Address</p> <p>The CSADRn field is a read only 16-bit address indicating the current address of the data being read. After the data has been read, the CSADRn field contains the next address which the data is to be read from. Writing a new value to the PDMACHnSADR register will update the CSADRn field with the lower 16-bit content of the PDMACHnSADR register rather than the complete 32-bit value in the PDMACHnSADR register. The CSADRn field will have 16-bit or 32-bit alignment according to the DWIDTHn field setting in the PDMACHnCR register.</p> <p>For example:</p> <ul style="list-style-type: none"> If the DWIDTHn field is set as 16-bit, the last bit of the CSADRn field will be 0. If the DWIDTHn field is set as 32-bit, the last 2 bits of the CSADRn field will be 0.
[15:0]	CDADRN	<p>Channel n Current Destination Address</p> <p>The CDADRN field is a read only 16-bit address indicating the current address of the data being written. After the data has been written, the CDADRN field contains the next address where the data is to be written. Writing a new value to the PDMACHnDADR register will update the CDADRN field with the lower 16-bit content of the PDMACHnDADR register rather than the whole 32-bit value in the PDMACHnDADR register. The CDADRN field will have 16-bit or 32-bit alignment according to the DWIDTHn field setting in the PDMACHnCR register.</p> <p>For example:</p> <ul style="list-style-type: none"> If the DWIDTHn field is set as 16-bit, the last bit of the CDADRN field will be 0. If the DWIDTHn field is set as 32-bit, the last 2 bits of the CDADRN field will be 0.

PDMA Channel n Transfer Size Register – PDMACHnTSR, n=0~7

This register is used to specify the block transaction count and block transaction length.

Offset: 0x010 (0), 0x028 (1), 0x040 (2), 0x058 (3), 0x070 (4), 0x088 (5), 0x0A0 (6), 0x0B8 (7)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
BLKCNTn[15:8]								
Type/Reset	RW 0							
BLKCNTn[7:0]								
Type/Reset	RW 0							
BLKLENn[15:8]								
Type/Reset	RW 0							
BLKLENn[7:0]								
Type/Reset	RW 0							

Bits	Field	Descriptions
[31:16]	BLKCNTn	Channel n Block Transaction Count BLKCNTn represents the number of block transactions for a channel n complete transfer. The capacity of a complete transfer is the product of the BLKCNTn and BLKLENn values. The maximum BLKCNTn value is 65,535.
[15:0]	BLKLENn	Channel n Block Length The BLKLENn represents the length of a data block. The data width is defined by the DWIDTHn field in the PDMACHnCR register. The maximum BLKLENn value is 65,535.

PDMA Channel n Current Transfer Size Register – PDMACHnCTSR, n=0~7

This register is used to indicate the current block transaction count and current block length.

Address: 0x014 (0), 0x02C (1), 0x044 (2), 0x05C (3), 0x074 (4), 0x08C (5), 0x0A4 (6), 0x0BC (7)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
CBLKCNTn[15:8]								
Type/Reset	RO 0							
23 22 21 20 19 18 17 16								
CBLKCNTn[7:0]								
Type/Reset	RO 0							
15 14 13 12 11 10 9 8								
CBLKLENn[15:8]								
Type/Reset	RO 0							
7 6 5 4 3 2 1 0								
CBLKLENn[7:0]								
Type/Reset	RO 0							

Bits	Field	Descriptions
[31:16]	CBLKCNTn	Channel n Current Block Count The CBLKCNTn field is a 16-bit read-only value indicating the number of data blocks that remain to be transferred. After a data block has transferred completely, the CBLKCNTn value will be decremented by 1. Writing a new value to the BLKCNTn field in the PDMACHnTSR register will update the CBLKCNTn field value.
[15:0]	CBLKLENn	Channel n Current Block Length The CBLKLENn field is a 16-bit read-only value that indicates how much data in the block remains to be transferred. After a block of data has transferred completely, the CBLKLENn field will be reloaded with the BLKLENn value. Writing a new value to the BLKLENn field in the PDMACHnTSR register will update the CBLKLENn field value.

PDMA Interrupt Status Register 0 – PDMAISR0

This register is used to indicate the corresponding interrupt status of the PDMA channel 0~5.

Offset: 0x120

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Type/Reset	Reserved		TEISTA5	TCISTA5	HTISTA5	BEISTA5	GEISTA5	TEISTA4
		RO 0						
	23	22	21	20	19	18	17	16
Type/Reset	TCISTA4	HTISTA4	BEISTA4	GEISTA4	TEISTA3	TCISTA3	HTISTA3	BEISTA3
	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	15	14	13	12	11	10	9	8
Type/Reset	GEISTA3	TEISTA2	TCISTA2	HTISTA2	BEISTA2	GEISTA2	TEISTA1	TCISTA1
	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	7	6	5	4	3	2	1	0
Type/Reset	HTISTA1	BEISTA1	GEISTA1	TEISTA0	TCISTA0	HTISTA0	BEISTA0	GEISTA0
	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0

Bits	Field	Descriptions
[29], [24], TEISTAn		Channel n Transfer Error Interrupt Status (n = 0 ~ 5) 0: No Transfer Error occurs 1: Transfer Error occurs
[19], [14], [9], [4]		This bit is set by hardware and is cleared by writing a “1” into the corresponding interrupt status clear bit in the PDMAISR0 register. A Transfer error will occur when the PDMA accesses a system reserved address space or the PDMA receives a request but when the corresponding transfer capacity is equal to zero.
[28], [23], TCISTAn		Channel n Transfer Complete Interrupt Status (n= 0 ~ 5) 0: No Transfer Completion Occurs 1: Transfer Completion Occurs
[18], [13], [8], [3]		This bit is set by hardware and is cleared by writing a “1” into the corresponding interrupt status clear bit in the PDMAISR0 register. The Transfer Completion event will occur when the PDMA has completed a data transfer task.
[27], [22], HTISTAn		Channel n Half Transfer Interrupt Status (n= 0 ~ 5) 0: No Half Transfer Event Occurs 1: Half Transfer Event Occurs
[17], [12], [7], [2]		This bit is set by hardware and is cleared by writing a “1” into the corresponding interrupt status clear bit in the PDMAISR0 register. A Half Transfer event will occur when the PDMA has completed half of the data transfer task.
[26], [21], BEISTAn		Channel n Block Transaction End Interrupt Status (n= 0 ~ 5) 0: No Block Transaction End Event Occurs 1: Block Transaction End Event Occurs
[16], [11], [6], [1]		This bit is set by hardware and is cleared by writing a “1” into the corresponding interrupt status clear bit in the PDMAISR0 register. A Block Transaction End event will occur when the PDMA completes a data block transaction task.

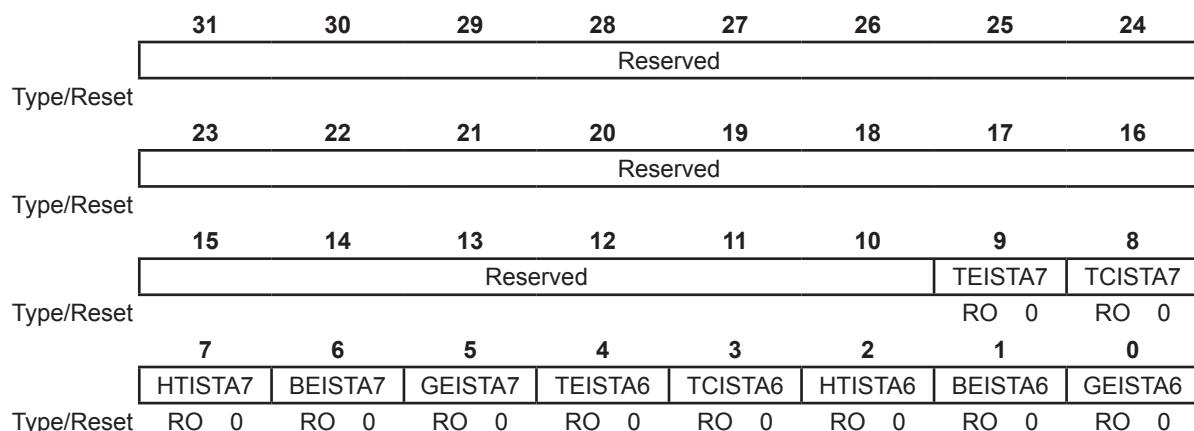
Bits	Field	Descriptions
[25], [20], [15], [10], [5], [0]	GEISTAn	Channel n Global Transfer Interrupt Status (n= 0 ~ 5) 0: No TE, TC, HT or BE event occurs 1: TE, TC, HT, or BE event occurs
		This bit is set by hardware and is cleared by writing a “1” into the corresponding interrupt status clear bit, GEICLRn, in the PDMAISR0 register. A Global Transfer Event will occur if any of the BE, HT, TC or TE events occur. Also clearing any of the BE, HT, TC or TE event interrupt flags will clear the GE interrupt flag. Note that if a “1” is written into the GEICLRn bit in the PDMAISR0 register to clear the GE interrupt flag, the BE, HT, TC and TE event interrupt flags will also be cleared to 0 together with the GE interrupt status flag.

PDMA Interrupt Status Register 1 – PDMAISR1

This register is used to indicate the corresponding interrupt status of the PDMA channel 6~7.

Offset: 0x124

Reset value: 0x0000_0000



Bits	Field	Descriptions
[9], [4]	TEISTA _m	Channel m Transfer Error Interrupt Status (m = 6 ~ 7) 0: No Transfer Error Occurs 1: Transfer Error Occurs This bit is set by hardware and is cleared by writing a “1” into the corresponding interrupt status clear bit in the PDMAISR1 register. A Transfer error will occur when the PDMA accesses a system reserved address space or the PDMA has received a request but the corresponding transfer capacity is equal to zero.
[8], [3]	TCISTA _m	Channel m Transfer Complete Interrupt Status (m = 6 ~ 7) 0: No Transfer Completion occurs 1: Transfer Completion occurs This bit is set by hardware and is cleared by writing a “1” into the corresponding interrupt status clear bit in the PDMAISR1 register. A Transfer Completion event will occur when the PDMA has completed a data transfer task.

Bits	Field	Descriptions
[7], [2]	HTISTAm	<p>Channel m Half Transfer Interrupt Status (m = 6 ~ 7)</p> <p>0: No Half Transfer Event Occurs 1: Half Transfer Event Occurs</p> <p>This bit is set by hardware and is cleared by writing a “1” into the corresponding interrupt status clear bit in the PDMAISR1 register. A Half Transfer event will occur when the PDMA has completed half of the data transfer task.</p>
[6], [1]	BEISTAm	<p>Channel m Block Transaction End Interrupt Status (m = 6 ~ 7)</p> <p>0: No Block Transaction End Event Occurs 1: Block Transaction End Event Occurs</p> <p>This bit is set by hardware and is cleared by writing a “1” into the corresponding interrupt status clear bit in the PDMAISR1 register. A Block Transaction End event will occur when the PDMA has completed a data block transaction task.</p>
[5], [0]	GEISTAm	<p>Channel m Global Transfer Event Interrupt Status (m = 6 ~ 7)</p> <p>0: No TE, TC, HT or BE Event Occurs 1: TE, TC, HT, or BE Event Occurs</p> <p>This bit is set by hardware and is cleared by writing a “1” into the corresponding interrupt status clear bit, GEICLRm, in the PDMAISR1 register. A Global Transfer Event will occur if any of the BE, HT, TC or TE events occur. Also clearing any of the BE, HT, TC or TE event interrupt flags will also clear the GE interrupt flag. Note that if a “1” is written into the GEICLRm bit in the PDMAISR1 register to clear the GE interrupt flag, the BE, HT, TC and TE event interrupt flags will also be cleared to 0 together with the GE interrupt status flag.</p>

PDMA Interrupt Status Clear Register 0 – PDMAISCR0

This register is used to clear the corresponding interrupt status bits in the PDMAISR0 Register.

Offset: 0x128

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Type/Reset		Reserved	TEICLR5	TCICLR5	HTICLR5	BEICLR5	GEICLR5	TEICLR4
	RW	0	RW	0	RW	0	RW	0
	23	22	21	20	19	18	17	16
Type/Reset	TCICLR4	HTICLR4	BEICLR4	GEICLR4	TEICLR3	TCICLR3	HTICLR3	BEICLR3
	RW	0	RW	0	RW	0	RW	0
	15	14	13	12	11	10	9	8
Type/Reset	GEICLR3	TEICLR2	TCICLR2	HTICLR2	BEICLR2	GEICLR2	TEICLR1	TCICLR1
	RW	0	RW	0	RW	0	RW	0
	7	6	5	4	3	2	1	0
Type/Reset	HTICLR1	BEICLR1	GEICLR1	TEICLR0	TCICLR0	HTICLR0	BEICLR0	GEICLR0
	RW	0	RW	0	RW	0	RW	0

Bits	Field	Descriptions
[29], [24], TEICLRn		Channel n Transfer Error Interrupt Status Clear (n = 0 ~ 5)
[19], [14], [9], [4]		0: No Operation 1: Clear the corresponding TEISTAn bit in the PDMAISR0 register Writing a “1” into the TEICLRn bit will clear the TEISTAn status bit in the PDMAISR0 register. This bit will be automatically cleared to 0 after a “1” is written.
[28], [23], TCICLRn		Channel n Transfer Complete Interrupt Status Clear (n = 0 ~ 5) 0: No Operation 1: Clear the corresponding TCISTAn bit in the PDMAISR0 register Writing a “1” into the TCICLRn bit will clear the TCISTAn status bit in the PDMAISR0 register. This bit will be automatically cleared to 0 after a “1” is written.
[27], [22], HTICLRn		Channel n Half Transfer Interrupt Status Clear (n = 0 ~ 5) 0: No Operation 1: Clear the corresponding HTISTAn bit in the PDMAISR0 register Writing a “1” into the HTICLRn bit will clear the HTISTAn status bit in the PDMAISR0 register. This bit will be automatically cleared to 0 after a “1” is written.
[17], [12], [7], [2]		
[26], [21], BEICLRn		Channel n Block Transaction End Interrupt Status Clear (n = 0 ~ 5) 0: No Operation 1: Clear the corresponding BEISTAn bit in the PDMAISR0 register Writing a “1” into the BEICLRn bit will clear the BEISTAn status bit in the PDMAISR0 register. This bit will be automatically cleared to 0 after a “1” is written.
[16], [11], [6], [1]		
[25], [20], GEICLRn		Channel n Global Transfer Event Interrupt Status Clear (n = 0 ~ 5) 0: No Operation 1: Clear the corresponding TEISTAn, TCISTAn, HTISTAn, BEISTAn, and GEISTAn bits in the PDMAISR0 register Writing a “1” into the GEICLRn bit will clear the GEISTAn status bit together with the TEISTAn, TCISTAn, HTISTAn, BEISTAn bits in the PDMAISR0 register. This bit will be automatically cleared to 0 after a “1” is written.
[15], [10], [5], [0]		

PDMA Interrupt Status Clear Register 1 – PDMAISCR1

This register is used to clear the corresponding interrupt status bits in the PDMAISR1 Register.

Offset: 0x12C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24	
Type/Reset	Reserved								
	23	22	21	20	19	18	17	16	
Type/Reset	Reserved								
	15	14	13	12	11	10	9	8	
Type/Reset	Reserved							TEICLR7 TCICLR7	
	7	6	5	4	3	2	1	0	
Type/Reset	HTICLR7	BEICLR7	GEICLR7	TEICLR6	TCICLR6	HTICLR6	BEICLR6	GEICLR6	
	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	

Bits	Field	Descriptions
[9], [4]	TEICLRm	Channel m Transfer Error Interrupt Status Clear (m = 6 ~ 7) 0: No Operation 1: Clear the corresponding TEISTAm bit in the PDMAISR1 register Writing a “1” into the TEICLRm bit will clear the TEISTAm status bit in the PDMAISR1 register. This bit will be automatically cleared to 0 after a “1” is written.
[8], [3]	TCICLRm	Channel m Transfer Complete Interrupt Status Clear (m = 6 ~ 7) 0: No Operation 1: Clear the corresponding TCISTAm bit in the PDMAISR1 register Writing a “1” into the TCICLRm bit will clear the TCISTAm status bit in the PDMAISR1 register. This bit will be automatically cleared to 0 after a “1” is written.
[7], [2]	HTICLRm	Channel m Half Transfer Interrupt Status Clear (m = 6 ~ 7) 0: No Operation 1: Clear the corresponding HTISTAm bit in the PDMAISR1 register Writing a “1” into the HTICLRm bit will clear the HTISTAm status bit in the PDMAISR1 register. This bit will be automatically cleared to 0 after a “1” is written.
[6], [1]	BEICLRm	Channel m Block Transaction End Interrupt Status Clear (m = 6 ~ 7) 0: No Operation 1: Clear the corresponding BEISTAm bit in the PDMAISR1 register Writing a “1” into the BEICLRm bit will clear the BEISTAm status bit in the PDMAISR1 register. This bit will be automatically cleared to 0 after a “1” is written.
[5], [0]	GEICLRm	Channel m Global Transfer Event Interrupt Status Clear (m = 6 ~ 7) 0: No Operation 1: Clear the corresponding TEISTAm, TCISTAm, HTISTAm, BEISTAm, and GEISTAm bits in the PDMAISR1 register Writing a “1” into the GEICLRm bit will clear the GEISTAm status bit together with the TEISTAm, TCISTAm, HTISTAm, BEISTAm bits in the PDMAISR1 register. This bit will be automatically cleared to 0 after a “1” is written.

PDMA Interrupt Enable Register 0 – PDMAIER0

This register is used to enable or disable the related interrupts of the PDMA channel 0~5.

Offset: 0x130

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Type/Reset	Reserved		TEIE5	TCIE5	HTIE5	BEIE5	GEIE5	TEIE4
	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
Type/Reset	TCIE4	HTIE4	BEIE4	GEIE4	TEIE3	TCIE3	HTIE3	BEIE3
	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
Type/Reset	GEIE3	TEIE2	TCIE2	HTIE2	BEIE2	GEIE2	TEIE1	TCIE1
	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
Type/Reset	HTIE1	BEIE1	GEIE1	TEIE0	TCIE0	HTIE0	BEIE0	GEIE0
	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[29], [24], TEIEn		Channel n Transfer Error Interrupt Enable control (n = 0 ~ 5) 0: Transfer Error interrupt is disabled 1: Transfer Error interrupt is enabled
[19], [14], [9], [4]		This bit is set and cleared by software.
[28], [23], TCIEn		Channel n Transfer Complete Interrupt Enable control (n = 0 ~ 5) 0: Transfer Completion interrupt is disabled 1: Transfer Completion interrupt is enabled
[18], [13], [8], [3]		This bit is set and cleared by software.
[27], [22], HTIEn		Channel n Half Transfer Interrupt Enable control (n = 0 ~ 5) 0: Half Transfer interrupt is disabled 1: Half Transfer interrupt is enabled
[17], [12], [7], [2]		This bit is set and cleared by software.
[26], [21], BEIEn		Channel n Block Transaction End Interrupt Enable control (n = 0 ~ 5) 0: Block Transaction End interrupt is disabled 1: Block Transaction End interrupt is enabled
[16], [11], [6], [1]		This bit is set and cleared by software.
[25], [20], GEIEn		Channel n Global Transfer Event Interrupt Enable control (n = 0 ~ 5) 0: Global Transfer Event interrupt is disabled 1: Global Transfer Event interrupt is enabled
[15], [10], [5], [0]		This bit is set and cleared by software.

PDMA Interrupt Enable Register 1 – PDMAIER1

This register is used to enable or disable the related interrupts of the PDMA channel 6~7.

Offset: 0x134

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Reserved								
Type/Reset	23	22	21	20	19	18	17	16
Reserved								
Type/Reset	15	14	13	12	11	10	9	8
Reserved							TEIE7	TCIE7
Type/Reset	7	6	5	4	3	2	1	0
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	HTIE7	BEIE7	GIE7	TEIE6	TCIE6	HTIE6	BEIE6	GEIE6

Bits	Field	Descriptions
[9], [4]	TEIEm	Channel m Transfer Error Interrupt Enable (m = 6 ~ 7) 0: Transfer Error interrupt is disabled 1: Transfer Error interrupt is enabled This bit is set and cleared by software.
[8], [3]	TCIEm	Channel m Transfer Complete Interrupt Enable (m = 6 ~ 7) 0: Transfer Completion interrupt is disabled 1: Transfer Completion interrupt is enabled This bit is set and cleared by software.
[7], [2]	HTIEm	Channel m Half Transfer Interrupt Enable (m = 6 ~ 7) 0: Half Transfer interrupt is disabled 1: Half Transfer interrupt is enabled This bit is set and cleared by software.
[6], [1]	BEIEm	Channel m Block Transaction End Interrupt Enable (m = 6 ~ 7) 0: Block Transaction End interrupt is disabled 1: Block Transaction End interrupt is enabled This bit is set and cleared by software.
[5], [0]	GEIEm	Channel m Global Transfer Event Interrupt Enable (m = 6 ~ 7) 0: Global Transfer Event interrupt is disabled 1: Global Transfer Event interrupt is enabled This bit is set and cleared by software.

26 Extend Bus Interface (EBI)

Introduction

The external bus interface is able to access external parallel interface devices such as SRAM, Flash and LCD modules. The interface is memory mapped into the internal address bus of the Cortex-M3. The data and address lines can be multiplexed in order to reduce the number of pins required to connect to external devices. The bus read/write timing can be adjusted to meet the timing specifications of the external devices. Note that the interface only supports asynchronous 8 or 16-bit bus interfaces.

Features

- Programmable interface for various memory types
 - Asynchronous static random access memory - SRAM
 - Read-only memory - ROM
 - NOR Flash memory
 - 8-bit or 16-bit parallel bus CPU interface device
- Translates AHB transactions into appropriate external device protocol
- 4 memory bank regions and independent chip select control for each memory bank
- Programmable timings to support a wide range of devices
 - Programmable wait states or external asynchronous ready signal control
 - Programmable bus turnaround cycles
 - Programmable output enable and write enable cycles extension for each memory bank
 - Individual active high or low setting of interface control signal for each memory bank
- Supports page read mode
- Automatic translation when AHB transaction width and external memory interface width is different
- Write buffer to decrease stalling of the AHB write burst transactions
- Supports multiplexed and non-multiplexed address and data line configurations
 - Up to 25 address lines
 - Up to 16-bit data bus width

Functional Descriptions

An overview of the EBI module is shown in Figure 170. The EBI enables internal CPU and other bus matrix master peripherals to access external memories or devices. The EBI automatically translates the internal AHB transactions into the external device protocol. In particular, if the selected external memory is 16 or 8 bits width, then 32-bit wide transactions on the AHB are auto split into consecutive 16 or 8-bit accesses.

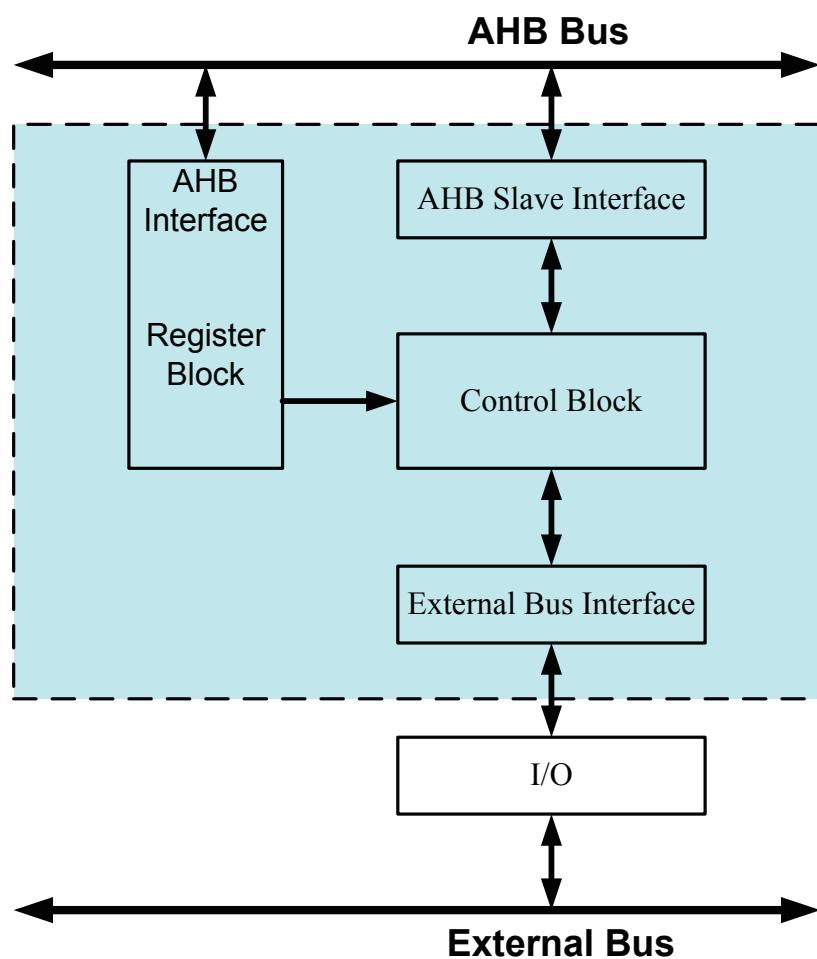


Figure 170. EBI block diagram

The EBI supports multiplexed and non-multiplexed addressing modes. The non-multiplexed addressing mode can be operated more efficiently and faster but it requires a higher number of pins. The multiplexed addressing modes are slower and require an external address latch device and a lower number of pins. The functionality of the 16 EBI_AD pins depends on what kind of the multiplexed addressing mode is used. They are used for both address and data in the multiplexed modes. Also for the non-multiplexed 8-bit address mode, both the address and data fit into these 16 EBI_AD pins. If more address bits or data bits are needed, an external latch can be used to support up to 24-bit addresses or 16-bit data in the multiplexed addressing modes using only the 16 EBI_AD pins. Furthermore, independent of the addressing mode, up to 25 non-multiplexed address lines can be enabled on the EBI_A pin connections. The detailed operation in the supported modes is presented in the following sections. The AHB clock (HCLK) is the reference clock for the EBI.

Non-multiplexed 8-bit Data 8-bit Address Mode

In this mode, 8-bit address and 8-bit data is supported. The address is located on the higher 8 bits of the EBI_AD lines and the data uses the lower 8 bits. This mode is set by programming the MODE field in the EBICR register to D8A8. Read and write timing in the 8-bit mode are shown in Figure 171 and Figure 172.

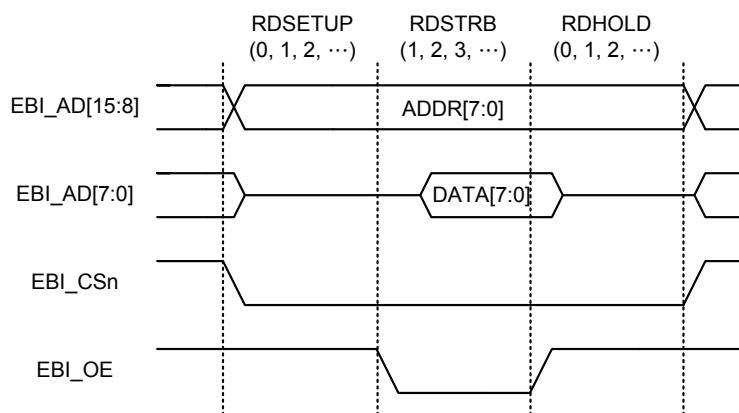


Figure 171. EBI Non-multiplexed 8-bit Data, 8-bit Address read operation

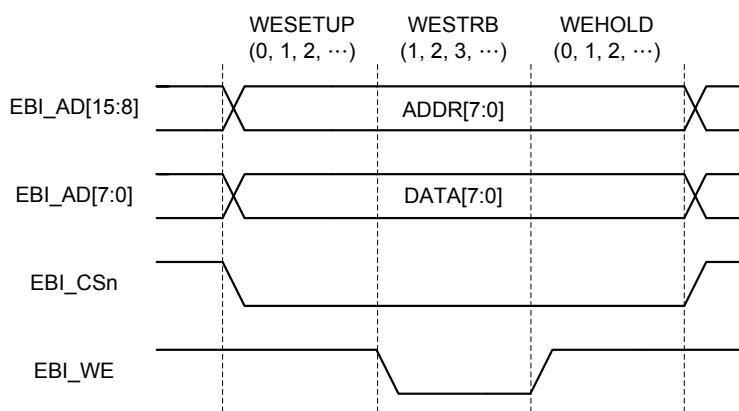


Figure 172. EBI Non-multiplexed 8-bit Data, 8-bit Address write operation

Non-multiplexed 16-bit Data N-bit Address Mode

In this non-multiplexed mode 16-bit data is provided on the 16 EBI_AD lines. The addresses are provided on the EBI_A lines. This mode is set by programming the MODE field in the EBICR register to D16. Read and write signals are shown in Figure 173 and Figure 174 for the case in which N address lines on EBI_A have been enabled.

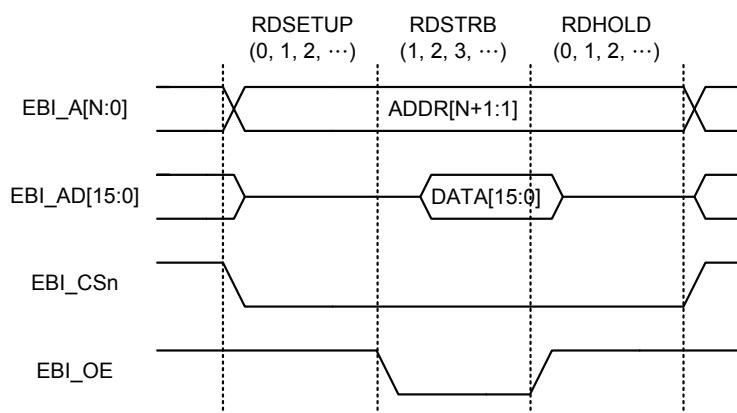


Figure 173. EBI Non-multiplexed 16-bit Data, N-bit Address read operation

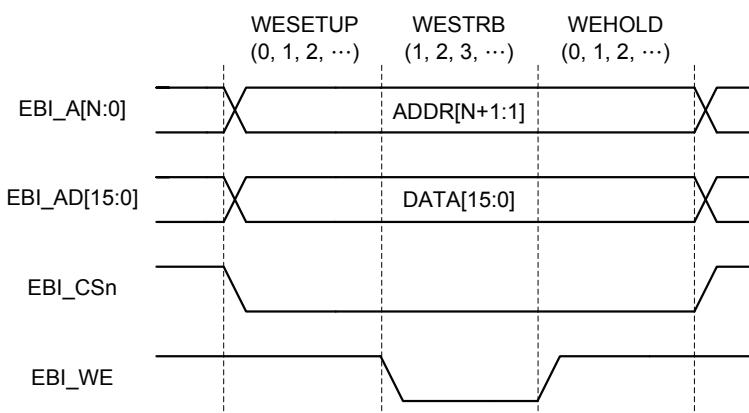


Figure 174. EBI Non-multiplexed 16-bit Data, N-bit Address write operation

Since the internal AHB address (HADDR) is a byte (8-bit) address whereas the 16-bit width of external device is addressed in words (16-bit), the address actually issued to the external device varies according to the data width as shown in the following table.

Memory width	Data address issued to the EBI
8-bit	HADDR[N:0] → EBI_A[N:0]
16-bit	HADDR[N+1:1] → EBI_A[N:0]

In case of a 16-bit external device width, the EBI will internally use HADDR[N+1:1] to generate the address EBI_A[N:0] for external device. Whatever the external memory width (16-bit or 8-bit), EBI_A[0] should be connected to external device address A[0].

Multiplexed 16-bit Data, 16-bit Address Mode

In this mode, 16-bit address and 16-bit data is supported, but the utilisation of an external latch and an extra signal EBI_ALE is required. The 16-bit address and 16-bit data bits are multiplexed on the EBI_AD pins. An EBI address latch setup diagram is shown in Figure 175 . This mode is set by programming the MODE field in the EBICR register to D16A16ALE.

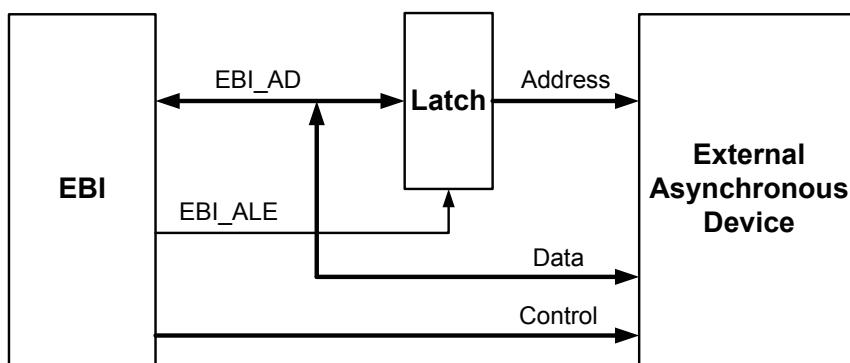


Figure 175. An EBI address latch setup diagram

At the start of the transaction the address is output on the EBI_AD lines. The external address latch is controlled by the EBI_ALE signal and stores the address. Then the data is read or written according to operation. Read and write signals are shown in Figure 176 and Figure 177.

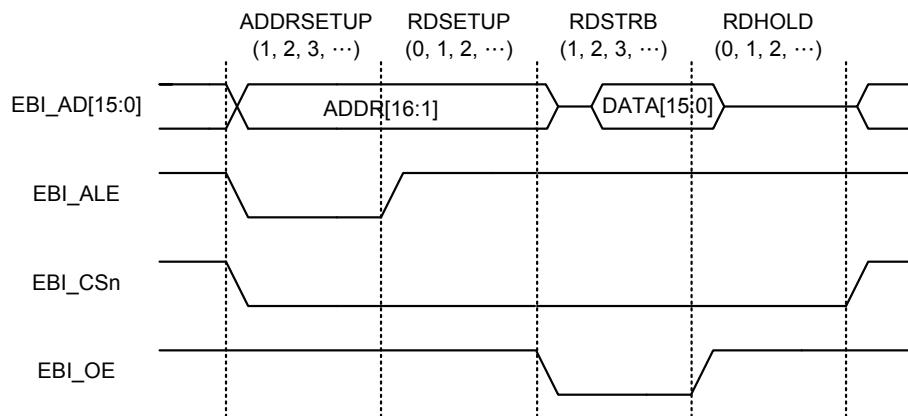


Figure 176. EBI Multiplexed 16-bit Data, 16-bit Address read operation

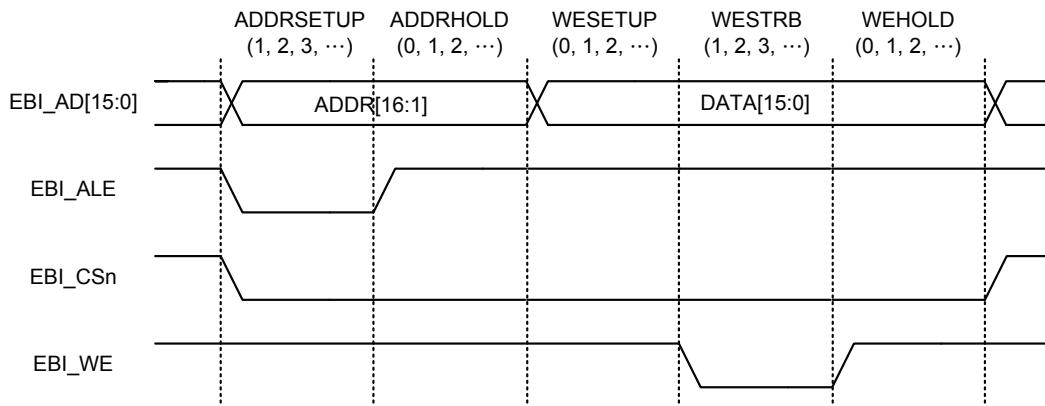


Figure 177. EBI Multiplexed 16-bit Data, 16-bit Address write operation

Multiplexed 8-bit Data, 24-bit Address Mode

This mode allows 24-bit address with 8-bit data multiplexed on the EBI_AD[15:0] lines to reduce the pins utilisation and uses the EBI_ALE signal to decode 8-bit data and 24-bit address. The upper 8 bits of the EBI_AD lines (EBI_AD[15:8]) are consecutively used for the highest 8 bits and the lowest 8 bits of the address. The lower 8 bits of the EBI_AD lines (EBI_AD[7:0]) are used for the middle 8 address bits and 8-bit data. This mode is set by programming the MODE field in the EBICR register to D8A24ALE. Read and write signals are shown in Figure 178 and Figure 179 respectively.

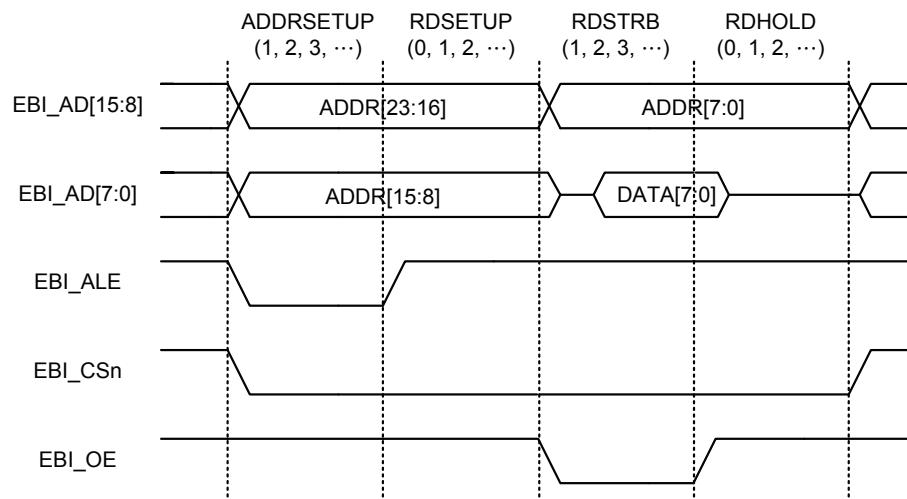


Figure 178. EBI Multiplexed 8-bit Data, 24-bit Address read operation

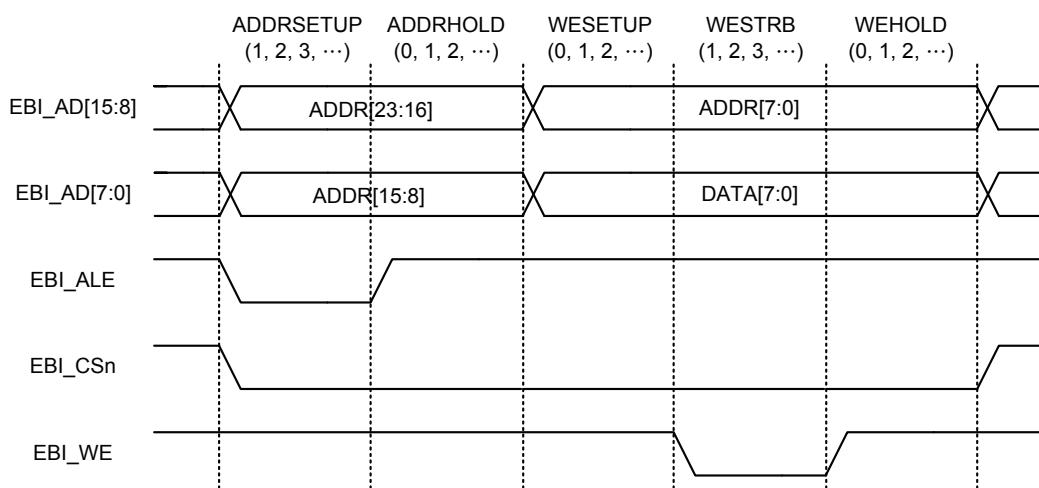


Figure 179. EBI Multiplexed 8-bit Data, 24-bit Address write operation

Page Read Operation

Page mode read operation is a performance-enhancing extension to the legacy asynchronous read transactions. In page-mode-capable devices, an initial asynchronous read access is performed and then adjacent addresses can be read quickly by simply changing the low-order address. For example, Addresses A[3:0] are used to determine the members of the 16-address page mode device. Any change in addresses A[4] or higher will stop the page read and initiate a new asynchronous read access time. Page mode takes advantage of the fact that adjacent addresses can be read faster than random addresses.

Page mode operation is enabled by setting the PAGEMODE bit in the EBIRTRn register to 1. If enabled, the RDPG field in the EBIPCR register defines the duration of an intrapage access and the PAGELEN field in the EBIPCR register defines the number of addresses members in a page. The INCHIT bit of the EBIPCR register defines whether page hits occur on any addresses member in a page or only on incremental addresses. Page mode reads can be triggered by consecutive reads resulting from wide AHB reads which are automatically translated into multiple narrow external device reads. The following figures show typical page mode read sequences for all addressing modes.

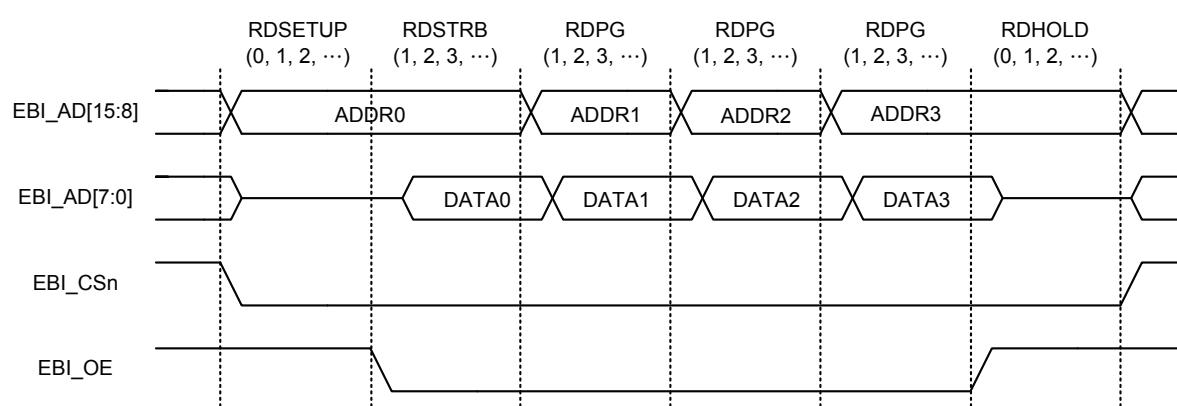


Figure 180. EBI Non-multiplexed 8-bit Data, 8-bit Address mode for page read operation

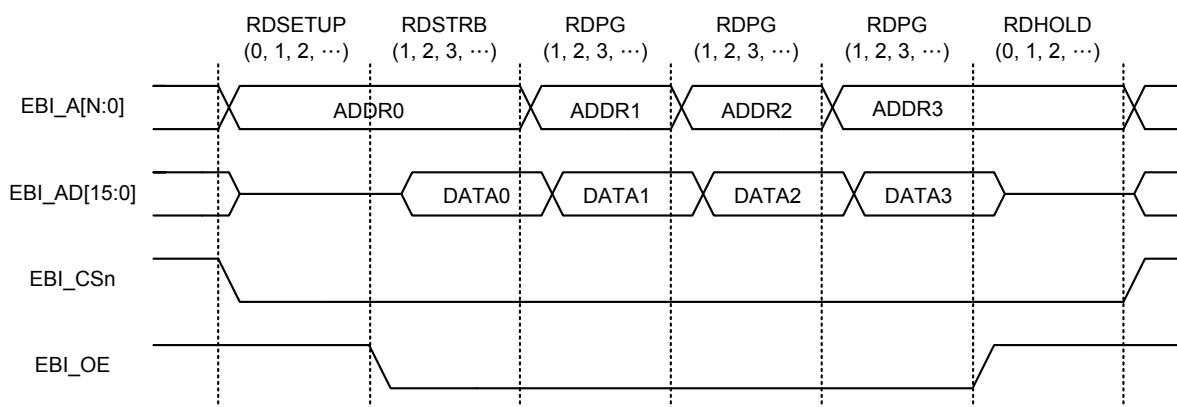


Figure 181. EBI Non-multiplexed 16-bit Data, N-bit Address mode for page read operation

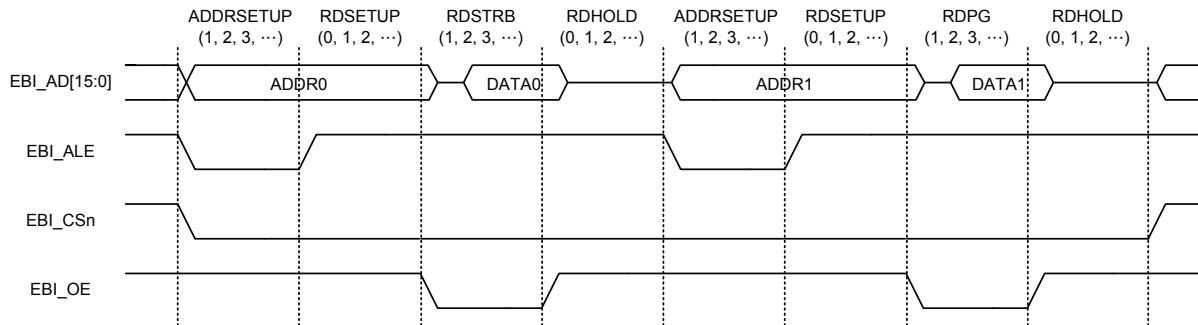


Figure 182. EBI Multiplexed 16-bit Data, 16-bit Address mode for page read operation

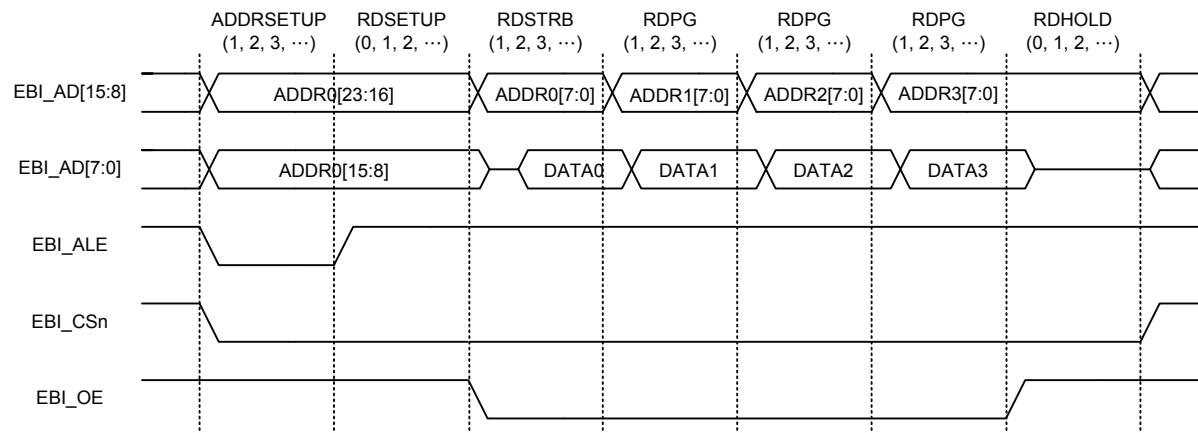


Figure 183. EBI Multiplexed 8-bit Data, 24-bit Address mode for page read operation

The PAGEOPEN field of the EBIPCR defines the maximum duration for which a page read is kept active. New read transactions which hit an open page are started with RDPG timing if the PAGEOPEN time has not been exceeded at the start of such a transaction. Page read transactions are allowed to close the page mode with the following conditions:

- The PAGEOPEN time is exceeded during the continuous read transactions
- The EBI transactions insert a write or a non-intrapage read
- The lack of a new EBI transaction

Figure 184 shows an example in which only ADDR1 benefits from intrapage timing because an unrelated address of AHB transfer is inserted and causes late arrival of ADDR2. The page is considered closed and ADDR2 can therefore not benefit from intrapage timing and it regards it as a normal read access.

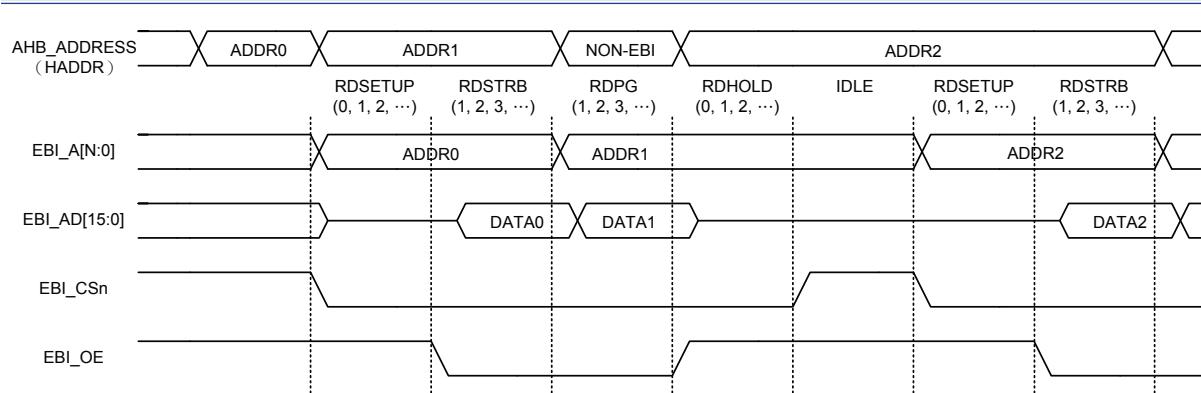


Figure 184. EBI page close example

Write Buffer and EBI Status

The EBI has a 32-bit wide write buffer. The write buffer can be used to limit stalling of a AHB write burst transaction which comes from the Cortex-M3 or PDMA to a potentially slow external device.

The EBIBUSY status bit in the EBISR register indicates whether an AHB transaction is still active in the EBI or not. When performing an AHB read or write, the EBIBUSY bit stays 1 until the required transaction(s) with the external device has finished.

Bus Turn-around and Idle Cycles

The EBI_AD lines can be driven by either the EBI or the external device depending on the cycle state of EBI bus. The RDHOLD timing parameter is for the bus turn-around time and should be programmed to ensure enough time for the characteristics of an external device. The default setting for the EBI is to insert an IDLE cycle between EBI transactions to the same bank. The IDLE cycle insertion is shown for two back-to-back read transactions in Figure 185. For cases where the IDLE state can also provide the required bus turn-around time, the RDHOLD parameter can be programmed to 0. For increased EBI access performance, the automatic IDLE state insertion can be disabled by setting the NOIDLEn bits in the EBICR register to 1. This example is shown in Figure 186 for two back-to-back reads in a non-multiplexed address mode.

An IDLE cycle will automatically be inserted for the following cases:

- Between two external device transactions to the same bank when the NOIDLEn bit is 0.
- Between two external device transactions to different banks.
- Between a read and a subsequent write on the EBI_AD lines.
- When no request for an external transaction is available in the EBI.

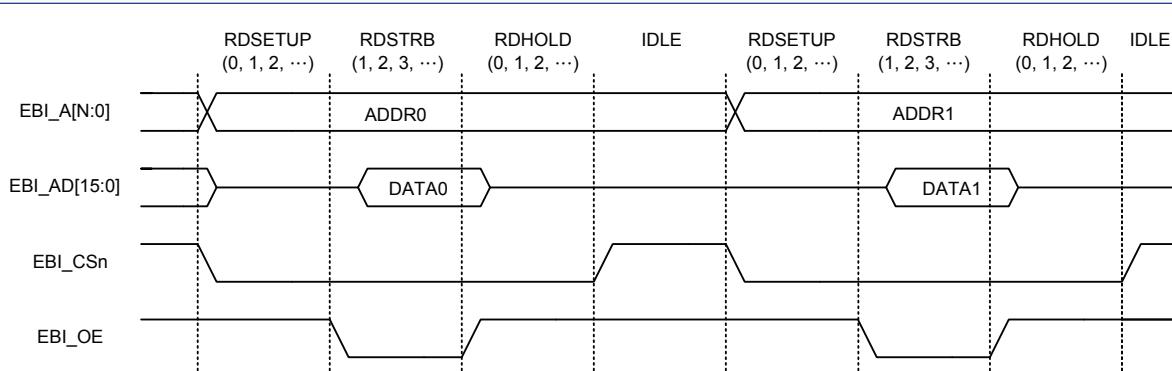


Figure 185. EBI inserts an IDLE cycle between transactions in the same bank (NOIDLE = 0)

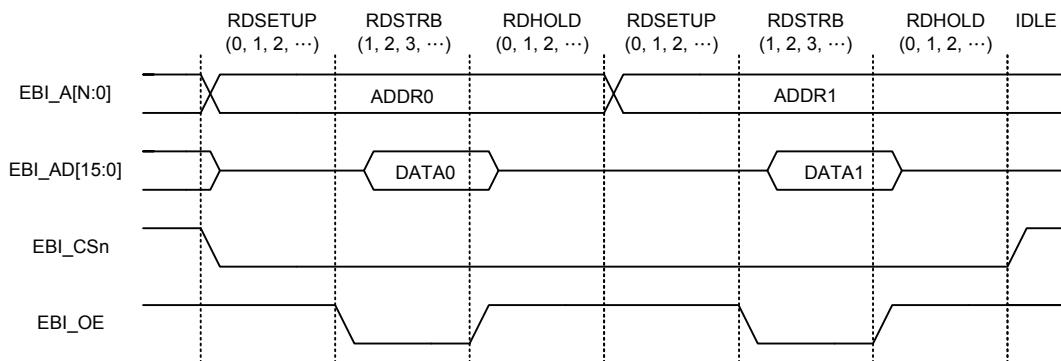


Figure 186. EBI de-asserts an IDLE cycle between transactions in the same bank (NOIDLE = 1)

AHB Transaction Width Conversion

The mapping of AHB transactions to an external device depends on the data width of the external device and whether the byte lanes of the external device are supported or not. The Table 69 shows the EBI mapping of AHB transactions to external device transactions. The EBI will automatically translate the different AHB transaction width to external device transactions which matches the external bus capabilities of the device.

- If the AHB master (CPU or PDMA) transaction width is larger than the external bus transaction width. The EBI will split and translate the AHB transaction into consecutive multiple external transactions which have consecutively incrementing the address and start with the least significant data from AHB transaction.
- If the AHB master (CPU or PDMA) transaction width is smaller than the external bus transaction width. The EBI behavior depends on whether the byte lanes are available or not. Reads either use byte lanes to select the required data when it is available, or read according to the full data bus width of the external device and ignore the superfluous data when a byte lane is not available. Writes either use a byte lane to select the required data when it is available, or EBI automatically perform a read-modify-write sequence when a byte lane is not available.

Table 69. The EBI maps the AHB transactions width to external device transactions

AHB Transaction	8-bit External Device Transaction	16-bit External Device Transaction (with byte lanes)	16-bit External Device Transaction (without byte lanes)
8-bit read	1 × 8-bit read	1 × 8-bit read (using byte lane)	1 × 16-bit read (EBI ignore the superfluous data)
16-bit read	2 × 8-bit read	1 × 16-bit read	1 × 16-bit read
32-bit read	4 × 8-bit read	2 × 16-bit read	2 × 16-bit read
8-bit write	1 × 8-bit write	1 × 8-bit write (using byte lane)	1 × 16-bit read; 1 × 16-bit write (EBI read-modify-write)
16-bit write	2 × 8-bit write	1 × 16-bit write	1 × 16-bit write
32-bit write	4 × 8-bit write	2 × 16-bit write	2 × 16-bit write

Table 70. The EBI maps the AHB transactions width to external device transactions width using byte lane EBI_BL[1:0]

External Bus Width	Access from AHB Master		Access to External Bus Interface (EBI)			
	Access type	Address HADDR[1:0] ^{Note}	Access split	Output value from EBI_A[1:0]	Valid data at EBI_AD[15:0]	Output value from EBI_BL[1:0]
8-bit	Byte (8-bit)	0b00	No split	0b00	EBI_AD[7:0]	0b10
		0b01	No split	0b01		
		0b10	No split	0b10		
		0b11	No split	0b11		
	Half-word (16-bit)	0b00	1/2 access	0b00		
			2/2 access	0b01		
	Half-word (16-bit)	0b10	1/2 access	0b10		
			2/2 access	0b11		
	Word (32-bit)	0b00	1/4 access	0b00		
			2/4 access	0b01		
			3/4 access	0b10		
			4/4 access	0b11		
16-bit	Byte (8-bit)	0b00	No split	0bx0	EBI_AD[7:0]	0b10
		0b01	No split	0bx0	EBI_AD[15:8]	0b01
		0b10	No split	0bx1	EBI_AD[7:0]	0b10
		0b11	No split	0bx1	EBI_AD[15:8]	0b01
	Half-word (16-bit)	0b00	No split	0bx0	EBI_AD[15:0]	0b00
		0b10	No split	0bx1	EBI_AD[15:0]	0b00
	Word (32-bit)	0b00	1/2 access	0bx0	EBI_AD[15:0]	0b00
			2/2 access	0bx1	EBI_AD[15:0]	0b00

Note: 1. HADDR is AHB bus address input.
2. Byte lane polarity is low active in this table.

EBI Bank Access

The EBI is split into 4 different address regions and each owns an individual EBI_CS_n line. When accessing one of the memory regions, the corresponding EBI_CS_n line is asserted. This way up to 4 separate devices can share the EBI lines and be identified by the EBI_CS_n line. Each bank can individually be enabled or disabled in the EBICR register. And each bank can individually define the external device behavior, including for example data width, timing definitions, page mode operation, and pin polarities. The data space of each bank can be accessed up to 64MB and is shown as Figure 187. The EBI regions address starts at 0x60000000 in the memory map and can also be used for code execution. When running code via EBI regions starting at this address, the Cortex-M3 uses the System bus interface to fetch instructions. This will result in reduced performance because the Cortex-M3 accesses stack, SRAM and peripherals also use the System bus interface.

In order to enhance efficiently for running code via the EBI, bank 0 of the EBI is also mapped into the code space at address 0x1B000000. When running code from this space, the Cortex-M3 fetches instructions through the I/D-Code bus interface, leaving the system bus interface free for data access. The instructions fetched via the I/D-Code bus interface can increase performance.

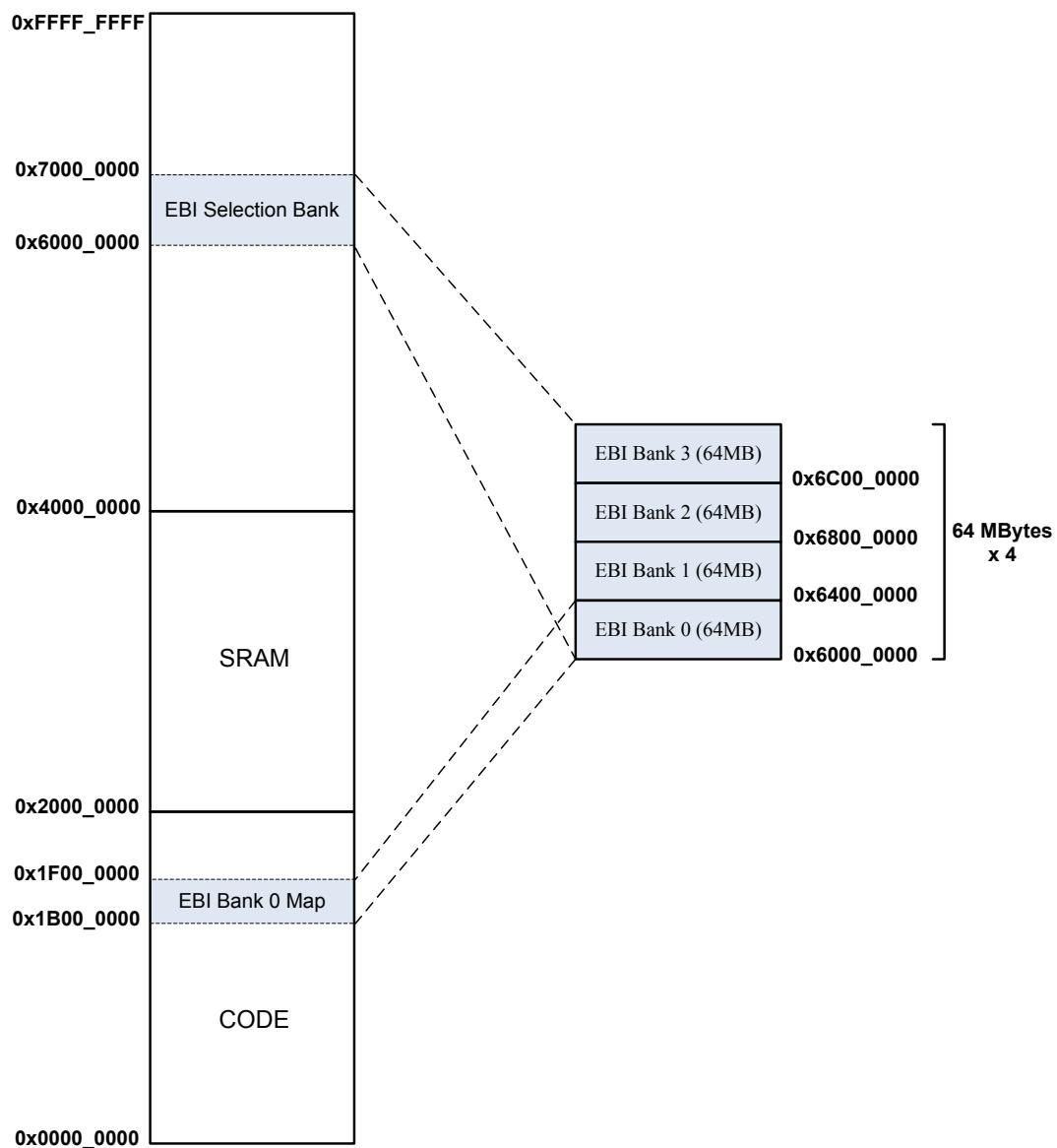


Figure 187. EBI bank memory map

EBI Ready

Some external devices are able to indicate that they have not finished their write or read operations by asserting the wait signal. The EBI_ARDY input signal of the EBI is used to extend the read or write cycles for slow external devices when it is enabled by setting the ARDYEN bit in the EBICR register. EBI_ARDY can be configured by the polarity of this signal with the RDYPOL bit in the EBIPR register. If the RDYPOL bit is set to active low, then the read or write cycle is extended while the EBI_ARDY line is kept high. It also provides a timeout check to prevent a system lock up condition in case where the external device does not de-assert the EBI_ARDY signal. It will generate a bus asynchronous ready time-out interrupt if EBI_ARDY is not deasserted within the timeout period. This timeout period has a default value of 32 HLCK clock cycles. Its functionality can be disabled by setting the ARDYTDIS bit in the EBICR register. Note that each memory bank can individually set its wait behavior definition.

PDMA Request

The EBI only supports using a software trigger for active PDMA service.

Register Map

The following table shows the EBI register and reset value.

Table 71. Register map of EBI

Register	Offset	Description	Reset Value
EBI Base Address = 0x4009_8000			
EBICR	0x000	EBI Control Register	0x0000_0000
EBIPCR	0x004	EBI Page Control Register	0x0000_0F00
EBISR	0x008	EBI Status Register	0x0000_0010
EBIATR0	0x010	EBI Address Timing Register 0	0x0000_0F0F
EBIRTR0	0x014	EBI Read Timing Register 0	0x000F_3F0F
EBIWTR0	0x018	EBI Write Timing Register 0	0x000F_3F0F
EBIPR0	0x01C	EBI Parity Register 0	0x0000_0000
EBIATR1	0x020	EBI Address Timing Register 1	0x0000_0F0F
EBIRTR1	0x024	EBI Read Timing Register 1	0x000F_3F0F
EBIWTR1	0x028	EBI Write Timing Register 1	0x000F_3F0F
EBIPR1	0x02C	EBI Parity Register 1	0x0000_0000
EBIATR2	0x030	EBI Address Timing Register 2	0x0000_0F0F
EBIRTR2	0x034	EBI Read Timing Register 2	0x000F_3F0F
EBIWTR2	0x038	EBI Write Timing Register 2	0x000F_3F0F
EBIPR2	0x03C	EBI Parity Register 2	0x0000_0000
EBIATR3	0x040	EBI Address Timing Register 3	0x0000_0F0F
EBIRTR3	0x044	EBI Read Timing Register 3	0x000F_3F0F
EBIWTR3	0x048	EBI Write Timing Register 3	0x000F_3F0F
EBIPR3	0x04C	EBI Parity Register 3	0x0000_0000
EBIENR	0x050	EBI Interrupt Enable Register	0x0000_0000
EBIIFR	0x054	EBI Interrupt Flag Register	0x0000_0000
EBIIFCR	0x058	EBI Interrupt Clear Register	0x0000_0000

Register Descriptions

EBI Control Register – EBICR

This register specifies the control setting for EBI bank.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Type/Reset	RW 0	RW 0						
	23	22	21	20	19	18	17	16
	ARDYTDIS3	ARDYEN3	ARDYTDIS2	ARDYEN2	ARDYTDIS1	ARDYEN1	ARDYTDIS0	ARDYEN0
Type/Reset	RW 0	RW 0						
	15	14	13	12	11	10	9	8
	NOIDLE3	NOIDLE2	NOIDLE1	NOIDLE0	BANKEN3	BANKEN2	BANKEN1	BANKEN0
Type/Reset	RW 0	RW 0						
	7	6	5	4	3	2	1	0
	Mode3		Mode2		Mode1		Mode0	
Type/Reset	RW 0	RW 0						

Bits	Field	Descriptions
[31:28]	IDLET	IDLE Time Sets the number of cycles between EBI transactions. If set to 0, one cycle is inserted by the hardware. The cycle unit is based on the HCLK clock period.
[27]	BLEN3	Byte Lane Enable 3 0: Disable EBI byte lane functionality 1: Enable EBI byte lane functionality Enable or disable byte lane functionality for bank 3.
[26]	BLEN2	Byte Lane Enable 2 0: Disable EBI byte lane functionality 1: Enable EBI byte lane functionality Enable or disable byte lane functionality for bank 2.
[25]	BLEN1	Byte Lane Enable 1 0: Disable EBI byte lane functionality 1: Enable EBI byte lane functionality Enable or disable byte lane functionality for bank 1.
[24]	BLEN0	Byte Lane Enable 0 0: Disable EBI byte lane functionality 1: Enable EBI byte lane functionality Enable or disable byte lane functionality for bank 0.
[23]	ARDYTDIS3	Asynchronous Ready Timeout Disable 3 0: Enable EBI asynchronous ready timeout control functionality 1: Disable EBI asynchronous ready timeout control functionality Enable or disable the asynchronous ready timeout functionality for bank 3. The default asynchronous ready timeout period is 32 HCLK clock cycles and cannot be changed.

Bits	Field	Descriptions
[22]	ARDYEN3	Asynchronous Ready Enable 3 0: Disable EBI asynchronous ready control functionality 1: Enable EBI asynchronous ready control functionality Enable or disable the asynchronous ready functionality for bank 3.
[21]	ARDYTDIS2	Asynchronous Ready Timeout Disable 2 0: Enable EBI asynchronous ready timeout control functionality 1: Disable EBI asynchronous ready timeout control functionality Enable or disable the asynchronous ready timeout functionality for bank 2. The default asynchronous ready timeout period is 32 HCLK clock cycles and cannot be changed.
[20]	ARDYEN2	Asynchronous Ready Enable 2 0: Disable EBI asynchronous ready control functionality 1: Enable EBI asynchronous ready control functionality Enable or disable the asynchronous ready functionality for bank 2.
[19]	ARDYTDIS1	Asynchronous Ready Timeout Disable 1 0: Enable EBI asynchronous ready timeout control functionality 1: Disable EBI asynchronous ready timeout control functionality Enable or disable the asynchronous ready timeout functionality for bank 1. The default asynchronous ready timeout period is 32 HCLK clock cycles and cannot be changed.
[18]	ARDYEN1	Asynchronous Ready Enable 1 0: Disable EBI asynchronous ready control functionality 1: Enable EBI asynchronous ready control functionality Enable or disable the asynchronous ready functionality for bank 1.
[17]	ARDYTDIS0	Asynchronous Ready Timeout Disable 0 0: Enable EBI asynchronous ready timeout control functionality 1: Disable EBI asynchronous ready timeout control functionality Enable or disable the asynchronous ready timeout functionality for bank 0. The default asynchronous ready timeout period is 32 HCLK clock cycles and cannot be changed.
[16]	ARDYEN0	Asynchronous Ready Enable 0 0: Disable EBI asynchronous ready control functionality 1: Enable EBI asynchronous ready control functionality Enable or disable the asynchronous ready functionality for bank 0.
[15]	NOIDLE3	No IDLE 3 0: Enable IDLE state insertion 1: Disable IDLE state insertion Enable or disable the insertion of an idle state between transactions for bank 3.
[14]	NOIDLE2	No IDLE 2 0: Enable IDLE state insertion 1: Disable IDLE state insertion Enable or disable the insertion of an idle state between transactions for bank 2.
[13]	NOIDLE1	No IDLE 1 0: Enable IDLE state insertion 1: Disable IDLE state insertion Enable or disable the insertion of an idle state between transactions for bank 1.
[12]	NOIDLE0	No IDLE 0 0: Enable IDLE state insertion 1: Disable IDLE state insertion Enable or disable the insertion of an idle state between transactions for bank 0.

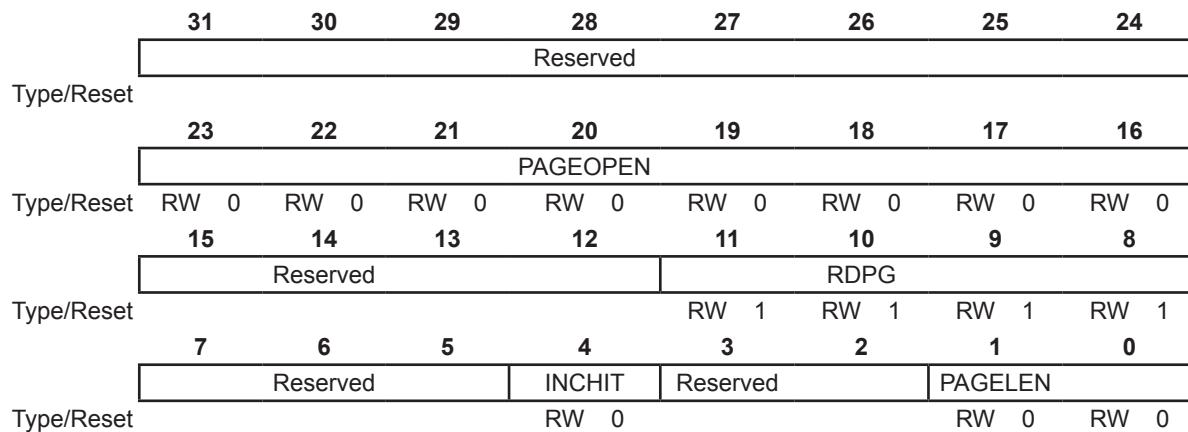
Bits	Field	Descriptions
[11]	BANKEN3	Bank 3 Enable 0: Disable 1: Enable This bit enables or disables bank 3.
[10]	BANKEN2	Bank 2 Enable 0: Disable 1: Enable This bit enables or disables bank 2.
[9]	BANKEN1	Bank 1 Enable 0: Disable 1: Enable This bit enables or disables bank 1.
[8]	BANKEN0	Bank 0 Enable 0: Disable 1: Enable This bit enables or disables bank 0.
[7:6]	MODE3	Set EBI bank 3 access mode 00: D8A8 01: D16A16ALE 10: D8A24ALE 11: D16
[5:4]	MODE2	Set EBI bank 2 access mode 00: D8A8 01: D16A16ALE 10: D8A24ALE 11: D16
[3:2]	MODE1	Set EBI bank 1 access mode 00: D8A8 01: D16A16ALE 10: D8A24ALE 11: D16
[1:0]	MODE0	Set EBI bank 0 access mode 00: D8A8 01: D16A16ALE 10: D8A24ALE 11: D16

EBI Page Control Register – EBIPCR

This register specifies the EBI page read configuration setting.

Offset: 0x004

Reset value: 0x0000_0F00



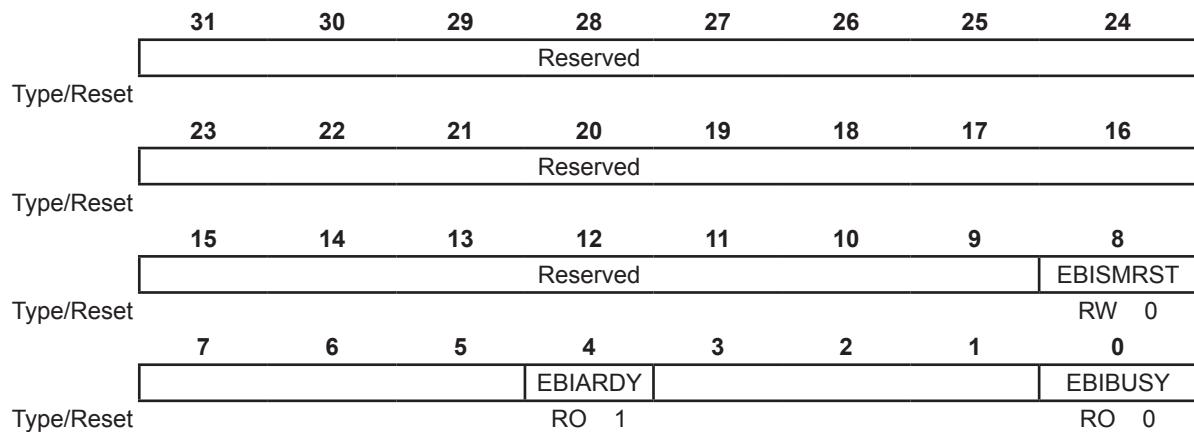
Bits	Field	Descriptions
[23:16]	PAGEOPEN	Maximum Page Open Time Sets the maximum interval of consecutive cycles that a page can be considered open. The cycle unit is basic on an HCLK clock period. Note the PAGEOPEN field should not be set to 0 if the page read is enabled.
[11:8]	RDPG	Page Read Access Time 0000: 1 HCLK clock period 0001: 1 HCLK clock period 0010: 2 HCLK clock periods 1111: 15 HCLK clock periods Sets the number of the cycles for an intrapage page read access time. The cycle unit is basic on an HCLK clock period.
[4]	INCHIT	Incremental Addresses Hit 0: Page hits that occurred on any member in a page 1: Page hits only on incremental addresses Sets the page hits that occurred on any member in a page or only on incremental addresses.
[1:0]	PAGELEN	Page Length 00: 4 members in a page 01: 8 members in a page 10: 16 members in a page 11: 32 members in a page Sets the amount of members in a page.

EBI Status Register – EBISR

This register indicates the EBI status.

Offset: 0x008

Reset value: 0x0000_0010



Bits	Field	Descriptions
[8]	EBISMRST	EBI State Machine Reset 0: Normal 1: Reset EBI state machine Write a “1” to reset the EBI internal state machine to its initial state and keep the original the register settings.
[4]	EBIARDY	EBI Asynchronous Ready Status 0: EBI_ARDY is inactive (Device is in busy state) 1: EBI_ARDY is active (Device is in ready state) Indicate the EBI_ARDY line status.
[0]	EBIBUSY	EBI BUSY 0: EBI is idle 1: EBI is busy Indicates the EBI is busy with an AHB transaction.

EBI Address Timing Register n – EBIATRn, n = 0 ~ 3

This register specifies the address timing setting for bank n. (n = 0 ~ 3)

Offset: 0x010 (n = 0), 0x20 (n = 1), 0x30 (n = 2), 0x40 (n = 3)

Reset value: 0x0000_0F0F

	31	30	29	28	27	26	25	24	
Type/Reset	Reserved								
	23	22	21	20	19	18	17	16	
Type/Reset	Reserved								
	15	14	13	12	11	10	9	8	
Type/Reset	Reserved				ADDRHOLD				
	7	6	5	4	RW 1	RW 1	RW 1	RW 1	
Type/Reset	Reserved				ADDRSETUP				
				RW 1	RW 1	RW 1	RW 1	RW 1	

Bits	Field	Descriptions
[11:8]	ADDRHOLD	Address Hold Time Sets the number of cycles the address is held the EBI_AD bus after EBI_ALE is asserted. This field allows setting to 0.
[3:0]	ADDRSETUP	Address Setup Time Sets the number of cycles the address is driven onto the EBI_AD bus before EBI_ALE is asserted. If set to 0, one cycles is inserted by HW. The cycle unit is basic on HCLK clock period.

EBI Read Timing Register n – EBIRTRn, n = 0 ~ 3

This register specifies the read timing setting for bank n. (n = 0 ~ 3)

Offset: 0x014 (n = 0), 0x24 (n = 1), 0x34 (n = 2), 0x44 (n = 3)

Reset value: 0x000F_3F0F

	31	30	29	28	27	26	25	24
Type/Reset	Reserved							
	23	22	21	20	19	18	17	16
Type/Reset	Reserved				RDHOLD			
					RW	1	RW	1
	15	14	13	12	11	10	9	8
Type/Reset	Reserved		RDSTRB					
			RW	1	RW	1	RW	1
	7	6	5	4	3	2	1	0
Type/Reset	Reserved				RDSETUP			
					RW	1	RW	1

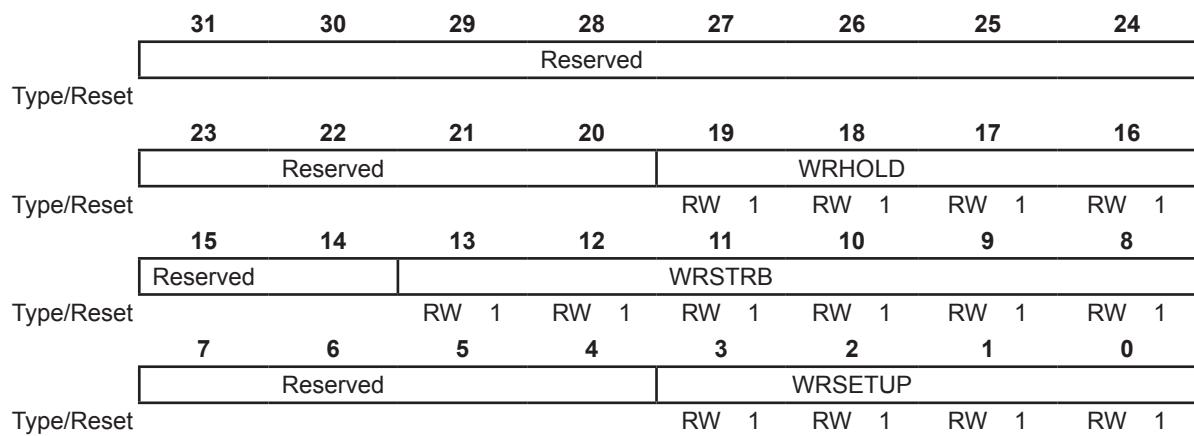
Bits	Field	Descriptions
[24]	PGEN	Page Enable 0: Page read disable 1: Page read enable This bit is used to enable the page read mode for the corresponding bank.
[19:16]	RDHOLD	Read Hold Time Sets the number of cycles that the EBI_CS _n is held active for after EBI_OE is de-asserted. This interval is used for bus turnaround.
[13:8]	RDSTRB	Read Strobe Time Sets the number of cycles that the EBI_OE is held active for. After the specified number of cycles, the data is read. If set to 0, one cycle is inserted by the hardware. The cycle unit is based on an HCLK clock period.
[3:0]	RDSETUP	Read Setup Time Sets the number of cycles for the address setup before EBI_OE is asserted. The cycle unit is basic on an HCLK clock period.

EBI Write Timing Register n – EBIWTRn, n = 0 ~ 3

This register specifies the write timing setting for bank n. (n = 0 ~ 3)

Offset: 0x018 (n = 0), 0x28 (n = 1), 0x38 (n = 2), 0x48 (n = 3)

Reset value: 0x000F_3F0F



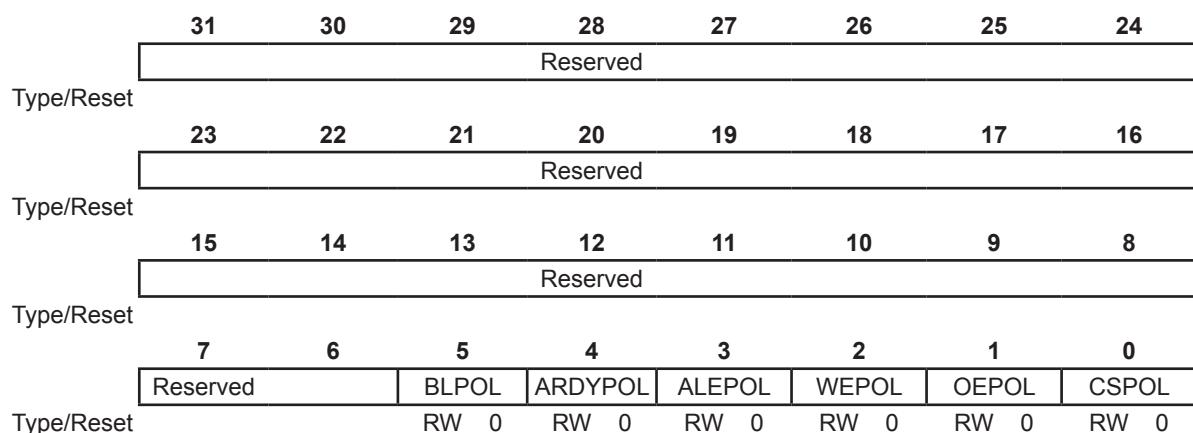
Bits	Field	Descriptions
[19:16]	WEHOLD	Write Hold Time Sets the number of cycles that EBI_CS _n is held active for after EBI_WE is deasserted.
[13:8]	WESTRB	Write Strobe Time Sets the number of cycles that EBI_WE is held active for. If set to 0, one cycle is inserted by the hardware. The cycle unit is basic on an HCLK clock period.
[3:0]	WESETUP	Write Setup Time Sets the number of cycles for the address setup before EBI_WE is asserted. The cycle unit is basic on an HCLK clock period.

EBI Parity Register n – EBIPR, n = 0 ~ 3

This register specifies the polarity of the EBI control signal for bank n. (n = 0 ~ 3)

Offset: 0x01C (n = 0), 0x2C (n = 1), 0x3C (n = 2), 0x4C (n = 3)

Reset value: 0x0000_0000



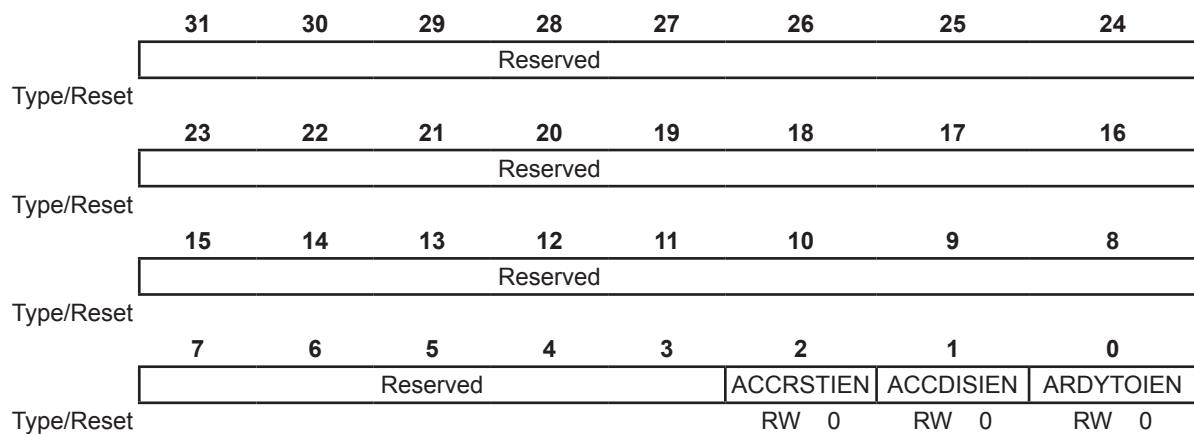
Bits	Field	Descriptions
[5]	BLPOL	Byte Lane Polarity 0: EBI_BL is active low 1: EBI_BL is active high Set the polarity of the EBI_BL line
[4]	ARDYPOL	Asynchronous Ready Polarity 0: EBI_ARDY is active low 1: EBI_ARDY is active high Set the polarity of the EBI_ARDY line
[3]	ALEPOL	Address Latch Polarity 0: EBI_ALE is active low 1: EBI_ALE is active high Set the polarity of the EBI_ALE line
[2]	WEPOL	Write Enable Polarity 0: EBI_WE is active low 1: EBI_WE is active high Set the polarity of the EBI_WE line.
[1]	OEPOL	Output Enable Polarity 0: EBI_OE is active low 1: EBI_OE is active high Set the polarity of the EBI_OE line.
[0]	CSPOL	Chip Selection Polarity 0: EBI_CS is active low 1: EBI_CS is active high Set the polarity of the EBI_CS line.

EBI Interrupt Enable Register – EBIIENR

This register specifies the EBI interrupt enable

Offset: 0x050

Reset value: 0x0000_0000



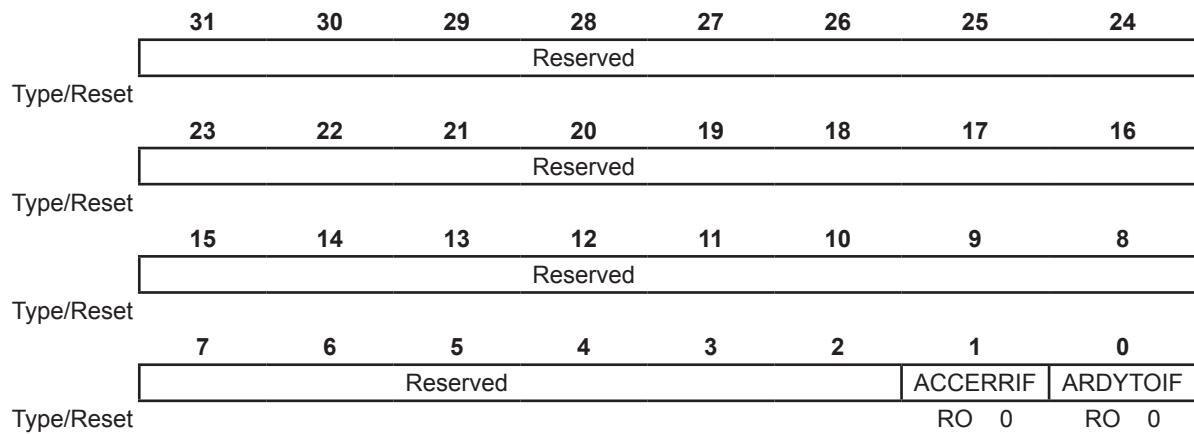
Bits	Field	Descriptions
[2]	ACCRSTIEN	Enable interrupt for issuing a transaction under an EBI state machine reset (EBISMRST bit is set as “1” in the EBISR register).
[1]	ACCDISIEN	Enable interrupt to access the disabled bank.
[0]	ARDYTOIEN	Enable interrupt for the EBI asynchronous ready time-out.

EBI Interrupt Flag Register – EBIIFR

This register specifies interrupt indication for EBI.

Offset: 0x054

Reset value: 0x0000_0000



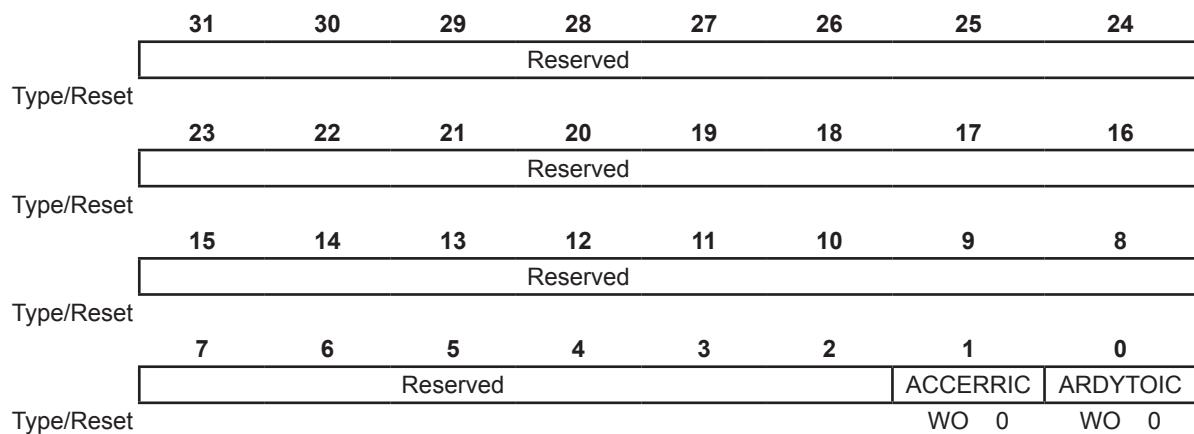
Bits	Field	Descriptions
[1]	ACCERRIF	Set “1” while EBI is accessing the disabled bank or under a EBI state machine reset.
[0]	ARDYTOIF	Set “1” when the EBI asynchronous ready time-out counter reaches a set value.

EBI Interrupt Clear Register – EBIIFCR

This register specifies interrupt clear for the EBI interrupt.

Offset: 0x058

Reset value: 0x0000_0000



Bits	Field	Descriptions
[1]	ACCERRIC	Write a “1” to clear the interrupt flag of the accessed disabled bank or under an EBI state machine reset. If software intends to read this bit then only a “0” is returned.
[0]	ARDYTOIC	Write a “1” to clear the interrupt flag of the EBI asynchronous ready time-out interrupt. If software intends to read this bit then only a “0” is returned.

27 Inter-IC Sound (I²S)

Introduction

The I²S is a synchronous communication interface that can be used as a master or slave to exchange data with other audio peripherals, such as ADCs or DACs. The I²S supports a variety of data formats. In addition to the stereo I²S-justified, Left-justified and Right-justified modes, there are mono PCM modes with 8/16/24/32-bit sample size. When the I²S operates in the master mode, then when using the fractional divider, it can provide an accurate sampling frequency output and support the rate control function and fine-tuning of the output frequency to avoid system problems caused by the cumulative frequency error between different devices.

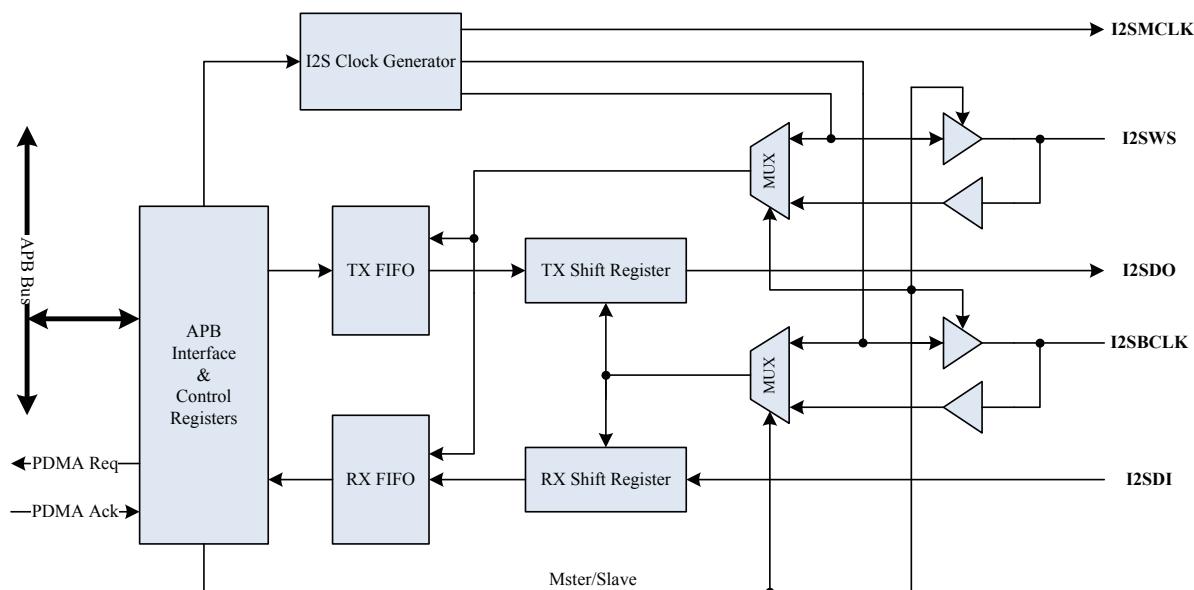


Figure 188. I²S Block diagram

Features

- Master or slave mode
- Mono and stereo
- I²S-justified, Left-justified, and Right-justified mode
- 8/16/24/32-bit sample size with 32-bit channel extended
- 8 × 32-bit Tx & Rx FIFO with PDMA supported
- 8-bit Fractional Clock Divider with rate control

Functional Descriptions

I²S Master and Slave Mode

The I²S can operate in slave or master mode. Within the I²S module the difference between these modes lies in the word select (WS) signal which determines the timing of data transmissions.

- In the master mode, the word select signal is generated internally by a clock rate generator.
- In the slave mode, the word select signal is input on the I²S_WS pin.
- When an I²S bus is enabled, the word select, bit clock signals are sent continuously by the bus master.
- The mute control bit will place the transmit channel in a mute condition. When the mute mode is enabled, the transmit channel FIFO operates normally, but the output data stream is discarded and replaced by zeroes. This bit does not affect the receive channel so data reception can occur normally.

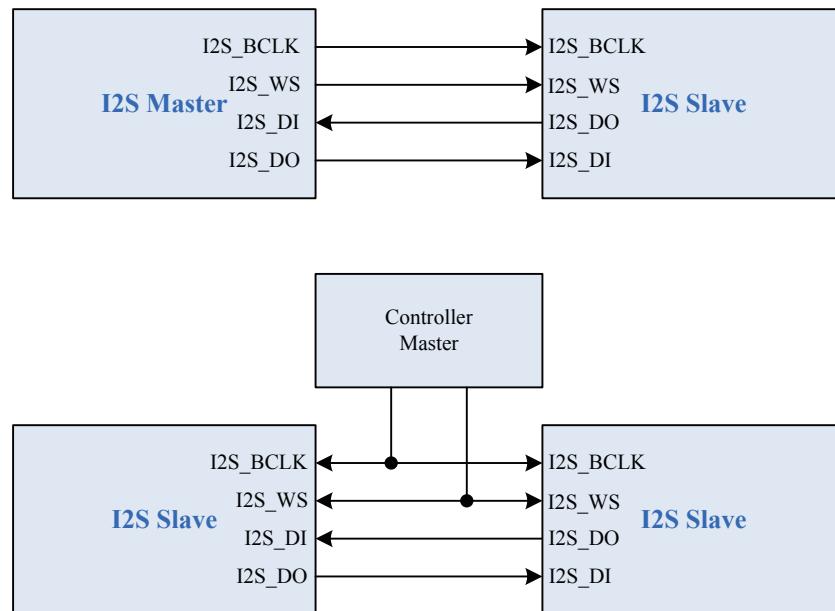


Figure 189. Simple I²S master/slave configuration

I²S Clock Rate Generator

The main (I²S_MCLK) and bit clock (I²S_BCLK) rates for the I²S are determined by the values in the I2SCDR register. The required I²S bit clock rate setting depends on the desired audio sample rate desired, the format (stereo/mono) used, and the data size. The main clock rate (I²S_MCLK) is generated using a fractional rate divider which is a divided down PCLK frequency of the I²S. Values of the numerator (X) and the denominator (Y) must be chosen to produce a frequency twice that of the main clock (I²S_MCLK). The output frequency of the divider is divided by 2 in order to get the duty cycle of the output clock more even. The I²S clock generator block diagram is shown in Figure 190. The equation for the fractional rate divider is:

$$\begin{aligned} \text{I}^2\text{S_MCLK} &= 1/2 * \text{PCLK} * (X/Y), \text{ and } 2X \leq Y, X \neq 0, Y \neq 0 \\ \text{I}^2\text{S_BCLK} &= \text{I}^2\text{S_MCLK} / N, N = \{1, 2, \dots, 64\} \end{aligned}$$

Because the fractional rate divider is a fully digital implementation function, the divider output clock transitions are synchronous with the input source clock. Therefore, the fractional rate divider will generate some jitter with some divider settings. Users should make note of this phenomenon when choosing the X and Y setup values. It is possible to avoid jitter entirely by choosing fractions such that X divides evenly into Y. For example, 2/4, 2/6, 3/9, 1/N, etc.

The tables below show the recommended setup values to reduce clock jitter for different source clocks and sample rates.

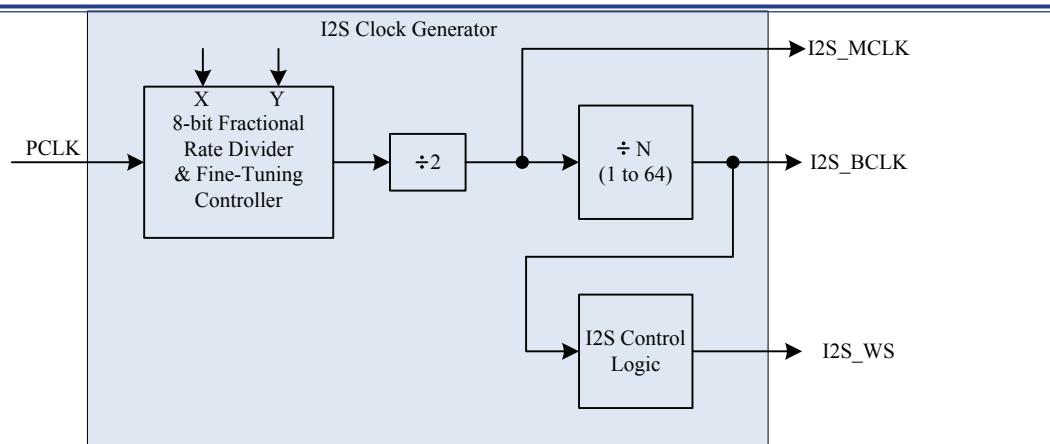


Figure 190. I²S clock generator diagram

Table 72. Recommend Fs List @ 8 MHz PCLK

Fs (Hz)	512 Fs		384 FS		256 FS		192 FS		128 Fs		64 FS		32 FS		16 FS	
	X	Y	X	Y	X	Y	X	Y	X	Y	X	Y	X	Y	X	Y
8,000	—	—	48	125	32	125	24	125	16	125	8	125	4	125	2	125
11,025	—	—	—	—	85	241	59	223	45	255	21	238	9	204	3	136
12,000	—	—	—	—	48	125	36	125	24	125	12	125	6	125	3	125
16,000	—	—	—	—	—	—	48	125	32	125	16	125	8	125	4	125
22,050	—	—	—	—	—	—	—	—	85	241	45	255	21	238	9	204
24,000	—	—	—	—	—	—	—	—	48	125	24	125	12	125	6	125
32,000	—	—	—	—	—	—	—	—	—	—	32	125	16	125	8	125
44,100	—	—	—	—	—	—	—	—	—	—	85	241	45	255	21	238
48,000	—	—	—	—	—	—	—	—	—	—	48	125	24	125	12	125
96,000	—	—	—	—	—	—	—	—	—	—	—	—	48	125	24	125
192,000	—	—	—	—	—	—	—	—	—	—	—	—	—	—	48	125

Table 73. Recommend Fs List @ 48 MHz PCLK

Fs (Hz)	512 Fs		384 FS		256 FS		192 FS		128 Fs		64 FS		32 FS		16 FS	
	X	Y	X	Y	X	Y	X	Y	X	Y	X	Y	X	Y	X	Y
8,000	18	211	8	125	9	211	4	125	5	234	1	94	1	188	—	—
11,025	2	17	3	34	1	17	3	68	1	34	1	68	1	136	—	—
12,000	16	125	12	125	8	125	6	125	4	125	2	125	1	125	1	250
16,000	43	252	16	125	18	211	8	125	9	211	5	234	1	94	1	188
22,050	4	17	3	17	2	17	3	34	1	17	1	34	1	68	1	136
24,000	32	125	24	125	16	125	12	125	8	125	4	125	2	125	1	125
32,000	71	208	32	125	43	252	16	125	18	211	9	211	5	234	1	94
44,100	119	253	85	241	4	17	3	17	2	17	1	17	1	34	1	68
48,000	—	—	48	125	32	125	24	125	16	125	8	125	4	125	2	125
96,000	—	—	—	—	—	—	48	125	32	125	16	125	8	125	4	125
192,000	—	—	—	—	—	—	—	—	—	—	32	125	16	125	8	125

Table 74. Recommend Fs List @ 72 MHz PCLK

Fs (Hz)	512 Fs		384 FS		256 FS		192 FS		128 Fs		64 FS		32 FS		16 FS	
	X	Y	X	Y	X	Y	X	Y	X	Y	X	Y	X	Y	X	Y
8,000	12	211	9	211	6	211	5	234	3	211	1	141	—	—	—	—
11,025	4	51	1	17	2	51	1	34	1	51	1	102	1	204	—	—
12,000	18	211	8	125	9	211	4	125	5	234	1	94	1	188	—	—
16,000	19	167	18	211	12	211	9	211	6	211	3	211	1	141	—	—
22,050	37	236	2	17	4	51	1	17	2	51	1	51	1	102	1	204
24,000	43	252	16	125	18	211	8	125	9	211	5	234	1	94	1	188
32,000	38	167	43	252	19	167	18	211	12	211	6	211	3	211	1	141
44,100	53	169	4	17	37	236	2	17	4	51	2	51	1	51	1	102
48,000	71	208	32	125	43	252	16	125	18	211	9	211	5	234	1	94
96,000	—	—	—	—	71	208	32	125	43	252	18	211	9	211	5	234
192,000	—	—	—	—	—	—	—	71	208	43	252	18	211	9	211	

I²S Interface Format

I²S-justified stereo mode

The standard I²S-justified mode is where the Most Significant Bit (MSB) of the stereo audio sample data is available on the second rising edge of the BCLK clock following a WS signal transition. In the stereo mode, a low WS state indicates left channel data and a high state indicates right channel data. Figure 191 and Figure 192 show the standard I²S-justified stereo mode format.

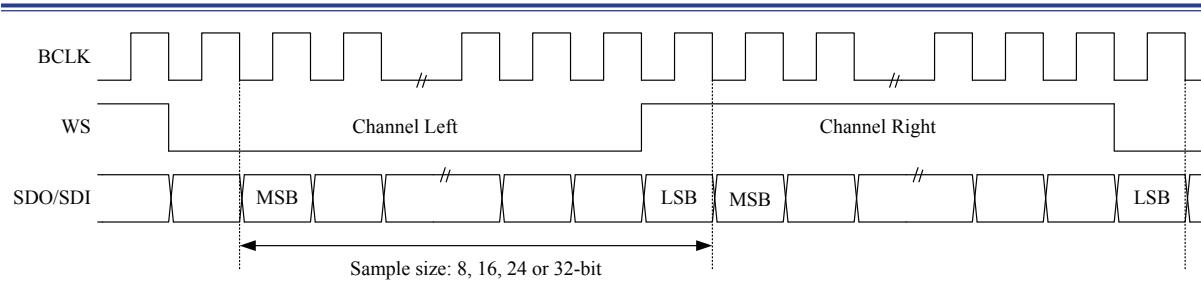


Figure 191. I²S-justified stereo mode waveforms

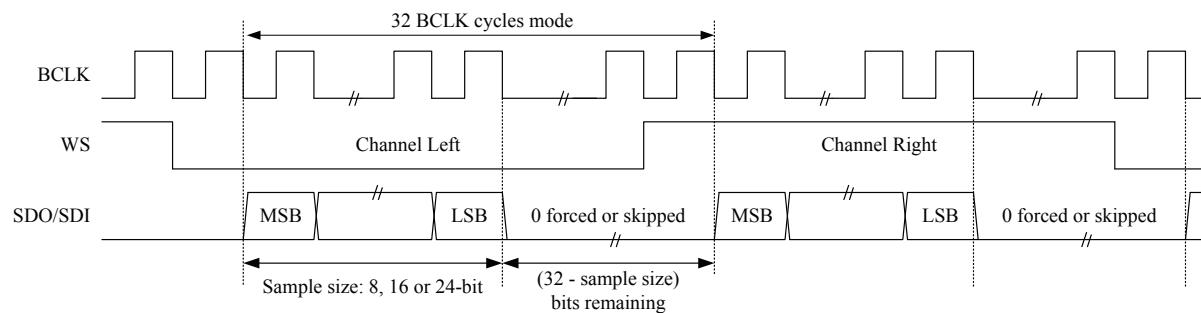


Figure 192. I²S-justified stereo mode waveforms (32-bit channel enabled)

Left-justified stereo mode

Left-Justified mode is where the Most Significant Bit (MSB) of the stereo audio sample data is available on the first rising edge of BCLK following a WS transition. Figure 193 and Figure 194 are shown with a left I²S-justified stereo mode format.

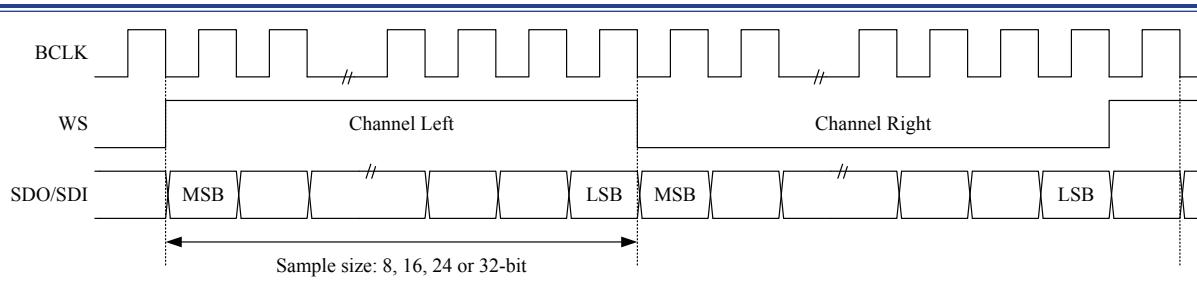


Figure 193. Left-justified stereo mode waveforms

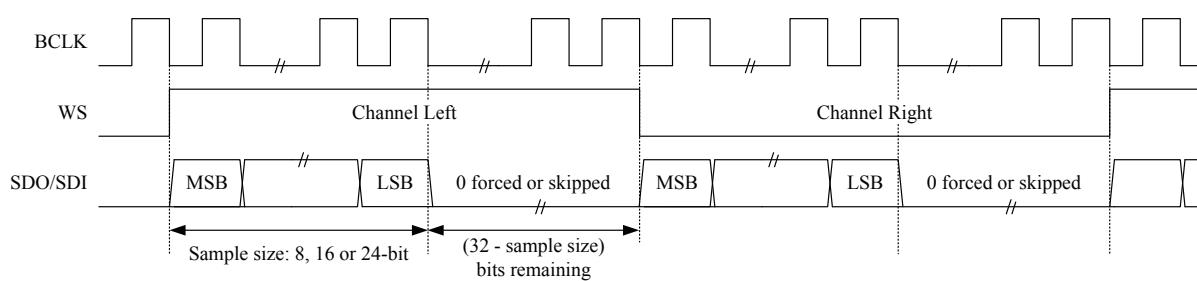


Figure 194. Left-justified stereo mode waveforms (32-bit channel enabled)

Right-justified stereo mode

Right-Justified mode is where the Least Significant Bit (LSB) of the stereo audio sample data is available on the rising edge of BCLK preceding a WS transition and where the MSB is transmitted first. Figure 195 and Figure 196 show a right I²S-justified stereo mode format.

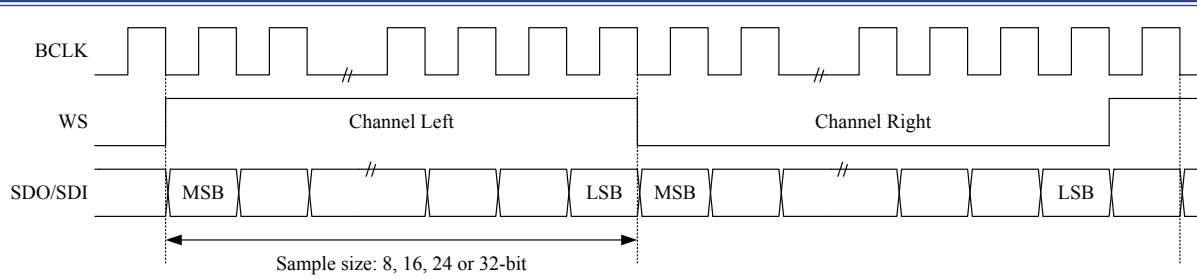


Figure 195. Right-justified stereo mode waveforms

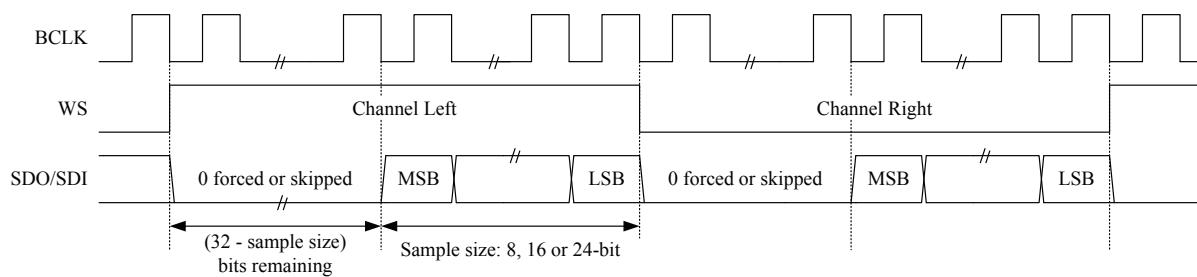


Figure 196. Right-justified stereo mode waveforms (32-bit channel enabled)

I²S-justified mono mode

In the I²S-justified mono mode, the Most Significant Bit (MSB) of the mono audio sample data is available on the second rising edge of the BCLK clock following a falling edge on the WS signal. Figure 197 and Figure 198 show a I²S-justified mono mode format.

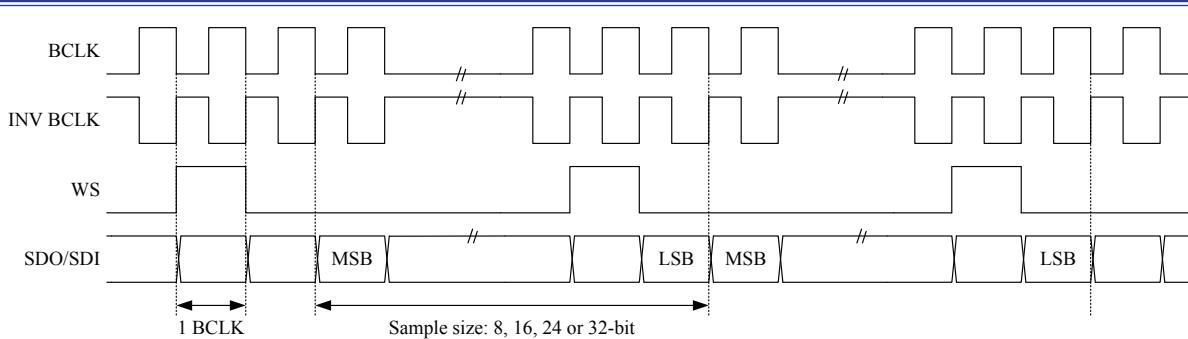


Figure 197. I²S-justified mono mode waveforms

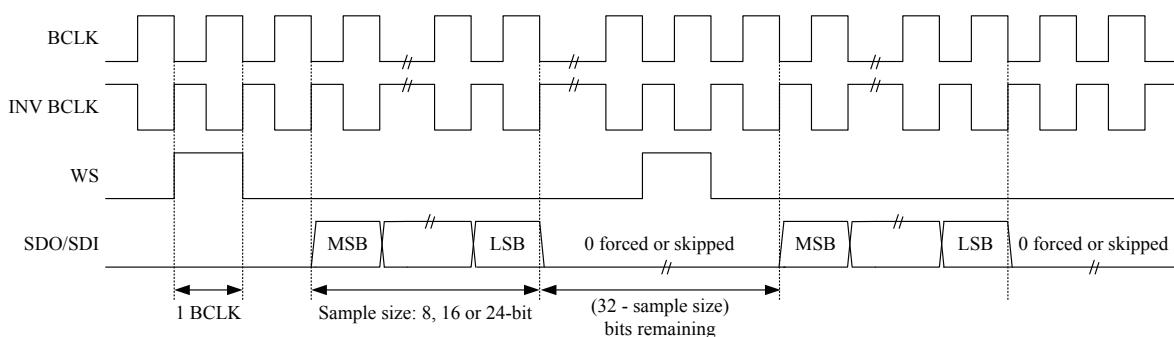


Figure 198. I²S-justified mono mode waveforms (32-bit channel enabled)

Left-justified mono mode

In the left-justified mono mode, the Most Significant Bit (MSB) of the mono audio sample data is available on the first rising edge of the BCLK clock following a falling edge on the WS signal. Figure 199 and Figure 200 show a left-justified mono mode format.

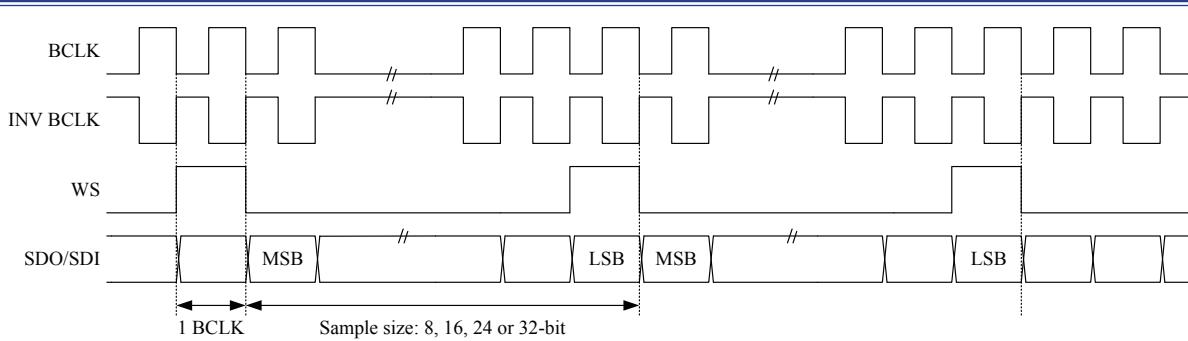


Figure 199. Left-justified mono mode waveforms

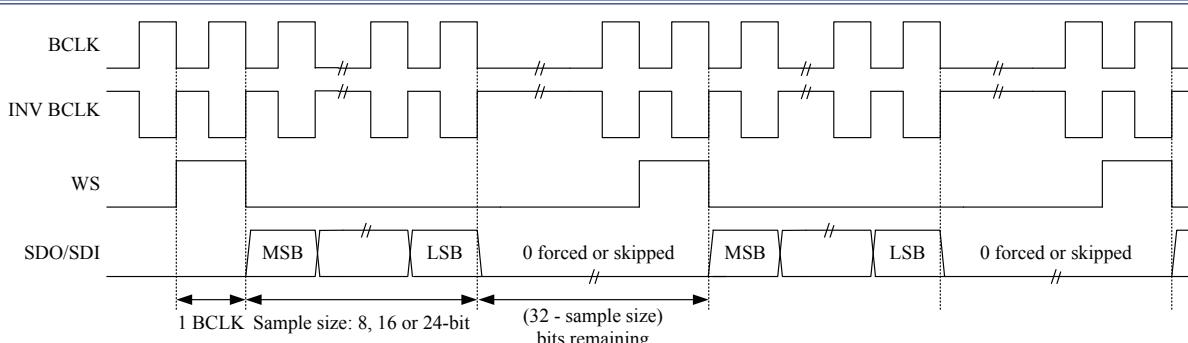


Figure 200. Left-justified mono mode waveforms (32-bit channel enabled)

Right-justified mono mode

In the right-justified mono mode, the Least Significant Bit (LSB) of the mono audio sample data is available on the last rising edge of the BCLK clock preceding a rising edge on the WS signal. Figure 201 and Figure 202 show the right-justified mono mode format.

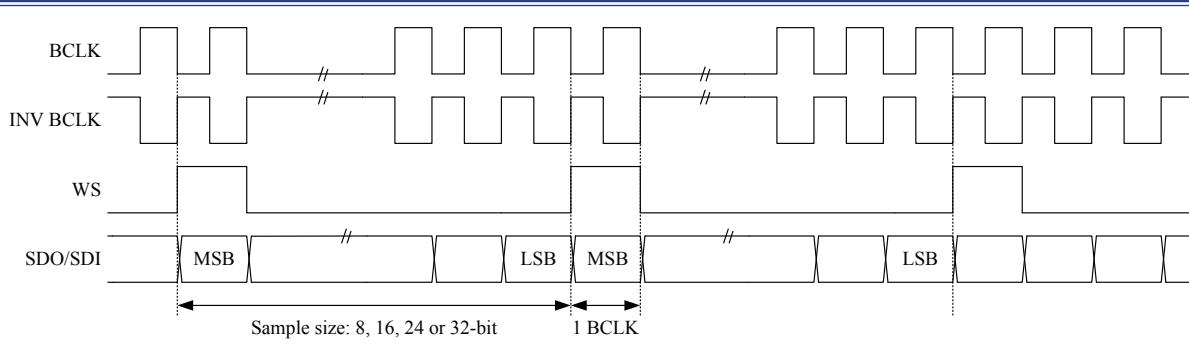


Figure 201. Right-justified mono mode waveforms

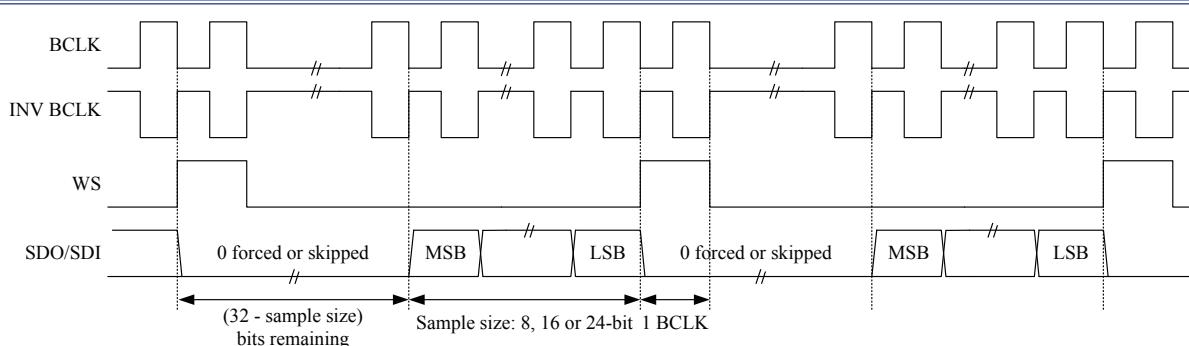


Figure 202. Right-justified mono mode waveforms (32-bit channel enabled)

I²S-justified repeat mode

In the I²S-justified repeat mode, the Most Significant Bit (MSB) of the mono audio sample data is available on the second rising edge of the BCLK clock following a WS signal transition. In this mode the same data is transmitted twice, once when WS is low and again when WS is high. Figure 203 and Figure 204 show the I²S-justified repeat mode format.

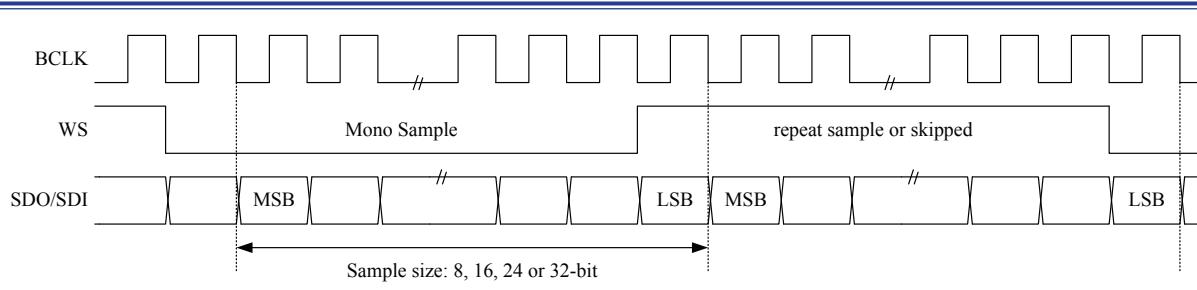


Figure 203. I²S-justified repeat mode waveforms

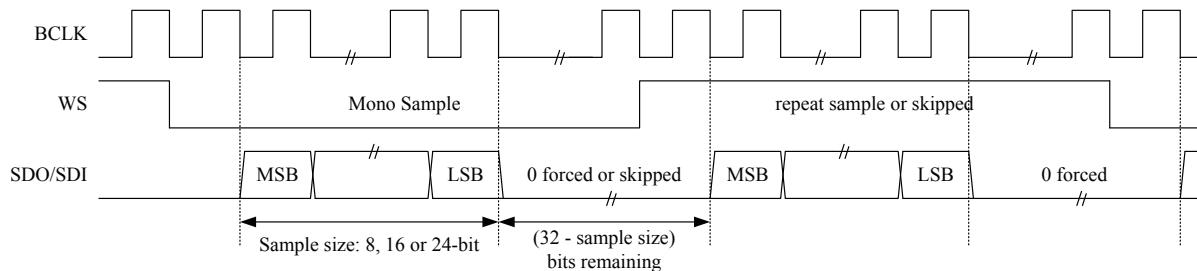


Figure 204. I²S-justified repeat mode waveforms (32-bit channel enabled)

FIFO Control and Arrangement

The I²S handles audio data for transmission and reception and is performed via the FIFO controller. Each transmitted or received FIFO has a depth of 8 words ($8 \times 32\text{-bit}$) and can buffer the data. The format is dependent upon the stereo/mono mode and sample size setting. The detailed FIFO data content format is shown in Figure 205. The FIFO controller consists of comparators which compare the current FIFO levels with configurable depth settings. The current level of the TX or RX FIFO status can be seen in the TXFS and RXFS fields of the I²S status register (I2SSR).

Mono 8-bit Data	FIFO Pointer Address	M
7 N+3 0 7 N+2 0 7 N+1 0 7 N 0		
Mono 16-bit Data		
15 N+1 0 15 N 0		M
Mono 24-bit Data		
31 23 N 0		M
Mono 32-bit Data		
31 N 0		M
Stereo 8-bit Data		
7 LEFT+1 0 7 RIGHT+1 0 7 LEFT 0 7 RIGHT 0		M
Stereo 16-bit Data		
15 LEFT 0 15 RIGHT 0		M
Stereo 24-bit Data		
31 23 LEFT 0		M
31 23 RIGHT 0		M+1
Stereo 32-bit Data		
31 LEFT 0		M
31 RIGHT 0		M+1

Figure 205. FIFO data content arrangement for various modes

PDMA and Interrupt Use and Configuration

When the level of received data in the RX FIFO is equal to or greater than the level defined by the RXFTLS field in the I²S FIFO control register (I2SFCR), the relative RXFTL flag will be set and then a I²S RX PDMA request will be generated. A CPU interrupt will be generated if the enable bit of the I²S RX PDMA request or the RX FIFO trigger level interrupt are asserted. When the level of transmitted data in the TX FIFO is equal to or less than the level defined by the TXFTLS field in the I²S FIFO control register (I2SFCR), the relative TXFTL flag will be set and a I²S TX PDMA request will be generated. A CPU interrupt will be generated if the enable bit of the I²S TX PDMA request or TX FIFO trigger level interrupt are asserted.

The I²S transmitter and receiver have separate PDMA requests and can be assigned to two different PDMA channels. When a PDMA request is enabled for the I²S transmitter (TXDMAEN = 1) then this will automatically request that data is transferred to the assigned I²S TX PDMA channel whenever TX FIFO space is available and TXFTL is active. When a PDMA request is enabled for the receiver (RXDMAEN = 1) then this will automatically request the data transfers to the I²S RX PDMA channel whenever data is present in the receive FIFO and when RXFTL is active.

Register Map

The following table shows the I²S registers and reset values.

Table 75. Register map of I²S

Register	Offset	Description	Reset Value
I²S Base Address = 0x40026000			
I2SCR	0x000	I ² S Control Register	0x0000_0000
I2SIER	0x004	I ² S Interrupt Enable Register	0x0000_0000
I2SCDR	0x008	I ² S Clock Divider Register	0x0000_0000
I2STXDR	0x00C	I ² S Tx Data Register	0x0000_0000
I2SRXDR	0x010	I ² S Rx Data Register	0x0000_0000
I2SFCR	0x014	I ² S FIFO Control Register	0x0000_0000
I2SSR	0x018	I ² S Status Register	0x0000_0809
I2SRCNTR	0x01C	I ² S Rate Counter Value Register	0x0000_0000

Register Descriptions

I²S Control Register – I2SCR

This register specifies the corresponding I²S function enable control.

Offset: 0x000

Reset value: 0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
Type/Reset							
Reserved							
Type/Reset				RW	0	RW	0
RW 0							
Type/Reset	15	14	13	12	11	10	9
CLKDEN RXDMAEN TXDMAEN TXMUTE CHANNEL REPEAT MCLKEN BITEXT							
Type/Reset	RW 0						
RW 0							
Type/Reset	7	6	5	4	3	2	1
FORMAT SMPSIZE MS RXEN TXEN I2SEN							
Type/Reset	RW 0						

Bits	Field	Descriptions
[19]	MCKINV	MCLK Inverse Enable 0: Disable 1: Enable
[18]	BCKINV	BCLK Inverse Enable 0: Disable 1: Enable
[17]	RCSEL	Rate Control Select (master only) 0: slower 1: faster
[16]	RCEN	Rate Control Enable (master only) 0: Disable 1: Enable
[15]	CLKDEN	Clock Divider Enable (master only) 0: Disable 1: Enable The clock divider can be used to generate the MCLK and BCLK clock of the I ² S interface for master mode.
[14]	RXDMAEN	RX PDMA Request Enable 0: Disable 1: Enable
[13]	TXDMAEN	TX PDMA Request Enable 0: Disable 1: Enable
[12]	TXMUTE	TX Mute Enable 0: Disable 1: Enable

Bits	Field	Descriptions
[11]	CHANNEL	<p>Stereo or Mono</p> <p>0: Stereo 1: Mono</p> <p>Note: This bit should be configured when I²S is disabled.</p>
[10]	REPEAT	<p>Repeat Mode</p> <p>0: Disable 1: Enable</p> <p>This mode is for I²S-justified stereo configuration only, transmitting the mono data on both channels and receiving just the left channel data and ignoring the right. Enabling the repeat mode will reset the CHANNEL bit automatically.</p> <p>Note: This bit should be configured when the I²S is disabled.</p>
[9]	MCLKEN	<p>MCLK Output Enable (master only)</p> <p>0: Disable 1: Enable</p> <p>Note: This bit should be configured when the I²S is disabled.</p>
[8]	BITEXT	<p>32-bit Channel Enable</p> <p>0: Disable 1: Enable</p> <p>Setting this bit will force the channel size to 32-bits. If the sample size is 8/16/24-bits, the remaining bits will be forced to 0 in the TX and ignored in the RX.</p> <p>Note: This bit should be configured when the I²S is disabled.</p>
[7:6]	FORMAT	<p>Data Format</p> <p>00: I²S-justified 01: Left-justified 10: Right-justified 11: reserved</p> <p>Note: This bit should be configured when the I²S is disabled.</p>
[5:4]	SMPSIZE	<p>Sample Size</p> <p>00: 8-bit 01: 16-bit 10: 24-bit 11: 32-bit</p> <p>Note: This bit should be configured when the I²S is disabled.</p>
[3]	MS	<p>Master or Slave Mode</p> <p>0: Master 1: Slave</p> <p>Note: This bit should be configured when the I²S is disabled.</p>
[2]	RXEN	<p>RX Enable</p> <p>0: Disable 1: Enable</p> <p>Note: This bit should be configured when the I²S is disabled.</p>
[1]	TXEN	<p>TX Enable</p> <p>0: Disable 1: Enable</p>
[0]	I ² SEN	<p>I²S Enable</p> <p>0: Disable 1: Enable</p>

I²S Interrupt Enable Register – I2SIER

This register contains the corresponding I²S interrupt enable bits.

Offset: 0x004

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
Reserved								
Type/Reset	23	22	21	20	19	18	17	16
Reserved								
Type/Reset	15	14	13	12	11	10	9	8
Reserved								
Type/Reset	7	6	5	4	3	2	1	0
	Reserved	RXOVIEN	RXUDIEN	RXFTLIEN	Reserved	TXOVIEN	TXUDIEN	TXFTLIEN
Type/Reset	RW	0	RW	0	RW	0	RW	0

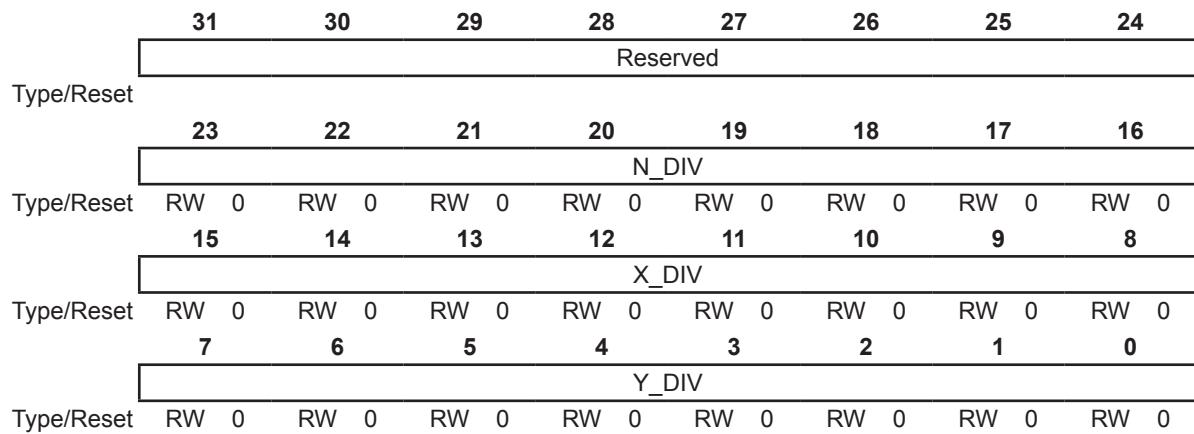
Bits	Field	Descriptions
[6]	RXOVIEN	RX FIFO Overflow Interrupt Enable 0: Disable 1: Enable
[5]	RXUDIEN	RX FIFO Underflow Interrupt Enable 0: Disable 1: Enable
[4]	RXFTLIEN	RX FIFO Trigger Level Interrupt Enable 0: Disable 1: Enable
[2]	TXOVIEN	TX FIFO Overflow Interrupt Enable 0: Disable 1: Enable
[1]	TXUDIEN	TX FIFO Underflow Interrupt Enable 0: Disable 1: Enable
[0]	TXFTLIEN	TX FIFO Trigger Level Interrupt Enable 0: Disable 1: Enable

I²S Clock Divider Register – I2SCDR

This register specifies the I²S clock divider ratio.

Offset: 0x008

Reset value: 0x0000_0000



Bits	Field	Descriptions
[23:16]	N_DIV	N divider for BCLK Note: This bit should be configured when the I ² S is disabled.
[15:8]	X_DIV	X divider for MCLK $(X \neq 0) \&\& (Y \neq 0) \&\& (X/Y \geq 1/255) \&\& (X/Y \leq 127/255)$ Note: This bit should be configured when the I ² S is disabled.
[7:0]	Y_DIV	Y divider for MCLK $(X \neq 0) \&\& (Y \neq 0) \&\& (X/Y \geq 1/255) \&\& (X/Y \leq 127/255)$ Note: This bit should be configured when the I ² S is disabled.

I²S Tx Data Register – I2STXDR

This register is used to specify the I²S transmitted data.

Offset: 0x00C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
TXDR								
Type/Reset	WO 0							
23 22 21 20 19 18 17 16								
TXDR								
Type/Reset	WO 0							
15 14 13 12 11 10 9 8								
TXDR								
Type/Reset	WO 0							
7 6 5 4 3 2 1 0								
TXDR								
Type/Reset	WO 0							

Bits	Field	Descriptions
[31:0]	TXDR	TX Data Register

I²S Rx Data Register – I2SRXDR

This register is used to store the I²S received data.

Offset: 0x010

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
RXDR								
Type/Reset	RO 0							
23 22 21 20 19 18 17 16								
RXDR								
Type/Reset	RO 0							
15 14 13 12 11 10 9 8								
RXDR								
Type/Reset	RO 0							
7 6 5 4 3 2 1 0								
RXDR								
Type/Reset	RO 0							

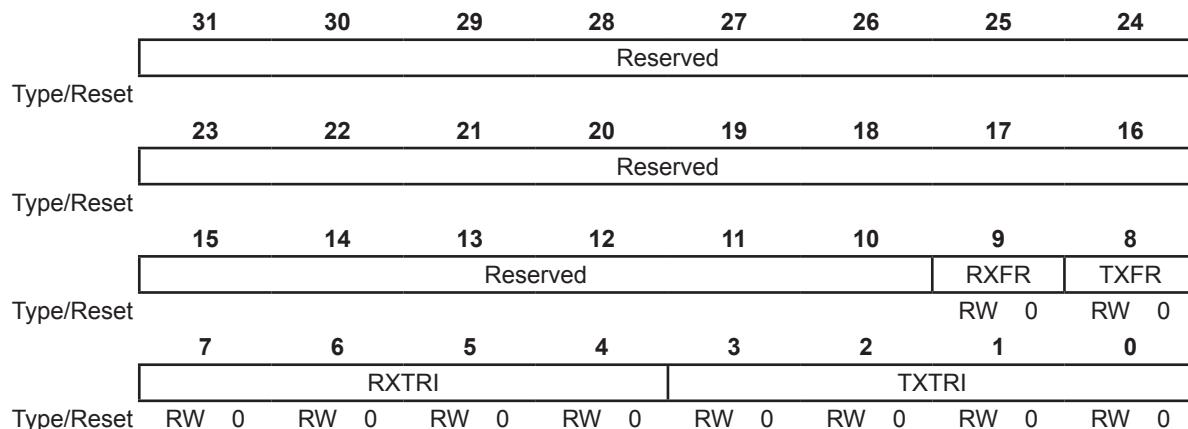
Bits	Field	Descriptions
[31:0]	RXDR	RX Data Register

I²S FIFO Control Register – I2SFCR

This register contains the related I²S FIFO control bits.

Offset: 0x014

Reset value: 0x0000_0000



Bits	Field	Descriptions
[9]	RXFRST	RX FIFO Reset Set this bit to reset the Rx FIFO.
[8]	TXFRST	TX FIFO Reset Set this bit to reset the Tx FIFO.
[7:4]	RXFTLS	RX FIFO Trigger Level Select 0000: Trigger level is 0 0001: Trigger level is 1 ... 0111: Trigger level is 7 1xxx: Trigger level is 8 When the data contained in the Rx FIFO is equal to or greater than the level defined by the RXFTLS field, the RXFTL flag will be set.
[3:0]	TXFTLS	TX FIFO Trigger Level Select 0000: Trigger level is 0 0001: Trigger level is 1 ... 0111: Trigger level is 7 1xxx: Trigger level is 8 When the data contained in the Tx FIFO is equal to or less than the level defined by the TXFTLS field, the TXFTL flag will be set.

I²S Status Register – I2SSR

This register contains the relevant I²S status.

Offset: 0x018

Reset value: 0x0000_0809

	31	30	29	28	27	26	25	24
	RXFS							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset	CLKRDY TXBUSY CHS							
	15	14	13	12	11	10	9	8
	Reserved RXFFUL RXFEMT RXFOV RXFUD RXFTL							
Type/Reset	RO 0 RO 1 WC 0 WC 0 WC 0							
	7	6	5	4	3	2	1	0
Type/Reset	Reserved TXFFUL TXFEMT TXFOV TXFUD TXFTL							
	RO 0	RO 1	WC 0	WC 0	WC 0	WC 0	WC 1	

Bits	Field	Descriptions
[31:28]	RXFS	Rx FIFO Status 0000: Rx FIFO empty 0001: Rx FIFO contains 1 data ... 1000: Rx FIFO contains 8 data Others: Reserved
[27:24]	TXFS	Tx FIFO Status 0000: Tx FIFO empty 0001: Tx FIFO contains 1 data ... 1000: Tx FIFO contains 8 data Others: Reserved
[18]	CLKRDY	Clock Divider Output Ready Flag 0: not ready 1: ready
[17]	TXBUSY	Tx Busy Flag 0: not busy 1: busy
[16]	CHS	Channel Status 0: left channel 1: right channel
[12]	RXFFUL	Rx FIFO Full Flag 0: Rx FIFO not full 1: Rx FIFO full
[11]	RXFEMT	Rx FIFO Empty Flag 0: Rx FIFO not empty 1: Rx FIFO empty

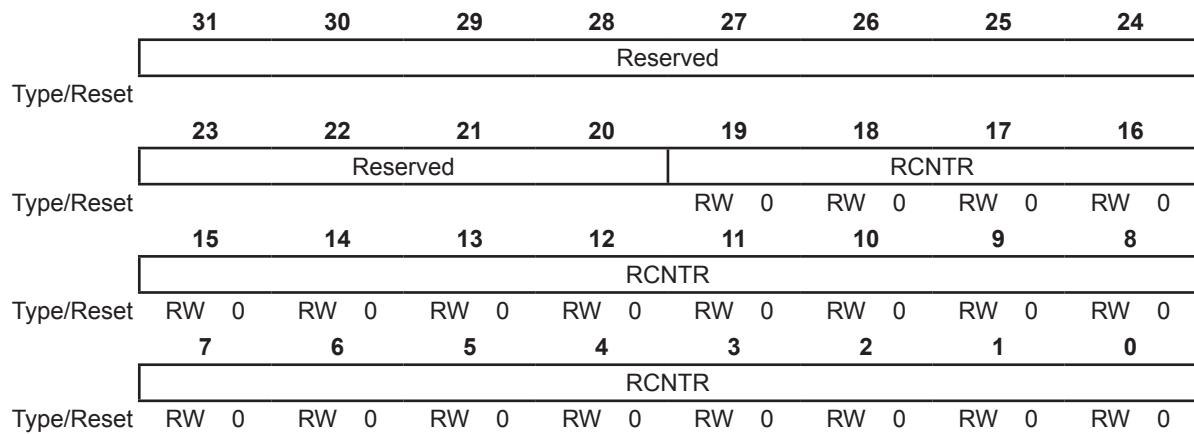
Bits	Field	Descriptions
[10]	RXFOV	Rx FIFO Overflow Flag 0: Rx FIFO not overflow 1: Rx FIFO overflow This bit is set by hardware and cleared by writing 1.
[9]	RXFUD	Rx FIFO Underflow Flag 0: Rx FIFO not underflow 1: Rx FIFO underflow This bit is set by hardware and cleared by writing 1.
[8]	RXFTL	Rx FIFO Trigger Level Flag 0: Data in the Rx FIFO is less than the trigger level 1: Data in the Rx FIFO is equal to or higher than the trigger level This bit is set by hardware and cleared by writing 1.
[4]	TXFFUL	Tx FIFO Full Flag 0: Tx FIFO not full 1: Tx FIFO full
[3]	TXFEMT	Tx FIFO Empty Flag 0: Tx FIFO not empty 1: Tx FIFO empty
[2]	TXFOV	Tx FIFO Overflow Flag 0: Tx FIFO not overflow 1: Tx FIFO overflow This bit is set by hardware and cleared by writing 1.
[1]	TXFUD	Tx FIFO Underflow Flag 0: Tx FIFO not underflow 1: Tx FIFO underflow This bit is set by hardware and cleared by writing 1.
[0]	TXFTL	Tx FIFO Trigger Level Flag 0: Data in the Tx FIFO is higher than the trigger level 1: Data in the Tx FIFO is equal to or less than the trigger level This bit is set by hardware and cleared by writing 1.

I²S Rate Counter Value Register – I2SRCNTR

This register specifies the I²S rate control counter value.

Offset: 0x01C

Reset value: 0x0000_0000



Bits	Field	Descriptions
[19:0]	RCNTR	<p>Rate Counter Value</p> <p>This value must be higher than zero for useful rate fine-tuning control.</p> <p>RCSEL=1, RCNTR = 1 ~ (2Y-1): $MCLK' = (1 + \frac{1}{(2Y-1)}) \times MCLK$</p> <p>RCSEL=1, RCNTR > (2Y-1): $MCLK' = (1 + \frac{1}{RCNTR}) \times MCLK$</p> <p>RCSEL=X, RCNTR = 0: $MCLK' = MCLK$</p> <p>RCSEL=0, RCNTR > (2Y+1): $MCLK' = (1 - \frac{1}{RCNTR}) \times MCLK$</p> <p>RCSEL=0, RCNTR = 1 ~ (2Y+1): $MCLK' = (1 - \frac{1}{(2Y+1)}) \times MCLK$</p>

28 Cyclic Redundancy Check (CRC)

Introduction

The CRC (Cyclic Redundancy Check) calculation unit is an error detection technique test algorithm and uses to verify data transmission or storage data correctness. A CRC calculation takes a data stream or a block of data as input and generates a 16- or 32-bit output remainder. Ordinarily, a data stream is suffixed by a CRC code and used as a checksum when being sent or stored. Therefore, the received or restored data stream is calculated by the same generator polynomial as described above. If the new CRC code result does not match the one calculated earlier, that means data stream contains a data error.

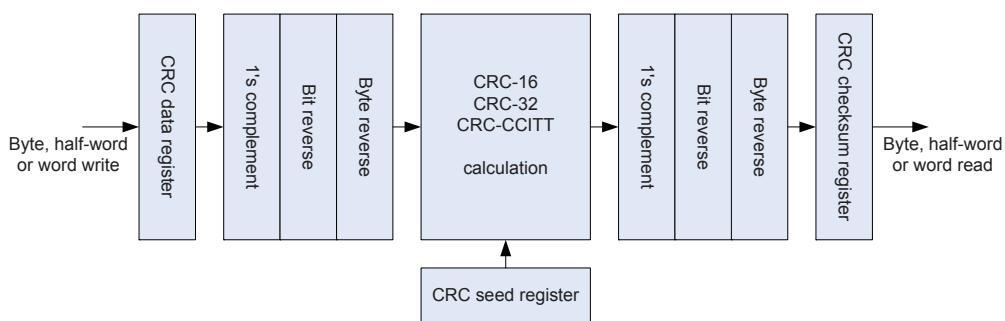


Figure 206. CRC Block Diagram

Features

- Support CRC16 polynomial: 0x8005, $X^{16}+X^{15}+X^2+1$
- Support CCITT CRC16 polynomial: 0x1021, $X^{16}+X^{12}+X^5+1$
- Support IEEE-802.3 CRC32 polynomial: 0x04C11DB7, $X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^8+X^7+X^5+X^4+X^2+X+1$
- Support 1's complement, byte reverse & bit reverse operation on data and checksum
- Support byte, half-word & word data size
- Programmable CRC initial seed value
- CRC computation done in 1 AHB clock cycle for 8-bit data and 4 AHB clock cycles for 32-bit data
- Support PDMA to complete a CRC computation of a block of memory

Functional Descriptions

CRC Computation

After setting the polynomial in the CRCCR register, put the 16-bit/32-bit seed value into the CRCSDR register and switch off the data and checksum 1's complement, byte reverse and bit reverse calculation. After all the data has been written to the CRCDR register one by one, read the 16-bit/32-bit checksum value from the CRCCSR register. If the data written to the CRCDR register is implemented using a half-word or word method, the data byte reverse calculation is needed additionally.

Reflect CRC Computation

Taking the CRC-CCITT as an example, its polynomial original value is 0x1021, but the reflected polynomial value is 0x8408. Open the data/checksum bit reverse calculation and checksum byte reverse calculation in the application, it can get the reflected checksum value. If the input data are written to the CRCDR register by half-word or word write way, the data byte reverse calculation is needed additionally. If there is any “1” in the seed value, the reflected value by bit reverse calculation should be written to CRCSDR register.

Co-work with PDMA

Use the software trigger PDMA to write all data in the memory to the CRCDR register in the correct order. After the PDMA transmission has completed, the CPU can read the checksum value from the CRCCSR register, for which the setup method is the same as for CPU usage. If the input data is written to the CRCDR register using a half-word or word method, the data byte reverse calculation is needed additionally.

Register Map

The following table shows the CRC registers and reset values.

Table 76. Register map of CRC

Register	Offset	Description	Reset Value
CRC Base Address = 0x4008A000			
CRCCR	0x000	CRC Control Register	0x0000_0000
CRCSDR	0x004	CRC Seed Register	0x0000_0000
CRCCSR	0x008	CRC Checksum Register	0x0000_0000
CRCDR	0x00C	CRC Data Register	0x0000_0000

Register Descriptions

CRC Control Register – CRCCR

This register specifies the corresponding CRC function enable control.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24	
Type/Reset	Reserved								
	23	22	21	20	19	18	17	16	
Type/Reset	Reserved								
	15	14	13	12	11	10	9	8	
Type/Reset	Reserved								
	7	6	5	4	3	2	1	0	
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	
	SUMCMPL	SUMBYRV	SUMBIRV	DATCMPL	DATBYRV	DATBIRV	POLY		

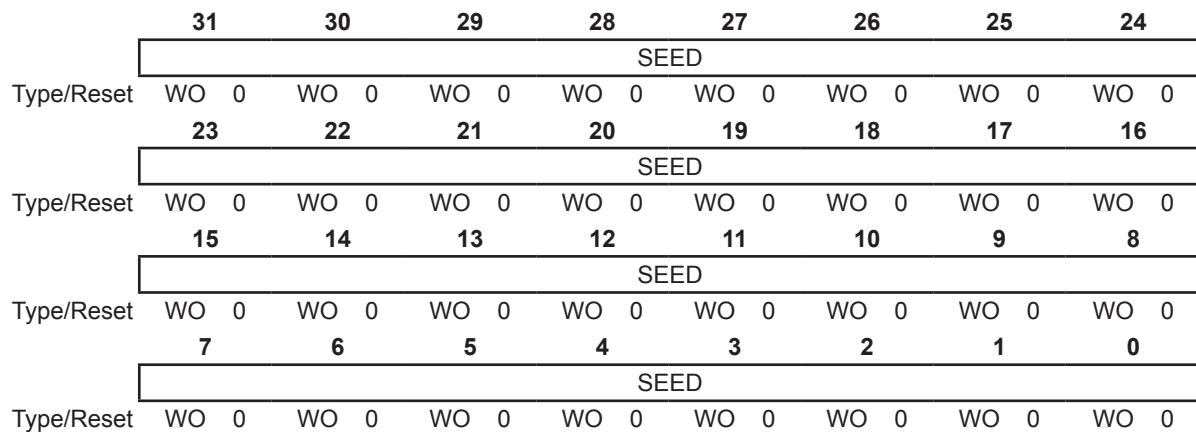
Bits	Field	Descriptions
[7]	SUMCMPL	1's Complement operation on Checksum 0: disable 1: enable
[6]	SUMBYRV	Byte Reverse operation on Checksum 0: disable 1: enable
[5]	SUMBIRV	Bit Reverse operation on Checksum 0: disable 1: enable
[4]	DATCMPL	1's Complement operation on Data 0: disable 1: enable
[3]	DATBYRV	Byte Reverse operation on Data 0: disable 1: enable
[2]	DATBIRV	Bit Reverse operation on Data 0: disable 1: enable
[1:0]	POLY	CRC polynomial 00: CRC-CCITT (0x1021) 01: CRC-16 (0x8005) 1X: CRC-32 (0x04C11DB7)

CRC Seed Register – CRCSDR

This register is used to specify the CRC seed.

Offset: 0x004

Reset value: 0x0000_0000



Bits	Field	Descriptions
[31:0]	SEED	Put the 16/32-bit seed value in this register according to the polynomial setting in the CRCCR register.

CRC Checksum Register – CRCCSR

This register contains the CRC checksum.

Offset: 0x008

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
CHKSUM								
Type/Reset	RO 0							
23 22 21 20 19 18 17 16								
CHKSUM								
Type/Reset	RO 0							
15 14 13 12 11 10 9 8								
CHKSUM								
Type/Reset	RO 0							
7 6 5 4 3 2 1 0								
CHKSUM								
Type/Reset	RO 0							

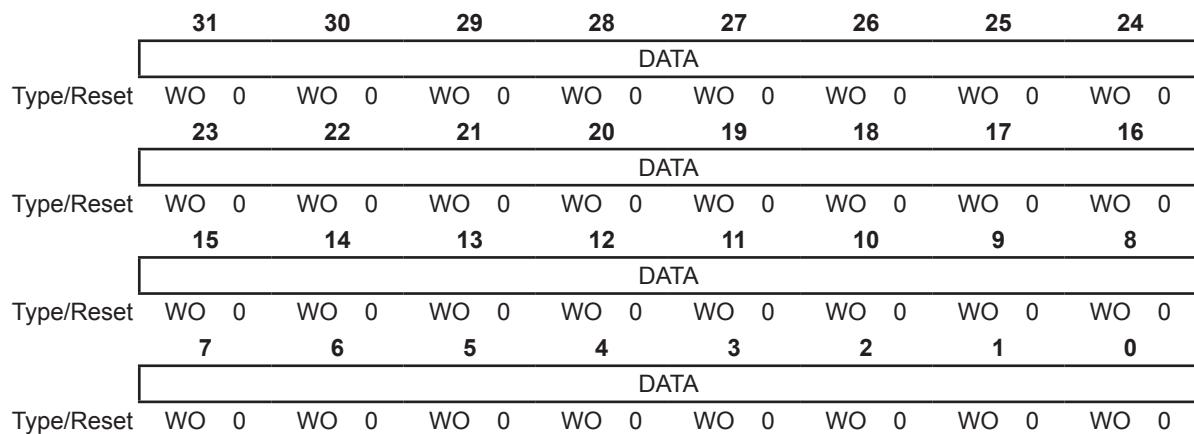
Bits	Field	Descriptions
[31:0]	CHKSUM	Get the 16/32-bit checksum via this register according to the polynomial setting in the CRCCR register after all data has been written to the CRCDR register.

CRC Data Register – CRCDR

This register is used to specify the CRC data.

Offset: 0x00C

Reset value: 0x0000_0000



Bits	Field	Descriptions
[31:0]	DATA	Byte, half-word & word write are allowed. 1's complement, byte reverse and bit reverse operation can be applied.

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