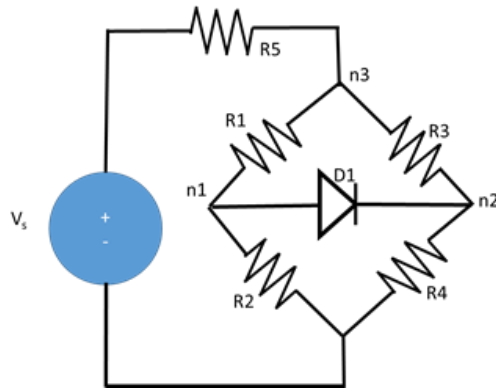


## Circuit Thermal Solution

This is the scenario: Your organization makes a Silicon based integrated circuit. This circuit contains a diode in this resistive circuit.



Since this particular diode is created by your semiconductor process and has never been characterized, you have no model to simulate it's behavior. Testing has indicated that the integrated circuit does not work properly, and

the technical team has decided the problem is that the diode is not behaving as expected. The technical team as asked you to determine why.

Use these parameters  $R_1 = 1k$ ,  $R_2 = 4k$ ,  $R_3 = 3k$ ,  $R_4 = 2k$ ,  $R_5 = 1k$  ohms for the resistors. Use source voltages  $V_s$  from 1V to 10V. For diode  $D_1$  use these parameters:

$$I_0 = 3e-9, q = 1.6e-19, k_B = 1.38e-23, n = 2.0$$

This device is broad and we know that as is typical in power devices we can assume all heat is conducted down through the device into the metal flag of the package and into the printed circuit board, that is we can assume that the heat transfer by radiation and convection are negligible. Also because it is a wide device we can assume the temperature profile is essentially one dimensional. Since we make the diode structure we know the diode's structure. It has this stack

A Si active región 10 mils thick, silicon has a thermal coefficient of  $1.3 \text{ W/cmC}$

A Si bulk bulk región 15 mils thick also with a thermal coefficient of  $1.3 \text{ W/cmC}$

A Cu back metal 5 mils thick with  $3.86 \text{ W/cmC}$

A thermal paste holding the die in the package 25 mils thick with a thermal coefficient of  $0.5 \text{ W/cmC}$

A Metal flag 100 mils thick with a thermal coefficient of  $5 \text{ W/cmC}$

Assume the die area is 10 microns square, and the base of the die is at 25 degrees C above room temperature or 325 degrees K. (The diode equations expects temperature in K!)

You should approach this analysis by breaking the problem into steps.

**Step 1)** Create a function to calculate the temperature of the diode given a voltage and current. You'll have to calculate how the temperature changes through the vertical stack of layers. The temperature change through a layer is calculated as follows:

$\text{heat\_flow} = \text{power\_dissipated} = \text{current} * \text{voltage}$

$\text{thermal\_resistance} = d/(K*A)$

where d is thickness, K is the thermal coefficient, and A is the area

$\text{temperature\_at\_top} = \text{temperature\_at\_bottom} + \text{heat\_flow} * \text{thermal\_resistance}$

**Step 2)** Create a function calculates the diode current and temperature error given a voltage and temperature guess. (Use the function created in Step 1 to calculate the temperature so you can find the difference between that and the guess.)

**Step 3)** Create a function to be called by fsolve. This function should take voltage guesses for each node and the temperature of the diode and calculate the current equation at each node. That is, the sum of all currents entering and exiting the node should be 0. Likewise, using the above functions, return the temperature difference which is also to be minimized. (Note that this is similar to problem 6.17 in Newman.) The deliverable is an error function that allows you to solve for the node voltages, and temperature.

**Step 4)** Sweep source voltage from 1 to 10 volts, and generate the following plots:

One plot showing the node voltage at n1, the node voltage at n2, and the node voltage at n3, all as a function of swept source voltage

Self heating temperature as a function of swept source voltage

Diode current as a function of swept source voltage