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Three Don't Cares

ECE 411 MP4 CP3 Check-in

What we did

For all advanced features, we first individually test them on their own and their individual components before putting them all together.

L1 Cache → 2-way Set Associative (Sohil)

Upgraded our L1 caches from the given directly mapped to a one cycle hit two way set associative cache. Using a set associative cache would improve performance as we do not have to constantly replace each line that often.

L1 Cache → 4-way Set Associative (Sohil, Edwin)

Upgraded the 2-way set associative cache with pseudo LRU algorithm. When we increase the number of ways for the L1, we decrease the likelihood of a miss when we have some larger and very repetitive code.

L2 Cache → 8-way Set Associative (Sohil)

Inserted an eight-way set associative L2 cache with pseudo LRU algorithm for the replacement policy. The L2 adds to the memory hierarchy and helps to reduce the number of cycles when we have a miss in the L1 caches. Hopefully, it is large enough where we don't need to read too much from physical memory.

Parameterized Caches (Sohil) -- Incomplete

Parameterized caches functionality-wise are the same as the above caches. They will increase our performance when placed in the pipeline. We use a python script to generate the systemverilog code, and more importantly the related pseudo LRU. The benefit of the parameterized caches is that we can choose to either increase or decrease the number of ways, lines, or data size as we wish. This also increases our programmability and flexibility

Tournament Branch Predictor (Edwin) – Partially working, minus a corner case

Included a Local Branch Predictor (LHR + PHT) and Global Branch Predictor (GHR + PHT). The branches were then decided using a meta predictor based on the 10 least significant bits of the PC. The branch predictor will allow us to improve performance by predicting if we should take a branch earlier in the pipeline. Assuming the branch predictor is working as intended, we will be able to reduce the time for branching from a 3 cycle delay down to a 1 cycle delay.

Eviction Write Buffer (Edwin, Ryan) -- Not tested, don't have functionality nor integration

Created an eviction write buffer for under the L2 cache and before the cacheline adaptor/physical memory. The eviction write buffer will speed up the cache miss dirty states. Since miss dirty is a write to

the next level memory/physical memory it can be costly. Having a parallel write buffer to store the evicted values will speed up the L2.

M Extension (Ryan)
Multiplier created with a Wallace tree. Used a python script to generate the Systemverilog code. Divider is repeated subtraction. We tested the functionality of it but did not integrate it. The M extension provides some speed up in the sense that a multiply function can be done within one clock cycle instead of having it written out in software as a large loop.

What we plan to do

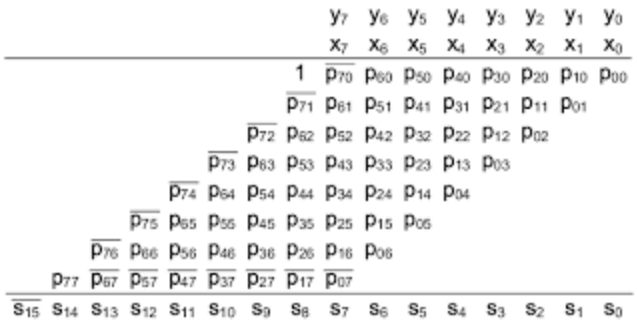
- Make L2 cache once cycle hit to decrease miss times. We may decrease the size if necessary as it may hinder our power and area usage. (Sohil)
- (maybe) improve our tournament branch predictor such that the global branch predictor will be two levels
- Adjust code and reduce the number of redundant and unnecessary wires and MUXes (Edwin)
- Integrate M extension modules into the pipeline (Ryan)

Performance of Each Feature

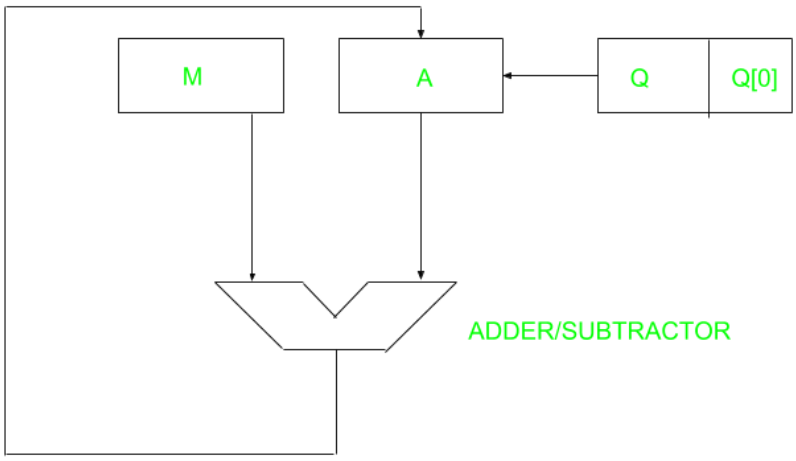
Baseline for CP3 Code: 5353185000ps
Upgraded L1 (4 way): 1632375000 ps
Upgraded L1 (4 way) + New L2 Cache (8 way): 1015245000 ps
Tournament Branch Predictor: *no data*
Upgraded L1 (4 way) + New L2 Cache (8 way) + Eviction Write Buffer: *no data*
M Extension: N/A

M – EXTENSION

Bough Wooley Wallace Tree (32 bits)



Restoration Divider



Power/Timing/Area Information

WALLCE TREE MULTIPLIER TIMING

```
out[63] (out)                                    0.00       6.95 f
data arrival time                                           6.95
-------------------------------------------------------------------
(Path is unconstrained)
```

WALLCE TREE MULTIPLIER POWER

```
--------------------------------------------------------------------------------
                                    Switch   Int      Leak     Total
Hierarchy                           Power    Power    Power    Power    %
--------------------------------------------------------------------------------
wallace                             2.44e+03 3.37e+03 1.03e+05 5.91e+03 100.0
  bestcra (cra)                       72.166  237.597 3.49e+03  313.251   5.3
    adds[63] (fa_63)                   0.470    1.186   73.583    1.730   0.0
```

WALLCE TREE MULTIPLIER AREA

```
Number of ports:                         6135
Number of nets:                          9678
Number of cells:                         3831
Number of combinational cells:           2633
Number of sequential cells:                 0
Number of macros/black boxes:               0
Number of buf/inv:                        195
Number of references:                    1137

Combinational area:               5752.782014
Buf/Inv area:                      106.932001
Noncombinational area:               0.000000
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                  5752.782014
Total area:                 undefined

Hierarchical area distribution
------------------------------

                                  Global cell area          Local cell area
                                  ------------------
----------------------------
Hierarchical cell                 Absolute   Percent  Combi-     Noncombi-  Black-
                                  Total      Total    national   national
boxes   Design
--------------------------------  ---------  -------  ---------  ---------
------  ---------
wallace                           5752.7820    100.0   977.0180     0.0000
0.0000  wallace
bestcra                            231.4200      4.0     0.0000     0.0000
0.0000  cra
```

RESTORATION DIVIDER TIMING

```
data arrival time                                          4.10

clock my_clk (rise edge)                                  10.00      10.00
clock network delay (ideal)                                0.00      10.00
clock uncertainty                                         -0.10       9.90
A_reg[32]/CK (DFF_X1)                                      0.00       9.90 r
library setup time                                        -0.04       9.86
data required time                                                    9.86
-----------------------------------------------------------------------------
data required time                                                    9.86
data arrival time                                                    -4.10
-----------------------------------------------------------------------------
slack (MET)                                                           5.75
```

RESTORATION DIVIDER POWER

```
Global Operating Voltage = 1.1
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1nW


--------------------------------------------------------------------------------
                                     Switch   Int      Leak     Total
Hierarchy                            Power    Power    Power    Power    %
--------------------------------------------------------------------------------
divider                               55.181   97.218 2.78e+04  180.163 100.0
  adder (addsub)                       3.472    9.516 2.16e+03   15.144   8.4
```

RESTORATION DIVIDER AREA

```
Number of ports:                          414
Number of nets:                          1262
Number of cells:                          867
Number of combinational cells:            718
Number of sequential cells:               110
Number of macros/black boxes:               0
Number of buf/inv:                        131
Number of references:                      27

Combinational area:                821.673995
Buf/Inv area:                       70.224001
Noncombinational area:             495.823983
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                  1317.497978
Total area:                 undefined

Hierarchical area distribution
------------------------------

                                  Global cell area          Local cell area
                                  ------------------  --------------------------
Hierarchical cell                 Absolute   Percent  Combi-    Noncombi-  Black
                                  Total      Total    national  national
boxes   Design
--------------------------------  ---------  -------  --------  ---------
------  --------------------------------
divider                           1317.4980     100.0  682.2900   479.8640
0.0000  divider
adder                              139.3840      10.6    0.0000     0.0000
0.0000  addsub
```

Verification Strategy

Wallace Tree

```
2059820608 * 3749318774 = 2815652224 actual 2815652224
 114670496 * 2824350411 = 4215539680 actual 4215539680
1456549881 * 2033280886 =  241322950 actual  241322950
2205263428 * 1642356730 = 1648335464 actual 1648335464
1420840436 *  851282607 =  598659532 actual  598659532
1879104593 *  414230641 =  279340993 actual  279340993
predicted     -10000, actual               -10000
predicted      10000, actual                10000
Tested 500 signed*signed, unsigned*unsigned, signed*unsigned  errors          0
```

Wrote a testbench that generated 500 combinations of signed/unsigned multiplication to verify the results. Checked output of multiplier against built in * operator to verify, increased error count on mismatch. Error count is 0…. Success Upper and Lower 32 bits are correct values!

Restoration Divider

```
3365190047/   3268493 Quotient:       1029 Remainder    1910750, Ready 1
2340900709/   2169496 Quotient:       1079 Remainder      14525, Ready 1
1965504673/   2503050 Quotient:        785 Remainder     610423, Ready 1
TESTED         500 runs. Finished UNSIGNED with           0 errors
```

```
 1875898847/     109624 Quotient:       17112 Remainder       12959, Ready 1
  944587120/    1077081 Quotient:         876 Remainder     1064164, Ready 1
-1463368623/      40611 Quotient:      -36033 Remainder      -32460, Ready 1
-1069124992/    4144449 Quotient:        -257 Remainder    -4001599, Ready 1
   58322182/    3752334 Quotient:          15 Remainder     2037172, Ready 1
TESTED         500 runs. Finished SIGNED with          0 errors
```

Wrote a testbench that generated 500 combinations of signed and unsigned divisions to verify results. Checkout the quotient and remainder against built-in / operator and % operator to verify, increased error count on mismatch. Error count is 0 …Successfully Division. Also test edge case division by 0. It does sets all bits in quotient to 1 as per spec.

```
 876074344/          0 Quotient:          -1 Remainder   876074344, Ready 1
```

(edge case division by 0 sets quotient to all 1's aka -1)