K. J. Somaiya College of Engineering, Mumbai-77
(Autonomous College Affiliated to University of Mumbai)

Course Code	Course Title	Teaching Scheme			Credits Assigned			
		Theory	Practical	Tutorial	Theory	Practical	Tutorial	Total
UEXA501	Reconfigurable Logic Design	--	02	--	--	--	--	--

Course Code	Course Title	Examination Scheme						
		Theory Marks			Term Work	Practical	Oral	Total
		Test		End Sem. Exam ESE				
		Test 1	Test 2					
UEXA501	Reconfigurable Logic Design	--	--	--	--	--	--	--

Reconfigurable computing refers to the computing on a reconfigurable platform, which is currently an FPGA, but can include other adaptable fabric. Many computer scientists consider FPGAs to be more than just hardware chips for fast prototyping.

Course Outcomes:

At the end of successful completion of the course a student will be able to

1. Develop simple applications from functional specification and Implement on FPGA / CPLD.
2. Use features in FPGA such as soft/ hard cores, Intellectual Property (IP) cores, high speed I/O etc.
3. Explore the scope of FPGA implementation in research areas.

Week No.	Topics	Hrs.
1-3	For a group of 2-3 students functional specifications will be given. They are supposed to write code in VHDL and implement the system on Helium or DE1 boards	06
4-6	Using features on DE1 Board such as serial interface, Monitor Interface, audio codec.	06
7-8	Introduction to Soft Embedded core , IP Core.	04
9	Searching research paper based on of FPGA Implementation	02
10,11	Presentation on one IEEE paper	04