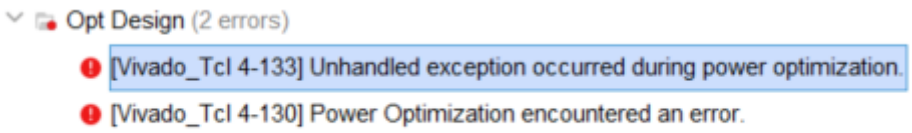
我们的系统测试程序在 vivado 生成比特流时遇到了如下问题，且无相关 INFO 说明：



我们查阅了一些资料后并未在代码方面找到有效方法，只在 Xlinx 社区查到了一条建议

68659 - 2016.3 Vivado - Power Optimization might crash during Block RAM optimization when run by default during opt_design

Sep 23, 2021 • Knowledge

TITLE

68659 - 2016.3 Vivado - Power Optimization might crash during Block RAM optimization when run by default during opt_design

DESCRIPTION

A crash can occur during Power Optimization of Block RAM during opt_design.

This optimization is run by default in opt_design.

```
Finished Running Vector-less Activity Propagation
```

```
ERROR: [Vivado_Tcl 4-131] Power Optimization encountered an exception: ERROR: [Common 17-70] Application Exception: !(flpInst->getEnable(CISynOptions::IDT_QUI) != "F" && enBDD == pwroptMgr->getCurrentBddMgr()->bddZero())
```

SOLUTION

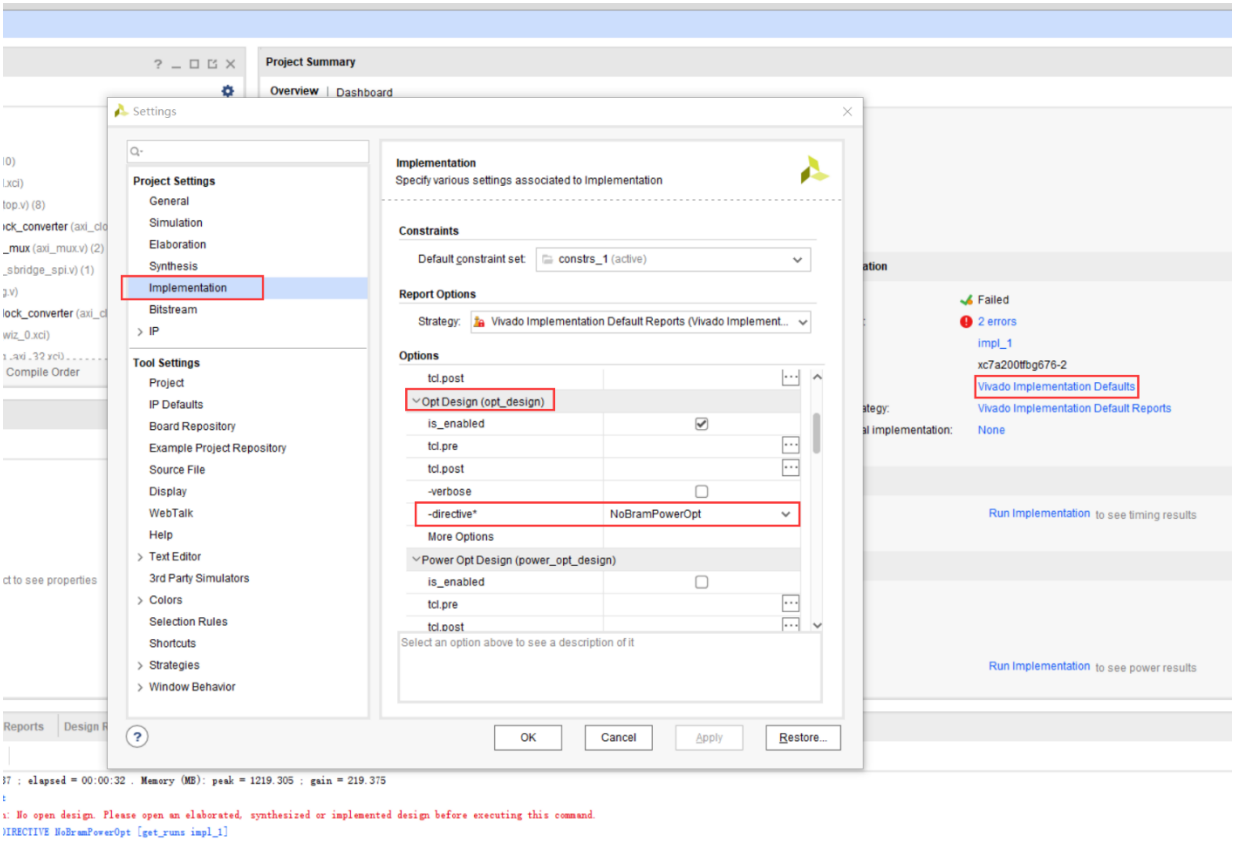
This issue has been fixed in Vivado 2016.4.

Vivado 2016.3 users can work around the problem by disabling Block Ram Power Optimization.

To do so, use the following opt_design switch:

```
opt_design -directive NoBramPowerOpt
```

对 implementation 的 Opt Design 进行了如下调整后可以正常生成比特流：将 drective 项设置为 NoBramPowerOpt



我们所提交的比特流文件是用这种方式生成的，可能会与测试脚本的结果略有差别