

**UART Characteristics**

**Synchronization:**Each data item (5-8 bits) requires synchronization

**Asynchronous data transfer:** Mismatch of clock frequencies in TX and RX**,** Requires overhead for synchronization -> additional bits**,** Requires effort for synchronization  additional hardware **Advantage:** Clock does not have to be transmitted**,** Transmission delays are automatically compensated

**On-board connections:** Signal levels are 3V or 5V with reference to ground**,** Off-board connections require stronger output drivers (circuits)

**Control registers**

32-bit memory-mapped control registers for each GPIO

Configure up to 16 I/Os

GPIOx\_MODER RM 8.4.1, pg. 278

- I/O direction (input, output, alternate function, analog)

GPIOx\_OTYPER RM 8.4.2, pg. 279

- output type (push-pull or open-drain)

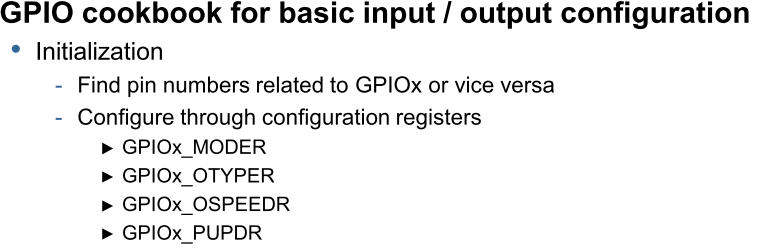
GPIOx\_OSPEEDR RM 8.4.3, pg. 279

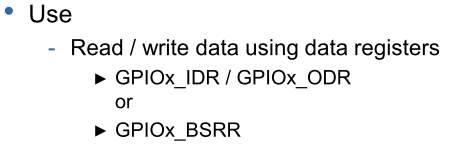
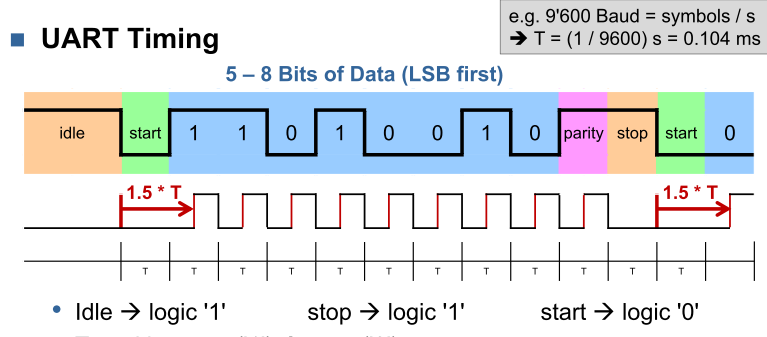
- speed (the I/O speed pins are directly connected to the

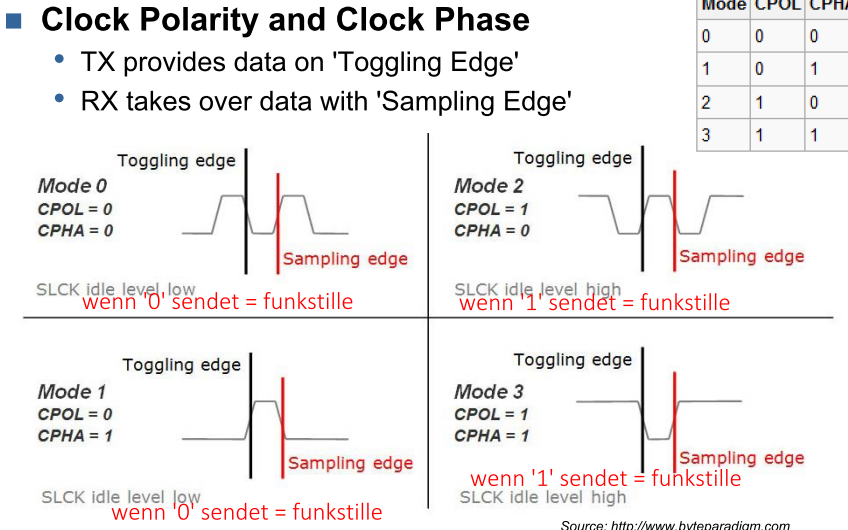
corresponding GPIOx\_OSPEEDR register bits whatever the I/O direction)

GPIOx\_PUPDR RM 8.4.4, pg. 280

- pull-up/pull-down independent of programmed I/O direction





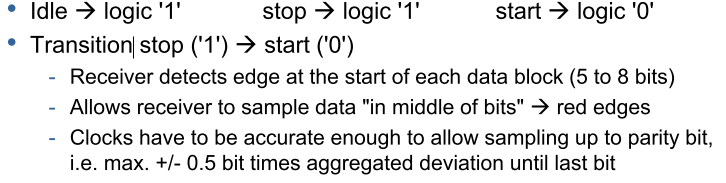


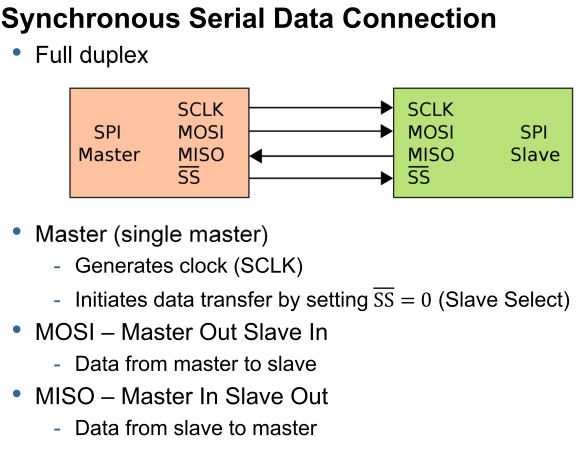
**SPI – Serial Peripheral Interface**

**Serial bus for on-board connections:** Used for short distance comm.

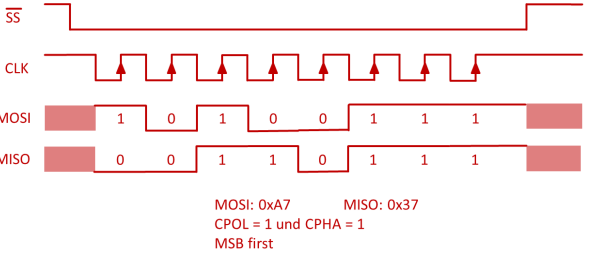
**Connects microcontroller and external devices:** Sensors, A/D converters, displays, flash memories, codecs**,** IOs, Real Time Clocks (RTC), wireless transceivers **Synchronous:** Master distributes the clock to slaves

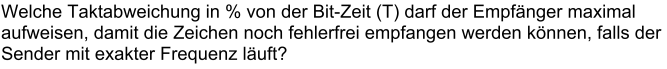
**Compared to a parallel bus:** Saves board areaLowers pin count on both chips (TX and RX)  smaller, low-cost**,** Simplifies EMC (Electromagnetic compatibility)

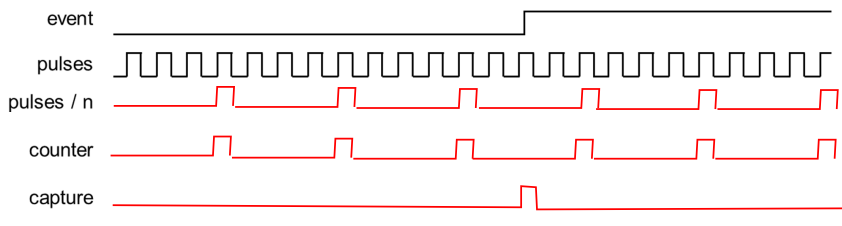
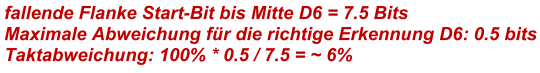


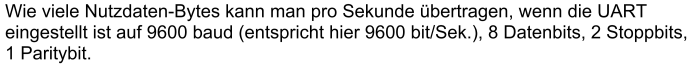




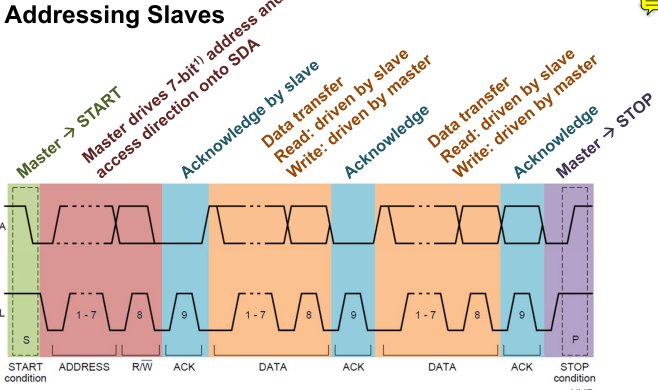


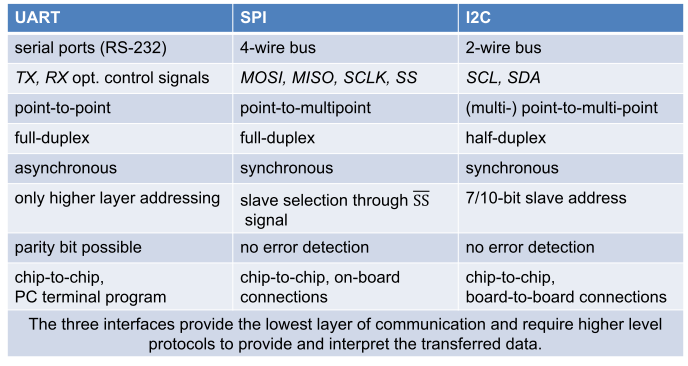
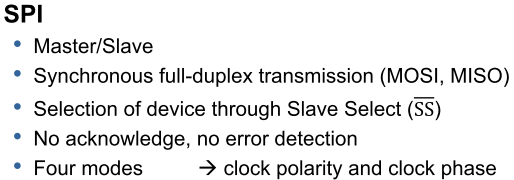


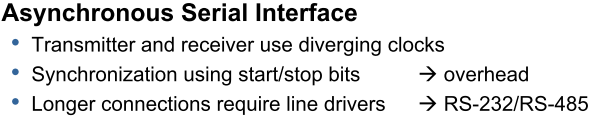






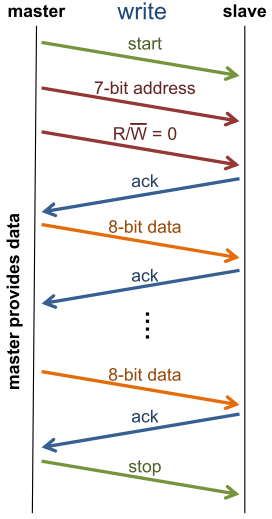
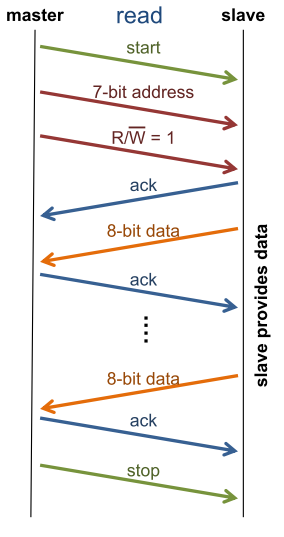
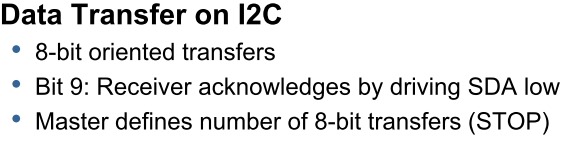


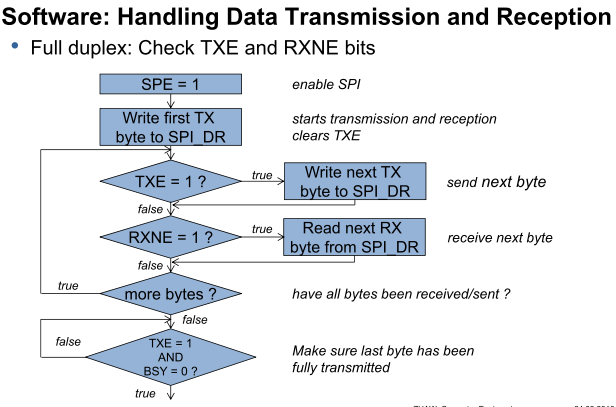


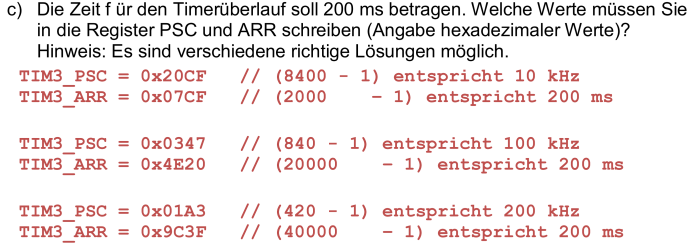


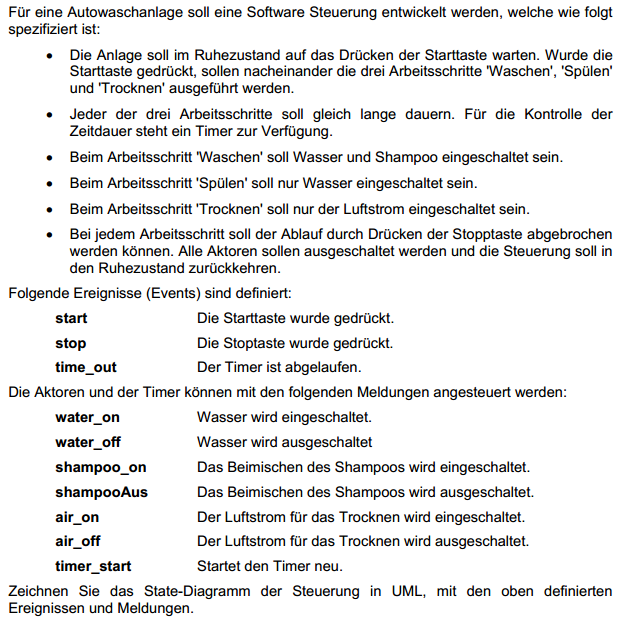
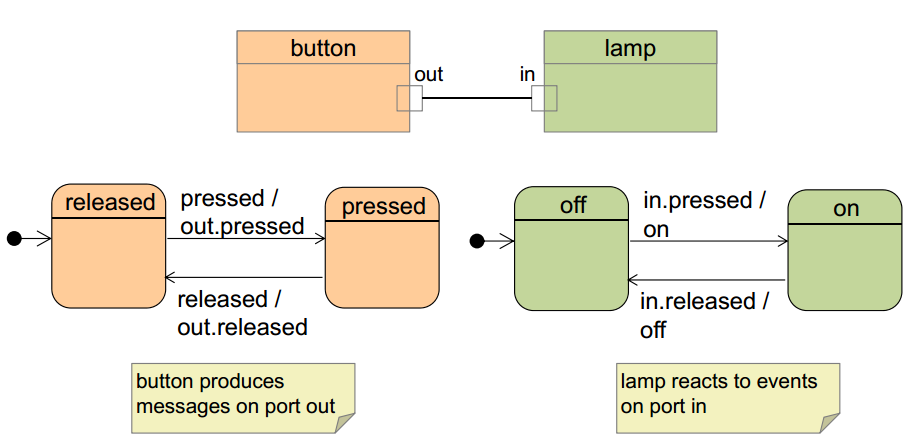
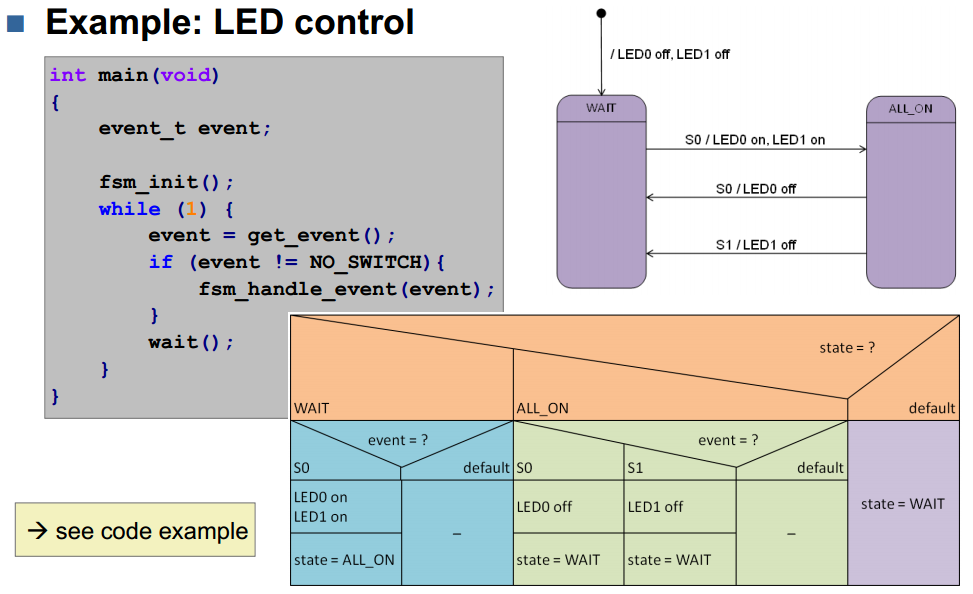
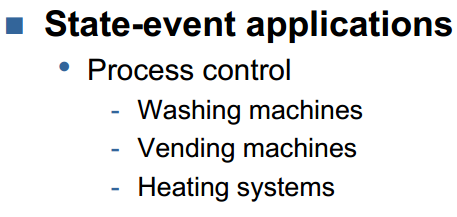
**I 2 C**

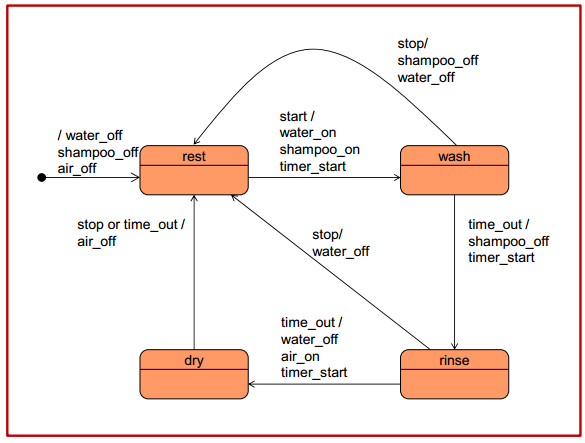
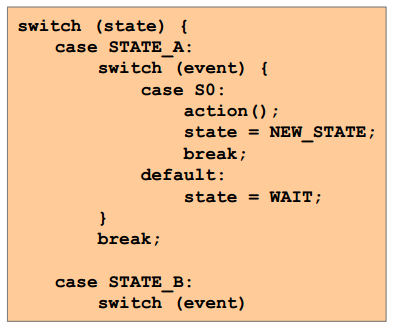
Synchronous half-duplex transmission (SCL, SDA), 7-bit slave addresses

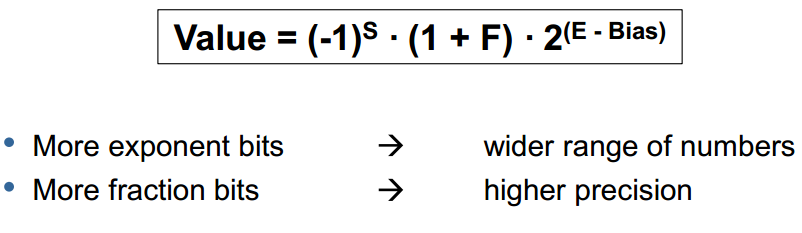


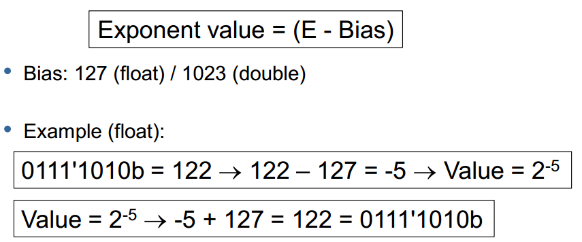


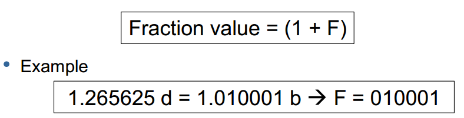
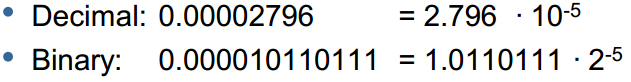


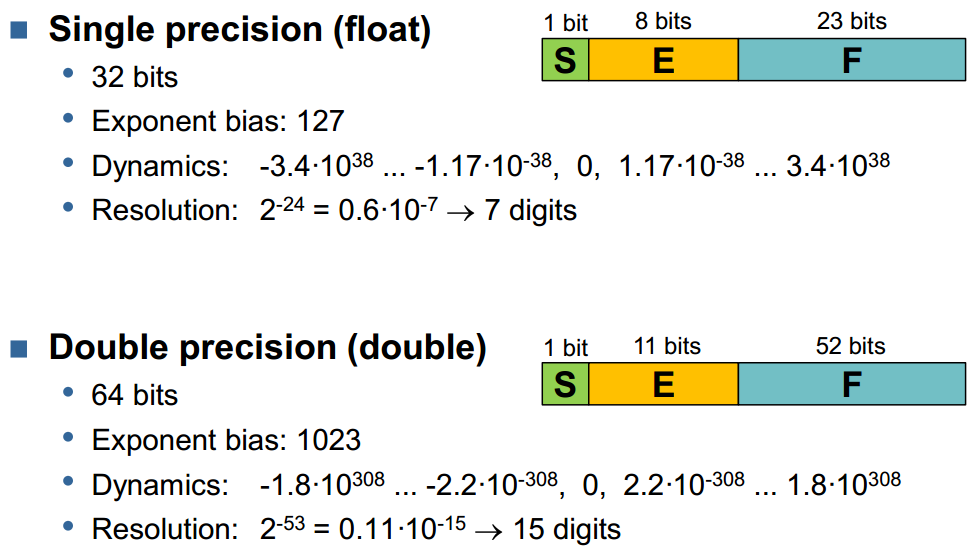


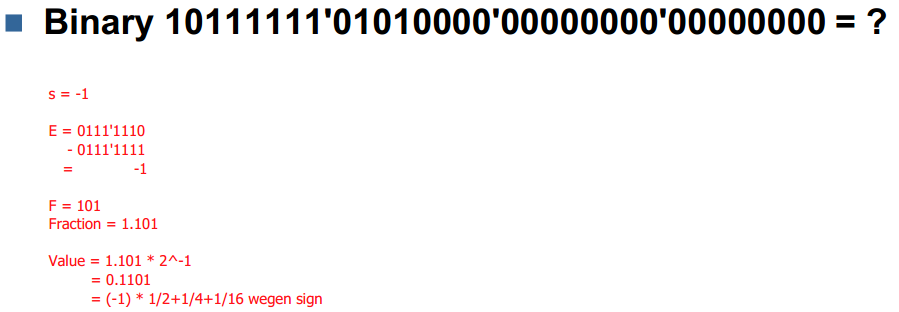


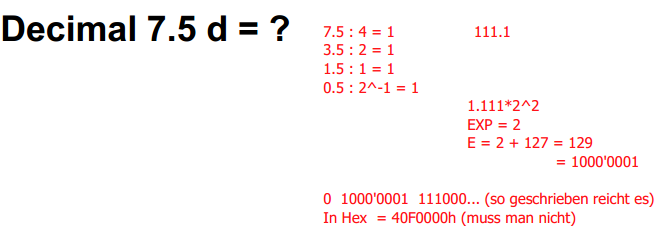


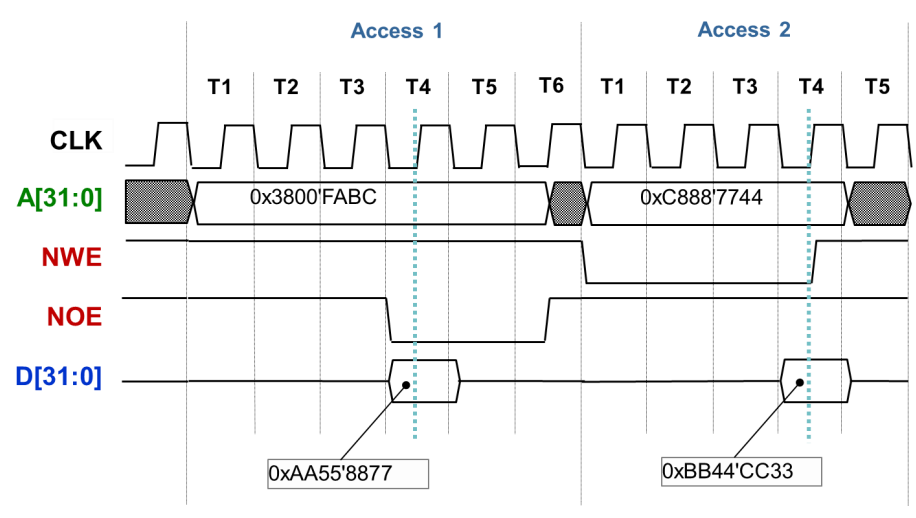
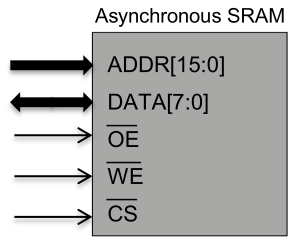
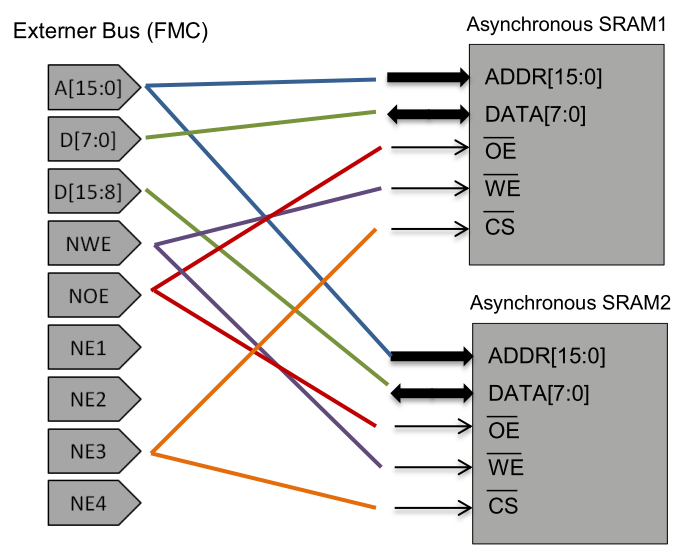






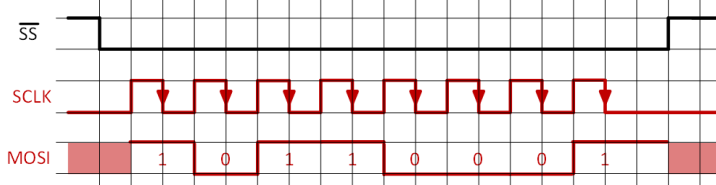






Ein Prozessor sendet über SPI das Byte 0x8D. Die Schnittstelle ist wie folgt konfiguriert: Mode 1, d.h. CPOL = 0 und CPHA = 1

LSB first



Was ist die Grösse y des Bausteines in KBytes ( y K x 8bit) ? **y = 2^16 = 64 KBytes**

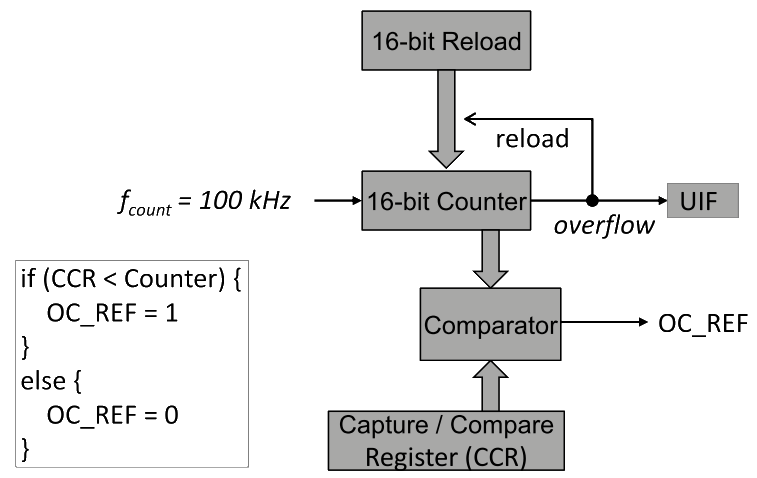


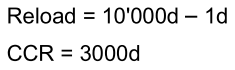
Mittels I²C soll ein Baustein zum Lesen adressiert werden. Die 7-Bit Adresse lautet 0x56. Zeichnen Sie die übertragenen Signale vom Start bis zum Acknowledge auf.



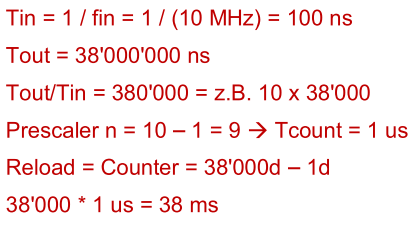
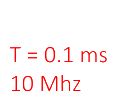
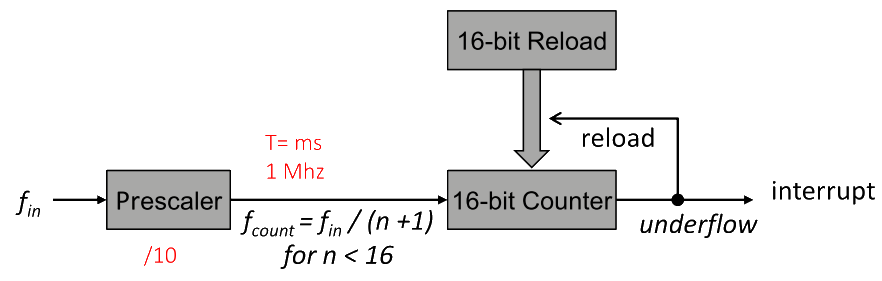


Nach schribzugriff





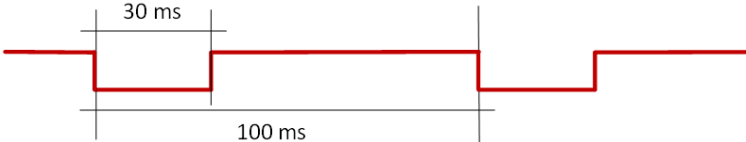
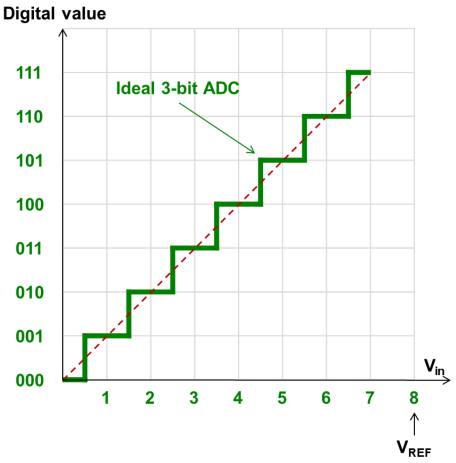
Die Eingangsfrequenz f in beträgt 10 MHz. Wie müssen die Register initialisiert werden, damit periodisch alle 38 ms ein Interrupt ausgelöst wird.





Gegeben ist ein 3-bit ADC. Die Referenzspannung VREF ist auf 8V festgelegt.

a) Nehmen Sie an, der ADC ist ,,idea|“. Zeichnen Sie die Ubertragungsfunktion!



In welchem Spannungsbereich (in V) bewegt sich der Quant-isierungsfehler?

1LSB =vREF/2“ =sv/2=\*= 1v

Quantisierungsfehler:

+/- 0.5 LSB = +/- 0.5V

Geben Sie an, wie -4.75d im Single Precision-Format nach IEEE Standard 754/ 854 abgelegt wird. lhr Lésungsweg muss nachvollziehbar sein.

Dezimal -> Binäir: -4.75d = -100.11b

Normalisieren: 100.11b = 1.0011b \* 22

Mantisse: 0011b

Exponent: E = 2d + 127d = 129d = 1000‘0001b

Sign: -4.75<0 -> V = 1

Packen: 11000000‘10011000‘00000000‘00000000

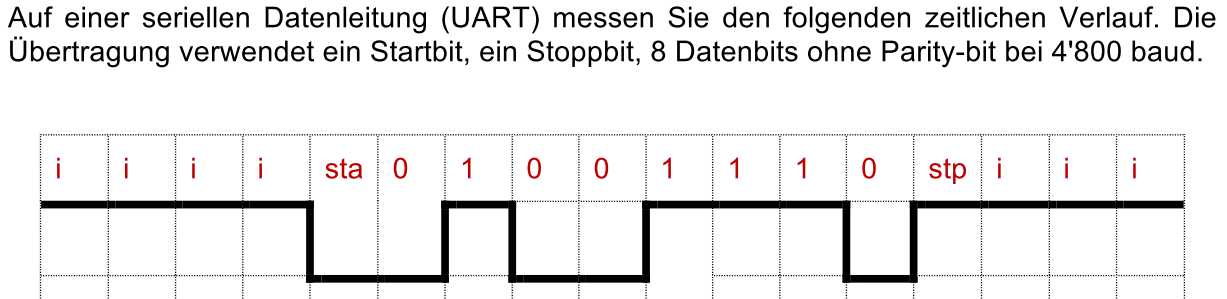
Hex: 0xC0980000

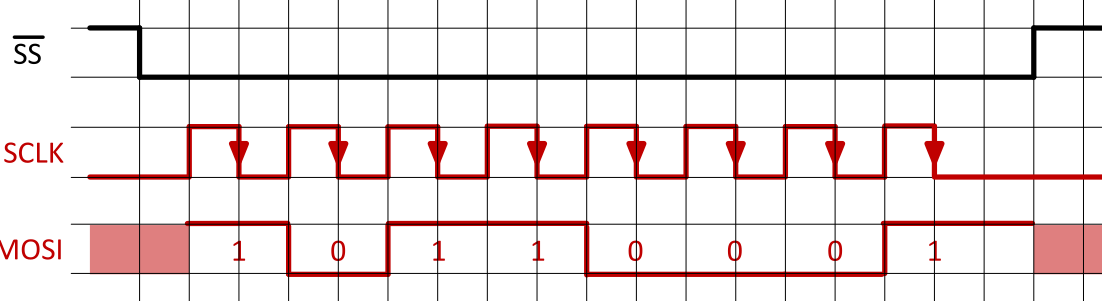
Gegeben ist ein realer 3-bit ADC. Er hat keinen Offsetfehler (offset error = O LSB). Ab einer Spannung von 5V gibt der ADC den digitalen Wert von ,,111“ aus. Wie gross ist der Verstarkungsfehler (Gain error)? Der Losungsweg muss nachvollziehbar sein.

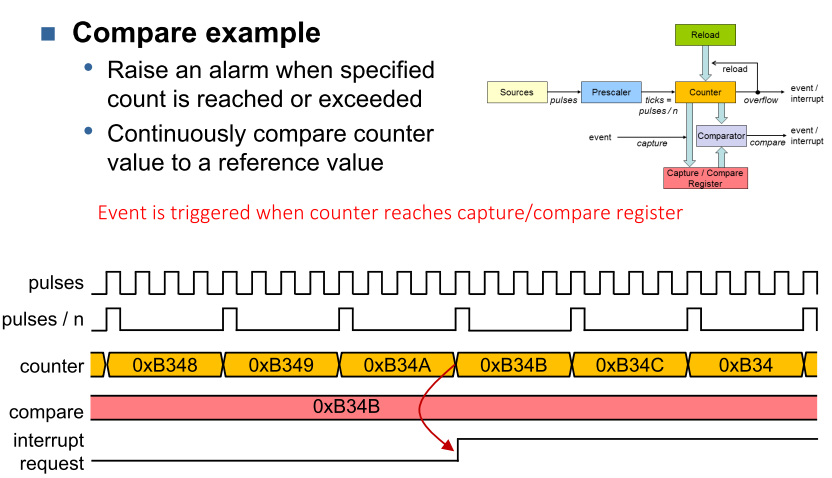
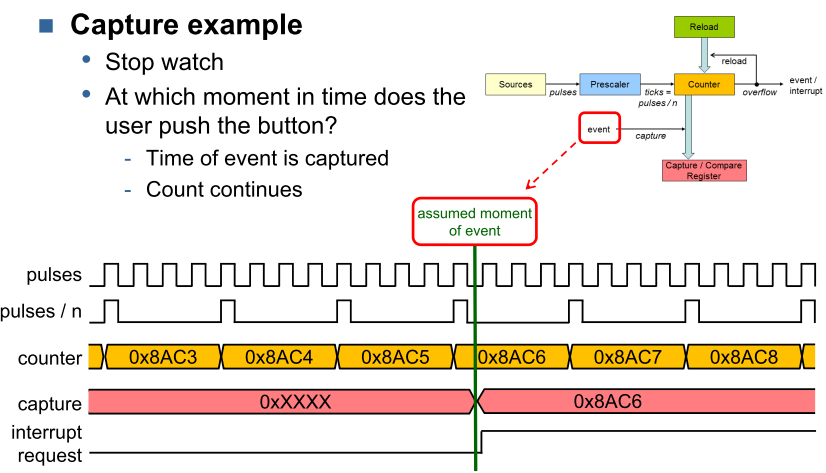
Full scale range FSR = VREF -1 LSB = 8V — 1V = 7V

111 sollte bei 6.5V erreioht werden (siehe Ubertragungsfunktion).

-> Gain error = 1.5V = 1.5LSB





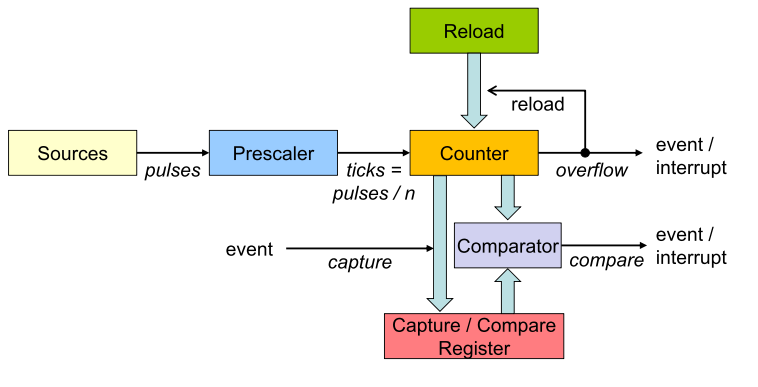
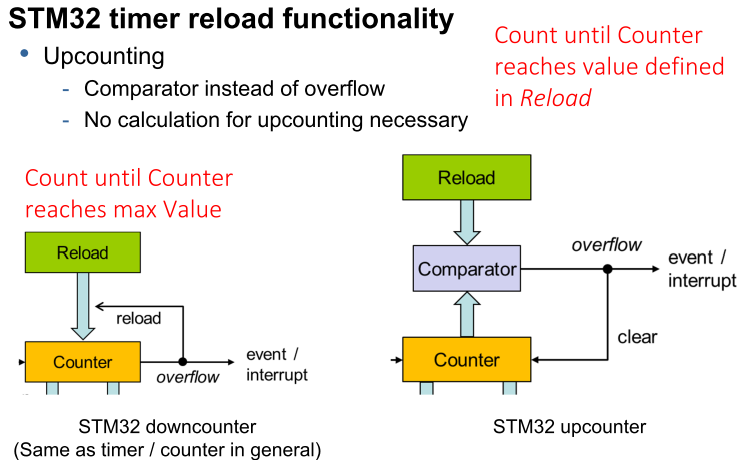


**Capture:**

Bei einem Event wird der lnhalt des Counter Registers in das Capture / Compare Register kopiert. Der Counter I läuft weiter.

**Compare:**

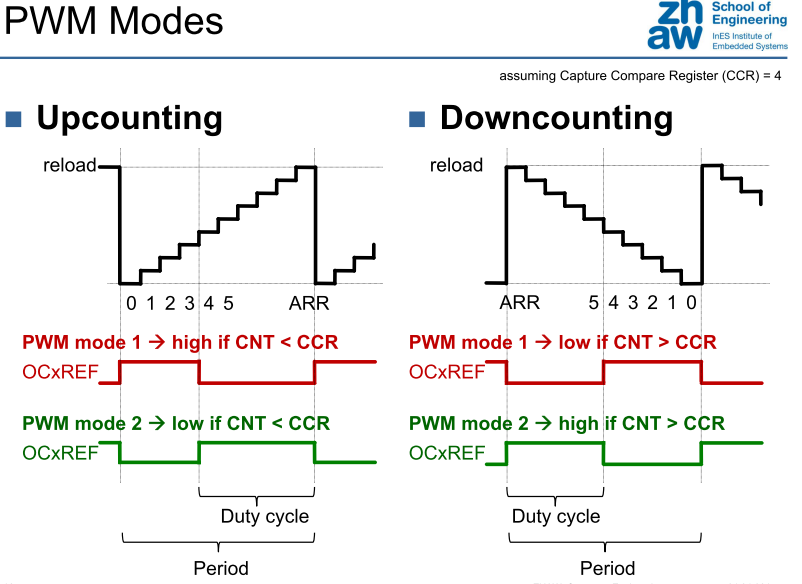
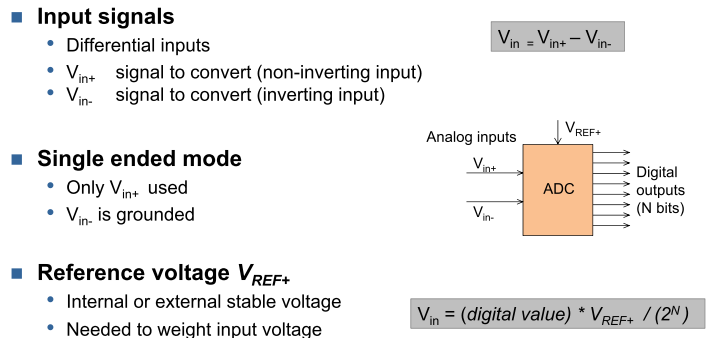
Sobald der Counter den Wert des Capture / Compare Register erreicht hat, wird ein Event oder ein Interrupt ausgelost. Der Counter Iäuft weiter.

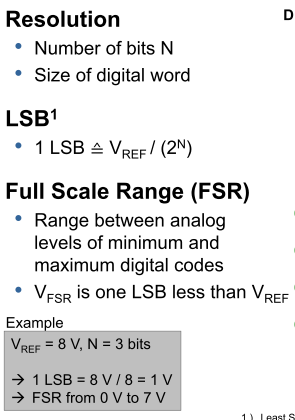




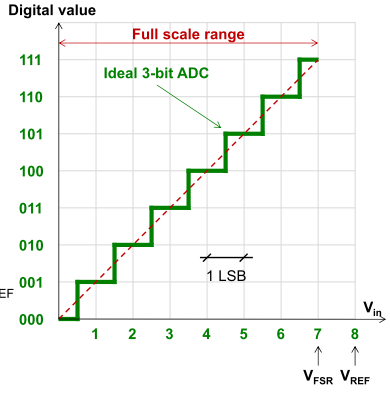
**Programming cookbook PMW**

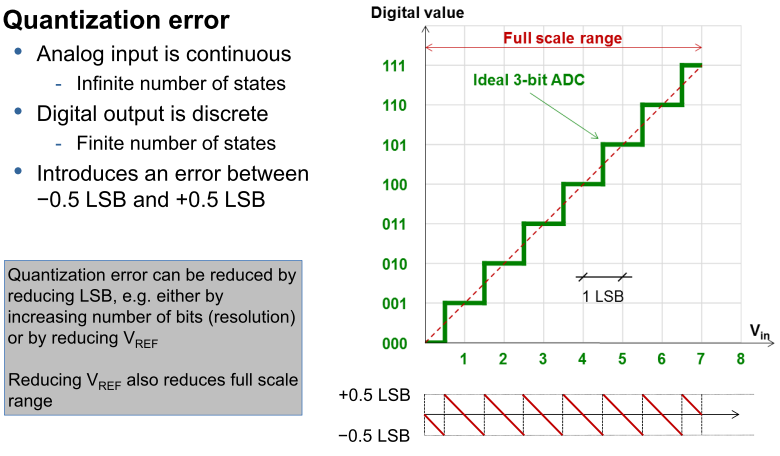
**1.** Select the counter clock (internal, external, prescaler) **2.** Write desired data in the TlMx\_ARR and TlMx\_CCRx registers **3.** Set CCXIE and/or CCXDE bits if an interrupt and/or a DMA request is to be generated (both in TlMx\_DlER register) **4.** Select the output mode (registers CCMRX / CCER) **5.** Enable counter by setting the CEN bit in the TlMx\_CR1 register

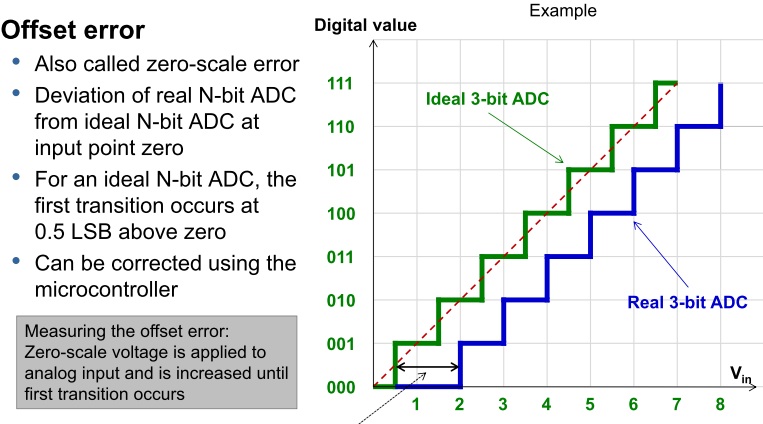




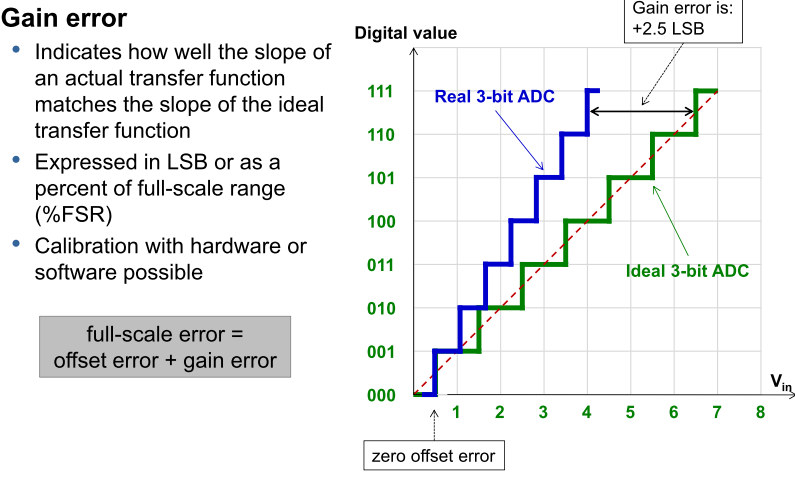


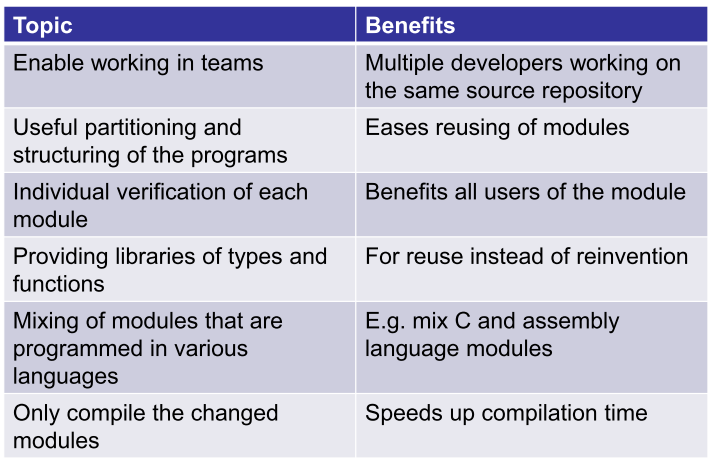
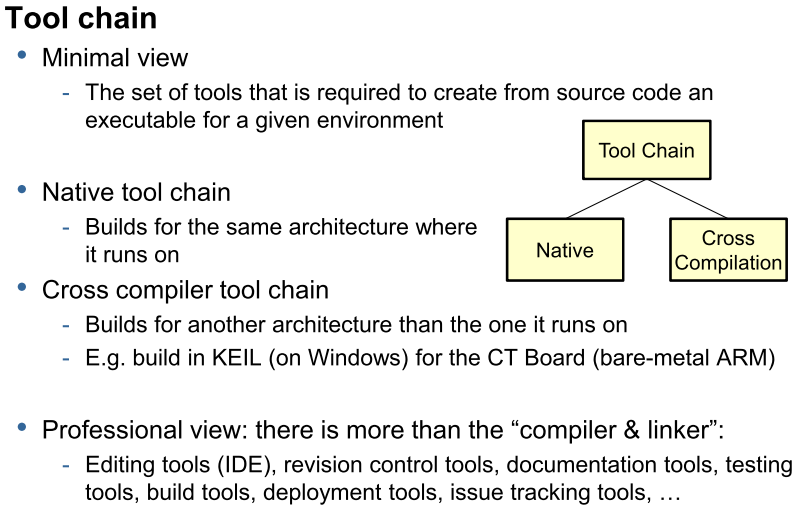


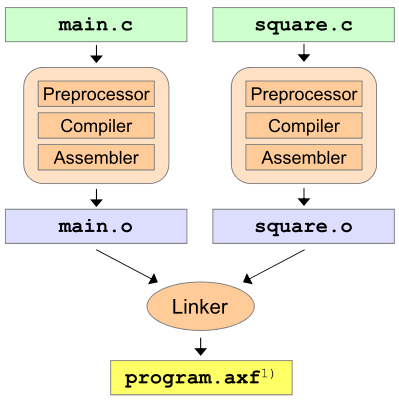


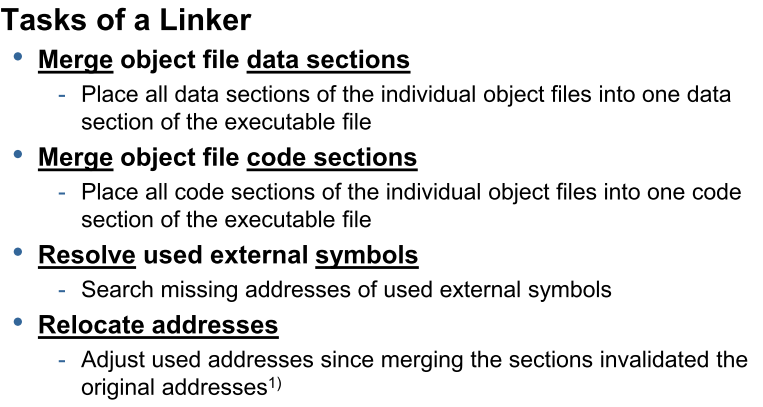
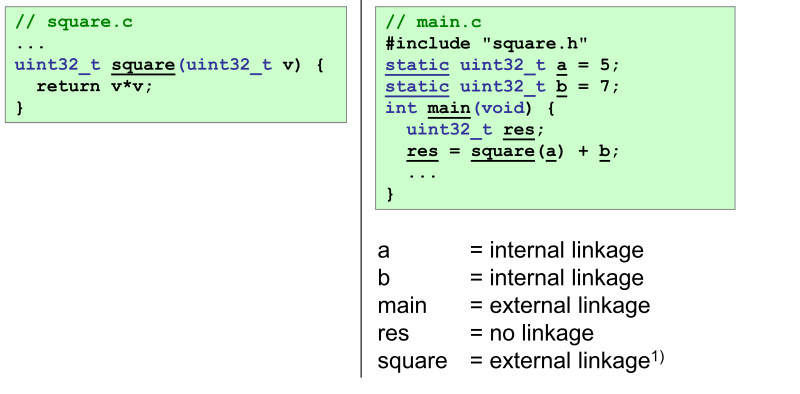


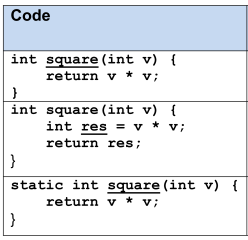






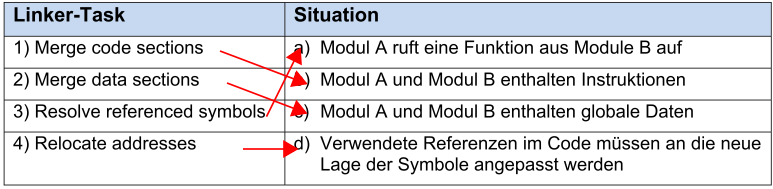




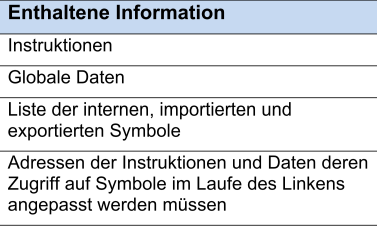
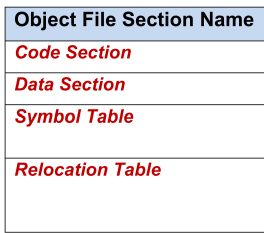












Quantifizieren Sie den Einfluss des Interrupts auf das System. D.h. welchen Anteil in Prozent der Gesamtrechenzeit verbringt das System mit der Behandlung der Interrupts?

lnterruptfrequenz = (16 kbit/s) / 32 bit = 500 Hz

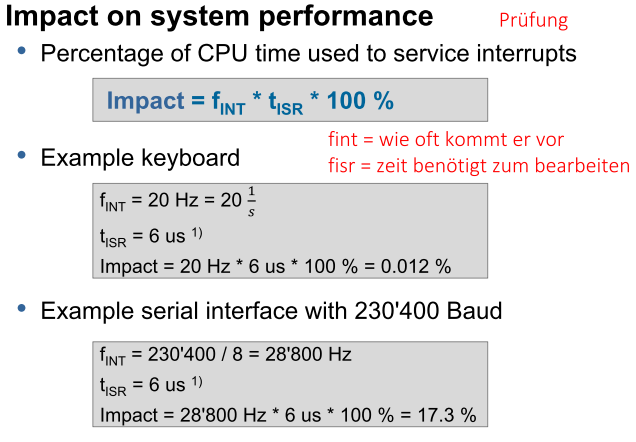
interrupt service time = 100 \* 1/(1 MHz) = 100 us

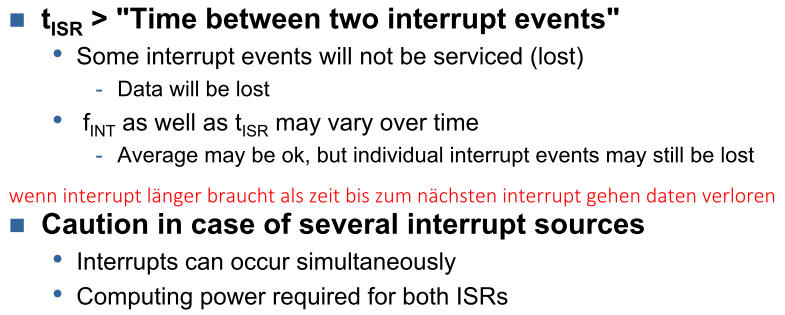
Impact = lnterruptfrequenz \* interrupt service time \* 100 % =500Hz\*100us\*100%=5%

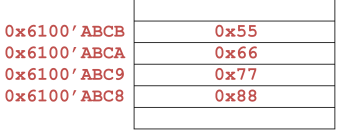
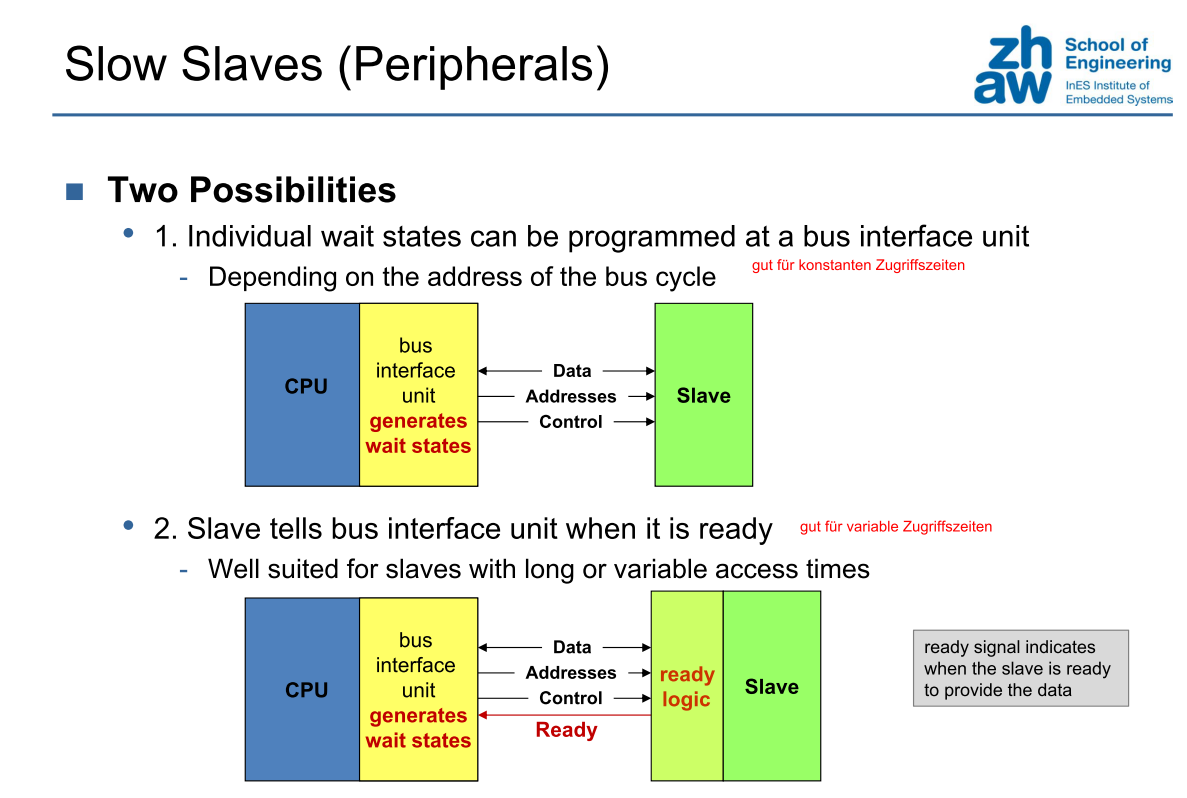
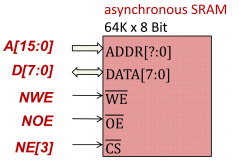
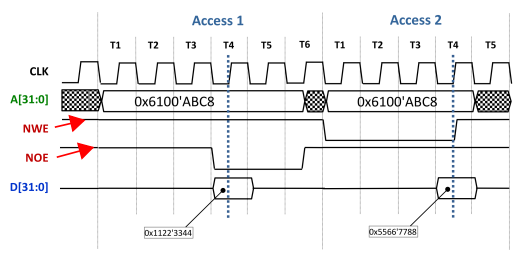
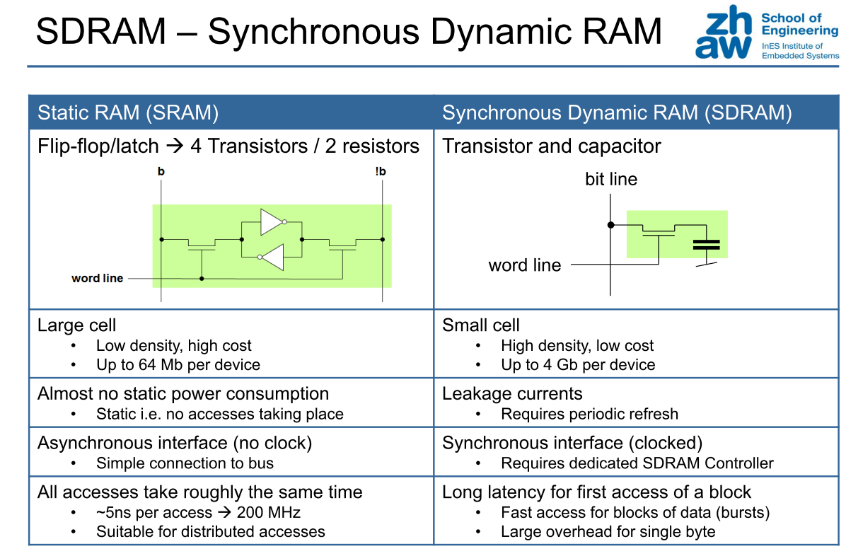
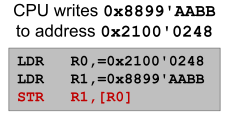
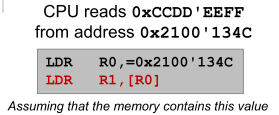
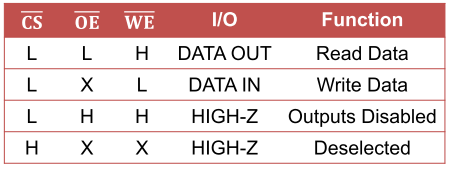
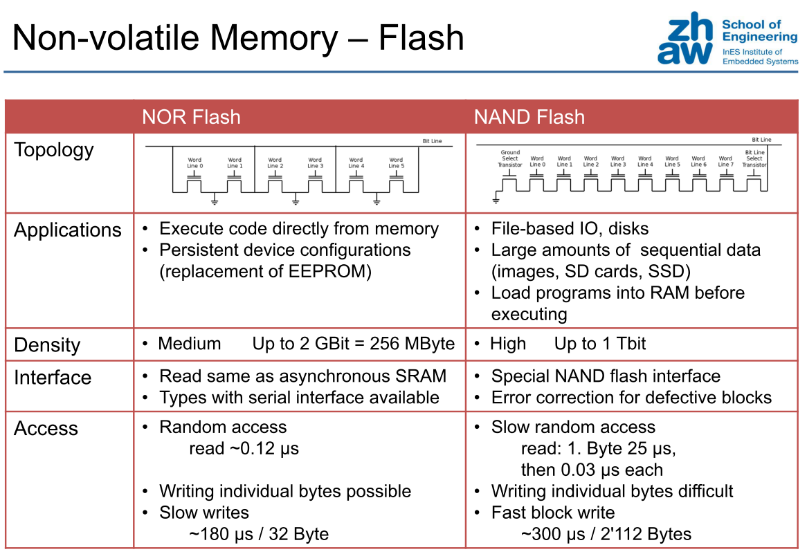
Bei welcher Datenrate der Schnittstelle wiirde der Prozessor 100% der Rechenzeit mit der Behandlung von Interrupts verbringen?

(X / 32 bit)\*1OO µs \*100 % =1OO % ->

X = 32 \* (1/100) Mbit/s = 320 kBit/s







Unter wie vielen 64KByte Adressblocken kann auf den Baustein zugegriffen werden?

A[25:16] -> 10 Adresslinien -> 2^10 = 1024 Adressblocke: 0X68XX'0000, 0X69XX'0000, 0x6AXX'0000, 0X6BXX'0000

Wie viele Adresspins benotigt der Baustein?

64K = 2"’ a 16 Adresspins a ADDR[15:0]

Lesen Sie den Wert eines 8-bit Control Registers an der Adresse 0x6100 ‘0007 in eine von lhnen zu definierende Variable ein.

#define M¥\_BYTE\_REG (\*((volatile uint8\_t \*)(0x61000007)))  
uint8\_t my\_var;  
my\_yar = M¥\_BYTE\_REG;

Bits eines 16-Bit Control Registers an Adresse 0x6100 ‘0008 auf ,1‘.

#define M¥\_HALFWORD\_REG (\*((volatile uint16\_t \*)(0x61000008))) MY\_HALFWORD\_REG = OXFFFF;

Warten Sie in einer Schleife, bis Bit 15 im 32-bit Control Register an der Adresse Ox6100 ‘OOOC auf ,1‘ gesetzt ist.

#define M¥;WORD\_REG (\*((volatile uint32\_t \*)(0x6100000C)))  
while(! (MY\_WORD\_REG & 0xOO008000)){}

Setzen Sie Bit 16 im Control Register an Adresse Ox61OO ‘0010 auf ,1‘ ohne die anderen Bits des Registers zu verandern.

#define MY\_WORD\_REG2 (\*((volatile uint32\_t \*> (Ox6l0O00l0)))  
MY\_WORD\_REG2 |= 0x00010000;

**Bus Timing Options**

Synchronous: Master and slaves use a common clock 1), Clock edges control bus transfer on both sides, Used by almost all on-chip busses, Off-chip: DDR and synchronous RAM

Asynchronous: Slaves have no access to the clock of the master Control signals carry timing information to allow synchronization, Widely used for low data-rate off-chip memories ->parallel flash memories and asynchronous RAM

**Address lines** Unidirectional: From master to slave, Number of lines -> yields size of address space, Cortex-M 32 parallel address lines, 2 32 = 4 Giga addresses 0x0000'0000 – 0xFFFF'FFFF

**Data lines** 8, 16, 32 or 64 parallel lines of data**,** bidirectional (read/write)

**Control signals** Control read/write direction**,** Provide timing information

genau unter der Adresse 0x28 angesprochen  
select = A[5] & !A[4] & A[3] & !A[2] & !A[1] & !A[O]

Unter welchen Adressen (in Hex) kann das Control Register angesprochen werden,wenn nur die oberen 4 Adressleitungen wie folgt dekodiert werden: *select = A[5] & A[4] & !A[3] & !A[2]*