Team: RAZAVUS

Team Members

1) Ashutosh Chakravarty
2) Manigandan D
3) Karan Gajanan Mali
4) N Nishchit
5) Vaibhav Kumar Gupta

Academic Experience:

- Three of us are Recent Graduates (B.E Class of 2025, 2 in EE and 1 in ECE)
- 2 of us are in their pre-final year in Undergrad (EE)

Work Experience: Nil (in Analog domain)

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Project Title : VGA (Variable gain Amplifier for MOSBius)

- **Goals:** To Design a simple digitally controlled VGA with Two Stage Op-amps and TG switches

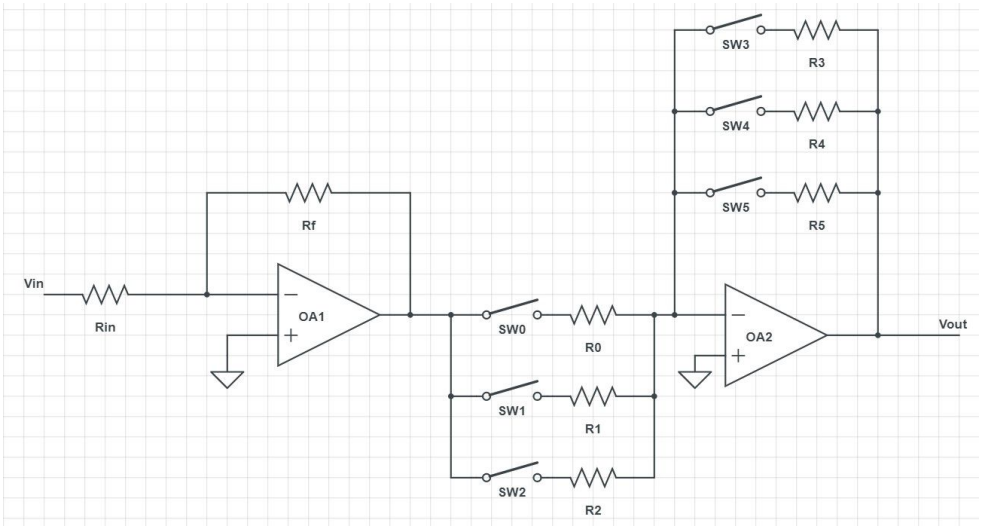

Image taken from https://repository.rit.edu/theses/11126/

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- **Specifications Currently Targeted:** (These are still debatable estimates , would like to have your opinion)

Gain Range	0 to 60 dB
Bandwidth	300 MHz
Linearity(THD)	< -50 dB (~0.316%)
Noise Figure	< 5dB
Input-Referred Noise	< 10 nV/√Hz
Control Method	Digital (Analog -> Using external circuits)
Power Consumption	< 20mW

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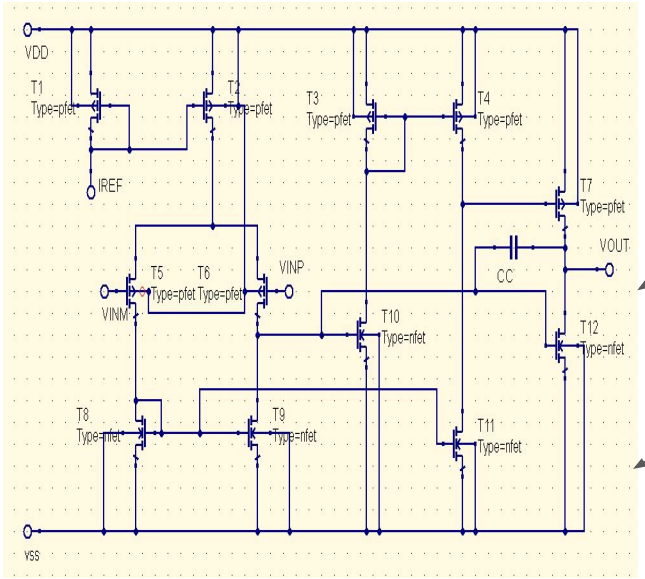
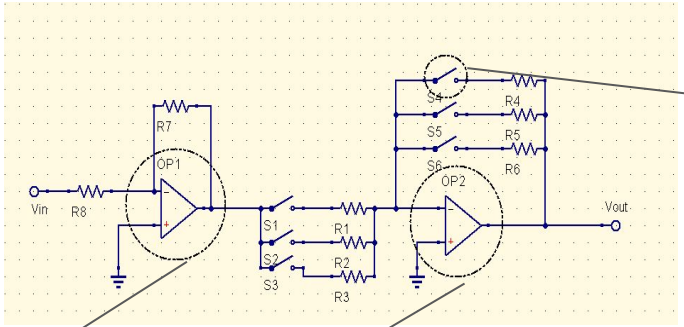
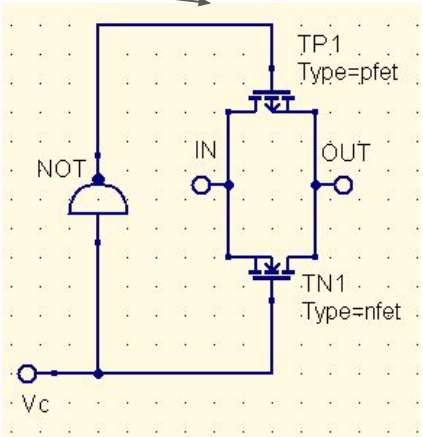
- **Design - High Level Proposal:** We plan to design a digitally controlled VGA using Transmission gate as switches and Resistor ladder for feedback. The op-amp is a two stage with first being differential stage and second being class AB amplifier.







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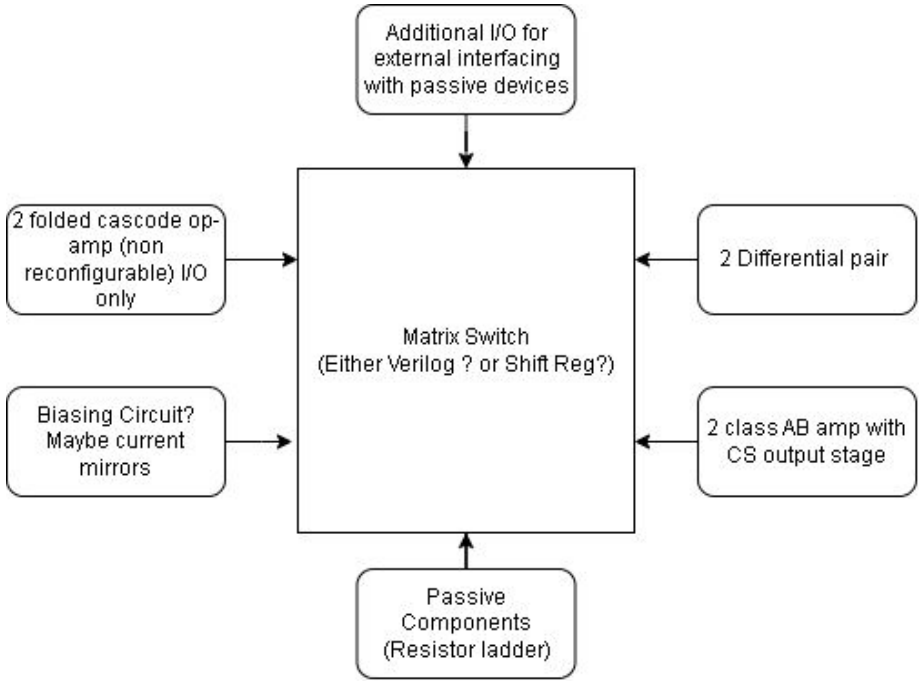
- **Design block Diagram :**



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Expected Timeline:

	Week 29	Week 30	Week 31	Week 32	Week 33	Week 34	Week 35	Week 36	Week 37	Week 38	Week 39	Week 40
Schematic	We expect to complete schematic Review and incorporate any suggestions											
Simulation				Block level Schematic simulations to be performed, convergence expectred								
Layout and Integration							Block level layout design to be completed with final top level integration					
Verification										Final Verification with PEX and characterization		

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Work Distribution:

	Week 29	Week 30	Week 31	Week 32	Week 33	Week 34	Week 35	Week 36	Week 37	Week 38	Week 39	Week 40
Ashutosh	Op-amp differential pair Schematic and Verification-W29 TG Design-W30 Top level Sch Integration-W31			Full block level and top level sims/ suggestions by prof Kinget-W32 Convergence of sims-W33 Layout guidelines-W34			TBD based on performance of previous weeks			TBD based on performance of previous weeks		
Manigandan	Op-amp differential pair Schematic and Verification-W29 Resistor Sizing-W30 Top level sch integration-W31			Full block level and top level sims/ suggestions by prof Kinget-W32 Convergence of sims-W33 Passive Layout -W34			TBD based on performance of previous weeks			TBD based on performance of previous weeks		
Karan	Op-amp Second stage schematic and verification-W29 Switch Matrix Design-W30 Top level sch Integration-W31			Full block level and top level sims/ suggestions by prof Kinget-W32 Convergence of sims-W33 Layout guidelines-W34			TBD based on performance of previous weeks			TBD based on performance of previous weeks		
Nischit	Op-amp Second stage schematic and verification-W29 TG Design-W30 Top level sch integration-W31			Full block level and top level sims/ suggestions by prof Kinget-W32 Convergence of sims-W33 Layout guidelines-W34			TBD based on performance of previous weeks			TBD based on performance of previous weeks		
Vaibhav	Op-amp differential pair Schematic and Verification-W29 Resistor Sizing-W30 Top level sch integration-W31			Full block level and top level sims/ suggestions by prof Kinget-W32 Convergence of sims-W33 Passive Layout -W34			TBD based on performance of previous weeks			TBD based on performance of previous weeks		

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- **Application:**

1) AGC for RFE
2) For basic circuits in UG level Analog IC design class like Differentiator , Integrator , Instrumentation Amplifier etc.
3) For Testing the circuits we will be using the oscilloscopes and signal generators in the lab and for simulation we can do some test circuits.

- **References:**

1. https://repository.rit.edu/theses/11126/
2. http://dx.doi.org/10.29292/jics.v17i1.583

- **Questions , Doubts ??**

1. What do you think about the proposal is it doable in stipulated time?
2. What should we be vary of considering the parasitics i.e pad frame caps etc?
3. Given a simpler configuration we might compromise on the area so do you think this can still be implemented?
4. Any suggestions that we should incorporate?

- Video Presentation: Link
- Github : Link