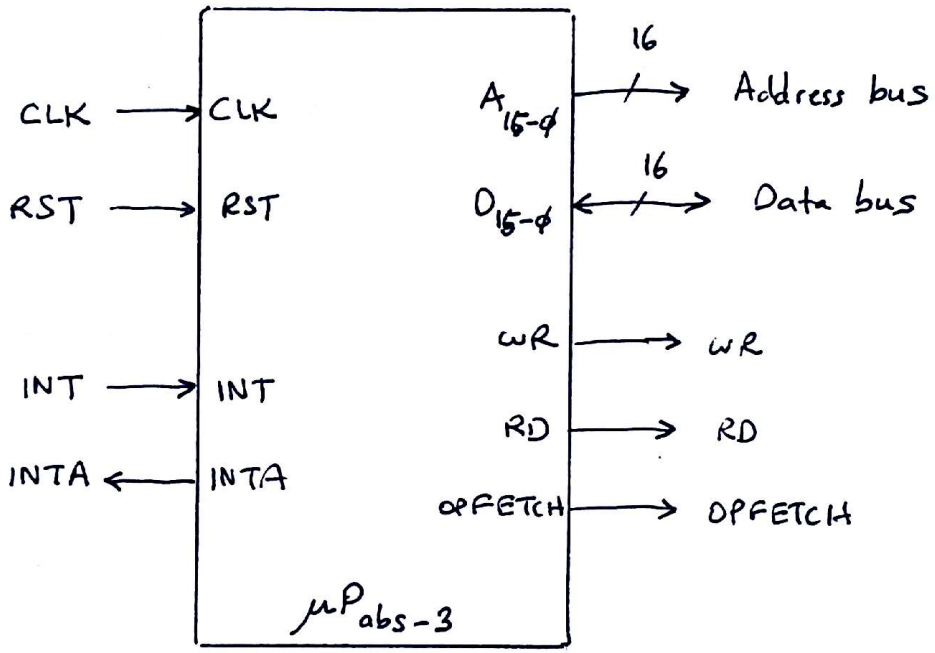
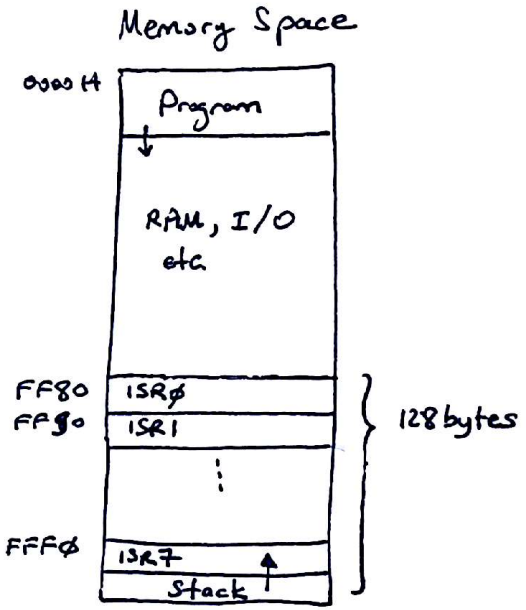
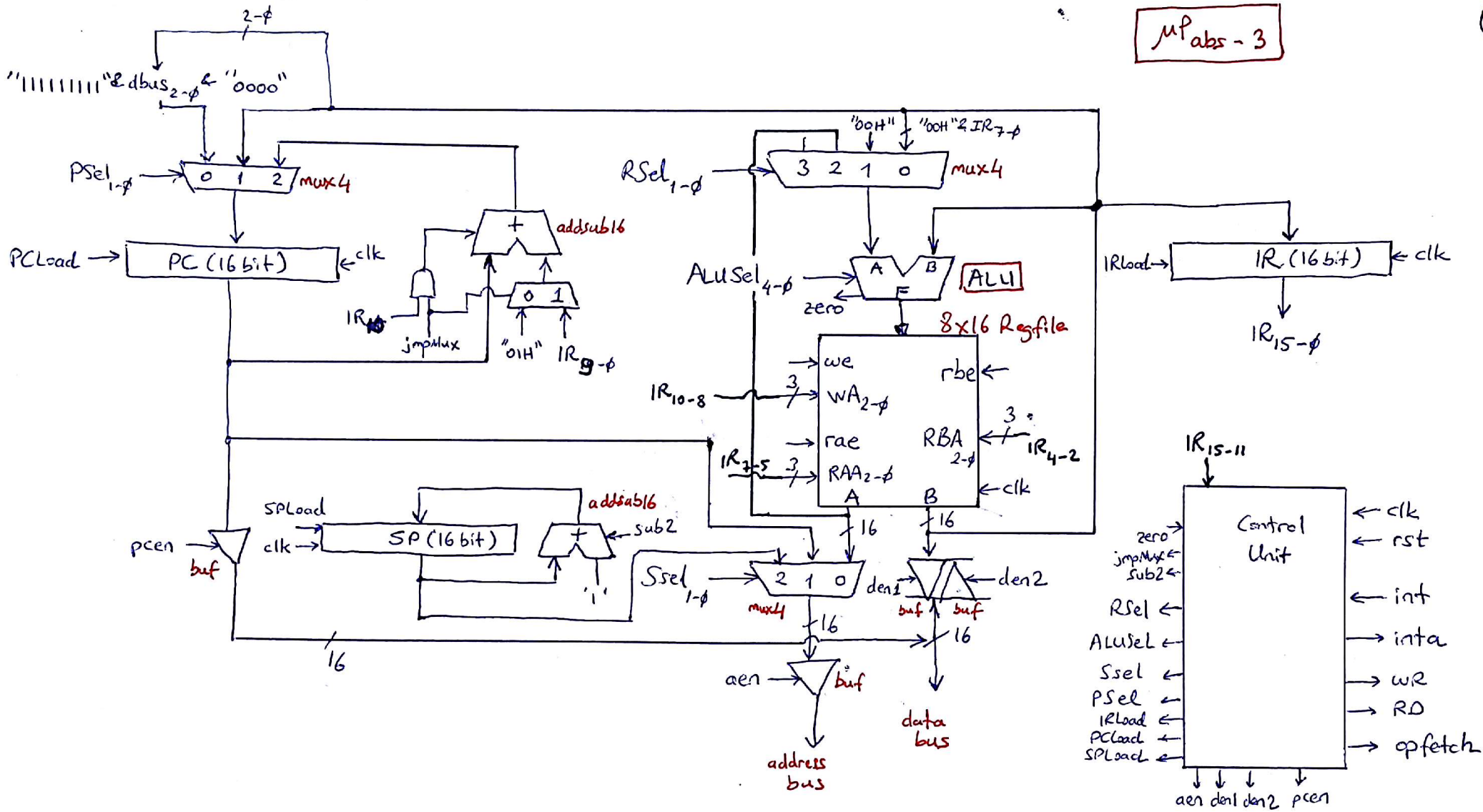
μP_{abs-3} Microprocessor



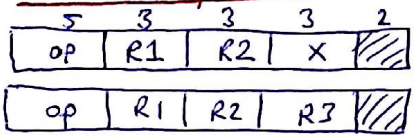
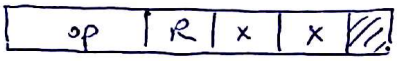
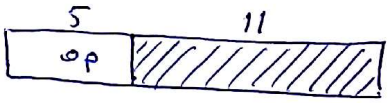
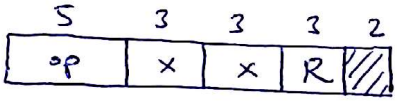
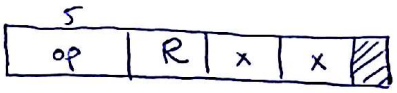
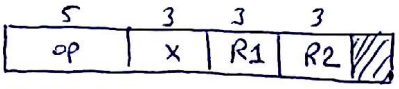
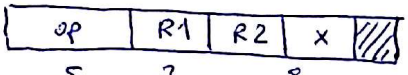
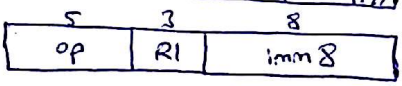
- 16 bit CPU
- 8 internal registers (GP)
- 64k memory space
- Stack Pointer register
- Supports 8 ISRs.



μP_{abs-3}



μP_{abs-3} Instructions

Opcode	command	explanation	Instruction format
0	mov R1, R2	$R1 \leftarrow R_2$	
1	add R1, R2, R3	$R1 \leftarrow R_2 + R_3$	
2	sub		
3	and	similarly	similarly
4	or		
5	not R	$R \leftarrow$ not R	
6	inc R	$R \leftarrow R+1$	
7	dec R	$R \leftarrow R-1$	
8	sr R	shift right R	
9	sl R	shift left R	
10	rr R	rotate right R	
11	clear R	$R \leftarrow \emptyset\emptyset\emptyset\emptyset H$	
12	jmp add11	PC ← PC + add11	
13	jz add11	if(zero) PC ← PC + add11	
14	jnz add11	if(!zero) PC ← PC + add11	jumps ∓ 1023 locations.
15	call add11	push PC ; PC ← PC + add11	
16	ret	pop PC ≡ SP ← SP+1 ; PC ← mem[PC];	
17	nop	no operation	
18	halt	halt processor	
19	push R	mem[SP] ← R ; SP ← SP − 1	
20	pop R	SP ← SP + 1 ; R ← mem[SP] ;	
21	write @R1, R2	mem[R1] ← R2	
22	read R1, @R2	R1 ← mem[R2]	
23	movi R, imm8	R ← imm8	

add11 : 11-bit signed integer
R : 16-bit register
imm8 : 8-bit immediate value
mem[65536] : 64 k-byte external memory
PC : Program Counter register
SP : Stack Pointer register
zero : zero flag

④ INTERRUPT CYCLE

③ WRITE CYCLE

② READ CYCLE

① FETCH CYCLE

* Minimum Configuration with Program Memory (1024 x 16 bit ROM)