A NOVEL APPROACH FOR DESIGN OF HIGH SPEED LOW POWER MULTIPLIER WITH REVERSIBLE LOGIC USING VEDIC MULTIPLICATION

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***Abstract*— The development of multipliers with improved properties is the main goal of this research, with a particular emphasis on speed, power consumption, and lower range complexity. The strategy makes use of reversible logic, a notion that is being used more and more in a variety of industries, including quantum circuits, multipliers, Reversible resonance, low power CMOS circuit, and optical data processing and Vedic mathematics are combined in this work. Specifically, well-known logical ideas the double key, kogge stone adder, reversible full and half adders are used in the suggested multipliers. The multipliers' effectiveness and performance are enhanced by these concepts. The research classifies multiple multipliers according to reversible logic circuits in order to guarantee better performance. The Xilinx VIVADO technique is then used to simulate and synthesize the intended multipliers. We plan to use Modified Full Adder [MFA] and Synthesis Based Clock Gating to our proposed Circuit after carefully examining the results of these simulations to conform and understand the performance and efficacy of the proposed multiplier designs.**

Keywords*— *Vedic multiplier, Reversible logic, Full and Half Adders ,Vedic mathematics MFA, Reversible gates, RCA

I. INTRODUCTION

The foundation of Vedic mathematics, an old Indian system, is the mathematical equations included in the Vedas. By using 16 sutras and 16 upa sutras from the old Indian texts, especially the Atharva Veda, Sri Bharati Krsna Tirtha was able to rebuild Vedic mathematics. Among these, Urdhva Tiryakbhayam, Nikhilam Sutram, and Anurupye are noteworthy, with Urdhva Tiryakbhayam being the most effective.

Its capacity to streamline intricate computations thatare part and parcel of traditional mathematics is what makes Vedic mathematics so fundamental. According to the claims made, the 16 sutras and their applications are grounded in natural principles that correspond with the functioning of the human mind. Particularly in digital signal processing (DSP) blocks, this simplicity is thought to speed up multiplications and enable quicker computing speeds. As it wraps up, the chapter emphasises how multidisciplinary Vedic mathematics is, pointing out how it may be applied to different engineering specialties and providing useful techniques.

An old Indian system of mathematics called Vedic mathematics forms the basis of a particular kind of multiplier referred to as a multiplier from the Vedas. The goal of the Vedic multiplier is to multiply numbers using mathematical formulas found in the Vedas. Reconstructing the 16 sutras and 16 upa sutras from the ancient Indian texts, especially the Atharva Veda, frequently requires specialized methods and algorithms.

An example of a multiplier circuit that draws inspiration from ancient Indian mathematical principles described in Vedic literature is called a Vedic multiplier. With the aid of a precise set of guidelines taken from Vedic mathematics, it is intended to carry out binary multiplication. The Vedic multiplier is renowned for being quick and effective in multiplying numbers.

Dividing the multiplication operation into smaller, more manageable parts is the fundamental structure of a Vedic multiplier.

Many principles are used to carry out the multiplication, such as the "Urdhva - Tiryakbhyam" method, which stands for "vertically and crosswise." The steps in creating a Vedic multiplier are summarised as follows:

The binary multiplier and multiplicand are partitioned into smaller sections.

1.1 Making Partial Products:

The multiplier and multiplicand's component bits are multiplied to create partial products.

1.2 Crosswise Addition of Partial Products:

In accordance with predetermined guidelines, the partial products are added crosswise.

A system of guidelines developed from Vedic mathematics is used to control carry propagation.

1.3 Complete Synopsis:

The ultimate product is then calculated by adding the results of the crosswise addition. The parallelism of the Vedic multiplier allows for the simultaneous generation and processing of several partial products, which is one of its benefits. When compared to certain conventional multiplication methods, this parallelism helps to speed up multiplication.

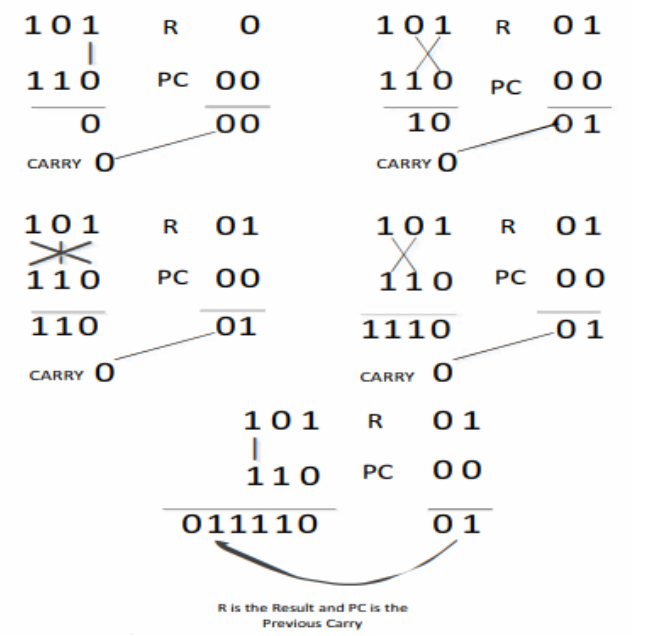


Fig. 1. URDHVA-TIRYAKBHAYAM ALGORITHM FOR BINARY MULTIPLICATION

The Vedic multiplier is often utilised for applications involving digital signal processing and hardware implementations where high-speed multiplication is crucial. While the Vedic multiplier has gained attention for its efficiency, its application potentially be influenced by the system's particular needs as well as the power, speed, and area trade-offs.

"Urdhva Tiryakbhayam," which means vertical and across, is one prominent Vedic multiplier that is referenced. This multiplier is recognized for its simplicity and efficiency in handling complex multiplication computations. The implementation of Vedic multipliers is believed to lead to faster multiplication operations, making them valuable in applications like digital signal processing (DSP). Additionally, some versions of Vedic multipliers are explored with reversible logic to reduce power dissipation, a crucial consideration in embedded systems. Overall, Vedic multipliers are promoted for their potential to simplify and expedite multiplication tasks in various computational applications.

Reversible logic is a computing design paradigm based on quantum mechanics principles, aiming to create computers with zero heat dissipation. The fundamental concept involves the how entropy and heat transfer are related, quantum particle probability, and quantum electrodynamics. Reversible computing relies on bijective devices with exactly the same amount of lines for input and output, ensuring predictability of future states and exploration of all possible states without heat dissipation. Reversible logic gates provide Accurate recovery of inputs from outputs is made possible by the inputs and outputs mapped exactly to one another. Quantum cost, gate, and garbage outputs are important parameters. count, and gate level in evaluating the efficiency and cost-effectiveness of reversible logic designs.

A unique class of digital logic gates known as reversible logic gates conducts operations so that the information from the input and output may be uniquely ascertained from one another. Reversible logic gates preserve information, which makes them valuable in applications such as emerging technologies, low-power computing and quantum computing. Compared to classical logic gates, which may lose information owing to irreversible operations. Reversible logic gates come in the following varieties.:

1.4 Toffoli Gate (CCNOT or Controlled-Controlled-NOT):

The Toffoli gate is a reversible gate having three inputs and three outputs. The target should both control bits be set to 1, the bit is flipped., else it stays unchanged. This is a controlled-NOT operation. Any classical computation can be stated using only Toffoli gates because they are ubiquitous for classical computing.

1.5 Fredkin Gate (CSWAP or Controlled-SWAP):

The Toffoli gate has three inputs and three outputs, making it a reversible gate. In the event that set both control bits to 1, the target bit flips., else it stays unchanged. This is a controlled-NOT operation.
Any classical computation can be stated using only Toffoli gates because they are ubiquitous for classical computing.

1.6 Gate of Peres:

Processing three inputs and three outputs and being reversible gate.
If both the first and second bits of control are set to 1, the third control bit will flip them; otherwise, the bits stay unchanged.

1.7 Feynman Gate:

A Feynman gate can be reversed given two inputs and two outputs reversed. With the additional requirement that the outputs be set to 1 if both inputs are 1, it executes an exclusive OR (XOR) operation.

Richard Feynman, a physicist who helped establish the ideas of quantum computing, is honored by the Feynman gate.

1.8 Controlled NOT (CNOT) Gate:

CNOT gates are frequently regarded as reversible gates in quantum computing.
Upon setting the control bit to 1, it flips the target bit; if not, the target bit remains unaltered.

1.9 SWAP Gate:

A two-input, two-output reversible gate is the SWAP gate. It switches the two input bits' values.
The fundamental components of reversible circuits are these gates. Particularly in the context of quantum computing and other advanced computing paradigms, the design of

reversible circuits is crucial for minimizing energy loss and guaranteeing the conservation of information.

Reversible logic circuits are subject to the following significant design limitations.

1. Fan-outs are not permitted with logic gates with reversals.

2. The smallest the reversible quantum cost logic circuits should be achieved.

3. It is possible to optimise the design to generate the fewest possible outputs of garbage.

4. Minimal constant input numbers are required for reversible logic circuits.

5. A minimum logic depth or number of gate levels must be used by the reversible logic circuits.

II. EARLIER WORK

Multipliers are essential in DSP calculations. Therefore, low power multipliers must be developed for modern DSP systems in order to lower power dissipation. Using the bypassing approach is one of the most effective techniques to lower power dissipation. Bypass multipliers get their name from the fact that the entire row, column, and/or diagonal array will be bypassed if a bit in the multiplier and/or multiplicand is zero. Applications exist for reversible logic, a more popular technology. in quantum calculations and low-power CMOS circuits. In this research, it is used to create two-dimensional bypass multiplier and column bypass multiplier. The input bit coefficients are the only factors that affect how any bypass multiplier component switches. These multipliers are used in FFT computing units for linear filtering, especially for zero padding where countless zeros will be present. When a bypass multiplier is used, reversible logic design works to further almost completely remove the dissipations lowers the amount of switching activities and power consumption. 10th edition, issue 1, page 507, Emerging Topics in Computing: An IEEE Transaction–513H. Waris, F. Lombardi, C. Wang, W. Liu, and J. Han, "High -Performance Approximate Recursive multipliers Using Hybrid Partial Product Approach," January 1–March 2, 2022 [1]

One argument is because devices that carry out logical operations without a single-valued inverse are invariably included in computing machines. The physical irreversibility of this logical irreversibility is linked to it, and each irreversible function necessitates a minimum heat generation, often measured in kilo-therms, per machine cycle. This process of dissipation standardises independently of their precise logical past, therefore creating signals. More in-depth switching kinetics analysis is performed on two straightforward but representative models of bistable devices to determine the link between energy dissipation and speed and evaluate the effects of errors brought on by temperature variations.[2]

Since its transition function does not have a single-valued inverse, the typical general-purpose computer automaton, such as a Turing machine, is theoretically irreversible. It can be demonstrated here that these machines can be designed to be logically reversible at every stage, all the while maintaining their general computation capabilities and simplicity. Because it suggests that thermodynamically reversible computers could exist and execute practical computations at a practical speed while using far less energy than kT per logical step, this conclusion is quite interesting from a physical standpoint. During the initial computation phase, the logically reversible automaton functions similarly to the analogous irreversible automaton, with the exception that it preserves all intermediate outcomes, so circumventing the irreversible erase process. Printing out the intended output is the second step. Then, the third phase reversely eliminates every unwanted intermediate result by going backwards through the first stage's steps (which is only possible because the first stage was completed reversibly). This returns the machine to its initial state, save for the output tape that has been written, and leaves everything else in place. The final machine configuration thus consists of only the necessary output and a reconstructed duplicate of the input, with no extraneous data. To make the preceding results clear, consider a three-tape Turing machine example. An analysis is conducted on messenger RNA production, the physical expression of reversible computation. [4]

The field of reversible logic has showed tremendous promise in recent years. It can be used in quantum and optical computing, nanotechnology, as well as low power CMOS. It is impossible to reverse conventional gates like AND, OR, and EXOR. The term "TSG" refers to a recently suggested 4x4 reversible gate. Due to its primary characteristic, which allows it to function independently as a full adder that is reversible. This gate may now be used to build a full adder that is reversible. This study demonstrates a MAT reversible multiplier based on TSG gates. There are two ideas at its base. Fredkin gates allow for the parallel generation of partial products with a delay of d. With the use of a reversible parallel adder based on TSG gates, Consequently the addition can be reduced to log(2)N steps. An further 4x4 architecture is seen in the proposed reversible multiplier. It is shown that, compared to its current counterparts in the literature, the suggested multiplier design with the TSG gate is far more optional and superior in the terms of optimization. Consequently, this work provides a first step towards developing a more advanced system that can perform tasks that get more complex by utilizing reversible logic.[6]

Power minimization is interested in reversible circuits for logic because of their uses in bioinformatics, low power computing with DNA, CMOS design, quantum computing, and nanotechnology and optical information processing. The study process a novel 4x4 bit reversible multiplier circuit. The proposed multiplier that reverses. exhibits superior speed and reduced hardware intricacy in contrast to its current equivalents. Regarding the quantity comprising continuous inputs, garbage outputs, and gates, it performs better than its predecessors. "HNG" is the name of a 4x4 reversible gate that Haghparast and Navi recently proposed. One reversible complete Using just the reversible HNG gate, an adder can be produced. The development of an HNG gate-based reversible multiplier circuit is presented in this work. An HNG gate is utilised in a bidirectional

multiplying circuit. is suggested in order to multiple two 4-bit binary values. This suggested For N x N bit multiplication, a generic reversible 4x4 multiplier circuit can be used. With nanotechnology, we can utilize it to build increasingly intricate systems. [9]

For each bit of lost information, irreversible logic circuits release heat. Information is lost when it is not possible to uniquely extract the output vector from the input vector. Reversible logic is said to dissipate zero power since it is possible to uniquely recover the output vector based on the vector input. Applications for reversible computation include quantum computing, low-power CMOS architecture, DNA, and digital signal processing. The topic of this article discusses a quantum implementation of the widely used reversible gates and provides an overview of them. We also present a quantum implementation of this new PFAG gate. Finally, Benefits of the new, less expensive quantum version of the reversible multiplier circuit over the current models are assessed.[13]

Logic circuit power consumption is reduced in this technological age thanks to advancements in nanotechnology. Because reversible logic architecture uses less power and produces less heat dissipation, it is one of the promising technologies that is garnering more attention. Code conversion is a commonly employed procedure in digital systems due to several benefits like improved data security, less hardware requirements due to simpler arithmetic operations, decreased switching activity, faster operation, and power savings, among others. In order to convert codes such as Grayscale to binary and excess three BCD, this study presents a revolutionary reversible logic design. [17]

By applying ancient Vedic mathematics and Vedic concepts, the proposed work seeks to enhance the binary Vedic multiplier. To improve the result, it modifies the size, energy usage, and latency of the current Vedic multiplier. Additions are nearly always required in integrated circuits these days in order to achieve satisfactory results. The adders need to fulfill two requirements: they need to be fast and energy-efficient regarding chip area and power usage. Choosing an adder requires combination that optimizes for area, power, and delay, the paper offers a useful alternate approach. The carry skip, carry choose, and carry look-ahead adders are the adders used in this design. In ancient Vedic mathematics, the solution is much simplified increasing the efficiency of the entire process. The amalgamation and simulation are completed in Xilinx tool, and the intended Vedic multiplier is imposed in Verilog. [21]

III. Existing State-of-the-Research Endeavors

The text presented describes the use of reversible logic design in addition to traditional logic gates to achieve the 32x32 Urdhva Tiryakbhayam multiplier implemented using digital logic.

3.1 Conventional Execution of Logic:

The 32x32 Urdhva Tiryakbhayam multiplier is implemented using conventional gates.

Figure probably shows how the AND, OR, and XOR gates are arranged to implement the multiplication logic.

The formulas that describe how the inputs are combined to get the desired outputs are provided for the four output bits.

Usually, irreversible logic In the traditional logic implementation, gates are employed.

3.2 Reversible Logic Implementation:

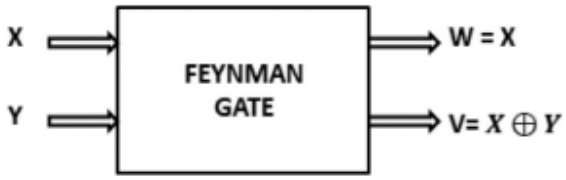


Fig. 2. FEYNMAN GATE

For all reversible linear functions, two ∗ two Feynman gates and converters are required. A Feynman gate with two inputs and two outputs is referred to as a CNOT gate, or copying gate. Logic functions include, for example, W=X& V=X⊕Y.

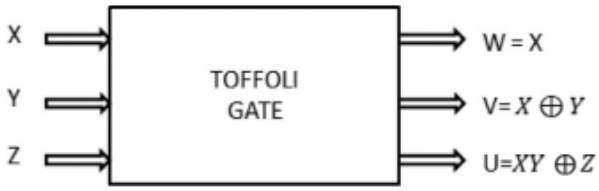


Fig. 3. TOFFOLI GATE

One of the Toffoli gate's greatest benefits is its tiny size. Three inputs and three outputs make up this logic gate's components. The Toffoli portal can be described as a "controlled-controlled-not gate" because The inputs, Y And Z stay constant ,the entry inverts A, and B=1 and C=1 . The logical functions V = Y, W = X, and U = Z ˆ (XY)

DOUBLE KEY GATE:

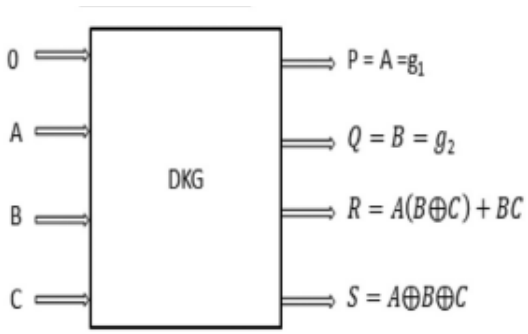


Fig. 4. GATE DKG AS FULLADDER.

Only full subtractor and FA applications are possible for a reversible DKG gate with4∗4. When A=0, the DKG gate

operates as an FA. It functions as a complete Subtractor when A = 1. It has been established that in order to generate distinct product combinations, a complete reversible circuit requires two or three discharges of rubbish.

3.3 Ripple Carry Adder using Dual Key Gate:

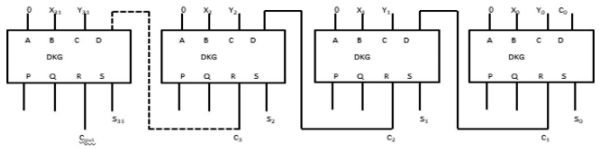


Fig. 5. 32-Bit Reversible RCA Based On DKG.

Utilizing the Dual Key Gate (DKG) for both addition and subtraction operations, a Reversible Ripple Carry Adder (RCA) is suggested in this study. Only complete subtractors or fully reversible adders are intended to be possible with the 4x4 DKG reversible logic gate. An reversible DKG Full Adder is represented by A=0, while a DKG Full Subtractor is shown by A=1. The input pattern controls how the gate operates. In order to ensure unique combinations of outputs, the design of the reversible complete adder circuit is designed with a minimum of two waste outputs.

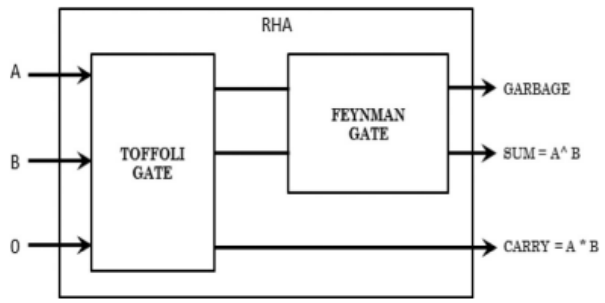


Fig. 6. Reversible Half Adder.

Toffoli and Feynman gates are integrated using the quantum characteristics About the reversible half adder that is suggested. Operations using reversible logic operations are intended to be achieved with this design while using the least amount of energy. Whereas the Feynman gate improves quantum parallelism, the Toffoli gate guarantees controlled-NOT operation. Half-adder computations are supported by the RHA, demonstrating the synergistic usage of these gates to provide efficient and reversible binary addition. An evaluation of the effectiveness of this proposed design must include both performance analysis and experimental validation.

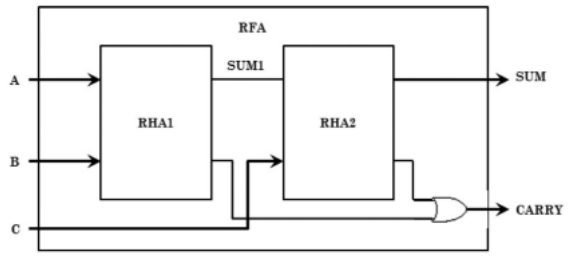


Fig. 7. Reversible Full Adder

The suggested idea for a reversible half-adder is included into the Reversible full-adder. Reversible binary addition with lower energy consumption is accomplished by the Full Adder by utilizing RHA's integration of Toffoli and Feynman gates. The Feynman gate improves quantum parallelism, and the Toffoli gate guarantees controlled-NOT functionality. A potential component in the quantum and reversible computing architectures because of its arrangement, which enables it to carry out effective and reversible operations.

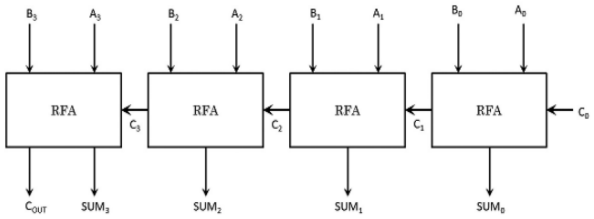


Fig. 8. Proposed Reversible RCA using proposed RFA.

The suggested Reversible Full Adder design is integrated with the Proposible Ripple Carry Adder. The goal of this combination is to build an energy-efficient, reversible circuit for binary addition. The RCA is reversible in part because of the RFA, which incorporates Feynman and Toffoli gates. In accordance with the tenets of both reversible and quantum computing, ripple carry addition can be carried out by the Reversible RCA in this setup. To determine whether this suggested design is useful in achieving reversible and energy-efficient computations, experimental validation and performance analysis are necessary.

3.4 Koggestone Adder:

In parallel, KSA adds prefixes. With regard to exceptional arithmetic circuit performance, it is the fastest and is often used in business. The hardest stage, carry generation, is the three-stage CLA adder structure used by KSA is improved. Carry computations in KSA are expedited using parallel carry computations. A decent adder with a trade-off between efficiency, area, and timing is typically desirable. Significantly faster overall operation is achieved by using the carry computation method. This increases speed while decreasing-area.

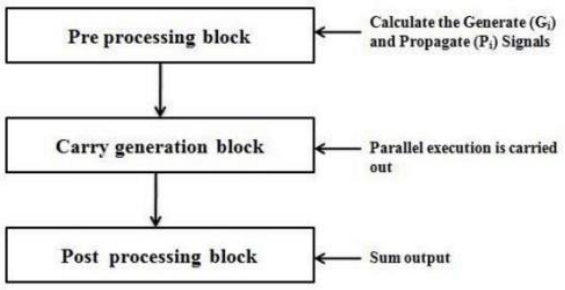


Fig. 9. The parallel prefix adder architecture of Kogge Stone.

3.5 Pre-Processing Block:

Equations such as these are used to compute the generation of both the signal that was produced and the both the signal that was produced and for the inputs. The Parallel Prefix Adder starts with this step.

Pi must be equal to Ai XOR Bi---(1)

Gi is equivalent to both Ai AND Bi----(2)

3.6 Transport Generation Block:

The most crucial component of this adder design is the carry produced stage. Black Cell and Gray Cell are two examples of its constituent parts. The signals that are generated and disseminated in order for the next stages to computation are produced using black cells. The Grey Cell only produces generated signals, which are used or necessary for the sum calculation in the next step.

3.7 Black Cell:

A single set of signals that propagate and generate (G, P) is calculated by the black cell operator upon the receipt of two sets of signals to create and propagate, Gi, Pi, and Gj , Pj

Pi AND Pj OR Gi=G……..…….. (3)

Pi+Pj=P Here we go……..……(4)

3.8 Grayscale:

The Gray operator receives two sets of propagate and generate signals (Gi, Pi). Using the other sets of signals, he computes one set of generate signal(G). (Gj, Pj).

G is Equal to Gi OR (Pi AND Pj)…….(5)

3.9 Post Processing Block:

The adder's ultimate step is this one, and its ultimate result is Sum and Carry.

Si = Pi XORCi-1……..……..……..……..……..…..(6)

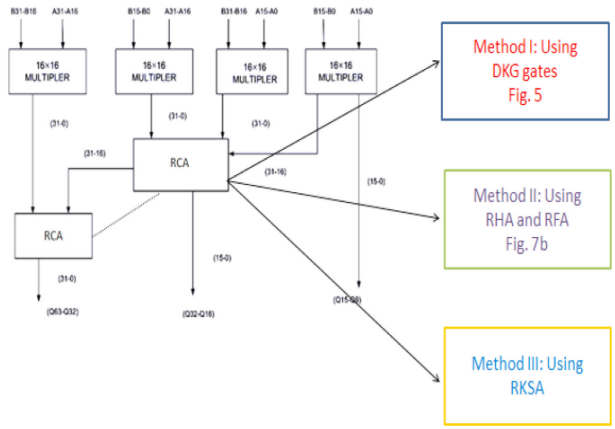


Fig. 10. 32- bit Urdhva Tiryakbhayam Sutra.

Utilizing four 16-bit Vedic multipliers, the 32-bit Urdhva Tiryakbhayam Sutra is a Vedic multiplication algorithm. It makes use of RCA_DKG, RCA_RFA, and RCA_RKSA, which are three distinct methods for the carry adder for Ripples? Reversible Kogge Stone Adder, Reversible Full Adder and Dual Key Gate are three separate components that are integrated into these variations of the Ripple Carry Adder. With the precise selection of RCA affecting the computation's overall efficiency and properties, the algorithm integrates these components to perform efficient and reversible binary addition in the context of 32-bit multiplication.

IV. PROPOSED

Utilizing four 16-bit Vedic multipliers, the 32-bit Urdhva Tiryakbhayam Sutra is a Vedic multiplication algorithm. It makes use of RCA_DKG, RCA_RFA, and RCA_RKSA, which are three distinct methods for the carry adder for ripples? Reversible Kogge Stone Adder(RKSA), Reversible Full Adder(RFA) and Double Key Gate (DKG) are three separate components that are integrated into these variations of the Ripple Carry Adder. With the precise selection of RCA affecting the computation's overall efficiency and properties, the algorithm integrates these components to perform efficient and reversible binary addition in the context of 32-bit multiplication.

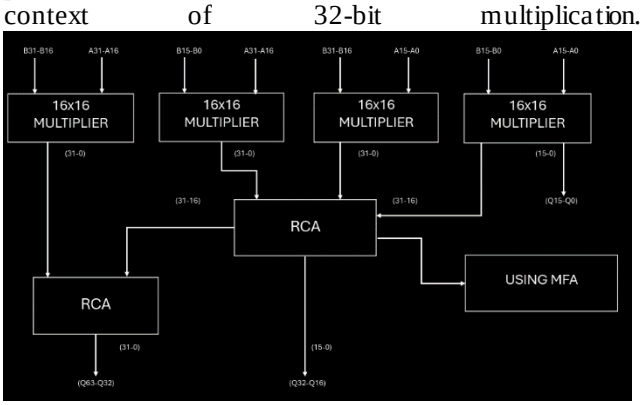


Fig. 11. 32- bit Urdhva Tiryakbhayam Sutra.

4.1 Clock Gating:

One crucial VLSI circuit design consideration is reducing power dissipation. A few decades ago, designers would primarily prioritize testability, area, and delay in their optimizations. More power leakage and dissipation in chips is observed as technology scales down. Utilizing optimization techniques such as voltage scaling and clock gating will help us minimize power leakage and dissipation during scaling.

There is a higher power dissipation with increasingly sophisticated procedures. We can cut down on power consumption significantly by gate-keeping the clock network when it's not needed because it's a big source of power dissipation.

In the design we proposed, we reduced signal activity to lessen the dynamic power dissipation. This was the major topic of our investigation. It is possible to save a substantial amount of power by gate the clock whenever it is not needed, since the clock network is one of the main sources of power dissipation.

4.2 Synthesis based clock gating technique:

By combining Logic gates: OR, EXOR, or EXNOR, AND with a positive or negative latch, as illustrated in the figure, a gated clock can be produced using this method. Clock gating approach based on synthesis with negative latch When the enable signal is continuous, the x signal may be one. As a result, the controlled clock may be high, which prevents the negative latch from functioning and yields the previous value as the output in employing a negative latch for gating of clocks using synthesis.

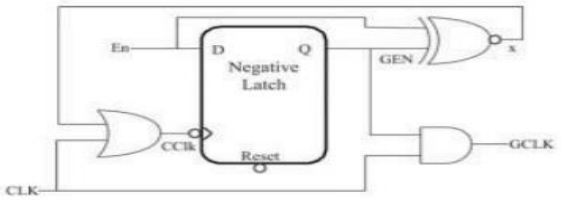


Fig. 12. Clock gating method based on synthesis and employing a negative latch.

When the signal for enablement shifts—which brings the X value down to zero—the clock-controlled negative latch circuit generates the output side having a different value. The clock signal's AND gate and the negative latch output signal are combined to create a gated clock signal.

An 8-bit arithmetic and logic unit supplied by the proposed work is capable of carrying out a wide range of arithmetic and logical operations. In this case, addition, subtraction, multiplication, and division are the arithmetic operations involved. The Booth method is used to construct operations using multiplication and division. Arithmetic, logical, complements of 1 and 2 as well as logical operators such as XOR, XNOR, NOR, AND, NAND, ,OR, and so on are among the several kinds of left and right shifts in mathematics. As anticipated, shift operations would shift up to three bits. In this case, the PIPO was created using a low power D latch and low power D flip flop were developed using the master-slave idea. In this instance, PIPO is being utilised to transmit the data to operations.

MFA [MODIFIED FULL ADDER]:

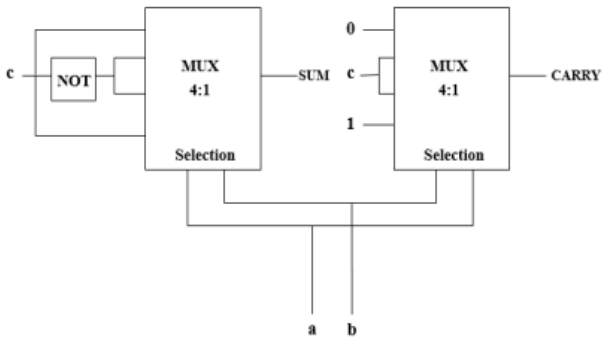


Fig. 13. Modified Full Adder.

One output line 'n' selection lines, and up to 'n' data inputs make up a multiplexer, which is a combinational circuit. An output will be attached to these based on selection lines values, these data inputs were created. The 'n' selection lines mean that there are only two possible combinations of ones and zeros. Consequently, each combination will have a single data input selected. A mux is an additional term for a multiplier. Four Data inputs (l3, l2, l1&l0), the components of the 4x1 multiplexer are one output (Y) and two selection lines (s1&s0).

The multiplexer 4x1 block diagram is displayed in the image below.

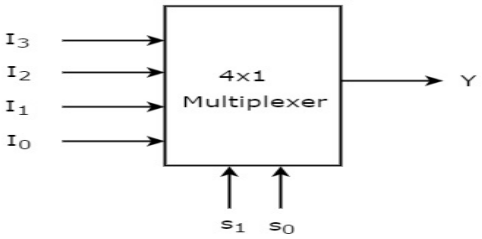


Fig. 14. 4:1 Multiplexer.

Here, a and b represent the two selection lines, each of which is a 4:1 multiplexer that make up this modified full adder. The multiplexer with the output of sum is limited to input C. Conversely, inputs 0, c, and 1 are sent into the multiplexer via the carry output. After the classic complete adder design is investigated, a multiplexer-based design is modelled employing the truth table, values for the input and output, when the next input line supplies logic 0 and logic 1. The greatest decrease in the number of logic design gates may be noticed with these multiplexer-based adder designs, indicating that the implementation is efficient.

Our suggested approach aims to reduce power and space while increasing circuit efficiency. Specifically, we will replace FULL ADDERS with a proposed MULTIPLIER based ADDER and GATED CLOCK, which is derived from SYNTHESIS BASED CLOCK GATING methodology, for the CLOCK signal.

V. Result and Analysis

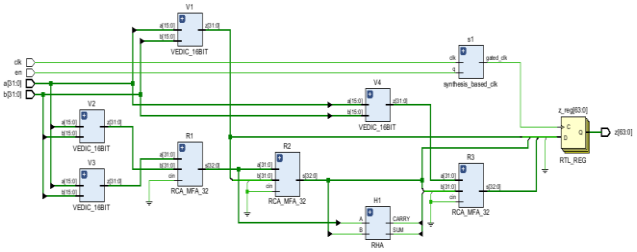
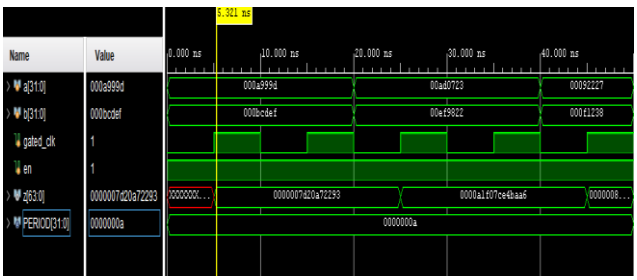


Fig. 15. SCHEMATIC.



Fig, 16. SIMULATION WAVEFORM.

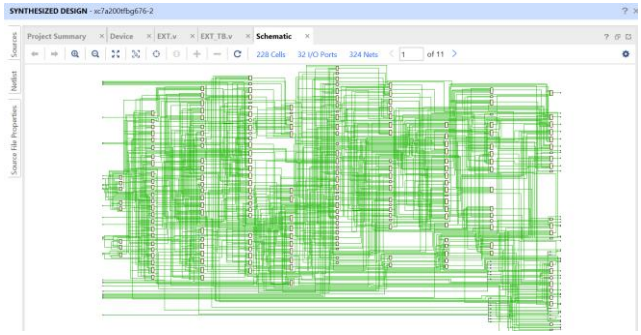


Fig. 17. TECHNOLOGY VIEW.

Name	Slice LUTs (134600)	Slice Registers (269200)	Bonded IOB (400)	BUFGCTRL (32)
EXT	1966	64	130	1
s1 (synthesis_based_clk)	1	1	0	0

Fig. 18. AREA.

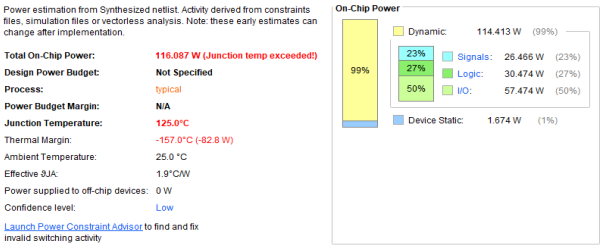


Fig. 19. POWER VALUE.

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay
Path 1	∞	28	29	76	a[1]	z_reg[57]/D	17.610

Fig. 20. DELAY VALUE.

COMPARISION TABLE:

	AREA	POWER	DELAY
RCA_DKG	1999	1674mW	20.866nS
RCA_RFA	2035	1674mW	21.811nS
RCA_RKSA	2395	1674mW	19.487nS
RCA_MFA	1966	1674mW	17.610nS

VI. CONCLUSION

Equipped with four 16-bit Vedic multipliers, the 32-bit Urdhva Tiryakbhayam Sutra is a Vedic multiplication algorithm. It utilizes RCA_DKG, RCA_RFA, and RCA_RKSA, three distinct techniques of the Adder with Ripple Carry(RCA). Double Key Gate(DKG),Reversible Kogge Stone Adder (RKSA),and Reversible Full Adder (RFA) are three distinct components that are incorporated into these RCA variants. By combining these elements, the technique may perform reversible and efficient binary addition in the context of 32-bit multiplication. By replacing the original full adders with modified full adders and using a synthesis-based clock, gating area and latency will be decreased, and overall computing performance and characteristics will be greatly impacted by the specific RCA application.

FUTURE SCOPE:

Replacing RCA with carry look ahead adder results in a slight increase in area but reduces delay significantly, without impacting power consumption.

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