

# BATTERY & PROTECTION & OR

Q1  
IRLML6401

+3V0 +5V

+BATTERY

BT1  
CR2032

TP: GND

82k  
R8

33k  
R9

GND

GND

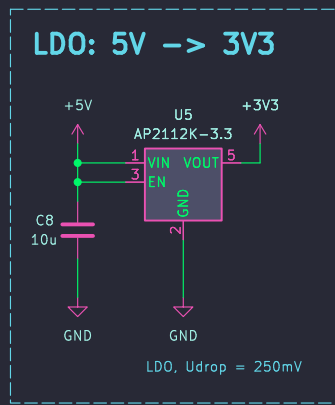
FET GATE

USB\_VBUS\_SENSE

Q1 works as a reverse polarity protection, closes on 5V presence from USB (Ugate > Usource)

CR2032 will have ~200mA till 2V5 discharge

Energizer CR2032



## LOW-PASS FILTER

The diagram illustrates a low-pass filter circuit. The signal path is shown in green. It starts from the left, goes up to a +3V3 supply, then right to a +3V0 supply, then down to a green dot. From this dot, the path goes right to a component labeled FB1 330 (a resistor), then down to another green dot. From this second dot, the path goes right to a third green dot, then down to a component labeled C7 10u (a capacitor), and finally down to a GND symbol. A VDD supply is also indicated with an upward arrow next to the third green dot.

## USB-C: POWER & MSD

The diagram illustrates the internal wiring of a USB-C connector (J1) for power and mass storage device (MSD) functionality. The connector is shown with its standard pins: VBUS (A4), CC1 (A5), CC2 (B5), D- (A7, B7), D+ (A6, B6), SBU1 (A8), and SBU2 (B8). The shield is connected to GND.

**Power Section:**

- A +5V power source is connected to the VBUS pin (A4) through a BAT60A diode (D1) and a 5k1 resistor (R1).
- The VBUS pin is also connected to a +5V source through a 5k1 resistor (R2).
- The CC1 (A5) and CC2 (B5) pins are connected to a VCC pin (D3) through a PRTR5V0U2X diode (D3).

**MSD Section:**

- The D- (A7, B7) and D+ (A6, B6) pins are connected to a differential pair of lines labeled I/O2 and I/O1, respectively, through a 3-pin connector (D3).
- The SBU1 (A8) and SBU2 (B8) pins are connected to a GND pin (D3) through a 1-pin connector (D3).

**Shield and Grounding:**

- The shield is connected to GND through a 1M resistor (R7) and a 4n7 capacitor (C10).
- The GND pin (D3) is connected to the GND shield.

**Legend:**

- D+/D- is differential pair
- Zdiff (differential impedance) is equal to  $2 * Z_{odd}$ , so a  $Z_{odd}$  of 45  $\Omega$  gives us a Zdiff of 90  $\Omega$

[illegible]

U3 SHT30-DIS

5V VDD

ADDR RESET

1 SDA

2 ADDR

3 SCL

4 SCL

5 VDD

6 RESET

7 ALERT

TEMP-INT

C4 100n

GND

GND

GND

SHT3x-DIS

0x44, ADDR=L

## I2C PULL-UPS

The diagram illustrates the pull-up circuitry for the SDA and SCL lines. Each line is connected to a pull-up resistor (R4 for SDA, R5 for SCL) to the VDD supply. The lines are shown as green traces with a green dot at the connection point to the resistor. A pink arrow points to the connection point for each line, labeled 'TP: SDA' and 'TP: SCL' respectively. The resistors are labeled 'R4 5k1' and 'R5 5k1'. The VDD supply is indicated by a red arrow pointing upwards from the resistor connection point.

A circuit diagram showing an LED connected to VDD. A resistor R3 (1k) is connected in series with the LED. The current I is 1 mA.

# ARM SWD

TagConnect SWD ARM

VDD

Vref

RESET

SWCLK/TCK

SWDIO/TMS

SWO/TDO

NC/TDI

J2

VDD

GND

GND

GND

GND

GND

GND

C18 100n

C15 100n

RESET