Dr. Elizabeth Polgreen

✉ elizabeth.polgreen@ed.ac.uk

Education

2020 – **Lecturer**, *Laboratory for Foundations of Computer Science*, University of Edinburgh.
My research interests are in program synthesis algorithms, applications of program synthesis and integration of synthesis into verification techniques.

2019 – 2020 **Visiting Research Scholar**, *Computer Science*, The University of California, Berkeley.

2016 – 2019 **PhD**, *Computer Science*, The University of Oxford.

2010 – 2011 **Masters of Engineering**, *Electrical and Electronic Engineering*, The University of Cambridge.

2007 – 2010 **Bachelor of Arts**, *Electrical and Electronic Engineering*, The University of Cambridge.

Relevant Publications

2022 **Synthesis and Satisfiability Modulo Oracles**, *E. Polgreen, A. Reynolds, S.A. Seshia*, International Conference on Verification, Model Checking, and Abstract Interpretation(VMCAI).

2021 **The SyGuS Language Standard Version 2.1**, *S. Padhi, E. Polgreen, M. Raghothaman, A. Reynolds, A. Udupa*.

2021 **Medley Solver: Online SMT Algorithm Selection**, *N. Pimpalkhare, F. Mora, E. Polgreen, S.A. Seshia*, International Conference on Satisfiability (SAT).

2020 **Using model checking tools to triage the severity of security bugs in the Xen hypervisor**, *B. Cook, B. Doebel, D. Kroening, N. Manthey, M. Pohlack, E. Polgreen, M. Tautschnig, P. Wieczorkiewicz* , Formal Methods in Computer-Aided Design (FMCAD).

2022 **Gradient Descent over Metagrammars for Syntax-Guided Synthesis**, *N. Chan, E. Polgreen, S.A. Seshia*, Workshop of Synthesis (SYNT).

2022 **Synthesis in UCLID5**, *F. Mora, K. Chan, E. Polgreen, S.A. Seshia*, Workshop of Synthesis (SYNT).

2018 **CounterExample Guided Inductive Synthesis Modulo Theories**, *A. Abate, C. David, P. Kesseli, D. Kroening, E. Polgreen*, Computer Aided Verification (CAV).

2017 **Automated Formal Synthesis of Digital Controllers for State-Space Physical Plants**, *A. Abate, I. Bessa, D. Cattaruzza, L. Cordeiro, C. David, P. Kesseli, D. Kroening, and E. Polgreen*, Computer Aided Verification (CAV).

2017 **DSSynth: An Automated Digital Controller Synthesis Tool for Physical Plants**, *A. Abate, I. Bessa, D. Cattaruzza, L. Chaves, L. Cordeiro, C. David, P. Kesseli, D. Kroening, and E. Polgreen*, Automated Software Engineering (ASM).

2017 **Automated Experiment Design for Efficient Verification of Parametric Markov Decision Processes**, *E. Polgreen, V. Wijesuriya, S. Hasaert, A. Abate*, Quantitative Evaluation of SysTems (QEST).

2016 **Data-efficient Bayesian Verification of Parametric Markov Chains**, *E. Polgreen, V. Wijesuriya, S. Haesaert, A. Abate*, Quantitative Evaluation of SysTems (QEST).

Invited Talks

CounterExample Guided Inductive Synthesis Modulo Theories, The Simons Institute for the Theory of Computing, 2021.

Supervision

2021-2022 **Portfolio solving for Syntax-Guided Synthesis**, *Universty of Edinburgh*, 2021.

2020-2021 **Online-learning for SMT-solver algorithm selection**, *UC Berkeley*, Undergraduate project.

2020-2021 **Metagrammars for syntax-guided synthesis**, *UC Berkeley*, Undergraduate research project.

2017-2018 **CounterExample Guided Neural Synthesis**, *University of Oxford*, MSc project.

Service

Program committees.
SMT workshop 2022, SAT 2022, CAV 2022, FMCAD 2022, QEST 2022, SYNT 2021 (chair), CAV 2021 (artefact evaluation), TACAS 2021 (artefact evaluation), FMCAD 2021, QEST 2021,SYNT 2019

Non-program committee reviews.
Acta Informatica, Transactions on Programming Languages and Systems, Robotics: Science and Systems 2017, CAV 2021, SOFSEM-FOCS2017, QEST 2017, QEST 2016, Information and Software Technology, 13th International Workshop on Discrete Event Systems

Experience

Jun 2018 – Sep 2018 **Software Development Intern**, *Amazon Web Services, Dresden*.
Continuation of previous internship applying formal verification techniques to C code for an x86 hypervisor

Aug 2017 – Oct 2017 **Software Development Intern**, *Amazon Web Services, Dresden*.
Development of analysis tools based on formal methods for hot-patching an x86 hypervisor

Sep 2015 – Mar 2016 **Research Assistant in Verification**, *Department of Computer Science, University of Oxford*.
Working with Professor Alessandro Abate on application of machine learning techniques in verification. This work produced the paper published at QEST 2016

Sep 2013 – Aug 2015 **Research Support**, *Department of Computer Science, University of Oxford*.
Lead aspects of research project execution over a broad variety of research projects within the Systems Verification and Validation group.

Jan 2013 – Aug 2013 **Electronics and Software Engineer**, *Peach Innovations*, Cambridge.
Manufacture, testing and debugging of real-time rowing instrumentation systems. Analysis of system output data with view to new product development.

Aug 2011 – Jan 2013 **Electronics and Software Engineer**, *Eg Technology*, Cambridge.
Design engineer developing electronics hardware and software for a variety of consumer and medical devices. Main contributor of C code to embedded software projects using ARM microcontrollers. Further experience in LabVIEW, and contributing to larger team projects written in C#.

Teaching

2021 **Formal Verification**, *University of Edinburgh*, Course organiser.

2020 **Formal Methods: Specification, Verification, and Synthesis**, *UC Berkeley*, Guest Lectures.

2018 **Computer Aided Verification Course**, *University of Oxford*, Guest Lecture.