Dr Elizabeth Polgreen

Education

2016 – 2020 **PhD**, *Computer Science*, The University of Oxford.

2010 – 2011 **Masters**, *Electrical and Electronic Engineering*, The University of Cambridge.

2007 – 2010 **Bachelor of Arts**, *Electrical and Electronic Engineering*, The University of Cambridge.

Employment

2020 – **Lecturer (Assistant Professor)**, *Laboratory for Foundations of Computer Science*, University of Edinburgh.

2019 – 2020 **Visiting Research Scholar**, *Computer Science*, The University of California, Berkeley.

Jun 2018 – Sep 2018 **Software Development Intern**, *Amazon Web Services, Dresden.*
Applying formal verification techniques to C code for an x86 hypervisor

Aug 2017 – Oct 2017 **Software Development Intern**, *Amazon Web Services, Dresden.*
Development of analysis tools based on formal methods for hot-patching an x86 hypervisor

Sep 2015 – Mar 2016 **Research Assistant in Verification**, *Department of Computer Science, University of Oxford.*
Application of machine learning techniques in verification.

Sep 2013 – Aug 2015 **Research Support**, *Department of Computer Science, University of Oxford.*
Research support for research projects within the Systems Verification and Validation group.

Jan 2013 – Aug 2013 **Electronics and Software Engineer**, *Peach Innovations*, Cambridge.
Manufacture, testing and debugging of real-time rowing instrumentation systems.

Aug 2011 – Jan 2013 **Electronics and Software Engineer**, *Eg Technology*, Cambridge.
Embedded software and circuit design for a variety of commerical and research products.

Selected Publications

2022 **UCLID5: Multi-Modal Formal Modeling, Verification, and Synthesis**, *E. Polgreen, K. Cheang, P. Gaddamadugu, A. Godbole, K. Laeufer, S. Lin, Y. Manerkar, F. Mora, S.A. Seshia*, Computer Aided Verification (CAV).

2022 **Synthesis and Satisfiability Modulo Oracles**, *E. Polgreen, A. Reynolds, S.A. Seshia*, International Conference on Verification, Model Checking, and Abstract Interpretation(VMCAI).

2020 **Using model checking tools to triage the severity of security bugs in the Xen hypervisor**, *B. Cook, B. Doebel, D. Kroening, N. Manthey, M. Pohlack, E. Polgreen, M. Tautschnig, P. Wieczorkiewicz* , Formal Methods in Computer-Aided Design (FMCAD).

2018 **CounterExample Guided Inductive Synthesis Modulo Theories**, *A. Abate, C. David, P. Kesseli, D. Kroening, E. Polgreen*, Computer Aided Verification (CAV).

2017 **Automated Formal Synthesis of Digital Controllers for State-Space Physical Plants**, *A. Abate, I. Bessa, D. Cattaruzza, L. Cordeiro, C. David, P. Kesseli, D. Kroening, and E. Polgreen*, Computer Aided Verification (CAV).

Service

Steering committee, ETAPS, 2022-onwards.

Workshop chair, International Workshop on Synthesis (SYNT), 2021.

Program committees.
2022: SMT workshop, SAT, CAV, FMCAD, QEST. 2021: CAV (artefact evaluation), TACAS (artefact evaluation), FMCAD, QEST. 2019: International Workshop on Synthesis (SYNT)