University of California, Berkeley,
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Dr Elizabeth Polgreen

Education and Experience

Sep 2019 – present **Postdoctoral Research Scholar**, *Computer Science*, University of California, Berkeley.
I work in Professor Sanjit Seshia's group. I am interested in integration of synthesis into verification techniques.

2016 – 2019 **PhD**, *Computer Science*, University of Oxford.
Program synthesis without syntactic templates.

Jun 2018 – Sep 2018 **Software Development Intern**, *Amazon Web Services, Dresden*.
Continuation of previous internship applying formal verification techniques to C code for an x86 hypervisor

Aug 2017 – Oct 2017 **Software Development Intern**, *Amazon Web Services, Dresden*.
Development of analysis tools based on formal methods for hot-patching an x86 hypervisor

Sep 2015 – Mar 2016 **Research Assistant in Verification**, *Department of Computer Science, University of Oxford*.
Working with Professor Alessandro Abate on application of machine learning techniques in verification. This work produced the paper published at QEST 2016

Sep 2013 – Aug 2015 **Research Support**, *Department of Computer Science, University of Oxford*.
Lead aspects of research project execution over a broad variety of research projects within the Systems Verification and Validation group.

Jan 2013 – Aug 2013 **Electronics and Software Engineer**, *Peach Innovations*, Cambridge.
Manufacture, testing and debugging of real-time rowing instrumentation systems. Analysis of system output data with view to new product development.

Aug 2011 – Jan 2013 **Electronics and Software Engineer**, *Eg Technology*, Cambridge.
Design engineer developing electronics hardware and software for a variety of consumer and medical devices. Main contributor of C code to embedded software projects using ARM microcontrollers. Further experience in LabVIEW, and contributing to larger team projects written in C#.

2010 – 2011 **Masters of Engineering**, *Electrical and Electronic Engineering*, The University of Cambridge.

2007 – 2010 **Bachelor of Arts**, *Electrical and Electronic Engineering*, University of Cambridge.

Publications

The main contributing author(s) of the paper are marked with *.

2019 **Automated Formal Synthesis of Provably Safe Digital Controllers for Continuous Plants**, *A. Abate, I. Bessa, L. Cordeiro, C. David, P. Kesseli, D. Kroening, and E. Polgreen**, Computer Aided Verification (CAV).

2018 **CounterExample Guided Inductive Synthesis modulo Theories**, *A. Abate, C. David, P. Kesseli, D. Kroening, E. Polgreen**, Computer Aided Verification (CAV).

2017 **Automated Formal Synthesis of Digital Controllers for State-Space Physical Plants**, *A. Abate, I. Bessa, D. Cattaruzza*, L. Cordeiro, C. David, P. Kesseli, D. Kroening, and E. Polgreen**, Computer Aided Verification (CAV).

2017 **DSSynth: An Automated Digital Controller Synthesis Tool for Physical Plants**, *A. Abate, I. Bessa*, D. Cattaruzza, L. Chaves, L. Cordeiro*, C. David, P. Kesseli, D. Kroening, and E. Polgreen*, Automated Software Engineering (ASM).

2017 **Automated Experiment Design for Efficient Verification of Parametric Markov Decision Processes**, *E. Polgreen*, V. Wijesuriya, S. Hasaert, A. Abate*, Quantitative Evaluation of SysTems (QEST).

2016 **Data-efficient Bayesian Verification of Parametric Markov Chains**, *E. Polgreen*, V. Wijesuriya, S. Haesaert, A. Abate*, Quantitative Evaluation of SysTems (QEST).

Arxiv, Work in Progress or Under Submission

2020 **Should We Wake the Developer Up? Using model checking tools to triage the severity of security bugs**, *B. Cook, B. Doebel, D. Kroening, N. Manthey, M. Pohlack, E. Polgreen*, M. Tautschnig, P. Wieczorkiewicz*, under submission.

2020 **SynRG: Syntax-Guided Synthesis of Invariants with Alternating Quantifiers**, *E. Polgreen, S. Seshia*, under submission.

2020 **CounterExample Guided Inductive Synthesis modulo Theories**, *A. Abate, H. Barbosa, C. Barrett, C. David, P. Kesseli, D. Kroening, E. Polgreen*, A. Reynolds, C. Tinelli*, in progress.

2019 **CounterExample Guided Neural Synthesis**, *E. Polgreen*, R. Abboud, D. Kroening*, arxiv, in progress.

2017 **Probabilistic IC3: a New Symbolic Model Checking Algorithm for Markov Chains**, *E. Polgreen*, M. Brain, M. Fraenzle, A. Abate*, arxiv.

Talks

CounterExample Guided Inductive Synthesis modulo Theories, Computer Aided Verification (CAV), 2018.

Automated Experiment Design for Efficient Verification of Parametric Markov Decision Processes, Quantitative Evaluation of SysTems (QEST), 2017.

Data-efficient Bayesian Verification of Parametric Markov Chains, Quantitative Evaluation of SysTems (QEST), 2016.

Student Supervision

2018 **MSc project - Supervised MSc project on CounterExample Guided Neural Synthesis**.

2020 **Supervising undergraduate research project on learning templates for Syntax-Guided Synthesis**.

Research grant experience

Grant applications.

Contributed to and helped to co-ordinate grant applications with Professor Daniel Kroening, including applications for Horizon2020, Chist-ERA and European Commission Proof of Concept grants

Grant reporting and support.
Assisted in managing and meeting intermediate reporting requirements for research grants from the European Research Commission, Semiconductor Research Corporation, ARTEMIS Joint Undertaking, and the EPSRC

Service

Program committees.
SYNT 2019

Reviewer.
ACM TOPLAS, Acta Informatica, SYNT 2019, Robotics: Science and Systems 2017, SOFSEM-FOCS 2017, QEST 2016, QEST 2017,13th International Workshop on Discrete Event Systems

Teaching

Guest lecture.
Computer Aided Verification course, Oxford,Michaelmas 2017

Guest lectures.
Formal Methods: Specification, Verification and Synthesis, Berkeley, Spring 2020

Admissions interviewer.
Computer Science undergraduate admissions interviewer, Oxford 2017, 2018

GCSE science teaching.
Work experience at various secondary schools in Oxfordshire

Courses studied.
Teaching Techniques for Electrical Engineering, Spring 2020