EE2016 Microprocessor Theory & Lab Aug – Nov 2022

Lab Exp1: Booth's Multiplier Implementation in FPGA

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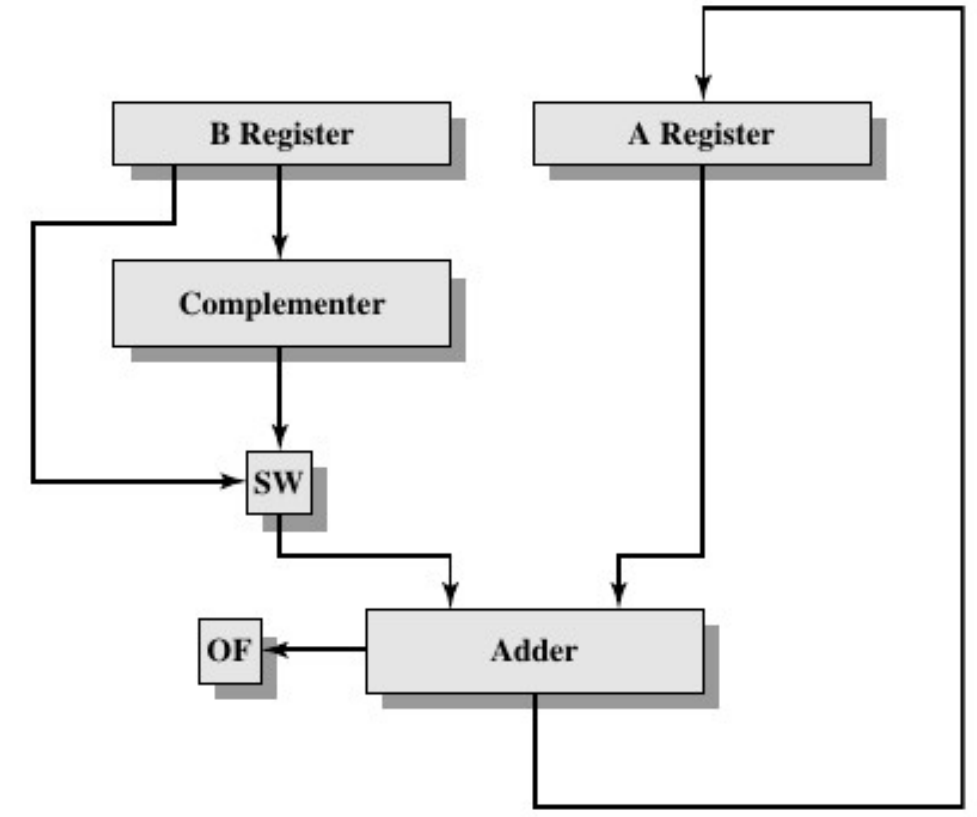
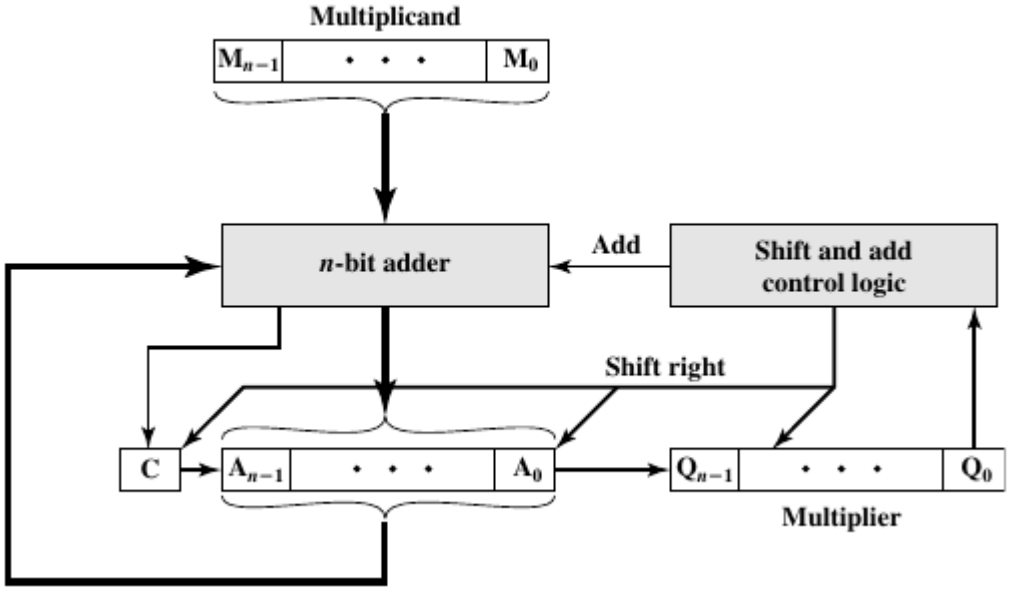
Hardware for Addition & Subtraction



OF = Overflow bit
SW = Switch (select addition or subtraction)

Unsigned Binary Multiplication

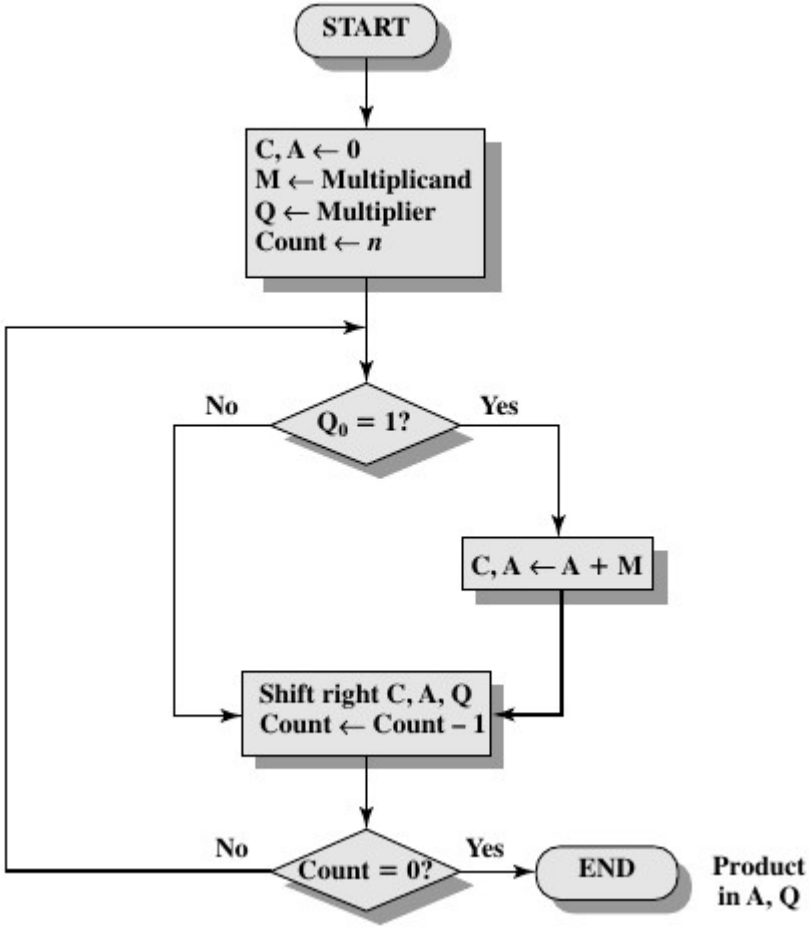
- Digital Circuit of Conventional Shift & Add Multiplier
- Improved version
  - Use of accumulator reduces memory space required
    - Save time in computation of partial products
    - 1 --> multiplicand
    - 0 --> zero
- Only unsigned binary multiplication
- S
- S



C	A	Q	M		
0	0000	1101	1011	Initial values	
0	1011	1101	1011	Add	First cycle
0	0101	1110	1011	Shift	
0	0010	1111	1011	Shift	Second cycle
0	1101	1111	1011	Add	Third cycle
0	0110	1111	1011	Shift	
1	0001	1111	1011	Add	Fourth cycle
0	1000	1111	1011	Shift	

Flow chart for unsigned binary multiplication

- Flow chart for unsigned binary multiplication
  - Only unsigned numbers
- Use of 2s compliment?
  - Problems
  - If both multiplicand and multiplier are negative
  - Either of them negative --> fails
- S



Booths Multiplier

A	Q	Q_{-1}	M		
0000	0011	0	0111	Initial values	
1001	0011	0	0111	A ← A − M	First cycle
1100	1001	1	0111	Shift	
1110	0100	1	0111	Shift	Second cycle
0101	0100	1	0111	A ← A + M	Third cycle
0010	1010	0	0111	Shift	
0001	0101	0	0111	Shift	Fourth cycle