Table of Contents

Notices....2
References....2
Conventions....2
Assigned Storage Locations....3
  Prefix Area Usage....3
    Low Address Prefix Area Usage (Addresses 000-1FF)....3
      Absolute Storage....4
      Real Storage....5
    High Address Prefix Area Usage (Addresses 1100-13FF)....8
      Absolute Storage....8
      Real Storage....9
Program Status Word (PSW)....11
  Program Status Word (Bits 0-31)....11
  Program Status Word (Bits 32-63)....12
  Program Status Word (Bits 64-127)....12
Control Registers....13
Dynamic Address Translation....24
  Control Register 0....26
  DAT Control Register....26
  Region Table Entries....26
  Segment Table Entries....26
  Page Table Entries....27
  Interrupt Information....27
    ASCE and Region Translation Exceptions....27
    Segment Exception....28
    Page Exception....28
External Interruptions....29
Input/Output Interruptions....31
Machine-Check Interruptions....32
Program Interruptions....35
Restart Interruptions....38
Supervisor-Call Interruptions....39
Features....40
Semi-privileged Operations....47
  ASN-Second Table Entry (ASTE)....49
  Entry Table Entry (ETE)....50
  Dispatchable Unit Control Table (DUCT)....51
  Basic Program Calls....53
    PROGRAM CALL to Current Primary....54
    PROGRAM CALL with Space Switching....54
    Basic Program Call Summary....54
  Stacking Program Calls....56
Appendix A - Assigned Storage Detail....57

Notices

References

IBM® System/360 Principles of Operation, A22-6821-7, September 1968

IBM System/370 Principles of Operation, GA22-7000-10, September 1987

Enterprise Systems Architecture/390 Principles of Operation, SA22-7201-08, June 2003

z/Architecture® Principles of Operation, SA22-7832-11, September 2017

Conventions

System/360 is not explicitly documented. Italics are used to identify architecture elements present in System/360.

Structures are compared using a table, where each cell represents a bit. Structures less than 32-bits are truncated on the right with black cells. Unused positions are indicated in gray. 64-bit addresses are truncated on the left (bits 0-31), only showing in the table the low-order bits (bits 32-63). Unpredictable information is indicated by question marks (?). The appropriate Principles of Operation manual should be consulted for the meaning of individual fields.

												bits				0	-	3	1										
S	/	3	7	0		U	s	a	g	e						Truncated													
E	S	A	/	3	9	0		U	s	a	g	e												Unused					
z	/	A	r	c	h	i	t	e	c	t	u	r	e		U	s	a	g	e					?	?	?	?	?	?	?	?
												bits				32	-	63													

Assigned Storage Locations

Assigned storage locations are confined to the CPU prefix area, the first 4096 or 8192 bytes of real or absolute storage depending upon the processor architecture mode.

Prefix Area Usage

Each 256-byte section of the prefix area is depicted in the following diagram. Eight zero bits should be appended to right of the values shown. Areas within the prefix area may be available for program usage (green) or contain areas assigned for system usage (red). Storage beyond the prefix area is designated in gray. Assigned functions include Initial Program Load (L), interrupt program status words (P), interrupt information (I) or save areas (S).

First 4096-byte Prefix Page																Second 4096-byte Prefix Page															
0000	0100	0200	0300	0400	0500	0600	0700	0800	0900	0A00	0B00	0C00	0D00	0E00	0F00	1000	1100	1200	1300	1400	1500	1600	1700	1800	1900	1A00	1B00	1C00	1D00	1E00	1F00
LSPI																															
LSPI																															
LPI																	I	S					I								

Each double word of the prefix area reserved for system usage is broken down into details in the following sections. The following colors are used to designate functions with which an assigned storage location is related:

Absolute Location descriptions associated with specific externally initiated functions

Initial Program Load	Store Status

Real Location descriptions associated with specific Interruptions

External	Input/Output	Machine-Check	Program	Restart	Supervisor

Low Address Prefix Area Usage (Addresses 000-1FF)

000	008	010	018	020	028	030	038	040	048	050	058	060	068	070	078	080	088	090	098	0A0	0A8	0B0	0B8	0C0	0C8	0D0	0D8	0E0	0E8	0F0	0F8
LP	LP	L	P	P	P	P	P	I	I	I	P	P	P	P	P	I	I	I	I		I	I	I				S	S	I		
LP	LP	L	P	P	P	P	P				P	P	P	P	P	I	I	I	I	IS			I	I	I	S	S	S	I	I	I
L	L	L														I	I	I	I	IS	I	I	I	I	I				I	I	I

100	108	110	118	120	128	130	138	140	148	150	158	160	168	170	178	180	188	190	198	1A0	1A8	1B0	1B8	1C0	0C8	1D0	1D8	1E0	1E8	1F0	1F8
S	I	I	I	I	I	I	I	I	I	I	I	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S
S	I			S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S
				P	P	P	P	P	P	P	P	P	P	P	P					P	P	P	P	P	P	P	P	P	P	P	P

Absolute Storage

Absolute Addresses: 00-1F

00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
Initial Program Load PSW								Initial Program Load CCW 1								Initial Program Load CCW 2															
Initial Program Load PSW								Initial Program Load CCW 1								Initial Program Load CCW 2															
Initial Program Load PSW								Initial Program Load CCW 1								Initial Program Load CCW 2															

Absolute Addresses: A0-BF

A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	AA	AB	AC	AD	AE	AF	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	BE	BF
			AM																												
			AM																												

Absolute Addresses: C0-DF

C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF
																								CPU Timer SA							
																				Ext. SA Addr.				CPU Timer SA							

Absolute Addresses: E0-FF

E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED	EE	EF	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	FA	FB	FC	FD	FE	FF
Clock Comparator SA																															
Clock Comparator SA																															

Absolute Addresses: 100-11F

00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
PSW Save Area								Prefix SA				Model Dep. Feature Area																			
PSW Save Area								Prefix SA																							

Absolute Addresses: 100-1FF

00	08	10	18	20	28	30	38	40	48	50	58	60	68	70	78	80	88	90	98	A0	A8	B0	B8	C0	C8	D0	D8	E0	E8	F0	F8
See Above												FP Reg. SA				General Register Save Area								Control Register Save Area							
See Above				Access Register Save Area								FP Reg. SA				General Register Save Area								Control Register Save Area							

Real Storage

Real Addresses: 00-1F

00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
Restart New PSW								Restart Old PSW																External Old PSW							
Restart New PSW								Restart Old PSW																External Old PSW							

Real Addresses: 20-3F

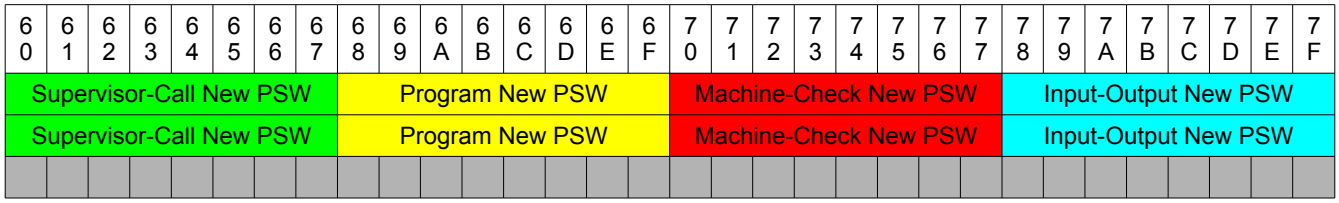
20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
Supervisor-Call Old PSW								Program Old PSW								Machine-Check Old PSW								Input-Output Old PSW							
Supervisor-Call Old PSW								Program Old PSW								Machine-Check Old PSW								Input-Output Old PSW							

Real Addresses: 40-5F

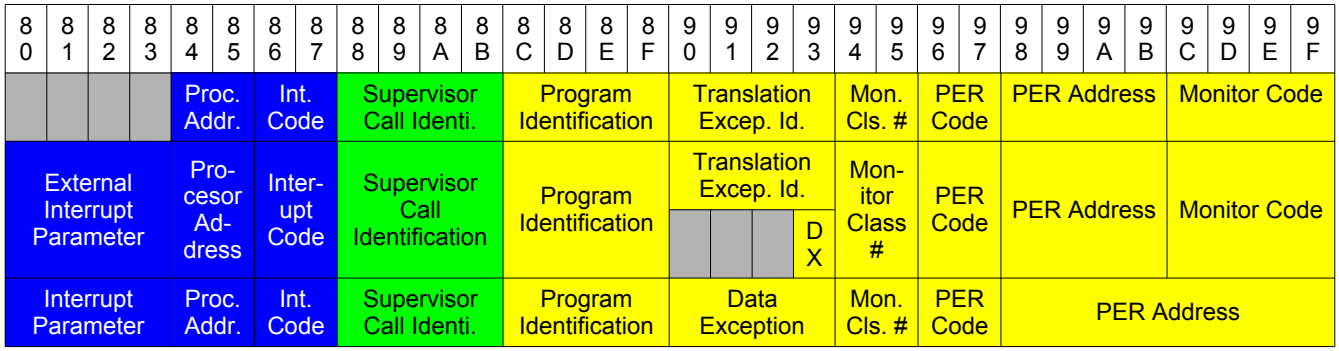
40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
Channel Status Word								Channel Address Word								Interval Timer				Trace Table Designation				External New PSW							
																								External New PSW							

Mainframe Architecture Comparisons

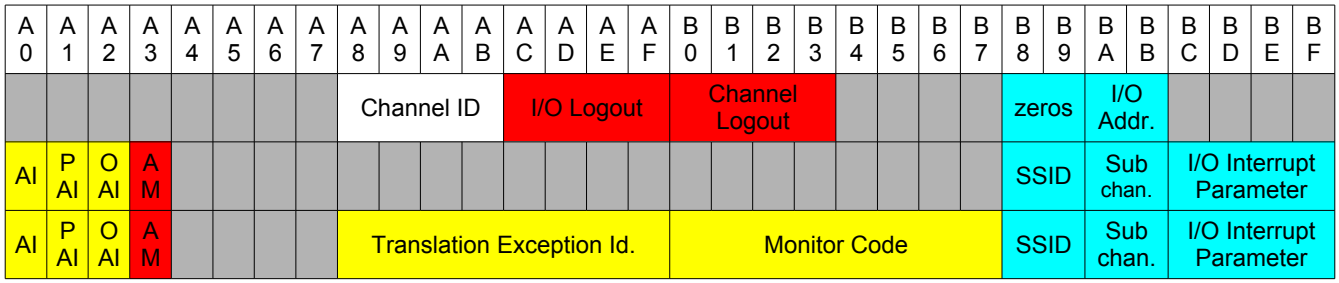
Real Addresses: 60-7F



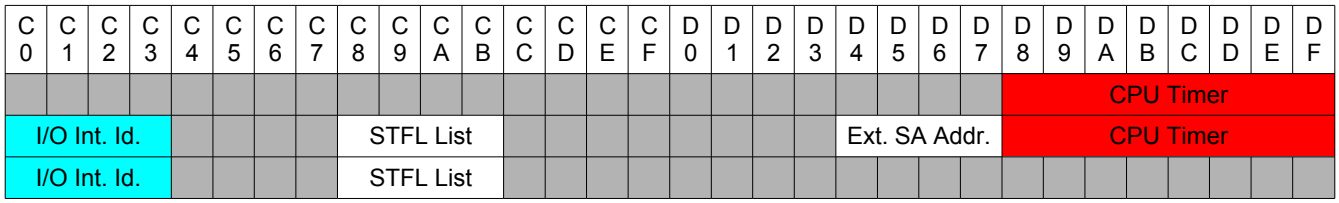
Real Addresses: 80-9F



Real Addresses: A0-BF



Real Addresses: C0-DF



Mainframe Architecture Comparisons

Real Addresses: E0-FF

E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED	EE	EF	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	FA	FB	FC	FD	FE	FF
Clock Comparator SA								Machine Check Inter. Code																Failing Address				Region Code			
Clock Comparator SA								Machine Check Inter. Code												External Damage Code				Failing Address							
								Machine Check Inter. Code												External Damage Code				Failing Address							

Real Addresses: 100-11F

100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E	10F	110	111	112	113	114	115	116	117	118	119	11A	11B	11C	11D	11E	11F
See Diagram Below																															
								Fixed Logout																							
Monitor Count Array Origin								Array Size				Excp. Count				PER Breaking Event Address															

Real Addresses: 100-1FF

100	108	110	118	120	128	130	138	140	148	150	158	160	168	170	178	180	188	190	198	1A0	1A8	1B0	1B8	1C0	1C8	1D0	1D8	1E0	1E8	1F0	1F8
Fixed Logout Area												FP Reg. SA				General Register Save Area								Control Register Save Area							
See Above	Access Register Save Area											FP Reg. SA				General Register Save Area								Control Register Save Area							
See Above	Restart Old		Ext. Old		SVC Old		Pgm. Old					MCk. Old		I/O Old						Restart New		Ext. New		SVC New		Pgm. New		MCk. New		I/O New	

High Address Prefix Area Usage (Addresses 1100-13FF)

Absolute Storage

Absolute Addresses: 1100-11FF

1100	1108	1110	1118	1120	1128	1130	1138	1140	1148	1150	1158	1160	1168	1170	1178	1180	1188	1190	1198	11A0	11A8	11B0	11B8	11C0	11C8	11D0	11D8	11E0	11E8	11F0	11F8

Absolute Addresses: 1200-12FF

1200	1208	1210	1218	1220	1228	1230	1238	1240	1248	1250	1258	1260	1268	1270	1278	1280	1288	1290	1298	12A0	12A8	12B0	12B8	12C0	12C8	12D0	12D8	12E0	12E8	12F0	12F8
Floating Point Register Save Area																General Register Save Area															

Absolute Addresses: 1300-13FF

1300	1308	1310	1318	1320	1328	1330	1338	1340	1348	1350	1358	1360	1368	1370	1378	1380	1388	1390	1398	13A0	13A8	13B0	13B8	13C0	13C8	13D0	13D8	13E0	13E8	13F0	13F8
See Detail Below								Access Register SA								Control Register Save Area															

Absolute Addresses: 1300-131F

1300	1301	1302	1303	1304	1305	2306	1307	1308	1309	130A	130B	130C	130D	130E	130F	1310	1311	1312	1313	1314	1315	1316	1317	1318	1319	131A	131B	131C	131D	131E	131F
Program Status Word Save Area																								Prefix SA				FPC SA			

Absolute Addresses: 1320-133F

1320	1321	1322	1323	1324	1325	2326	1327	1328	1329	132A	132B	132C	132D	132E	132F	1330	1331	1332	1333	1334	1335	1336	1337	1338	1339	133A	133B	133C	133D	133E	133F
				TOD Pgm Reg.				CPU Timer Save Area								Clock Comparator Save Area																	

Real Storage

Real Addresses: 1100-11FF

1100	1108	1110	1118	1120	1128	1130	1138	1140	1148	1150	1158	1160	1168	1170	1178	1180	1188	1190	1198	11A0	11A8	11B0	11B8	11C0	11C8	11D0	11D8	11E0	11E8	11F0	11F8
1																								Available for Programming							

Note 1: Machine-Check-Extended-Save-Area Designation

Real Addresses: 1200-12FF

1200	1208	1210	1218	1220	1228	1230	1238	1240	1248	1250	1258	1260	1268	1270	1278	1280	1288	1290	1298	12A0	12A8	12B0	12B8	12C0	12C8	12D0	12D8	12E0	12E8	12F0	12F8
Floating Point Register Save Area																General Register Save Area															

Real Addresses: 1300-13FF

1300	1308	1310	1318	1320	1328	1330	1338	1340	1348	1350	1358	1360	1368	1370	1378	1380	1388	1390	1398	13A0	13A8	13B0	13B8	13C0	13C8	13D0	13D8	13E0	13E8	13F0	13F8
See Detail Below								Access Register SA								Control Register Save Area															

Real Addresses: 1320-133F

1320	1321	1322	1323	1324	1325	2326	1327	1328	1329	132A	132B	132C	132D	132E	132F	1330	1331	1332	1333	1334	1335	1336	1337	1338	1339	133A	133B	133C	133D	133E	133F
				TOD Pgm Reg.				CPU Timer Save Area								Clock Comparator Save Area																	

Real Addresses: 1800-18FF

1800	1808	1810	1818	1820	1828	1830	1838	1840	1848	1850	1858	1860	1868	1870	1878	1880	1888	1890	1898	18A0	18A8	18B0	18B8	18C0	18C8	18D0	18D8	18E0	18E8	18F0	18F8
Program-Interruption Transaction Diagnostic Block																															

Program Status Word (PSW)

The program status word has different formats and structures depending upon the architecture and modes. The PSW is either 2 words or 4 words (or 4 or 8 half-words). The assigned usage is described in the following table based half-words.

Half Word	0.0	0.1	1.0	1.1	2.0	2.1	3.0	3.1
S/370 BC	Sys State	Int Code	Program State					
S/370 EC	System	Program	Instruction Address					
ESA/390	System	Program	Instruction Address and Basic Address Mode					
z/Architecture	System	Program	Basic Address Mode		Instruction Address			

Three architecture changes affected the format of the Program Status Word:

- Dynamic Address Translation (System/370) - changed the PSW from basic control to the extended control format
- Bimodal 24- or 31-bit Addressing (System 370 Extended Architecture) - added an address mode to the instruction address and
- Trimodal 24-, 31- or 64-bit Addressing (z/Architecture) - extended the PSW from two words to four.

Each of the two or four words are described below in detail using the word detail convention described in the preface. Instead of a single line for System/370, two are used. The first line is for System/370 in basic control mode and the second for System/370 extended control mode.

The different program states influences the ability of the program to alter the content of the PSW. This is illustrated in the diagram by different background colors:

- control program (white) vs.
- problem program (green) vs.
- semi-privileged operations (yellow).

Zero or one indicate required values.

Program Status Word (Bits 0-31)

Byte 0								Byte 1								Byte 2								Byte 3							
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Channel 0-5 Masks						I	E	Key				0	M	W	P	Interruption Code															
0	R	0	0	0	T	I	E	Key				1	M	W	P	S	0	CC		Pgm Masks				0	0	0	0	0	0	0	0
0	R	0	0	0	T	I	E	Key				1	M	W	P	AS		CC		Pgm Masks				0	0	0	0	0	0	0	0
0	R	0	0	0	T	I	E	Key				0	M	W	P	AS		CC		Pgm Masks				0	0	0	0	0	0	0	E
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

Program Status Word (Bits 32-63)

Byte 4								Byte 5								Byte 6								Byte 7							
32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
ILC		CC		Pgm Masks				Instruction Address																							
0	0	0	0	0	0	0	0	Instruction Address																							
A	Instruction Address																														
A	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	28	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63

Program Status Word (Bits 64-127)

Byte 8	Byte 9	Byte 10	Byte 11	Byte 12	Byte 13	Byte 14	Byte 15
64-71	72-79	80-87	88-95	96-103	104-111	112-1219	120-127
Instruction Address							
64-71	72-79	80-87	88-95	96-103	104-111	112-1219	120-127

Control Registers

Controls influencing CR usage and operation

PSW.R=1	PSW.T=1	PSW.I=1	PSW.E=1	PSW.M=1

PSW.AS=00	PSW.AS=01	PSW.AS=10	PSW.AS=11

	Controlled by this CR	CR0 Misc. Controls

Unused/Unassigned

CR	s370	s390	s390x
0	External Interruptions	External Interruptions	External Interruptions
0	Misc. Controls	Misc. Controls	Misc. Controls
1	Primary Space Controls	Primary Space Controls	Primary Space Controls
2	Input/Output	Access-Register Translation	Access-Register Translation
3	Secondary ASN	Secondary ASN	Secondary ASN
3	Authorization	Authorization	Authorization
3			ASN-and-LX Reuse
4	Primary ASN	Primary ASN	Primary ASN
4	Authorization	Authorization	Authorization
4			ASN-and-LX Reuse
5		Access-Register Translation	Access-Register Translation
5	Linkage Table	Linkage Table	
6		Input/Output	Input/Output
7	Secondary Space Controls	Secondary Space Controls	Secondary Space Controls
8	Monitoring	Monitoring	Monitoring
8		Access-Register Translation	Access-Register Translation
9	PER	PER	PER
10	PER	PER	PER
11	PER	PER	PER
12		Tracing	Tracing

CR	s370	s390	s390x
13		Home Space Controls	Home Space Controls
14	Machine Checks	Machine Checks	Machine Checks
14	ASN-translation	ASN-translation	ASN-translation
15	Machine Checks	Linkage Stack	Linkage Stack

Unassigned bits are unpredictable at initialization
Unused bits are set to zero at initialization

The following abbreviations are used in the control register diagrams:

AFP = Additional-floating-point-register Control
ALR = ASN-and-LX-reuse Control
ASF = Address-space-function Control
BM = Block-Multiplexing Control
CC = Clock-comparator subclass Mask
CCS = Clock-comparator sign Control
CRY = Crypto Control
CT = CPU-timer subclass Mask
DAS = Dual-address-space Control
EA = Extraction-authority Control
EC = External-call subclass Mask
EDE = Enhanced-DAT-enablement Control
ETR = External-time-reference subclass Mask
FP = Fetch-protection-override Control
IK = Interrupt-key subclass Mask
IT = Interval-timer subclass Mask
LAP = Low-Address-Protection Control
MA = Malfunction-alert subclass Mask
MAS = Measurement-alert subclass Mask
MC = Measurement-counter-extraction-authorization Control
MS = Emergency-signal subclass Mask
PCF = PROGRAM CALL FAST Control
PS = Page-size Control
SP = Secondary-space Control
SPO = Storage-protection-override Control
SS = Segment-size Control
SSM = SSM-Suppression Control
SVS = Service-signal subclass Mask
TK = TOD-clock sync-check subclass Mask
TS = TOD-Clock-Synchronization Control
TTC = TRACE TOD-clock Control
TX = Transaction-execution Control
TXF = Transaction-execution program-interruption filtering Override

VC = Vector Control
WT= Warning-track-interruption enablement
XS = External-signal subclass Mask

Control Register 0

CR0 Bits 0-31 (64-bit register)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
								TX	TXF	CCS					MC															WT	
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

CR0 Bits: 0-31 (32-bit register), 32-63 (64-bit register)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
BM	SSM	TS	LAP	DAS	SP	?	SPO	PS	PS	0	SS	SS	?	VC	?	MA	MS	EC	TK	CC	CT	SVS	?	IT	IK	XS	?	?	?	IUCV	?
	SSM	TS	LAP	EA	SP	FP	SPO	1	0	1	1	0	AFP	VC	ASF	MA	MS	EC	TK	CC	CT	SVS			IK		ETR	PCF	CRY	IUCV	
TTC	SSM	TS	LAP	EA	SP	FP	SPO	EDE				ALR	AFP	VC		MA	MS	EC		CC	CT	SVS			IK	MAS	ETR		CRY	IUCV	
32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	28	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63

CR	s370 bits	s390 bits	s390x bits	Init.	PSW Control	Description
0			0-7	0		unused
0			8	0		Transaction-execution control
0			9	0		Transaction-execution program-interruption filtering Override
0			10	0		Clock-comparator sign control
0			11-14	0		unused
0			15	0		Measurement-counter-extraction-authorization Control
0			16-29	0		unused
0			30	0	E=1	Warning-track-interruption enablement

CR	s370 bits	s390 bits	s390x bits	Init.	PSW Control	Description
0			31	0		unused
0	0			0		BM - Block-Multiplexing Control
0			32	0		TTC - TRACE TOD-clock Control
0		0		0		unused
0	1	1	33	0		SSM - SSM-Suppression Control
0	2	2	34	0	E=1	TS - TOD-Clock-Synchronization Control
0	3	3	35	0		LAP - Low-Address-Protection Control
0	4			0		DAS - Dual-address-space Control
0		4	36	0	T=1, AS=01	EA - Extraction-authority Control
0	5	5	37	0	T=1	SP - Secondary-space Control
0	6			?		unassigned
0		6	38	0		FP - Fetch-protection-override Control
0	7	7	39	0		SPO -Storage-protection-override Control
0		8-12		0	T=1	Translation Format (10110)
0	8-9			0	T=1	PS - Page-Size Control (01=2K, 10=4K)
0			40	0	T=1	Enhanced-DAT-enablement Control
0			41-43	0		unassigned, must be zero
0	10			0	T=1	unassigned, must be zero
0	11-12			0	T=1	SS - Segment-Size Control (00=64K, 10=1M)
0			44	0		ALR - ASN-and-LX-reuse Control
0	13			?		unassigned
0		13	45	0		AFP - Additional-floating-point-register Control
0	14	14	46	0		Vector enablement Control
0	15			?		unassigned
0		15		0	T=1, AS=01	ASF - Address-space-function Control
0			47	0		unused
0	16	16	48	0	E=1	MA - Malfunction-alert subclass Mask
0	17	17	49	0	E=1	MS - Emergency-signal subclass Mask
0	18	18	50	0	E=1	EX - External-call subclass Mask

CR	s370 bits	s390 bits	s390x bits	Init.	PSW Control	Description
0	19	19		0	E=1	TK - TOD-clock sync-check subclass Mask
0			51	0		unused
0	20	20	52	0	E=1	CC - Clock-comparator subclass Mask
0	21	21	53	0	E=1	CT - CPU-timer subclass Mask
0	22	22	54	0	E=1	SVS - Service-signal subclass Mask
0	23			?		unassigned
0		23	55	0		unused
0	24			1	E=1	IT - Interval-Timer Mask
0		24	56	1		unused
0	25	25	57	1	E=1	IK - Interrupt-key subclass Mask
0	26			1	E=1	XS -External-Signal Mask
0		26	58	1	E=1	Measurement-alert subclass Mask
0	27-29			?		unassigned
0		27	59	0	E=1	ETR - External-time-reference subclass Mask
0		28		0		PCF - Program-call-fast control
0			60			unused
0		29	61	0		CR - Crypto control
0	30	30	62	0	E=1	IUCV – Inter-user Communication Vehicle mask
0	31			?		unassigned
0		31	63	0		unused
1			0-51		T=1, AS=0x	Primary table origin
1	0-7			0	T=1	Primary Segment-Table Length
1		0		0	T=1, AS=00	Primary space-switch-event control
1		1-19		0	T=1, AS=0x	Primary segment table origin
1	8-25			0	T=1	Primary Segment-Table Origin
1			52-53	0		unused
1		22	54	0	T=1, ?	Primary subspace group control
1		23	55	0	T=1, ?	Primary private-space control

CR	s370 bits	s390 bits	s390x bits	Init.	PSW Control	Description
1		24	56	0	R=1	Primary storage-alteration-event control
1	26-30			?		unassigned
	31			0		Space-switch event control
1		25-31		0	T=1, AS=00	Primary segment-table length
1			57	0		Primary space-switch-event control
1			58	0	T=1, AS=0x	Primary real-space control
1			59	0		unused
1			60-61	0	T=1, AS=0x	Primary designation-type control
1			62-63	0	T=1, AS=0x	Primary table length
2	0-31			1		Channel Masks
2		0	0-32	0		unused
2		1-25	33-57	0	T=1, AS=01	Dispatchable-unit-control-table origin
2		26-31				unused
2			58-60	0		unused
2			61	0		Transaction diagnostic scope
2			62-63	0		Transaction diagnostic control
3			0-31	0		Secondary ASN-second-table-entry instance number
3	0-15	0-15	32-47	0	T=1, AS=10	PSW-key mask
3	16-31	16-31	48-63	0	T=1, AS=10	Secondary ASN
4			0-31			Primary ASN-second-table-entry instance number
4	0-15	0-15	32-47	0	T=1, AS=10	Authorization index
4	16-31	16-31	48-63	0	T=1, AS=10	Primary ASN
5			0-32	0		unused
5	0-31			?		unassigned

CR	s370 bits	s390 bits	s390x bits	Init.	PSW Control	Description
5	0	0		0		Subsystem-linkage control (CR0.15=0)
5	1-7			?		unassigned
5		1-24		0		Linkage-table origin (CR0.15=0)
5		8-24		0		Linkage-table origin
5	25-31	25-31		0		Linkage-table length (CR0.15=0)
5		1-25	33-57	0	T=1, AS=01	Primary-ASN-second-table-entry origin (CR0.15=1)
5		26-31	58-63	0		unused
6			0-31	0		unused
6	0-31			?		unassigned
6		0-7	32-39	0		I/O-interruption subclass mask
6		8-31	40-63	0		unused
7	0-7			0		Secondary Segment-table length
7	8-25			0		Secondary segment-table origin
7		0		0		unused
7		1-19		0	T=1, AS=10, 01	Secondary segment-table origin
7		20-21		0		unused
7		22	54	0	T=1, AS=10, 01	Secondary subspace-group control
7		23	55	0	T=1, AS=10, 01	Secondary private-space control
7		24	56	0	R=1	Secondary storage-alteration event control
7		25-31		0	T=1, AS=10, 01	Secondary segment-table length
7			58	0	T=1, AS=10, 01	Secondary real-space control
7			59	0		unused
7			60-61		T=1,	Secondary designation-type control

CR	s370 bits	s390 bits	s390x bits	Init.	PSW Control	Description
					AS=10, 01	
7			62-63	0	T=1, AS=10, 01	Secondary table length
8			0-31	0		unused
8	0-15			?		unassigned
8			16-31	0		Enhanced monitor masks
8		0-15	32-47	0	T=1, AS=01	Extended authorization index
8	16-31	16-31	48-63	0		Monitor masks
9	0	0	32	0	R=1	Successful-Branching-Event Mask
9	1	1	33	0	R=1	Instruction-Fetching-Event Mask
9	2	2	34	0	R=1	Storage-Alteration-Event Mask
9	3	3		0	R=1	GR-Alteration-Event Mask
9			35	0		unused
9	4-15			?		unassigned
9		4	36	0	R=1	Store-using-real-address-event mask
9		5-7		0		unused
9			37	0	R=1	Zero-address-detection-event mask
9			38	0	R=1	Transaction-end-event mask
9			39	0	R=1	Instruction fetching-nullification-event mask
9		8	40	0	R=1	Branch-address control
9		9		0		unused
9			41		R=1	PER-event-suppression control
9		10	42	0	R=1	Storage-alteration-space control
9		11-15	43-63	0		unused
9	16-31	16-31		0	R=1	PER-General-Register-Event Masks
10			0-63	0	R=1	PER starting address
10	0-7			?		unassigned
10		0		0		unused
10		1-31		0	R=1	PER starting address

CR	s370 bits	s390 bits	s390x bits	Init.	PSW Control	Description
10	8-31			0	R=1	PER starting address
11			0-63		R=1	PER ending address
11	0-7			?		unassigned
11		0		0		unused
11		1-31		0	R=1	PER ending address
11	8-31			0	R=1	PER ending address
12	0-31			?		unassigned
12		0	0	0		Branch-trace control
12		1-29		0		Trace-entry address
12			1			Mode-trace control (addressing mode switches)
12			2-61			Trace-entry address
12		30	62	0		ASN-trace control
12		31	63	0		Explicit-trace control
13			0-51		T=1, AS=11	Home table origin
13	0-31			?		unassigned
13		0		0	T=1, AS=11	Home-space-switch event control
13		1-19		0	T=1, AS=11	Home segment-table origin
13		20-21		0		unused
13		22		0	T=1, AS=11	ignored
13		23	55	0	T=1, AS=11	Home private-space control
13		24	56	0	R=1	Home space-alteration event control
13		25-31		0	T=1, AS=11	Home segment-table length
13			57	0		Home space-switch-event control
13			58	0	T=1, AS=11	Home real-space control
13			59	0		unused
13			60-61	0		Home designation-type control

CR	s370 bits	s390 bits	s390x bits	Init.	PSW Control	Description
13			62-63	0		Home table length
14			0-31	0		unused
14	0			1		Check-stop control
14		0	32	1		unused
14	1			1	M=1	Synchronous-MCEL control
14		1	33	1		unused
14	2			0		I/O extended-logout control
14		2		0		Extended save-area control
14			34	0		Extended save-area control (ESA/390 compatibility mode only)
14	3			?		unassigned
14		3	35	0	M=1	Channel-report-pending subclass mask
14	4	4	36	0	M=1	Recovery subclass mask
14	5	5	37	0	M=1	Degradation subclass mask
14	6	6	38	1	M=1	External-damage subclass mask
14	7	7	39	0	M=1	Warning subclass mask
14		8-9	40-41	0		unused
14	8			0	M=1	Asynchronous-MCEL Control
14	9			0	M=1	Asynchronous-Fixed-Log Control
14	10-11			?		unassigned
14		10	42	0		TOD-clock-control-override control
14		11	43	0		unused
14	12	12	44	0	T=1, AS=01	ASN-translation control
14	13-19			?		unassigned
14		13-31	45-63	0	T-1, AS=01	ASN-first-table origin
14	20-31					ASN-first-table origin
15			0-60	0		Linkage-stack-entry address
15	0			?		unassigned
15		0		0		unused

CR	s370 bits	s390 bits	s390x bits	Init.	PSW Control	Description
15		1-28				Linkage-stack-entry address
15	1-7			?		unassigned
15	8-28			512	M=1	MCEL Address
15		29-31	61-63	0		unused

Dynamic Address Translation

Region Table (RT) Attributes (s390x only)	Region First	Region Second	Region Third
RT or ST origin in ASCE (bits)	0-51	0-51	0-51
RT Type in ASCE (bits)	62-63=11	62-63=10	62-63=01
RT Length in ASCE (bits)	60-61	60-61	60-61
Region Size	16 exabytes	8 petabytes	4 terabytes
RT Alignment	4K	4K	4K
RT Units Physical Length	4K	4K	4K
RTE Size (bytes)	8	8	8
RTE's per RT Unit	512 (2**10)	512	512
RTE Invalid in RTE (bit)	58	58	58
RTE Type in RTE (bits)	62-63=11	62-63=10	62-63=01
RTE Offset in RTE (bits)	56-57	56-57	56-57
Storage addressed by RTE	8 petabytes	4 terabytes	2 gigabytes

Segment Table (ST) Attributes	s370	s390	s390x
PSW Controls	T=1	T=1, AS=00, A=0/1	T=1, AS=00, E/BA=00,01,11
DAT Control Registers	1, 7 = x	1, 7, 13 = x	1, 7, 13 = x
ST Origin	CRx.8-25	CRx.1-19	CRx.0-51
Subspace-group control	not applicable	CRx.22	CRx.54
Private-space control	not applicable	CRx.23	CRx.55
Storage-alteration event control	not applicable	CRx.24	CRx.56
Space-switch-event control	CRx.31	CRx.0	CRx.57
Real-space control	not applicable	not applicable	CRx.58=0
ST Length in ST Units	CRx.0-7	CRx.25-31	CRx.62-63
ST Length Range	1-256 minus 1	1-256 minus 1	1-4 minus 1
ST Units Physical Length	64 bytes	64 bytes	4K
STE's per ST Unit	16 page tables	16 page tables	512
Storage addressed per ST Unit	16M	16M	512M

Segment Table (ST) Attributes	s370	s390	s390x
ST Alignment	64-byte	4K	4K
STE Size	4 bytes	4 bytes	8 bytes
PT Origin in STE (bits)	8-28	1-25	0-52
STE invalid (bit)	31	26	58
STE common (bit)	not applicable	27	59
PT Length in PT Units in STE (bits)	0-3	28-31	N/A
PT Length Range in STE	1-16 minus 1	1-16 minus 1	N/A

Page Table (PT) Attributes	s370	s370	s370	s370	s390	s390x
CR0.8-9 (Page Size)	01	01	10	10	10	N/A
CR0.10	0	0	0	0	1	N/A
CR0.11-12 (Segment Size)	00	10	00	10	10	N/A
Page Size (bytes)	2K	2K	4K	4K	4K	4K
PTE Size (bytes)	2	2	2	2	4	8
Segment Size (bytes)	64K	1M	64K	1M	1M	1M
Maximum PTE's per ST	32	512	16	256	256	256
PT Alignment	8-byte	8-byte	8-byte	8-byte	64-byte	8K
Maximum Physical PT Size (bytes)	64	1024	32	512	1024	2048
Maximum PT Units per STE	16	16	16	16	16	N/A
PTE's per Unit	2	32	1	16	16	N/A
Physical Size of PT Unit (bytes)	4	64	2	32	64	N/A
Storage addressed by PT Unit	4K	64K	4K	64K	64K	N/A
Page Origin in PTE (bits)	0-12	0-12	0-11	0-11	1-19	0-51
Page Origin shifted right in PTE	8 bits	8 bits	8 bits	8 bits	0 bits	0 bits
Page Invalid in PTE (bit)	13	13	12	12	21	53
Page protection in PTE (bit)	N/A	N/A	N/A	N/A	22	54

Control Register 0

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
					D			P	S	0	S	S																			
					D			1	0	1	1	0																			
					D																									
32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	28	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63

DAT Control Register

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
STL								Segment-Table Origin																							X
	Segment-Table Origin																					G	P	S	STL						
Segment-Table Origin (bits 0-51)																						G	P	S	X	R		DT		TL	
32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	28	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63

Region Table Entries

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Not Applicable (not used)																															
Not Applicable (not used)																															
Region or Segment Table Origin (bits 0-51)																								TF	I		TT		TL		
32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	28	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63

Segment Table Entries

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
PTL				0	0	0	0	Page-Table Origin																					P	C	I
0	Page-Table Origin																									I	C	PTL			
Page-Table Origin (bits 0-52)																						P				I	C	T	T		
32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	28	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63

Page Table Entries

<table>
<tr><td>0</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td><td>9</td><td>10</td><td>11</td><td>12</td><td>13</td><td>14</td><td>15</td><td>16</td><td>17</td><td>18</td><td>19</td><td>20</td><td>21</td><td>22</td><td>23</td><td>24</td><td>25</td><td>26</td><td>27</td><td>28</td><td>29</td><td>30</td><td>31</td></tr>
<tr><td colspan="12">Page-Frame Real Address</td><td>I</td><td>E</td><td>A</td><td></td><td colspan="20">Not applicable (16-bit PTE's)</td></tr>
<tr><td>0</td><td colspan="19">Page-Frame Real Address</td><td>0</td><td>I</td><td>O</td><td>0</td><td colspan="8"></td></tr>
<tr><td colspan="20">Page-Frame Real Address (bits 0-51)</td><td>0</td><td>I</td><td>O</td><td>0</td><td colspan="8"></td></tr>
<tr><td>32</td><td>33</td><td>34</td><td>35</td><td>36</td><td>37</td><td>38</td><td>39</td><td>40</td><td>41</td><td>42</td><td>43</td><td>44</td><td>45</td><td>46</td><td>47</td><td>28</td><td>49</td><td>50</td><td>51</td><td>52</td><td>53</td><td>54</td><td>55</td><td>56</td><td>57</td><td>58</td><td>59</td><td>60</td><td>61</td><td>62</td><td>63</td></tr>
</table>

Interrupt Information

Interrupt information relating to DAT is always stored in the Translation Exception Identification (TEI) assigned storage location. Additional information may be stored when in Access Register Mode or the MOVE PAGE instruction causes the interruption. Consult the appropriate Principles of Operation manuals in these cases. Further, the TEI assigned storage location is used for conditions that may occur in translation activities other than related to DAT. Consult the appropriate Principles of Operation manuals for the information stored in these cases.

Information related to DAT is stored when handling any of the following DAT-related exceptions:

- ASCE-type,
- Region-first translation,
- Region-second translation,
- Region-third translation,
- Segment translation or
- Page translation.

The first-four will only occur in a z/Architecture environment when DAT is enabled. The last two may occur in all of the architectures when DAT is enabled.

ASCE and Region Translation Exceptions

<table>
<tr><td>0</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td><td>9</td><td>10</td><td>11</td><td>12</td><td>13</td><td>14</td><td>15</td><td>16</td><td>17</td><td>18</td><td>19</td><td>20</td><td>21</td><td>22</td><td>23</td><td>24</td><td>25</td><td>26</td><td>27</td><td>28</td><td>29</td><td>30</td><td>31</td></tr>
<tr><td colspan="32">Not applicable (exception can not occur)
Not applicable (exception can not occur)</td></tr>
<tr><td colspan="20">Address Causing the Exception (bits 0-51)</td><td>?</td><td>?</td><td>?</td><td>?</td><td>?</td><td>?</td><td>?</td><td>?</td><td>?</td><td>?</td><td colspan="2">AS</td></tr>
<tr><td>32</td><td>33</td><td>34</td><td>35</td><td>36</td><td>37</td><td>38</td><td>39</td><td>40</td><td>41</td><td>42</td><td>43</td><td>44</td><td>45</td><td>46</td><td>47</td><td>28</td><td>49</td><td>50</td><td>51</td><td>52</td><td>53</td><td>54</td><td>55</td><td>56</td><td>57</td><td>58</td><td>59</td><td>60</td><td>61</td><td>62</td><td>63</td></tr>
</table>

Segment Exception

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
S	0	0	0	0	0	0	0	SX				PX								?	?	?	?	?	?	?	?	?	?	?	?
S	SX											PX								?	?	?	?	?	?	?	?	?	?	AS	
Address Causing the Exception (bits 0-51)																				?	?	?	?	?	?	?	?	?	?	AS	
32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	28	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63

Page Exception

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
S	0	0	0	0	0	0	0	SX				PX								?	?	?	?	?	?	?	?	?	?	?	?
S	SX											PX								?	?	?	?	?	?	?	?	?	M	AS	
Address Causing the Exception (bits 0-51)																				?	?	?	?	?	?	?	?	?	M	AS	
32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	28	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63

External Interruptions

Assigned Storage	s370	s390	s390x
PSW Control (bit)	7	7	7
Control Registers	0	0	0
CPU Address (A)	x'84'-x'85'	x'84'-x'85'	x'84'-x'85'
Interruption Code	x'86'-x'87'	x'86'-x'87'	x'86'-x'87'
External Interruption Parameter (P)	not applicable	x'80'-x'83'	x'80'-x'83'
Old PSW	x'18'-x'1F'	x'18'-x'1F'	x'130'-x'13F'
New PSW	x'58'-x'5F'	x'58'-x'5F'	x'1B0'-x'1BF'

Interruption	A	P	Interruption Code	s370	s390	s390x
Interval Timer	Y*		0000 0000 1xxx xxxx	CR0.24	N/A	N/A
Interrupt Key	Y*		0000 0000 x1xx xxxx	CR0.25		N/A
Interrupt Key			0000 0000 0100 0000		CR0.25	N/A
External Signal **	Y		0000 0000 xxXX XXXX	CR0.26	N/A	N/A
Malfunction Alert	Y		0001 0010 0000 0000	CR0.16	CR0.16	CR0.48
Emergency Signal	Y		0001 0010 0000 0001	CR0.17	CR0.17	CR0.49
External Call	Y		0001 0010 0000 0010	CR0.18	CR0.18	CR0.50
TOD Clock Sync Ck	Y*		0001 0000 0000 0011	CR0.19	CR0.19	N/A
Clock Comparator	Y*		0001 0000 0000 0100	CR0.20	CR0.20	CR0.52
CPU Timer	Y*		0001 0000 0000 0101	CR0.21	CR0.21	CR0.53
ETR			0001 0100 0000 0110	N/A	CR0.27	N/A
Service Signal		Y	0010 0100 0000 0001	N/A	CR0.22	CR0.54
Timing Alert		Y	0010 0100 0000 0110	N/A	N/A	CR0.59
IUCV Event		***	0100 0000 0000 0000	CR0.30	CR0.30	CR0.62

* CPU Address of zeros is stored by System/370 for this external interruption.
** External signals are associated with the direct-control feature that includes the READ DIRECT and WRITE DIRECT control instructions. The direct-control feature is not supported by Hercules.
*** The real address of the 40-byte IUCV interruption parameter area is provided by the IUCV DECLARE BUFFER function. Two different addresses may be specified, one for control path

interrupts and one for application path interrupts.

Input/Output Interruptions

Assigned Storage	s370	s390	s390x
PSW Control (bit)	6	6	6
Control Registers	2	6	6
Channel Status Word	x'40'-x'47'	not applicable	not applicable
Channel Address Word	x'48'-x'4B'	not applicable	not applicable
Channel ID	x'A8'-x'AB'	not applicable	not applicable
Subsystem Identification	x'B8'-x'B9'	x'B8'-x'B9'	x'B8'-x'B9'
I/O Interruption Source	x'BA'-x'BB'	x'BA'-x'BB'	x'BA'-x'BB'
I/O Interruption Parameter	not applicable	x'BC-x'BF'	x'BC-x'BF'
I/O Interruption Identification Word	not applicable	x'C0'-x'C3'	x'C0'-x'C3'
Old PSW	x'38'-x'3F'	x'38'-x'3F'	x'170'-x'17F'
New PSW	x'78'-x'7F'	x'78'-x'7F'	x'1F0'-x'1FF'

Machine-Check Interruptions

Assigned Storage	s370	s390	s390x
PSW Control (bit)	13	13	13
Control Registers Masks	14	14	14
Machine-Check Extended Logout Address	CR15	not applicable	not applicable
Machine-Check Extended-Save-Area Address	not applicable	x'D4'-x'D7' CR14.2	not applicable
Machine Check Save Areas	x'D8'-x'1FF'	x'D8'-x'1FF'	x'1200'-x'13FF'
Architecture-Mode Identification	not applicable	x'A3'	x'A3'
Machine-Check Interruption Code (MCIC)	x'E8'-x'EF'	x'E8'-x'EF'	x'E8'-x'EF'
External Damage Code	not applicable	x'F4'-x'F7'	x'F4'-x'F7'
Failing Storage Address	x'F8'-x'FB'	x'F8'-x'FB'	x'F8'-x'FF'
Region Code	x'FC'-x'FF'	not applicable	not applicable
Old PSW	x'30'-x'37'	x'30'-x'37'	x'160'-x'16F'
New PSW	x'70'-x'70'	x'70'-x'70'	x'1E0'-x'1EF'

Interruption	MCIC bits	s370	s390	s390x
System Damage Subclass	0	X	X	X
Instruction Processing Damage Subclass	1	X	X	X
System Recovery Subclass	2	CR14.4	CR14.4	CR14.36
Timer Damage Subclass	3	CR14.6		
Timing Facility Damage Subclass	4	CR14.6	CR14.6	CR14.38
External Damage Subclass	5	CR14.6	CR14.6	CR14.38
Vector Facility Failure	6		X	
Degradation Subclass	7	CR14.5	CR14.5	CR14.37
Warning Subclass	8	CR14.7	CF14.7	CR14.39
Channel Report Pending	9		CR14.3	CR14.35
Service Processor Report Damage	10		X	X
Channel Subsystem Damage	11		X	X

Interruption	MCIC bits	s370	s390	s390x
unassigned	12			
Vector-Facility Source	13		X	
Backed Up Occurrence	14	X	X	X
Delayed Occurrence	15	X		
Storage Error Uncorrected	16	X	X	X
Storage Error Corrected	17	X	X	X
Key-in-storage Error Uncorrected	18	X	X	X
Storage Degradation	19		X	X
PSW MWP Validity	20	X	X	X
PSW Masks and Key Validity	21	X	X	X
PSW Program Mask and Condition Code Validity	22	X	X	X
PSW Instruction Address Validity	23	X	X	X
Failing Storage Address Validity	24	X	X	X
Region Code Valid	25	X		
External-Damage Code Validity	26		X	X
Floating Point Registers Validity	27	X	X	X
General Registers Validity	28	X	X	X
Control Registers Validity	29	X	X	X
Logout Valid	30	X		
Storage Logical Validity	31	X	X	X
Indirect Storage Error	32		X	X
Access Register Validity	33		X	X
Delayed Access Exception	34		X	X
unassigned	35-41			
TOD-Programmable-Register Validity	42			X
Extended Floating-Point Validity	43		X	
Floating Point Control Register Validity	43			X
Ancillary Report	44		X	X
unassigned	45			
CPU Timer Validity	46	X	X	X

Interruption	MCIC bits	s370	s390	s390x
Clock Comparator Validity	47	X	X	X
Machine-Check Extended Logout Length	48–63	X		

Control Register 14	Init	s370 bit	s390 bit	s390x bit
Check Stop Control	1	0		
Synchronous Machine Check Logout Control	1	1		
Input/Output Extended Logout Control	0	2		
Extended Save Area Control	0		2	
Channel Report Pending Subclass Mask	0		3	35
Recovery Report Mask	0	4	4	36
Degradation Report Mask	0	5	5	37
External Damage Report Mask	1	6	6	38
Warning Mask	0	7	7	39
Asynchronous Machine Check Extended Logout Control	0	8		
Asynchronous Fixed Logout Control	0	9		

Program Interruptions

Assigned Storage	s370	s390	s390x
PSW Control (bit)	none	none	none
Control Registers	none	none	none
Program Interruption Code	x'8E'-x'8F'	x'8E'-x'8F'	x'C0'-x'C3'
Translation Exception Identification (T)	x'90'-x'93'	x'90'-x'93'	x'A8'-x'AF'
Address Space Number (ASN)	x'90'-x'93'	x'90'-x'93'	x'AC'-x'AF'
PC-number (PCN)	x'90'-x'93'	x'90'-x'93'	x'AC'-x'AF'
Data Exception Code (D)	not applicable	x'93'	x'90'-x'93'
Suppression-on-protection Info. (S)	not applicable	x'90'-x'93'	x'A8'-x'AF'
Monitor Class Number (N)	x'94'-x'95'	x'94'-x'95'	x'94'-x'95'
PER Data (R)	x'98'-x'9B	x'98'-x'9B	x'96'-x'9F'
Monitor Code (M)	x'9C'-x'9F'	x'9C'-x'9F'	x'B0'-x'B7'
Exception Access Identification (A)	not applicable	x'A0'	x'A0'
Access Register Number (ARN)	not applicable	x'A0'	x'A0'
PER Access Identification (P)	not applicable	x'A1'	x'A1'
Operand Access Identification (O)	not applicable	x'A2'	X'A2'
Old PSW	x'28'-x'2F'	x'28'-x'2F'	x'150'-x'15F'
New PSW	x'68'-x'6F'	x'68'-x'6F'	x'1D0'-x'1DF'

Exception	Data	Interruption Code	s370	s390	s390x
Operation		0000 0000 p000 0001	X	X	X
Privileged Operation		0000 0000 p000 0010	X	X	X
Execute		0000 0000 p000 0011	X	X	X
Protection	A*, S*	0000 0000 p000 0100	X	X	X
Addressing		0000 0000 p000 0101	X	X	X
Specification		0000 0000 p000 0110	X	X	X
Data	D*	0000 0000 p000 0111	X	X, FPC, CR0.13	X, FPC, CR0.45

Exception	Data	Interruption Code	s370	s390	s390x
Fixed Point Overflow		xxxx xxxx p000 1000	PSW.20	PSW.20	PSW.20
Fixed Point Divide		0000 0000 p000 1001	X	X	X
Decimal Overflow		0000 0000 p000 1010	PSW.21	PSW.21	PSW.21
Decimal Divide		0000 0000 p000 1011	X	X	X
HFP Exp. Overflow		xxxx xxxx p000 1100	X	X	X
HFP Exp. Underflow		xxxx xxxx p000 1101	PSW.22	PSW.22	PSW.22
HFP Significance		xxxx xxxx p000 1110	PSW.23	PSW.23	PSW.23
HFP-Divide		xxxx xxxx p000 1111	X	X	X
Segment Translation	T,A*,O*	0000 0000 p001 0000	X	X	X
Page Translation	T,A*,O*	0000 0000 p001 0001	X	X	X
Trans. Specification		0000 0000 p001 0010	X	X	X
Special Operation		0000 0000 p001 0011	X	X	X
Operand		0000 0000 p001 0101		X	X
Trace-Table		0000 0000 p001 0110		X	X
ASN-Trans. Spec.		0000 0000 p001 0111	CR0.15	CR0.15	
Vector-Operation		0000 0000 p001 1001	CR0.14	CR0.14	
Space-Switch Event	ASN	0000 0000 p001 1100	X	CR1.0, CR13.0	X
HFP-Square Root		0000 0000 p001 1101		X	X
Unnormalized Opr'nd		xxxx xxxx p001 1110	CR0.14	CR0.14	
PC-Trans. Spec.		0000 0000 p001 1111	X	X	X
AFX Translation	ASN	0000 0000 p010 0000	X	X	X
ASX Translation	ASN	0000 0000 p010 0001	X	X	X
LX-Translation	PCN	0000 0000 p010 0010	X	X	CR0.44
EX-Translation	PCN	0000 0000 p010 0011	X	X	CR0.44
Primary Authority	ASN	0000 0000 p010 0100	X	X	X

Exception	Data	Interruption Code	s370	s390	s390x
Secondary Authority	ASN	0000 0000 p010 0101	X	X	X
LFX-Translation	PCN	0000 0000 p010 0110			CR0.44
LSX-Translation	PCN	0000 0000 p010 0111			CR0.44
ALET-Specification	A	0000 0000 p010 1000		AS=01	AS=01
ALEN-Translation	ARN	0000 0000 p010 1001		AS=01	AS=01
ALE-Sequence	ARN	0000 0000 p010 1010		AS=01	AS=01
ASTE Validity	ARN	0000 0000 p010 1011		AS=01	AS=01
ASTE Sequence	ARN	0000 0000 p010 1100		AS=01	AS=01
Extended Authority	ARN	0000 0000 p010 1101		AS=01	AS=01
LSTE Sequence	PCN	0000 0000 p010 1110			X
ASTE Instance	A	0000 0000 p010 1111			X
Stack-Full		0000 0000 p011 0000		X	X
Stack-Empty		0000 0000 p011 0001		X	X
Stack-Specification		0000 0000 p011 0010		X	X
Stack-Type		0000 0000 p011 0011		X	X
Stack-Operation		0000 0000 p011 0100		X	X
ASCE-Type	T,A,O	0000 0000 p011 1000			X
Region-1st-Trans.	T,A,O	0000 0000 p011 1001			X
Region-2nd-Trans.	T,A,O	0000 0000 p011 1010			X
Region-3rd-Trans.	T,A,O	0000 0000 p011 1011			X
Monitor Event	M,N	0000 0000 p100 0000	CR8.16-31	CR8.16-31	CR8.48-63
Program Event	R,P*	0000 000e 1eee eeee	PSW.1, CR9	PSW.1, CR9	PSW.1, CR9
Crypto Operation		0000 0001 p001 1001		CR0.29	CR0.61

p = May be combined with a Program Event (always 0 on a System/360)
e = May be combined with other exception conditions
x = Exception Extension Code (s390 Vector instructions only)

* = s390 and s390x only

Restart Interruptions

Assigned Storage	s370	s390	s390x
PSW Control (bit)	none	none	none
Control Registers	none	none	none
Old PSW	x'08'-x'0F'	x'08'-x'0F'	x'120'-x'12F'
New PSW	x'00'-x'07'	x'00'-x'07'	x'1A0'-x'1AF'

Supervisor-Call Interruptions

Assigned Storage	s370	s390	s390x
PSW Control (bit)	none	none	none
Control Registers	none	none	none
Supervisor Identification	x'88'-x'8B'	x'88'-x'8B'	x'88'-x'8B'
Old PSW	x'08'-x'0F'	x'08'-x'0F'	x'120'-x'12F'
New PSW	x'00'-x'07'	x'00'-x'07'	x'1A0'-x'1AF'

Features

X=New
B=architecture base
- =Not available
<=Back ported to architecture
Italics indicates features also available in System/360.

External Feature/Facility	S/370	370-XA	ESA/370	ESA/390	z/Arch.
Timing Facilities	X	B	B	B	B
Time-of-Day Clock	X	B	B	B	B
Extended TOD Clock Facility				X	B
TOD-Clock Override Facility				X	B
TOD-Clock Steering Facility					X
Server Time Protocol					X
Clock-Comparator	X	B	B	B	B
CPU Timer	X	B	B	B	B
Interval Timer	B	-	-	-	-
External-Time Reference				X	B
SCLP	X	B	B	B	B
List Directed IPL					X

Input/Output Feature/Facility	S/370	370-XA	ESA/370	ESA/390	z/Arch.
Channel-I/O	B	-	-	-	-
CLRCH	X	-	-	-	-
CLRIO	X	-	-	-	-
HDV	X	-	-	-	-
SIOF	X	-	-	-	-
Channel-Set Switching	X	-	-	-	-
Block-Multiplexor Channel	X	B	B	B	B
Channel Indirect Data Addressing	X	B	B	B	B
31-bit IDAW	X	B	B	B	B
Suspend and Resume	X	B	B	B	B
Channel Subsystem		X	B	B	B

Input/Output Feature/Facility	S/370	370-XA	ESA/370	ESA/390	z/Arch.
Incorrect-Length Suppression Facility		X	B	B	B
XSCH				X	B
Channel Subsystem Call				X	B
Concurrent Sense				X	B
Format-2 IDAW				X	B
64-bit Addresses					X
2K or 4K Blocks					X
I/O Device Self Description				X	B
ORB-extension				X	B
64-bit Addressing					X
I/O Priority					X
Extended I/O Measurement Block					X
Extended I/O Measurement Word					X
MIDAW					X
Console Integration				X	B

CPU Facility/Feature	S/370	370-XA	ESA/370	ESA/390	z/Arch.
Basic-Control Mode	B	-	-	-	-
Extended-Control Mode	X	B	B	B	B
16 General Registers	B	B	B	B	B
64-bit Registers					X
4 Floating Point Registers	X	B	B	B	B
16 Registers				X	B
16 Control Registers	B	B	B	B	B
64-bit Registers					X
16 Access Registers			X	B	B
Bimodal Addressing		X	B	B	B
Trimodal Addressing					X
Extended Real Addressing	X	-	-	-	-
31-bit Addressing		X	B	B	B

CPU Facility/Feature	S/370	370-XA	ESA/370	ESA/390	z/Arch.
64-bit Addressing					X
4K Prefix Area	B	B	B	B	-
8K Prefix Area					X
2K-page protection	B	-	-	-	-
4K-page protection	X	B	B	B	B
ISKE, RRBE, SSKE	X	B	B	B	B
TB	X	B	B	B	B
Expanded Storage	X	B	B	B	B
Protection Facilities		X	B	B	B
Segment Protection	X	B	B	B	B
Access-list controlled protection				X	B
Storage-protection override				X	B
Suppression-on-protection				X	B
Virtual-address enhancements				X	B
Dynamic Address Translation	X	B	B	B	b
LRA, PTLB, RRB, STNSM, STOSM	X	B	B	B	B
Dual Address Space	X	B	B	B	B
Primary Address Space	X	B	B	B	B
Secondary Address Space	X	B	B	B	B
Home-space mode			X	B	B
Access-register mode			X	B	B
Private-space facility			X	B	B
SACF				X	B
Subspace-group facility				X	B
Region Tables					X
ASN-and-LX Reuse facility					X
Control Facilities					
Direct Control	B	-	-	-	-
Program Event Recording	X	B	B	B	B
PER-2				X	B
SIE Extensions				X	B

CPU Facility/Feature	S/370	370-XA	ESA/370	ESA/390	z/Arch.
PER-3					X
Monitoring	X	B	B	B	B
Enhanced-Monitor Facility					X
Tracing Facility		X	B	B	B
Interpretive Execution Facility		X	B	B	B
SIE Improvements				X	B
Asynchronous Pageout Facility				X	-
Asynchronous Datamover Facility				X	-
Architecture Mode Switching					X
IPK, SPKA	X	B	B	B	B
IPT, TPROT	X	B	B	B	B
IPTE-Range Facility					X
MVCSK, MVCDK, MVPG1			X	B	B
MVPG2				X	B
STSI				X	B
New Instructions [detail]					X
SSKE					X
CSPG, IPTE					X
LPTE					X
PC	X	B	B	B	B
Linkage Stack (PC, PR, BAKR)			X	B	B
BSA				X	B
BSG				X	B
Called-space Identification				X	B
PCF				X	B
RP				X	B
Reset-Reference-Bits-Multiple Facility					X
SCP-Initiated Reset				X	B
General Instructions	B	B	B	B	B
Decimal Feature	B	B	B	B	B
Distinct-operands Facility					X

CPU Facility/Feature	S/370	370-XA	ESA/370	ESA/390	z/Arch.
Fast-BCR-Serialization Facility					X
Floating Point	B	B	B	B	B
HFP	X	B	B	B	B
Extended Precision	X	B	B	B	B
Square-Root				X	B
HFP extensions				X	B
HFP Multiply-Add/Subtract					X
Unnormalized Extensions					X
Support Extensions				X	B
64-bit Integer conversions					X
Sign Handling Facility					X
FPR-GR Transfer					X
PFPO					X
BFP				X	B
DFP					X
DFP Rounding Facility					X
IEEE-Exception Simulation					X
Vector Facility	X	B	B	B	-
Vector Extensions				X	-
Compression Facility				X	B
CMPSC-Enhancement Facility					X
Cryptographic Facility				X	B
BAS, BASR	X	B	B	B	B
CS, CDS	X	B	B	B	B
MVCIN	X	B	B	B	B
CFC, UPT		X	B	B	B
CUSE			X	B	B
CKSM				X	B
CLCLE, MVCLE				X	B

CPU Facility/Feature	S/370	370-XA	ESA/370	ESA/390	z/Arch.
CLCLU, MVCLU, PKA, PKU, TP, TROO, TROT, TRTO, TRTT, UNPKA, UNPKU				X	B
ETF2					X
ETF2 Enhancements					X
CUTFU, CUUTF, TRE				X	B
ETF3					X
ETF3 Enhancements					X
MVST, CLST				X	B
PLO				X	B
TRAP2, TRAP4				X	B
CSST					X
ECTG					X
STCKF					X
STFLE					X
Extended Sorting				X	B
High-word Facility					X
Immediate-and-relative Facility				X	B
Extended Immediate Facility					X
Load/Store-on-Condition Facility					X
64-bit Instructions					X
Numerous New Instructions					X
Population Count Facility					X
Trimodal Instructions: BASSM, BSM, SAM24, SAM31, SAM64					X
Modal Instructions					X
Long Displacement Facility					X
Message Security Assist					X
MSA Extension 1					X
MSA Extension 2					X
MSA Extension 3					X
MSA Extension 4					X

Semi-privileged Operations

Privileged operations are exclusively available to a program operating in supervisor state. Non-privileged operations are available to a program operating in either supervisor or problem state. Semi-privileged operations are operations are available to a program in supervisor state and optionally can be made available to a problem state program by a supervisor state program.

At a high level the following semi-privileged capabilities are offered by each architecture.

Capability	S/370EC	370-XA	ESA/370	ESA/390	z/Architecture
ASN Translation	yes	yes	yes	yes	yes
Access-Register Translation	no	no	yes	yes	yes
Subspace Groups	no	no	no	yes	yes
ASN-and-LX Reuse	no	no	no	no	yes

Numerous tables are used by the processor for these operations and they have changed over time. The following table identifies the usage and other attributes of the tables.

Table	Size	S/370 EC	370-XA	ESA/370	ESA/390	z/Arch.
Secondary Space Control	1 bit	CR0.5=1 for PC	CR0.5=1 for PC	CR0.5=1 for MVC(P/S)	CR0.5=1 for MVC(P/S)	CR0.37=1 for MVC(P/S)
Subsystem Linkage Control	1 bit	LTD.0=1 for PC	LTD.0=1 for PC	LTD.0=1 for PC	LTD.0=1 for PC	LTD.0=1 for PC
ASN-Translation Control	1 bit	CR14.12=1 for PC-ss	CR14.12=1 for PC-ss	CR14.12=1 for PC-ss	CR14.12=1 for PC-ss	CR14.44=1 for PC-ss
Address Space Function Control	1 bit	none	none	CR0.15	CR0.15	none
ASN-and-LX Reuse Control	1 bit	none	none	none	none	CR0.44
CR 5 contain Linkage Table Designation	4	yes (bPC only)	yes (bPC only)	CR0.15=0 for bPC	CR0.15=0 for bPC	no
CR 5 contains Primary ASTE	4	no	no	CR0.15=1 for sPC	CR0.15=1 for sPC	yes
Two-level PC-number lookup		yes	yes	yes	yes	CR0.44=0
Linkage Table Designation in Primary ASTE	4	no	no	CR0.15=1	CR0.15=1	CR0.44=0
Linkage Table Entry	4	used	used	CR0.15=0 or CR0.15=1 and	CR0.15=0 or CR0.15=1	CR0.44=0

Table	Size	S/370 EC	370-XA	ESA/370	ESA/390	z/Arch.
				ETE.128=0	and ETE.128=0	
Three-level PC-number lookup		no	no	no	no	CR0.44=1
Linkage First Table Designation is Primary ASTE	4	no	no	no	no	CR0.44=1
Linkage First Table Entry	4	no	no	no	no	CR0.44=1
Linkage Second Table Entry	8	no	no	no	no	CR0.44=1
Entry Table Entry	16	used	used	CR0.15=0	CR0.15=0	no
Entry Table Entry	32	no	no	CR0.15=1	CR0.15=1	used
ASTE found by ASN-translation (for bPC)		yes	yes	CR0.15=0 or CR0.15=1 and ETE.128=0	CR0.15=0 or CR0.15=1 and ETE.128=0	ETE.128=0
ASTE found in ETE (for sPC)		no	no	CR0.15=1 and ETE.128=1	CR0.15=1 and ETE.128=1	ETE.128=1
ASN Second Table Entry	16	used	used	CR0.15=0	CR0.15=0	no
ASN Second Table Entry	64	no	no	CR0.15=1	CR0.15=1	used
Dispatchable Unit Control Table (Format 0)	64	no	no	CR0.15=1	CR0.15=1	no
Dispatchable Unit Control Table (Format 1)	64	no	no	no	no	used
Access-List Designation Format	4	no	no	no	0 or 1	0 only

Two forms of semi-privileged operations are available: basic and stacking operations. Stacking semi-privileged operations are an evolution of the basic operations. Which form of operations is being used is determined by the address-space-function control, bit 15 of control register 0. The effect of the setting of the address-space-function control is summarized below.

Address Space Function Control (CR0.15)	Bit set to zero	Bit set to one
Affected instructions	PROGRAM CALL PROGRAM TRANSFER LOAD ADDRESS SPACE PARAMETERS	PROGRAM CALL PROGRAM TRANSFER LOAD ADDRESS SPACE PARAMETERS
Translation mechanism used	ASN	Access register
ASN second table usage (see detailed description below)	ASN translation definitions	Access register translation definitions and subspace group definitions.

Address Space Function Control (CR0.15)	Bit set to zero	Bit set to one
Enabled Instructions		BRANCH AND SET AUTHORITY BRANCH AND STACK BRANCH IN SUBSPACE GROUP EXTRACT STACKED REGISTERS EXTRACT STACKED STATE MODIFY STACKED STATE PROGRAM RETURN RESUME PROGRAM SET ADDRESS SPACE CONTROL SET ADDRESS SPACE CONTROL FAST TEST ACCESS
Supported program call types	basic only	basic or stacking
Program call type (ETE bit 128 is 0)	always basic	Determined by Entry Table Entry bit 128
PC-ss source of Primary ASN (CR4)	Entry Table Entry	
Control Register 5	Linkage Table Designation	Primary ASN-second-table-entry origin
Linkage Table Designation location	Control Register 5	Primary ASN-second-table entry
Entry Table Entry size	16 bytes	32 bytes
ASN-second-table located	ASN-translation	from Entry Table Entry
ASN-second-table entry boundary	16 bytes	64 bytes
ASN-second-table entry size	16 bytes	64 bytes
Linkage Stack	not available	available
Linkage Stack address space	not applicable	home address space
Linkage Stack address space segment descriptor	not applicable	control register 13
Current Linkage Stack entry address	not applicable	control register 15

ASN-Second Table Entry (ASTE)

The foundation of semi-privileged operations is the ASN (address-space number) Second Table Entry. Fields within the entry are used for three purposes:

1. ASN-translation (address space function control set to 0)
2. Access-register translation (address space function control set to 1)
3. Subspace group definitions (address space function control set to 1)

The following table compares the structure and fields for each of the three usages.

Definition	Acronym	Location	ASN Tran.	AR Tran.	Group
ASTE size			16 bytes	64 bytes	64 bytes

Definition	Acronym	Location	ASN Tran.	AR Tran.	Group
ASX-invalid bit	I	0		X	X
Authority table origin	ATO	1-29	X	X	X
reserved (zero)		30			
Base-space bit	B	31	zero	zero	one
Authorization Index	AX	32-47	X		
Authority table length	ATL	48-49	X	X	
reserved (zeros)		60-63			
Segment table designation	STD	64-95	X	X	X
Space Switch Event Control	X	64	X	X	X
Segment Table Origin	STO	65-83	X	X	X
reserved (zero)		84-85			
Group-space control	G	86	zero	zero	one
Private-space control	P	87	X	X	X
Storage alteration event bit	S	88	X	X	X
Segment Table Length	STL	89-95	X	X	X
Linkage Table Designation	LTD	96-127	X		
Subsystem Linkage Control	V	96	X		
Linkage Table Origin	LTO	97-120	X		
Linkage Table Length	LTL	121-127	X		
Access-List Designation		128-157		X	
ASTE Sequence Number	ASTESN	160-191		X	
reserved (zeros)		191-223			
reserved for program usage		224-255		X	X
reserved (zeros)		256-512			

Semi-privileged operations are provided by means of features. Associated with each feature is a set of controls that define the details of the operations, authorize their usage and optionally a set of semi privileged instructions used to invoke the operations by a program. The following table articulates these features and architectural availability.

Entry Table Entry (ETE)

Transferring control between address spaces utilizes the PROGRAM CALL (PC) instruction which implicitly utilizes PC-number translation to arrive at an ASTE. PC-number translation relies upon a two-stage look up that locates the ETE. As with the ASTE, two different definitions apply to the ETE depending upon the purpose of the tables usage. The following table compares the structure and fields for each of the three usages.

Definition	Acronym	Format 0 (bits)	Format 1 (bits)	ASN Tran.	AR Tran.	Subspace Group
ETE Format		bit 129=0	bit 129=1	0	Bit 129	Bit 129
ETE size *		16 bytes	32 bytes	16 bytes	32 bytes	32 bytes
Authorization key mask		0-15	64-79	X	X	
Address Space Number	ASN	16-31	80-95	X	X	
Entry addressing mode	A	32		X	X	
Entry instruction address		33-62	0-62	X	X	
Entry problem state	P	63	63	X	X	
Entry parameter		64-95	192-255	X	X	
Entry key mask		96-111	96-111			
reserved (zeros)		112-127	112-127			
End of 16-byte ETE						
Linkage Stack fields (Format 0)		128-159				
PC-Type bit	T	128			X	
Entry Extended Addressing Mode	G	129			X	
Linkage Stack fields (Format 1)			130-159		X	
reserved (zeros)		130				
PSW-key Control	K	131	131		X	
PSW-key-mask Control	M	132	132		X	
Extended-authorization-index Control	E	133	133		X	
Address-space Control	C	134	134		X	
Secondary ASN Control	S	135	135		X	
Entry Key	EK	136-139	136-139		X	
reserved (zeros)		140-143	140-143			
Entry Extended Authorization Index		144-159	144-159		X	
reserved (zero)		160	160			
ASTE Origin		161-185	161-185		X	X
reserved (zeros)		186-191	186-191			
reserved (zeros)		186-255				

* For System/370, the ETE is always 16 bytes in length. For z/Architecture, the ETE is always 32 bytes in length with the format determined by bit 129. For ESA/390 the size is determined by CR0.15 but only format 0 is used.

Dispatchable Unit Control Table (DUCT)

Access-register translation introduces the concept of a dispatchable unit as distinguished

from a program. Taken from the ESA/390 or z/Architecture Principles of Operation:

> A program is a sequence of instructions and may be referred to as a program module. A program may be a sequence of calling and called programs. A dispatchable unit, which is sometimes called a process or a task, is a unit of work that is performed through the execution of a program by one CPU at a time.
>
> The dispatchable unit access list is intended to be associated with a dispatchable unit; that is it is intended that a dispatchable unit have the same dispatchable-unit access list regardless of which program is currently being executed to perform the dispatchable unit.
>
> Thus for a dispatachable unit, the dispatchable unit access list is intended to be constant and the primary space access list is a function of which program is being executed, through being a function of the primary address space of the program. Also all dispatchable units and programs in the same primary address space have the same primary-address space access list.

The DUCT is 64 bytes, or 16 four-byte words, in length. The individual words are assigned to specific capabilities associated with access-register translation. The word designations have the following meanings:

- AR = Access register translation
- BSA = BRANCH AND SET AUTHORITY instruction
- SG = Subspace Group
- PGM = Reserved for program usage
- TRAP = TRAP instructions
- Gray background = reserved for future use, should be all zeros.

Word	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Fmt0	SG	SG		SG	AR			PGM	BSA	BSA		TRAP				
Fmt1	SG	SG		SG	AR	BSA		PGM	BSA	BSA		TRAP				

Definition	Acronym	Format 0 (bits)	Format 1 (bits)	AR	SG	TRAP
DUCT size		64 bytes	64 bytes			
Subspace Group controls		Words 0, 1, 3	Words 0, 1, 3			
reserved (zero)		0.0	0.0		X	
Base-ASTE Origin	BASTEO	0.1-25	0.1-25		X	
Subspace Active Bit	SA	1.0	1.0		X	
Subspace ASTE Origin	SSASTEO	1.1-25	1.1-25		X	

Definition	Acronym	Format 0 (bits)	Format 1 (bits)	AR	SG	TRAP
Subspace ASTE Sequence Number	SSASTESN	3.0-31	3.0-31		X	
Dispatchable Unit Access List Designation (Format 0) *	DUALD	Word 4	Word 4	X		
reserved (zero)		4.0	4.0	X		
Real Access-list Origin	ALO	4.1-24	4.1.24	X		
Access-list Length	ALL	4.25-31	4.25.31	X		
Dispatchable Unit Access List Designation (Format 1) **	DUALD	Word 4	Word 4	X		
reserved (zero)		4.0	4.0	X		
Real Access-list Origin	ALO	4.1-23	4.1-23	X		
Access-list Length	ALL	4.24-31	4.24-31	X		
reserved for program use		Word 7	Word 7			
BRANCH AND SET AUTHORITY Save Area		Words 8, 9	Words 5, 8, 9		X	
24- or 31-bit Addressing Mode	A	8.0	9.0		X	
Return Address (24- or 31-bit)		8.1-31	9.1-31		X	
Return Address (64-bit)			Words 8, 9		X	
PSW Key Mask		9.0-15	5.0-15		X	
reserved		9.16-23	5.16-23		X	
PSW Key		9.24-27	5.24-27		X	
Reduced Authority	RA	9.28	5.28		X	
reserved		9.29-30	5.29-30		X	
Problem State	P	9.31	5.31		X	
Trap Controls		Word 10	Word 10			X
reserved (zero)		10.0	10.0			X
TRAP Control Block Home Address		10.1-28	10.1-28			X
reserved (zeros)		10.29-30	10.29-30			X
TRAP Enabled	E	10.31	10.31			X

* Only Format 0 ALD's are supported by z/Architecture

** Requires special configuration in Hercules for ESA/390 to be used. Hercules defaults to Format 0 ALD's.

Basic Program Calls

The Dual Address Space Feature was introduced in System/370 Extended Control mode. It provided the basic program call. The linchpin of the feature is the PROGRAM CALL and PROGRAM TRANSFER instructions. PROGRAM CALL selects a new primary address space and turns the current primary space into the secondary space. The address space is identified by use of a program-call number translated to an Entry Table entry that identifies

the new address space, instruction address and problem or supervisor state of the PSW following the call. Depending upon the new address space identified, either

- the current primary is the target of the call (PROGRAM CALL to current primary) or
- a new address space is the target of the call (PROGRAM CALL with space switching).

PROGRAM CALL to Current Primary

When a PROGRAM CALL to current primary is specified, only the PSW and general registers are updated. A PROGRAM CALL to current primary effectively provides a mechanism for within address space dynamic linking independent of the linked program's location. Because the authorization mechanism is based upon the PSW-key, this is useful for a control program that supports multiple programs within a single address space using PSW-key protection for the real pages backing the virtual storage mappings created by dynamic address translation.

PROGRAM CALL with Space Switching

When a PROGRAM CALL with space switching is identified, the address space number (ASN) in the Entry Table entry is used to identify an ASN Second Table entry from which is established:

- a new Primary Segment Table Designation (CR1),
- a new Linkage Table (CR5),
- a new Primary ASN (CR4) and
- authorization index (CR4).

Following the PROGRAM CALL, data may be moved between the primary and secondary address spaces using the MOVE TO PRIMARY or MOVE TO SECONDARY instructions. Information is saved in general registers as the result of the PROGRAM CALL that is used by the PROGRAM TRANSFER instruction to reverse the effects of the PROGRAM CALL.

Basic Program Call Summary

Controls	Location	Related Program Interruptions	Related Instructions
Address Space Function Control (set to 0)	CR0.15		PROGRAM CALL (basic)
Subsystem Linkage Control (set to 1)	CR5.0		PROGRAM CALL PROGRAM TRANSFER
Linkage Table Origin and Length	CR5		PROGRAM CALL
Linkage Table	Real	LX-translation PC-translation specification	PROGRAM CALL
Entry Table	Real	EX-Translation PC-translation	PROGRAM CALL

Controls	Location	Related Program Interruptions	Related Instructions
		specification	
Space Switch Event	CR1.31	Space-switch event	PROGRAM CALL PROGRAM TRANSFER
ASN Translation Control	CR14.12		LOAD ADDRESS SPACE PARAMETERS SET SECONDARY ASN
ASN First Table Origin	CR14.20-31		
ASN First Table	Real	AFX-translation ASN-translation specification Primary Authority	LOAD ADDRESS SPACE PARAMETERS PROGRAM CALL with space switching PROGRAM TRANSFER with space switching SET SECONDARY ASN with space switching
ASN Second Table (16-byte entries)	Real	ASN-translation specification	LOAD ADDRESS SPACE PARAMETERS PROGRAM CALL with space switching PROGRAM TRANSFER with space switching SET SECONDARY ASN with space switching
Primary ASN Second Table entry (16-bytes)	Real	ASN-translation specification ASX translation	LOAD ADDRESS SPACE PARAMETERS PROGRAM CALL with space switching PROGRAM TRANSFER with space switching SET SECONDARY ASN with space switching
Authority Table	Real	Primary Authority Secondary Authority	PROGRAM TRANSFER with space switching SET SECONDARY ASN
Address Space Control	PSW.16		EXECUTE INSERT ADDRESS SPACE CONTROL LOAD REAL ADDRESS SET ADDRESS SPACE CONTROL
PSW key	PSW.8-11		INSERT PSW KEY
Secondary Space Control	CR0.5		MOVE TO PRIMARY MOVE TO SECONDARY
Primary Segment Table Designation	CR1		PROGRAM CALL MOVE TO PRIMARY MOVE TO SECONDARY
Secondary Segment Table Designation	CR7		MOVE TO PRIMARY MOVE TO SECONDARY
Authorization Index	CR4.0-15	Primary Authority	PROGRAM CALL with space switching PROGRAM TRANSFER with space switching
Primary ASN	CR4.16-31		EXTRACT PRIMARY ASN LOAD ADDRESS SPACE PARAMETERS

Controls	Location	Related Program Interruptions	Related Instructions
			PROGRAM CALL
PSW Key Mask	CR3.0-15		MOVE WITH KEY PROGRAM CALL
Secondary ASN	CR3.16-31		EXTRACT SECONDARY ASN PROGRAM CALL
Extraction Authority Control	CR0.4		EXTRACT PRIMARY ASN EXTRACT SECONDARY ASN INSERT ADDRESS SPACE CONTROL INSERT PSW KEY INSERT VIRTUAL STORAGE KEY

Stacking Program Calls

Appendix A - Assigned Storage Detail

Overlapping areas are highlighted in different colors. **Bold** font indicates absolute storage locations. Normal font indicates real storage locations. 'X' indicates it is assigned. Colors indicate what enables the locations usage. Externally initiated functions are identified in brown. Descriptions in italics were also present in System/360.

From	To	s370	s390	s390x	Description
0000	1FFF			X	2-page per-CPU Prefix Area
0000	0FFF	X	X		1-page per-CPU Prefix Area
0000	**0007**	X	X	X	***Initial Program Load Program Status Word***
0000	0007	X	X		Restart New Program Status Word
0008	**000F**	X	X	X	***Initial Program Load Channel Command Word 1***
0008	000F	X	X		Restart Old Program Status Word
0010	**0017**	X	X	X	***Initial Program Load Channel Command Word 2***
0010	0013				reserved (MVS CVT pointer)
0014	0017				reserved (DOS COMREG pointer)
0018	001F	PSW.E	PSW.E		*External Old Program Status Word*
0020	0027	X	X		*Supervisor Call Old Program Status Word*
0028	002F	X	X		*Program Old Program Status Word*
0030	0037	PSW.M	PSW.M		*Machine-Check Old Program Status Word*
0038	003F	PSW.I	PSW.I		*Input-Output Old Program Status Word*
0040	0047	PSW.I			*Channel Status Word*
0048	004B	PSW.I			*Channel Address Word*
004C	004F				reserved (MVS CVT pointer)
0050	0053	X			*Interval Timer*
0054	0057	X			Trace-Table Designation Word
0058	005F	PSW.E	PSW.E		*External New Program Status Word*
0060	0067	X	X		*Supervisor Call New Program Status Word*
0068	006F	X	X		*Program New Program Status Word*
0070	0077	PSW.M	PSW.M		*Machine Check New Program Status Word*

From	To	s370	s390	s390x	Description
0078	007F	PSW.I	PSW.I		*Input-Output New Program Status Word*
0080	0083		PSW.E	PSW.E	External Interruption Parameter
0084	0085	PSW.E	PSW.E	PSW.E	Processor Address
0086	0087	PSW.E	PSW.E	PSW.E	External Interruption Code
0088	008B	X	X	X	Supervisor Call Interruption Identification
008C	008F	X	X	X	Program Interruption Identification
0090	0093	PSW.T	PSW.T		Translation Exception Identification
0090	0093			X	Data Exception Code
0093			X		Data Exception Code
0094	0095	CR8. 16-31	CR8. 16-31	CR8. 48-63	Monitor Class Number
0096	0097	PSW.R	PSW.R		Program Event Recording Code
0098	009F			PSW.R	Program Event Recording Address
0098	009B	PSW.R	PSW.R		Program Event Recording Address
009C	009F	CR8.16 -31	CR8.16 -31		Monitor Code
00A0			PSW. AS=01	PSW. AS=01	Exception Access Identification
00A1			PSW.R	PSW.R	Program Event Recording Access Identification (PSW.AS=01)
00A2			X	X	Operand Access Identification (MOVE PAGE)
00A3			PSW.M	PSW.M	**Store-Status Architectural Mode Identification**
00A4	00A7				reserved
00A8	00AF			PSW.T	Translation Exception Identification
00A8	00AB	X			Channel ID
00AC	00AF	CR14.2			Input/Output Extended Logout Address
00B0	00B7			CR8. 48-63	Monitor Code
00B0	00B3	X			Limited Channel Logout
00B8		X			reserved
00B8			PSW.I	PSW.I	x'00' stored (Subsystem Identification Word)
00B9		PSW.I			x'00' (or Measurement Byte stored if SIOF facility is installed) on I/O interruption

From	To	s370	s390	s390x	Description
00B9			PSW.I	PSW.I	B'000000xx1' (Subsystem Identification Word)
00BA	00BB	PSW.I			Input/Output Address
00BA	00BB		PSW.I	PSW.I	Subchannel (Subsystem Identification Word)
00BC	00BF		PSW.I	PSW.I	Input/Output Interruption Parameter
00C0	00C3		PSW.I	PSW.I	Input/Output Interruption-Identification Word
00C8	00CB		X	X	STFL Facility List
00CC	00D3				reserved
00D4	**00D7**		X		**Store-Status Extended-Save-Area Address**
00D4	00D7		PSW.M		Machine-Check Extended-Save-Area Address
00D8	**00DF**	X	X		**Store-Status CPU Timer Save Area**
00D8	00DF	PSW.M	PSW.M		Machine-Check CPU Timer Save Area
00E0	**00E7**	X	X		**Store-Status Clock Comparator Save Area**
00E0	00E7	PSW.M	PSW.M		Machine-Check Clock Comparator Save Area
00E8	00EF	PSW.M	PSW.M	PSW.M	Machine-Check Interruption Code
00F0	00F3				reserved
00F4	00F7		PSW.M	PSW.M	External Damage Code
00F8	00FF			PSW.M	Failing Storage Address
00F8	00FB	PSW.M	PSW.M		Failing Storage Address
00FC	00FF	PSW.M			Region Code
0100	**0107**	X	X		**Store-Status Program Status Word Save Area**
0108	**010B**	X	X		**Store-Status Prefix Save Area**
0108	010F		PSW.M		Fixed Logout Area
010C	**010F**	X			**Store-Status Model Dependent Feature Area**
0100	015F	PSW.M			Fixed Logout Area
0120	**015F**		X		**Store-Status Access Register Save Area**
0120	015F		PSW.M		Machine-Check Access Register Save Area
0120	012F			X	Restart Old Program Status Word
0130	013F			PSW.E	External Old Program Status Word
0140	014F			X	Supervisor Call Old Program Status Word
0150	015F			X	Program Old Program Status Word
0160	**017F**	X	X		**Store-Status Floating-Point Register Save Area**

From	To	s370	s390	s390x	Description
0160	017F	PSW.M	PSW.M		Machine-Check Floating-Point Register Save Area
0160	016F			PSW.M	Machine-Check Old Program Status Word
0170	017F			PSW.I	Input/Output Old Program Status Word
0180	**01BF**	X	X		**Store-Status General Register Save Area**
0180	01BF	PSW.M	PSW.M		Machine-Check General Register Save Area
01A0	01AF			X	Restart New Program Status Word
01B0	01BF			PSW.E	External New Program Status Word
01C0	**01FF**	X	X		**Store-Status Control Register Save Area**
01C0	01FF	PSW.M	PSW.M		Machine-Check Control Register Save Area
01C0	01CF			X	Supervisor-Call New Program Status Word
01D0	01DF			X	Program New Program Status Word
01E0	01EF			PSW.M	Machine-Check New Program Status Word
01F0	01FF			PSW.I	Input/Output New Program Status Word
0200	11FF	X	X	X	4096-bytes available to programming
1200	13FF	X	X		Available for programming
1200	**127F**			X	**Store-Status Floating-Point Register Save Area**
1200	127F			PSW.M	Machine-Check Floating-Point Register Save Area
1280	**12FF**			X	**Store-Status General-Register Save Area**
1280	12FF			PSW.M	Machine-Check General-Register Save Area
1300	**130F**			X	**Store-Status Program Status Word Save Area**
1300	130F			PSW.M	Machine-Check Fixed Logout Area
1310	1317			X	reserved
1318	**131B**			X	**Store-Status Prefix Save Area**
131C	**131F**			X	**Store-Status Floating-Point-Control-Register Save Area**
131C	131F			PSW.M	Machine-Check Floating-Point-Control-Register Save Area
1320	1323			X	reserved
1324	**1327**			X	**Store-Status Time-of-Day-Programmable-Register Save Area**
1324	1327			PSW.M	Machine-Check Time-of-Day-Programmable-Register Save Area

From	To	s370	s390	s390x	Description
1328	**132F**			X	**Store-Status CPU-Timer Save Area**
1328	132F			PSW.M	Machine-Check CPU-Timer Save Area
1330	**1337**			X	**Store-Status Clock-Comparator Save Area**
1330	1337			PSW.M	Machine-Check Clock-Comparator Save Area
1338	133F			X	reserved
1340	**137F**			X	**Store-Status Access-Register Save Area**
1340	137F			PSW.M	Machine-Check Access-Register Save Area
1380	**13FF**			X	**Store-Status Control-Register Save Area**
1380	13FF			PSW.M	Machine-Check Control-Register Save Area
1400	1FFF	X	X	X	Available for programming