CVSD Final Report: QR Decomposition R12921088 周志芳

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QR decomposition algorithm introduction:

我們使用的演算法是直接使用助教給的 0~3 iteration。主要是使用 Modified Gram-Schmidt 進行矩陣的 QR 分解，和投影片中給的李宏毅老師教的 Gram-Schmidt 主要差在計算投影的方式。在 Modified Gram-Schmidt 中，我們會即時更新正交基底，而不是像 Gram-Schmidt 一樣一次性計算所有投影。而這樣做的原因是因為硬體在計算上會有精度的問題，透過 Modified Gram-Schmidt 方法可以減少一般 Gram-Schmidt 計算造成的累積誤差。

FXP setting:

我們的小數計算流程如下：

Iteration 0:

S1.22 H1~H4 input -> 進行平方相加 -> 小數點變 44 位 -> 捨棄 16 位 -> 變成 28 位小數 -> 開根號 -> 變成 14 位小數 -> 捨棄 6 位 -> 得到 8 位小數 r11 再補到 s3.16。

算出 e1 之後進行 h' = h(s1.22) – R(s3.16)*e(s3.16)，然後 h'取小數 16 位，為 s7.16。

Iteration 1, 2, 3:

將算出來的 24bit s7.16 進行平方運算，得到 32 位小數 -> 捨棄 16 位 -> 變成 16 位小數 -> 開根號 -> 變成 8 位小數再補到 s3.16（r22, r33, r44）-> 再進行前面的 h' = h(s1.22)-R(s3.16)*e(s3.16) 運算。

討論：

我們嘗試過全部保留、捨棄 18 位、捨棄 16 位、捨棄 12 位四種方法。

但全部保留以及捨棄 12 位都會讓 sqrt_pipeline 的 latency 太高導致 synthesis 時無法壓下來。

最後剩下 16 和 18 在選，而這兩者的面積只差三萬，所以我們選擇 16 bit 因為有較低的 error rate。

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Error rate:

SNR10 P1: The soft error rate is 1.0279%

SNR10 P2: The soft error rate is 1.1972%

SNR10 P3: The soft error rate is 0.89956%

SNR15 P4: The soft error rate is 0.63882%

SNR15 P5: The soft error rate is 0.74173%

SNR15 P6: The soft error rate is 0.80651%

HW Implementation:

硬體運用:

Sram256x8:x6

Dw_sqrt_pipe:x1

Dw02_mult_2_stagea:x12

CORDIC_Div:x8

Register:

[47:0]REG[19:0]

[39:0]output_w[3:0]

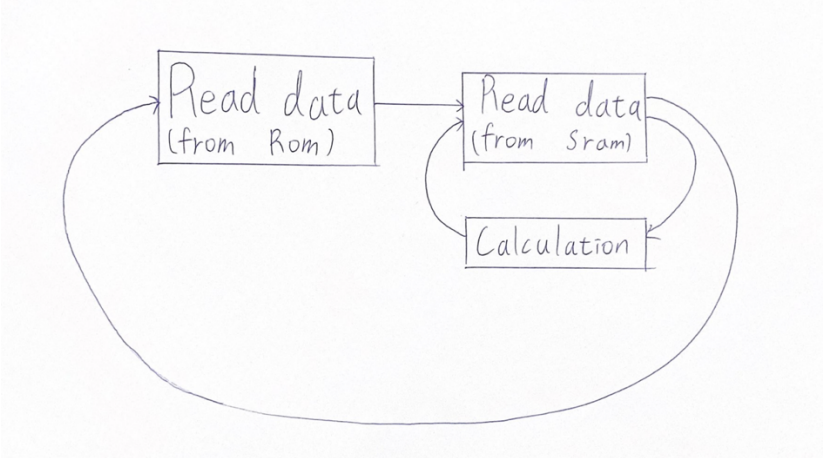
[7:0]cal_ind

[7:0]Addr_Load

[4:0]ind

HW Block Diagram:

Main Block:

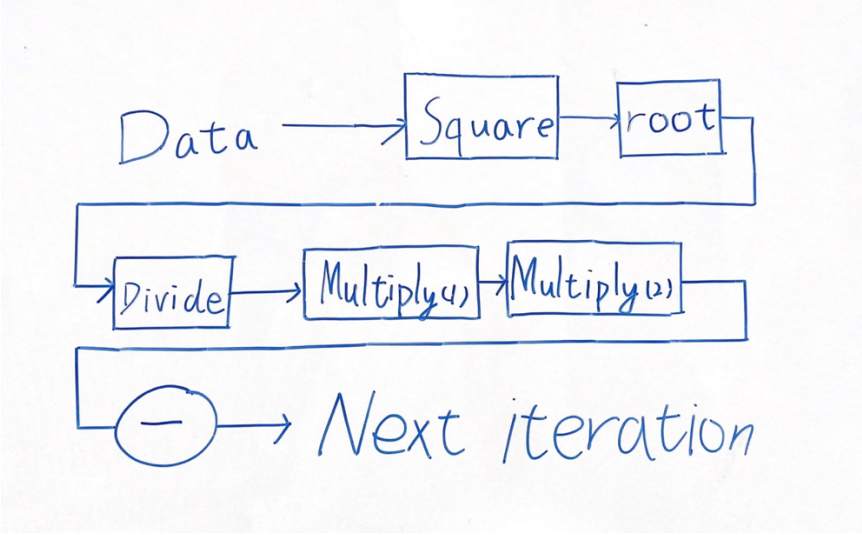


Read data (from Rom):

從 ROM 讀取 200 筆資料進入 SRAM，而當所有資料計算完畢之後再讀取 200 筆。

Read data(from SRAM)：將資料從 SRAM 中讀出並每次放 20 筆資料到 register 計算。

Calculation block:



以下以 iteration0 為例：

Square block：

將 h_1^(0)中 4 筆資料的實部與虛部各自與相同的值放入乘法器並得到平方的結果。

Root block:

將前結果放入 design ware 根號器得到 root。

Divide block:

將 h_1^(0)的 4 筆資料與 root 相除得到單位向量 e。此過程我們使用的方式是 Cordic 的除法運算。

Multiply(1) block:

將 e1 與 h_2^(0) h_3^(0) h_4^(0) 做內積得到 R12 R13 R14。

Multiply(2) block:

將 R12 R13 R14 與 e1 相乘。

Minus block:

將 h_2^(0) h_3^(0) h_4^(0)分別與 R 及 r 的乘積相減完成投影計算。

HW Scheduling:

我們的實作可以分為兩個階段，第一階段為讀取資料，第二階段為運算。

先用 200 個 cycle 將資料放到 sram 裡，再用 20 個 cycle 將資料放到 REG 中，準備之後的計算。

我們使用的 qr 分解演算法跟助教所提供的是相同的，可以大致分為四個 iteration 並在每個 iteration 中執行同樣的算法，以下詳述每一個 iteration 所做的運算:

1. 平方
2. 開根號
3. 計算單位向量(e)

4. 將單位向量(e)與剩餘向量相乘得出 R

5. 將 h^(i-1)-R 與單位向量(e)相乘得出 h^(i)

而計算完此四個 iteration 總共需要 138 個 cycle。

Area:

```
************************** Analyze Floorplan **************************
    Die Area(um^2)             : 2533770.27
    Core Area(um^2)            : 2048851.76
    Chip Density (Counting Std Cells and MACROs and IOs): 77.913%
    Core Density (Counting Std Cells and MACROs): 96.353%
    Average utilization        : 100.000%
    Number of instance(s)      : 225526
    Number of Macro(s)         : 6
    Number of IO Pin(s)        : 533
    Number of Power Domain(s) : 0
************************** Estimation Results **************************
************************************************************************
```

Power

```
  Attributes
  ----------
      i  -  Including register clock pin internal power
      u  -  User defined power group

                        Internal  Switching  Leakage    Total
Power Group             Power     Power      Power      Power   (     %)  Attrs
------------------------------------------------------------------------------
clock_network           2.136e-03 3.367e-03 4.031e-06 5.506e-03 ( 7.91%)
register                   0.0280 2.826e-04 1.620e-04    0.0285 (40.90%)  i
combinational              0.0124 6.982e-03 6.875e-04    0.0201 (28.87%)
sequential                 0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory                     0.0155 6.726e-06 6.600e-05    0.0155 (22.32%)
io_pad                     0.0000    0.0000    0.0000    0.0000 ( 0.00%)
black_box                  0.0000    0.0000    0.0000    0.0000 ( 0.00%)

  Net Switching Power  =    0.0106   (15.28%)
  Cell Internal Power  =    0.0581   (83.40%)
  Cell Leakage Power   = 9.195e-04   ( 1.32%)
                         ---------
Total Power            =    0.0696  (100.00%)

X Transition Power     = 1.101e-07
Glitching Power        = 1.227e-04

Peak Power             =    1.3703
Peak Time              =    33.303

1
report_power -verbose > try_active.power
# exitInformation: Defining new variable 'CYCLE'. (CMD-041)
```

Slack:

我們合成設定的 clock period 為 4.93 ns，並達到 slack met。

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 20
Design : QR_Engine
Version: U-2022.12
Date   : Mon Dec 18 02:43:04 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

 Operating Conditions: slow   Library: slow
 Wire Load Model Mode: top

  Startpoint: cal_ind_reg[4]
              (rising edge-triggered flip-flop clocked by i_clk)
  Endpoint: MULT6/mult_x_1/i_clk_r_REG47_S1
            (rising edge-triggered flip-flop clocked by i_clk)
  Path Group: i_clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  QR_Engine          tsmc13_wl10           slow

  Point                                                   Incr       Path
  ------------------------------------------------------------------------
  clock i_clk (rise edge)                                 0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  cal_ind_reg[4]/CK (DFFRX4)                              0.00 #     0.00 r
  cal_ind_reg[4]/QN (DFFRX4)                              0.54       0.54 r
  U11743/Y (NOR3X4)                                       0.22       0.76 f
  U11723/Y (NAND2X2)                                      0.20       0.95 r
  U22570/Y (NAND3X8)                                      0.17       1.12 f
  U18546/Y (NOR2X6)                                       0.15       1.27 r
  U17344/Y (INVX12)                                       0.10       1.37 f
  U11606/Y (INVX16)                                       0.10       1.47 r
  U11342/Y (INVX16)                                       0.07       1.54 f
  U13966/Y (AND2X2)                                       0.20       1.74 f
  U14778/Y (NOR2X4)                                       0.13       1.87 r
  U21552/Y (NAND4BX4)                                     0.13       1.99 f
  U21551/Y (NAND4BBX4)                                    0.22       2.21 f
  MULT6/B[2] (QR_Engine_DW02_mult_2_stage_J1_6)           0.00       2.21 f
  MULT6/U625/Y (XNOR2X4)                                  0.27       2.48 r
  MULT6/U1072/Y (AND2X8)                                  0.23       2.70 r
  MULT6/U370/Y (INVX12)                                   0.09       2.80 f
  MULT6/U614/Y (INVX4)                                    0.08       2.88 r
  MULT6/U628/Y (NAND2X6)                                  0.07       2.94 f
  MULT6/U627/Y (NAND2X6)                                  0.08       3.02 r
  MULT6/U631/Y (CLKXOR2X2)                                0.31       3.33 f
MULT6/U323/CO (ADDFHX2)                                   0.40       3.73 f
MULT6/U322/S (ADDFHX2)                                    0.37       4.10 r
MULT6/U1595/S (ADDFHX4)                                   0.31       4.41 f
MULT6/U1236/S (ADDFHX2)                                   0.27       4.68 f
MULT6/mult_x_1/i_clk_r_REG47_S1/D (DFFHQX4)               0.00       4.68 f
data arrival time                                                    4.68

clock i_clk (rise edge)                                   4.93       4.93
clock network delay (ideal)                               0.00       4.93
clock uncertainty                                        -0.10       4.83
MULT6/mult_x_1/i_clk_r_REG47_S1/CK (DFFHQX4)              0.00       4.83 r
library setup time                                       -0.15       4.68
data required time                                                   4.68
------------------------------------------------------------------------
data required time                                                   4.68
data arrival time                                                   -4.68
------------------------------------------------------------------------
slack (MET)                                                          0.00
```

Packet1 latency:

```
Pattern   26#: Golden_r = 0966cffe02ffcca0286001632ff61dfd4550d9c7f5cf8ff700f91ba034c00c3de00e2bf7b2e0e7a8
Pattern   26#: Output_r = 09600ffe04ffcbf028c101662ff61bfd44c0d800f5b68ff6e7f91c3034b80c20000e27f7b280e7a8
Pattern   26#: Golden_y_hat = 0516e0d05b0822ef6a1715b89117c70cb61f1dd4
Pattern   26#: Output_y_hat = 052240ce5b07f8af6e0515ed911a6b0cb48f1dc4
Pattern   27#: Golden_r = 08d24fe58afd283fb607049d000df4032e305a3dfee75fd76dfb83cf83800769bffeb6f8fc710286
Pattern   27#: Output_r = 08c00fe56cfd275fb5a704a3e00df7032eb05a00fee5cfd731fb83af837607600ffeb7f8fc010280
Pattern   27#: Golden_y_hat = fe2b206f3609a2402c2ded871025c7ee482f23ba
Pattern   27#: Output_y_hat = fe3da06e09098e102b91ed6c9025e9ee476f23b2
Pattern   28#: Golden_r = 08f6500dcbfe41bfb888ff1a0fcb45fd6b40a612f7137064e60296a031f50967d030d30b6fc10fe3
Pattern   28#: Output_r = 08e0000dccfe41bfb84aff190fcb47fd6b70a600f70c20652e02967031fa09600030d30b6f210fe0
Pattern   28#: Golden_y_hat = f8da8f5846f42aa0a605f1086f49aaf2f240e97a
Pattern   28#: Output_y_hat = f8d3ef5556f446f0a545f0fb5f492af2f1c0e975
Pattern   29#: Golden_r = 03349fd6530189dfed2f0cfb00062800614139db012c1fd60e02402ff4ac0b34afa731fa6c509917
Pattern   29#: Output_r = 03200fd612018c0fed100d12d006240060d13800012e3fd5c002402ff4af0b200fa72afa6ba09910
Pattern   29#: Golden_y_hat = ffd4c01a1012c19ef3c411b17f758af64740af05
Pattern   29#: Output_y_hat = fee7e0299f12e4eef1a711d04f748af64670af11
Pattern   30#: Golden_r = 016d607df1fc5200193f016ddfc5ccf57ea0c648fcd48003cb063f8fd9d806da5f714afad080d758
Pattern   30#: Output_r = 0160007e12fc510019b001736fc5cdf57df0c600fcc7c003e906400fd9db06c00f7146fad040d758
Pattern   30#: Golden_y_hat = fa6a7078180d6a1ff22efbdb20a26604934f1a16
Pattern   30#: Output_y_hat = fa5c007b9c0d59eff180fbcd90a4de0493cf1a06
Pattern    1# ~  100# are written
Pattern  101# ~  200# are written
Pattern  201# ~  300# are written
Pattern  301# ~  400# are written
Pattern  401# ~  500# are written
Pattern  501# ~  600# are written
Pattern  601# ~  700# are written
Pattern  701# ~  800# are written
Pattern  801# ~  900# are written
Pattern  901# ~ 1000# are written
$finish called from file "./testfixture-3.v", line 340.
$finish at simulation time           895026500
           V C S   S i m u l a t i o n   R e p o r t
Time: 895026500 ps
CPU Time:   1272.910 seconds;       Data structure size:  18.6Mb
Tue Dec 19 07:08:38 2023
```

DRC:

```
  VERIFY DRC ..... Sub-Area : 43 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {579.360 965.600 772.480 1158.720} 44 of 64
  VERIFY DRC ..... Sub-Area : 44 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {772.480 965.600 965.600 1158.720} 45 of 64
  VERIFY DRC ..... Sub-Area : 45 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {965.600 965.600 1158.720 1158.720} 46 of 64
  VERIFY DRC ..... Sub-Area : 46 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {1158.720 965.600 1351.840 1158.720} 47 of 64
  VERIFY DRC ..... Sub-Area : 47 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {1351.840 965.600 1542.380 1158.720} 48 of 64
  VERIFY DRC ..... Sub-Area : 48 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {0.000 1158.720 193.120 1351.840} 49 of 64
  VERIFY DRC ..... Sub-Area : 49 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {193.120 1158.720 386.240 1351.840} 50 of 64
  VERIFY DRC ..... Sub-Area : 50 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {386.240 1158.720 579.360 1351.840} 51 of 64
  VERIFY DRC ..... Sub-Area : 51 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {579.360 1158.720 772.480 1351.840} 52 of 64
  VERIFY DRC ..... Sub-Area : 52 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {772.480 1158.720 965.600 1351.840} 53 of 64
  VERIFY DRC ..... Sub-Area : 53 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {965.600 1158.720 1158.720 1351.840} 54 of 64
  VERIFY DRC ..... Sub-Area : 54 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {1158.720 1158.720 1351.840 1351.840} 55 of 64
  VERIFY DRC ..... Sub-Area : 55 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {1351.840 1158.720 1542.380 1351.840} 56 of 64
  VERIFY DRC ..... Sub-Area : 56 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {0.000 1351.840 193.120 1537.090} 57 of 64
  VERIFY DRC ..... Sub-Area : 57 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {193.120 1351.840 386.240 1537.090} 58 of 64
  VERIFY DRC ..... Sub-Area : 58 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {386.240 1351.840 579.360 1537.090} 59 of 64
  VERIFY DRC ..... Sub-Area : 59 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {579.360 1351.840 772.480 1537.090} 60 of 64
  VERIFY DRC ..... Sub-Area : 60 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {772.480 1351.840 965.600 1537.090} 61 of 64
  VERIFY DRC ..... Sub-Area : 61 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {965.600 1351.840 1158.720 1537.090} 62 of 64
  VERIFY DRC ..... Sub-Area : 62 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {1158.720 1351.840 1351.840 1537.090} 63 of 64
  VERIFY DRC ..... Sub-Area : 63 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {1351.840 1351.840 1542.380 1537.090} 64 of 64
  VERIFY DRC ..... Sub-Area : 64 complete 0 Viols.

  Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:38.7  ELAPSED TIME: 60.00  MEM: 0.0M) ***
```

LVS:

```
******** Start: VERIFY CONNECTIVITY ********
Start Time: Mon Dec 18 22:28:00 2023

Design Name: QR_Engine
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (1542.3800, 1537.0900)
Error Limit = 1000; Warning Limit = 50
Check all nets
**** 22:28:02 **** Processed 5000 nets.
**** 22:28:02 **** Processed 10000 nets.
**** 22:28:03 **** Processed 15000 nets.
**** 22:28:03 **** Processed 20000 nets.
**** 22:28:04 **** Processed 25000 nets.
**** 22:28:05 **** Processed 30000 nets.
**** 22:28:05 **** Processed 35000 nets.
**** 22:28:06 **** Processed 40000 nets.
**** 22:28:06 **** Processed 45000 nets.
**** 22:28:06 **** Processed 50000 nets.
**** 22:28:07 **** Processed 55000 nets.
**** 22:28:07 **** Processed 60000 nets.
**** 22:28:08 **** Processed 65000 nets.
**** 22:28:08 **** Processed 70000 nets.
**** 22:28:09 **** Processed 75000 nets.
**** 22:28:09 **** Processed 80000 nets.
**** 22:28:10 **** Processed 85000 nets.
**** 22:28:11 **** Processed 90000 nets.
**** 22:28:11 **** Processed 95000 nets.

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Mon Dec 18 22:28:17 2023
Time Elapsed: 0:00:17.0

******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:10.5  MEM: 135.145M)
```

Antenna:

```
******* START VERIFY ANTENNA ********
Report File: QR_Engine.antenna.rpt
LEF Macro File: QR_Engine.antenna.lef
5000 nets processed: 0 violations
10000 nets processed: 0 violations
15000 nets processed: 0 violations
20000 nets processed: 0 violations
25000 nets processed: 0 violations
30000 nets processed: 0 violations
35000 nets processed: 0 violations
40000 nets processed: 0 violations
45000 nets processed: 0 violations
50000 nets processed: 0 violations
55000 nets processed: 0 violations
60000 nets processed: 0 violations
65000 nets processed: 0 violations
70000 nets processed: 0 violations
75000 nets processed: 0 violations
80000 nets processed: 0 violations
85000 nets processed: 0 violations
90000 nets processed: 0 violations
95000 nets processed: 0 violations
Verification Complete: 0 Violations
******* DONE VERIFY ANTENNA ********
(CPU Time: 0:00:10.1  MEM: 0.000M)
```