```
1   module lab11_hdl (
2         input a,
3         input [1:0] b,
4         output [1:0] f,
5         output [1:0] s,
6         output [1:0] r
7   );
8
9   assign f[0] = a & !b[0] & b[1];
10  assign f[1] = a | (!b[0] & b[1]);
11  assign s[0] = (a & !b[0]) | a | (!b[0 & b[1]]);
12  assign s[1] = (!a & !b[0] & !b[1]) | (a & !b[0] & b[1]);
13  assign r[0] = b[0] & !b[1];
14  assign r[1] = (b[0] & !b[1]) | a | (!a & b[0]);
15
16  endmodule
```