MIMXRT1170-EVKB

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Revision History

Rev. Code	Date	By	Description
A	2022-04-11	Shawn Shi	Initial release, the main changes comparing to RT1170EVK are highlighted in Blue color of blockdiagram page.
B	2022-08-12	Shawn Shi	1.Add R/C for SD card power switch control to avoid power rush. 2.Change UART12 pinmux to GPIO_LPSR_00/GPIO_LPSR_01 and add jumper for config. 3.Add 3V3 option to RPI LCD connector PIN14&PIN15, default open. 4.Remove WIFII# LBEE5KL1DX-883 and connectivity will be covered by M.2 modules. 5.Replace R2108/R2110/R2112/R2114/ to jumper config. 6.Add Jumper for PMIC_INTB, ENET_RST_B,WDOG1_RESET_B,WIFI_WAKE_B_3V3,TRG_RST. 7.Change OCT Flash back to MXIC MX25UM51345GXDI00 which was reused and verified. 8.Replace R2080/R1076 to Jumper config for LPUART1 9.Add I2C signals for 8CH DMIC.
C	2022-10-12	Shawn Shi	1.Changed Flash part number from W25Q128JWSIQ to W25Q512NWEIQ. 2.Add Pull up resistors for boot mode and ISP control pins. 3.Add J116 dedicated for ADC_VREF which reserve possibility for custom power option. 4.Remove route of MCULINK TRG_RST to MCU JTAG_nTRST.
C1	2022-10-27	Shawn Shi	DNP U115 FXLS8974CFR3 as it is out of stock and change it's address

Jumper Setting

REF DES	JUMPER(DEFAULT)	PAGE NAME
J38,J41,J67,J71,J73	1-2	03 MAIN POWER
J53,J68,J69	1-2	05 POWER DOMAIN
J14,J19,J23,J28,J49,J56,J116	1-2	06 MIMXRT1170 PART1
J97,J98,J99,J100	1-2	15 SAI
J79,J80	1-2	23 M.2 SOCKET
J102,J103,J114,J115,JP6,JP7	1-2	25 MCU-Link
J90,J91,J93	1-2	27 MISC

Switch Setting

REF DES	SWITCH(DEFAULT)	PAGE NAME
SW1	off,off,on,off	25 BOOT

1. Unless Otherwise Specified:

   All resistors are in ohms, 1/16 Watt,0402
   All capacitors are in uF,0402
   All voltages are DC
   All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

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ICAP Classification: CP: IUO: PUBI:

Designer: Shawn Shi	Drawing Title: MIMXRT1170-EVKB		
Drawn by: Shawn Shi	Page Title: COVER		
Approved: Yes	Size: C	Document Number: SCH-55139, PDF: SPF-55139	Rev: C1
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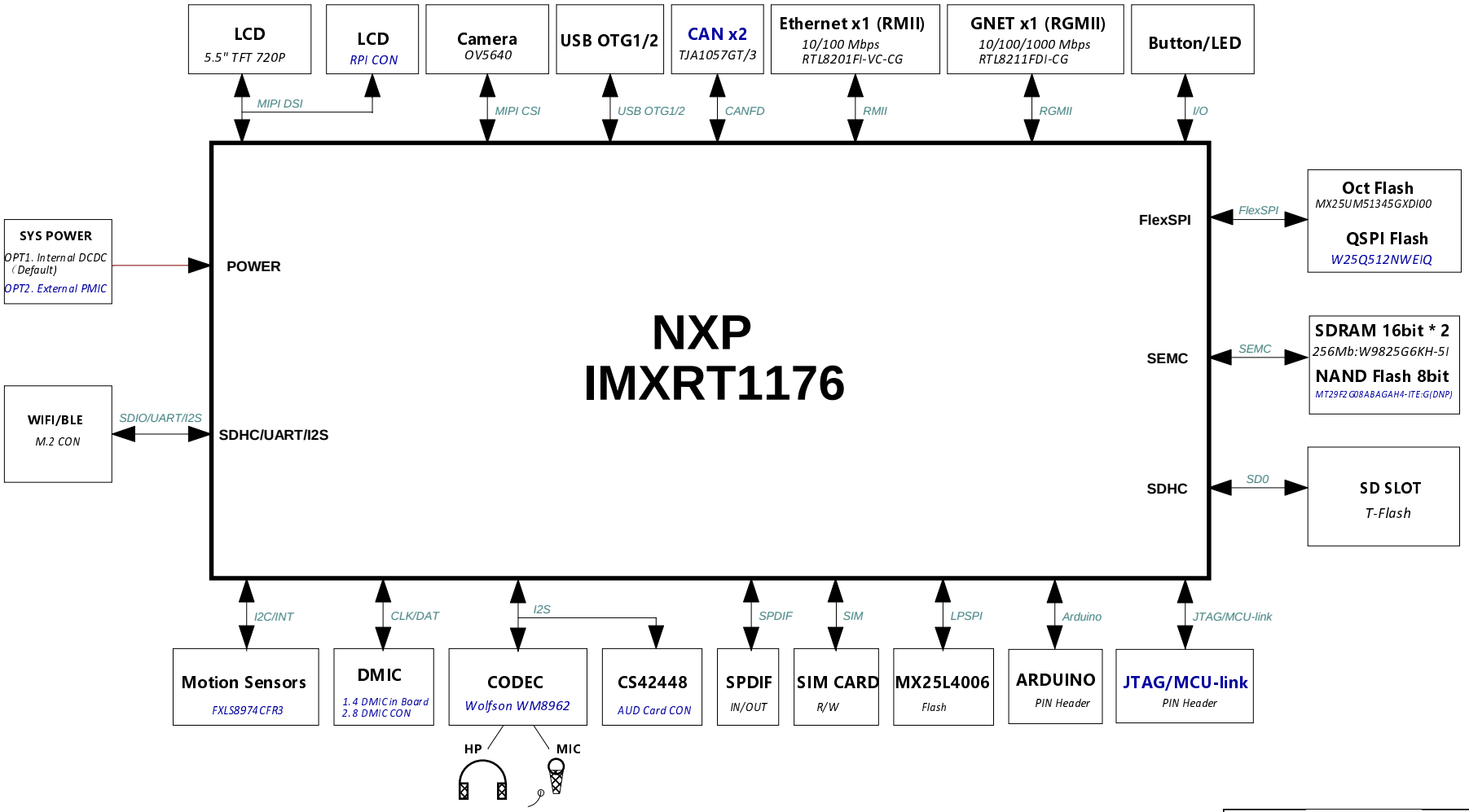
MIMXRT1170-EVKB

Block Diagram Rev C1



ICAP Classification: CP: ___ IUO: PUBL ___

Drawing Title: MIMXRT1170-EVKB

Page Title: BLOCK DIAGRAM

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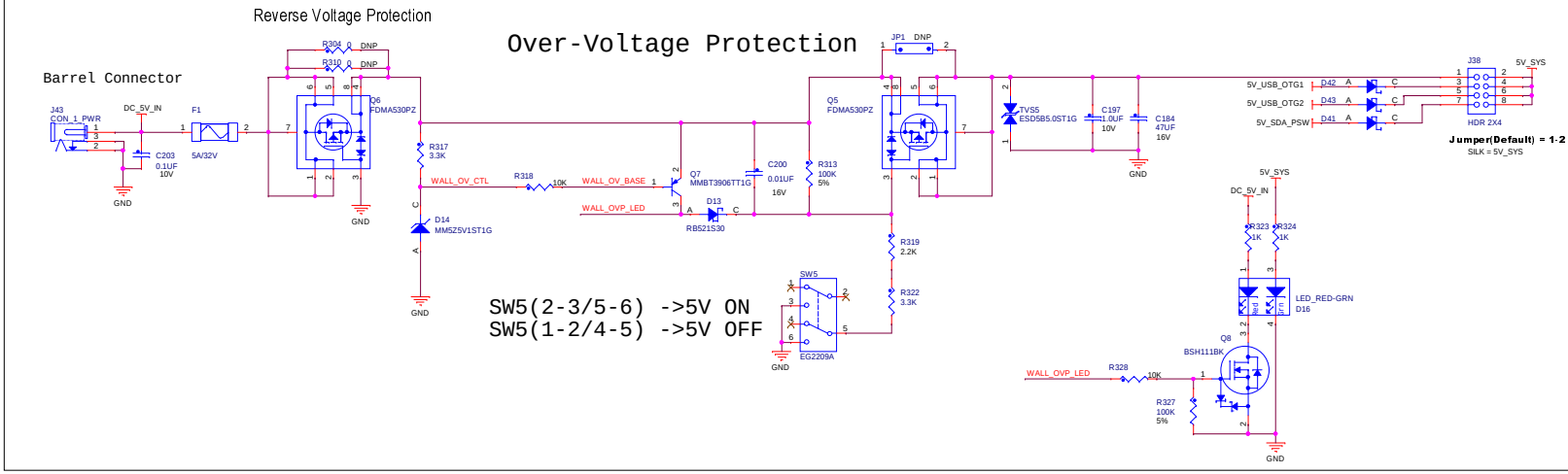
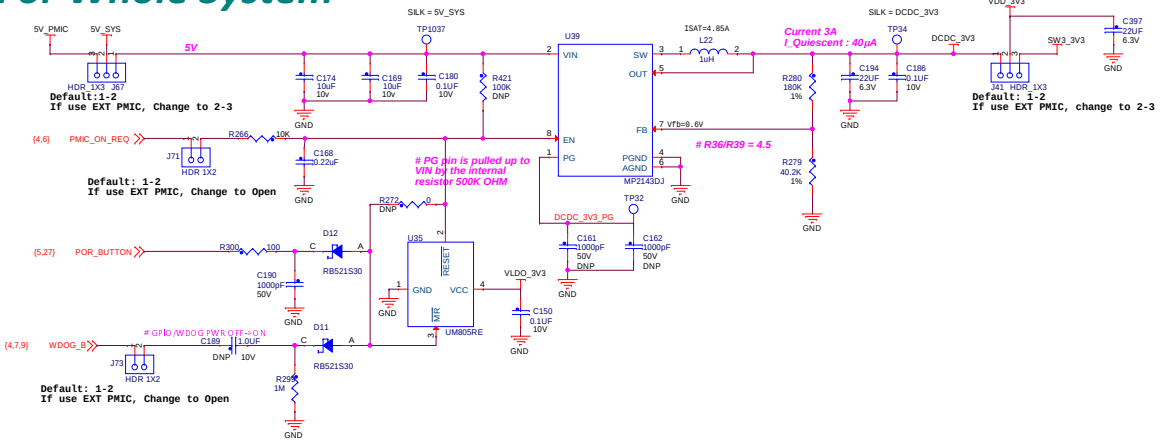
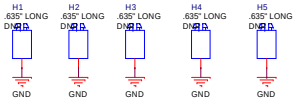
Main Power



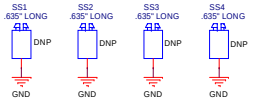
5V To 3.3V For Whole System



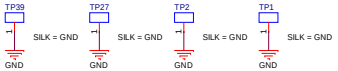
Board Mounting Holes



LCD Mounting Holes



Ground TPs



Layout Note: Place Ground TPs to assist signal measurement.

NXP

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Drawing Title: MIMXRT1170-EVKB

Page Title: MAIN POWER

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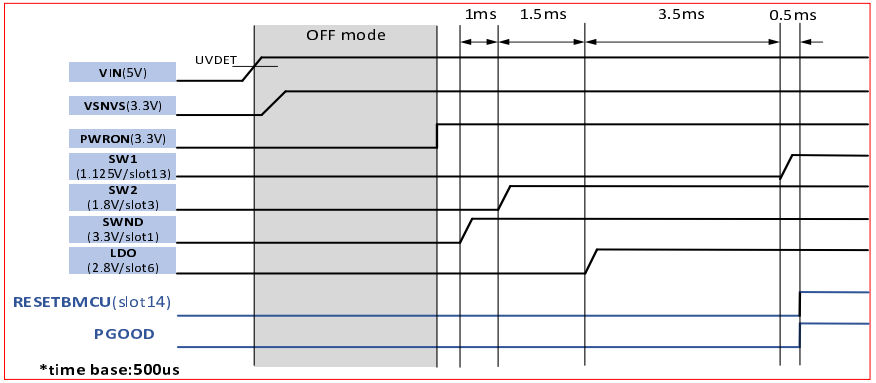
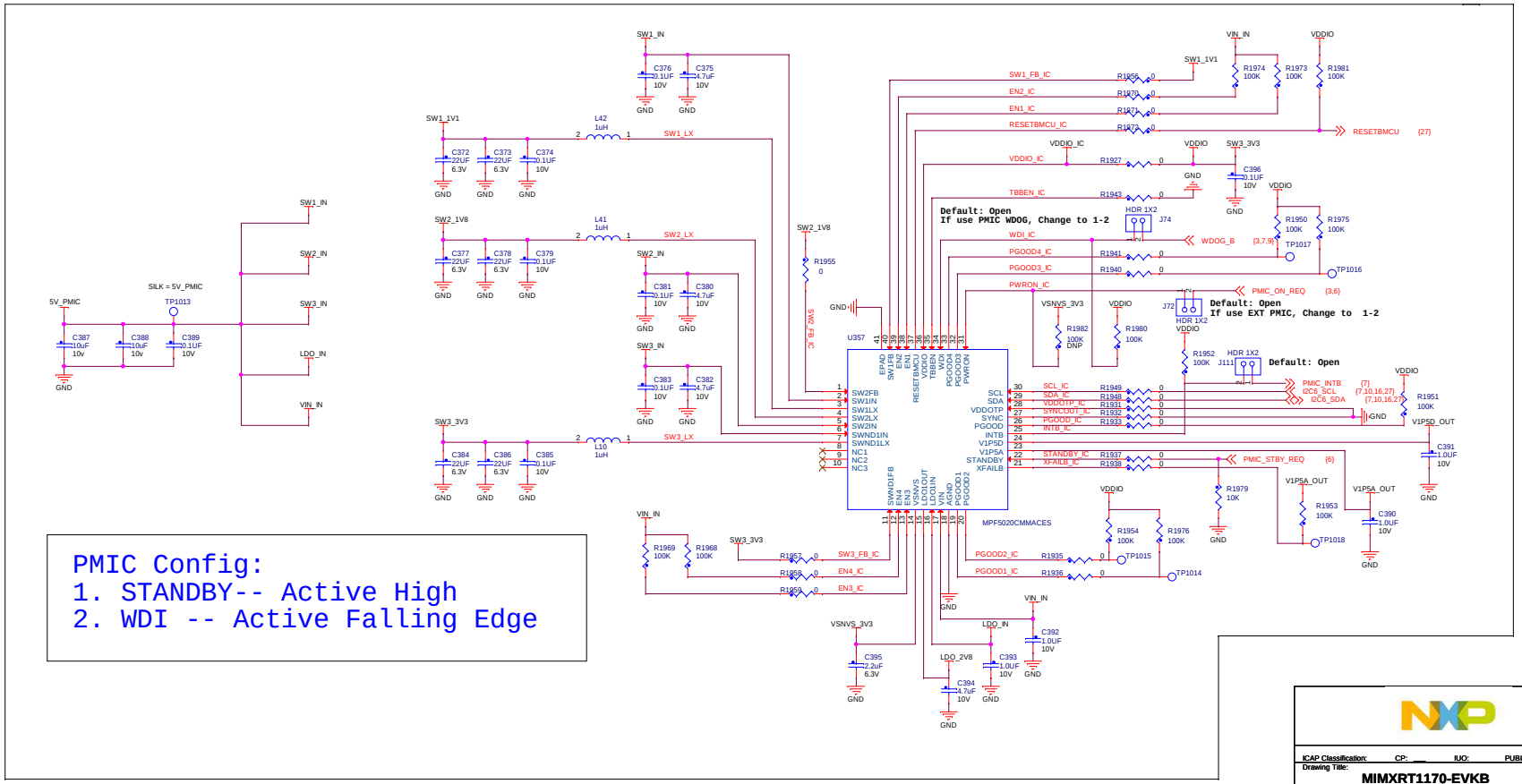
To use EXT PMIC, Please do following Config Changes:

1. Change J41/J53/J67/J68/J69 Jumper Setting from 1-2 to 2-3
2. Change J71/J73/J19 Jumper Setting from 1-2 to OPEN
3. Change J72/J74/J77 Jumper Setting from OPEN to 1-2
4. DNP R1851,R1853 Populate R1852,R1854





PMIC Config:
1. STANDBY-- Active High
2. WDI -- Active Falling Edge

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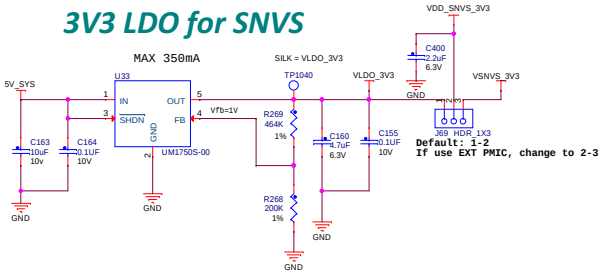
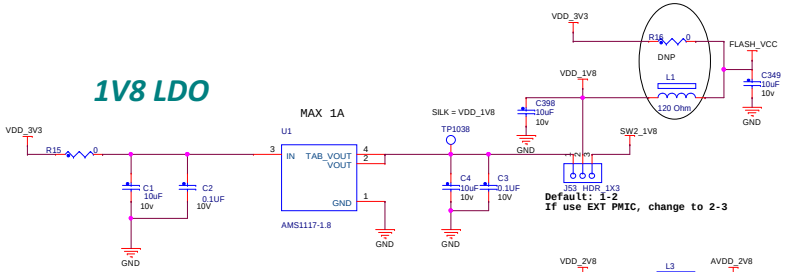
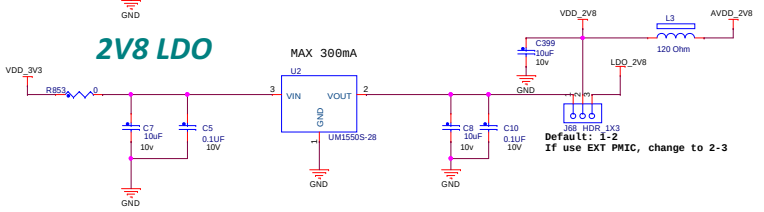
3V3 LDO for SNVS



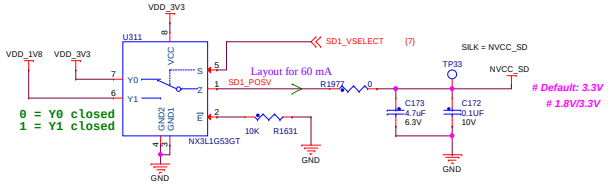
1V8 LDO



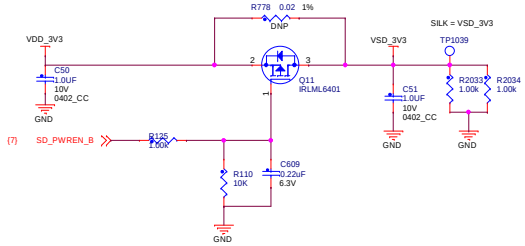
2V8 LDO



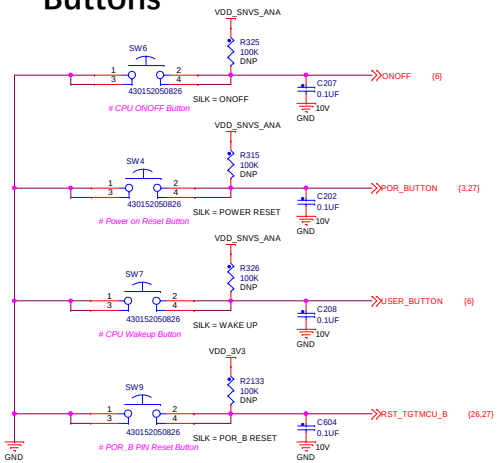
NVCC_SD <SD3.0>



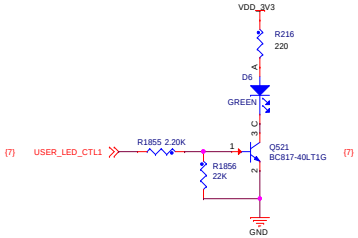
SD Card Power Switch



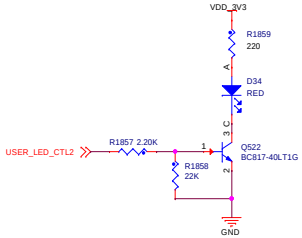
Buttons



USER LED1



USER LED2



Flash VCC Option
1.8V default

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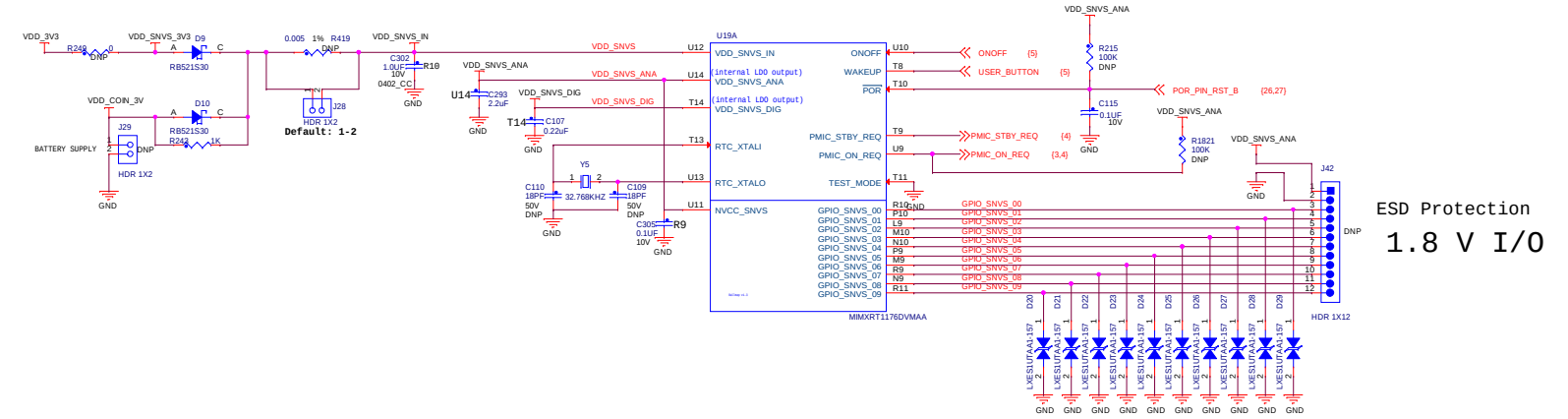
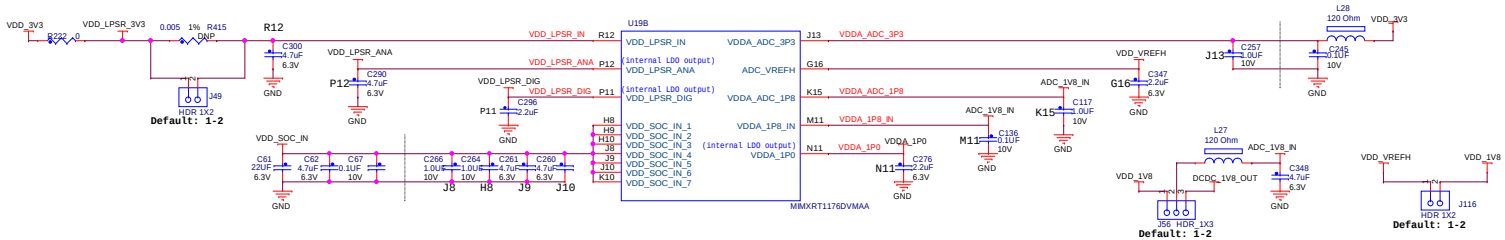
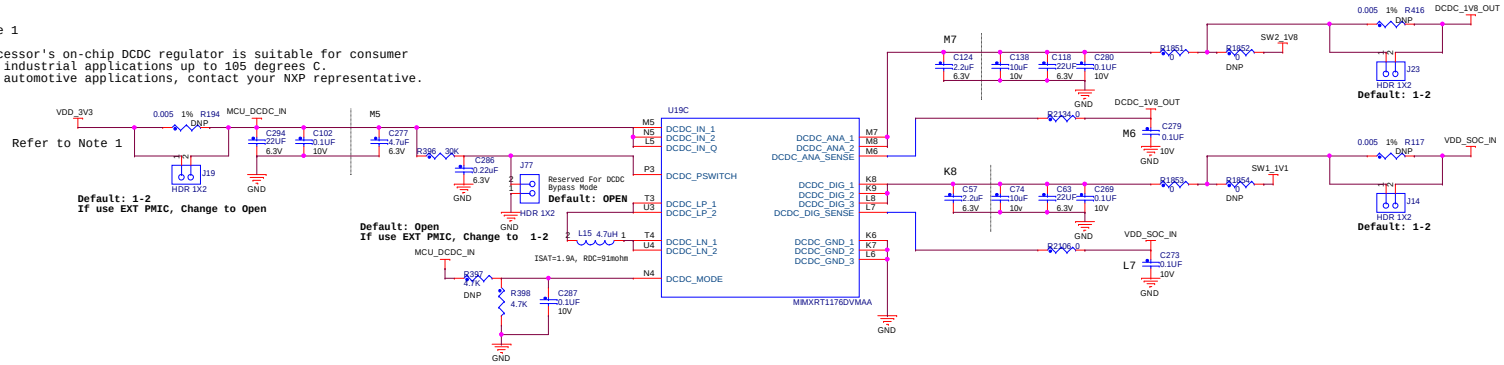
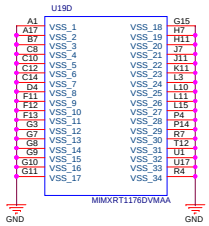


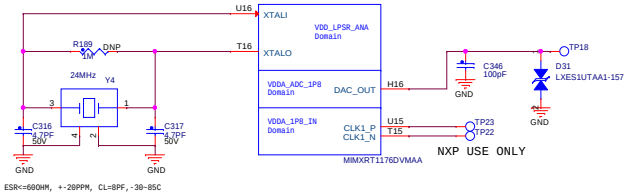


Note 1

Processor's on-chip DCDC regulator is suitable for consumer and industrial applications up to 105 degrees C.
For automotive applications, contact your NXP representative.







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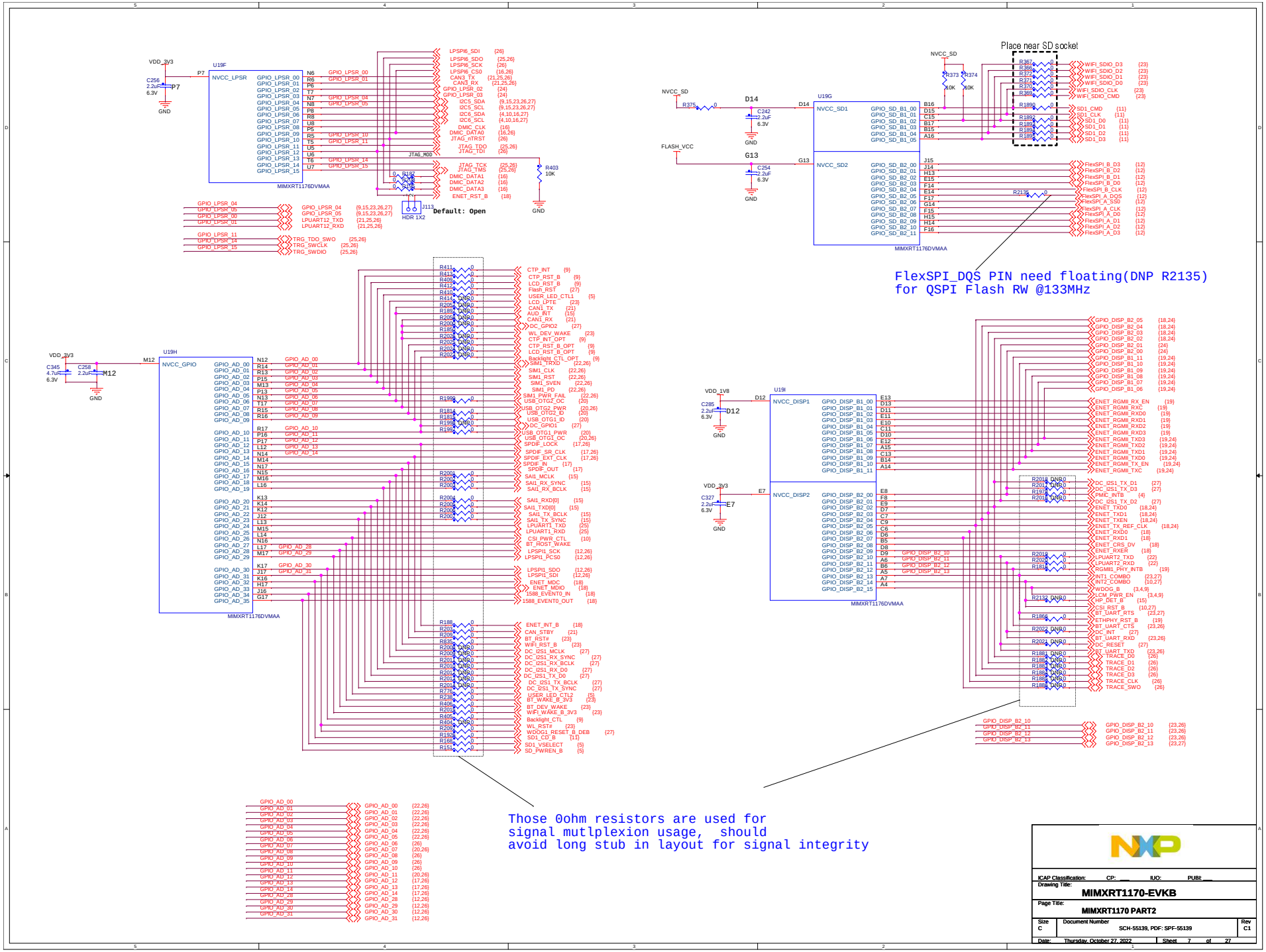
Place near SD socket
FlexSPI_DQS PIN need floating(DNP R2135)
for QSPI Flash RW @133MHz
Those 0ohm resistors are used for
signal mutlplexion usage, should
avoid long stub in layout for signal integrity
Default: Open
MIMXRT1176DVMAA
ICAP Classification:
Drawing Title:
MIMXRT1170-EVKB
Page Title:
MIMXRT1170 PART2
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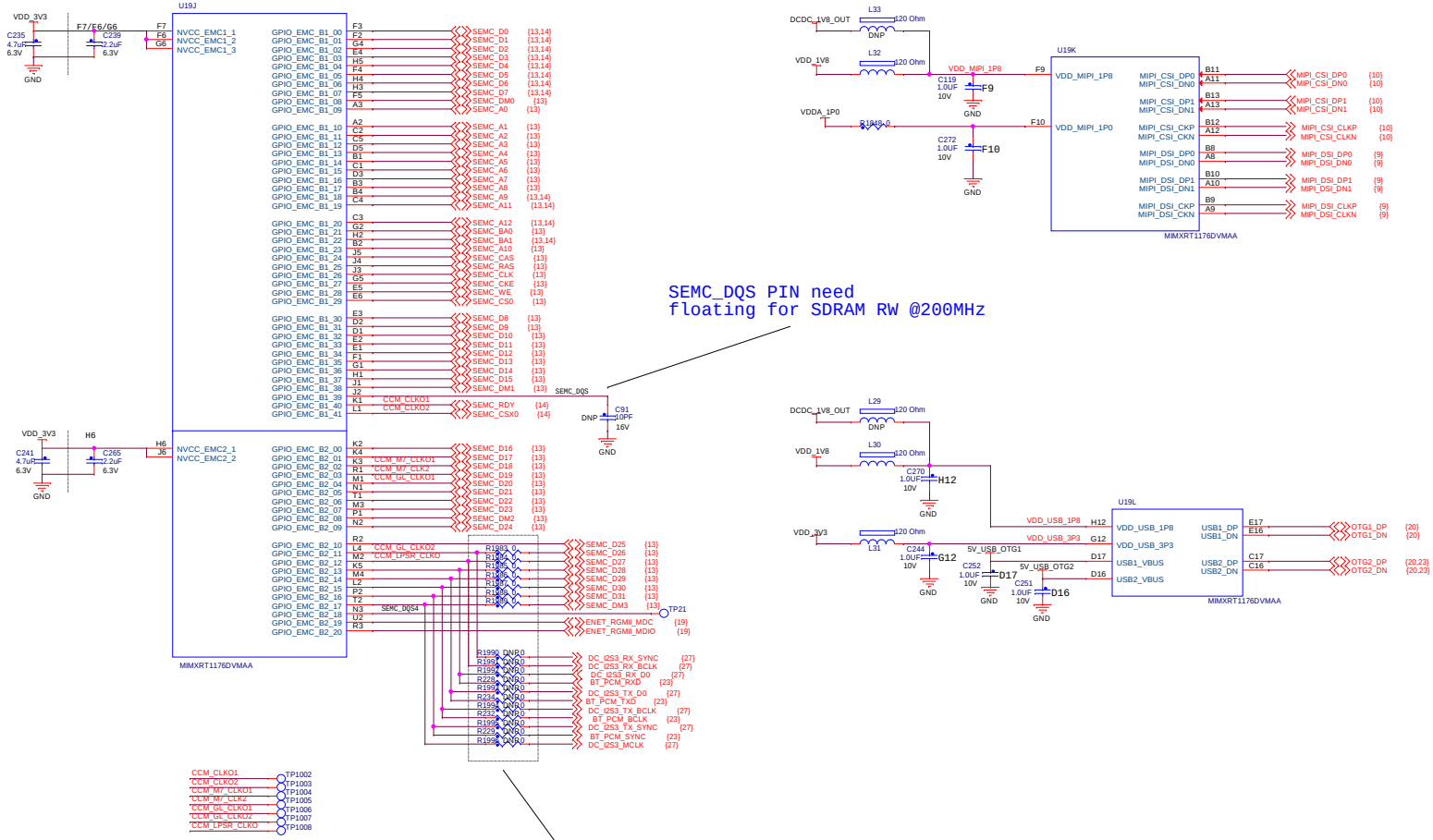

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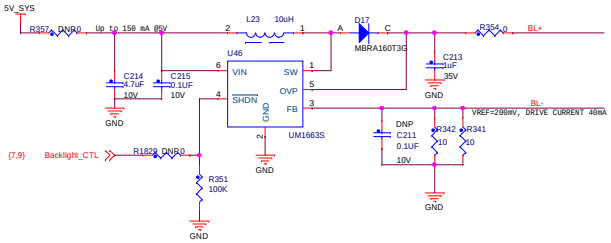
MIPI Display

RPI Display(J84)

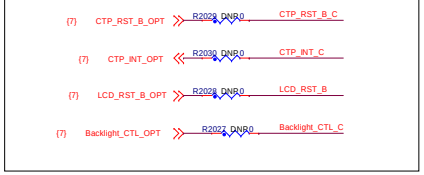
LCD P/N From Rocktech(J48):

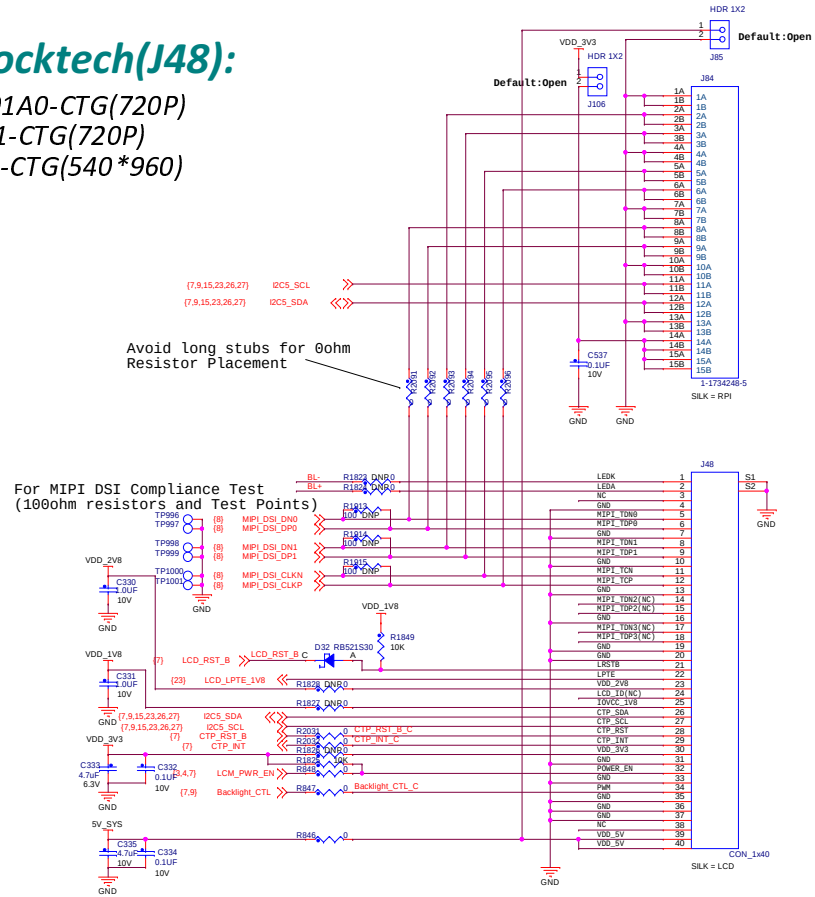
1.RK055MHD091A0-CTG(720P)
2.RK055AHD091-CTG(720P)
3.RK055IQH091-CTG(540*960)

Backlight Control



Resereved for use case which need both LCD and Motor Control





I2C ADD: 0X28/0X29 or 0XBA/0XBB

ICAP Classification:	CP:	IUO:	PUBL
Drawing Title:	MIMXRT1170-EVKB		
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MIPI CSI

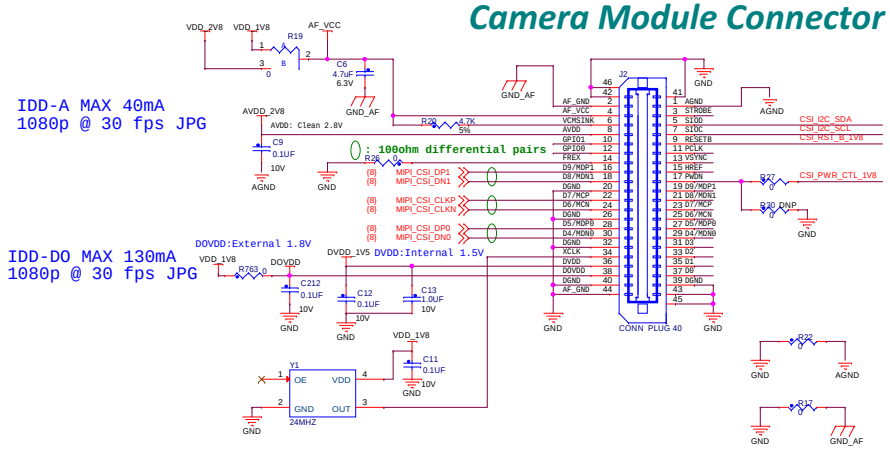
Wuxi A-KERR Science & Technology

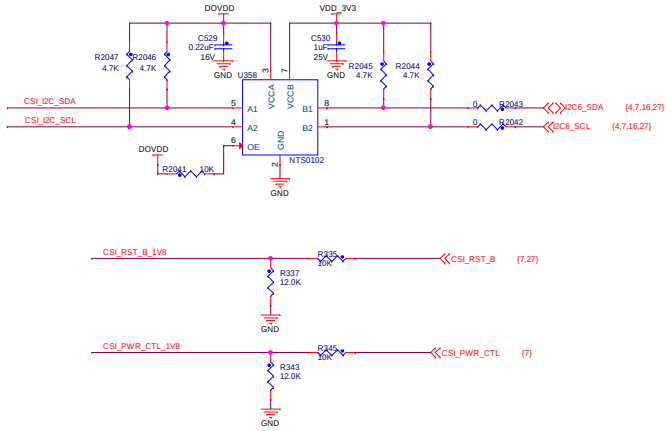
Camera# OV5640

Camera Module Connector

IDD-A MAX 40mA
1080p @ 30 fps JPG

IDD-DO MAX 130mA
1080p @ 30 fps JPG





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Drawing Title:	MIMXRT1170-EVKB
Page Title:	MIPI CAMERA
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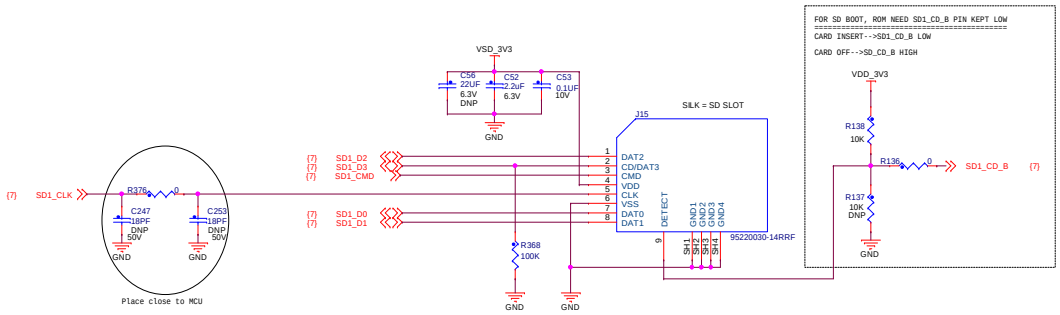
SD Card Socket



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Drawing Title:	MIMXRT1170-EVKB	
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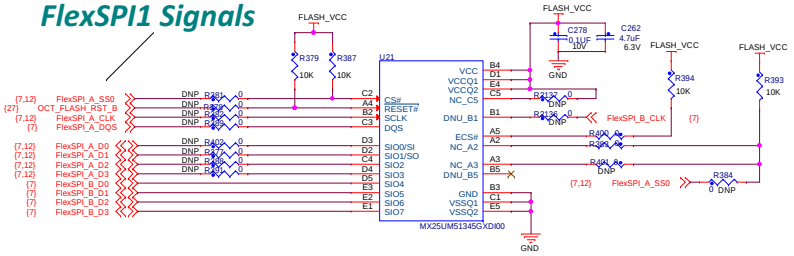
SERIAL FLASH

QSPI Flash as default(Through FlexSPI1)

OPTION1: USE QSPI FLASH(Mount R380/R399/ R386/R390/R392/R385,DNP R381/R378/R382/R389/R402/R377/R388/R391)
OPTION2: USE Octal Flash(Mount R381/R378/R382/R389/R402/R377/R388/R391, DNP R380/R399/R386/R390/R392/R385)

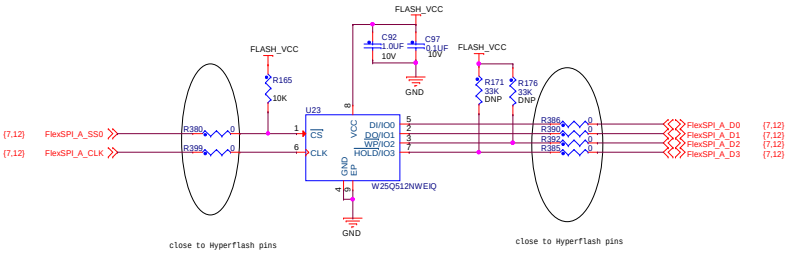
FlexSPI1 Signals

1V8 Octal Flash

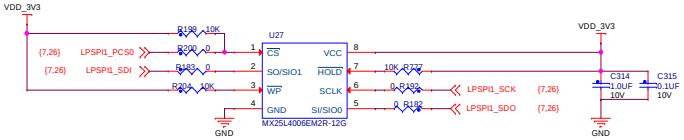


Share the same package with S27KS0641DPBHI023
(if HYPERRAM is used, DNP R383/R400,Mount R401/R384)

1V8 QSPI Flash



LPSPI Flash(Secondary Boot)



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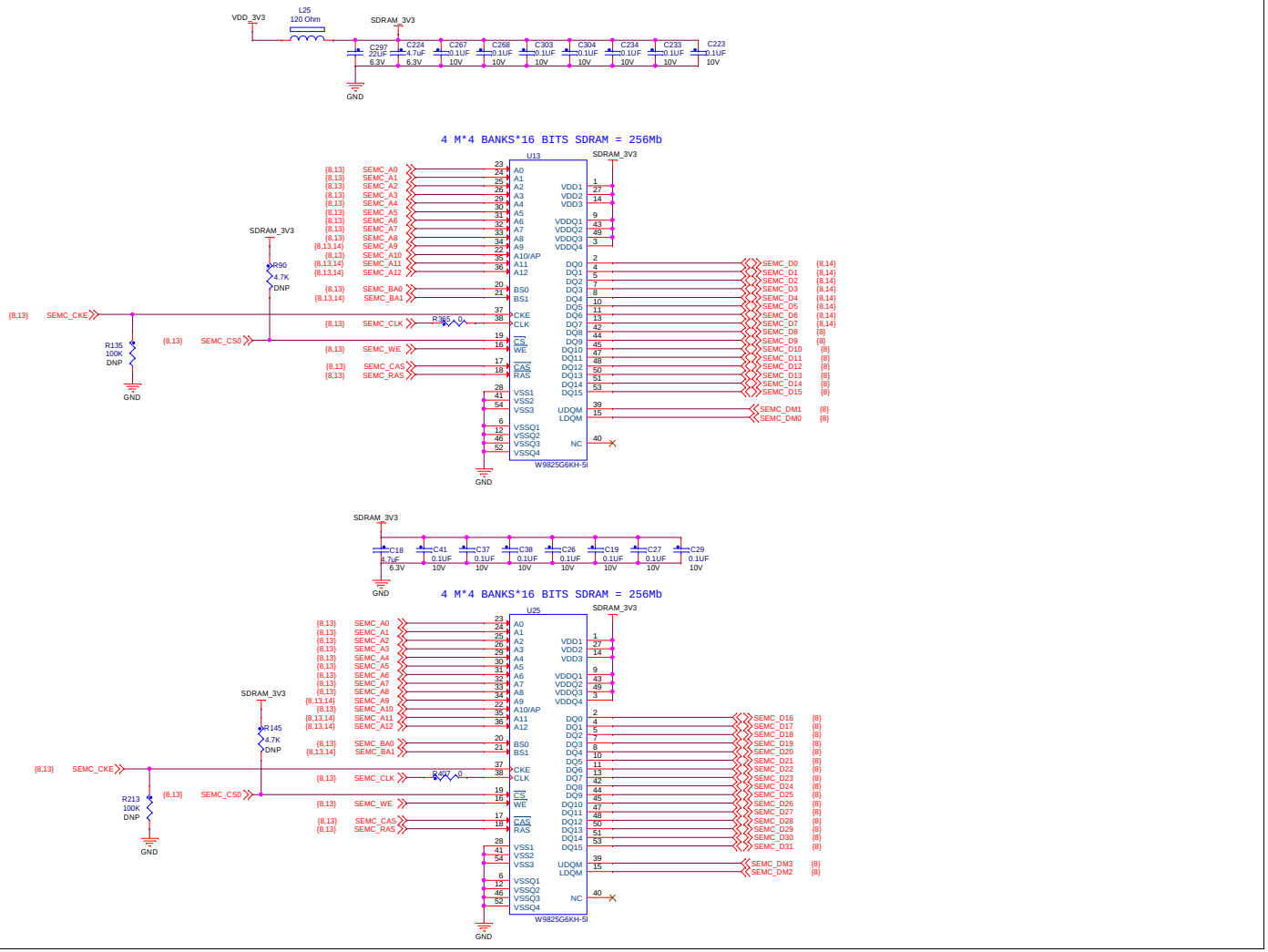
SDRAM



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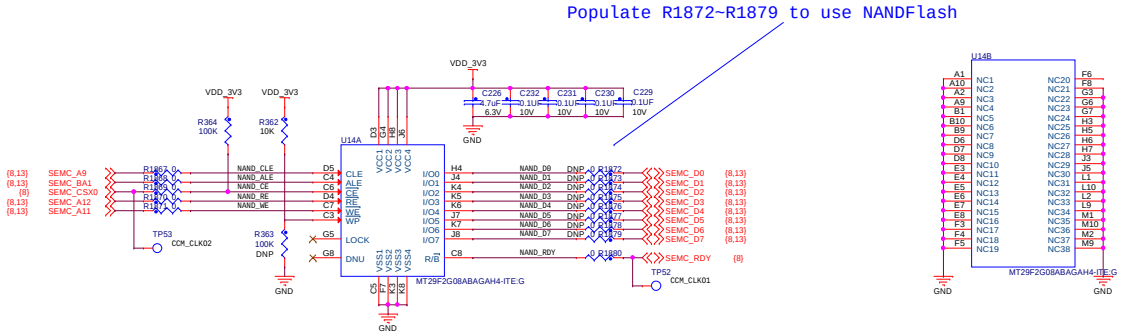
NAND FLASH



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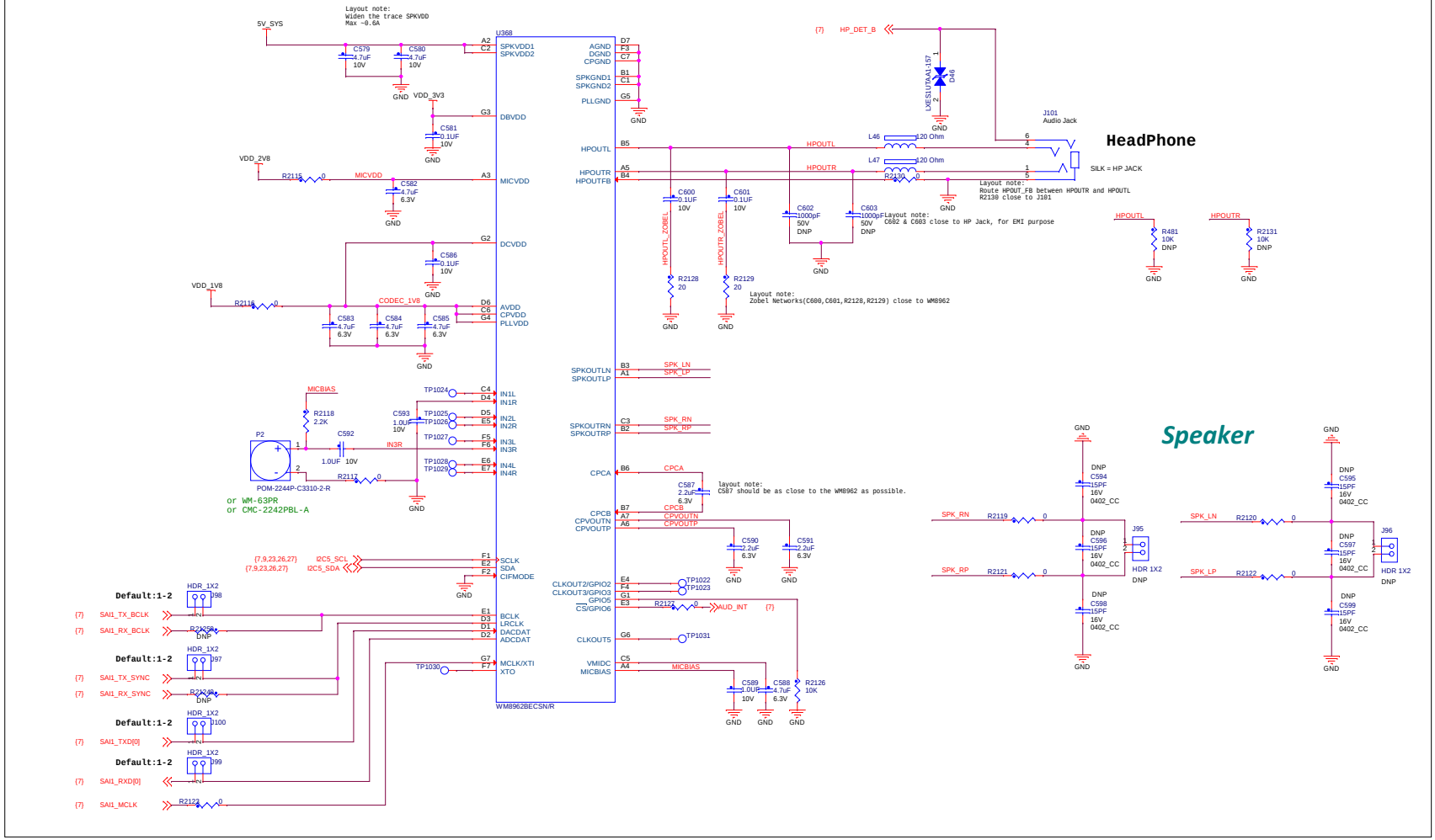
Audio Codec



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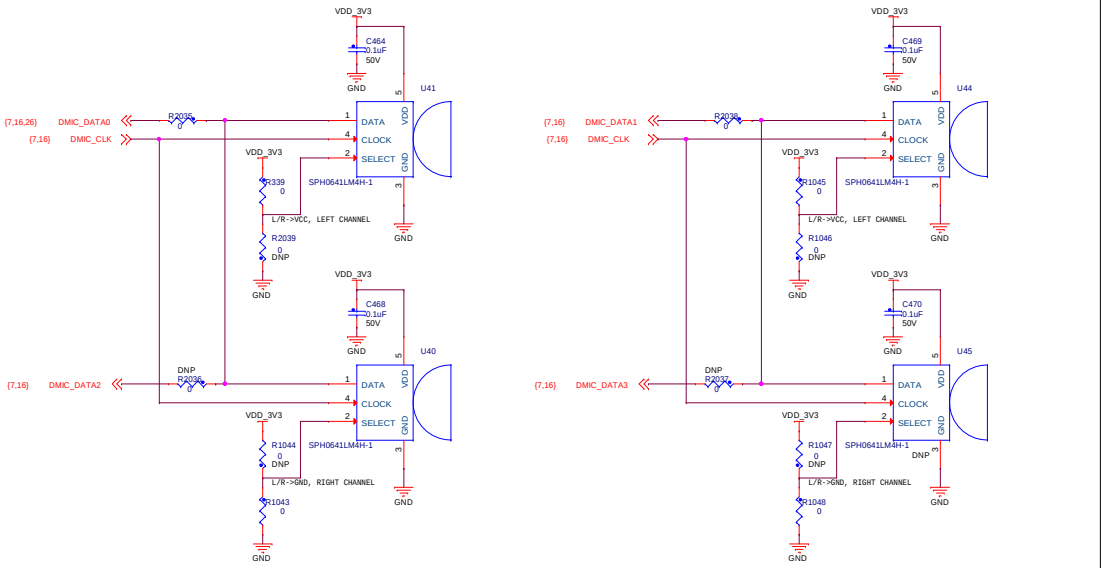
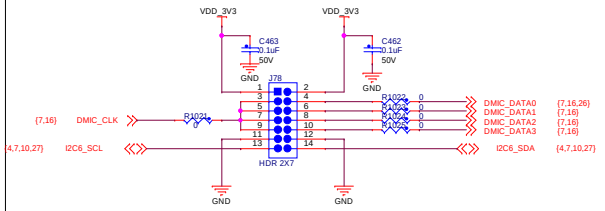
Board DMIC

Notes: Placing the mic under PCB which is opening to face the user



8CH-DMIC Extension



ICAP Classification:	CP: ___ IUO: PUBL ___	
Drawing Title:	MIMXRT1170-EVKB	
Page Title:	DMIC	
Size: C	Document Number: SCH-55139, PDF: SPF-55139	Rev: C1
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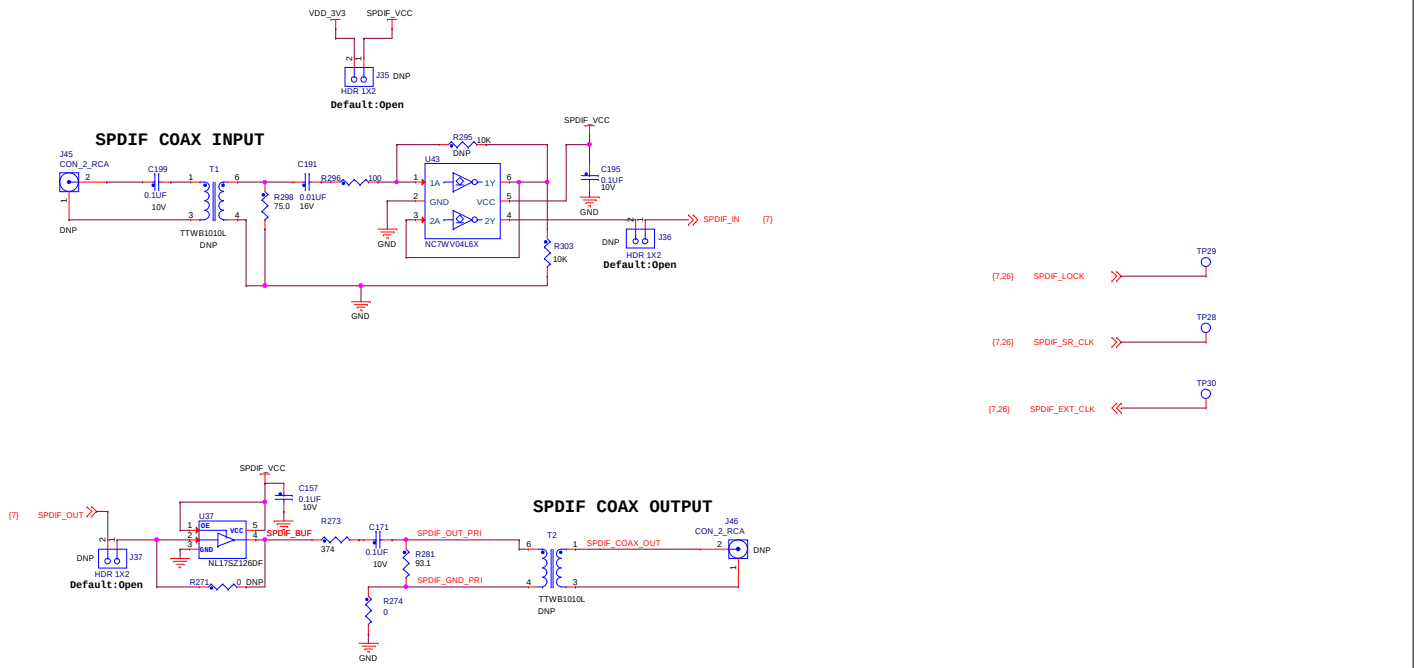
SPDIF Interface



ICAP Classification:	CP: ___	IUO:	PUBL ___
Drawing Title:	MIMXRT1170-EVKB		
Page Title:	SPDIF		
Size: C	Document Number: SCH-55139, PDF: SPF-55139		Rev: C1
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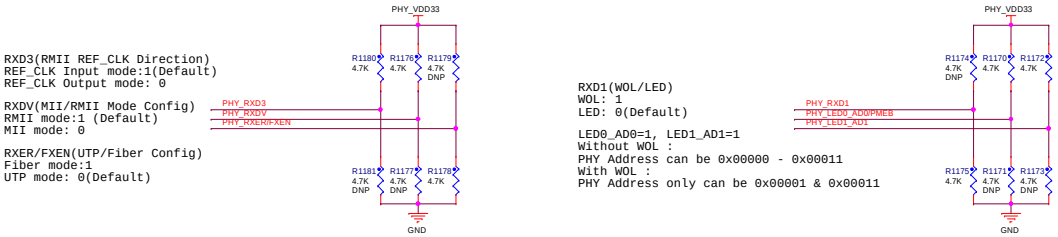
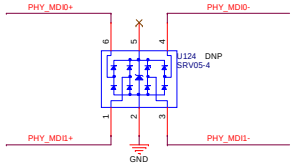
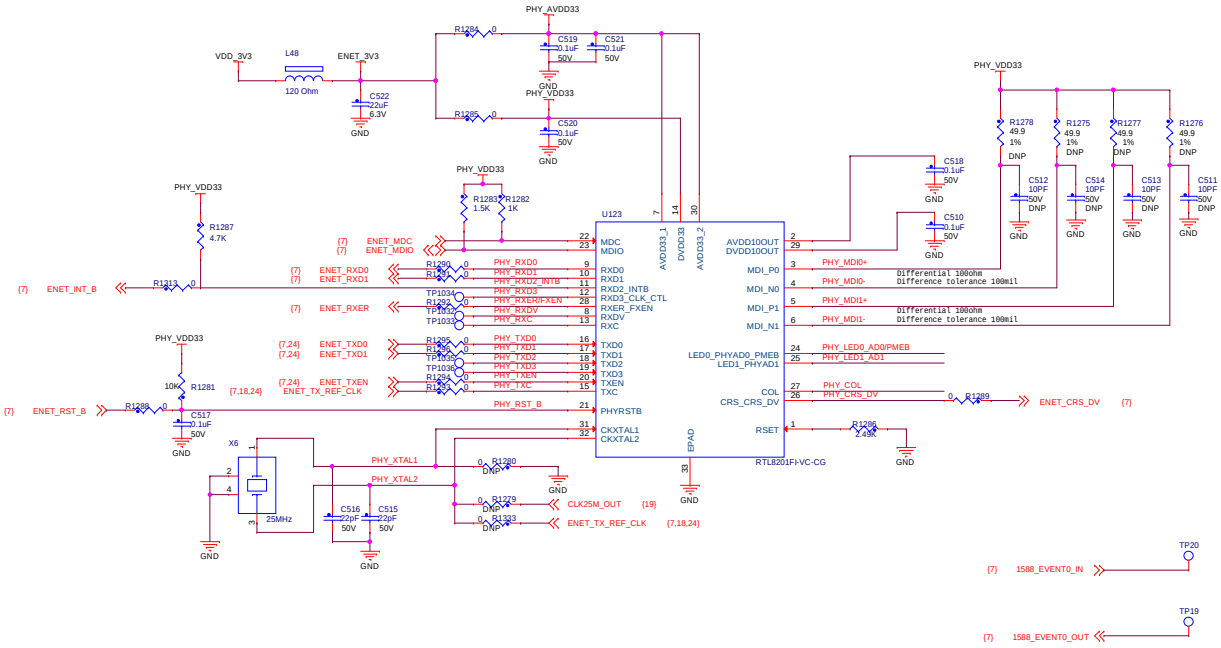
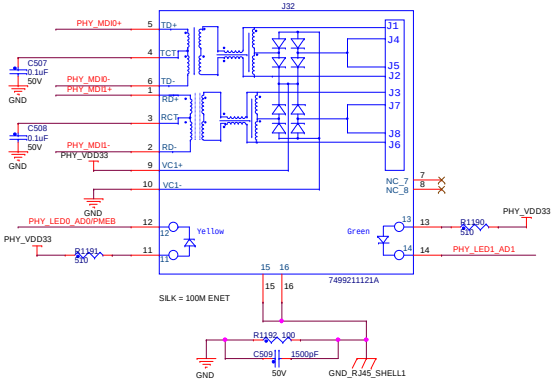
10/100Mbps Ethernet Circuit



ESD PROTECTION







ICAP Classification:	CP: ___	IUO:	PUBL ___
Drawing Title:	MIMXRT1170-EVKB		
Page Title:	10M/100M ETHERNET		
Size: C	Document Number: SCH-55139, PDF: SPF-55139		Rev: C1
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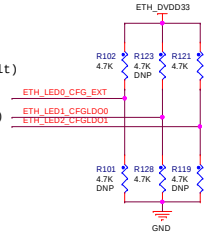
SOC RGMII 1.8V SIGNALS

{7,24} ENET_RGMII_TXC → ENET_RGMII_TXC
{7,24} ENET_RGMII_TX_EN → ENET_RGMII_TX_EN
{7,24} ENET_RGMII_TXD0 → ENET_RGMII_TXD0
{7,24} ENET_RGMII_TXD1 → ENET_RGMII_TXD1
{7,24} ENET_RGMII_TXD2 → ENET_RGMII_TXD2
{7,24} ENET_RGMII_TXD3 → ENET_RGMII_TXD3

{7} ENET_RGMII_RXC → ENET_RGMII_RXC
{7} ENET_RGMII_RX_EN → ENET_RGMII_RX_EN
{7} ENET_RGMII_RXD0 → ENET_RGMII_RXD0
{7} ENET_RGMII_RXD1 → ENET_RGMII_RXD1
{7} ENET_RGMII_RXD2 → ENET_RGMII_RXD2
{7} ENET_RGMII_RXD3 → ENET_RGMII_RXD3

CFG_EXT
EXTERNAL: 1(Default)
INTERNAL: 0

CFG_LDO[1:0]
1.8V: 10 (Default)
2.5V: 01
3.3V: 00

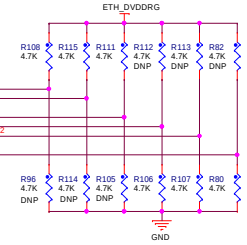


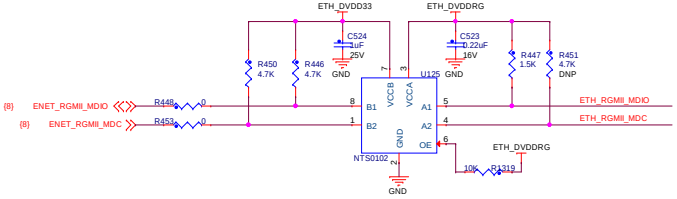
Pull-up for additional 2ns delay to TXC/RXC for data latching.

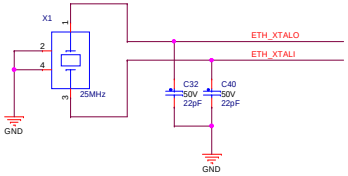
TXC Delay Config → ETH_RXD1_TXDLY
RXC Delay Config → ETH_RXD0_RXDLY

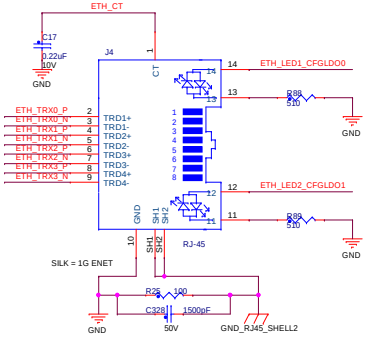
PHY_ADDR0 → ETH_RXD3_PHYAD0
PHY_ADDR1 → ETH_RXC_PHYAD1
PHY_ADDR2 → ETH_RXCTL_PHYAD2
PHY_ADDR: 00001

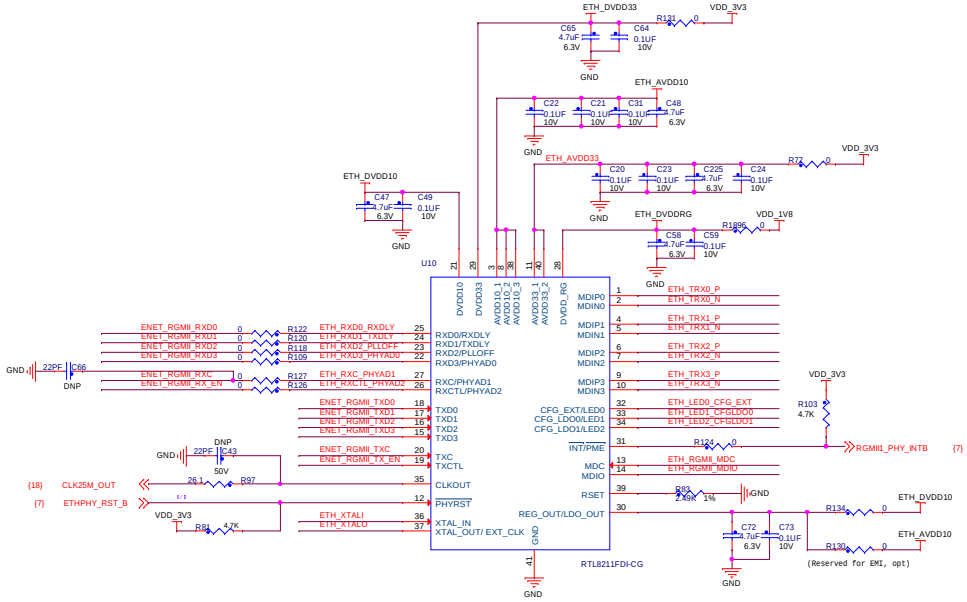
Pull-up to disable PLL @ ALDPS mode. → ETH_RXD2_PLLOFF

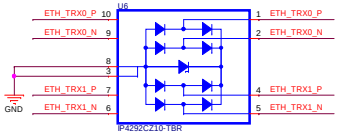


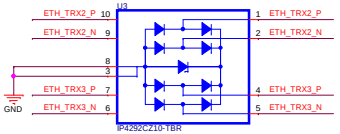












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Page Title: **GIGABIT ETHERNET**

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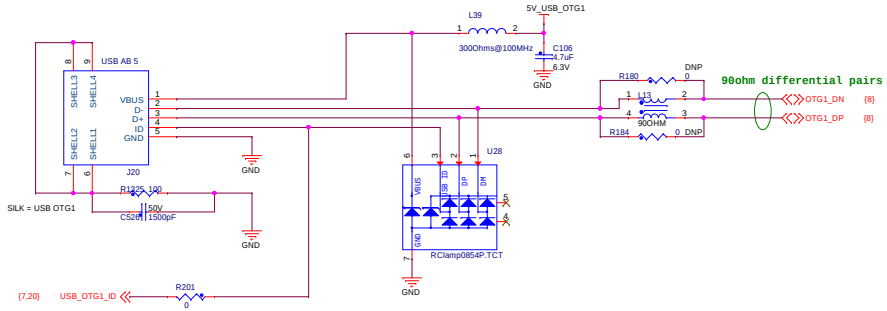
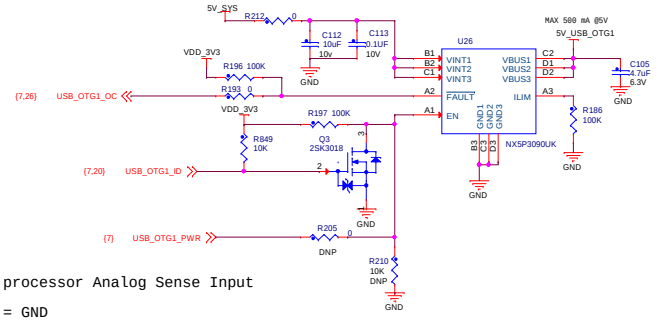
USB OTG1



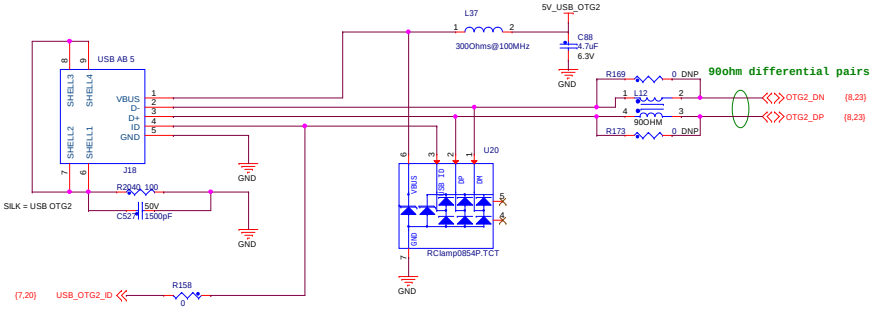
USB Power



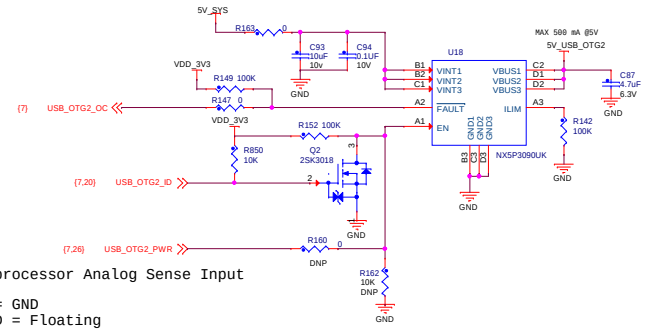
USB ID is a processor Analog Sense Input

Host --> ID = GND
Device --> ID = Floating

USB OTG2



USB Power



USB ID is a processor Analog Sense Input

Host --> ID = GND
Device --> ID = Floating

ICAP Classification:	CP: ___ IUO: PUBL ___	
Drawing Title:	MIMXRT1170-EVKB	
Page Title:	USB	
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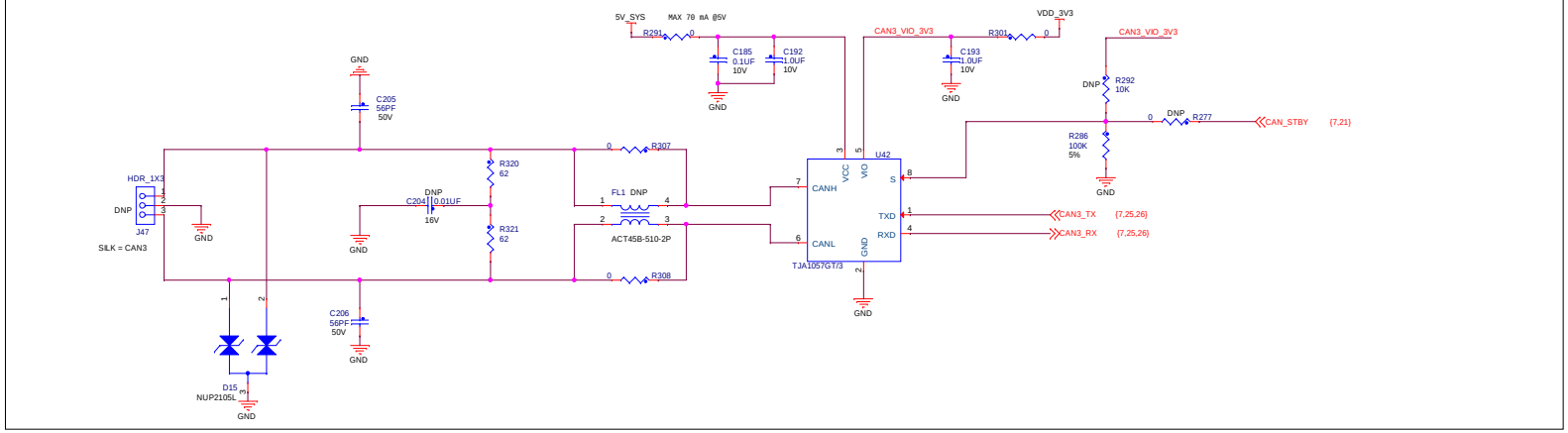
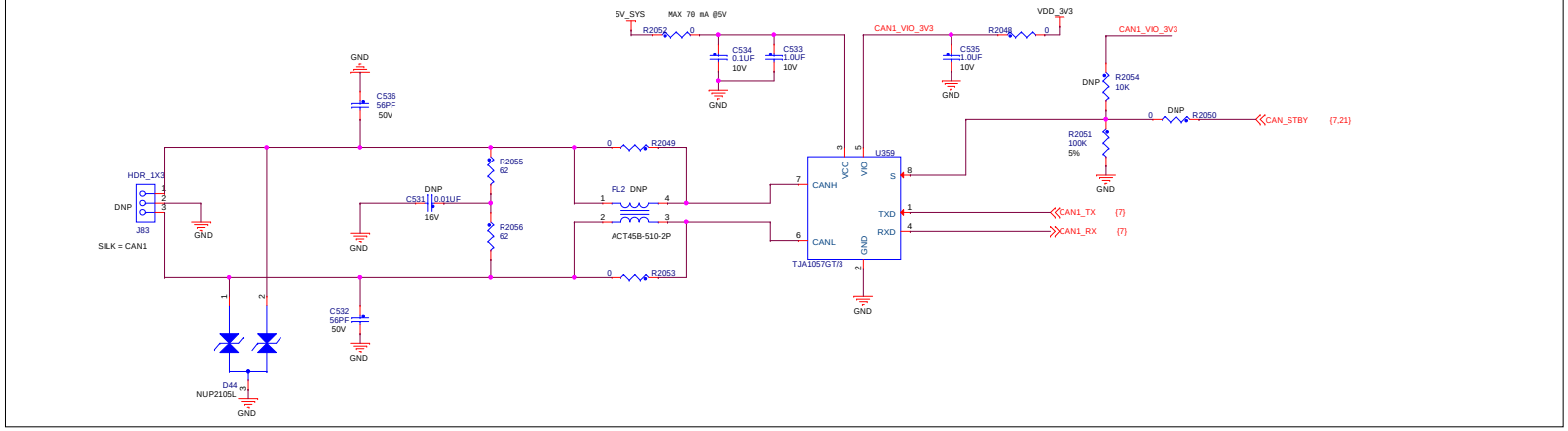
CAN3 Bus



CAN1 Bus



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Drawing Title: **MIMXRT1170-EVKB**

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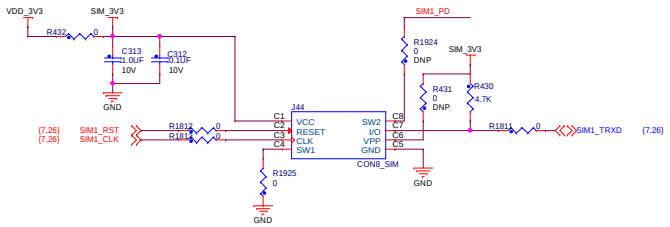
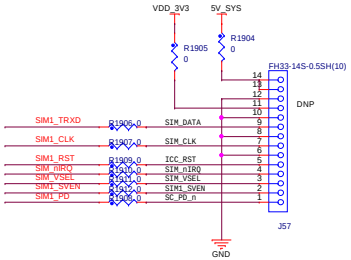
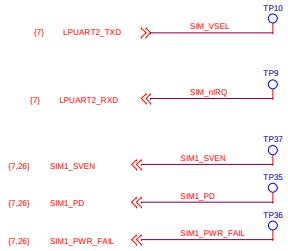
SIM CARD

If using detection function:
Populate R1924, DNP R410



Connector reserved for EMV L1 test





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Drawing Title: MIMXRT1170-EVKB

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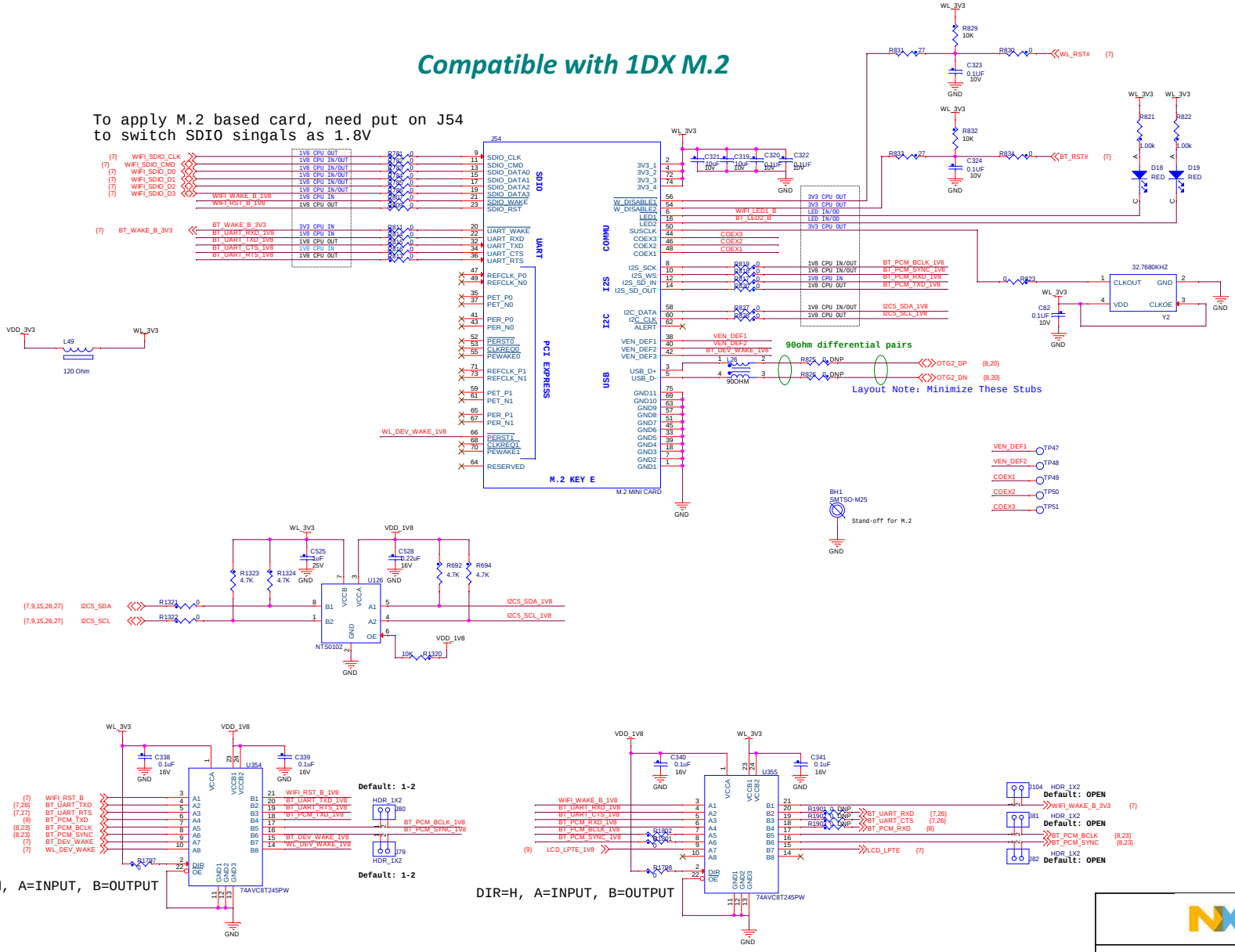
Compatible with 1DX M.2

To apply M.2 based card, need put on J54
to switch SDIO singals as 1.8V



ICAP Classification:	CP: ___ IUO: PUBL ___
Drawing Title:	MIMXRT1170-EVKB
Page Title:	M.2 SOCKET
Size: C	Document Number: SCH-55139, PDF: SPF-55139
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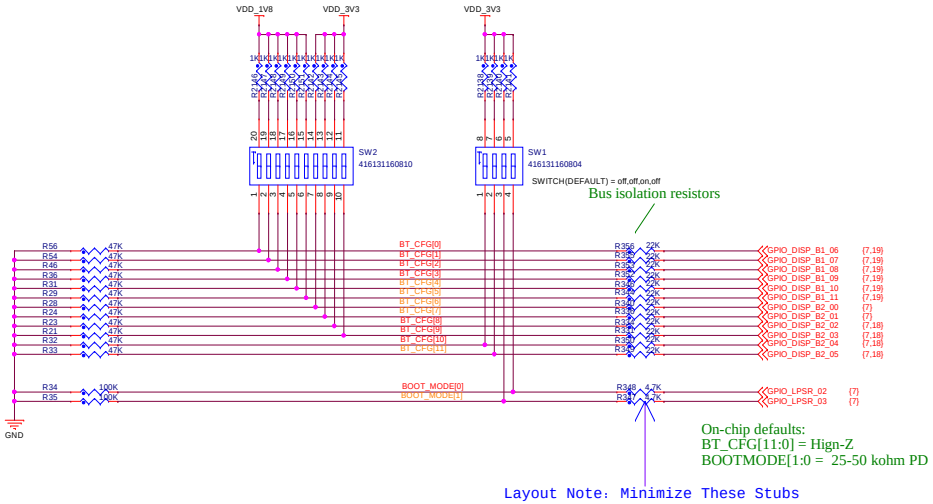
Boot Configuration

TYPE	BOOT_CFG[11]	BOOT_CFG[10]	BOOT_CFG[9]	BOOT_CFG[8]	BOOT_CFG[7]	BOOT_CFG[6]	BOOT_CFG[5]	BOOT_CFG[4]	BOOT_CFG[3]	BOOT_CFG[2]	BOOT_CFG[1]	BOOT_CFG[0]
	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
FlexSPI1 - Serial NOR	FLEXSPI_INSTANCE 0 - FLEXSPI1 1 - FLEXSPI2	xSPI_FLASH_TYPE 0 - Boot with default 0x03 Read Enabled / 1 - Reserved 2 - HyperFLASH 1V8 / 3 - HyperFLASH 3V0 4 - MXIC Octal Read / 5 - Micron Octal Read			0	0	0	0	FLASH_PROBE_TYPE 0 - QuadSPI NOR 1 - MXIC Octal 2 - Micron Octal 3 - Adesto Octal		ENCRYPT_XIP_EN	FLALSH_AUTO_PROBE_EN
SD Card	Reserved	Reserved	Bus Width: 0 - 1-bit 1 - 4-bit	Reserved	0	1	SD/SDXC Speed: 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104		SD Power Cycle Enable: '0' - No power cycle '1' - Enabled via USDHC_RST pad	SD Loopback Clock Source Sel: (for SDR50 and SDR104 only) '0' - through SD '1' - direct	Port Select: 0 - eSDHC1 1 - eSDHC2	Reserved
SEMC (NAND)	Reserved	SEMC Access Command: 0 - IPG 1 - AXI	SEMC EDO Mode: 0 - EDO Mode 1 - Non-EDO mode	ONFI compliant: 0 – Yes, ONFI 1 – No, spec	0	0	1	BOOT_SEARCH_STRIDE: Search Stride for FCB and DBBT Search strides in terms of page 0000 - 64 other: Value = 2^(BOOT_SEARCH_STRIDE)				BOOT_SEARCH_COUNT: 0 - 1 1 - 2

External Boot Switch



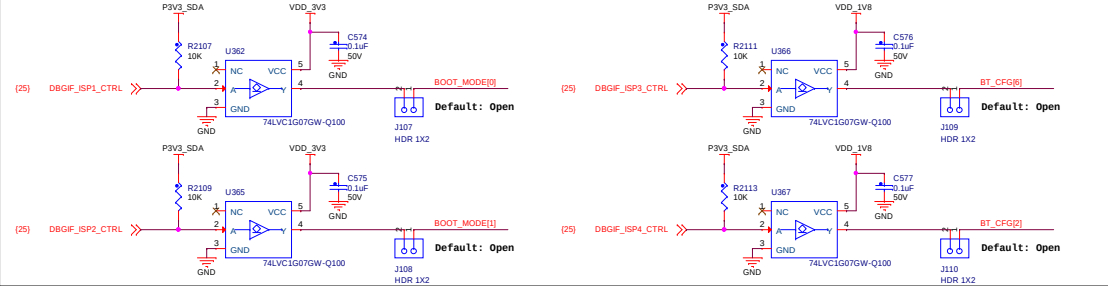
Boot MODE pin settings

BOOT_MODE[1:0]	Boot Type
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot
11	Reserved

Boot Switch settings

DEVICE	SW1	SW2
SDP MODE	0,0,0,1	0,0,0,0,0,0,0,0,0,0
OSPI FLASH	0,0,1,0	0,0,0,0,0,0,0,0,0,0
OCTAL FLASH	0,0,1,0	0,0,1,0,0,0,0,0,0,0
NAND FLASH	0,0,1,0	0,0,0,0,0,1,0,0,0,0
SD CARD	0,0,1,0	0,0,0,0,0,0,1,0,0,0

ISP Control for Factory Automation



ICAP Classification: CP: IUO: PUBL

Drawing Title: MIMXRT1170-EVKB

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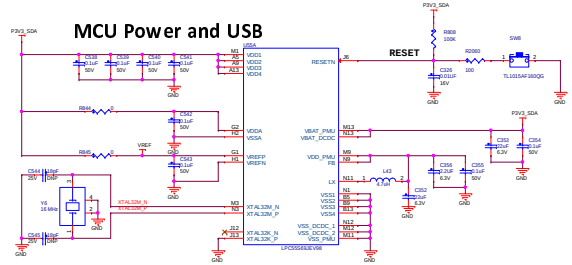
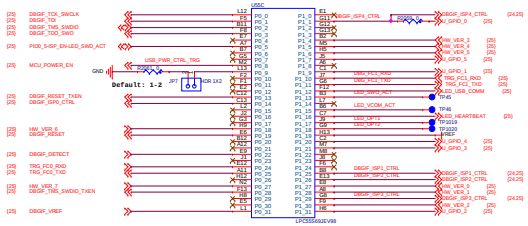
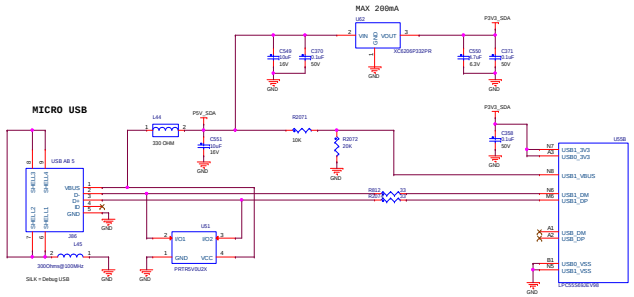
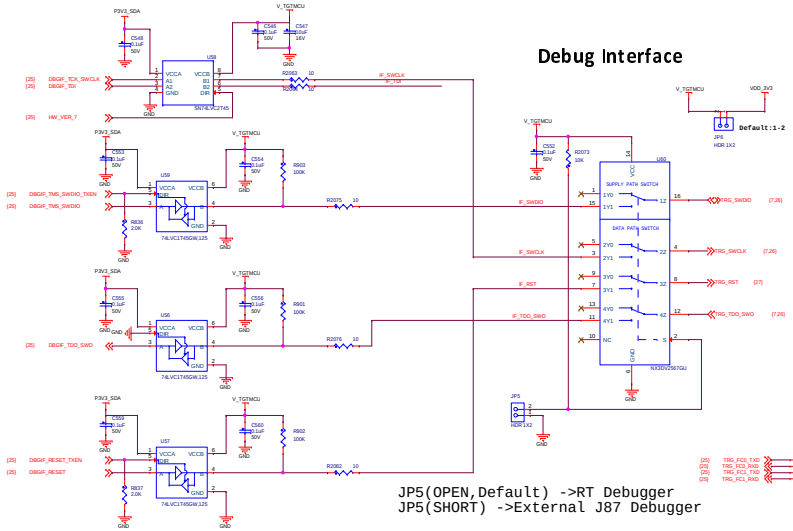
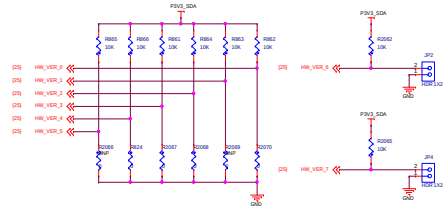


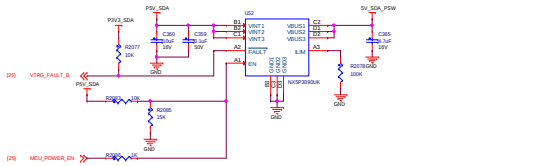


Items	Description	OB setting
HW_VER_0(PIO1_27)	Power negotiation when low	0
HW_VER_1(PIO1_28)	Reserved	1
HW_VER_2(PIO1_30)	USBSIO bridge disabled / not present when 0	0
HW_VER_3(PIO1_4)	OB (0) / Pro (1) type select	0
HW_VER_4(PIO1_5)	Board identity code used (when low)	0
HW_VER_5(PIO1_6)	Power measurement enabled/present when low	1
HW_VER_6(PIO0_18)	VCOM disabled when low	1
HW_VER_7(PIO0_27)	SWD debug disabled when low	1



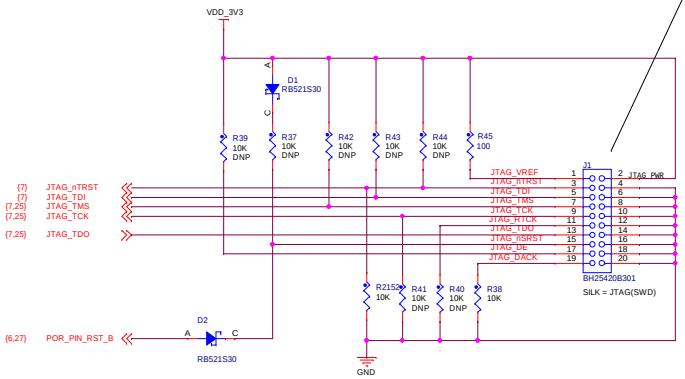




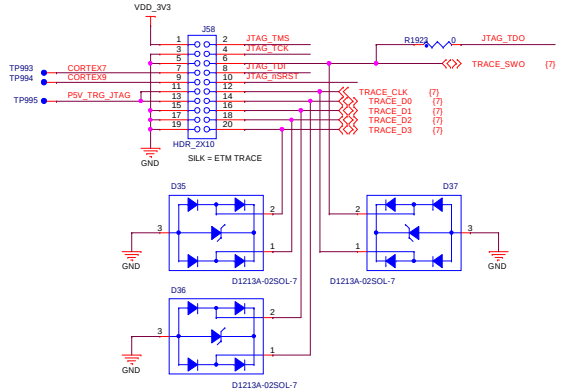


JTAG(SWD)

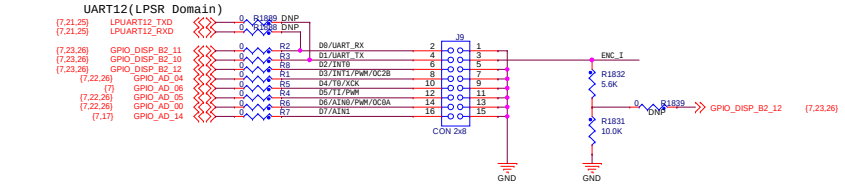
1.SWD debug is enabled by default
2.Board rework are needed to support JTAG debug

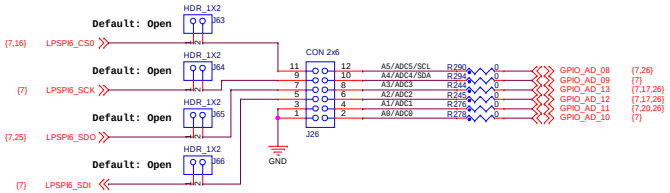


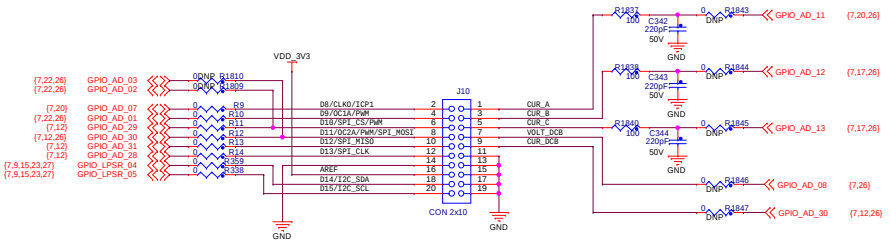
Cortex Debug + ETM

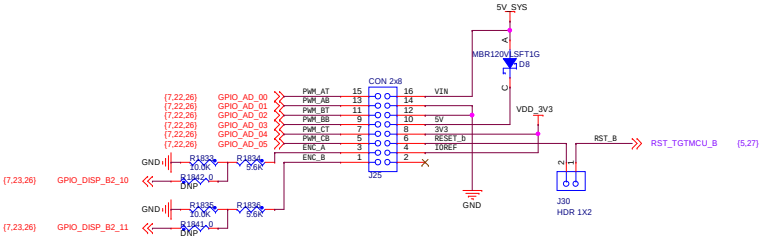


Arduino&Moto Control Interface









NXP

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Drawing Title: **MIMXRT1170-EVKB**

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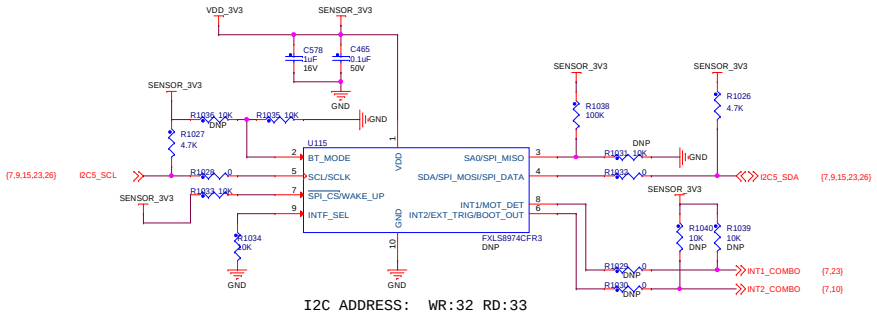
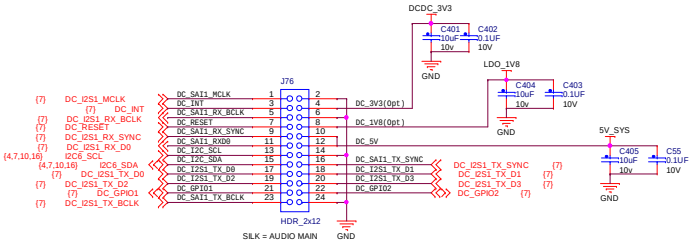
Accelerometer



I2C ADDRESS: WR:32 RD:33

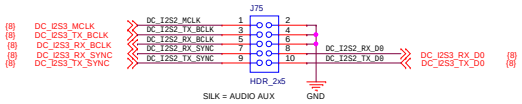
AUDIO MAIN CONN

If Audio main conn (J76) is used, please mount resistors below, R2008,R2022,R2011,R2021,R2009,R2010,R2012,R2016,R1998,R2013,R2014, R2018,R2017,R2000

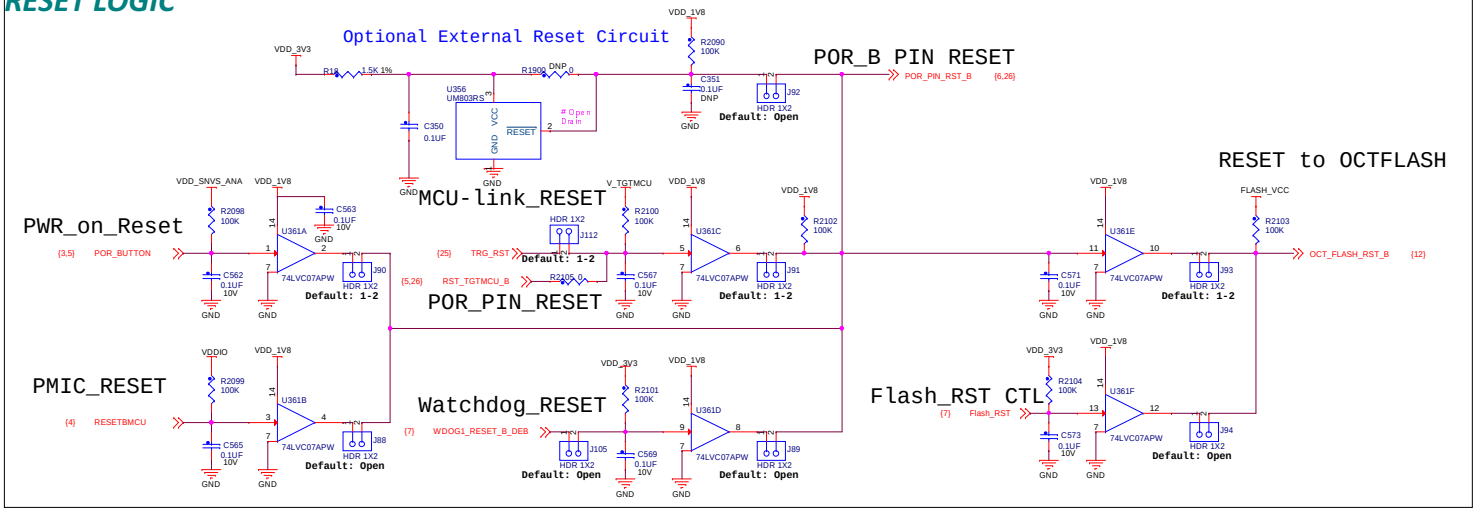


AUDIO AUX CONN

If Audio aux conn (J75) is used, please mount resistors below, R1996,R1994,R1991,R1990,R1995,R1992,R1993



RESET LOGIC



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