Radiation hardness of FDSOI and FinFET Technologies

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Silicon-On-Insulator (SOI) has long been recognized to provide inherent resistance to transient ionizing radiation effects due to the isolation from the substrate. The buried insulating layer (buried oxide – BOX) is also known to introduce problematic considerations for total ionizing dose (TID) radiation effects, particularly for fully-depleted (FD) SOI. Recent work in characterization of TID effects in partially depleted (PD) SOI indicates that the inherently high doping levels of the body region result in insensitivity to TID [1-2]. The pros and cons generally apply to all SOI-based technologies, including thin-film CMOS as well as thick film bipolar, LDMOS, and power MOSFETs. Space and military devices continue to be an opportunity for thin and thick SOI devices where the BOX limits global photocurrets in high dose-rate environments, and local photocurrents in heavy-ion space environments. At the same time, single-event effects (SEE) have become an increasing reliability concern in terrestrial electronics, particularly in sub-65 nm CMOS circuits. Small amounts of charge representing each bit of information, high clock speeds, low operating voltages, and high packing densities all exacerbate the sensitivity to ionizing particles. Terrestrial neutron effects, and more recently direct ionization by protons and muons, are significant considerations in present and emerging electronic devices [3-4], motivating a closer look at SEE in ultra-thin (UT) FDSOI.

The amount of charge required to upset a circuit, typically referred to as critical charge (Q_{crit}), is a circuit parameter that depends on capacitances (primarily gate capacitance), drive currents, operating voltages, and the circuit topology. To first order, these are comparable in bulk and SOI technologies. The primary differences between bulk and SOI are in the mechanisms of the conversion of energy (charge) generated by a particle to collected charge at circuit nodes. Historically, the single-event benefit of SOI over bulk was viewed in the following way: (1) bulk drains were the most sensitive areas in CMOS circuits since they collected charge most efficiently; (2) placement of an insulator beneath a fully-bottomed junction (i.e., SOI) truncated this charge collection and an ion could not deposit sufficient charge in the limited drain depletion region (Figure 1); (3) floating body parasitic bipolar amplification of charge deposited in an SOI channel resulted in a longer equivalent path length so channel regions were the most sensitive regions for SOI; (4) the channel area was smaller than the drain area so that SOI had a net improvement for soft error rates (SERs).

The general trend in SOI is towards thinner-layer, fully-depleted planar devices, or non-planar structures such as raised junction FETs or FinFETS. Previous work has shown that bulk FinFETs will tend to collect more charge than SOI FinFETS due to substrate contributions [5]; however the significance of this for upset threshold is unclear and depends on the circuit application. CMOS scaling (Moore's Law) has lead us to a regime where critical charges are estimated to be approaching values on the order of < 0.1 fC, which can be deposited over very short path lengths. And while UT-FDSOI channels are very thin, the raised junctions are several times thicker, meaning that we may be back to the drain and source regions being considerations. Figure 2 plots the maximum generated charge vs. path length in silicon for the peak linear energy transfer (LET) values of a common alpha particle and a muon.

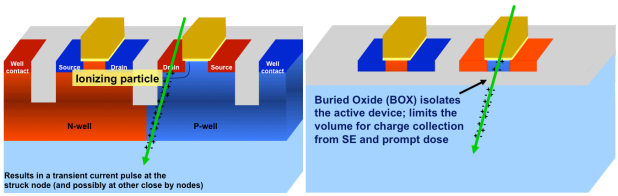

Figure 1. Classic view of single events in bulk vs. SOI.

Quantification of SERs (also called failures in time, FITs) is more complex than just the silicon thickness story. To calculate SERs, one must also consider the sensitive area (volume) of the device, and the distribution of particle energies in a given environment (i.e., only a small percentage of the particles will have the maximum LET, while some may induce rare, extreme events). Defining the effective path length and sensitive regions has become much less clear with device dimensions and layer thicknesses that are much smaller than the characteristic region of influence of an ionizing particle. In fact, the mechanism for energy deposition is a cascading series of many atomic-scale interactions, each producing products that vary in mass, energy, and direction, and typically having ranges that are comparable or greater than single device dimensions [6]. The details of these interactions cannot necessarily be ignored, as has largely been the case in the past where an average energy per unit path length was used (as in Figure 2). Further, with critical charges on the orders on 1000 electrons, it is not clear that insulating regions can be ignored as they have in the past. The high-Z metals used for gate materials and for silicided junctions have the potential to enhance the single event sensitivity (true for bulk and SOI). Issues of capacitive coupling among proximal devices UT-FDSOI technologies have not been well characterized, and may also be a consideration for radiation effects analysis [7]. Figure 3 illustrates several considerations for SERs.

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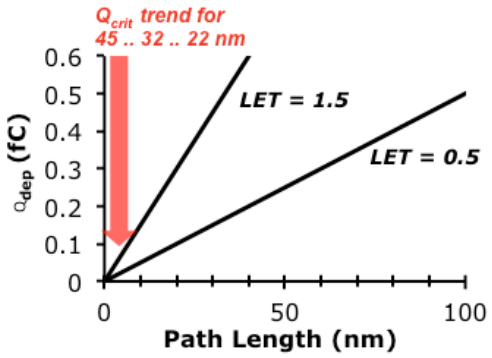

Figure 2. Deposited charge vs. path length for two linear energy transfer (LET) values of interest for terestrial environments using simple average LET model.

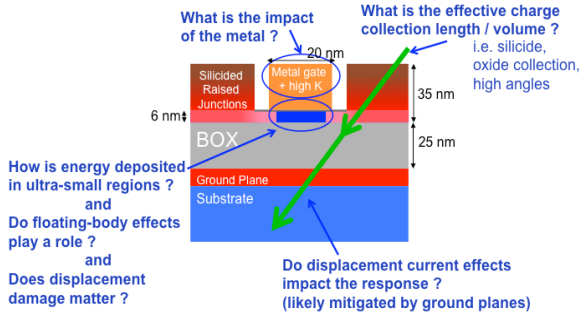

Figure 3. Considerations for quanitative single -event analysis of advanced UT-FDOI devices.

While there is much quantitative uncertainty, and a clear need for experimental and theoretical study, it is useful to use a set of assumptions based on what is known about the structures of bulk and UT-FDSOI and make a preliminary guess at the relative parameters of interest. Comparing an SRAM in bulk and UT-FDSOI, the maximum collection depth in bulk may be on the order of 10× larger (well depth vs. raised SOI junctions), and the sensitive area may be more than 2× greater in bulk (well area vs. active area). This means that more of the particles in a given environment will be able to upset the bulk cell, and there will be a higher probability of an upset due to the larger sensitive area. Further, the bulk technology will tend to be more susceptible to multiple bit upsets (MBUs). Table 1 summarizes a set of assumptions for such a comparison, and some possible outcomes for comparison of SERs (shown as FITs) based upon Monte Carlo Radiation Energy Deposition (MRED) simulations.

In order to quantify the radiation sensitivity with any confidence, it is necessary to experimentally characterize technologies, and develop calibrated models of radiation response mechanisms, enabling estimates of higher order parameters, such as SERs. Present and emerging technology variants, such as PDSOI CMOS, UT-FDSOI CMOS, and non-planar multi-gate structures each present some unique considerations. One common challenge is the treatment of the very small volumes of the active silicon regions; in particular the processes of energy deposition and charge transport in the complex device structures. This is presently one of the greatest sources of uncertainty in the translation of a radiation environment into the device response and associated event rate. Present Monte-Carlo Energy Deposition codes (such as Vanderbilt's MRED [8]), can be used to simulate the energy deposition of complex structures; however, the small dimensions of devices such as UT-FDSOI push the limits of such codes.

Table 1. PRELIMINARY UNCALIBRATED 22 nm SRAM SER PARAMATER COMPARISON OF BULK AND UT-FDSOI.

Parameter	Bulk	UT-FDSOI	Possible SOI Advantage
Q_{crit}	0.1 fC	0.1 fC	=
Cell area	0.1 μm²	0.1 μm²	=
Sensitive area/bit	0.05-0.1 μm²	0.02-0.05 μm²	> 2X
Sensitive depth	~ 500 nm	< 50 nm	> 10X
FIT (neutrons)	100-300	< 100	3X-6X
FIT (muons)	10000	< 100	>1000X

There are several ongoing efforts in the study of radiation effects in advanced technologies, including SOI. PDSOI CMOS is being studied at the 45 nm node both experimentally and using modeling [3, 9-10]. Vanderbilt is currently characterizing a new 45 nm SOI CMOS radiation test chip, and has designed a 32 nm SOI CMOS test chip. Vanderbilt is also working to enhance simulation capabilities to address the energy deposition in very small volumes, and to develop better single-event models for SOI devices (including compact models for process design kits), as well as collaborating with several leading organizations within the SOI community to study and quantify SEE in emerging SOI devices. The combination of experimental and theoretical studies will be vital to quantify the single event advantages that may be offered by next generation SOI-based devices. The preliminary estimates indicating the possibility of exploding FIT rates due to scaling, and the potential of UT-FDOSI to address the challenge, certainly present a compelling picture of the need for detailed studies.

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