Data sheet

BMM150
Geomagnetic Sensor

Bosch Sensortec

BMM150: Data sheet	
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BMM150

THREE-AXIS GEOMAGNETIC SENSOR

Key features

Three-axis magnetic field sensor

x Ultra-Small package	**W**afer **L**evel **C**hip **S**cale **P**ackage (12 pins, 0.4mm diagonal ball pitch) footprint 1.56 x 1.56 mm^2, height 0.6 mm
x Digital interface	SPI (4-wire, 3-wire), I²C, 4, 2 interrupt pins
x Low voltage operation	V_{DD} supply voltage range: 1.62V to 3.6V V_{DDIO} interface voltage range: 1.2V to 3.6V
x Flexible functionality	Magnetic field range typical: ±1300µT (x, y-axis), ±2500µT (z-axis) Magnetic field resolution of ~0.3µT
x On-chip interrupt controller	Interrupt-signal generation for - new data - magnetic Low-/High-Threshold detection
x Ultra-low power	Low current consumption (170µA @ 10 Hz in low power preset), short wake-up time, advanced features for system power management
x Temperature range	-40 °C … +85 °C
x RoHS compliant, halogen-free	

Typical applications

- x Magnetic heading information
- x Tilt-compensated electronic compass for map rotation, navigation and augmented reality
- x Gyroscope calibration in 9-DoF applications for mobile devices
- x In-door navigation, e.g. step counting in combination accelerometer
- x Gaming

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General Description

The BMM150 is a standalone geomagnetic sensor for consumer market applications. It allows measurements of the magnetic field in three perpendicular axes. Based on Bosch's proprietary FlipCore technology, performance and features of BMM150 are carefully tuned and perfectly match the demanding requirements of all 3-axis mobile applications such as electronic compass, navigation or augmented reality.

An evaluation circuitry (ASIC) converts the output of the geomagnetic sensor to digital results which can be read out over the industry standard digital interfaces (SPI and I2C).

Package and interfaces of the BMM150 have been designed to match a multitude of hardware requirements. As the sensor features an ultra-small footprint and a flat package, it is ingeniously suited for mobile applications. The wafer level chip scale package (WLCSP) with dimensions of only 1.56 x 1.56 x 0.6 mm^3 ensures high flexibility in PCB placement.

The BMM150 offers ultra-low voltage operation (V_{DD} voltage range from 1.62V to 3.6V, V_{DDIO} voltage range 1.2V to 3.6V) and can be programmed to optimize functionality, performance and power consumption in customer specific applications. The programmable interrupt engine gives design flexibility to the developer.

The BMM150 senses the three axis of the terrestrial field in cell phones, handhelds, computer peripherals, man-machine interfaces, virtual reality features and game controllers.

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1. Specification

If not stated otherwise, the given values are over lifetime and full performance temperature and voltage ranges, minimum/maximum values are ±3 V

1.1 Electrical operation conditions

Table 1: Electrical parameter specification

OPERATING CONDITIONS						
Parameter	**Symbol**	**Condition**	**Min**	**Typ**	**Max**	**Unit**
Supply Voltage Internal Domains	V_{DD}		1.62	2.4	3.6	V
Supply Voltage I/O Domain	V_{DDIO}		1.2	1.8	3.6	V
Voltage Input Low Level	$V_{IL,a}$	SPI & I²C			$0.3V_{DDIO}$	-
Voltage Input High Level	$V_{IH,a}$	SPI & I²C	$0.7V_{DDIO}$			-
Voltage Output Low Level	V_{OL}	V_{DDIO} = 1. 2V I_{OL} = 3mA, SPI & I²C			$0.2V_{DDIO}$	-
Voltage Output High Level	V_{OH}	V_{DDIO} = 1.62V I_{OH} = 2mA, SPI & I²C	$0.8V_{DDIO}$			-
Magnetic field range	$B_{rg,xy}$	T_A=25°C[1]	±1200	±1300		µT
	$B_{rg,z}$		±2000	±2500		µT
Magnetometer heading accuracy [2]	$Ac_{heading}$	30µT horizontal geomagnetic field component, T_A=25°C			±2.5	deg
Supply Current in Active Mode (average)[3]	$I_{DD,lp,m}$	Low power preset Nominal V_{DD} supplies T_A=25°C, ODR=10Hz		170		µA
	$I_{DD,rg,m}$	Regular preset Nominal V_{DD} supplies T_A=25°C, ODR=10Hz		0.5		mA
	$I_{DD,eh,m}$	Enhanced regular preset Nominal V_{DD} supplies		0.8		mA

[1] Full linear measurement range considering sensor offsets.
[2] The heading accuracy depends on hardware and software. A fully calibrated sensor and ideal tilt compensation are assumed.
[3] For details on magnetometer current consumption calculation refer to chapter 4.2.1 and 4.2.2.

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		T_A=25°C, ODR=10Hz				
	$I_{DD,ha,m}$	High accuracy preset Nominal V_{DD} supplies T_A=25°C, ODR=20Hz		4.9		mA
Supply Current in Suspend Mode	$I_{DDsm,m}$	Nominal V_{DD}/V_{DDIO} supplies, T_A=25°C		1	3	µA
Peak supply current in Active Mode	$I_{DDpk,m}$	In measurement phase Nominal V_{DD} supplies T_A=25°C		18	20	mA
Peak logic supply current in active mode	$I_{DDIOpk,m}$	Only during measurement phase Nominal V_{DDIO} supplies T_A=25°C		210	270	µA
POR time	$t_{w_up,m}$	from OFF to Suspend; time starts when VDD>1.5V and VDDIO>1.1V			1.0	ms
Start-Up Time	$t_{s_up,m}$	from Suspend to sleep			3.0	ms

1.2 Magnetometer output signal specification

MAGNETOMETER OUTPUT SIGNAL						
Parameter	**Symbol**	**Condition**	**Min**	**Typ**	**Max**	**Unit**
Device Resolution	$D_{res,m}$	T_A=25°C		0.3		µT
Gain error[4]	$G_{err,m}$	After API compensation T_A=25°C Nominal V_{DD} supplies		±2	±5	%
Sensitivity Temperature Drift	TCS_m	After API compensation - f & "A 7 f & Nominal V_{DD} supplies		±0.01	±0.03	%/K
Zero-B offset	OFF_m	T_A=25°C		±40		µT

[4] Definition: gain error = ((measured field after API compensation) / (applied field)) - 1

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Zero-B offset	$OFF_{m,cal}$	After software calibration with Bosch Sensortec eCompass software[5] - ƒ & "A 7 ƒ &		±2		µT
ODR (data output rate), normal mode	odr_{lp}	Low power preset		10		Hz
	odr_{rg}	Regular preset	9.2	10	10.8	Hz
	odr_{eh}	Enhanced regular preset		10		Hz
	odr_{ha}	High accuracy preset		20		Hz
ODR (data output rate), forced mode	odr_{lp}	Low power preset	0		>300	Hz
	odr_{rg}	Regular preset	0		100	Hz
	odr_{eh}	Enhanced regular preset	0		60	Hz
	odr_{ha}	High accuracy preset	0		20	Hz
Full-scale Nonlinearity	$NL_{m,\ FS}$	best fit straight line			1	%FS
Output Noise	$n_{rms,lp,m,xy}$	Low power preset x, y-axis, T_A=25°C Nominal V_{DD} supplies		1.0		µT
	$n_{rms,lp,m,z}$	Low power preset z-axis, T_A=25°C Nominal V_{DD} supplies		1.4		µT
	$n_{rms,rg,m}$	Regular preset T_A=25°C Nominal V_{DD} supplies		0.6		µT
	$n_{rms,eh,m}$	Enhanced regular preset T_A=25°C Nominal V_{DD} supplies		0.5		µT
	$n_{rms,ha,m}$	High accuracy preset T_A=25°C Nominal V_{DD} supplies		0.3		µT
Power Supply Rejection Rate	$PSRR_m$	T_A=25°C Nominal V_{DD} supplies		±0.5		µT/V

[5]Magnetic zero-B offset assuming calibration with Bosch Sensortec eCompass software. Typical value after applying calibration movements containing various device orientations (typical device usage).

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2. Absolute maximum ratings

The absolute maximum ratings are provided in Table 2. At or above these maximum ratings operability is not given. The specification limits in Chapter 1 only apply under normal operating conditions.

Table 2: Absolute maximum ratings

Parameter	Condition	Min	Max	Unit
Voltage at Supply Pin	V_{DD} Pin	-0.3	4.0	V
	V_{DDIO} Pin	-0.3	4.0	V
Voltage at any Logic Pad	Non-Supply Pin	-0.3	VDDIO + 0.3	V
Operating Temperature, T_A	Active operation	-40	+85	°C
Passive Storage Temp. Range	” U H O +	-50	+150	°C
None-volatile memory (NVM) Data Retention	T = 85°C	10		year
Mechanical Shock according to JESD22-B111….	Duration ” 200µs		10,000	g
	Duration ” .0ms		2,000	g
	Free fall onto hard surfaces		1.8	m
ESD	HBM, at any Pin		2	kV
	CDM		500	V
Magnetic field	Any direction		> 7	T

Note:
Stress above these limits may cause damage to the device. Exceeding the specified limits may affect the device reliability or cause malfunction.

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3. Block diagram

Figure 1 shows the basic building blocks of the BMM150:

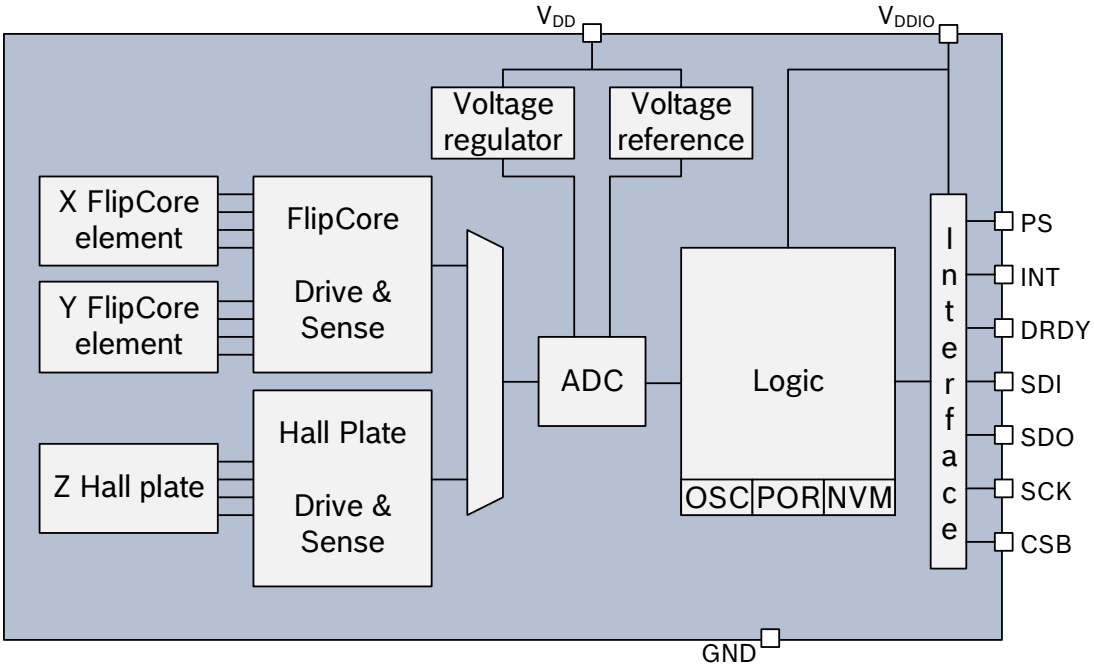

Figure 1: Block diagram of BMM150

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4. Functional description

BMM150 is a triaxial standalone geomagnetic sensor (Sensing element and ASIC) in chip scale wafer level package and can be operated via I2C or SPI as a slave device.

4.1 Power management

The BMM150 has two distinct power supply pins:
• V_{DD} is the main power supply for all internal analog and digital functional blocks;
• V_{DDIO} is a separate power supply pin, used for the supply of the digital interface as well as the digital logic.
The device can be completely switched off (V_{DD} = 0V) while keeping the V_{DDIO} supply on (V_{DDIO} > 0V) or vice versa.

It is absolutely prohibited to keep any interface at a logical high level when V_{DDIO} is switched off. Such a configuration will permanently damage the device (i.e. if V_{DDIO} = 0 Æ[SDI & SDO & SCK & CSB] • high).

The device contains a power on reset (POR) generator. It resets the logic part and the register values of the concerned ASIC after powering-on V_{DD} and V_{DDIO}. Please note, that all application specific settings which are not equal to the default settings (refer to register maps in chapter 5.2), must be re-set to its designated values after POR.
In case the I²C interface is used, a direct electrical connection between V_{DDIO} supply and the PS pin is recommended in order to ensure reliable protocol selection.

4.2 Power modes

The BMM150 features configurable power modes. The BMM150 magnetometer part has four power modes:In the following chapters, power modes are described.

4.2.1 Power off mode

In Power off mode, V_{DD} and/or V_{DDIO} are unpowered and the device does not operate. When only one of V_{DD} or V_{DDIO} is supplied, the magnetic sensor will still be in Power off mode. Power on reset is performed after both V_{DD} and V_{DDIO} raised above their detection thresholds.

4.2.2 Suspend mode

Suspend mode is the default power mode of BMM150 after the chip is powered. When V_{DD} and V_{DDIO} are turned on the POR (power on reset) circuits operate and the device's registers are initialized. After POR becomes inactive, a start up sequence is executed. In this sequence NVM content is downloaded to shadow registers located in the device core. After the start up sequence the device is put in the Suspend mode. In this mode only registers which store power control bit information and SPI3 wire enable can be accessed by the user. No other registers can be accessed in Suspend mode. All registers lose their content, except the control register (0x4B). In particular, in this mode a Chip ID read (register 0x40) returns "0x00" (I²C) or high-Z (SPI).

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4.2.3 Sleep mode

The user puts device from suspend into Sleep mode by setting the Power bit to “1”, or from active modes (normal or forced) by setting OpMode bits to “11”. In this state the user has full access to the device registers. In particular, the Chip ID can be read. Setting the power control bit to “0” (register 0x4B bit0) will bring the device back into Suspend mode. From the Sleep mode the user can put the device back into Suspend mode or into Active mode.

4.2.4 Active mode

The device can switch into Active mode from Sleep mode by setting OpMode bits (register 0x4C). In this mode the magnetic field measurements are performed and all registers are accessible.
In active mode, two operation modes can be distinguished:

- Normal mode: selected channels are periodically measured according to settings set in user registers. After measurements are completed, output data is put into data registers and the device waits for the next measurement period, which is set by programmed output data rate (ODR). From normal mode, the user can return to sleep mode by setting OpMode to “11” or by performing a soft reset (see chapter 5.6). Suspend mode can be entered by setting power control bit to “0”.
- Forced mode (single measurement): When set by the host, the selected channels are measured according to settings programmed in user registers. After measurements are completed, output data is put into data registers, OpMode register value returns to “11” and the device returns to sleep mode. The forced mode is useful to achieve synchronized operation between host microcontroller and BMM150. Also, different data output rates from the ones selectable in normal mode can be achieved using forced mode.

Figure 2: Magnetometer power mode transition diagram

In Active Mode and normal operation, in principle any desired balance between output noise and active time (hence power consumption) can be adjusted by the repetition settings for x/y-axis and z-axis and the output data rate ODR. The average power consumption depends on the ratio of high current phase time (during data acquisition) and low current phase time (between data acquisitions). Hence, the more repetitions are acquired to generate one magnetic field data point, the longer the active time ratio in one sample phase, and the higher the average current. Thanks

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to longer internal averaging, the noise level of the output data reduces with increasing number of repetitions.
By using forced mode, it is possible to trigger new measurements at any rate. The user can therefore trigger measurements in a shorter interval than it takes for a measurement cycle to complete. If a measurement cycle is not allowed to complete, the resulting data will not be written into the data registers. To prevent this, the manually triggered measurement intervals must not be shorter than the active measurement time which is a function of the selected number of repetitions. The maximum selectable read-out frequency in forced mode can be calculated as follows:

$$f_{max,ODR} \mid \frac{1}{145\mu s \ unXY \quad 500\mu s \ unZ \quad 980\mu s}$$

Hereby nXY is the number of repetitions on X/Y-axis (not the register value) and nZ the number of repetitions on Z-axis (not the register value) (see description of XY_REP and Z_REP registers in chapter 5).

Although the repetition numbers for X/Y and Z axis and the ODR can be adjusted independently and in a wide range, there are four recommended presets (High accuracy preset, Enhanced regular preset, Regular preset, Low power preset) which reflect the most common usage scenarios, i.e. required output accuracy at a given current consumption, of the BMM150.

The four presets consist of the below register configurations, which are automatically set by the BMM150 API or driver provided by Bosch Sensortec when a preset is selected. Table 3 shows the recommended presets and the resulting magnetic field output noise and current consumption:

Table 3: Recommended presets for repetitions and output data rates:

Preset	**Rep. X/Y** **nXY**	**Rep. Z** **nZ**	**recommended ODR** **[Hz]**	**Max ODR in forced mode fmax,ODR** **[Hz]**	**RMS Noise x/y/z** **[µT]**	**Average current consumption at recommended ODR** **[mA]**
Low power preset	3	3	10	>300	1.0/1.0/1.4	0.17
Regular preset	9	15	10	100	0.6/0.6/0.6	0.5
Enhanced regular preset	15	27	10	60	0.5/0.5/0.5	0.8
High accuracy preset	47	83	20	20	0.3/0.3/0.3	4.9

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4.3 Sensor output data

4.3.1 Magnetic field data

The representation of magnetic field data is different between X/Y-axis and Z-axis. The width of X- and Y-axis magnetic field data is 13 bits each and stored in two's complement.
DATAX_LSB (0x42) contains 5-bit LSB part [4:0] of the 13 bit output data of the X-channel.
DATAX_MSB (0x43) contains 8-bit MSB part [12:5] of the 13 bit output data of the X-channel.
DATAY_LSB (0x44) contains 5-bit LSB part [4:0] of the 13 bit output data of the Y-channel.
DATAY_MSB (0x45) contains 8-bit MSB part [12:5] of the 13 bit output data of the Y-channel.

The width of the Z-axis magnetic field data is 15 bit word stored in two's complement.
DATAZ_LSB (0x46) contains 7-bit LSB part [6:0] of the 15 bit output data of the Z-channel.
DATAZ_MSB (0x47) contains 8-bit MSB part [14:7] of the 15 bit output data of the Z-channel.

For all axes, temperature compensation on the host is used to get ideally matching sensitivity over the full temperature range. The temperature compensation is based on a resistance measurement of the hall sensor plate. The resistance value is represented by a 14 bit unsigned output word.
RHALL_LSB (0x48) contains 6-bit LSB part [5:0] of the 14 bit output data of the RHALL-channel.
RHALL_MSB (0x49) contains 8-bit MSB part [13:6] of the 14 bit output data of the RHALL-channel.

All signed register values are in two´s complement representation. Bits which are marked "reserved" can have different values or can in some cases not be read at all (read will return 0x00 in I²C mode and high-Z in SPI mode).

Data register readout and shadowing is implemented as follows:
After all enabled axes have been measured; complete data packages consisting of DATAX, DATAY, DATAZ and RHALL are updated at once in the data registers. This way, it is prevented that a following axis is updated while the first axis is still being read (axis mix-up) or that MSB part of an axis is updated while LSB part is being read.
While reading from any data register, data register update is blocked. Instead, incoming new data is written into shadow registers which will be written to data registers after the previous read sequence is completed (i.e. upon stop condition in I²C mode, or CSB going high in SPI mode, respectively). Hence, it is recommended to read out at all data at once (0x42 to 0x49 or 0x4A if status bits are also required) with a burst read.
Single bytes or axes can be read out, while in this case it is not assured that adjacent registers are not updated during readout sequence.

The "Data ready status" bit (register 0x48 bit0) is set "1" when the data registers have been updated but the data was not yet read out over digital interface. Data ready is cleared (set "0") directly after completed read out of any of the data registers and subsequent stop condition (I²C) or lifting of CSB (SPI).

In addition, when enabled the "Data overrun" bit (register 0x4A bit7) turns "1" whenever data registers are updated internally, but the old data was not yet read out over digital interface (i.e. data ready bit was still high). The "Data overrun" bit is cleared when the interrupt status register 0x4A is read out. This function needs to be enabled separately by setting the "Data overrun En" bit (register 0x4D bit7)).

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Note:
Please also see chapter 5 for detailed register descriptions.

4.3.2 Magnetic field data temperature compensation

The raw register values DATAX, DATAY, DATAZ and RHALL are read out from the host processor using the BMM150 API/driver which is provided by Bosch Sensortec. The API/driver performs an off-chip temperature compensation and outputs x/y/z magnetic field data in 16 LSB/µT to the upper application layer:

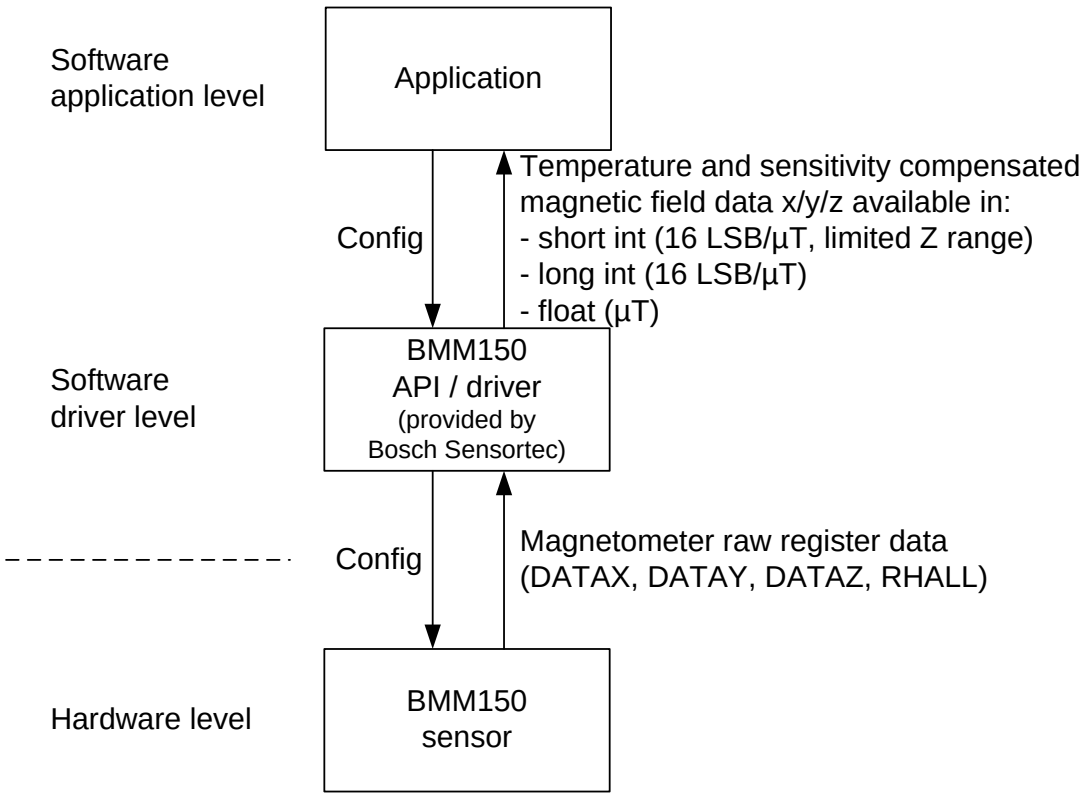

Figure 3: Calculation flow of magnetic field data from raw BMM150 register data

The API/driver performs all calculations using highly optimized fixed-point C-code arithmetic. For platforms that do not support C code, a floating-point formula is available as well.

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4.4 Self-test

BMM150 supports two self-tests modes: Normal self-test and advanced self-test.

4.4.1 Normal self test

During normal self-test, the following verifications are performed:
FlipCore signal path is verified by generating signals on-chip. These are processed through the signal path and the measurement result is compared to known thresholds.

- FlipCore (X and Y) connection to ASIC are checked for connectivity and short circuits
- Hall sensor connectivity is checked for open and shorted connections
- Hall sensor signal path and hall sensor element offset are checked for overflow.

To perform a self test, the sensor must first be put into sleep mode (OpMode = “11”). Self-test mode is then entered by setting the bit “Self test” (register 0x4C bit0) to “1”. After performing self test, this bit is set back to “0”. When self-test is successful, the corresponding self-test result bits are set to “1” (“X-Self-Test” register 0x42 bit0, “Y-Self-Test” register 0x44 bit0, “Z-Self-Test” register 0x46 bit0). If self-test fails for an axis, the corresponding result bit returns “0”.

4.4.2 Advanced self test

Advanced self test performs a verification of the Z channel signal path functionality and sensitivity. An on-chip coil wound around the hall sensor can be driven in both directions with a calibrated current to generate a positive or negative field of around 100 µT.

Advanced self test is an option that is active in parallel to the other operation modes. The only difference is that during the active measurement phase, the coil current is enabled. The recommended usage of advanced self test is the following:

1. Set sleep mode
2. Disable X, Y axis
3. Set Z repetitions to desired level
4. Enable positive advanced self test current
5. Set forced mode, readout Z and R channel after measurement is finished
6. Enable negative advanced self test current
7. Set forced mode, readout Z and R channel after measurement is finished
8. Disable advanced self test current (this must be done manually)
9. Calculate difference between the two compensated field values. This difference should be around 200 µT with some margins.
10. Perform a soft reset of manually restore desired settings

Please refer to the corresponding application note for the exact thresholds to evaluate advanced self-test.

The table below describes how the advanced self-test is controlled:

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Table 4: Magnetometer advanced self-test control

(0x4C) Adv.ST <1:0>	Configuration
00b	Normal operation (no self-test), default
01b	Reserved, do not use
10b	Negative on-chip magnetic field generation
11b	Positive on-chip magnetic field generation

The BMM150 API/driver provided by Bosch Sensortec provides a comfortable way to perform both self-tests and to directly obtain the result without further calculations. It is recommended to use this as a reference.

4.5 Non-volatile memory

Some of the memory of the BMM150 magnetometer is non-volatile memory (NVM). This NVM is pre-programmed in Bosch Sensortec fabrication line and cannot be modified afterwards. It contains trimming data which are required for sensor operation and sensor data compensation, thus it is read out by the BMM150 API/driver during initialization.

4.6 Magnetometer interrupt controller

Four magnetometer based interrupt engines are integrated in the BMM150: Low-Threshold, High-Threshold, Overflow and Data Ready (DRDY). Each interrupt can be enabled independently.

When enabled, an interrupt sets the corresponding status bit in the interrupt status register (0x4A) when its condition is satisfied.
When the “Interrupt Pin Enable” bit (register 0x4E bit6) is set, any occurring activated interrupts are flagged on the BMM150’s INT output pin. By default, the interrupt pin is disabled (high-Z status).

Low-Threshold, High-Threshold and Overflow interrupts are mapped to the INT pin when enabled, Data Ready (DRDY) interrupt is mapped to the DRDY pin of BMM150 when enabled. For High- and Low-Threshold interrupts each axis X/Y/Z can be enabled separately for interrupt detection in the registers “High Int Z en”, “High Int Y en”, “High Int X en”, “Low Int Z en”, “Low Int Y En” and “Low Int X En” in register 0x4D bit5-bit0. Overflow interrupt is shared for X, Y and Z axis.

When the “Data Ready Pin En” bit (register 0x4E bit7) is set, the Data Ready (DRDY) interrupt event is flagged on the BMM150’s DRDY output pin (by default the “Data Ready Pin En” bit is not set and DRDY pin is in high-Z state).
The interrupt status registers are updated together with writing new data into the magnetic field data registers. The status bits for Low-/High-Threshold interrupts are located in register 0x4A, the Data Ready (DRDY) status flag is located at register 0x48 bit0.

If an interrupt is disabled, all active status bits and pins are reset after the next measurement was performed.

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4.6.1 General features

An interrupt is cleared depending on the selected interrupt mode, which is common to all interrupts. There are two different interrupt modes: non-latched and latched. All interrupts (except Data Ready) can be latched or non-latched. Data Ready (DRDY) is always cleared after readout of data registers ends.

A non-latched interrupt will be cleared on a new measurement when the interrupt condition is not valid anymore, whereas a latched interrupt will stay high until the interrupts status register (0x4A) is read out. After reading the interrupt status, both the interrupt status bits and the interrupt pin are reset. The mode is selected by the “Interrupt latch” bit (register 0x4A bit1), where the default setting of “1” means latched. Figure 4 shows the difference between the modes for the example Low-Threshold interrupt.

INT and DRDY pin polarity can be changed by the “Interrupt polarity” bit (register 0x4E bit0) and “DR polarity” (register 0x4E bit2), from the default high active (“1”) to low active (“0”).

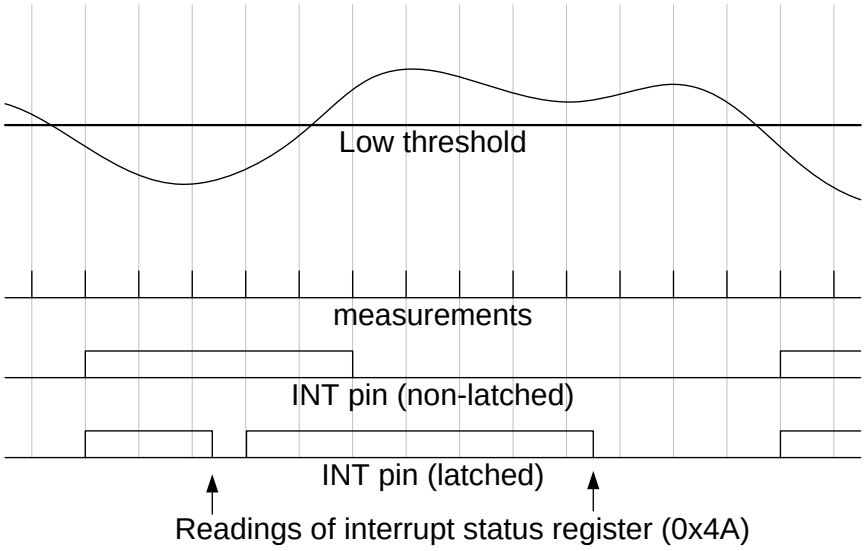

Figure 4: Interrupt latched and non-latched mode

4.6.2 Electrical behavior of magnetic interrupt pins

Both interrupt pins INT and DRDY are push/pull when the corresponding interrupt pin enable bit is set, and are floating (High-Z) when the corresponding interrupt pin enable bit is disabled (default).

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4.6.3 Data ready / DRDY interrupt

This interrupt serves for synchronous reading of magnetometer data. It is generated after storing a new set of values (DATAX, DATAY, DATAZ, RHALL) in the data registers:

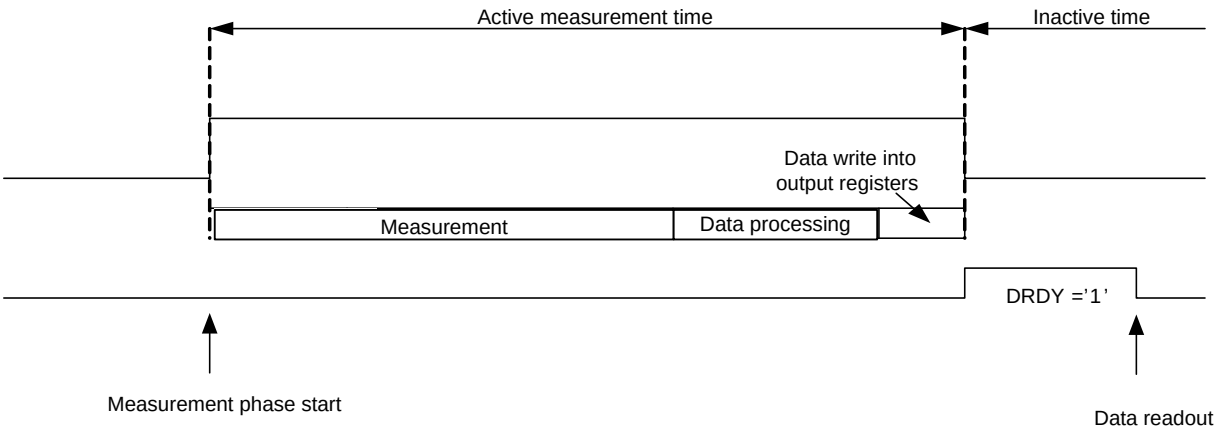

Figure 5: Data acquisition and DRDY operation (DRDY in “high active” polarity)

The interrupt mode of the Data Ready (DRDY) interrupt is fixed to non-latched.
It is enabled (disabled) by writing “1” (“0”) to “Data Ready pin En” in register 0x4E bit7.

DRDY pin polarity can be changed by the “DR polarity” bit (register 0x4E bit2), from the default high active (“1”) to low active (“0”).

4.6.4 Low-threshold interrupt

When the data registers’ (DATAX, DATAY and DATAZ) values drop below the threshold level defined by the “Low Threshold register (0x4F), the corresponding interrupt status bits for those axes are set (“Low Int X”, “Low Int Y” and “Low Int Z” in register 0x4A). This is done for each axis independently. Please note that the X and Y axis value for overflow is -4096. However, no interrupt is generated on these values. See chapter 4.6.6 for more information on overflow.

Hereby, one bit in “Low Threshold” corresponds to roughly 6µT (not exactly, as the raw magnetic field values DATAX, DATAY and DATAZ are not temperature compensated).

The Low-threshold interrupt is issued on INT pin when one or more values of the data registers DATAX, DATAY and DATAZ drop below the threshold level defined by the “Low Threshold” register (0x4F), and when the axis where the threshold was exceeded is enabled for interrupt generation:

Result = (DATAX < “Low Threshold” x 16) AND “Low Int X en” is “0” OR
(DATAY < “Low Threshold” x 16) AND “Low Int Y en” is “0” OR
(DATAZ < “Low Threshold” x 16) AND “Low Int Z en” is “0”

Note: Threshold interrupt enable bits (“Low INT [XYZ] en”) are active low and “1” (disabled) by default.

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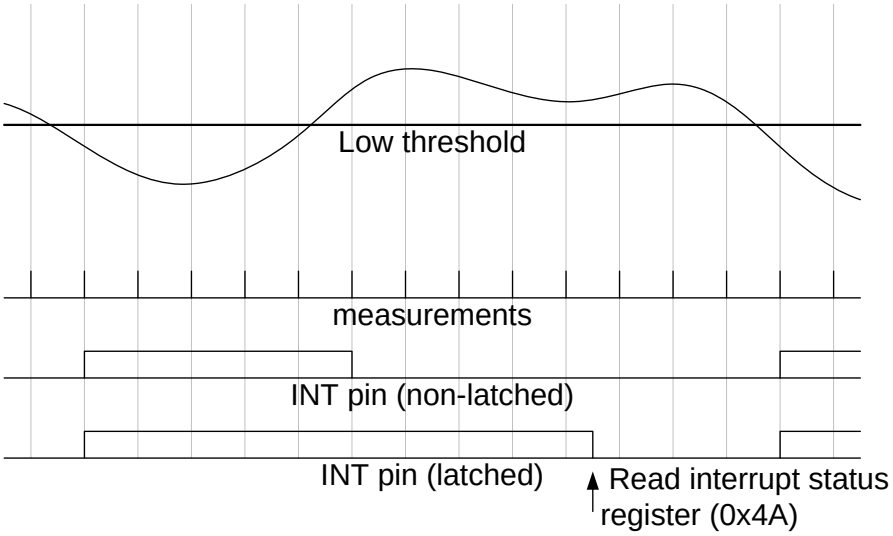

Figure 6: Low-threshold interrupt function

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4.6.5 High-threshold interrupt

When the data registers' (DATAX, DATAY and DATAZ) values exceed the threshold level defined by the "High Threshold register (0x50), the corresponding interrupt status bits for those axes are set ("High Int X", "High Int Y" and "High Int Z" in register 0x4A). This is done for each axis independently.
Hereby, one bit in "High Threshold" corresponds to roughly 6µT (not exactly, as the raw magnetic field values DATAX, DATAY and DATAZ are not temperature compensated).

The High-threshold interrupt is issued on INT pin when one or more values of the data registers DATAX, DATAY and DATAZ exceed the threshold level defined by the "High Threshold" register (0x50), and when the axis where the threshold was exceeded is enabled for interrupt generation:

Result = (DATAX > "High Threshold" x 16) AND "High Int X en" is "0" OR
(DATAY > "High Threshold" x 16) AND "High Int Y en" is "0" OR
(DATAZ > "High Threshold" x 16) AND "High Int Z en" is "0"

Note:
Threshold interrupt enable bits ("High INT [XYZ] en") are active low and "1" (disabled) by default.

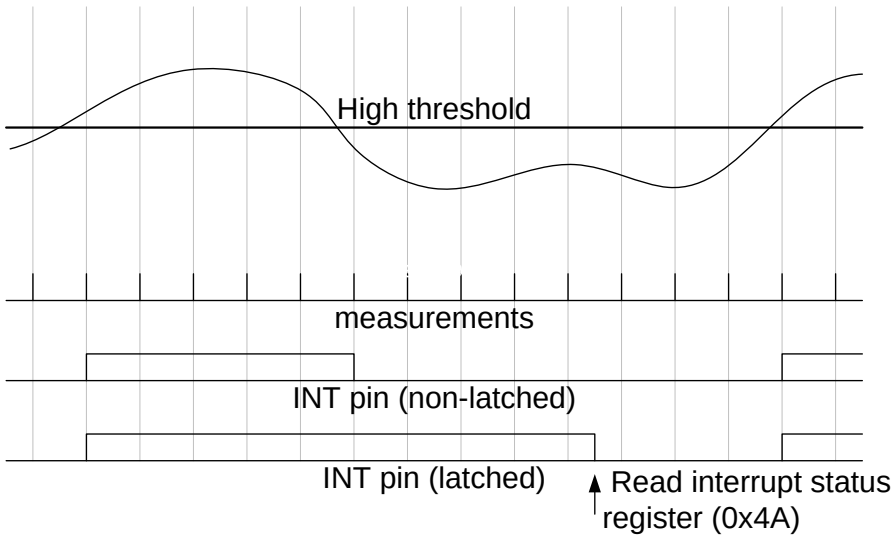

Figure 7: High-threshold interrupt function

4.6.6 Overflow

When a measurement axis had an overflow, the corresponding data register is saturated to the most negative value. For X and Y axis, the data register is set to the value -4096. For the Z axis, the data register is set to the value -16384.
The "Overflow" flag (register 0x4A bit6) indicates that the measured magnetic field raw data of one or more axes exceeded maximum range of the device. The overflow condition can be flagged on the INT pin by setting the bit "overflow int enable" (register 0x4D bit6, active high, default value "0"). The channel on which overflow occurred can by determined by assessing the DATAX/Y/Z registers.

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5. Register Description

5.1 General Remarks

The entire communication with the device's magnetometer part is performed by reading from and writing to registers. Registers have a width of 8 bits; they are mapped to a common space of 50 addresses from (0x40) up to (0x71). Within the used range there are several registers which are marked as 'reserved'. Any reserved bit is ignored when it is written and no specific value is guaranteed when read. Especially, in SPI mode the SDO pin may stay in high-Z state when reading some of these registers.

Registers with addresses from (0x40) up to (0x4A) are read-only. Any attempt to write to these registers is ignored.

5.2 Register map

Register Address	Default Value	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x71	N/A	reserved							
0x70	N/A								
0x6F	N/A								
0x6E	N/A								
0x6D	N/A								
0x6C	N/A								
0x6B	N/A								
0x6A	N/A								
0x69	N/A								
0x68	N/A								
0x67	N/A								
0x66	N/A								
0x65	N/A								
0x64	N/A								
0x63	N/A								
0x62	N/A								
0x61	N/A								
0x60	N/A								
0x5F	N/A								
0x5E	N/A								
0x5D	N/A								
0x5C	N/A								
0x5B	N/A								
0x5A	N/A								
0x59	N/A								
0x58	N/A								
0x57	N/A								
0x56	N/A								
0x55	N/A								
0x54	N/A								
0x53	N/A								
0x52	0x00	REPZ Number Of Repetitions (valid for Z) [7:0]							
0x51	0x00	REPXY Number Of Repetitions (valid for XY) [7:0]							
0x50	0x00	High Threshold [7:0]							
0x4F	0x00	Low Threshold [7:0]							
0x4E	0x07	Data Ready Pin En	Interrupt Pin En	Channel Z	Channel Y	Channel X	DR Polarity	Interrupt Latch	Interrupt Polarity
0X4D	0x3F	Data Overrun En	Overflow Int En	High Int Z en	High Int Y en	High Int X en	Low Int Z en	Low Int Y en	Low Int X en
0x4C	0x06	Adv. ST [1:0]		Data Rate [2:0]			Opmode [1:0]		Self Test
0x4B	0x00	Soft Reset '1'	fixed '0'	fixed '0'	fixed '0'	fixed '0'	SPI3en	Soft Reset '1'	Power Control Bit
0x4A	0x00	Data Overrun	Overflow	High Int Z	High Int Y	High Int X	Low Int Z	Low Int Y	Low Int X
0x49	N/A	RHALL [13:6] MSB							
0x48	N/A	RHALL [5:0] LSB						fixed '0'	Data Ready Status
0x47	N/A	DATA Z [14:7] MSB							
0x46	N/A	DATA Z [6:0] LSB							Z-Self-Test
0x45	N/A	DATA Y [12:5] MSB							
0x44	N/A	DATA Y [4:0] LSB					fixed '0'	fixed '0'	Y-Self-Test
0x43	N/A	DATA X [12:5] MSB							
0x42	N/A	DATA X [4:0] LSB					fixed '0'	fixed '0'	X-Self-Test
0x41	N/A	reserved							
0x40	0x32	Chip ID = 0x32 (can only be read if power control bit ="1")							

	w/r
	w/r accessible in suspend mode
	read only
	reserved

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5.3 Chip ID

Register (0x40) Chip ID contains the magnetometer chip identification number, which is 0x32. This number can only be read if the power control bit (register 0x4B bit0) is enabled.

Table 5: Chip identification number, register (0x40)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	1	1	0	0	1	0

Register (0x41) is reserved

5.4 Magnetic field data

Register (0x42) contains the LSB part of x-axis magnetic field data and the self-test result flag for the x-axis.

Table 6: LSB part of x-axis magnetic field, register (0x42)

(0x42) Bit	Name	Description
Bit 7	DATAX_lsb <4>	Bit 4 of x-axis magnetic field data
Bit 6	DATAX_lsb <3>	Bit 3 of x-axis magnetic field data
Bit 5	DATAX_lsb <2>	Bit 2 of x-axis magnetic field data
Bit 4	DATAX_lsb <1>	Bit 1 of x-axis magnetic field data
Bit 3	DATAX_lsb <0>	Bit 0 of x-axis magnetic field data = x LSB
Bit 2	-	(fixed to 0)
Bit 1	-	(fixed to 0)
Bit 0	SelfTestX	Self-test result flag for x-axis, default is “1”

Register (0x43) contains the MSB part of x-axis magnetic field data.

Table 7: MSB part of x-axis magnetic field, register (0x43)

(0x43) Bit	Name	Description
Bit 7	DATAX_msb <12>	Bit 12 of x-axis magnetic field data = x MSB
Bit 6	DATAX_msb <11>	Bit 11 of x-axis magnetic field data
Bit 5	DATAX_msb <10>	Bit 10 of x-axis magnetic field data
Bit 4	DATAX_msb <9>	Bit 9 of x-axis magnetic field data
Bit 3	DATAX_msb <8>	Bit 8 of x-axis magnetic field data
Bit 2	DATAX_msb <7>	Bit 7 of x-axis magnetic field data
Bit 1	DATAX_msb <6>	Bit 6 of x-axis magnetic field data
Bit 0	DATAX_msb <5>	Bit 5 of x-axis magnetic field data

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Register (0x44) contains the LSB part of y-axis magnetic field data and the self-test result flag for the y-axis.

Table 8: LSB part of y-axis magnetic field, register (0x44)

(0x44) Bit	Name	Description
Bit 7	DATAY_lsb <4>	Bit 4 of y-axis magnetic field data
Bit 6	DATAY_lsb <3>	Bit 3 of y-axis magnetic field data
Bit 5	DATAY_lsb <2>	Bit 2 of y-axis magnetic field data
Bit 4	DATAY_lsb <1>	Bit 1 of y-axis magnetic field data
Bit 3	DATAY_lsb <0>	Bit 0 of y-axis magnetic field data = y LSB
Bit 2	-	(fixed to 0)
Bit 1	-	(fixed to 0)
Bit 0	SelfTestY	Self-test result flag for y-axis, default is “1”

Register (0x45) contains the MSB part of y-axis magnetic field data.

Table 9: MSB part of y-axis magnetic field, register (0x45)

(0x45) Bit	Name	Description
Bit 7	DATAY_msb <12>	Bit 12 of y-axis magnetic field data = y MSB
Bit 6	DATAY_msb <11>	Bit 11 of y-axis magnetic field data
Bit 5	DATAY_msb <10>	Bit 10 of y-axis magnetic field data
Bit 4	DATAY_msb <9>	Bit 9 of y-axis magnetic field data
Bit 3	DATAY_msb <8>	Bit 8 of y-axis magnetic field data
Bit 2	DATAY_msb <7>	Bit 7 of y-axis magnetic field data
Bit 1	DATAY_msb <6>	Bit 6 of y-axis magnetic field data
Bit 0	DATAY_msb <5>	Bit 5 of y-axis magnetic field data

Register (0x46) contains the LSB part of z-axis magnetic field data and the self-test result flag for the z-axis.

Table 10: LSB part of z-axis magnetic field, register (0x46)

(0x46) Bit	Name	Description
Bit 7	DATAZ_lsb <6>	Bit 6 of z-axis magnetic field data
Bit 6	DATAZ_lsb <5>	Bit 5 of z-axis magnetic field data
Bit 5	DATAZ_lsb <4>	Bit 4 of z-axis magnetic field data
Bit 4	DATAZ_lsb <3>	Bit 3 of z-axis magnetic field data
Bit 3	DATAZ_lsb <2>	Bit 2 of z-axis magnetic field data
Bit 2	DATAZ_lsb <1>	Bit 1 of z-axis magnetic field data
Bit 1	DATAZ_lsb <0>	Bit 0 of z-axis magnetic field data = z LSB
Bit 0	SelfTestZ	Self-test result flag for z-axis, default is “1”

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Register (0x47) contains the MSB part of z-axis magnetic field data.

Table 11: MSB part of z-axis magnetic field, register (0x47)

(0x47) Bit	Name	Description
Bit 7	DATAZ_msb <14>	Bit 14 of y-axis magnetic field data = z MSB
Bit 6	DATAZ_msb <13>	Bit 13 of y-axis magnetic field data
Bit 5	DATAZ_msb <12>	Bit 12 of y-axis magnetic field data
Bit 4	DATAZ_msb <11>	Bit 11 of y-axis magnetic field data
Bit 3	DATAZ_msb <10>	Bit 10 of y-axis magnetic field data
Bit 2	DATAZ_msb <9>	Bit 9 of y-axis magnetic field data
Bit 1	DATAZ_msb <8>	Bit 8 of y-axis magnetic field data
Bit 0	DATAZ_msb <7>	Bit 7 of y-axis magnetic field data

Register (0x48) contains the LSB part of hall resistance and the Data Ready (DRDY) status bit.

Table 12: LSB part of hall resistance, register (0x48)

(0x48) Bit	Name	Description
Bit 7	RHALL_lsb <5>	Bit 5 of hall resistance
Bit 6	RHALL_lsb <4>	Bit 4 of hall resistance
Bit 5	RHALL_lsb <3>	Bit 3 of hall resistance
Bit 4	RHALL_lsb <2>	Bit 2 of hall resistance
Bit 3	RHALL_lsb <1>	Bit 1 of hall resistance
Bit 2	RHALL_lsb <0>	Bit 0 of hall resistance = RHALL LSB
Bit 1	-	(fixed to 0)
Bit 0	Data Ready Status	Data ready (DRDY) status bit

Register (0x49) contains the MSB part of hall resistance.

Table 13: MSB part of hall resistance, register (0x49)

(0x49) Bit	Name	Description
Bit 7	RHALL_msb <13>	Bit 13 of hall resistance = RHALL MSB
Bit 6	RHALL_msb <12>	Bit 12 of hall resistance
Bit 5	RHALL_msb <11>	Bit 11 of hall resistance
Bit 4	RHALL_msb <10>	Bit 10 of hall resistance
Bit 3	RHALL_msb <9>	Bit 9 of hall resistance
Bit 2	RHALL_msb <8>	Bit 8 of hall resistance
Bit 1	RHALL_msb <7>	Bit 7 of hall resistance
Bit 0	RHALL_msb <6>	Bit 6 of hall resistance

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5.5 Interrupt status register

Register (0x4A) contains the states of all interrupts.

Table 14: Interrupt status, register (0x4A)

(0x4A) Bit	Name	Description
Bit 7	Data overrun	Data overrun status flag
Bit 6	Overflow	Overflow status flag
Bit 5	High Int Z	High-Threshold interrupt z-axis status flag
Bit 4	High Int Y	High-Threshold interrupt y-axis status flag
Bit 3	High Int X	High-Threshold interrupt x-axis status flag
Bit 2	Low Int Z	Low-Threshold interrupt z-axis status flag
Bit 1	Low Int Y	Low-Threshold interrupt y-axis status flag
Bit 0	Low Int X	Low-Threshold interrupt x-axis status flag

5.6 Power and operation modes, self-test and data output rate control registers

Register (0x4B) contains control bits for power control, soft reset and interface SPI mode selection. This special control register is also accessible in suspend mode.

Soft reset is executed when both bits (register 0x4B bit7 and bit1) are set “1”. Soft reset does not execute a full POR sequence, but all registers are reset except for the “trim” registers above register 0x54 and the power control register (0x4B). Soft reset always brings the device into sleep mode. When device is in the suspend mode, soft reset is ignored and the device remains in suspend mode. The two “Soft Reset” bits are reset to “0” automatically after soft reset was completed. To perform a full POR reset, bring the device into suspend and then back into sleep mode.
When SPI mode is selected, the “SPI3En” bit enables SPI 3-wire mode when set “1”. When “SPI3En” is set “0” (default), 4-wire SPI mode is selected.
Setting the “Power Control bit” to “1” brings the device up from Suspend mode to Sleep mode, when “Power Control bit” is set “0” the device returns to suspend mode (see chapter 4.2 for details of magnetometer power modes).

Table 15: Power control, soft reset and SPI mode control register (0x4B)

(0x4B) Bit	Name	Description
Bit 7	Soft Reset ‘1’	One of the soft reset trigger bits.
Bit 6	-	(fixed to 0)
Bit 5	-	(fixed to 0)
Bit 4	-	(fixed to 0)
Bit 3	-	(fixed to 0)
Bit 2	SPI3en	Enable bit for SPI3 mode
Bit 1	Soft Reset ‘1’	One of the soft reset trigger bits.
Bit 0	Power Control bit	When set to “0”, suspend mode is selected

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Register (0x4C) contains control bits for operation mode, output data rate and self-test.

The two "Adv. ST" bits control the on-chip advanced self-test (see chapter 4.4.2 for details of the magnetometer advanced self-test).
The three "Data rate" bits control the magnetometer output data rate according to below Table 17.
The two "Opmode" bits control the operation mode according to below Table 18 (see chapter 4.2 for a detailed description of magnetometer power modes).

Table 16: Operation mode, output data rate and self-test control register (0x4C)

(0x4C) Bit	Name	Description
Bit 7	Adv. ST <1>	Advanced self-test control bit 1
Bit 6	Adv. ST <0>	Advanced self-test control bit 0
Bit 5	Data rate <2>	Data rate control bit 2
Bit 4	Data rate <1>	Data rate control bit 1
Bit 3	Data rate <0>	Data rate control bit 0
Bit 2	Opmode <1>	Operation mode control bit 1
Bit 1	Opmode <0>	Operation mode control bit 0
Bit 0	Self Test	Normal self-test control bit

Three "Data rate" bits control the output data rate (ODR) of the BMM150 magnetometer part:

Table 17: Output data rate (ODR) setting (0x4C)

(0x4C) Data rate <2:0>	Magnetometer output data rate (ODR) [Hz]
000b	10 (default)
001b	2
010b	6
011b	8
100b	15
101b	20
110b	25
111b	30

Two "Opmode" bits control the operation mode of the BMM150 magnetometer part:

Table 18: Operation mode setting (0x4C)

(0x4C) Opmode <1:0>	Magnetometer operation mode[6]
00b	Normal mode
01b	Forced mode
10b	Reserved, do not use
11b	Sleep Mode

[6] See chapter 4.2 for a detailed description of magnetometer power modes.

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5.7 Interrupt and axis enable settings control registers

Register (0x4D) contains control bits for interrupt settings. (Also refer to chapter 4.6 for the details of magnetometer interrupt operation).

Table 19: Interrupt settings control register (0x4D)

(0x4D) Bit	Name	Description
Bit 7	Data Overrun En	Enables data overrun indication in the “Data Overrun” flag (active high, default is “0” disabled)
Bit 6	Overflow Int En	Activates mapping of Overflow flag status to the INT pin (active high, default is “0” disabled)
Bit 5	High Int Z En	Enables the z-axis detection for High-Threshold interrupts (active low, default is “1” disabled)
Bit 4	High Int Y En	Enables the y-axis detection for High-Threshold interrupts (active low, default is “1” disabled)
Bit 3	High Int X En	Enables the x-axis detection for High-Threshold interrupts (active low, default is “1” disabled)
Bit 2	Low Int Z En	Enables the z-axis detection for Low-Threshold interrupts (active low, default is “1” disabled)
Bit 1	Low Int Y En	Enables the y-axis detection for Low-Threshold interrupts (active low, default is “1” disabled)
Bit 0	Low Int X En	Enables the x-axis detection for Low-Threshold interrupts (active low, default is “1” disabled)

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Register (0x4E) contains control bits interrupt settings and axes enable bits. (Also refer to chapter 0 for the details of magnetometer interrupt operation). If a magnetic measurement channel is disabled, its last measured magnetic output values will remain in the data registers. If the Z channel is disabled, the resistance measurement will also be disabled and the resistance output value will be set to zero. If interrupts are set to trigger on an axis that has been disabled, these interrupts will still be asserted based on the last measured value.

Table 20: Interrupt settings and axes enable bits control register (0x4E)

(0x4E) Bit	Name	Description
Bit 7	Data Ready Pin En	Enables data ready status mapping on DRDY pin (active high, default is “0” disabled)
Bit 6	Interrupt Pin En	Enables interrupt status mapping on INT pin (active high, default is “0” disabled)
Bit 5	Channel Z	Enable z-axis and resistance measurement (active low, default is “0” enabled)
Bit 4	Channel Y	Enable y-axis (active low, default is “0” enabled)
Bit 3	Channel X	Enable x-axis (active low, default is “0” enabled)
Bit 2	DR Polarity	Data ready (DRDY) pin polarity (“0” is active low, “1” is active high, default is “1” active high)
Bit 1	Interrupt Latch	Interrupt latching (“0” means non-latched - interrupt pin is on as long as the condition is fulfilled, “1” means latched - interrupt pin is on until interrupt status register 0x4A is read, default is “”1” latched)
Bit 0	Interrupt Polarity	Interrupt pin INT polarity selection (“1” – is active high, “0” is active low, default is “1” active high)

Register (0x4F) contains the Low-Threshold interrupt threshold setting. (Also refer to chapter 0 for the details of magnetometer interrupt operation and the threshold setting).

Table 21: Low-threshold interrupt threshold setting control register (0x4F)

(0x4F) Bit	Name	Description
Bit 7	LowThreshold <7>	Bit 7 of Low-Threshold interrupt threshold setting
Bit 6	LowThreshold <6>	Bit 6 of Low-Threshold interrupt threshold setting
Bit 5	LowThreshold <5>	Bit 5 of Low-Threshold interrupt threshold setting
Bit 4	LowThreshold <4>	Bit 4 of Low-Threshold interrupt threshold setting
Bit 3	LowThreshold <3>	Bit 3 of Low-Threshold interrupt threshold setting
Bit 2	LowThreshold <2>	Bit 2 of Low-Threshold interrupt threshold setting
Bit 1	LowThreshold <1>	Bit 1 of Low-Threshold interrupt threshold setting
Bit 0	LowThreshold <0>	Bit 0 of Low-Threshold interrupt threshold setting

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Register (0x50) contains the High-Threshold interrupt threshold setting. (Also refer to chapter 0 for the details of magnetometer interrupt operation and the threshold setting).

Table 22: High-threshold interrupt threshold setting control register (0x4F)

(0x50) Bit	Name	Description
Bit 7	HighThreshold <7>	Bit 7 of High-Threshold interrupt threshold setting
Bit 6	HighThreshold <6>	Bit 6 of High-Threshold interrupt threshold setting
Bit 5	HighThreshold <5>	Bit 5 of High-Threshold interrupt threshold setting
Bit 4	HighThreshold <4>	Bit 4 of High-Threshold interrupt threshold setting
Bit 3	HighThreshold <3>	Bit 3 of High-Threshold interrupt threshold setting
Bit 2	HighThreshold <2>	Bit 2 of High-Threshold interrupt threshold setting
Bit 1	HighThreshold <1>	Bit 1 of High-Threshold interrupt threshold setting
Bit 0	HighThreshold <0>	Bit 0 of High-Threshold interrupt threshold setting

5.8 Number of repetitions control registers

Register (0x51) contains the number of repetitions for x/y-axis. Table 24 below shows the number of repetitions resulting out of the register configuration. The performed number of repetitions nXY can be calculated from unsigned register value as nXY = 1+2xREPXY as shown below, where b7-b0 are the bits 7 to 0 of register 0x51:

$$nXY = 1 + 2 \cdot (b7 \cdot 2^7 + b6 \cdot 2^6 + b5 \cdot 2^5 + b4 \cdot 2^4 + b3 \cdot 2^3 + b2 \cdot 2^2 + b1 \cdot 2^1 + b0 \cdot 2^0)$$

$$= 1 + 2 \cdot (REPXY)$$

Table 23: X/y-axis repetitions control register (0x51)

(0x51) Bit	Name	Description
Bit 7	REPXY <7>	Bit 7 of number of repetitions (valid for XY)
Bit 6	REPXY <6>	Bit 6 of number of repetitions (valid for XY)
Bit 5	REPXY <5>	Bit 5 of number of repetitions (valid for XY)
Bit 4	REPXY <4>	Bit 4 of number of repetitions (valid for XY)
Bit 3	REPXY <3>	Bit 3 of number of repetitions (valid for XY)
Bit 2	REPXY <2>	Bit 2 of number of repetitions (valid for XY)
Bit 1	REPXY <1>	Bit 1 of number of repetitions (valid for XY)
Bit 0	REPXY <0>	Bit 0 of number of repetitions (valid for XY)

Table 24: Numbers of repetition for x/y-axis depending on value of register (0x51)

(0x51) **register value (binary)**	(0x51) **register value (hex)**	**Number of repetitions for x- and y-axis each**
00000000b	0x00h	1
00000001b	0x01h	3
00000010b	0x02h	5
00000011b	0x03h	7
…		…
11111111b	0xFFh	511

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Register (0x52) contains the number of repetitions for z-axis.
Table 26 below shows the number of repetitions resulting out of the register configuration. The performed number of repetitions nZ can be calculated from unsigned register value as nZ = 1+REPZ as shown below, where b7-b0 are the bits 7 to 0 of register 0x52:

$$nZ = 1 + (b7 \cdot 2^7 + b6 \cdot 2^6 + b5 \cdot 2^5 + b4 \cdot 2^4 + b3 \cdot 2^3 + b2 \cdot 2^2 + b1 \cdot 2^1 + b0 \cdot 2^0)$$

$$= 1 + REPZ$$

Table 25: Z-axis repetitions control register (0x52)

(0x52) Bit	Name	Description
Bit 7	REPZ <7>	Bit 7 of number of repetitions (valid for Z)
Bit 6	REPZ <6>	Bit 6 of number of repetitions (valid for Z)
Bit 5	REPZ <5>	Bit 5 of number of repetitions (valid for Z)
Bit 4	REPZ <4>	Bit 4 of number of repetitions (valid for Z)
Bit 3	REPZ <3>	Bit 3 of number of repetitions (valid for Z)
Bit 2	REPZ <2>	Bit 2 of number of repetitions (valid for Z)
Bit 1	REPZ <1>	Bit 1 of number of repetitions (valid for Z)
Bit 0	REPZ <0>	Bit 0 of number of repetitions (valid for Z)

Table 26: Numbers of repetition for z-axis depending on value of register (0x52)

(0x52) **register value (binary)**	(0x52) **register value (hex)**	**Number of repetitions for z-axis**
00000000b	0x00h	1
00000001b	0x01h	2
00000010b	0x02h	3
00000011b	0x03h	4
…		…
11111111b	0xFFh	256

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6. Digital interfaces

The BMM150 supports SPI and I²C digital interface protocols for communication as a slave with a host device.

The active interface is selected by the state of the “protocol select” pin (PS):
PS: “0” (“1”) selects SPI (I²C).

By default, SPI operates in the standard 4-wire configuration. It can be re-configured by software to work in 3-wire mode instead of standard 4-wire mode.

Both interfaces share the same pins. The mapping for each interface is given in the following table:

Table 27: Mapping of the interface pins

Pin#	Name	use w/ SPI	use w/ I²C	Description
C1	SDO	SDO	I²C address selection	SPI: Data Output (4-wire mode) I²C: Used to set LSB of I²C address
B4	SDI	SDI	SDA	SPI: Data Input (4-wire mode) Data Input / Output (3-wire mode) I²C: Serial Data
A5	CSB	CSB	I²C address selection	SPI: Chip Select (enable) I²C: Used to set bit1 of I²C address
A3	SCK	SCK	SCL	SPI: Serial Clock I²C: Serial Clock

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The following table shows the electrical specifications of the interface pins:

Table 28: Electrical specification of the interface pins

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Pull-up Resistance CSB	$R_{up, CSB}$	Internal Pull-up Resistance to VDDIO; deactivated in I²C mode	80	100	120	k :
Input Capacitance	C_{in}				10	pF
I²C Bus Load Capacitance (max. drive capability)	C_{I2C_Load}				400	pF

6.1 Serial peripheral interface (SPI)

The timing specification for SPI of the BMM150 is given in the following table:

Table 29: SPI timing for BMM150

Parameter	Symbol	Condition	Min	Max	Unit
Clock Frequency	f_{SPI}	Max. Load on SDI or SDO = 25pF		10	MHz
SCK Low Pulse	t_{SCKL}		20		ns
SCK High Pulse	t_{SCKH}		20		ns
SDI Setup Time	t_{SDI_setup}		20		ns
SDI Hold Time	t_{SDI_hold}		20		ns
SDO Output Delay	t_{SDO_OD}	Load = 25pF		30	ns
		Load = 250pF, V_{DDIO} = 2.4V		40	ns
CSB Setup Time	t_{CSB_setup}		20		ns
CSB Hold Time	t_{CSB_hold}		40		ns

The following figure shows the definition of the SPI timings given in Table 29:

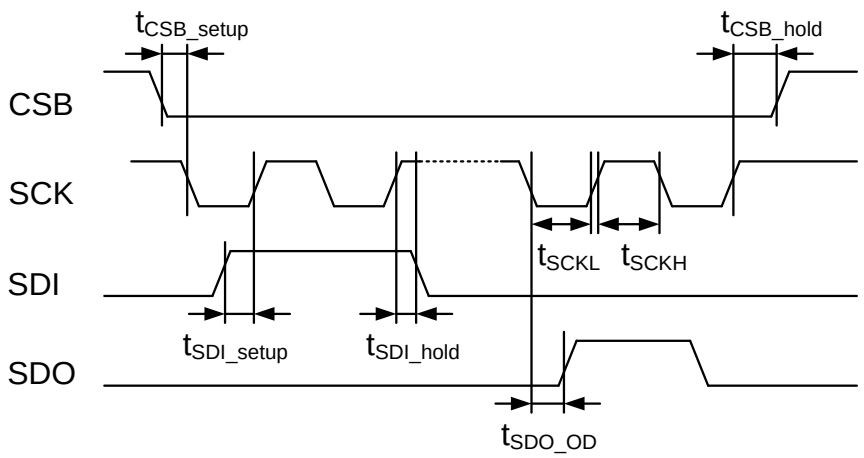

Figure 8: SPI timing diagram

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The SPI interface of the BMM150 is compatible with two modes, “00” and “11”. The automatic selection between [CPOL = “0” and CPHA = “0”] and [CPOL = “1” and CPHA = “1”] is done based on the value of SCK after a falling edge of CSB.

Two configurations of the SPI interface are supported by the BMM150: 4-wire and 3-wire. The same protocol is used by both configurations. The device operates in 4-wire configuration by default. It can be switched to 3-wire configuration by writing “1” to (0x4B) “SPI3en” after power control bit was set. Pin SDI is used as the common data pin in 3-wire configuration.
For single byte read as well as write operations, 16-bit protocols are used. The BMM150 also supports multiple-byte read operations.

In SPI 4-wire configuration CSB (chip select low active), SCK (serial clock), SDI (serial data input), and SDO (serial data output) pins are used. The communication starts when the CSB is pulled low by the SPI master and stops when CSB is pulled high. SCK is also controlled by SPI master. SDI and SDO are driven at the falling edge of SCK and should be captured at the rising edge of SCK.

The basic write operation waveform for 4-wire configuration is depicted in Figure 9. During the entire write cycle SDO remains in high- impedance state.

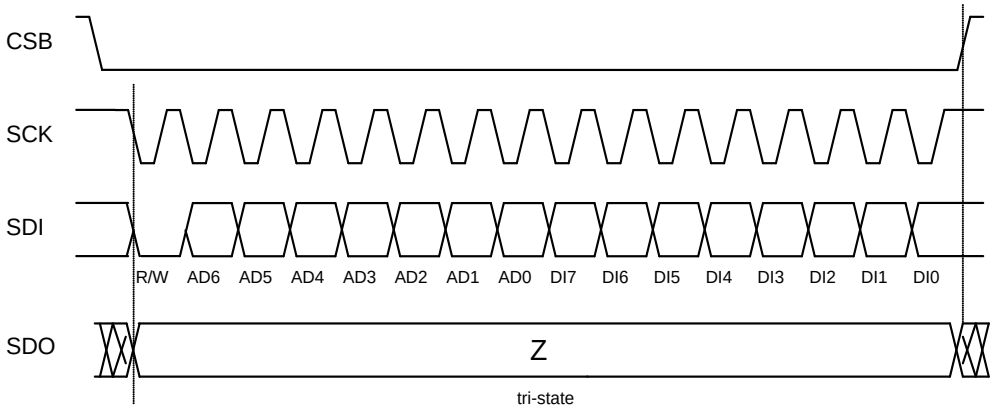

Figure 9: 4-wire basic SPI write sequence (mode “11”)

The basic read operation waveform for 4-wire configuration is depicted in Figure 10:

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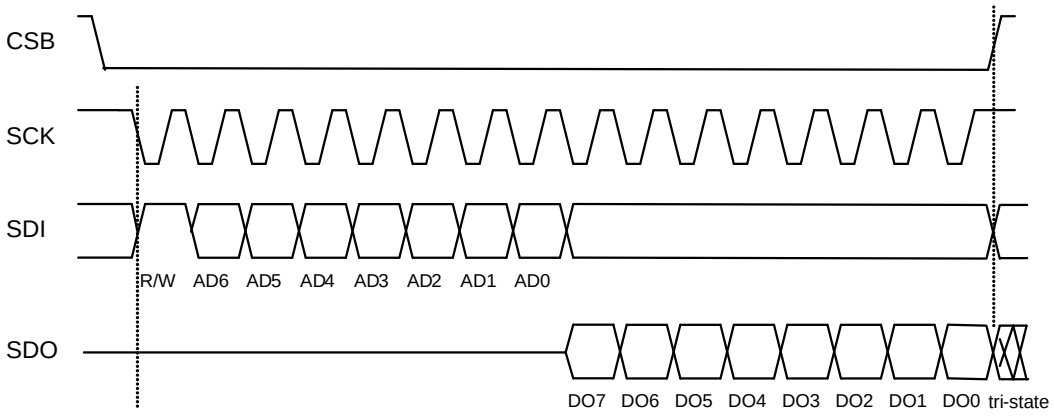

Figure 10: 4-wire basic SPI read sequence (mode “11”)

The data bits are used as follows:

Bit0: Read/Write bit. When 0, the data SDI is written into the chip. When 1, the data SDO from the chip is read.

Bit1-7: Address AD(6:0).

Bit8-15: when in write mode, these are the data SDI, which will be written into the address. When in read mode, these are the data SDO, which are read from the address.

Multiple read operations are possible by keeping CSB low and continuing the data transfer. Only the first register address has to be written. Addresses are automatically incremented after each read access as long as CSB stays active low.

The principle of multiple read is shown in Figure 11:

	Control byte		Data byte	Data byte	Data byte	
Start	RW	Register adress (02h)	Data register - adress 02h	Data register - adress 03h	Data register - adress 04h	Stop
CSB = 0	1	0 0 0 0 0 1 0	X X X X X X X X	X X X X X X X X	X X X X X X X X	CSB = 1

Figure 11: SPI multiple read

In SPI 3-wire configuration CSB (chip select low active), SCK (serial clock), and SDI (serial data input and output) pins are used. The communication starts when the CSB is pulled low by the SPI master and stops when CSB is pulled high. SCK is also controlled by SPI master. SDI is driven (when used as input of the device) at the falling edge of SCK and should be captured (when used as the output of the device) at the rising edge of SCK.

The protocol as such is the same in 3-wire configuration as it is in 4-wire configuration. The basic operation waveform (read or write access) for 3-wire configuration is depicted in Figure 12:

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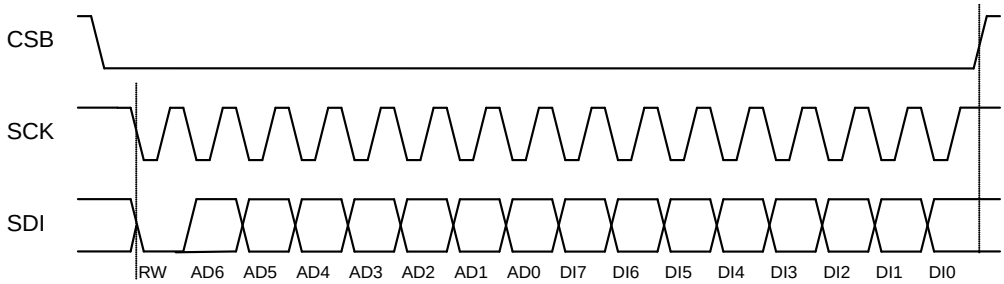

Figure 12: 3-wire basic SPI read or write sequence (mode “11”)

6.2 Inter-Integrated Circuit (I²C)

The I²C bus uses SCL (= SCK pin, serial clock) and SDA (= SDI pin, serial data input and output) signal lines. Both lines are connected to V_{DDIO} externally via pull-up resistors so that they are pulled high when the bus is free.

The I²C interface of the BMM150 is compatible with the I²C Specification UM10204 Rev. 03 (19 June 2007), available at http://www.nxp.com. The BMM150 supports I²C standard mode and fast mode, only 7-bit address mode is supported.

The default I²C address of the BMM150 is 0x10. The five MSB are hardwired to “00100”. In order to prevent bus conflicts bit0 can be inverted by setting ‘1’ to SDO, and the bit 1 can be inverted by setting ‘1’ to the CSB line according to below Table:

Table 30: BMM150 I²C addresses

CSB pin	SDO pin	I²C address
GND	GND	0x10
GND	VDDIO	0x11
VDDIO	GND	0x12
VDDIO	VDDIO	0x13

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The timing specification for I²C of the BMM150 is given in Table 31:

Table 31: I²C timings[7].

Parameter	Symbol	Condition	Min	Max	Unit
Clock Frequency	f_{SCL}			400	kHz
SCL Low Period	t_{LOW}		1.3		µs
SCL High Period	t_{HIGH}		0.6		
SDA Setup Time	t_{SUDAT}		0.1		
SDA Hold Time	t_{HDDAT}		0		
Setup Time for a repeated Start Condition	t_{SUSTA}		0.6		
Hold Time for a Start Condition	t_{HDSTA}		0.6		
Setup Time for a Stop Condition	t_{SUSTO}		0.6		
Time before a new Transmission can start	t_{BUF}		1.3		

[7] fully compliant to the I²C specification"UM10204 I²C-bus specification Rev.03 – 19 June 2007"

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Figure 13 the definition of the I²C timings given in Table 31:

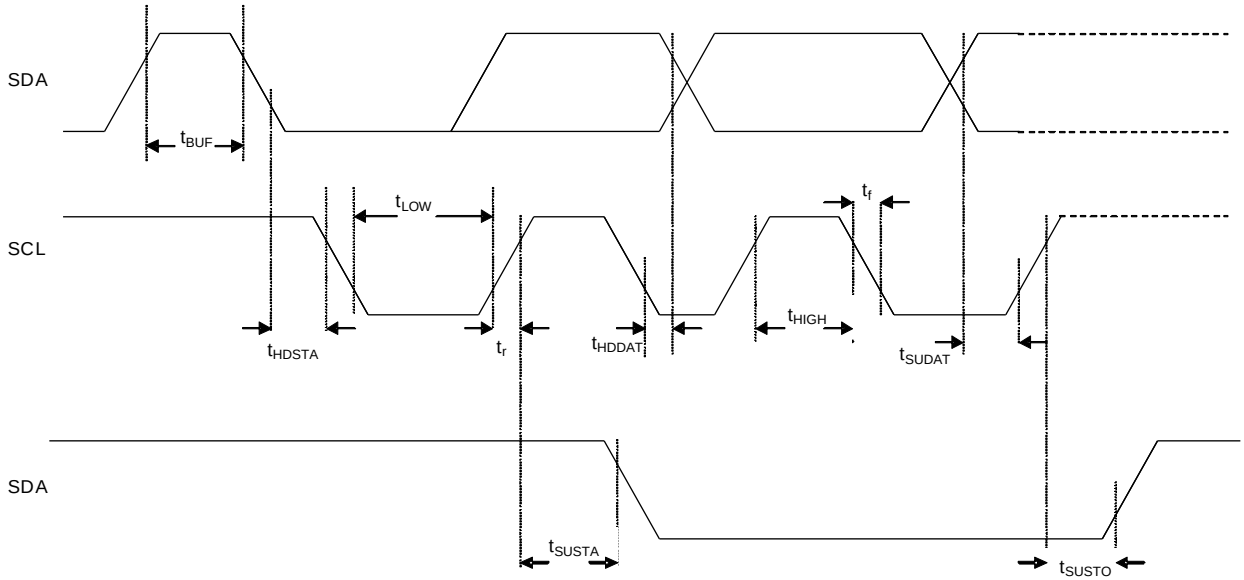

Figure 13: I²C timing diagram

The I²C protocol works as follows:

START: Data transmission on the bus begins with a high to low transition on the SDA line while SCL is held high (start condition (S) indicated by I²C bus master). Once the START signal is transferred by the master, the bus is considered busy.

STOP: Each data transfer should be terminated by a Stop signal (P) generated by master. The STOP condition is a low to HIGH transition on SDA line while SCL is held high.

ACK: Each byte of data transferred must be acknowledged. It is indicated by an acknowledge bit sent by the receiver. The transmitter must release the SDA line (no pull down) during the acknowledge pulse while the receiver must then pull the SDA line low so that it remains stable low during the high period of the acknowledge clock cycle.

In the following diagrams these abbreviations are used:

S	Start
P	Stop
ACKS	Acknowledge by slave
ACKM	Acknowledge by master
NACKM	Not acknowledge by master
RW	Read / Write

A START immediately followed by a STOP (without SCK toggling from logic “1” to logic “0”) is not supported. If such a combination occurs, the STOP is not recognized by the device.

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I²C write access:
I²C write access can be used to write a data byte in one sequence.

The sequence begins with start condition generated by the master, followed by 7 bits slave address and a write bit (RW = 0). The slave sends an acknowledge bit (ACK = 0) and releases the bus. Then the master sends the one byte register address. The slave again acknowledges the transmission and waits for the 8 bits of data which shall be written to the specified register address. After the slave acknowledges the data byte, the master generates a stop signal and terminates the writing protocol.

Example of an I²C write access:

										Control byte									Data byte									
Start	Slave Adress								RW	ACKS	Register adress (0x10)								ACKS	Data (0x09)								ACKS	Stop
S	0	0	1	0	0	0	0	0			0	0	0	1	0	0	0	0		X	X	X	X	X	X	X	X		P

Figure 14: Example of an I²C write access

I²C read access:
I²C read access also can be used to read one or multiple data bytes in one sequence.

A read sequence consists of a one-byte I²C write phase followed by the I²C read phase. The two parts of the transmission must be separated by a repeated start condition (Sr). The I²C write phase addresses the slave and sends the register address to be read. After slave acknowledges the transmission, the master generates again a start condition and sends the slave address together with a read bit (RW = 1). Then the master releases the bus and waits for the data bytes to be read out from slave. After each data byte the master has to generate an acknowledge bit (ACK = 0) to enable further data transfer. A NACKM (ACK = 1) from the master stops the data being transferred from the slave. The slave releases the bus so that the master can generate a STOP condition and terminate the transmission.
The register address is automatically incremented and, therefore, more than one byte can be sequentially read out. Once a new data read transmission starts, the start address will be set to the register address specified in the latest I²C write command. By default the start address is set at 0x00. In this way repetitive multi-bytes reads from the same starting address are possible.

In order to prevent the I²C slave of the device to lock-up the I²C bus, a watchdog timer (WDT) is implemented in the BMM150. The WDT observes internal I²C signals and resets the I²C interface if the bus is locked-up. The activity and the timer period of the WDT is predefined with a default time period of 50 ms by factory trimming.

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Example of an I²C multiple read accesses:

														Control byte																		
Start	Slave Adress							RW	ACKS	dummy	Register adress (0x02)							ACKS	Stop													
S	0	0	1	0	0	0	0	0		X	0	0	0	0	0	1	0		P													
														Data byte									Data byte									
Start	Slave Adress							RW	ACKS	Read Data (0x02)								ACKM	Read Data (0x03)								ACKM					
Sr	0	0	1	0	0	0	0	1		X	X	X	X	X	X	X	X		X	X	X	X	X	X	X	X		…				
														Data byte									Data byte									
														Read Data (0x04)				ACKM	Read Data (0x05)								ACKM					
										…	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		…				
														Data byte									Data byte									
														Read Data (0x06)				ACKM	Read Data (0x07)								NACK	Stop				
										…	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		P				

Figure 15: Example of an I²C multiple read access

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7. Pin-out and connection diagram

7.1 Pin-out

Figure 16 depicts the bump association. The arrows indicate the A1 marking.

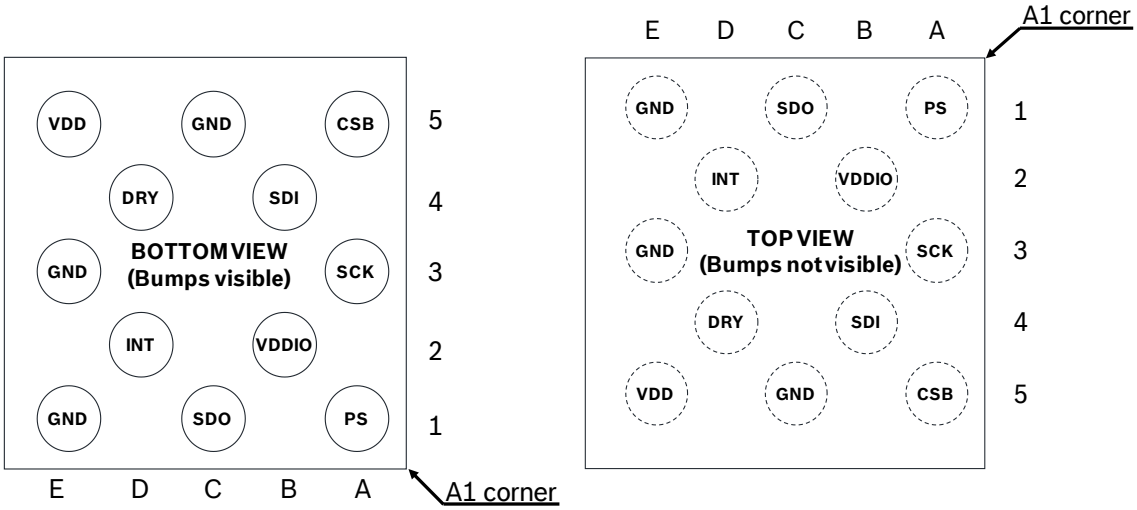

Figure 16: Pin-out bottom view, Pin-out top view

Table 32: Pin description

Pin	Name	I/O Type	Description	Connect to		
				SPI 4W	SPI 3W	I²C
A1	PS	In	Protocol select	GND	GND	V_{DDIO}
D2	INT	Out	Interrupt output	INT input or DNC if unused		
A5	CSB	In	Chip Select	CSB	CSB	GND for default address
C5	GND	Supply	Ground	GND		
E1	GND	Supply	Ground	GND		
D4	DRDY	Out	Data ready	DRDY input or DNC if unused		
C1	SDO	Out	SPI: Data out	SDO / MISO	DNC (float)	GND for default address
B4	SDI	In/Out	SPI: Data, I²C: Data	SDI / MOSI	SDI/SDO	SDA
E3	GND	Supply	Ground	GND		
E5	VDD	Supply	Supply voltage	V_{DD}		
B2	VDDIO	Supply	I/O voltage	V_{DDIO}		
A3	SCK	In	Serial clock	SCK	SCK	SCL

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7.2 Connection diagram 4-wire SPI

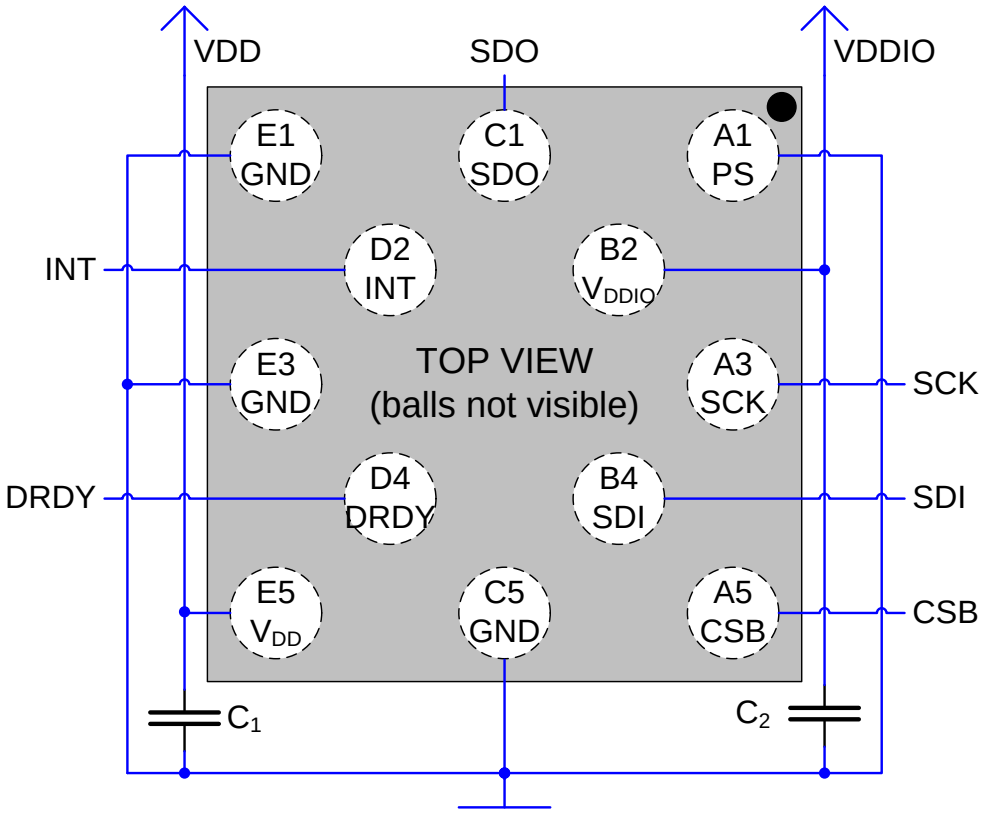

Figure 17: 4-wire SPI connection diagram

Note: The recommended value for C_1, C_2 is 100 nF.

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7.3 Connection diagram 3-wire SPI

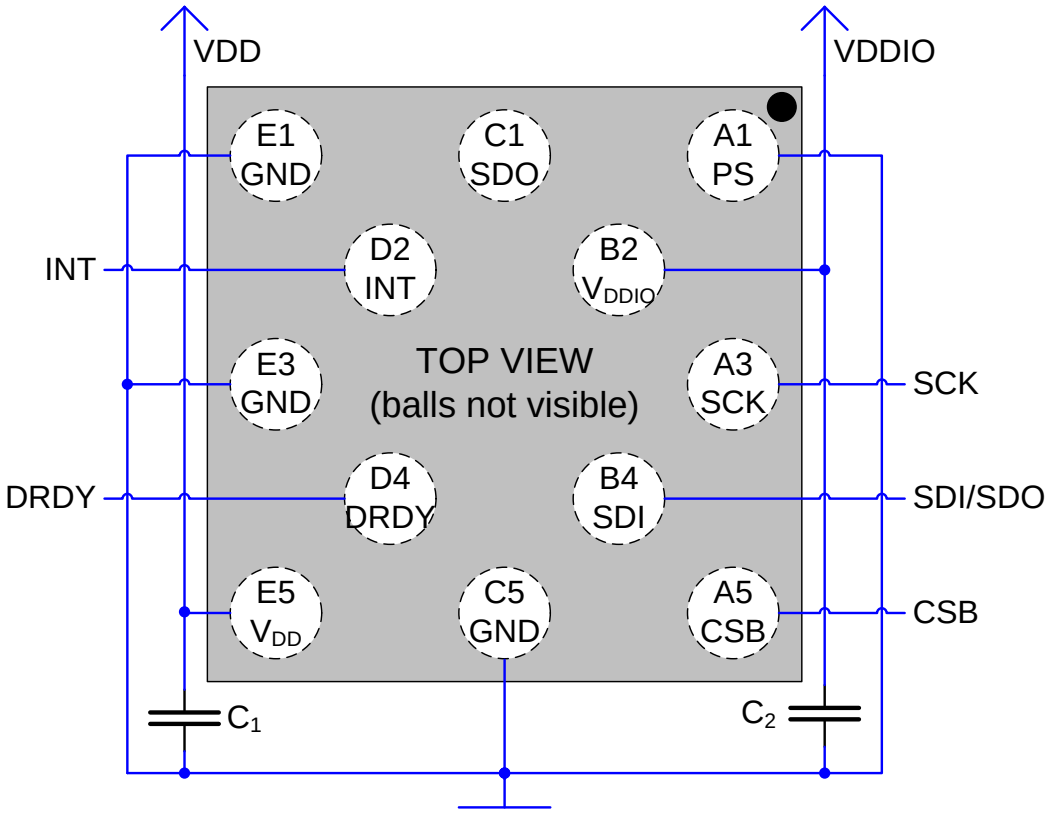

Figure 18: 3-wire SPI connection diagram

Note: The recommended value for C_1, C_2 is 100 nF.

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7.4 Connection diagram I²C

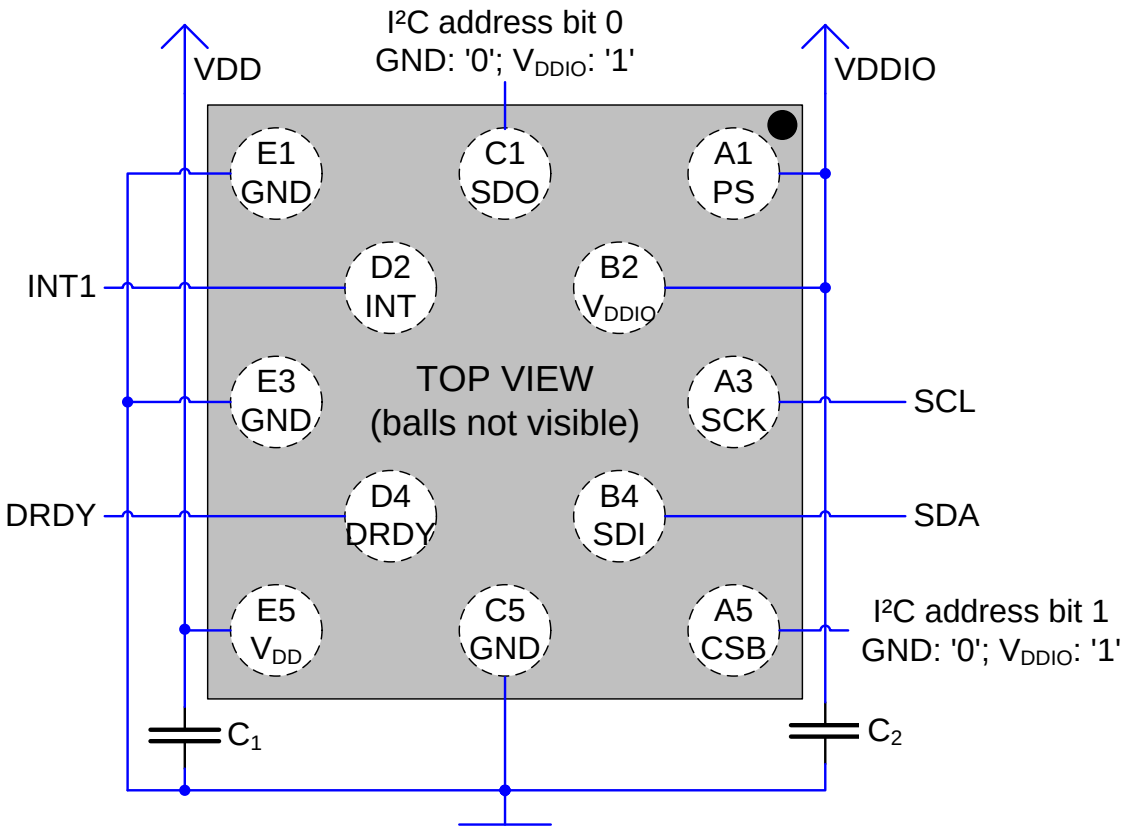

Figure 19: I²C connection diagram

Note:
The recommended value for C_1, C_2 is 100 nF.

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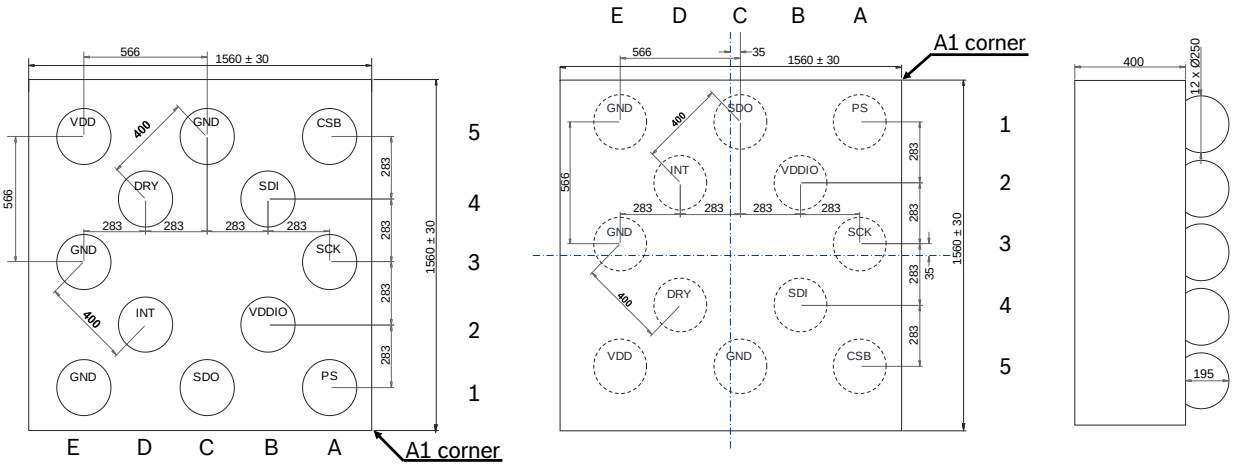
8. Package

8.1 Outline dimensions

The sensor housing is 12 pin chip scale wafer level package (1.56 × 1.56 × 0.6 mm³). Its dimensions are the following:



Bottom view (Bumps visible) **TOP view (Bumps not visible)** **Side view**

Figure 20: Package outline dimensions in µm

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8.2 Sensing axes orientation

The orientation of the device axes with respect to the applied field is shown in Figure 21. A remapping of the axes orientation is possible via API.

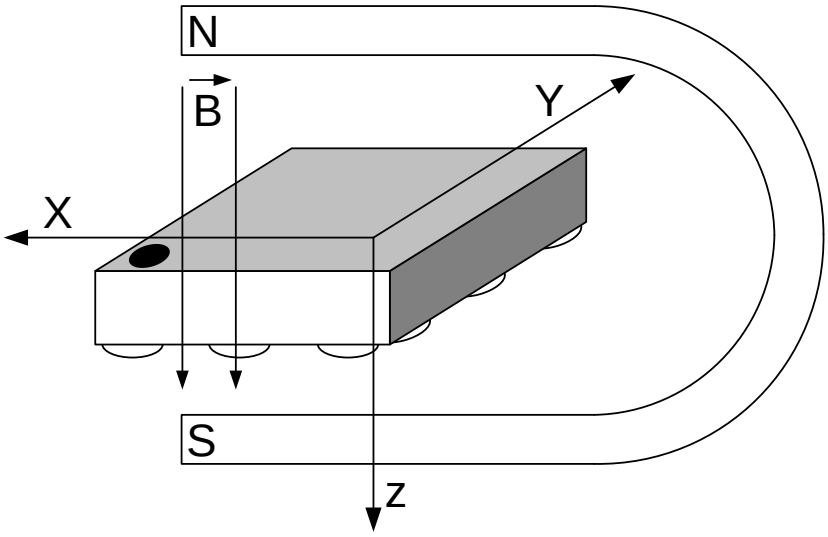
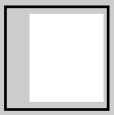
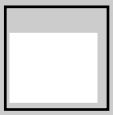
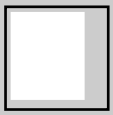
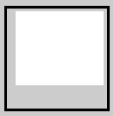
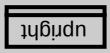


Figure 21: Orientation of sensing axes

Please note that the planet's north pole is a magnetic south pole. This means that when the BMM150's X axis points towards the north pole, the measured field will be positive.

Table 33: Output signals depending on sensor orientation

magnetic vector È						
Output Signal X	0 µT	-|B| µT	0 µT	+|B| µT	0 µT	0 µT
Output Signal Y	-|B| µT	0 µT	+|B| µT	0 µT	0 µT	0 µT
Output Signal Z	0 µT	0 µT	0 µT	0 µT	+|B| µT	-|B| µT

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8.3 Android axes orientation

The Android coordinate system is shown in Figure 22. The origin is in the lower-left corner with respect to the screen, with the X axis horizontal and pointing right, the Y axis vertical and pointing up and the Z axis pointing outside the front face of the screen. In this system, coordinates behind the screen have negative Z values.

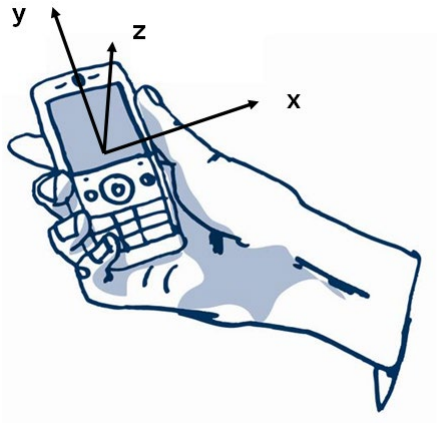

Figure 22: Android coordinate system

Attitude terms are defined in the following way (see Figure 23):

- Heading / Azimuth – angle between the magnetic north direction and the Y axis, around the Z axis (0° to 360°). 0° = North, 90° = East, 180° = South, 270° = West.
- Pitch – rotation around X axis (-180° to 180°), with positive values when the z-axis moves toward the y-axis.
- Roll – rotation around Y axis (-90° to 90°), with positive values when the x-axis moves toward the z-axis.

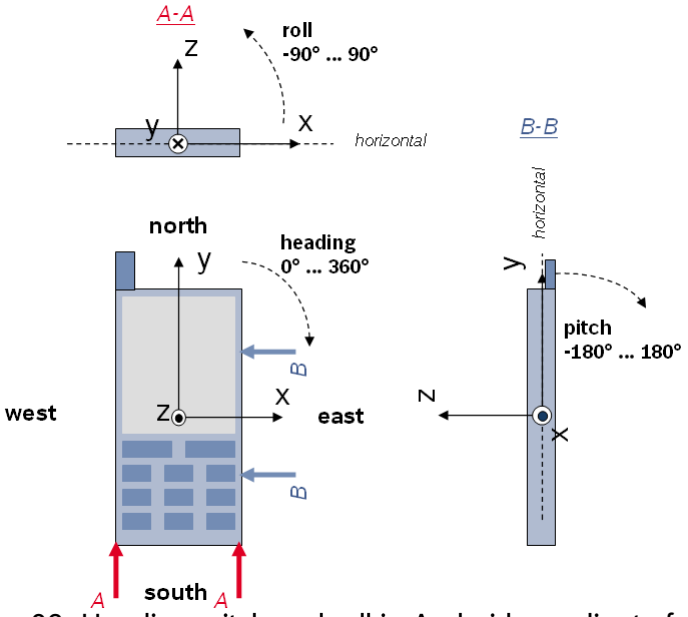

Figure 23: Heading, pitch and roll in Android coordinate frame

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