MIMXRT1170-EVK

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Revision History

Rev. Code	Date	By	Description
X1	2019-02-30	Shawn Shi	Draft version
A	2019-03-15	Shawn Shi	Initial release
B	2019-06-30	Shawn Shi	1.Swap BT_PCM_TXD_1V8 and BT_PCM_RXD_1V8. 2.Correct FREELINK JTAG_TDI_L signal. 3.Add POR_B for OCT Flash. 4.Add stand-off for M.2. 5.Refine the BOM for lower cost,
B1	2019-09-06	Shawn Shi	No Layout change compared to REVB, only BOM update: 1.Populate C91,C66,R102, DNP R1872~R1879. 2.DNP C56, DNP R101, DNP R408, DNP R404.
B2	2020-03-06	Shawn Shi	No Layout change compared to REVB, only BOM update : 1.DNP U16.
C	2020-05-08	Shawn Shi	1.Exchange BT_RST# and SD_PWREN_B. 2. Multiplex AUD_INT to GPIO_AD_06. 3.Change RGMII PHY IO to external power. 4.Add Optional External Reset Circuit and EMV L1 test interface. 5.Add 100 ohm DNP on MIPI DSI for compliance test. 6.Exchange PINMUX between ENET_RGMII_MDC/ENET_RGMII_MDIO and ENET_MDC/ENET_MDIO. 7.Add interface for Cortex Debug + ETM Trace. 8.Add I2S audio port on ARDUINO interface reserved pins. 9.Replace the SIM card socket with detection fucntion. 10. DNP board level 1DX wifi module. 11. Multiplexed SD1_CD_B to GPIO_AD_32 instead of GPIO_AD_03.
C1	2020-07-24	Shawn Shi	No Layout change compared to REVC, only BOM update: 1.Change C346 from 100nF to 100pF. 2.Change R368 from DNP 10K ohm to populate 100K ohm. 3.DNP R136 and default to use SD CD/DAT3 for card detection.
C2	2020-12-02	Shawn Shi	No Layout change compared to REVC, only BOM update: 1. DNP Nand Flash U14 (MX30LF2GE8AB-XKI) 2. DNP R1821
C3	2020-12-02	Albert Li	No Layout change compared to REVC, only BOM update: 1. DNP C66

1. Unless Otherwise Specified:

   All resistors are in ohms, 1/16 Watt,0402
   All capacitors are in uF,0402
   All voltages are DC
   All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: CP: IUO: PUBI:

Designer: Shawn Shi	Drawing Title: MIMXRT1170-EVK	
Drawn by: Shawn Shi	Page Title: COVER	
Approved: Yes	Size C	Document Number SCH-32171, PDF: SPF-32171 Rev C3
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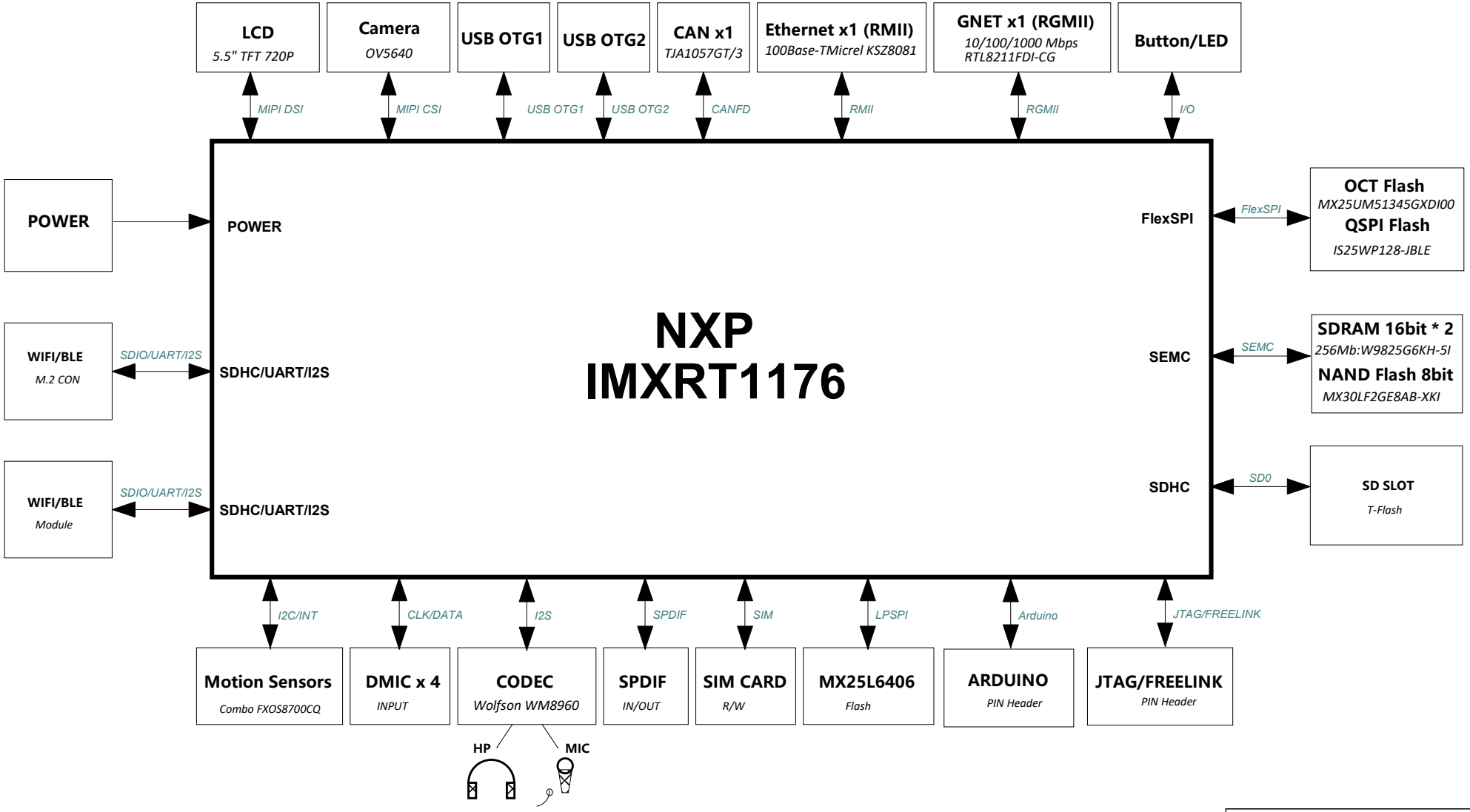
MIMXRT1170-EVK

Block Diagram Rev C3



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Page Title:	BLOCK DIAGRAM	
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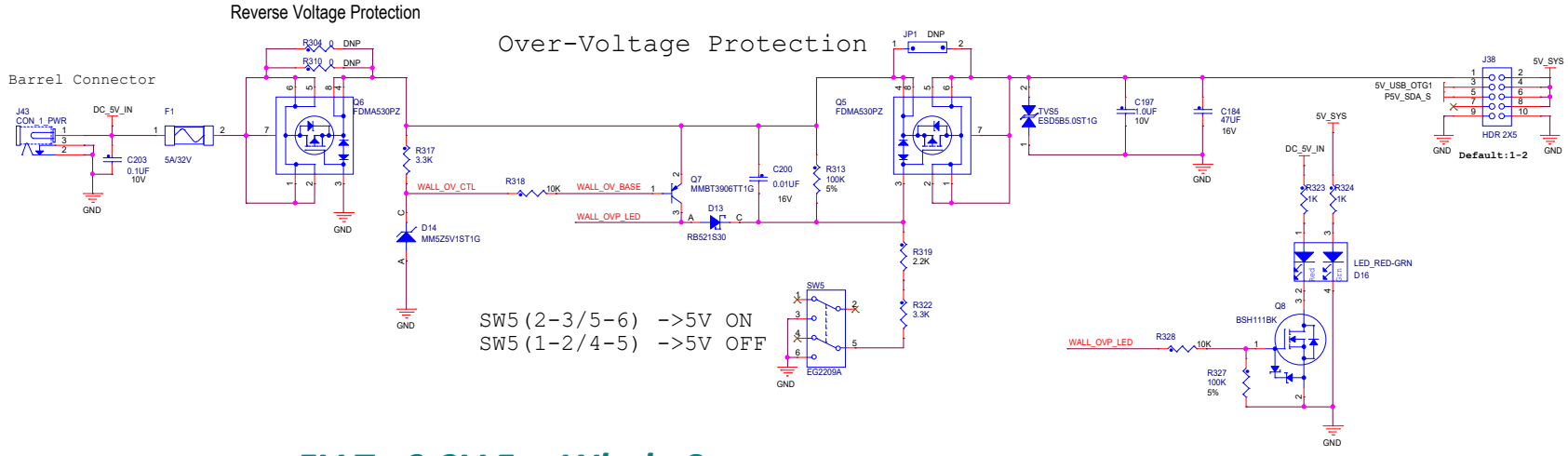
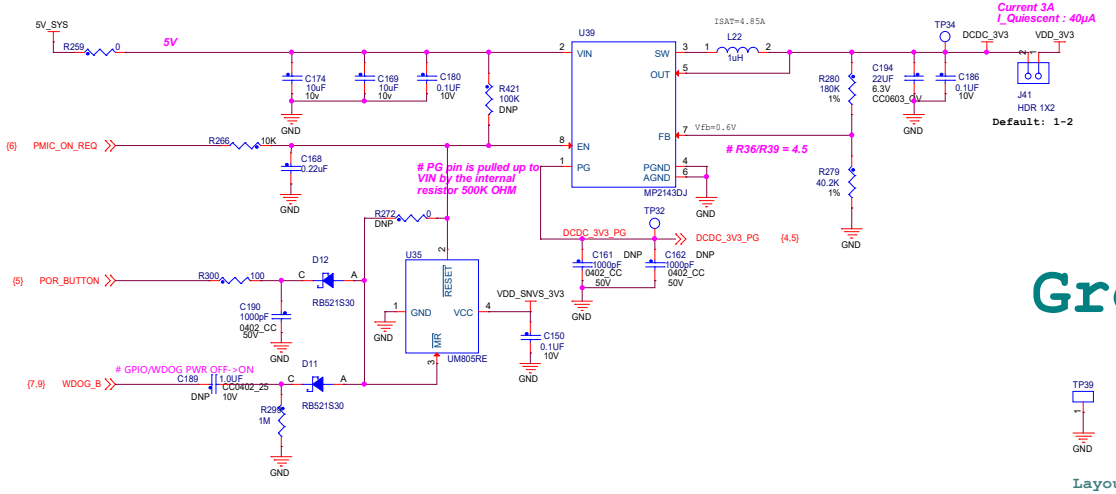
Main Power



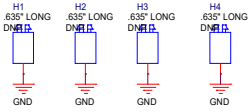
5V To 3.3V For Whole System



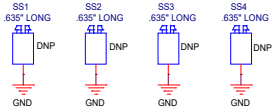
Ground TPs

Layout Note: Place Ground TPs to assist signal measurement.

Board Mounting Holes



LCD Mounting Holes



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Page Title: **MAIN POWER**

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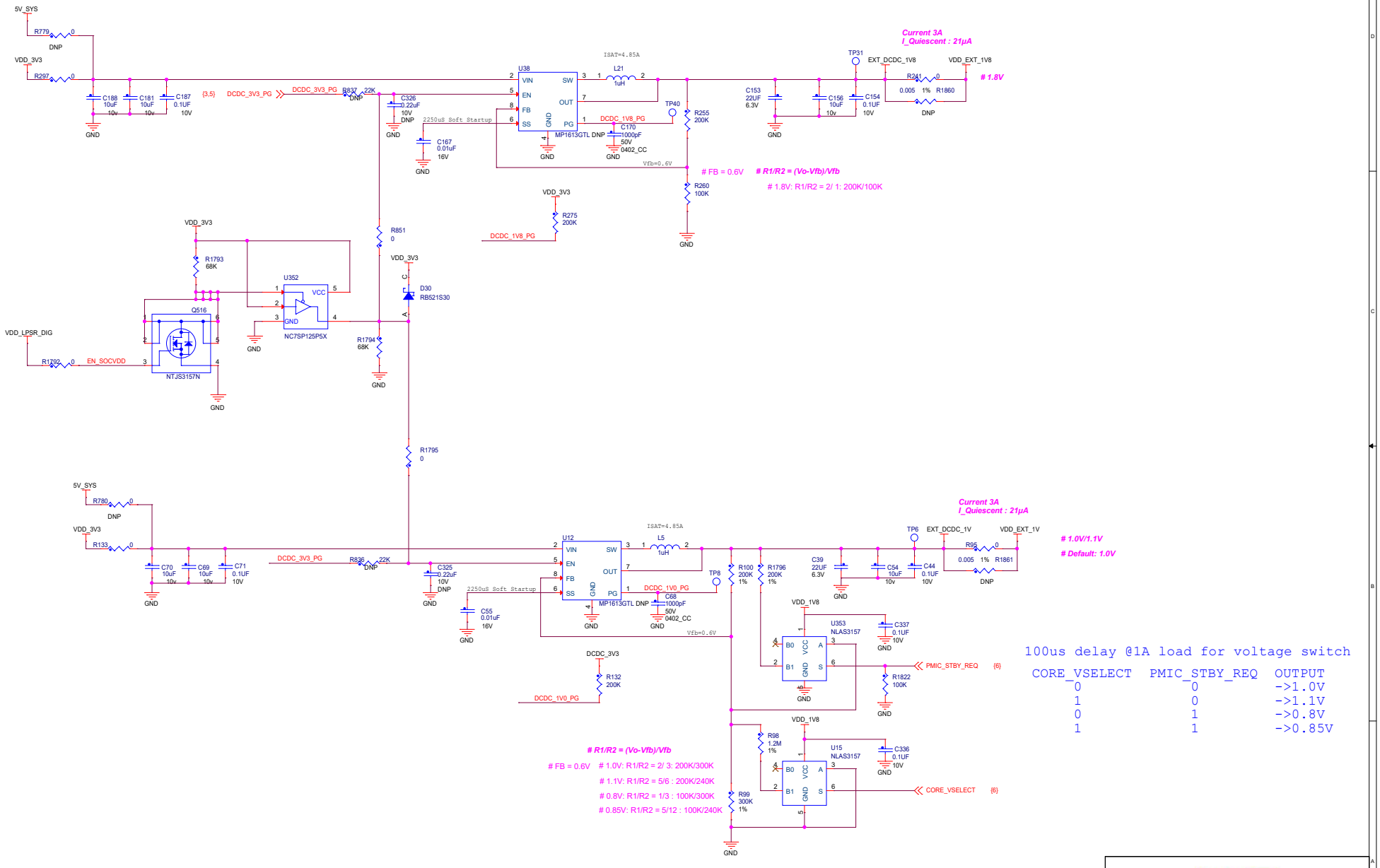
External DC/DC Reserved



100us delay @1A load for voltage switch

CORE_VSELECT	PMIC_STBY_REQ	OUTPUT
0	0	->1.0V
1	0	->1.1V
0	1	->0.8V
1	1	->0.85V

ICAP Classification: CP: ___ IUO: PUBI: ___

Drawing Title: **MIMXRT1170-EVK**

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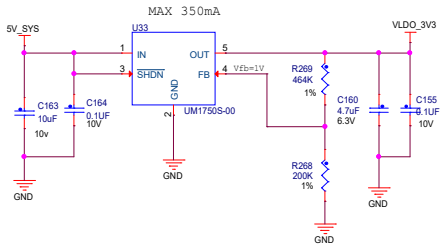
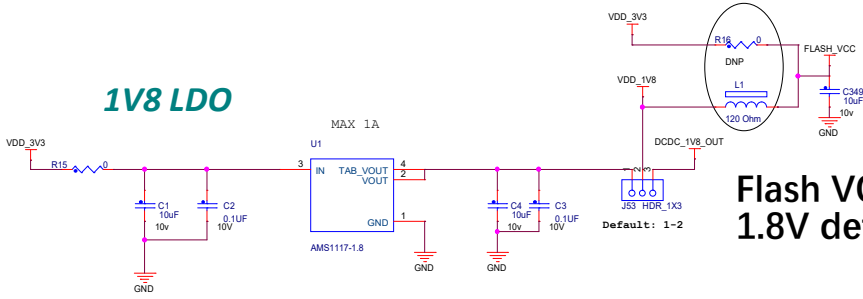
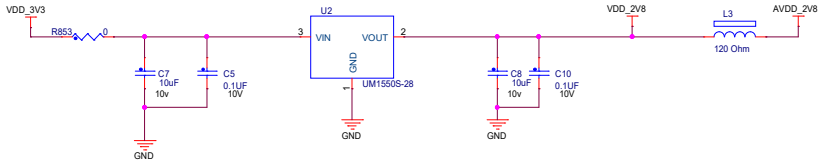
3V3 LDO for SNVS



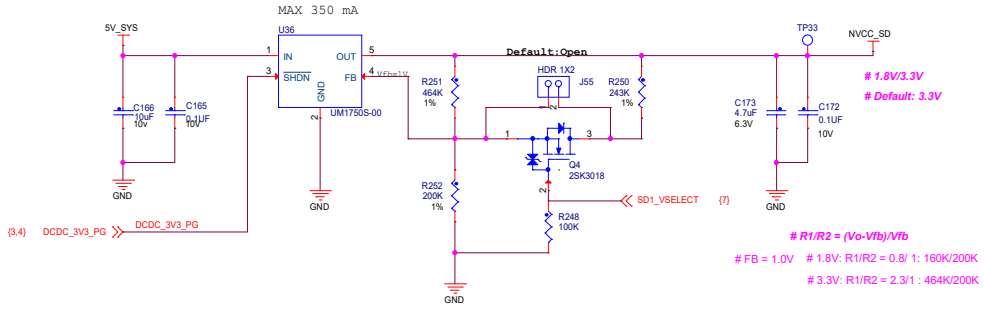
1V8 LDO



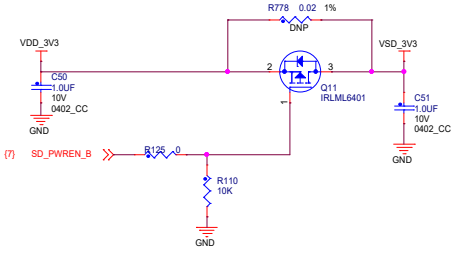
2V8 LDO



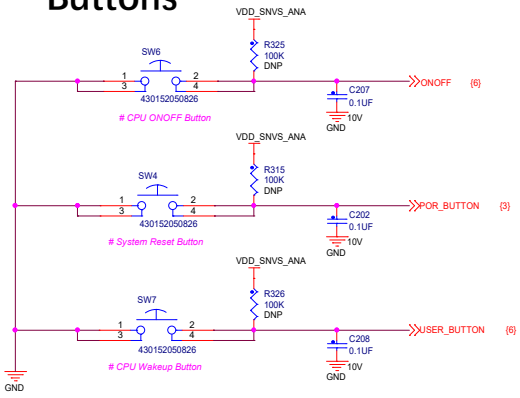
NVCC_SD <SD3.0>



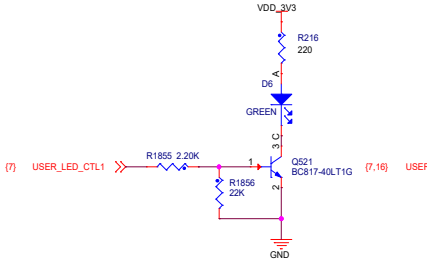
SD Card Power Switch



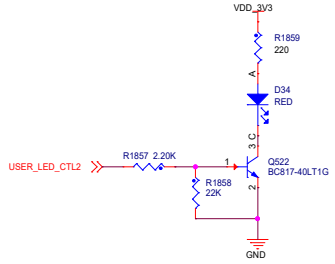
Buttons



USER LED1



USER LED2



Flash VCC Option
1.8V default

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Drawing Title: **MIMXRT1170-EVK**

Page Title: **POWER DOMAIN**

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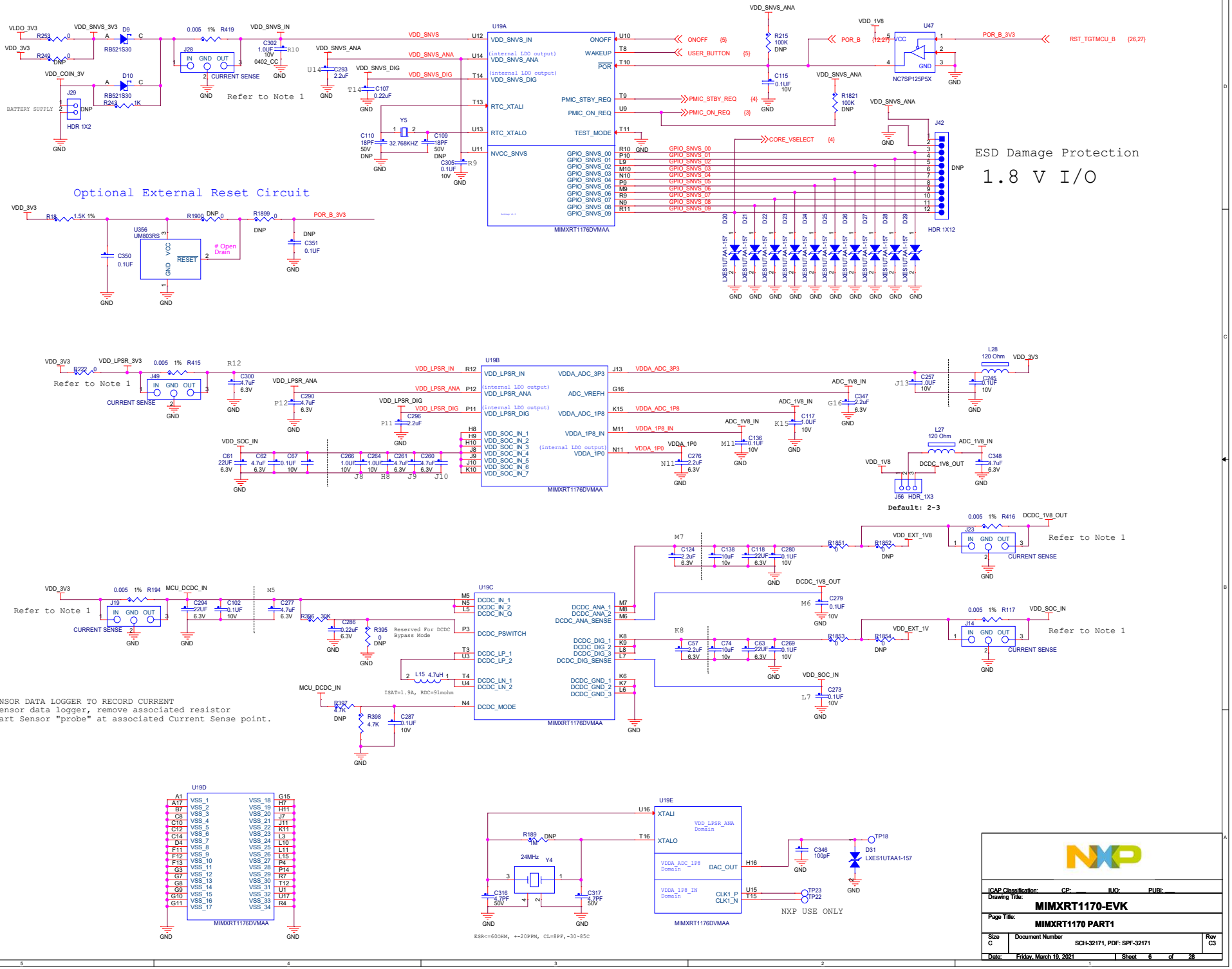
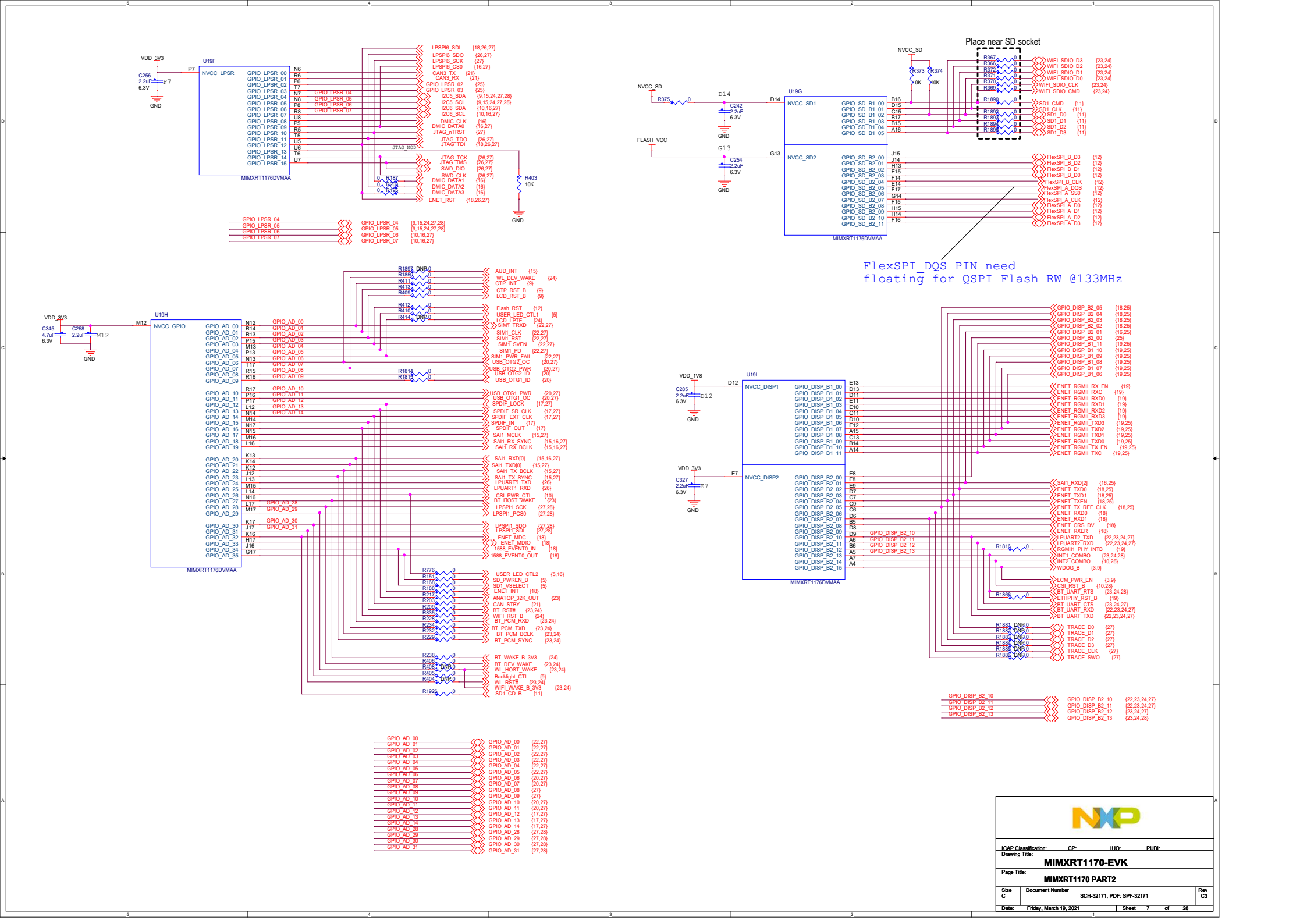

ESD Damage Protection
1.8 V I/O
Optional External Reset Circuit
Refer to Note 1
Default: 2-3
Note 1
USING SMART SENSOR DATA LOGGER TO RECORD CURRENT
To use Smart Sensor data logger, remove associated resistor
and install Smart Sensor "probe" at associated Current Sense point.
NXP USE ONLY
MIMXRT1170-EVK
MIMXRT1170 PART1
SCH-32171, PDF: SPF-32171
Friday, March 19, 2021


Place near SD socket
FlexSPI_DQS PIN need
floating for QSPI Flash RW @133MHz
MIMXRT1176DVMAA
ICAP Classification:
CP:
IUO:
PUBI:
Drawing Title:
MIMXRT1170-EVK
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MIMXRT1170 PART2
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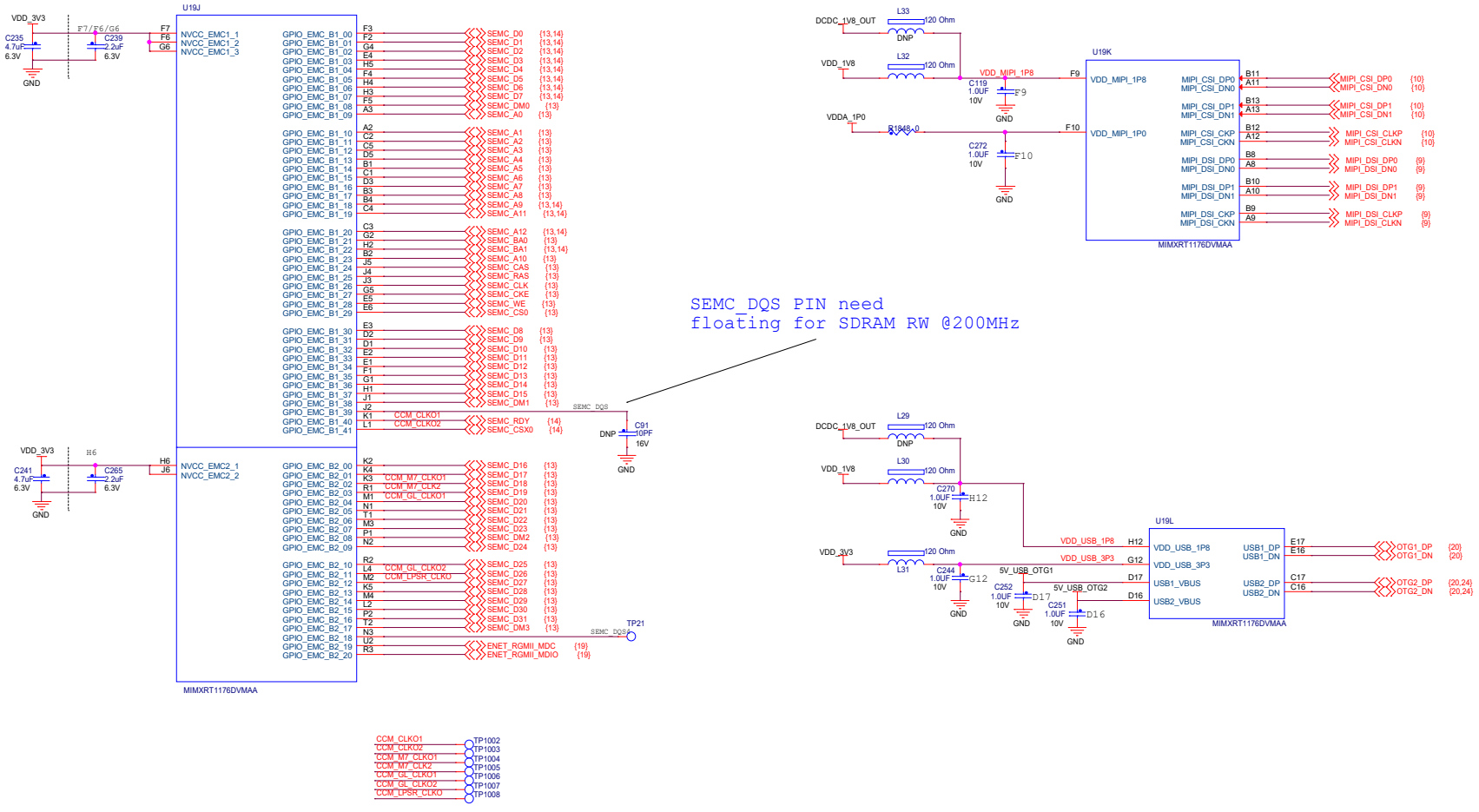

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Drawing Title: **MIMXRT1170-EVK**

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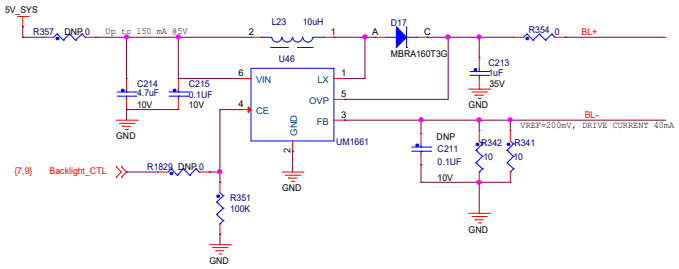
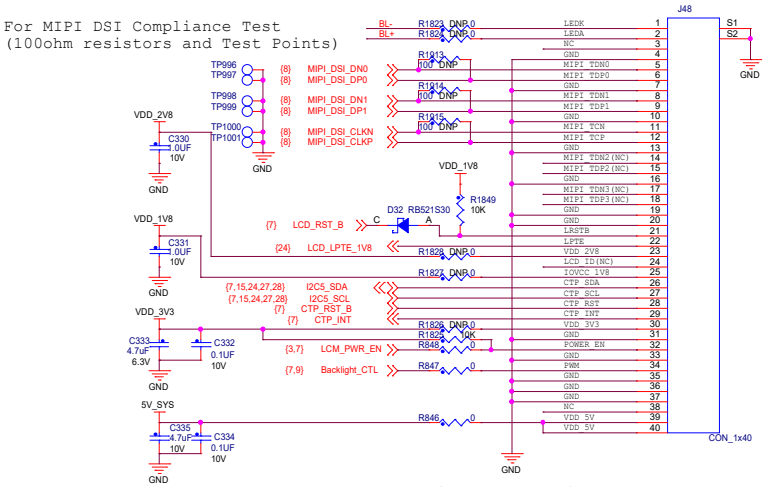
Backlight Control



LCD P/N From Rocktech:
RK055AHD091-CTG(720P) -- Default
RK055IQH091-CTG(540*960) -- Optional



I2C ADD: 0X28/0X29 or 0XBA/0XBB

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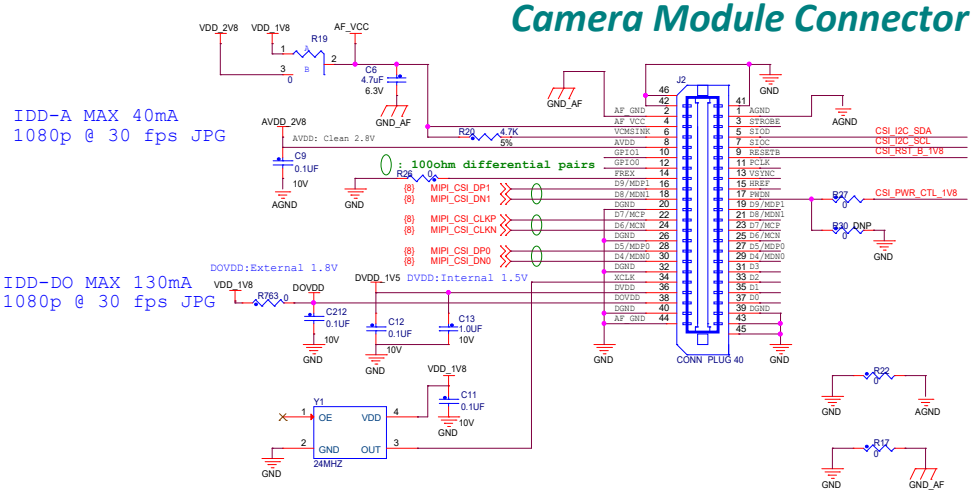
Wuxi A-KERR Science & Technology

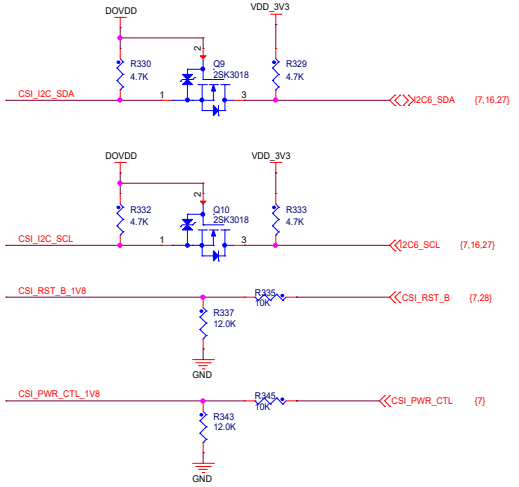
Camera# OV5640

Camera Module Connector

IDD-A MAX 40mA
1080p @ 30 fps JPG

IDD-DO MAX 130mA
1080p @ 30 fps JPG





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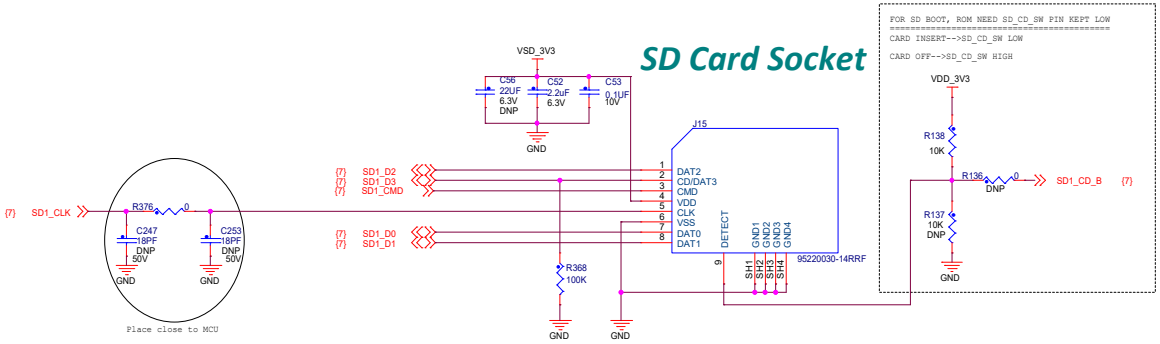

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Drawing Title:	MIMXRT1170-EVK	
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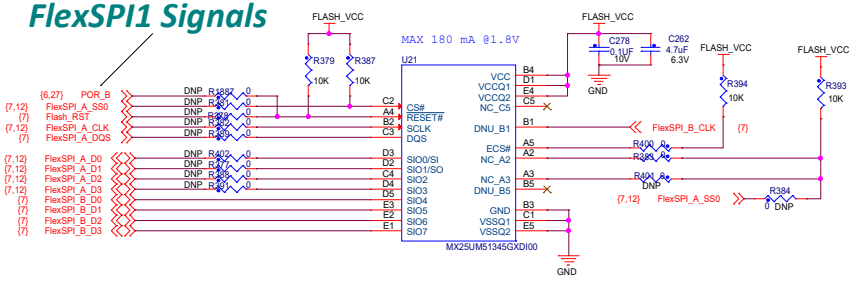
QSPI Flash as default Through FlexSPI1

OPTION1: USE QSPI FLASH(Mount R380/R399/ R386/R390/R392/R385,DNP R381/R378/R382/R389/R402/R377/R388/R391)
OPTION2: USE Octal Flash(Mount R381/R378/R382/R389/R402/R377/R388/R391, DNP R380/R399/R386/R390/R392/R385)

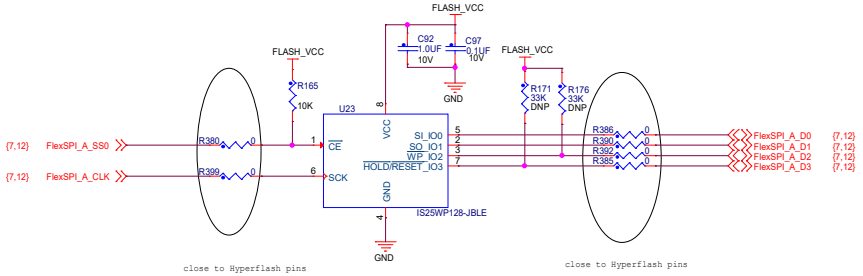
FlexSPI1 Signals

1V8 Octal Flash



Share the same package with S27KS0641DPBHI023
(if HYPERRAM is used, DNP R383/R400,Mount R401/R384)

1V8 QSPI Flash



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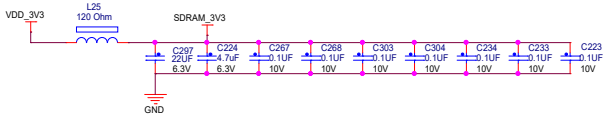
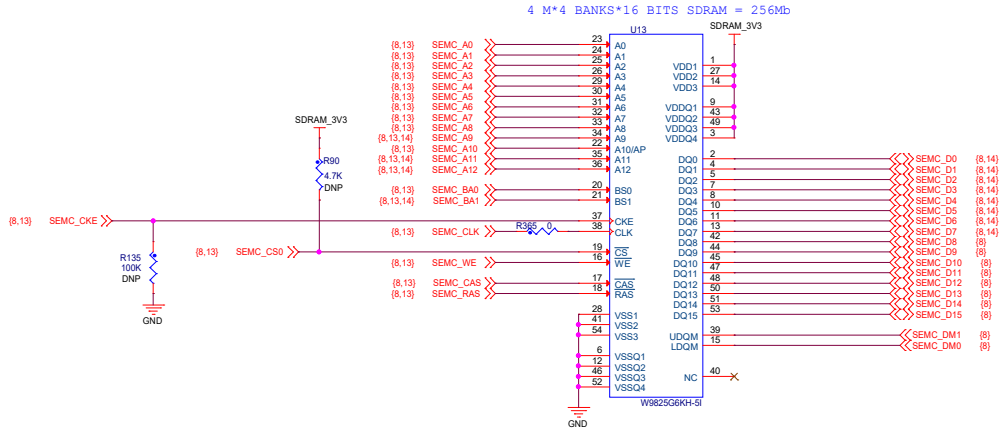
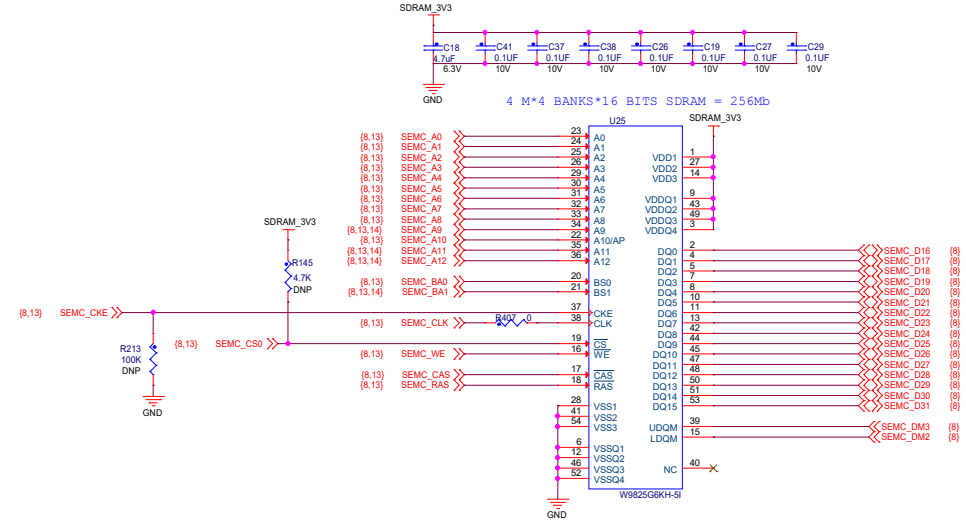


SDRAM





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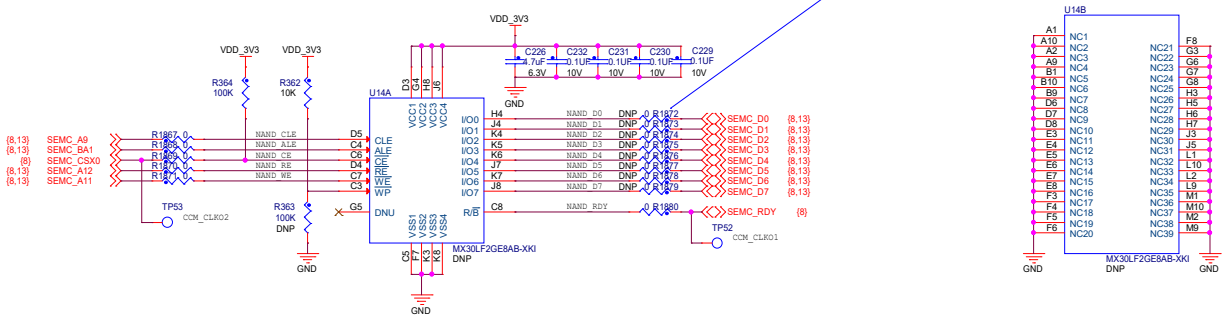
NAND FLASH

Populate R1872~R1879 to use NANDFlash



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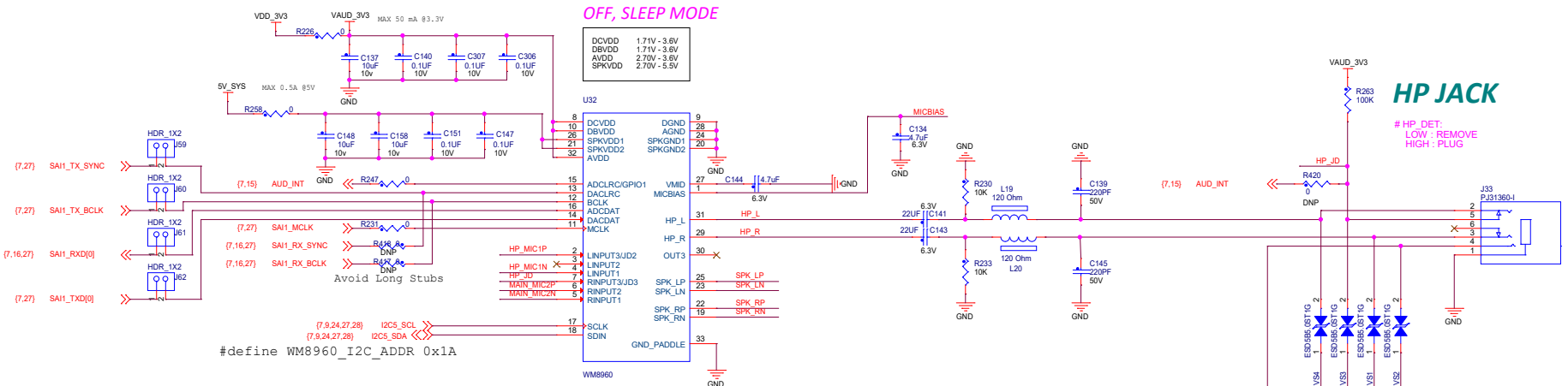

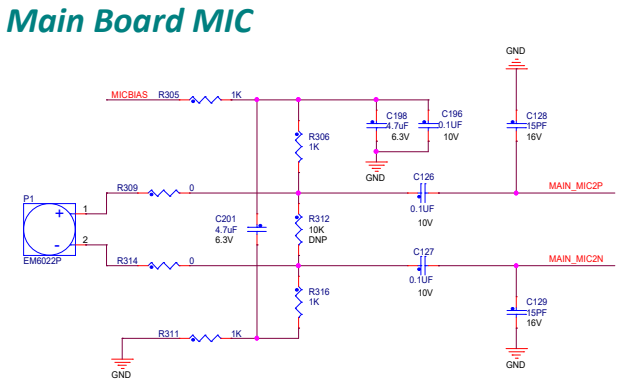

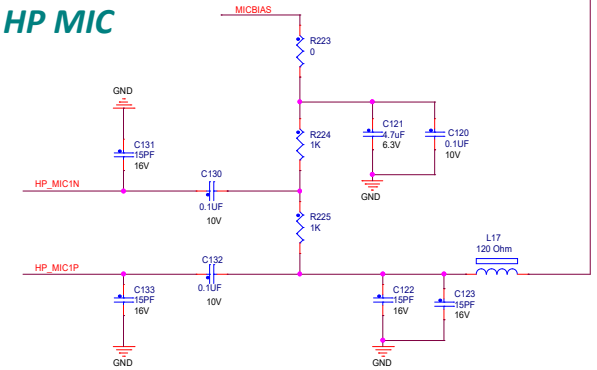

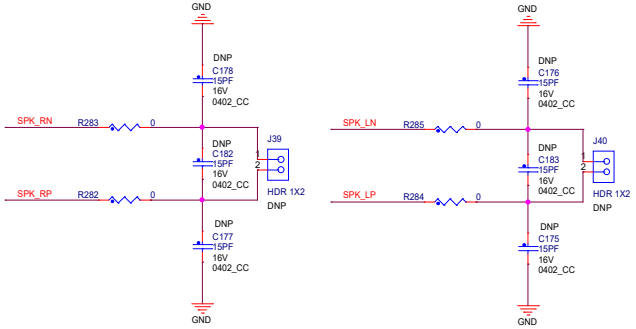

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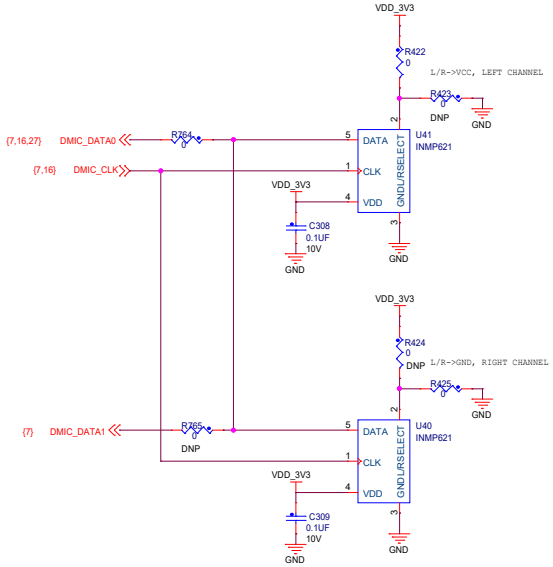
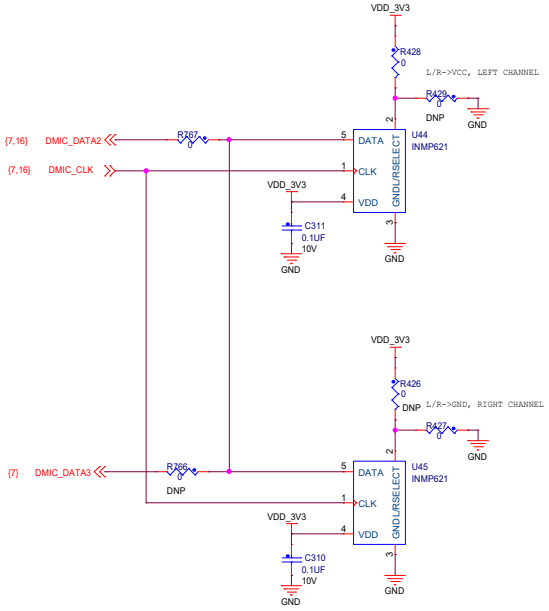
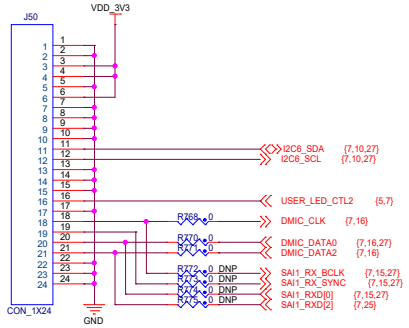
DMIC Interface





MIC ARRAY EXTENSION



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Page Title: **DMIC**

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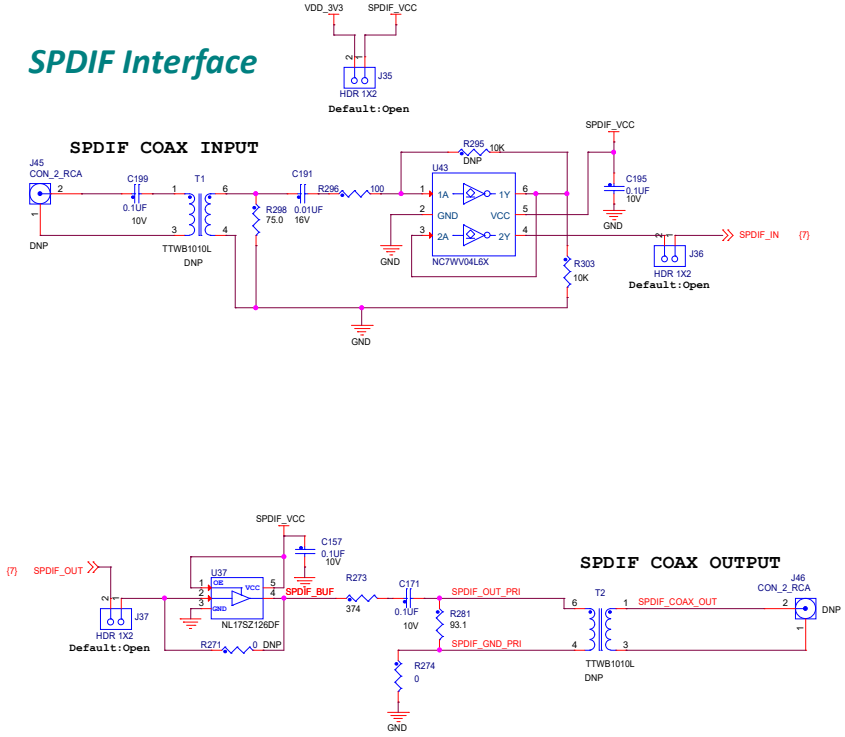
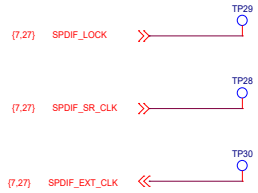
SPDIF Interface





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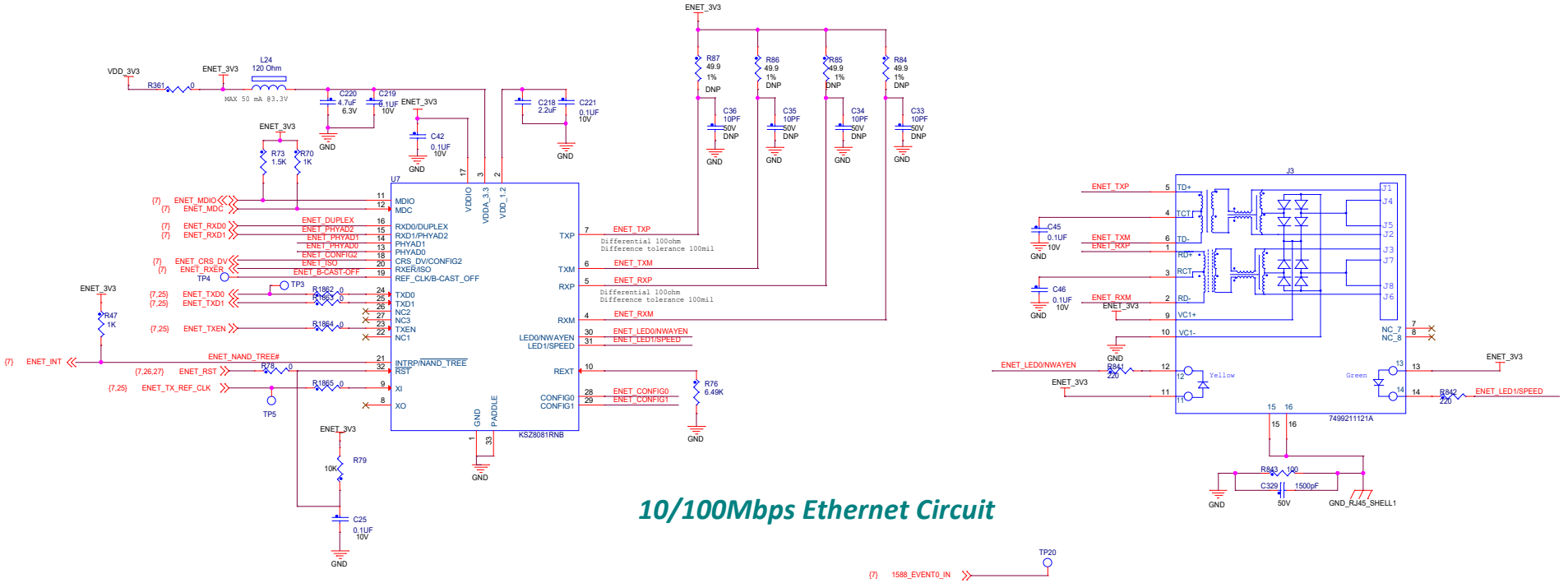
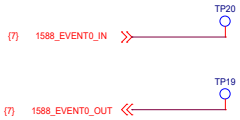
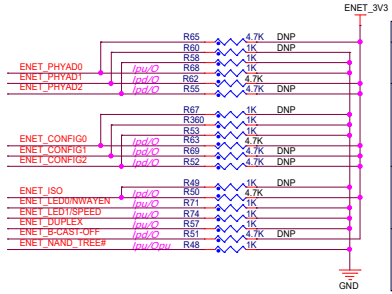


10/100Mbps Ethernet Circuit

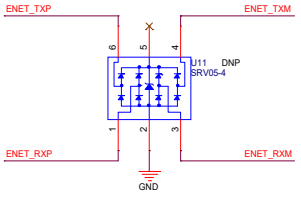




# CFG	Description
PHYAD[2:0]	PHY ADDR 00-XXX (00010 DEFAULT)
CONFIG[2:0]	IF MODE 001 RMII 101 RMII Back-to-Back xxx Reserved-not used
ISO	ISOLATE mode Pull-up = Enable Pull-down (default) = Disable
SPEED	SPEED mode Pull-up (default) = 100Mbps Pull-down = 10Mbps

# CFG	Description
DUPLEX	DUPLEX mode Pull-up (default) = Half Duplex Pull-down = Full Duplex
NWAYEN	Nway Auto-Negotiation Pull-up (default) = Enable Pull-down = Disable
B_CAST_OFF	Broadcast Off - for PHY Address 0 Pull-up = PHY Address 0 set as unique PHY addr Pull-down (default) = PHY Address 0 set as broadcast PHY addr
NAND_TREE#	NAND Tree Mode Pull-up (default) = Disable Pull-down = Enable

ESD PROTECTION



ICAP Classification: CP: ___ IUO: PUBI: ___

Drawing Title: **MIMXRT1170-EVK**

Page Title: **10M/100M ETHERNET**

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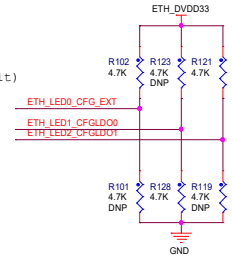
SOC RGMII 1.8V SIGNALS

{7,25} ENET_RGMII_TXC → ENET_RGMII_TXC
{7,25} ENET_RGMII_TX_EN → ENET_RGMII_TX_EN
{7,25} ENET_RGMII_TXD0 → ENET_RGMII_TXD0
{7,25} ENET_RGMII_TXD1 → ENET_RGMII_TXD1
{7,25} ENET_RGMII_TXD2 → ENET_RGMII_TXD2
{7,25} ENET_RGMII_TXD3 → ENET_RGMII_TXD3

{7} ENET_RGMII_RXC → ENET_RGMII_RXC
{7} ENET_RGMII_RX_EN → ENET_RGMII_RX_EN
{7} ENET_RGMII_RXD0 → ENET_RGMII_RXD0
{7} ENET_RGMII_RXD1 → ENET_RGMII_RXD1
{7} ENET_RGMII_RXD2 → ENET_RGMII_RXD2
{7} ENET_RGMII_RXD3 → ENET_RGMII_RXD3

CFG_EXT
EXTERNAL: 1(Default)
INTERNAL: 0

CFG_LDO[1:0]
1.8V: 10 (Default)
2.5V: 01
3.3V: 00

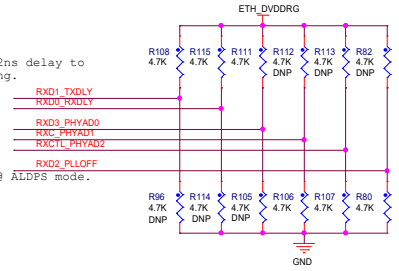


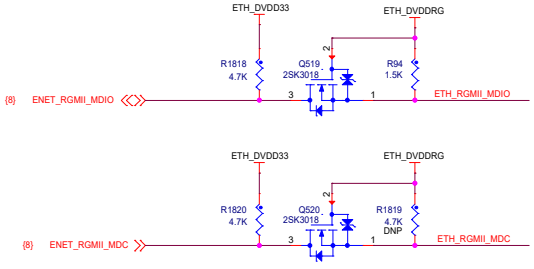
Pull-up for additional 2ns delay to TXC/RXC for data latching.

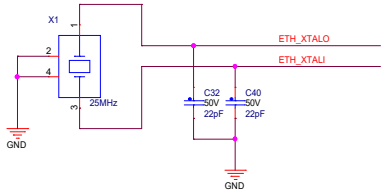
TXC Delay Config
RXC Delay Config

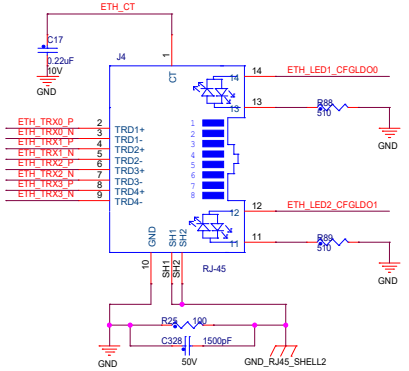
PHY_ADDR0
PHY_ADDR1
PHY_ADDR2
PHY_ADDR: 00001

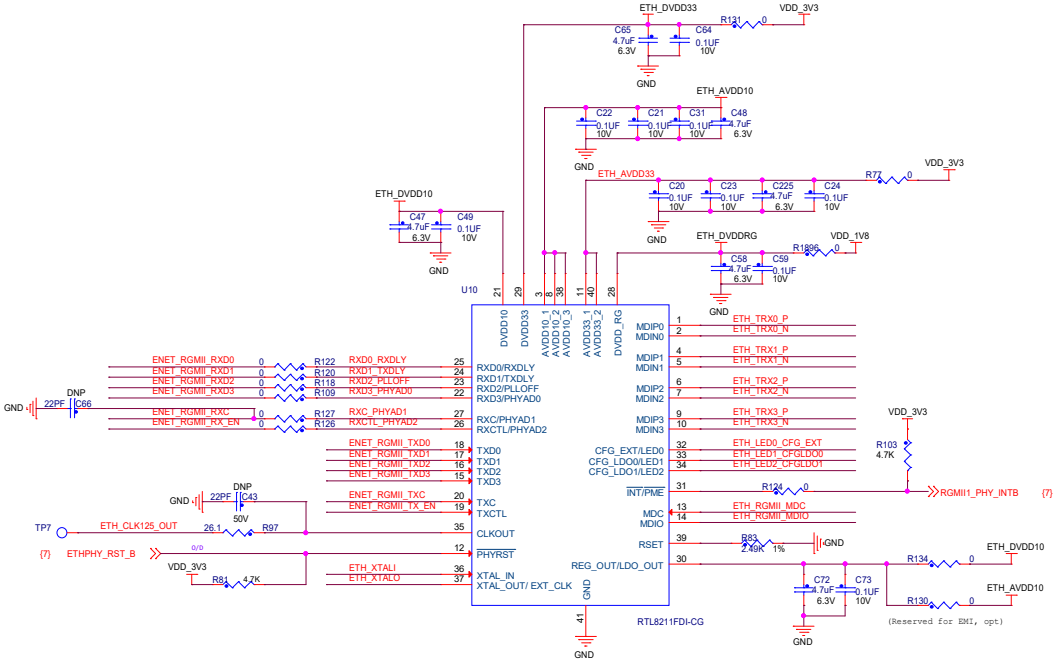
Pull-up to disable PLL @ ALDPS mode.

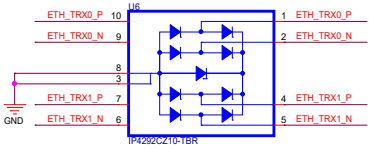


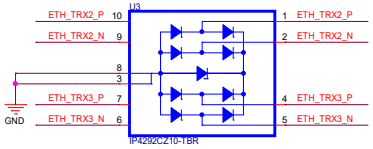












NXP

ICAP Classification: CP: ___ IUO: PUBI: ___
Drawing Title: **MIMXRT1170-EVK**
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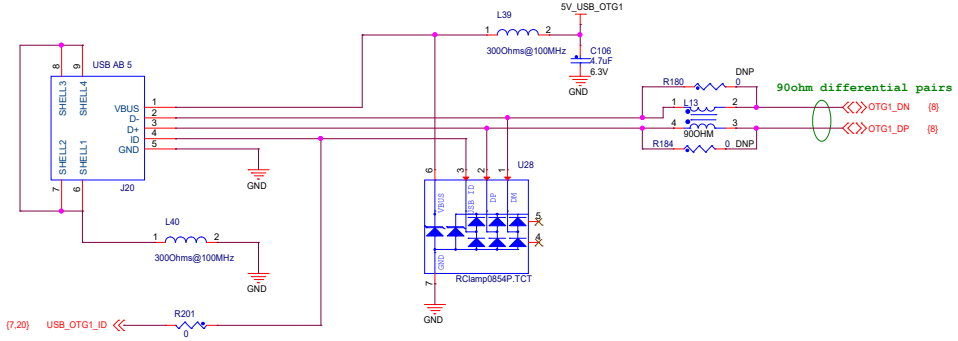
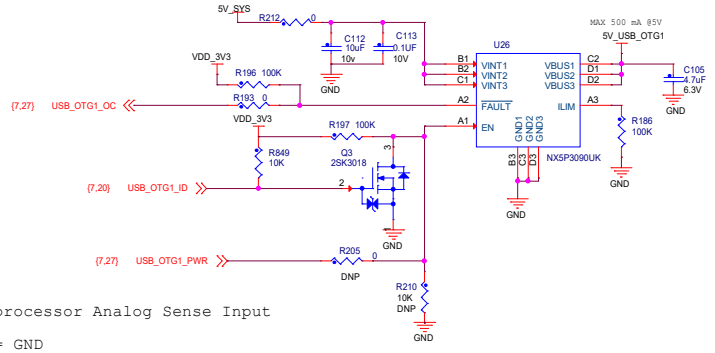
USB OTG1



USB ID is a processor Analog Sense Input

Host --> ID = GND
Device --> ID = Floating

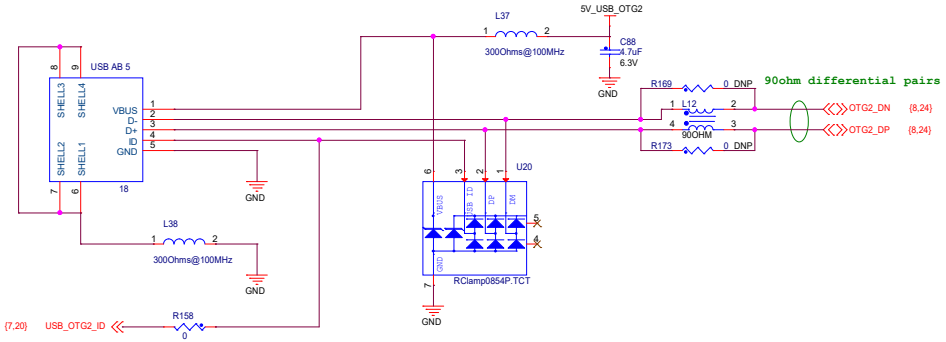
USB Power



USB ID is a processor Analog Sense Input

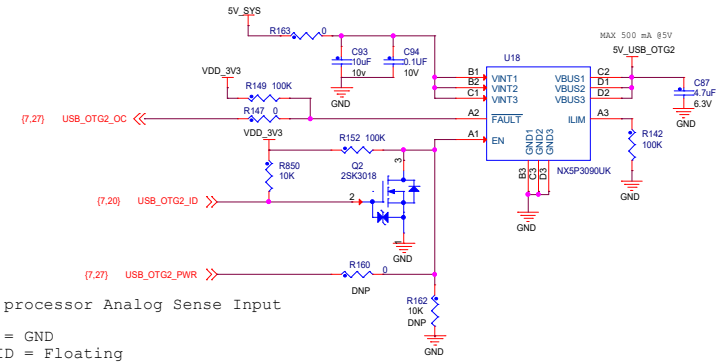
Host --> ID = GND
Device --> ID = Floating

USB OTG2



USB ID is a processor Analog Sense Input

Host --> ID = GND
Device --> ID = Floating



ICAP Classification: CP: ___ IUO: PUBI: ___

Drawing Title: **MIMXRT1170-EVK**

Page Title: **USB**

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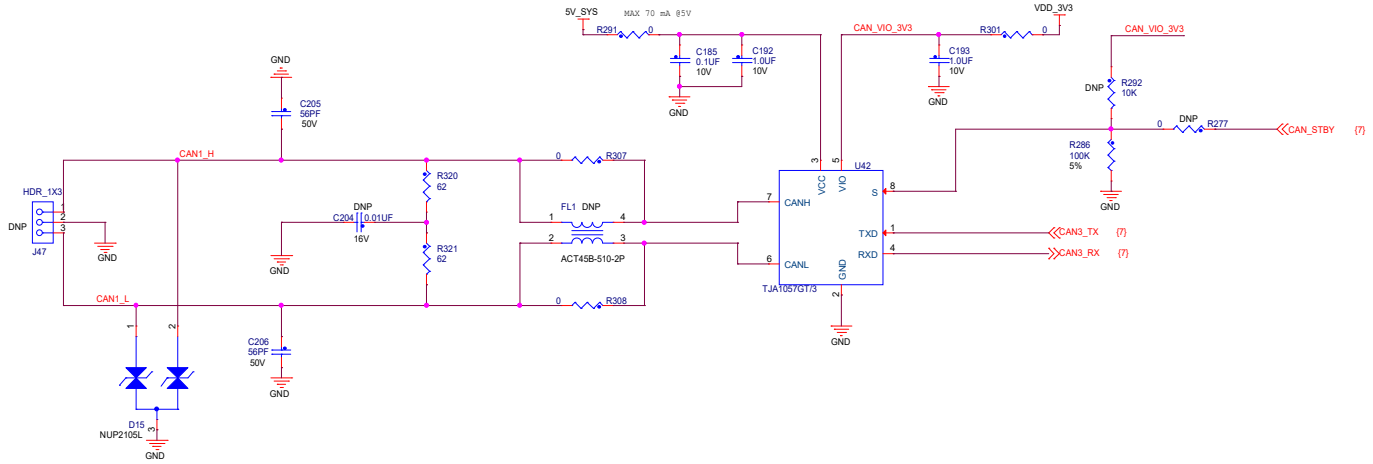
CAN Bus



ICAP Classification:	CP: ___ IUO:	PUBI: ___
Drawing Title:	MIMXRT1170-EVK	
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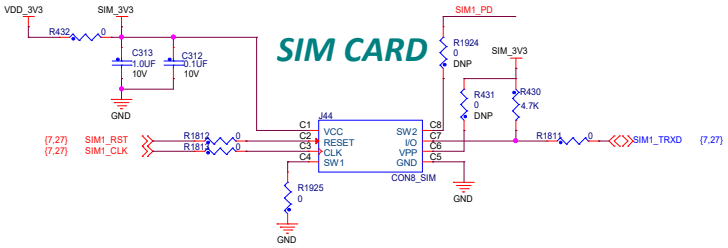
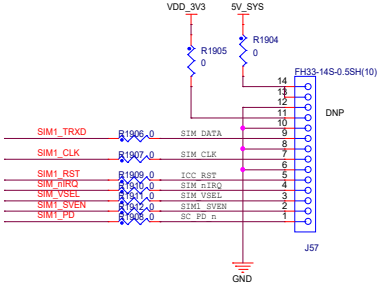
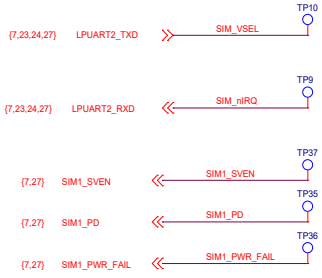
If using detection function:
Populate R1924, DNP R410

Connector reserved for EMV L1 test







ICAP Classification: CP: ___ IUO: PUBI: ___

Drawing Title: **MIMXRT1170-EVK**

Page Title: **SIM CARD**

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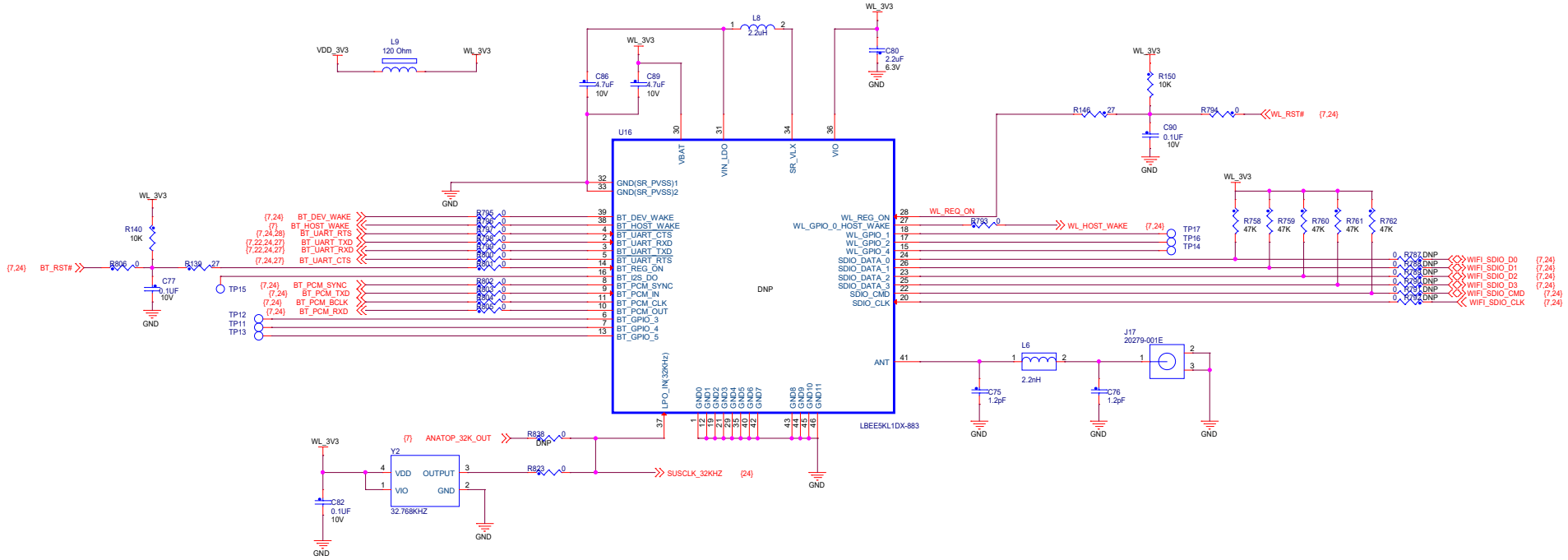
WIFI# LBEE5KL1DX-883



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Drawing Title:	MIMXRT1170-EVK	
Page Title:	WiFi&BT	
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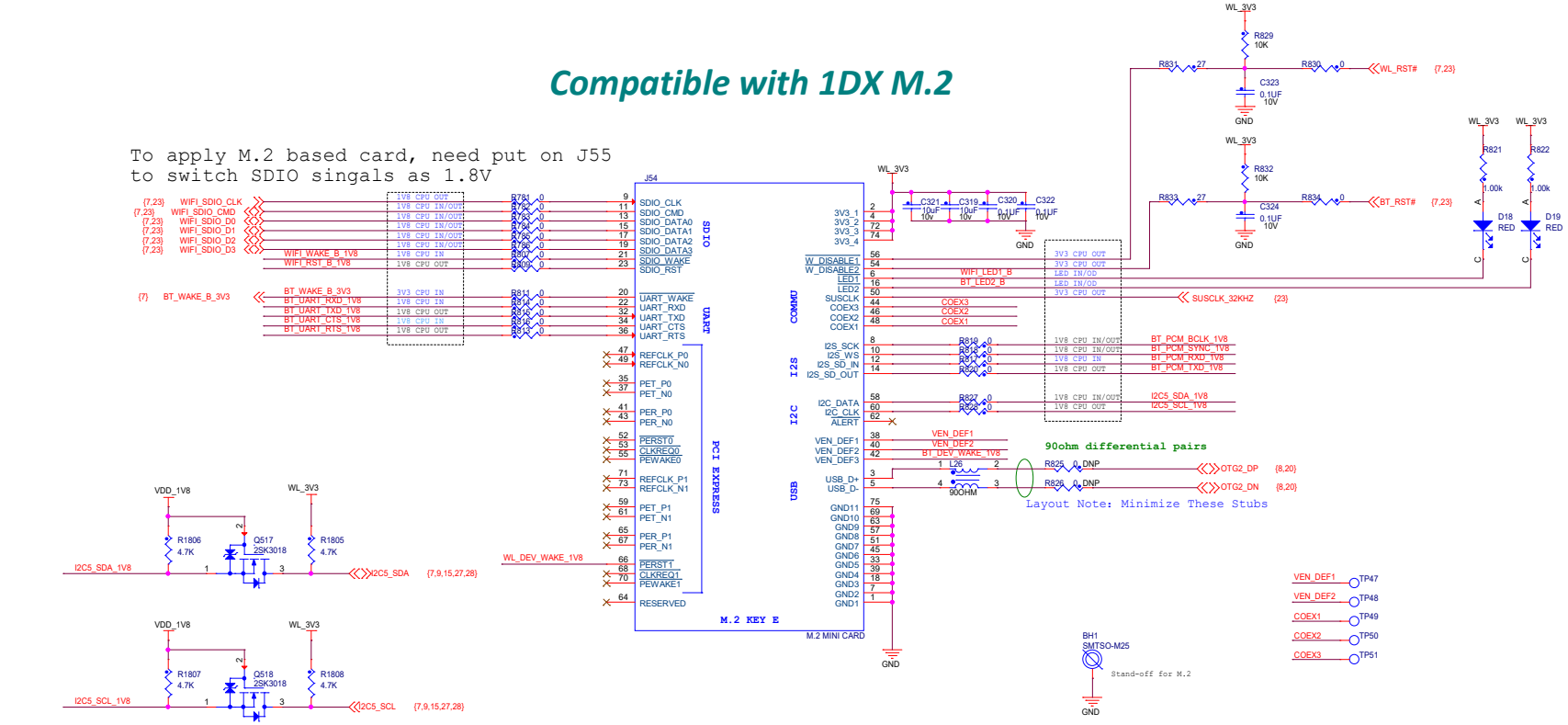
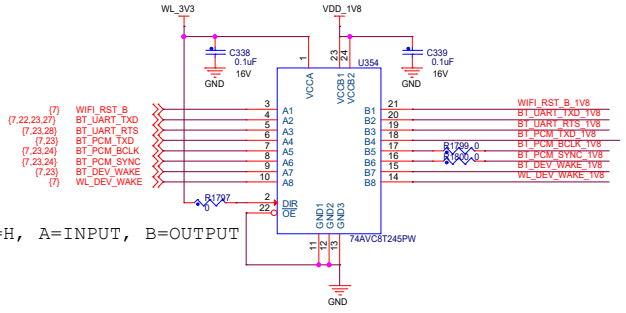
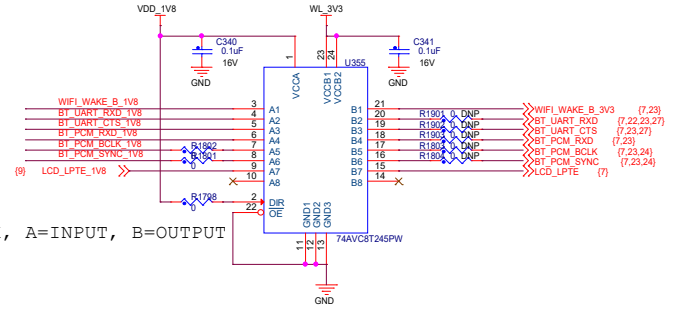
Compatible with 1DX M.2

To apply M.2 based card, need put on J55
to switch SDIO singals as 1.8V





DIR=H, A=INPUT, B=OUTPUT



DIR=H, A=INPUT, B=OUTPUT

ICAP Classification:	CP:	IUO:	PUBI:
Drawing Title:	MIMXRT1170-EVK		
Page Title:	M.2 SOCKET		
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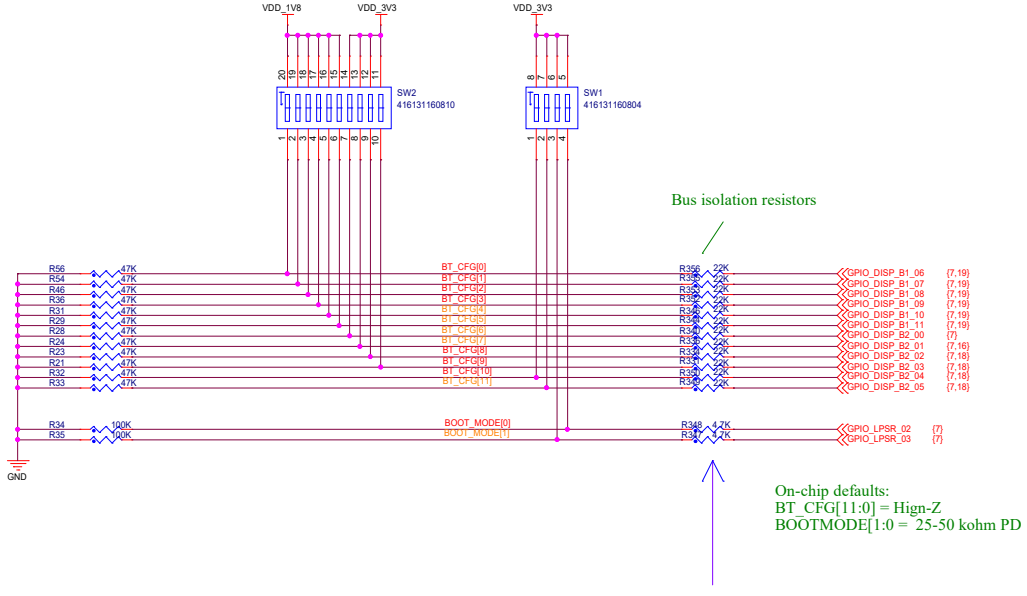
Boot Configuration

	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
TYPE	**BOOT_CFG[11]**	**BOOT_CFG[10]**	**BOOT_CFG[9]**	**BOOT_CFG[8]**	**BOOT_CFG[7]**	**BOOT_CFG[6]**	**BOOT_CFG[5]**	**BOOT_CFG[4]**	**BOOT_CFG[3]**	**BOOT_CFG[2]**	**BOOT_CFG[1]**	**BOOT_CFG[0]**
FlexSPI1 - Serial NOR	FLEXSPI_INSTANCE 0 - FLEXSPI1 1 - FLEXSPI2	xSPI_FLASH_TYPE 0 - Boot with default 0x03 Read Enabled / 1 - Reserved 2 - HyperFLASH 1V8 / 3 - HyperFLASH 3V0 4 - MXIC Octal Read / 5 - Micron Octal Read			0	0	0	0	FLASH_PROBE_TYPE 0 - QuadSPI NOR 1 - MXIC Octal 2 - Micron Octal 3 - Adesto Octal		ENCRYPT_XIP_EN	FLALSH_AUTO_PROBE_EN
SD Card	Reserved	Reserved	Bus Width: 0 - 1-bit 1 - 4-bit	Reserved	0	1	SD/SDXC Speed: 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104		SD Power Cycle Enable: '0' - No power cycle '1' - Enabled via USDHC_RST pad	SD Loopback Clock Source Sel: (for SDR50 and SDR104 only) '0' - through SD '1' - direct	Port Select: 0 - eSDHC1 1 - eSDHC2	Reserved
SEMC (NAND)	Reserved	SEMC Access Command: 0 - IPG 1 - AXI	SEMC EDO Mode: 0 - EDO Mode 1 - Non-EDO mode	ONFI compliant: 0 – Yes, ONFI 1 – No, spec	0	0	1	BOOT_SEARCH_STRIDE: Search Stride for FCB and DBBT Search strides in terms of page 0000 - 64 other: Value = 2^(BOOT_SEARCH_STRIDE)				BOOT_SEARCH_COUNT: 0 - 1 1 - 2

Boot MODE pin settings

BOOT_MODE[1:0]	Boot Type
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot
11	Reserved

External Boot Switch



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Drawing Title: **MIMXRT1170-EVK**
Page Title: **BOOT**
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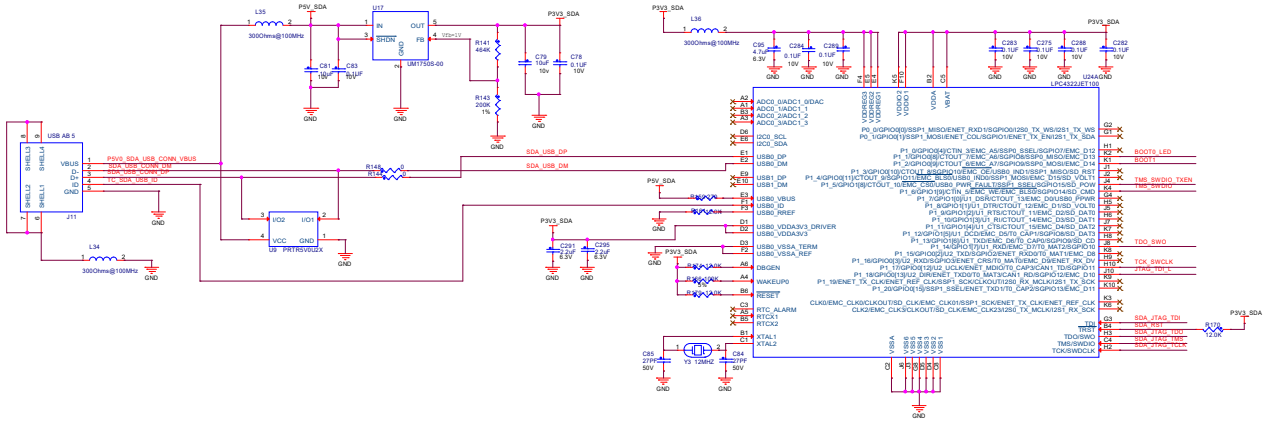
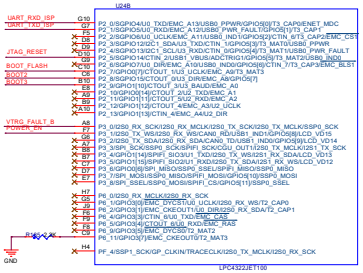
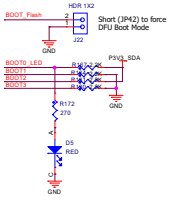
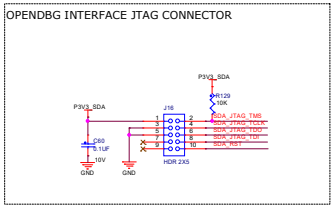
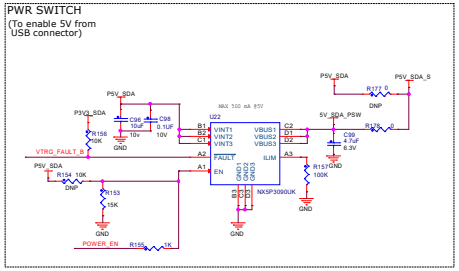
Freelink Interface











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Drawing Title:	MIMXRT1170-EVK		
Page Title:	FREELINK		
Size: D	Document Number: SCH-32171, PDF: SPF-32171		Rev: C3
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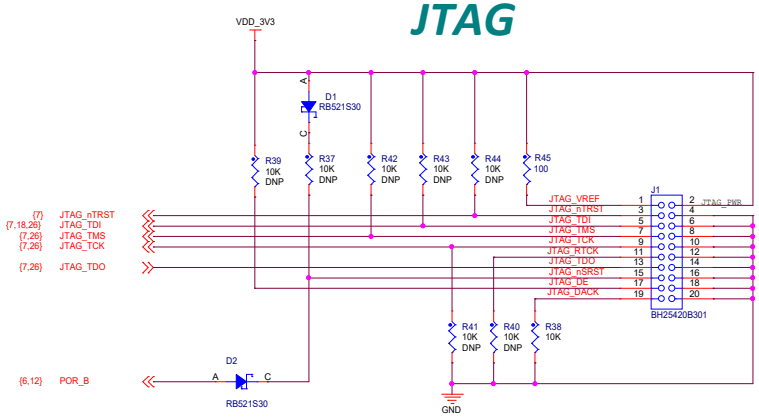
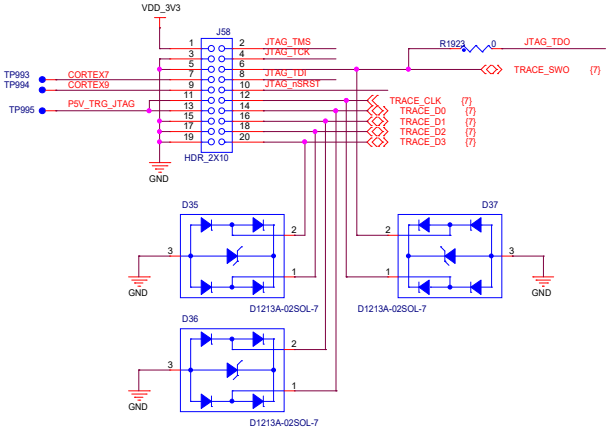
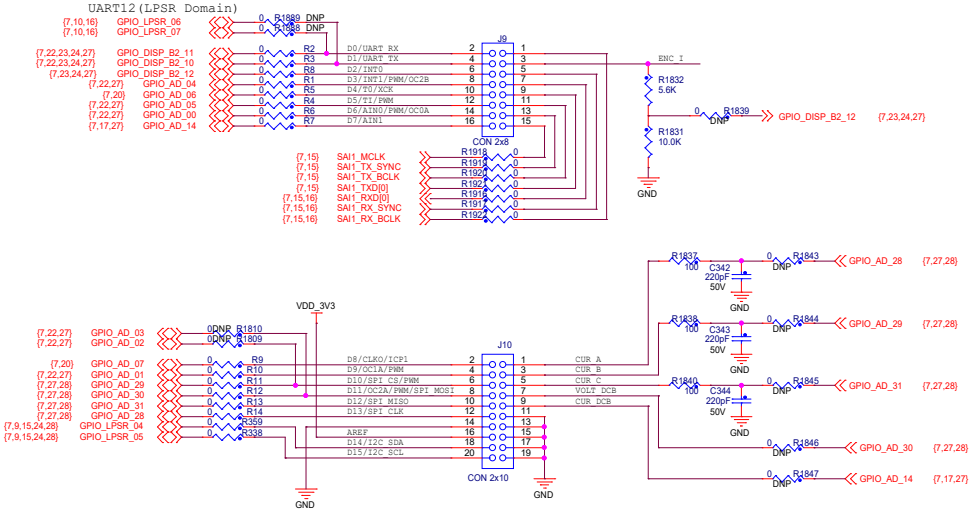
JTAG

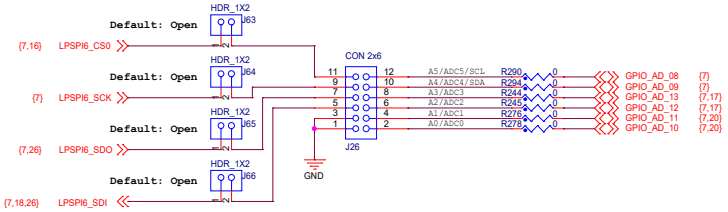


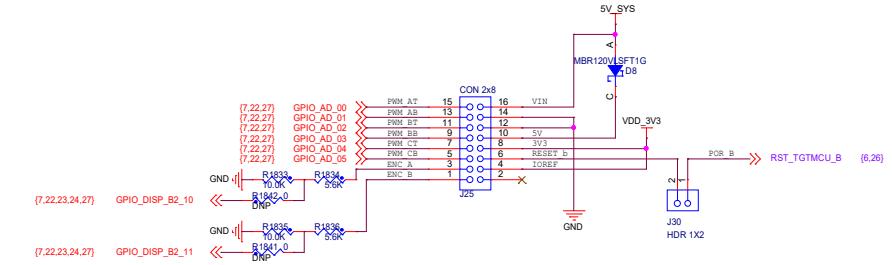
Cortex Debug + ETM



Arduino&MC Interface







ICAP Classification: CP: ___ IUO: PUBI: ___
Drawing Title: MIMXRT1170-EVK
Page Title: INTERFACE/JTAG
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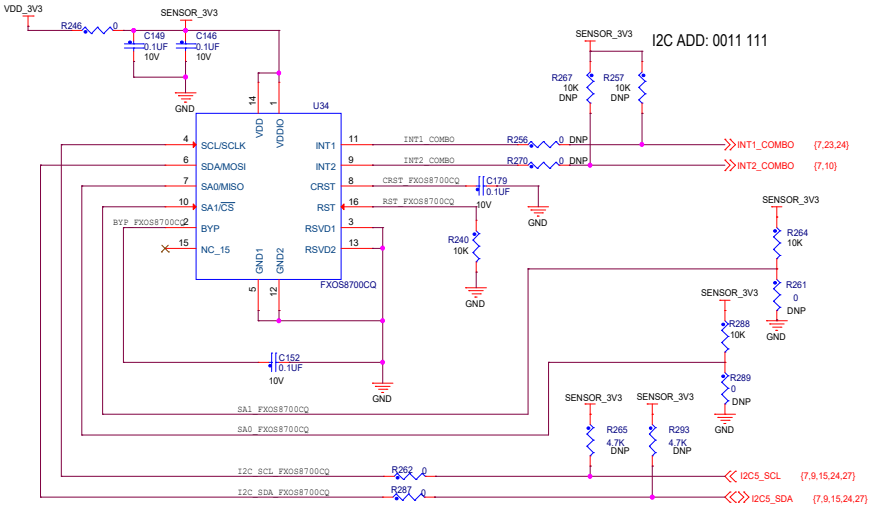
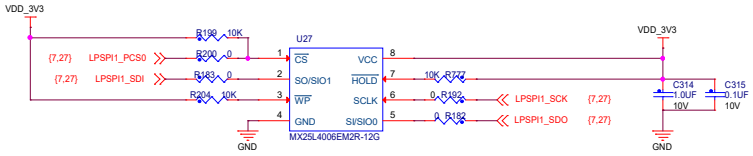
COMBO SENSOR



I2C SLAVE ADDRESS ARE:
0x3E = write
0x3F = read

FXOS8700CQ Combo Sensor to include both Accelerometer and Magnetometer

LPSPI Flash(Secondary Boot)



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Size: C	Document Number: SCH-32171, PDF: SPF-32171		Rev: C3
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