Single Event Effects Characterization of the ST-DDR4 Spin-transfer Torque Magnetoresistive Random Access Memory (STT-MRAM)

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***Abstract*—We present single event effects (SEE) evaluation of the Everspin Technologies 1Gb non-volatile ST-DDR4 spin-transfer torque MRAM.**

I. Introduction

SPIN-TRANSFER torque magnetic random-access memory is a promising solution for radiation-tolerant memory for space environments since its base magnetic tunnel junctions (MTJs) elements have previously demonstrated substantial resilience to radiation effects [1], [2], [3], [4]. The non-volatility and speed of MTJs also make them a viable solution for both working and storage memory applications-thus a potential universal memory for the harsh radiation environments. Commercial STT-MRAM devices with non-volatile memory are available including those from Everspin designed with DDR3 and DDR4 interface with specific improvement in both density and performance. We have previously presented radiation test results of a 256Mb DDR3 component [5]. The EMD4E001G16 is a newly available commercial MRAM device from Everspin with 1Gb of data density with a DDR4 interface developed on the 28-nm CMOS technology node [6]. In this paper, we present heavy-ion and pulsed-laser induced SEE evaluation of the 1Gb ST-DDR4 STT-MRAM, which includes single event functional interrupt (SEFI) characterization of the device.

II. Experimental Procedure

A. Device Datasheet Features (EMD4E001G16G2)

- 1Gb (64Mb x16) ST-DDR4 STT-MRAM, 28 nm CMOS
- 667 MHz clock frequency (fCK), 1333 MT/s data rate
- Bit Error Rate (BER) = $1x10^{-11}$, Data Retention = 3 months @ 70°C, Cycle Endurance = $1x10^{10}$
- Standard 96-ball (FBGA) plastic package

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B. Electrical Test Setup

All test samples were mounted by reflowing onto the MTA4ATF51264HZ-2G3B2 (Micron 4GB x16 260pin) DDR4 SODIMMs as shown in Fig. 1. The process involves removing all four original DDR4 components and reflowing a single STT-MRAM component on the U2 SODIMM footprint. Xilinx's Zynq UltraScale+ MPSoC ZCU104 Evaluation Kit featuring the XCZU7EV-2FFVC1156 MPSoC was used to initialize, calibrate, exercise, and evaluate the MRAM SODIMM before, during, and after irradiation. The evaluation board shown in Fig. 2 was used for exercising the DUT and as a carrier board.

Xilinx's Vivado Design Suite 2018.3 was used for all RTL/HDL development and testing. We executed a script provided by Everspin, and available on their website, to implement necessary changes to the MIG DDR4 example project to successfully exercise the STT-MRAM using DDR4 interface. All tests were performed with a 1333 MHz DDR clock setting.

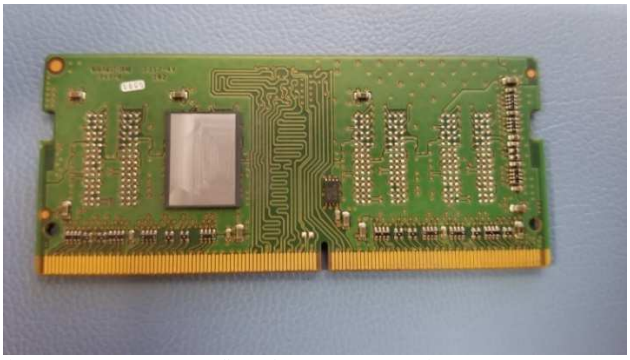

Fig. 1. EMD4E001G16 reflowed on a 4GB x16 Micron DDR4 SODIMM with substrate thinned to ~45 µm for heavy ion testing

Fig. 2. Xilinx MPSoC ZCU104 evaluation board with the DUT inserted in the SODIMM socket

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1) Heavy Ion

For the heavy ion single event latchup (SEL) measurement, we irradiated two devices and kept one additional device for control. The evaluation board was modified in order to provide direct power to the DUT while monitoring device voltages and currents during SEL testing. Fig. 3 shows an illustrative diagram of the device die and substrate in the and packaging. For heavy ion testing, the exposed top-side plastic was etched, and the Si substrate was milled (thinned) to less than 45 µm of thickness to enable high LET ions to penetrate the sensitive volume of the device. It is important to note that the samples prepared for heavy ion testing passed the Xilinx MIG calibration conducting all operation modes within timing and power specification; however, they exhibited bit errors while reading and writing data on the benchtop. These bit errors were not observed prior to thinning the samples. We therefore concluded that the observed bit errors in this set of 45um thick samples are attributed to the sample preparation in etching the top-side plastic and milling the Si substrate, and have conducted the SEL test and analysis accordingly.

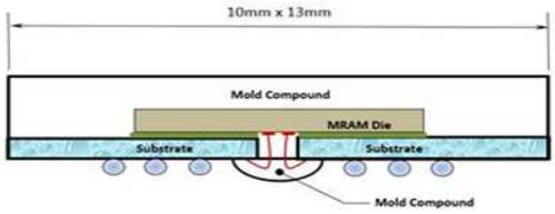

Fig. 3. EMD4E001G16G2 substrate and packaging cartoon diagram

For the heavy ion SEFI characterization, we irradiated two devices and withheld one for control. Test samples were prepared and evaluated similarly to the SEL test except for the substrate thickness. To avoid the bit errors found in the 45 µm thick SEL samples, only 130 µm of substrate was removed in the SEFI samples compared to the 180 µm removed in the SEL samples. We found that the resulting 95 µm samples to be free of bit errors when tested in the same manner.

2) Pulsed Laser

For the pulsed laser SEE test, we evaluated two devices and withheld one additional device for control. We etched the top-side plastic and polished the substrate of both samples; however, thinning was not necessary, as pulse laser penetration is sufficient at the sample thickness of 225 µm. Since the samples prepared for the laser test were not thinned, there is no concern for the thinning-induced bit errors seen on the SEL samples. The ZCU104 on-board switching regulator (IRPS5401) from Infineon allows the user to monitor the 1.2V supply voltage and current in real time through their PowIRCenter software over USB-I2C interface. Consequently, we used a stock ZCU104 evaluation board for the laser test instead of the modified version used for the heavy ion measurements. The 1.2V rail current was monitored during the entirety of the test.

C. Test Facilities

1) Heavy Ion SEL

The heavy ion induced SEL measurements were performed at the Texas A&M University K500 Cyclotron. This facility provides a variety of heavy and light ion beams over a range of energies for SEE testing. The ion beam used for the latchup test is listed in Table I. All measurements were performed in air at normal incidence; the beam flux ranged from $1x10^4$ to $5x10^4$ ions $cm^{-2}s^{-1}$.

TABLE I.
List of ion beams(s) used for SEL measurements at TAMU

Beam Energy (MeV/u)	**Ion**	**Effective LET** (MeV-cm^2/mg)	**Range** (µm)
15	^{197}Au	89.6	85.5

2) Heavy Ion SEFI

The heavy ion induced SEFI characterization was performed at the Lawrence Berkley National Laboratory's 88-inch Cyclotron. Measurements were done both in air, and in vacuum at normal incidence. The heavy ions used for the SEFI test are listed in Table II. The beam flux varied between $1x10^2$ to $5x10^3$ ions $cm^{-2}s^{-1}$ during testing. Except for Xe, the 16 MeV/amu ions were used in air, and the 10 MeV/amu ions were used in the vacuum chamber.

TABLE II.
List of ion beams(s) used for SEL measurements at TAMU

Energy (MeV/amu)	*Ion*	*Effective LET (MeV-cm^2/mg)*	*Range (µm)*
16	Xe	59.7	63.0
16	Cu	30.8	39.9
16	Ar	10.6	105.6
16	Si	6.48	124.5
16	Ne	3.13	198.2
16	N	1.36	356.6
10	Ar	15.9	39.1
10	Si	9.5	47.9
10	Ne	4.6	88.9

3) Pulsed Laser

JPL's single-photon, PULSCAN pulsed laser was used for SEFI screening. The PULSYS-RAD shown in Fig. 4 is optimized for backside (flip chip) SEE testing. It is ideal for SEE testing, screening, and localization. Furthermore, pulsed laser testing is great for test setup verification, complex circuit evaluation, and fault injection. It is important to note that the pulsed laser test is not a replacement for heavy ion measurements. The PULSYS-RAD features include:

- 1064 nm wavelength, 30 ps pulse duration, energy up to 50 nJ
- 3 axis motorized stage (100 nm resolution)
- Backside testing validated without thinning on Si substrate
- Class 1 laser system with safety interlocked enclosure

Fig. 4. JPL's Pulscan PULSYS-RAD single photon laser in B300-121

The laser energies and approximated equivalent LETs (in 225 µm of Si) used for the SEFI test are listed in Table III.

TABLE III.
List of pulsed laser energies used for the SEFI test at JPL

Pulsed Laser Energy (pJ)	**Energy Incident on the DIE** (pJ)	**LET** (MeV-cm^2/mg)
800	528	50
250	165	15
200	138	12
100	68	6

D. Experimental Methods & Radiation Test Setup

1) Heavy Ion SEL

Since bit errors are not a consideration for a SEL test, the bit errors we previously attributed to thinning on these 45 µm thick SEL samples are ignored during the SEL testing. For the latchup test, we chose to power the DUT voltage rails V_{DD}/V_{DDQ} and V_{PP} directly through a four-channel Keysight N6700B power supply which was controlled, monitored, and logged through our custom software over Ethernet. The SEL detection software is capable of detecting increases in the DUT supply current and initiate power cycles while maintaining an event count. The user inputs the current threshold which is typically twice the nominal device operating current. The nominal current draw on the 1.2V rail was around 1A while the current for 2.5V was 135mA. Both nominal currents were fairly large since it was not possible to isolate the DUT 1.2V and 2.5V rails from the rest of the Xilinx evaluation board components that use the same power source. Regardless, we were able perform our SEL measurements by providing direct power, by-passing on-board regulators and current limiting components.

Identifying failure mechanisms and the source for the high current events due to SEE in complex devices can be challenging. Consequently, we performed SEL verification test methods such as testing at both ambient and elevated temperatures and by removing all current clamps from the power supply to analyze the behavior of the DUT supply current. A heat gun was used to elevate the device temperature while monitoring the DUT temperature using a Keysight 34972A data acquisition unit with thermocouples and a FLIR IR thermal imager as shown in Fig. 5. The block diagram of the test setup is shown in Fig. 6, and an actual picture of the setup in front of the beam is shown in Fig. 7.

Fig. 5. EMD4E001G16 in front of the TAMU K500 beam, heated to 75°C

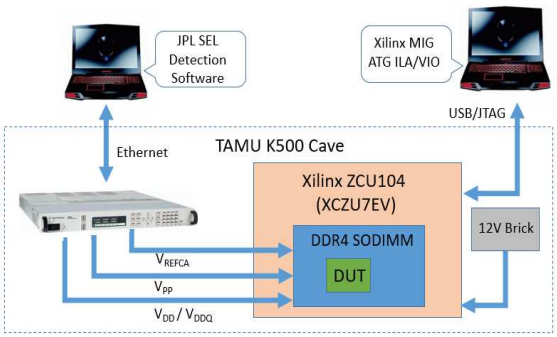

Fig. 6. Heavy ion SEL test setup block diagram

Both samples were tested at ambient (20°C) and at an elevated temperature of 75°C. Typically, to determine each cross-section point, either a minimum of fifty SEL events are recorded or an accumulation of 1x10^7 ions cm^{-2} of beam fluence. All SEL measurements were done in active-idle mode and after each run, the FPGA was reprogrammed to reinitiate the calibration sequence; the result was then recorded. In between each run, both power supplies for the evaluation board and the DUT were power cycled and the FPGA was reprogrammed, and the device was put in the active-idle mode.

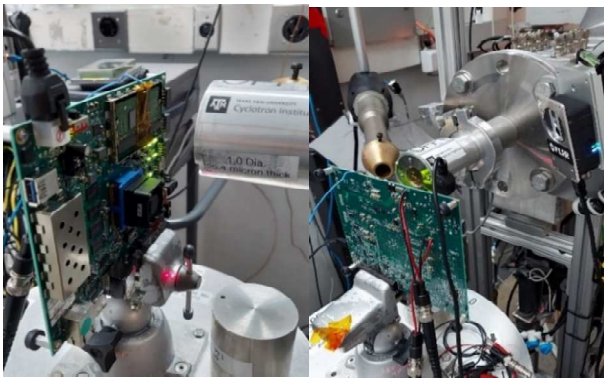

Fig. 7. DUT with the ZCU104 evaluation board in front of the K500 beam

2) Heavy Ion SEFI

The samples prepared for SEFI testing are thicker at 95µm and did not have any preexisting bit errors from sample thinning, which is important for the SEFI testing. The ZCU104 on-board switching regulator (IRPS5401) was used to monitor the 1.2V supply during testing. A block diagram of the SEFI test setup is shown in Fig. 8, and the actual test setup in front of the beam is shown in Fig. 9. Both samples were tested at ambient (23°C) temperature only.

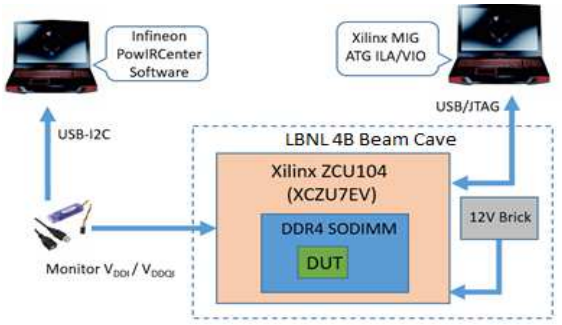

Fig. 8. Heavy ion SEFI test setup block diagram

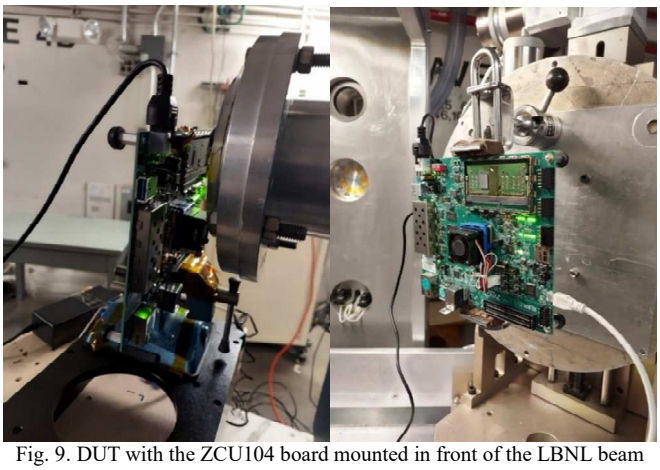

Fig. 9. DUT with the ZCU104 board mounted in front of the LBNL beam line (air and vacuum)

For the majority of the SEFI measurements, we operated the MIG in "write-once read forever" mode (to the entire device) with PRB23 data pattern at maximum speed of 1333 MT/s. Before each run, we power cycled the FPGA board, which means the DUT was also power cycled. We then reprogrammed the FPGA, noted the MIG calibration status, set the traffic generator parameters accordingly, and ran the memory controller. We observed that there were no errors while the device was continuously being read without beam. An error flag trigger was set on the Xilinx debugger ILA waveform to capture any bit-error(s) observed while reading; the MIG ATG reports 128-bit data (64-bit from upper and 64-bit from lower bytes) at once, and if any bitwise mismatch occurs between the actual read data and the expected data, the flag is asserted.

While continuously reading the device and waiting for the error trigger, we began irradiating the device. After a certain amount of beam fluence, the error flag was asserted, the ILA waveform was captured (including raw data and addresses), and the number of bit errors was recorded. The following data was saved as. ila and .csv files for post analysis. The beam/test was stopped immediately after the error flag was asserted. After recording all the data, we performed recovery tests by first trying to do a single read of the entire device and observing the number of bit errors, then by resetting (calibration and mode register reload) and re-reading. If the upsets did not clear by a reset, we initiated a power cycle and read the device again. Finally, if the errors still persisted, we executed a single write-read command to clear all errors. It is important to note that the internal device error correction code (ECC) is enabled by default, and we had no control over its behavior.

Due to some firmware limitation, we had to run the test in "write-read" mode in order to capture majority of the million-SEFIs (MSEFI). We followed all the steps exactly the same as before, except we exercised the device in a continuous write-read mode instead of just read. This allowed us to filter out the smaller error captures, in order to accumulate enough beam fluence to induce the MSEFIs that are less likely to occur compared to the more commonly occurring events that result in small number of bit errors. We also observed write-SEFIs while running in this mode.

3) SEE (Pulsed Laser)

Both samples were tested at only ambient temperature (25°C) since we were only testing for SEFIs. The first sample was tested at a higher laser energy of 800 pJ while the second sample was tested within the 100-250 pJ energy range. For both parts, we focused the laser on the center section of the die where typically most of the memory control logic is located at as shown in Fig. 10.

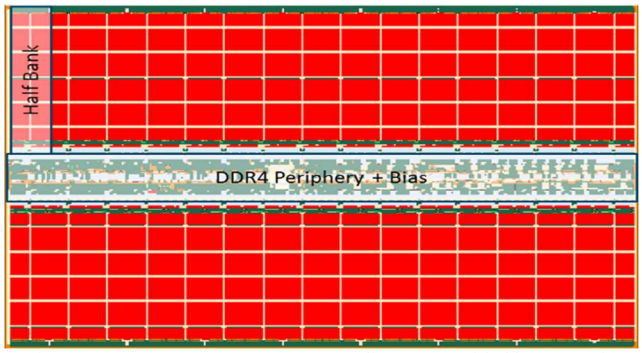

Fig. 10. EMD4E001G16 STT-MRAM die map provided by Everspin

The purpose of this test was to observe and analyze the test readiness of our setup rather than to characterize the device for SEFIs. For all the tests, we picked the "write once read forever" data command mode, which means after writing a specific data pattern (PRBS23/Walking1/Walking0) once to the entire device (1Gb), the MIG traffic generator executed continuous read commands while looking for bit errors at 1333 MT/s. Every time we observed a SEFI, we paused the laser (closed shutter), recorded the number of total bit errors, marked the SEFI sensitive structure/region on the die, and executed a sequence of configurations to try to recover from the event.

III. Test Results & Discussion

1) Heavy Ion SEL

Two devices were tested for SEL at ambient and at 75°C. All tests were performed in air with the 15 MeV/u ^{197}Au ion beam at normal incidence. V_{DD}/V_{DDQ} was set to 1.2V and V_{PP} was set to 2.5V. The nominal current on the 1.2V rail was about 1A while the current for 2.5V was 135mA. The software SEL current thresholds were set to 2A and 250mA respectively. We did not observe any SEL events for both temperatures at a LET of 89.6 MeV-cm^2/mg. We saw a few events where the V_{DDI} current increased by about a 100 mA but it dropped back to nominal on its own. We also observed few events where the current dropped by a few hundred mA and returned to nominal. These events were most likely just upsets or contention in the internal control logic. The plot of the DUT supply currents versus time for one of the test runs is shown in Fig. 11. Both test samples passed Xilinx's MIG calibration after irradiation.

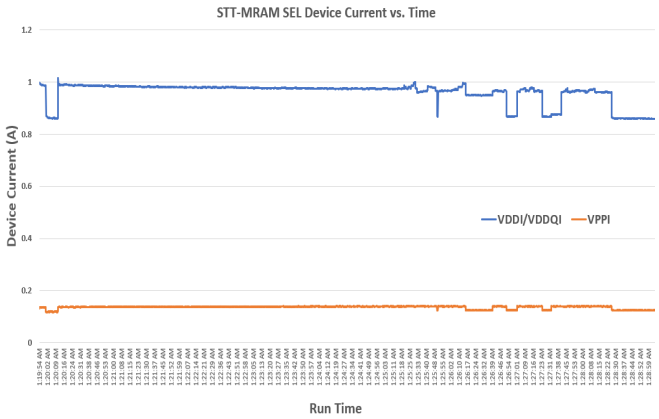

Fig. 11. DUT supply current vs. time for one complete test run. Disruptions in the device current are likely upsets/SEFIs in the control logic

2) Heavy Ion SEFI

Two devices were characterized for heavy ion induced SEFIs at ambient temperature. Measurements were performed in air and in vacuum at normal incidence. V_{DD}/V_{DDQ} was set to nominal 1.2V, and was monitored during testing. No significant current increases were detected during testing. Multiple SEFI types were observed ranging from one to several million bit-errors. Some errors cleared with a device reset, while some errors only cleared by re-writing to the memory. Single bit (SBU) and multibit (MBU) upsets were also observed due to possible bit flips in the control logic's data-cache. The different SEFI modes were categorized as Class I (Million SEFI), Class II (row SEFI), and Class III (SBUs/MBUs). Here is a list of the SEFI categories with detailed descriptions:

Class I (Million-SEFI):

- *Millions of bit-errors observed when reading the device*
- *Significant impact on device operation and data corruption*
- *Saw MSEFIs for both read-only and write-read modes*
  - *Captured read and write SEFIs*
- *For most read-MSEFIs, a reset cleared majority if not all of the bit errors*
  - *Remaining bit errors had to be cleared by a write command*
  - *Read back data all 0s after certain address, complete failure*
- *Reset and power cycle did not clear write-MSEFIs as anticipated*
- *In order to capture MSEFIs, we had to filter out Class II and III events and run to higher fluences*

Class II (Row SEFI):

- *Hundreds of bit-errors in consecutive addresses*
- *Scrambled data for an entire page (2kb) on either the lower or upper byte (not both at the same time). The "scrambled data" is random patterns of 0s, 1s, 2s, and 3s or patterns of 0s, 4s, 8s, Cs. In some cases, it was just a totally random pattern.*
  - *Example 1: Expected data: 0x14cad2fa279e6918, Read data: 0x1002123223122110*
  - *Example 2: Expected data: 0x35548b9cfe229ebf, Read data: 0x3110031032221230*
  - *Example 3: Expected data: 0x2e085795d328922b, Read data: 0x0c084484c0088008*
  - *Example 4: Expected data: 0x 9d2da0bbf23664a1, Read data: 0xdb02f917b5809b45*
- *This event could be defined as a row SEFI corrupting the data in an entire page*
- *Majority of the time the errors only cleared with a write command*
- *Occasionally reset cleared most of these errors but a few remained and had to be cleared by a write command*
- *Similar cross-section to MSEFI*

Class III (SBUs/MBUs):

- *1-5 bit-errors, mostly single bit, but appeared as SBUs and 128-bit word MBUs*
- *Did not clear with a read command, reset (calibrate and mode register reload), or power cycle*
- *Only cleared with a write command (re-writing to the memory)*
- *Did not interrupt functionality and operation of the device*
- *Can hardly be defined as SEFIs, since the errors do not come in a burst, do not continue to accumulate after the initial event, and the device continues to function properly*
- *Has the largest cross-section from all the SEFI events, possible to generate a per bit cross-section if we can find out the bit density of the sensitive area in the control logic*
- *Control logic error can cause erroneous operation in the non-volatile memory, causing incorrect data in the memory that needs a write command to clear the error.*

Fig. 12 shows the cross-section versus LET curve for the three SEFI types. As expected, the cross-section for Class III SEFI is about an order of magnitude bigger due to the presence of data-cache SBUs and MBUs. The drop-off in the cross-section at the higher LETs is due to limited ion range. The parameters for the Weibull fits are listed in Table IV. All SEFIs and bit upsets were results of exposing the die's DDR4 control logic to the heavy ions.

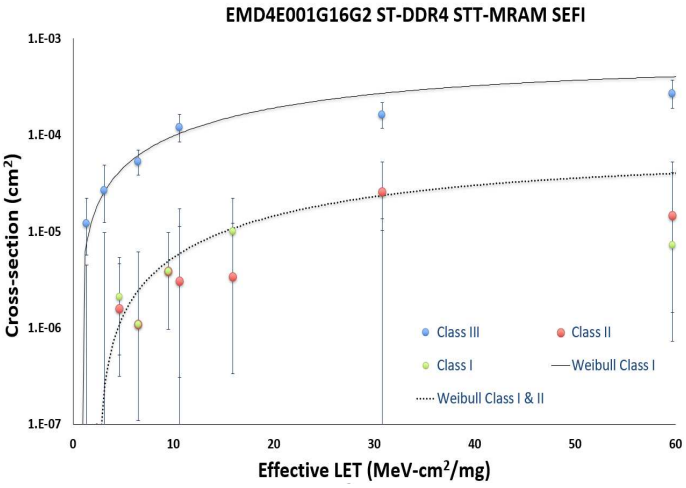

Fig. 12. ST-DDR4 STT-MRAM heavy ion induced SEFI cross-section versus LET curve

TABLE IV.
STT-MRAM SEFI Weibull parameters

Weibull Fit	LET_{th} (MeV-cm²/mg)	Saturated Cross-section	Shape	Width
Class III	0.5	$5.0x10^{-4}$	1.1	38
Class I & II	2.5	$5.0x10^{-5}$	1.3	40

Everspin's DDR3 STT-MRAM (EMD3D256M08B) was previously tested for SEE and limited SEFI data was collected [7]. The SEFI cross-section versus LET curve is shown in Fig. 13. Although it is difficult to come up with any conclusive correlation between the SEFI measurements of the two device types, it is clear that the SEFI cross-section for the DDR4 interface is about an order of magnitude larger than the DDR3, especially at the lower LETs. This is not surprising, since the ST-DDR4 has a larger density, faster interface, great number of mode registers, and an overall more complex control logic than the ST-DDR3. Both devices seem to experience SEFIs that can corrupt large portions of the memory.

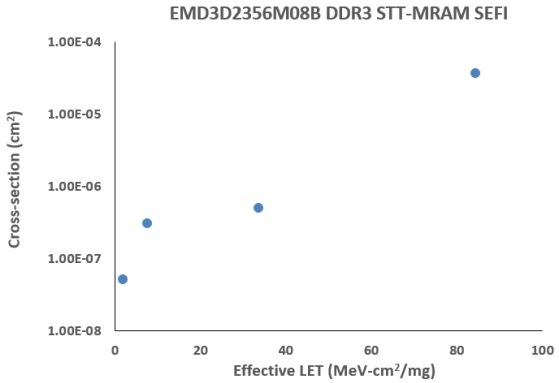

Fig. 13. DDR3 STT-MRAM heavy ion induced SEFI cross-section versus LET curve

3) Pulsed Laser

Two devices were screened for SEFI at ambient temperature of 24°C. During this screening, the laser was directed only at the DDR4 control logic region of the die. The first sample was tested with a laser energy of 800 pJ. While randomly scanning the DDR4 control logic region of the die, we saw a single SEFI that caused a burst of bit errors (few hundred bits) on the lower data byte. The same number of bit errors accumulated on every read cycle even after stopping the laser. We tried resetting the MIG traffic generator, reprogramming the FPGA, and power cycling the evaluation board including the DUT; however, the number of bit errors persisted until a write command cleared the errors. This was a row SEFI similar to the Class II events described previously. The second event we observed resulted in a much bigger burst of bit errors (in the order of 10^7). After applying the recovery methods mentioned above including a write command which cleared most of the errors except for some, we observed about $5x10^5$ "stuck bits" on the lower data byte. Those errors would not clear regardless of resetting, power cycling, write commands, or data pattern selection. We concluded that the high energy setting and frequency of the pulsed laser most likely damaged the device, which is supported by the fact that marks were observed etched into the control logic region of the die by exposure to the laser at this energy.

Following the results of the first test sample, we decided to lower the laser energy to 250 pJ for the second sample. This energy proved to be a much more effective setting for capturing SEFIs. We observed several Class II with similar failure behavior (bit error) as the first event observed on the first sample. These SEFIs resulted in a few hundred bit-errors after reading the entire device. The errors did not clear (persisted at every read cycle) with a MIG reset, FPGA reprogram, or a complete power cycle. However, a single write command did clear the errors. All initial errors observed were on the lower data byte.

After scanning and marking a few more SEFI sensitive structures, we turned down the laser energy to 100 pJ. After rescanning the previously marked SEFI sites with this laser energy, we were only able to induce a single bit error in the control logic; we did not observe any multi-bit error SEFIs at 100 pJ.

We increased the laser energy to 200 pJ and observed several more SEFIs. However, the burst of bit errors was at least an order of magnitude lower than what we captured at 250 pJ. We observed less than 10 bit-errors accumulate on every read cycle. These errors were still on the lower data byte. Although we did not collect sufficient data or do any in-depth analysis, the number of bit errors induced by the observed SEFI events at the different laser energies could be roughly plotted as shown in Fig. 14. This plot is only a rough observation of our pulsed laser measurement with limited data. We did not observe any MSEFIs with the pulsed laser.

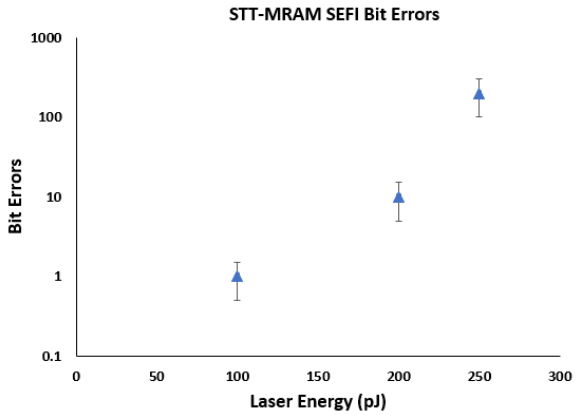

Fig. 14. Laser energy vs. bit errors induced by a single SEFI event

Lastly, we scanned the opposite side of the die and increased the energy back to 250 pJ. We observed several SEFIs on the upper data byte (instead of the lower byte) with similar bit-error behavior to previous SEFIs seen at this energy. All these bit errors and those in Fig. 14 are understood to be a result of exposing the DDR control logic region of the die to the laser.

IV. ACKNOWLEDGMENTS

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V. Conclusion

The EMD4E001G16 ST-DDR4 STT-MRAM from Everspin Technologies was evaluated for heavy ion induced SEE and pulsed laser induced SEFI screen. The device is shown to be SEL immune up to a LET of 89.6 MeV-cm^2/mg. Multiple SEFI types were observed by exposing the control logic of the device to heavy ions and pulsed laser. No significant supply current increases were observed during SEE testing. Due to the non-volatile nature of the device, and the DDR4 control logic, the majority of the SEFIs resulted in erroneous operation of the non-volatile memory and could only be cleared by rewriting/scrubbing the memory. The control logic SEFI cross-section appears to be comparable to SEFI measurements from similar non-volatile SDRAM devices [8], [9].

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