Total Ionizing Dose and Reliability Evaluation of the ST-DDR4 Spin-transfer Torque Magnetoresistive Random Access Memory (STT-MRAM)

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***Abstract*—We present total ionizing dose (TID) evaluation of the Everspin Technologies 1Gb non-volatile ST-DDR4 spin-transfer torque MRAM, and its effects on the reliability of the magnetic tunnel junctions (MTJs).**

I. Introduction

SPIN-TRANSFER torque magnetic random-access memory is a promising solution for radiation-tolerant memory for space environments since its base magnetic tunnel junctions (MTJ) elements have previously demonstrated substantial resilience to radiation effects [1], [2], [3], [4]. The non-volatility and speed of MTJs also make them a viable solution for both working and storage memory applications-thus a potential universal memory for the harsh radiation environments. Commercial STT-MRAM devices with non-volatile memory are available including those from Everspin designed with DDR3 and DDR4 interfaces with specific improvement in both density and performance. We have previously presented single event effects (SEE) test results of a 256Mb DDR3 component, and the ST-DDR4 STT-MRAM [5], [6]. The EMD4E001G16 is a newly available commercial MRAM device from Everspin with 1Gb of data density with a DDR4 interface developed on the 28-nm CMOS technology node [6]. In this paper, we present TID evaluation of the 1Gb ST-DDR4 STT-MRAM, and its reliability response to TID.

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II. Experimental Procedure

A. Device Features (EMD4E001G16G2)

- 1Gb (64Mb x16) ST-DDR4 STT-MRAM, 28 nm CMOS
- 667 MHz clock frequency (fCK), 1333 MT/s data rate
- Bit Error Rate (BER) = $1x10^{-11}$, Data Retention = 3 months @ 70°C, Cycle Endurance = $1x10^{10}$
- Standard 96-ball (FBGA) plastic package

B. Electrical Test Setup

All test samples were mounted by reflowing onto the MTA4ATF51264HZ-2G3B2 (Micron 4GB x16 260pin) DDR4 SODIMMs as shown in Fig. 1. The process involves removing all four original DDR4 components and reflowing a single STT-MRAM component on the U2 SODIMM footprint. Xilinx's Zynq UltraScale+ MPSoC ZCU104 Evaluation Kit featuring the XCZU7EV-2FFVC1156 MPSoC was used to initialize, calibrate, exercise, and evaluate the MRAM SODIMM before, during, and after irradiation. The evaluation board shown in Fig. 2 was used for exercising the DUT and as a carrier board.

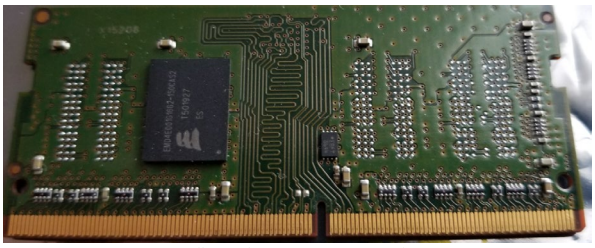

Fig. 1. EMD4E001G16 reflowed on a 4GB x16 Micron DDDR4 SODIMM

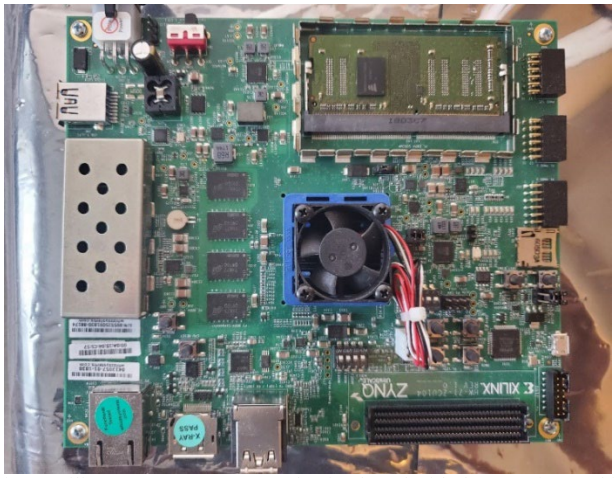

Fig. 2. Xilinx MPSoC ZCU104 evaluation board with the DUT inserted in the SODIMM socket

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We irradiated nine devices and withheld one additional device for control. Eight parts were irradiated in a static biased configuration, while one device was irradiated in an active-idle mode. A discrete bias card based on JPL's standard TID test card was used for the static biased irradiation instead of the evaluation board. The two-layer bias card uses a 280-pin through-hole DDR4 DIMM connector to route all power/ground pins. Additionally, all input/output pins associated with the component including data, address, clock, control, and command, were pulled low (ground) through 10kΩ resistors. None of the device pins were left floating. Fig. 3 shows a DDR4 DIMM-to-SODIMM adapter and a 90-degree SODIMM extender that was used with the bias card to extend and align the device accordingly in the TID cell. The static bias test setup diagram is shown in Fig. 4.

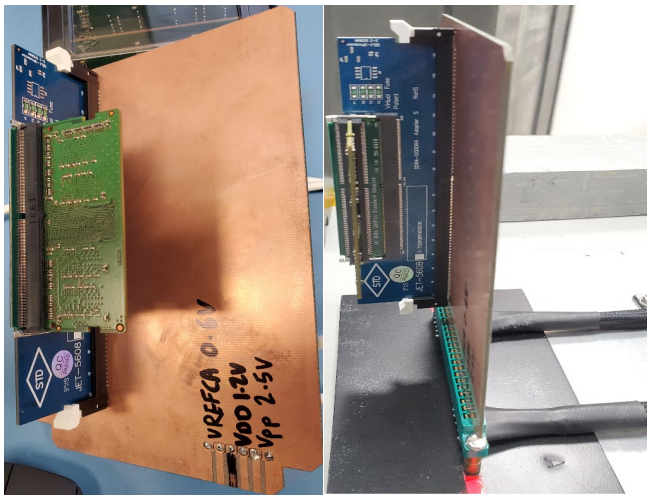

Fig. 3. TID bias card with the DUT inserted in the 90-deg extender inserted in the DIMM-to-SODIMM adapter, vertically facing away from the source

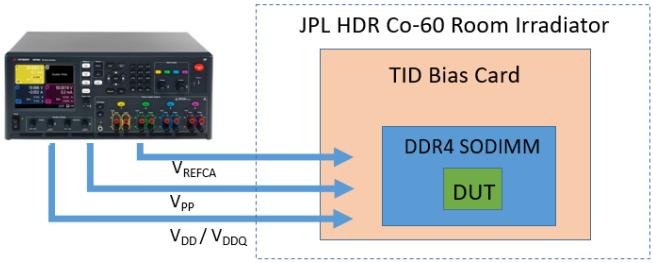

Fig. 4. Static bias test setup during HDR Co-60 irradiation

During static bias irradiation, all device power rails, listed in Table I, were powered directly and independently using a 4 channel Keysight N6705C power supply; voltages and currents were monitored and recorded while irradiating.

TABLE I
STT-MRAM DC supply bias condition

EMD4E001G16	V_{DD} / V_{DDQ}	V_{PP}	V_{REFCA}
Voltage (V)	1.2	2.5	0.6

One device was irradiated in active-idle biased condition to compare the results to the static bias measurements. During irradiation, the STT-MRAM was put in an active-idle mode which means the FPGA was powered and programed, the device was powered, it passed Xilinx's MIG calibration, and it was put in an idle clocked state waiting to receive a command from the controller. Normally, a DDR memory would sit in this idle state and simply execute continuous refresh commands; however, for the non-volatile MRAM, the refresh command translates into no operation. Several DDR4 SODIMM extenders stacked on top of each other, as shown in Fig. 5, were used to elevate the DUT in order for us to isolate the evaluation board and easily shield it from the Co-60 source. With substantial lead brick shielding, we were able to protect the board for the entire test.

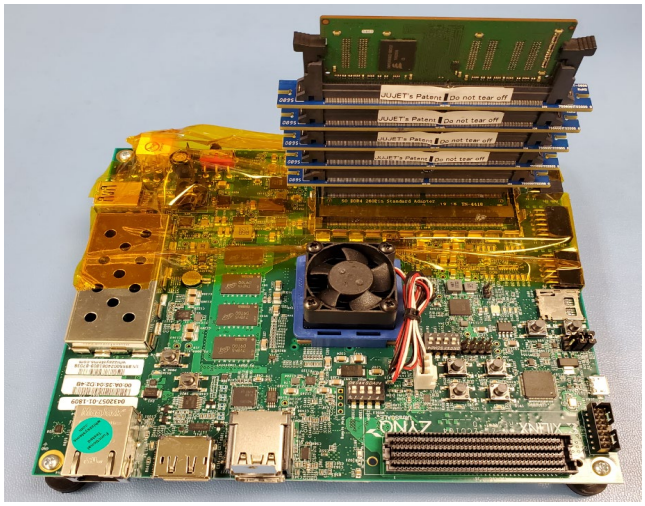

Fig. 5. Xilinx ZCU104 evaluation board with additional SODIMM extenders used for the active-idle TID bias test

C. Test Facility

All TID exposures were performed at JPL's high dose rate (HDR) Co-60 facility. Dose calibrations were performed prior to testing using a calibrated ion chamber (Radcal Accu-Dose, model 2186); exposure is controlled by time and distance from the source. We irradiated one device at a time while covering the DUT with a lead-aluminum box to ensure dose uniformity and to minimize back scattering during radiation.

D. Experimental Methods & Radiation Test Setup

The test samples were subjected to multiple dose levels as shown in Table II. We tested one device at a time in the order listed in the table. The dose rate varied between the static and active-idle biased tests due to the added distance as a result of lead brick shielding to protect the ZCU104 board. The dose rate was 60 and 30 rad(Si)/s for the static bias and active-idle tests respectively. The first sample, serial number 5817, was irradiated at a finer dose step. Based on the results from the first sample, we adjusted the dose steps for the rest of the samples. DUT supply current was recorded and functional tests were performed at each dose step including pre-irradiation. If any degradation or failure modes were to be observed, test samples would have been put through post-annealing at elevated temperatures before repeating the measurements.

TABLE II
Test samples and dose levels

Serial #	Bias	Dose Rate rad(Si)/s	Dose Levels (krad(Si))
5817	Static	60	10, 25, 50, 75, 100, 150, 200, 300
5818	Static	60	50, 100, 150, 200, 300, 400, 500
5819	Static	60	50, 100, 150, 200, 300, 400, 500
5816	Active-idle	30	50, 100, 150, 200, 300, 400
5440	Static	60	250, 500, 750, 1000
5441	Static	60	250, 500, 750, 1000
5442	Static	60	300
5443	Static	60	300
5444	Static	60	300

Since this was a pathfinder test evaluating overall device functionality and tolerance in response to TID, we did not perform AC/DC parametric measurements typically associated with total dose tests. The benchtop test setup diagram is shown in Fig. 6. The following measurements and functional tests were performed at each dose step:

1. *Static and active idle device current measurements*
   - *Static measurements were performed with the static bias card*
   - *Active idle device current measurements were performed for all test devices using the Infineon USB-I2C interface and PowIRCenter software*
2. *MIG Calibration Status*
   - *Initialization, calibration, and device health status*
3. *Bit error functional test*
   - *Split entire 1Gb of the device into four 256Mb partitions*

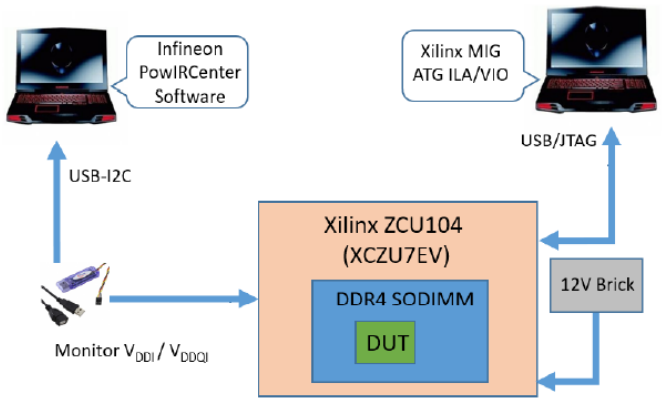

Fig. 6. Diagram of the test setup used for functional measurement

A summary of the functional tests performed at each dose step is shown in Table III. Bit errors were recorded for all test cases. Xilinx's Vivado Design Suite 2018.3 was used for all RTL/HDL development and testing. We executed a script provided by Everspin to implement necessary changes to the MIG DDR4 example project to successfully exercise the STT-MRAM using its DDR4 interface. All tests were performed with a 1333 MHz DDR clock.

TABLE III
Bit error functional measurements performed at each dose step

Partition	Size (Mb)	Mode	Data Pattern
1st	256	Read only, once	PRBS23
2nd	256	Write once, read for 15 min	PRBS23
3rd	256	Write once, read once	PRBS23, Linear, Walking 0 & 1
4th	256	Write and read for 15 min	PRBS23

E. Post TID Data Retention

In order to find out the TID effect on the reliability performance of the device, we performed data retention tests at 150°C and 125°C on both dosed and control parts. For the initial test, pre-bakeout measurements were performed on serial number 5818 and a control device. Both devices were configured and tested identically to one another. The devices were split into four partitions: two 500 Mb blocks, one 10 Mb block, and a 100 Kb block. Prior to the bakeout, all partitions were written with the Walking 1 data pattern, and a readback was performed to observe that there were zero errors. At 150°C, we performed readbacks at the four bakeout steps of 1, 2, 4, and 21 hours. At each step, the devices were taken out of the oven, and brought back to ambient temperature, before measurements were performed. The oven temperature was monitored and logged by an external thermocouple to make sure it stayed consistent.

At 125°C, we performed readbacks of the devices at the bakeout steps of 1, 2, 4, 6, 24, 168, 216, and 312 hours. The data pattern and partitions were the same as for 150°C.

F. Post TID Life Cycle

Cycling endurance tests were also performed on several dosed and control devices. The data pattern and partitions matched the data retention tests. Due to time and resource constraints, the 500 Mb blocks were cycled through for a total of $1x10^4$ and $1x10^6$ cycles, while the 10 Mb and 100 Kb blocks were cycled through for a total of $1x10^8$ and $1x10^{10}$ respectively. A single cycle consisted of executing a write and a read to the entire block.

III. Test Results & Discussion

1) TID

We irradiated nine devices in total; eight in static biased condition using the custom TID bias card and one in active-idle mode using the ZCU104 evaluation board. We did not observe any significant differences in the measurements between the bias conditions. Infineon's USB-I2C software was used to measure the active idle mode V_{DDI}/V_{DDQI} current for all devices at each dose level. There were no changes in the device operating current.

The static bias card was used to measure the static V_{DDI}/V_{DDQI} current for the eight devices at each dose level as shown in Fig. 7. Some of the plots are not entirely visible due to overlapping data. The minor current increase with dose shown in the plot is caused by the increase in the device leakage current in response to TID, which is typical for a

CMOS device based on trapped charges in the gate oxide. There were no increases in V_{PPI} and V_{REFCAI} supply currents.

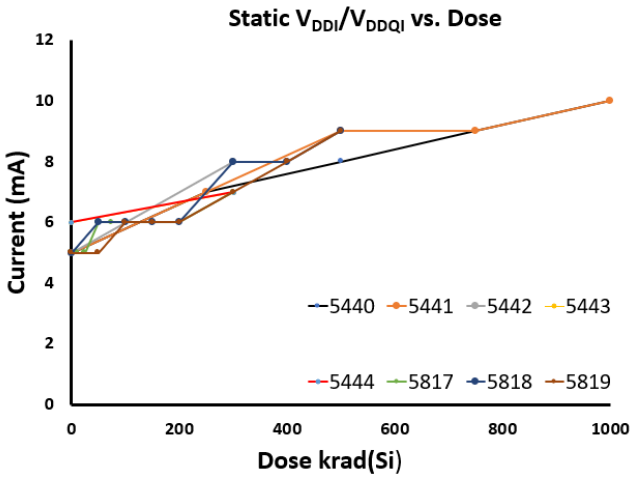

Fig. 7 Static bias device current versus dose

All nine devices passed the Xilinx MIG calibration at every dose step. We did not observe any bit errors for any of the samples; all devices were fully functional up to the corresponding total dose. The summary of the TID test results is shown in Table IV.

TABLE IV
Summary of the TID test results

Sample	Total Dose krad(Si)	Failures/Degradation	Bit Errors
5817	300	None, passed MIG Cal	0
5818	500	None, passed MIG Cal	0
5819	500	None, passed MIG Cal	0
5816	400	None, passed MIG Cal	0
5440	1000	None, passed MIG Cal	0
5441	1000	None, passed MIG Cal	0
5442	300	None, passed MIG Cal	0
5443	300	None, passed MIG Cal	0
5444	300	None, passed MIG Cal	0

2) Data Retention

Data retention tests were performed on control, cycled, and dosed parts at 125°C and 150°C. For the 150°C data retention test, there was a slight correlation in the error rate observed between the dosed and the control samples as shown in Fig 8. The dosed sample shows slightly more errors than the control part at any bake time, but this difference is comparable to the typical variation from die to die even among control dies. Also, the observation of data retention errors even in the control die is not unexpected for this 150°C test since these parts are rated for 70°C data retention of 3 months, and the test method is strongly temperature-accelerated. We did not observe any errors at 125°C up to 312 hours.

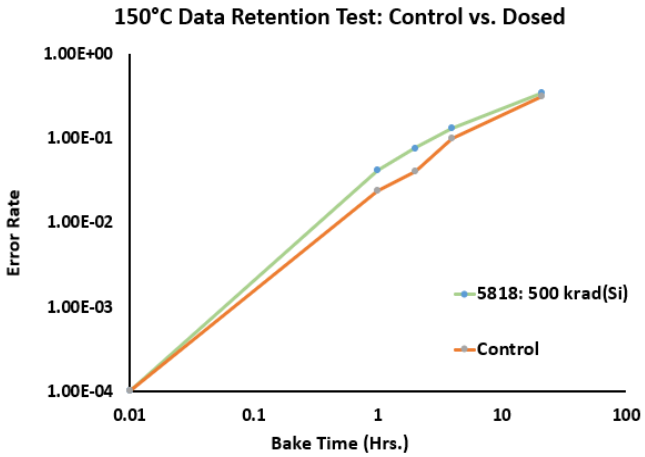

Fig. 8 Retention test results for control and dosed samples

3) Cycling Endurance

Cycling endurance testing was performed on control and dosed samples; the devices were partitioned into four sizes. The total number of write-read cycles performed on each partition incremented by two orders of magnitude accordingly. No errors were observed as shown in Table V.

TABLE V
Cycling endurance test results

Sample	Size	Total W-R Cycles	Bit Errors
Control	500 Mb	10^4	0
	500 Mb	10^6	0
	10 Mb	10^8	0
	100 Kb	10^{10}	0
500 krad(Si)	500 Mb	10^4	0
	500 Mb	10^6	0
	10 Mb	10^8	0
	100 Kb	10^{10}	0

It is important to note that with the internal error correction code (ECC) engine in place, we were not expecting to be able to measure small changes below the ECC correction level. This, combined with the $1x10^{-11}$ bit error rate (BER) limit at the end of cycle endurance life ($1x10^{10}$), would explain why we did not observe any errors during testing.

IV. ACKNOWLEDGMENT

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V. CONCLUSION

The EMD4E001G16 STT-MRAM from Everspin Technologies was evaluated for total ionizing dose, and was previously characterized for single event effects.

We irradiated nine samples up to various dose levels. We did not observe any significant changes in device supply

currents. All parts passed calibration and operated nominally post irradiation. We did not observe any device-level functional-degradation or bit errors such as “stuck bits” typically associated with DDR SDRAMs. It is important to note that ECC was enabled by default for all the measurements.

Post TID life-cycle and data retention tests were performed to study the effects of dose on the reliability of the MTJs. The reliability data, collected with internal ECC in place, does not indicate any significant change after irradiation.

REFERENCES

[1] B. R. Zink, J. Yang-Scharlotta, F. B. Mancoff, J. J. Sun, K. M. Han and J. -P. Wang, "Influence of total ionizing dose on magnetic tunnel junctions with perpendicular anisotropy," in *IEEE Transactions on Nuclear Science*.

[2] D. N. Nguyen and F. Irom, "Radiation effects on MRAM," *2007 9th European Conference on Radiation and Its Effects on Components and Systems*, Deauville, 2007, pp. 1-4.

[3] J. Heidecker, G. Allen and D. Sheldon, "Single Event Latchup (SEL) and Total Ionizing Dose (TID) of a 1 Mbit Magnetoresistive Random Access Memory (MRAM)," *2010 IEEE Radiation Effects Data Workshop*, Denver, CO, 2010, pp. 4-4.

[4] Xiao, T. & Bennett, Christopher & Mancoff, Frederick & Manuel, Jack & Hughart, David & Jacobs-Gedrim, Robin & Bielejec, Edward & Vizkelethy, Gyorgy & Sun, Ji & Aggarwal, Sanjeev & Arghavani, Reza & Marinella, Matthew. (2021). Heavy-ion-induced displacement damage effects in magnetic tunnel junctions with perpendicular anisotropy. IEEE Transactions on Nuclear Science.

[5] R. R. Katti, S. M. Guertin, J. Y. Yang-Scharlotta, A. C. Daniel and R. Some, "Heavy Ion Bit Response and Analysis of 256 Megabit Non-Volatile Spin-Torque-Transfer Magnetoresistive Random Access Memory (STT-MRAM)," *2018 IEEE Radiation Effects Data Workshop (REDW)*, Waikoloa, HI, USA, 2018, pp. 1-4.

[6] Everspin Technologies, “1Gb Non-Volatile ST-DDR4 Spin-transfer Torque MRAM,” EMD4E001GAS2 datasheet, 2020 [Revised Aug. 2020].