User Manual

RM3100 Testing Boards

Geomagnetic Sensor Modules

PNI SENSOR CORPORATION

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1 Copyright & Warranty Information

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2 Introduction

Thank you for purchasing PNI Sensor Corporation's RM3100 Evaluation Board (pn 13606) or PNI 3-Axis Magnetometer Breakout Board (pn 14190). Both parts are referred to in this documentation as RM3100 Testing Boards. The RM3100 Testing Boards are plug-and-play module (PCA) versions of PNI's RM3100 Geomagnetic Sensor, principally intended for quickly evaluating and prototyping PNI's magnetic sensor technology. The primary components of the RM3100 Testing Boards are two Sen-XY-f sensor coils, one Sen-Z-f sensor coil, and PNI's MagI^{2}C ASIC controller. They also incorporate resistors, capacitors, and connectors, all mounted on a PCB, to provide a complete magnetic-field sensing module. The RM3100 Testing Boards incorporate both I^{2}C and SPI interfaces for system design flexibility.

PNI's geomagnetic sensor technology provides high resolution, low power consumption, large signal noise immunity, a large dynamic range, and high sampling rates. Measurements are stable over temperature and inherently free from offset drift. The RM3100 Testing Boards feature both continuous measurement mode and single measurement polling, an alarm feature for monitoring magnetic field strength, software-configurable resolution and sample rate, and the ability to operate one, two, or all three PNI sensor coils. These advantages make PNI's RM3100 Testing Boards not only the choice for prototyping high-volume solutions, but also for lower volume applications that require a complete solution.

Each sensor coil of the RM3100 serves as the inductive element in a simple LR relaxation oscillation circuit, where the coil's effective inductance is proportional to the magnetic field parallel to the sensor axis. The LR circuit is driven by the MagI^{2}C ASIC and the MagI^{2}C's internal clock is used to measure the circuit's oscillation frequency, and hence the magnetic field. Since the RM3100 works in the frequency domain, resolution and noise are established cleanly by the number of MagI^{2}C internal clock counts (cycle counts). In comparison, fluxgate and MR technologies require expensive and complex signal processing to obtain similar resolution and noise, and in many respects the geomagnetic sensor's performance simply cannot be matched. Also, the output from the MagI^{2}C is inherently digital and can be fed directly into a microprocessor, eliminating the need for signal conditioning or an analog/digital interface between the sensor and a microprocessor. The simplicity of PNI's geomagnetic sensor, combined with the lack of signal conditioning, makes it easier and less expensive to implement than alternative fluxgate or magneto-resistive (MR) technologies.

For more information on PNI's magneto-inductive sensor technology, see PNI's whitepaper "Magneto-Inductive Technology Overview" at https://www.pnicorp.com/white-papers/.

3 Specifications

3.1 RM3100 Testing Boards Characteristics

Table 3-1: Operating Performance[1]

Parameter	Cycle Counts[2] 50	100	200	Units
Field Measurement Range[3]	-800 to +800			µT
Gain	20	38	75	LSB/µT
Sensitivity	50	26	13	nT
Noise	30	20	15	nT
Noise Density @ Max. Single-Axis Sample Rate	1.2			nT/√Hz
Repeatability over ±200 µT	15	8	8	nT
Hysteresis over ±200 µT	15			nT
Linearity over ±200 µT	0.5			%
Maximum Single-Axis Sample Rate (divide by 3 for max. 3-axis sample rate)	1600	850	440	Hz
Single-Axis Average Current @ 24 Hz Sample Rate (equivalent to 3-axis @ 8 Hz)	70	135	260	µA

Footnotes:

1. Specifications are typical and subject to change. Performance specifications established with a 3.0 V supply voltage at room temperature.
2. The cycle count values (50, 100, and 200) are user-configurable and set in the Cycle Count Registers. See Section 5.1 for how to set the registers.
3. Field measurement range is defined as the monotonic region of the output characteristic curve.

Table 3-2: Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units
Analog/Digital DC Supply Voltage, AVDD & DVDD	-0.3	+3.7	VDC
Input Pin Voltage	-0.3	AVDD or DVDD	VDC
Input Pin Current @ 25C	-10.0	+10.0	mA
Storage Temperature	-40°	+85°	C

CAUTION:

Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only. Operation of the device at these or other conditions beyond those indicated in the operational sections of the specifications is not implied.

Table 3-3: Operating Conditions

Parameter	Min	Typ	Max	Units
Analog/Digital DC Supply Voltage, AVDD & DVDD[1]	2.0	3.0	3.6	VDC
Voltage Ripple on AVDD or DVDD			0.05	V_{PP}
Idle Mode Current			1	µA
Leakage Current @ DVDD pin (AVDD=AVSS=DVSS=0V, DVDD=3.6V)			100	nA
Operating Temperature	-40		+85	C

Footnote:

1. Please contact PNI if operation at <2.0 V is required.

3.2 Dimensions

Dimensions in mm
Dimensions are max. unless otherwise noted

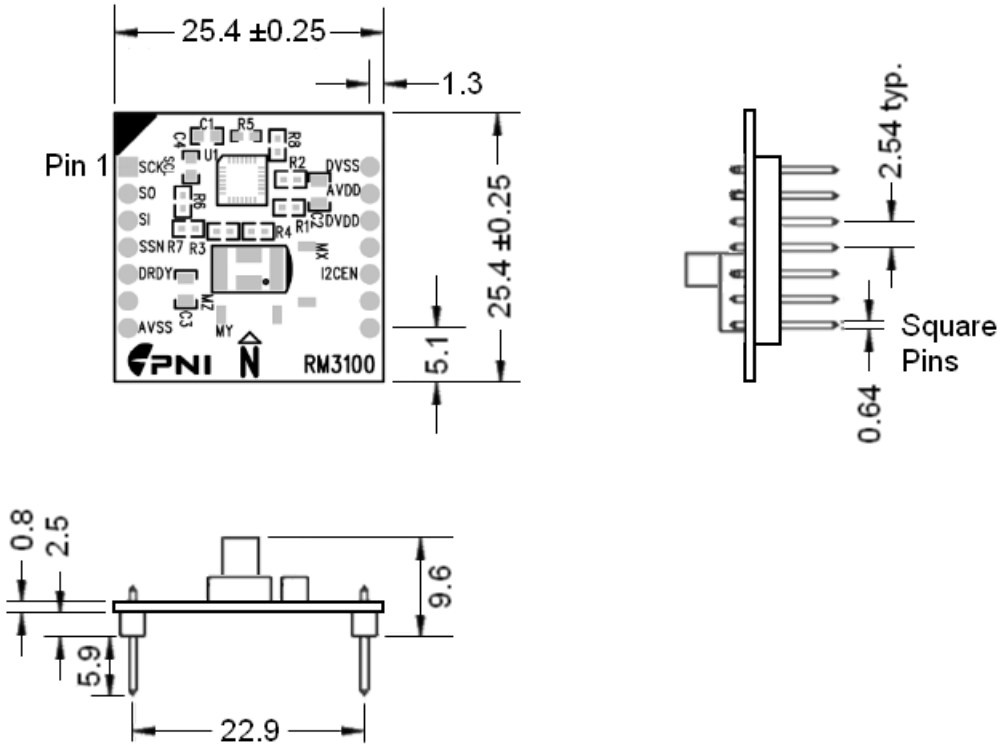


Figure 3-1: RM3100 Evaluation Board Mechanical Drawing

Note: *RM3100 3-Axis Magnetometer Breakout Board is identical to RM3100 Evaluation Board but without the header pins installed.*

4 RM3100 Testing Boards Overview & Set-Up

This section provides an overview of how to set up the RM3100 Testing Boards and the basic I^2C and SPI communications requirements. For a discussion of PNI's magneto-inductive sensor technology, please refer to either the RM3100 Geomagnetic Sensor User Manual or PNI's white paper "Magneto-Inductive Technology Overview", both of which can be found on PNI's website at www.pnicorp.com.

4.1 PCB Orientation and Output Polarities

The arrow printed on the RM3100 modules indicates the intended line-of-sight. The RM3100 modules are arranged in a north-east-down (NED) coordinate system, and the arrow is parallel to the x-axis sensor. When the module is pointing directly magnetic south, the x-axis reading will be maximized and the y-axis will be zero. In similar fashion, when the module is pointing west, the y-axis reading will be maximized and the x-axis reading will be zero. The z-axis reading will depend on the dip angle at the given location. At the geomagnetic equator, where Earth's magnetic field is horizontal, the z-axis reading will be zero when flat.

4.2 Local Magnetic Field Considerations

Because the RM3100 sensor modules measure magnetic field, it is important to consider what items in the vicinity of the module can affect the sensor readings. Note that magnetic field drops off as (1/distance^3). Specific issues to consider include:

- The sensors have a specified linear regime of ±200 μT. (Earth's field is ~50 μT.) To ensure the sensors operate in their linear regime, do not place the RM3100 close to large electric currents, large masses of ferrous material, or devices incorporating permanent magnets, such as speakers and electric motors.
- Locate the RM3100 Testing Boards away from changing magnetic fields. If this is not possible, but the local magnetic field is known to have multiple states, try to take readings only when the field is in a known state. For instance, if a motor runs part of the time, take readings only when the motor is in a known state.
- If you are uncertain about the effect a specific component may have on the system, place the RM3100 Testing Boards on a firm surface and gradually bring the component in question close to the board, then note when the magnetic field starts to change. If the component cannot be moved, then gradually move the RM3100 module toward the component, carefully ensuring that the orientation of the board remains constant while doing this.

4.3 RM3100 Testing Boards Pin Assignments

The RM3100 Testing Boards' pin assignments are summarized below in Table 4-1. Pin numbers run counterclockwise, when looking from the top, starting at the Pin 1 designator as shown in Figure 3-1.

Table 4-1: RM3100 Testing Boards Pin Assignments

Pin#	Pin Name	Description
1	SCK / SCL	SPI interface (SCK) – Serial clock input I²C interface (SCL) – Serial clock line
2	SO / SA1	SPI interface (SO) – Master Input, Slave Output I²C interface – Bit 1 of slave address
3	SI SDA	SPI interface (SI) – Master Output, Slave Input Serial Data I²C interface (SDA) – Serial Data Line
4	SSN / SA0	SPI interface – Active low to select port I²C interface – Bit 0 of slave address
5	DRDY	Status line
7	AVSS	Ground pin for analog section of ASIC
10	I2CEN	I²C enable pin (HIGH = I²C, LOW = SPI)
12	DVDD	Supply voltage for digital section of ASIC.
13	AVDD	Supply voltage for analog section of ASIC
14	DVSS	Ground pin for digital section of ASIC
6, 8, 9, 11	NC	Do not connect

4.3.1 General Purpose Pins

DVDD and AVDD (pins 12 & 13)

AVDD and DVDD should be tied to the analog and digital supply voltages, respectively. The recommend voltages are defined in

Table 3-3, and the maximum voltages are given in Table 3-2. DVDD must be on whenever AVDD is on, so DVDD should either be brought up first or at precisely the same time as AVDD. AVDD can be turned off when not making a measurement to conserve power, since all other operations are supported with DVDD. Under this condition, register values will be retained as long as DVDD is powered. Also, AVDD must be within 0.1 V of DVDD when AVDD is on.

AVSS and DVSS (pins 7 & 14)

AVSS and DVSS should be tied to the analog and digital ground, respectively. Assuming the ground plane is clean, they may share a common ground. Alternatively, they may have their own ground planes if this is more convenient. DVSS and AVSS should be within 0.1 V of each other.

DRDY (pin #5)

DRDY is used to ensure data is read from the RM3100 Testing Board only when it is available. The DRDY pin will go HIGH when the measurement is complete. This signals the host that data is ready to be read. The DRDY pin automatically is set LOW when the Measurement Result registers are read or a write operation is performed.

It is not mandatory to use the DRDY pin, as alternative methods exist to determine if data is available. Specifically, the STATUS register provides this information. And, if using the SPI interface where CPHA=CPOL=1, the MISO line also indicates if data is available when SSN is LOW.

I2CEN (pin #10)

This pin should be pulled LOW when using the SPI interface or pulled HIGH when using the I^2C interface.

4.3.2 SPI Pins

SCK (pin 1)

SCK is a SPI input used to synchronize the data sent in and out through the MISO and MOSI pins. SCK is generated by the customer-supplied master device and should be 1 MHz or less. One byte of data is exchanged over eight clock cycles. Data is captured by the master device on the rising edge of SCK. Data is shifted out and presented to the RM3100 Testing Board on the MOSI pin on the falling edge of SCK, except for the first bit (MSB) which must be present before the first rising edge of SCK.

SO (pin 2)

SO, or more commonly MISO (master input, slave output), is a SPI output transmitting data from the RM3100 Testing Board to the host. Data is transferred most significant bit first and is captured by the master device on the rising edge of SCK. The MISO pin is placed in a high impedance state if the RM3100 Testing Board is not selected (i.e. if SSN=1).

SI (pin 3)

SI, or more commonly MOSI (master output, slave input), is a SPI input providing data from the host to the RM3100 Testing Board. Data is transferred most significant bit first. Data must be presented at least 50 ns before the rising edge of SCK, and remain valid for 50 ns after the edge. New data typically is presented to the MOSI pin on the falling edge of SCK.

SSN (pin 4)

This signal sets the RM3100 Testing Board as the operating slave device on the SPI bus. The SSN pin must be LOW prior to data transfer in either direction, and must stay LOW during the entire transfer.

The SSN pin must transition from HIGH to LOW prior to reading from or writing to the registers. It must stay LOW for the remainder of the operation.

After communication between the RM3100 Testing Board and host is complete, the SPI bus can be freed (SSN set HIGH) so the host may communicate with other slave devices while the RM3100 Testing Board takes a measurement or is idle.

4.3.3 I^2C Pins

SCL (pin 1)

SCL is used to synchronize the data sent between the RM3100 Testing Board (slave) and the host system (master) on the SDA pin. SCL needs to be generated by the host system and should be 1 MHz or less. Data is captured by the master device on the rising edge of SCL. Data is shifted out and presented to the RM3100 Testing Board on the SDA pin on the falling edge of SCL, except for the first bit which must be present before the first rising edge of SCL.

SDA (pin 3)

The SDA line is a bi-directional line used to send commands between the RM3100 Testing Board (slave) and the host system (master). Data is transferred most significant bit first. All communication between the host and the RM3100 Testing Board occurs on this line when implementing the I^2C interface.

SA0 (pin 4)

SA0 represents the least significant bit in the between the RM3100 Testing Board's slave address. Pulling this HIGH represents a '1' and pulling it low represents a '0'. Along with pin 3 (bit 1) and the higher 5 bits (0b01000), which are pre-defined in

hardware, SA0 establishes the 7-bit slave address of the RM3100 Testing Board on the I^2C bus.

SA1 (pin 2)

SA1 represents the second-least significant bit in the RM3100 Testing Board's slave address. Pulling this HIGH represents a '1' and pulling it low represents a '0'. Along with pin 28 (bit 0) and the higher 5 bits (0b01000), which are pre-defined in hardware, SA1 establishes the 7-bit slave address of the module on the I^2C bus.

4.4 SPI Timing Requirements

The RM3100 Testing Boards can act as a slave device on either a SPI or I^2C bus. This section discusses basic requirements for SPI operation. The SPI interface consists of four signals, as carried on SCK, (MO)SI, (MI)SO, and SSN. The SPI clock, SCK, should run at 1 MHz or less. Data sent out on MOSI is considered valid while SCK is HIGH, and data is in transition when SCK is LOW. The first byte sent to the RM3100 Testing Boards contains the Read/Write bit (Write=0) followed by the 7-bit register address. When the register address byte is received the module returns the STATUS register contents. Assuming SSN stays low and SCK continues, multiple registers can be written to or read from, since the RM3100 Testing Boards will automatically increment to the next register address. The clock polarity when the bus is idle can either be LOW (CPOL=CPHA=0) or HIGH (CPOL=CPHA=1).

As long as SSN is LOW, data can transfer to or from the RM3100 Testing Boards. Generally it is a good idea to pull SSN to HIGH after a read or write operation has completed such that the SPI bus can be freed up for other devices. The module can perform measurements while the SSN line is HIGH, as this does not involve communication with the master. Pulling the SSN to HIGH during a data read or write will terminate the transaction.

The timing parameters, defined in Figure 4-1 or Figure 4-2 and specified in Table 4-2, must be met to ensure reliable communication.

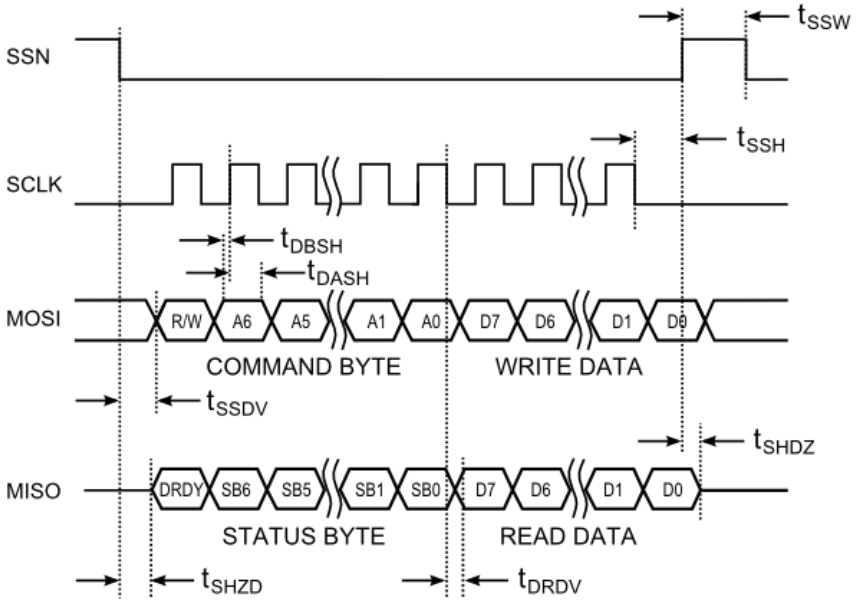


Figure 4-1: SPI Timing Diagram, CPOL = CPHA = 0

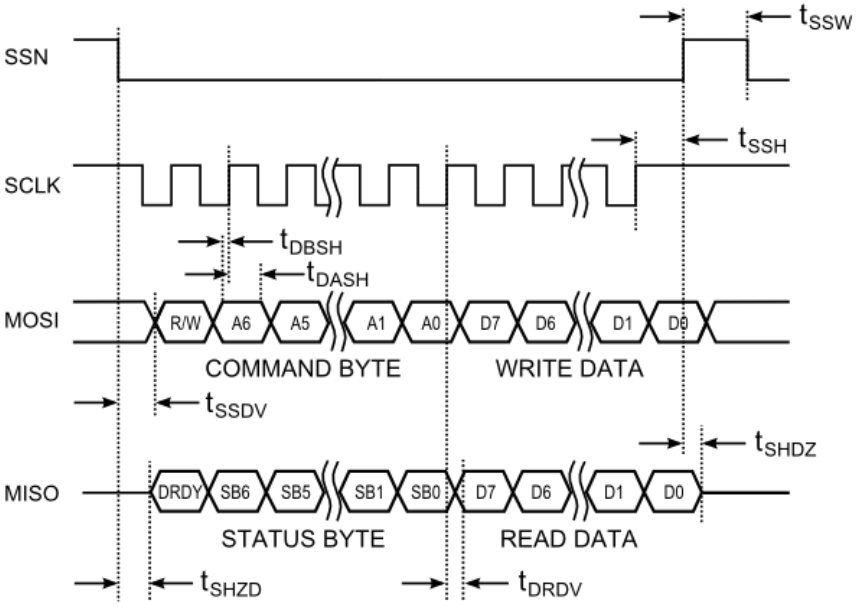


Figure 4-2: SPI Timing Diagram, CPOL = CPHA = 1

Table 4-2: SPI Timing Specifications

Symbol	Description	Min	Max	Units
t_{SHZD}	SSN LOW to data output		100	ns
t_{SSDV}	SSN LOW to Command Byte	100		ns
t_{DBSH}	Setup data before active edge	50		ns
t_{DASH}	Hold data after active edge	50		ns
t_{DRDV}	Clock falling edge to valid data		20	ns
t_{SSH}	Final clock cycle falling edge to SSN HIGH	100		ns
t_{SHDZ}	SSN HIGH to output data tri-state		100	ns
t_{SSW}	SSN HIGH to LOW (time between transactions)	100		

4.5 I²C Requirements

The RM3100 Testing Boards can operate as slave devices on either an I²C or SPI bus. This section discusses basic requirements for operation on an I²C bus. The module is identified by a 7-bit slave address, where the higher 5 bits of the slave address are pre-defined in hardware and the same for all RM3100 Testing Boards. PNI has registered these first 5 bits as 0b01000. The lower 2 bits of the slave address are user-configurable, using pins 3 and 28. As such, 4 different slave addresses are possible. For example, setting pin 3 HIGH and pin 28 LOW results in an address of 0b0100001.

The RM3100 Testing Boards' I²C interface complies with NXP's UM10204 specification and user manual, revision 03. Standard, fast, fast plus, and high speed modes of the I²C protocol are supported. Below is a link to this document.

http://www.nxp.com/documents/user_manual/UM10204.pdf

4.5.1 I²C Register Write

A generic Write transaction is given below.

START	RM3100 Testing Boards ADDRESS							RW	ACK	RM3100 Testing Boards REG. ADDRESS (N)								ACK	DATA TO REGISTER (N)								ACK	DATA TO REGISTER (N+1)								ACK	STOP
S	A6	A5	A4	A3	A2	A1	A0	0	0	A7	A6	A5	A4	A3	A2	A1	A0	0	A7	A6	A5	A4	A3	A2	A1	A0	0	A7	A6	A5	A4	A3	A2	A1	A0	0	P

From Host to RM3100 E.B.

From RM3100 E.B. to Host

---------- Data Transferred (n bytes + acknowledge) ----------

All communication is on the SDA line. The transaction is initiated by the host, or master, sending the Start condition followed by the RM3100 Testing Boards' slave address, and then the RW bit is set to '0', indicating a Write operation. The slave address is acknowledged by the module by setting SDA to LOW. This is followed by the desired 7-bit register address and then the register data. The register value automatically increments after every received data byte. The transaction is terminated by the host sending the Stop condition.

The RM3100 Testing Boards will always acknowledge the start of an I^2C Write transaction by sending a '0' (i.e. the ACK signal). But if the Write command cannot be executed for some reason, the module will send a '1' instead (i.e. the NACK signal). The reasons a NACK signal might be sent are established by the HSHAKE register, and include writing to an undefined register or writing to the POLL register while CMM is in progress, or vice versa. See Section 5.6.2 for more information.

4.5.2 I^2C Register Read

To perform a Read transaction, it is first necessary for the master to Write the desired register address, and then to Read the register data. A generic transaction is given below.

START	RM3100 Testing Boards ADDRESS							RW	ACK	REGISTER ADDRESS (N)								ACK	STOP
S	A6	A5	A4	A3	A2	A1	A0	0	0	A7	A6	A5	A4	A3	A2	A1	A0	0	P

From Host to RM3100 E.B.

From RM3100 E.B. to Host

STAR T	RM3100 Testing Boards ADDRESS							RW	ACK	DATA FROM REG. (N)								AC K	DATA FROM REG. (N+1)								NAC K	STO P
S	A6	A5	A4	A3	A2	A1	A0	1	0	A7	A6	A 5	A4	A3	A2	A1	A0	0	A7	A6	A 5	A4	A3	A2	A1	A0	1	P

---------- Data Transferred (n bytes + acknowledge) ----------

The Write sequence is described in the prior section; except for this case there is no data to send. For the Read sequence, the host again sends the RM3100 Testing Boards' slave address, but this time sets the RW bit is set to '1'. The module acknowledges that it is has been addressed and then sends data from the register address that was previously sent. The host acknowledges receipt of the data, and then the module increments the register address and sends data from this register. This continues until the host sends the NACK command followed by the Stop command, which terminates the transaction.

5 RM3100 Testing Boards Operation

The primary functions of the RM3100 Testing Boards are:

- Set the Cycle Count Registers if the default is not desired
- Initiate either a Single Measurement or Continuous Measurement
- Confirm New Data Ready
- Read the Measurement Results Registers

Each of these steps is discussed in detail in the following sections.

Note: *The RM3100 module incorporates an Idle Mode to reduce power consumption. The device is in Idle Mode when not exchanging data or taking a measurement. The module powers up into Idle Mode.*

The RM3100 Testing Boards' register map is given in Table 5-1. Register addresses are 7 bits. To Write to a register, a '0' followed by the 7-bit register number should be sent, followed by the register value. ***To Read from a register, a '1' followed by the 7-bit register number should be sent, effectively adding 0x80 to the register number.***

Table 5-1: RM3100 Testing Boards Register Map

Name	Register # (Hex)	R/W	Default (Hex)	Payload Format	Description
POLL	00	RW	00	[7:0]	Polls for a Single Measurement
CMM	01	RW	00	[7:0]	Initiates Continuous Measurement Mode
CCX	04 – 05	RW	00C8	UInt16	Cycle Count Register – X Axis
CCY	06 – 07	RW	00C8	UInt16	Cycle Count Register – Y Axis
CCZ	08 – 09	RW	00C8	Uint16	Cycle Count Register – Z Axis
TMRC	0B	RW	96	[7:0]	Sets Continuous Measurement Mode Data Rate
ALLX	0C – 0E	RW	000000	Sint24	Alarm Lower Limit – X Axis
AULX	0F – 11	RW	000000	Sint24	Alarm Upper Limit – X Axis
ALLY	12 – 14	RW	000000	Sint24	Alarm Lower Limit – Y Axis
AULY	15 – 17	RW	000000	Sint24	Alarm Upper Limit – Y Axis
ALLZ	18 – 1A	RW	000000	Sint24	Alarm Lower Limit – Z Axis
AULZ	1B – 1D	RW	000000	Sint24	Alarm Upper Limit – Z Axis
ADLX	1E – 1F	RW	0000	SInt16	Alarm Hysteresis Value – X Axis
ADLY	20 – 21	RW	0000	SInt16	Alarm Hysteresis Value – Y Axis
ADLZ	22 – 23	RW	0000	SInt16	Alarm Hysteresis Value – Z Axis
MX	24 – 26	R	000000	Sint24	Measurement Results – X Axis
MY	27 – 29	R	000000	Sint24	Measurement Results – Y Axis
MZ	2A – 2C	R	000000	Sint24	Measurement Results – Z Axis
BIST	33	RW	00	[7:0]	Built-In Self-Test
STATUS	34	R	00	[7:0]	Status of DRDY
HSHAKE	35	RW	1B	[7:0]	Handshake Register
REVID	36	R	--	Unit8	MagI^{2}C Revision Identification

5.1 Set the Cycle Count Registers (0x04 – 0x09)

The Cycle Count Registers establish the number of sensor oscillation cycles (cycle counts) that will be counted for each sensor in both the forward and reverse bias directions during a measurement sequence. Each sensor has its own cycle count value, and each can be different. Increasing the cycle count value increases measurement gain and resolution. Lowering the cycle count value reduces acquisition time, which increases maximum achievable sample rate or, with a fixed sample rate, decreases power consumption. The Cycle Count read and write addresses, plus their default values, are given in Table 5-2

Table 5-2: Cycle Count Registers

Register Description	Default Value (Hex)	Write Address (Hex)	Read Address (Hex)
X Axis Cycle Count Value - MSB	0x00	04	84
X Axis Cycle Count Value - LSB	0xC8	05	85
Y Axis Cycle Count Value - MSB	0x00	06	86
Y Axis Cycle Count Value - LSB	0xC8	07	87
Z Axis Cycle Count Value - MSB	0x00	08	88
Z Axis Cycle Count Value - LSB	0xC8	09	89

Since the registers are adjacent, it is not necessary to send multiple register addresses, as the RM3100 Testing Boards will automatically read/write to the next adjacent register.

The default values for the Cycle Count Registers are 0xC8 in the LSB and 0x0 in the MSB, or 200_D. This default value provides a good trade-off between acquisition time and resolution, but favors resolution. If the user is more interested in low power consumption or running at high data rates, a lower cycle count value of (ex. 50_D or 100_D) would be more appropriate. To estimate the appropriate cycle count value for your application, review the specifications given at 50, 100, and 200 cycle counts in Table 3-1. Note that these 3 cycle counts by no means represent all the cycle count options, as the minimum value is ‘0’ and the maximum is 65,536. However, quantization issues generally dictate working above a cycle count value of ~30, while noise limits the useful upper range to ~400 cycle counts.

Assuming a non-default cycle count value is desired, then it is necessary to Write values to the Cycle Count Registers prior to sending a command to take a sensor measurement. Once the Cycle Count Registers are set, they do not need to be repopulated unless the user wants to change the values or the system is powered down, in which case the default value repopulates the register fields when powered up again.

5.2 Initiate Continuous Measurement Mode (0x01)

The RM3100 Testing Boards can either take measurements automatically on a regular frequency (Continuous Measurement Mode) or by polling for single measurement. This section discusses Continuous Measurement Mode. See Section 5.3 for polling for a single measurement.

To initiate Continuous Measurement Mode, write to the CMM register address, 0x01, followed by the CMM register contents. To set the rate of data acquisition in Continuous Measurement Mode, see Section 5.2.1. Below are the contents of the CMM register.

Bit #	7	6	5	4	3	2	1	0
Value	LDM	CMZ	CMY	CMX	DRDM1	DRDM0	ALARM	START

Where:

- START – A “1” in this bit position initiates Continuous Measurement Mode. To turn off Continuous Measurement Mode it is necessary to write a “0” to this bit position. Note that writing to POLL (i.e., initiating a single measurement command) while operating in Continuous Measurement Mode results in the single measurement command being ignored.
- ALARM – A feature of the RM3100 Testing Boards while operating in Continuous Measurement Mode is that the ALARM bit will go HIGH if a measurement reading is outside a predefined range of values, set by the Alarm Upper and Lower Limit Registers. This bit is set to ‘1’ if a limit is exceeded. The ALARM bit is reset by writing a ‘0’ to this bit. See Section 5.2.2 for additional information.
- DRDM – These two bits establish the required condition to trigger the DRDY pin to HIGH. There are 4 possible conditions, as set out in Table 5-3.

Table 5-3: Continuous Mode DRDY Options

DRDY Requirements	DRDM1	DRDM0
DRDY to HIGH when ALARM = 1, AND a full measurement sequence is completed, as established by CMX, CMY, and CMZ.	0	0
DRDY to HIGH after the completion of a measurement on any axis.	0	1
DRDY to HIGH after a full measurement sequence is completed, as established by CMX, CMY, and CMZ.	1	0
DRDY to HIGH when Alarm = 1.	1	1

- CMX, CMY, CMZ – A "1" in either of these three bit positions indicates a measurement will be taken on that sensor axis when operating in Continuous Measurement Mode. For instance, to take measurements on all three axis, CMX = CMY = CMZ = 1.
- LDM – This bit indicates whether Absolute or Relative Alarm Mode is being implemented. A "0" indicates Absolute Alarm Mode, while a "1" indicates Relative Alarm Mode. See Section 5.2.2 for additional information.

To read from the CMM register, send 0x81. The return byte will provide the same information as above, specifically indicating if ALARM is HIGH.

Note: *Certain commands, such as reading from the CMM register or writing to the TMRC register, will stop Continuous Measurement Mode.*

5.2.1 Setting the CMM Update Rate with TMRC (0x0B)

The time between measurements in Continuous Measurement Mode is established with the TMRC register. The TMRC register is defined below.

Bit #	7	6	5	4	3	2	1	0
Value	1	0	0	1	TMRC3	TMRC2	TMRC1	TMRC0

The LSB is used set the CMM update rate. The MSB should be 0x9, as indicated above. The larger the TMRC value, the longer the interval between measurements. Available data rates are given in Table 5-4. Note that the update rates are approximate, and have a one standard deviation tolerance of about ~7%. The default value for TMRC is 0x96, establishing a data update rate of ~37 Hz.

To set the TMRC register, send the register address, 0x0B, followed by the desired TMRC register value. To read the TMRC register, send 0x8B.

Note: *The Cycle Count Registers establish the maximum data rate of the sensors. For instance, if the cycle count is set to 200_D, then the maximum single-axis update rate is ~430 Hz. If TMRC is set to 0x92, indicating an update rate of ~600 Hz, the rate established by the cycle count will override the TMRC request, and the actual update rate will be ~430 Hz.*

Table 5-4: CMM Update Rates

TMRC Value (Hex)	Time Between Readings	Update Rate
92	~1.7 ms	~600 Hz
93	~3 ms	~300 Hz
94	~7 ms	~150 Hz
95	~13 ms	~75 Hz
96	~27 ms	~37 Hz
97	~55 ms	~18 Hz
98	~110 ms	~9 Hz
99	~220 ms	~4.5 Hz
9A	~440 ms	~2.3 Hz
9B	~0.8 s	~1.2 Hz
9C	~1.6 s	~0.6 Hz
9D	~3.3 s	~0.3 Hz
9E	~6.7 s	~0.015 Hz
9F	~13 s	~0.075 Hz

5.2.2 Alarm Mode

The RM3100 Testing Boards incorporate an Alarm Mode feature that sets the ALARM bit to “1” in the CMM register whenever measurement results exceed an established limit. This feature can be particularly useful for applications where the user’s device is briefly waking up to take a magnetic field measurement reading and trying to determine if the field has changed in an appreciable manner.

This is an optional feature and does not need to be implemented. To disable the feature, the Alarm Lower Limit and Alarm Upper Limit register values should be `“0”, which are the defaults.

There are two types of limits, Absolute and Relative. The LDM bit in the CMM register establishes which type will be used, where "0" indicates Absolute and "1" indicates Relative. In Absolute Alarm Mode, the limits are fixed and do not change, while in Relative Alarm Mode the limits change whenever the current Alarm Limits are exceeded. As the name suggests, Absolute Alarm Mode is used for monitoring the absolute magnetic field, while Relative Alarm Mode is used to monitor changes in magnetic field.

Absolute Alarm Mode

In Absolute Alarm Mode the limits are set for each axis by the Alarm Lower Limit and Alarm Upper Limit registers, as given in Table 5-5. The register values are unsigned integers. The ALARM bit will go HIGH if the measured value (MX, MY, or MZ) on any given axis is either greater than the Alarm Upper Limit for that axis or less than the Alarm Lower Limit for that axis. This is an "OR" function, looking at both the Alarm Upper and Lower Limits, and looking at all sensors being measured.

Table 5-5: Alarm Lower and Upper Limit Registers

Register Description	Register Name	Read (Hex)	Write (Hex)
X Axis Alarm Lower Limit - MSB	ALLX2	8C	0C
X Axis Alarm Lower Limit - mid	ALLX1	8D	0D
X Axis Alarm Lower Limit - LSB	ALLX0	8E	0E
X Axis Alarm Upper Limit - MSB	AULX2	8F	0F
X Axis Alarm Upper Limit - mid	AULX1	90	10
X Axis Alarm Upper Limit - LSB	AULX0	91	11
Y Axis Alarm Lower Limit - MSB	ALLY2	92	12
Y Axis Alarm Lower Limit - mid	ALLY1	93	13
Y Axis Alarm Lower Limit - LSB	ALLY0	94	14
Y Axis Alarm Upper Limit - MSB	AULY2	95	15
Y Axis Alarm Upper Limit - mid	AULY1	96	16
Y Axis Alarm Upper Limit - LSB	AULY0	97	17
Z Axis Alarm Lower Limit - MSB	ALLZ2	98	18
Z Axis Alarm Lower Limit - mid	ALLZ1	99	19
Z Axis Alarm Lower Limit - LSB	ALLZ0	9A	1A
Z Axis Alarm Upper Limit - MSB	AULZ2	9B	1B
Z Axis Alarm Upper Limit - mid	AULZ1	9C	1C
Z Axis Alarm Upper Limit - LSB	AULZ0	9D	1D

Since the registers are adjacent, it is not necessary to send multiple register addresses, as the RM3100 Testing Boards automatically will read/write to the next adjacent register.

Relative Alarm Mode

In Relative Alarm Mode the limits for each axis initially are set by the Alarm Lower Limit and Alarm Upper Limit value registers, as given in Table 5-5, similar to Absolute Alarm Mode. However, when the ALARM bit is triggered and set HIGH, the limit values are changed using the Alarm Hysteresis Values, given in Table 5-6.

Table 5-6: Alarm Hysteresis Registers

Register Description	Register Name	Read (Hex)	Write (Hex)
X Axis Alarm Hysteresis - MSB	ADLX1	9E	1E
X Axis Alarm Hysteresis - LSB	ADLX0	9F	1F
Y Axis Alarm Hysteresis - MSB	ADLY1	A0	20
Y Axis Alarm Hysteresis - LSB	ADLY0	A1	21
Z Axis Alarm Hysteresis - MSB	ADLZ1	A2	22
Z Axis Alarm Hysteresis - LSB	ADLZ0	A3	23

Since the registers are adjacent, it is not necessary to send multiple register addresses, as the RM3100 Testing Boards will automatically read/write to the next adjacent register.

The new lower and upper limit values are defined as follows:

$$AUL = M + ADL$$

$$ALL = M - ADL$$

Where AUL and ALL represent the new lower and upper limit register values, M is the measured value that caused the ALARM bit to go HIGH, and ADL is the Alarm Hysteresis Value.

Example of Absolute vs. Relative Alarm Modes

Table 5-7 provides an example of how the Absolute and Relative Alarm Modes work under the same conditions. This is for illustrative purposes, and the MX readings would depend on many things including the cycle count value and the magnetic field.

In this case only the X axis sensor is being monitored, the ALLX register is set to 0x0A00, the AULX register is set to 0x1000, and the ADLX register is set to 0x0100.

Table 5-7: Absolute vs. Relative Alarm Mode Example

State Description	MX	Absolute Alarm Mode			Relative Alarm Mode		
		UL	LL	ALARM bit	UL	LL	ALARM bit
Initial State & Measure	0x0F00	0x10000	0x0A00	0	0x10000	0x0A00	0
Perturbation Applied & Measure	0x1100	0x10000	0x0A00	1	0x10000	0x0A00	1
Measure Again	0x1100	0x10000	0x0A00	1	0x12000	0x1000	0
Measure Again	0x1100	0x10000	0x0A00	1	0x12000	0x1000	0
Remove Perturbation & Measure	0x0F00	0x10000	0x0A00	0	0x12000	0x1000	1
Measure Again	0x0F00	0x10000	0x0A00	0	0x10000	0x0A00	0
Measure Again	0x0F00	0x10000	0x0A00	0	0x10000	0x0A00	0

5.3 Initiate a Single Measurement (0x00)

The RM3100 Testing Boards can operate in either a continuous measurement mode or a polling mode. This section discusses the Single Measurement Command used in a polling mode. See Section 5.2 for operation in continuous measurement mode.

To make a single measurement, it is necessary to send the Single Measurement Command byte to the POLL register, 0x00. This byte establishes which axes are to be measured. It is defined as follows, where a “1” for PMX, PMY, and/or PMZ indicates the X, Y, and/or Z axis, respectively, is to be measured. Note that the DRDY line will go HIGH after all measurements requested in the Single Measurement Command byte have been completed.

Bit #	7	6	5	4	3	2	1	0
Value	0	PMZ	PMY	PMX	0	0	0	0

5.4 Confirm New Data Ready

There are several ways to determine if a measurement has been completed and data is available in the Measurement Results Registers. One method is monitoring the DRDY line

for it to go HIGH. Recall that for continuous measurement mode, the DRDM bits of the Continuous Measurement Command byte establish the conditions for DRDY to go HIGH. Another option when using the SPI interface is monitoring the MISO pin for it to go HIGH. (The MISO pin is unavailable when using the I^2C interface, as it is used to set the slave address of the device.) Another option is to read from the STATUS register, as discussed below. Only one method need be used.

5.4.1 STATUS Register (0x34)

To read the Status Register, first send a read command to the STATUS register, 0xB4.

The return byte provides the contents of the Status Register:

Bit #	7	6	5	4	3	2	1	0
Value	DRDY	-	-	-	-	-	-	-

Bit 7 will be HIGH if data is available and LOW if it is unavailable. Bits 0 – 6 are indeterminate and should be ignored.

5.5 Read the Measurement Results

Each sensor reading consists of 3 bytes of data which are stored in 2's complement format (range: -8388608 to 8388607) in the Results Registers within the RM3100 Testing Boards. These registers are read by sending the Read Results byte, as defined below, where the values of A, B, C, and D establish the register to be addressed, as given in Table 5-8.

Bit #	7	6	5	4	3	2	1	0
Value	1	0	1	0	A	B	C	D

Table 5-8: Measurement Results Registers

Register Description	Write Address (Hex)	Read Address (Hex)
X Axis Measurement (2)	24	A4
X Axis Measurement (1)	25	A5
X Axis Measurement (0)	26	A6
Y Axis Measurement (2)	27	A7
Y Axis Measurement (1)	28	A8
Y Axis Measurement (0)	29	A9
Z Axis Measurement (2)	2A	AA
Z Axis Measurement (1)	2B	AB
Z Axis Measurement (0)	2C	AC

Normally it is only necessary to send "$A4_H$", since the register value automatically increments on the clock cycles such that after sending "$A4_H$" all 3 bytes for the X axis measurement would be clocked out, then the 3 bytes for the Y axis measurement, then the 3 bytes for the Z axis measurement. After these 9 bytes have been clocked out, the subsequent output data has no relevance.

5.6 Troubleshooting and General Information

The RM3100 Testing Boards incorporates several registers that can be used to help troubleshoot the system or device. These include the Built-In Self-Test (BIST) register, the Handshake register, and the RevID register.

5.6.1 BIST Register (0x33)

The BIST register checks the status of the internal LR circuit oscillator. Write to the BIST register by sending 0x33 followed by the BIST register values, and request a read from the BIST register by sending 0xB3. The register contents are defined below.

Bit #	7	6	5	4	3	2	1	0
Value	STE	ZOK	YOK	XOK	BW1	BW0	BP1	BP0

Where:

- STE – Setting this to ‘1’ commands the RM3100 Testing Boards to run the built-in self-test when the POLL register is written to. The end of the built-in self-test sequence will be indicated by DRDY going HIGH.
- ZOK, YOK, and XOK – These read-only bits indicate whether or not the X, Y, and Z LR oscillators functioned correctly during the built-in self-test. A ‘1’ indicates a properly function oscillator. Note that STE also should be HIGH when this is read; or the reading is invalid.
- BW – These two bits define the timeout period for the LR oscillator periods, as given in Table 5-9.

Table 5-9: BIST Timeout Period

BIST Wait Time	BW1	BW0
Unused	0	0
1 Sleep Oscillation Cycle (30 µs)	0	1
2 Sleep Oscillation Cycles (60 µs)	1	0
4 Sleep Oscillation Cycles (120 µs)	1	1

- BP – These two bits define the number of LR periods for measurement during the built-in self-test, as given in Table 5-10.

Table 5-10: BIST LR Periods

BIST LR Periods	BW1	BW0
Unused	0	0
1 LR Period	0	1
2 LR Periods	1	0
4 LR Periods	1	1

5.6.2 HSHAKE Register (0x35)

The HSHAKE register is used to set conditions for clearing the DRDY pin and for determining why a register command was not fulfilled. Write to the HSHAKE register by sending 0x35 followed by the BIST register values, and request a read from the HSHAKE register by sending 0xB5. The register contents are defined below.

Bit #	7	6	5	4	3	2	1	0
Value	0	NACK2	NACK1	NACK0	1	0	DRC1	DRC0

Where:

- DRC0 – Setting this to ‘1’ means DRDY is cleared by any device register write. Clearing occurs during reception of the register address byte for the write transaction on either the SPI or I^2C interface. This is the default setting.
- DRC1 – Setting this to ‘1’ means DRDY is cleared by reading the Measurement Results registers. Clearing occurs when the RM3100 Testing Boards sends back the first byte of data. This is the default setting.
- NACK0 – This read-only bit is set to ‘1’ when writing to an undefined register.
- NACK1 – This read-only bit is set to ‘1’ when writing into POLL when CMM is in progress or when writing to CMM when POLL is in progress.
- NACK2 – This read-only bit is set to ‘1’ when a read for the Measurement Results registers is requested but data is not ready (DRDY = 0).

5.6.3 REVID Register (0x36)

The REVID register provides revision identification of the MagI^2C ASIC. This is a single byte, read-only register. To read the REVID register, send 0xB6.

5.7 Examples using the SPI Interface

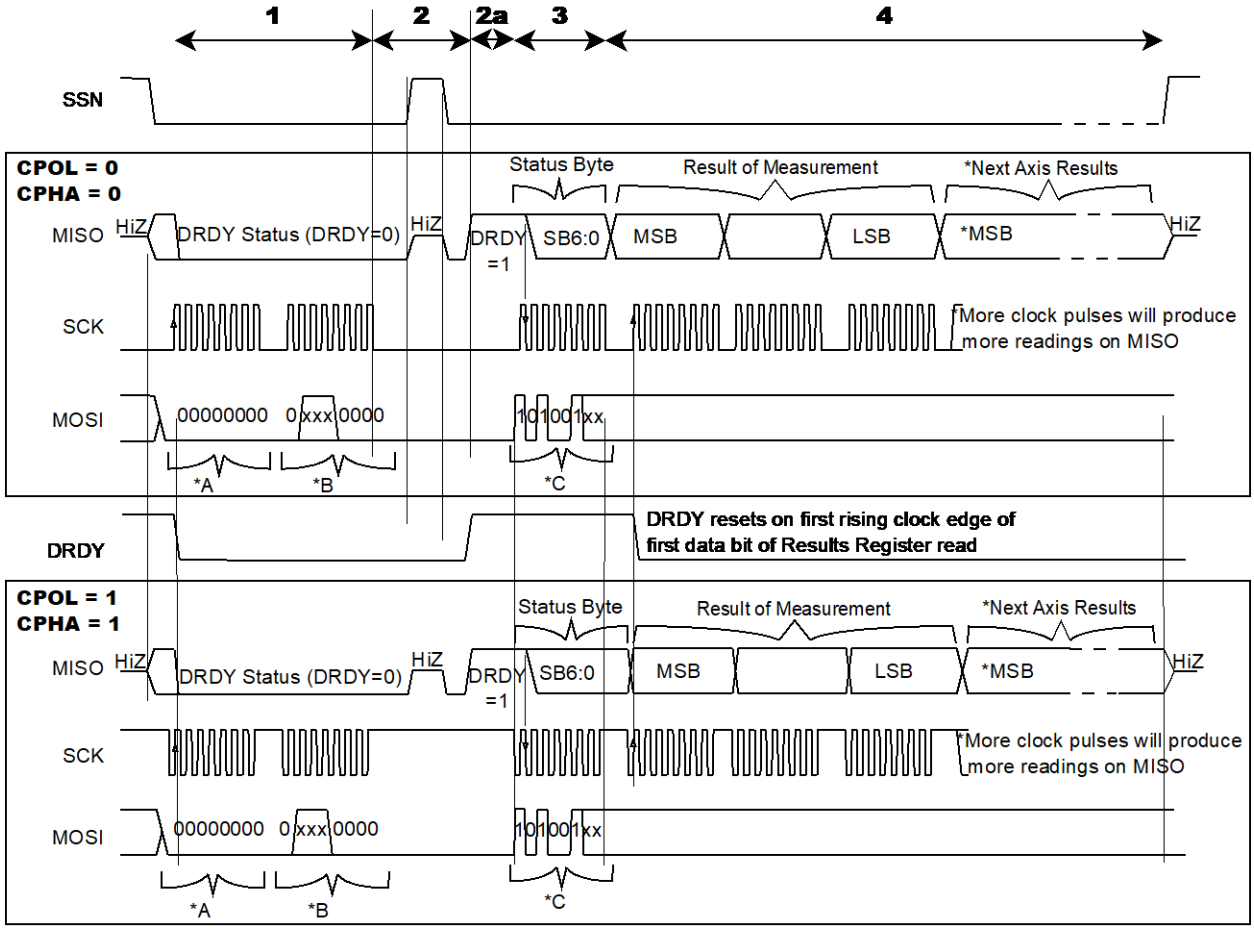
5.7.1 Set the Cycle Count Registers

A sample command sequence is provided below to set the cycle count value to 100_D (64_H) for all 3 axes. This is purely for illustrative purposes; the value could be different and/or the number of axes to be addressed could be different.

- Start with SSN set HIGH, then set SSN to LOW.
- Send 04_H (this is the Write Command Byte to address the MSB for the X axis)
- Send 0 (value for the MSB for the X axis)
- Send 64_H (value for the LSB for the X axis - pointer automatically increments)
- Send 0 (value for the MSB for the Y axis - pointer automatically increments)
- Send 64_H (value for the LSB for the Y axis - pointer automatically increments)
- Send 0 (value for the MSB for the Z axis - pointer automatically increments)
- Send 64_H (value for the LSB for the Z axis - pointer automatically increments)
- Set SSN to HIGH

5.7.2 Making and Reading Measurements

Figure 5-1 gives the SPI activity sequence for initiating a single measurement and reading the results. While the RM3100 Testing Boards are designed for CPOL = 0 and CPHA = 0 operation, they also can operate with CPOL = 1 and CPHA =1, so both cases are given. The assumption in the diagram is that the DRDY pin or the MISO line is used to establish when data is ready, but a query of the Status Register could be used instead. SPI timing requirements are discussed in Section 4.4.



1) Host writes to MAG register (*A) with measurement parameters (*B). MAG register Address = 0x00.
2) Host waiting for measurement to complete by reading the dedicated DRDY pin or DRDY status bit on the MISO pin
   2a) Host response time from DRDY
3) Host Adresses QX,QY or QZ register (*C >=0x24) for measurement results
4) Host Reads measurement results

Figure 5-1: SPI Activity Sequence Diagram

The steps to make measurements in Continuous Measurement Mode are given below.

- Start with SSN set HIGH, then set SSN to LOW.
- Initiate Continuous Measurement Mode by writing to the CMM register address, 0x01, followed by the CMM register value. This value defines which axes are to be measured, how the DRDY line will be set HIGH, and which type of Alarm will be implemented assuming the Alarm feature is being utilized. Assuming all 3 axes are to be measured, DRDY goes HIGH after completing measurements on all axes, and the Alarm feature is not utilized, the CMM value would be 0x79.
- The RM3100 Testing Board will now initiate Continuous Measurement Mode.
- Return SSN to HIGH. This will not affect the measurement process, but will free up the host to communicate with other devices and ensure the next Write command sent to the module is interpreted properly.
- Once the measurement sequence is completed on all axes, the MISO pin goes low and the DRDY pin is set HIGH, assuming 0x79 is the CMM register value. The module will be placed in Idle Mode until it is time to take another measurement, as defined by the TMRC register.
- When the host is ready to read the measured values, set SSN to LOW. If SSN already is LOW, then toggle SSN from LOW to HIGH to LOW.
- Assuming the X axis was one of the axes to be measured, send the MX2 Read address, 0xA4, to begin reading the Measurement Results registers. The measurement readings will now clock out, with the 3 bytes of X-axis data presented first, then Y-axis data, then Z-axis data. The first nine (9) bytes represent a complete 3-axis measurement. This will clear the DRDY line.
- Return SSN to HIGH to free up the host to communicate with other devices and to ensure the next Command Byte sent to the module is interpreted properly.

The steps to make a single measurement are given as follows.

- Start with SSN set HIGH, then set SSN to LOW.
- Initiate a single measurement by writing to the POLL register address, 0x00, followed the register address with either the POLL register value. This defines which axes are to be measured, and should be 0x70 if measurements on all three axes are desired.
- The MagI^2C will now take the prescribed measurements.
- Return SSN to HIGH. This will not affect the measurement process, but will free up the host to communicate with other devices and ensure the next Write command sent to the MagI^2C is interpreted properly.

- Once the measurement sequence is completed on all desired axes, the DRDY pin is set HIGH and the MISO pin goes low, indicating data is read. The MagI^{2}C is placed in Idle Mode.
- When the host is ready to read the measured values, set SSN to LOW. If SSN already is LOW, then toggle SSN from LOW to HIGH to LOW.
- Assuming the X axis was one of the axes to be measured, send the MX2 Read address, 0xA4, to begin reading the Measurement Results registers. The measurement readings will now clock out, with the 3 bytes of X-axis data presented first, then Y-axis data, then Z-axis data. The first nine (9) bytes represent a complete 3-axis measurement.
- Return SSN to HIGH to free up the host to communicate with other devices and to ensure the next Command Byte sent to the module is interpreted properly.

5.8 Examples using the I^{2}C Interface

5.8.1 Set the Cycle Count Registers

A sample command sequence is provided below that sets the cycle count value to 100_D (64_H) for all 3 axes. This is for illustrative purposes; the value could be different and/or the number of axes to be addressed could be different. Note that only the initial Cycle Count register address needs to be sent, as the RM3100 Testing Board automatically increments to the next register.

START	RM3100 Testing Board ADDRESS							RW	ACK	CCX1 REG. ADDRESS (N)								ACK	DATA TO CCX1 REG (N)								ACK	DATA TO CCX0 REG (N+1)								ACK
S	0	1	0	0	0	X	X	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0

From Host to RM3100 E.B.

From RM3100 E.B. to Host

DATA TO CCY1 REG (N+2)								ACK	DATA TO CCY0 REG (N+3)								ACK	DATA TO CCZ1 REG (N+4)								ACK	DATA TO CCZ0 REG (N+5)								ACK	STOP
0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	P

5.8.2 Initiate a Single Measurement

The I^2C transactions to initiate a single measurement on all 3 axes are given below.

START	RM3100 Testing Boards ADDRESS							RW	ACK	POLL REG. ADDRESS (N)								ACK	DATA TO POLL REG (N)								ACK	STOP
S	0	1	0	0	0	X	X	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	P

From Host to RM3100 E.B.

From RM3100 E.B. to Host

After this transaction sequence the RM3100 Testing Board will initiate a measurement sequence; this can run in the background. At the end of the measurement sequence the DRDY pin is set HIGH and the Status Register will have a "1" in bit 7, indicating data is ready. The module will be placed in Idle Mode.

5.8.3 Initiate Continuous Measurement Mode

A sample I^2C transaction to initiate continuous measurement mode is given below.

START	RM3100 Testing Boards ADDRESS							RW	ACK	CMM REG. ADDRESS (N)								ACK	DATA TO CMM REG (N)								ACK	STOP
S	0	1	0	0	0	X	X	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	1	0	0	1	0	P

From Host to RM3100 E.B.

From RM3100 E.B. to Host

In this example, the CMM register is set to initiate measurements on all 3 axes, and to set DRDY to HIGH after all three measurements are made.

5.8.4 Read the Measurement Results

When the host is ready to read the Measurement Results registers, the following transactions should occur. Note that only the initial Measurement Results register address needs to be sent, as the module automatically increments to the subsequent registers.

START	RM3100 Testing Boards ADDRESS							RW	ACK	MX2 ADDRESS (N)								ACK	STOP
S	0	1	0	0	0	X	X	0	0	0	0	1	0	0	1	0	0	0	P

From Host to RM3100 E.B.

From RM3100 E.B. to Host

START	RM3100 Testing Boards ADDRESS							RW	ACK	DATA FROM MX2 (N)								ACK	DATA FROM MX1 (N+1)								ACK
S	0	1	0	0	0	X	X	1	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	0

DATA FROM MX0 REG (N+2)								ACK	DATA FROM MY2 REG (N+3)								ACK	DATA FROM MY1 REG (N+4)								ACK	DATA FROM MY0 REG (N+5)								ACK
X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	0

DATA FROM MZ2 REG (N+6)								ACK	DATA FROM MZ1 REG (N+7)								ACK	DATA FROM MZ0 REG (N+8)								NACK	STOP
X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	0	P

The final NACK is optional, as communication will stop by simply implementing the Stop condition.