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Work

Test Engineer I **Jabil Circuit**, San Jose, CA Spring 2019 - Present

- ☐ Design and develop a tab completer framework for the Python REPL to use in building completers that improve technicians' debug workflow and operator on-boarding process
- ☐ Build a Continuous Delivery pipeline for internal tools to get faster iterations
- ☐ Training in *Design For Testing* for electronics mass manufacturing

Test Engineering Intern **Jabil Circuit**, San Jose, CA Summer 2018

- ☐ End to end development of a tool for live analysis of internal test and debugging data
- ☐ Design and develop a failure resistant *testcell grid* data aggregator, backend and a simple frontend
- ☐ For high impact in workcell efficiency, selected for competition: *Jabil - Design Best Practices* (ongoing)
- ☐ *Experience with:* Golang, Python, MySQL, JS/React

Gradudate Research Assistant **Computer Science, Purdue** Spring 2017–Spring 2018

- ☐ *Worked on:* 3-way merging data structures research project
- ☐ *Workshop paper:* Mergeable Types, ML Workshop, 2017
- ☐ *Experience with:* OCaml, Git internals, Database Consistency

Teaching Assistant **Computer Engineering, Purdue** Spring 2015

- ☐ *Course:* Computer Design and Prototyping (ECE437)
- ☐ Assist students in benchmarking, analyzing performance and taking design decisions to develop a multicore pipelined MIPS processor
- ☐ *Experience with:* Verilog, Python, Logic synthesis targeting FPGA

Student Software Developer **Krannert Computing, Purdue** Summer 2012–Fall 2016

- ☐ *Worked with a team on:* Backend and frontend for web and desktop applications
- ☐ CV Parser, Job Queue, Calendar Application, Course Content aggregator. ...
- ☐ Mentor new students on coding standards, best practices and version control
- ☐ *Experience with:* C#, MSSQL, Regex, XML/XSLT, HTML/CSS/JS, MVC, TFS

Education

MSc Computer Science **Purdue**, West Lafayette, IN Spring 2016–*Fall 2018*

- ☐ *Courses:* Distributed systems, Advanced database systems (Relational and non-relational), Programming Language Theory, Algorithm design and analysis

BSc Computer Engineering **Purdue**, West Lafayette, IN Fall 2011–Spring 2015

- ☐ *Courses:* Circuit analysis, Computer design and prototyping, Signals and systems, Data structures and algorithms, Discrete Mathematics, Advanced C, Intro to AI, Intro to Infosec, Compilers, Operating Systems

Notable projects

Mergeable Types *ocaml* https://github.com/sransara/mtypes-lib

- ☐ Extend Okasaki's Purely functional data structures with 3-way merge operations

Distributed Key-Value Store *java* https://github.com/sransara/kvs-transactions

- ☐ Key level granular multi key transactions, 2PL/2PC concurrency control, Strong consistency

Micro Language Compiler *java* https://github.com/sransara/microbe-lang

- ☐ Implement Register allocation, IR generation, Control flow graph analysis and a VM to run the serialized IR

Multicore MIPS processor *verilog* https://github.com/sransara/aww-processor

- ☐ Develop a multicore processor for MIPS instruction set architecture optimized for synthesis

Other

- ☐ Recognized in hall of fame as reward recipient for disclosure of XSS bugs in Gmail: 2012 July, 2012 October
- ☐ Awarded bronze medal at International Junior science olimpiad, Baku, Azerbaijan: 2009