EVD310 VLSI Design
Monsoon 2020
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Project Documentation

1. Introduction

The objective of this project was to implement a boolean equation using combinational circuits. First we simplified the given boolean equation [F = $(\overline{A} + \overline{B})$(C + D)] using De Morgan's laws, prepared the truth table and then implemented the resultant equation [F = (A B) + $(\overline{C}\,\overline{D})$] using tools like Electric VLSI and LTSpice. Using Electric VLSI we made the schematic and layout diagrams for the boolean equation and then simulated the final output in LTSpice.

2. Introduction to Combinational Circuits

Combinational circuits are basic building blocks of all digital systems. They generally consist of NAND, NOR and NOT gates. The defining characteristics of combinational circuits are

a. Having no memory
b. Having no clock
c. Having no feedback.

Having no memory means that combinational circuits do not remember any past inputs. Having no clock makes the circuit a time independent circuit. Lastly, lack of feedback is due to non usage of previous output states as inputs. All these characteristics make a combinational circuit operation instantaneous.

Functions of the combinational logic circuit can be specified using

a. Boolean algebra
b. Truth table

c. Logic diagram.

3. Introduction to Tools

ELECTRIC:

The Electric VLSI Design System is a free to use EDA tool written completely in Java in the early 1980s by Steven M. Rubin. Electric is used to draw schematics and to do integrated circuit layout. It can also handle hardware description languages such as VHDL and Verilog. The system has many analysis and synthesis tools, including Design rule checking, Simulation, Routing, Layout vs. Schematic, Logical Effort, and more. Here it was used to design the schematic and the layout of the combinational circuit of the assigned boolean expression.

LTspice:

LTspice is Analog Devices' high performance circuit simulation program, which allows you to draft, probe, and analyze the performance of your circuit design. It contains an integrated schematic editor, waveform viewer, and advanced features that are easy to use after learning some basic commands. In this project, LTSpice was used to simulate the output waveforms for the given boolean equation.

4. Equations and Truth Table

Assigned equation:

$F = (\overline{A} + \overline{B})(C + D)$

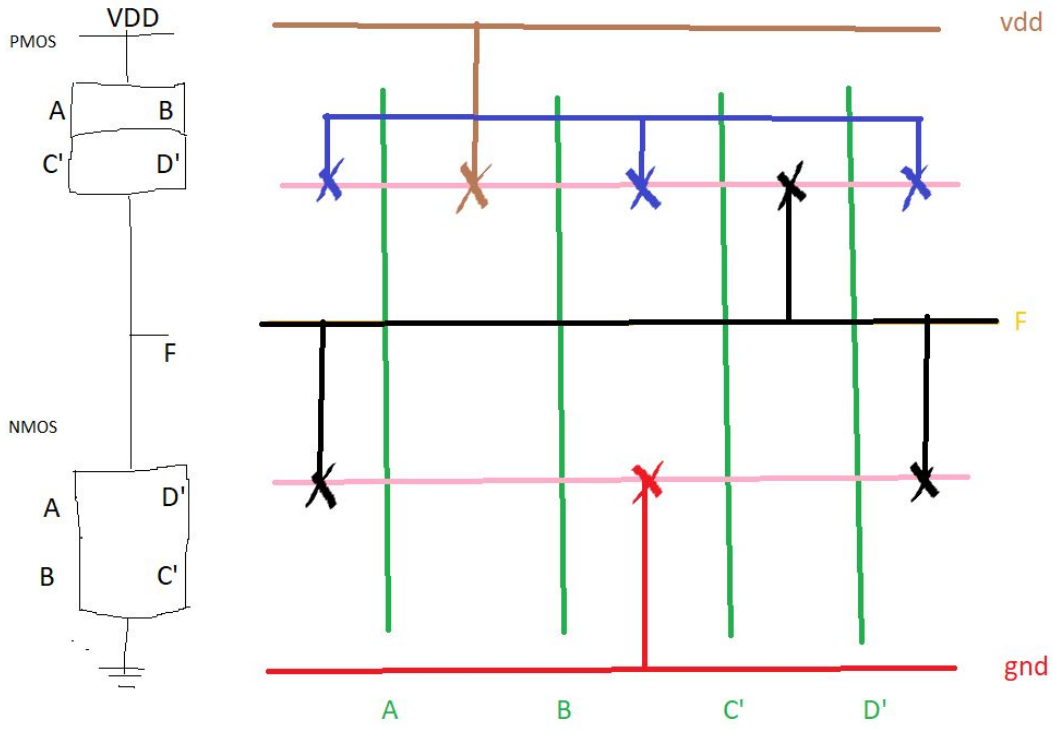
$= \overline{\overline{(\overline{A} + \overline{B})\,(C + D)}}$ (∵ **De Morgan's laws**)

$= \overline{(\overline{A} + \overline{B})} + \overline{(C + D)}$

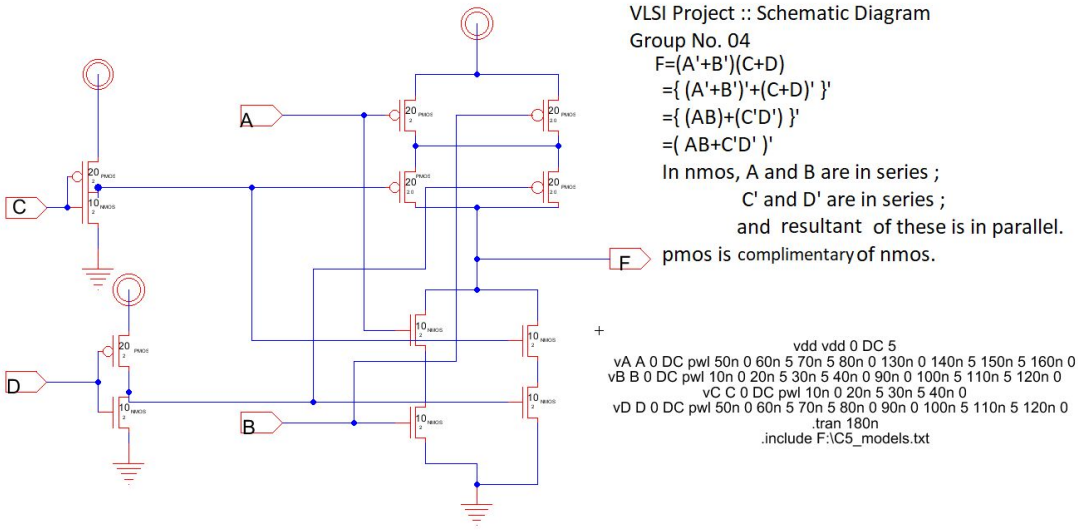
$= (A\,B) + \overline{(C\,\overline{D})}$

A	B	C	D	F= (A B) + $\overline{(C\ D)}$	F = $\overline{(A} + \overline{B}$)(C + D)
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	1	1
0	0	1	1	1	1
0	1	0	0	0	0
0	1	0	1	1	1
0	1	1	0	1	1
0	1	1	1	1	1
1	0	0	0	0	0
1	0	0	1	1	1
1	0	1	0	1	1
1	0	1	1	1	1
1	1	0	0	0	0
1	1	0	1	0	0
1	1	1	0	0	0
1	1	1	1	0	0

Stick Diagram:

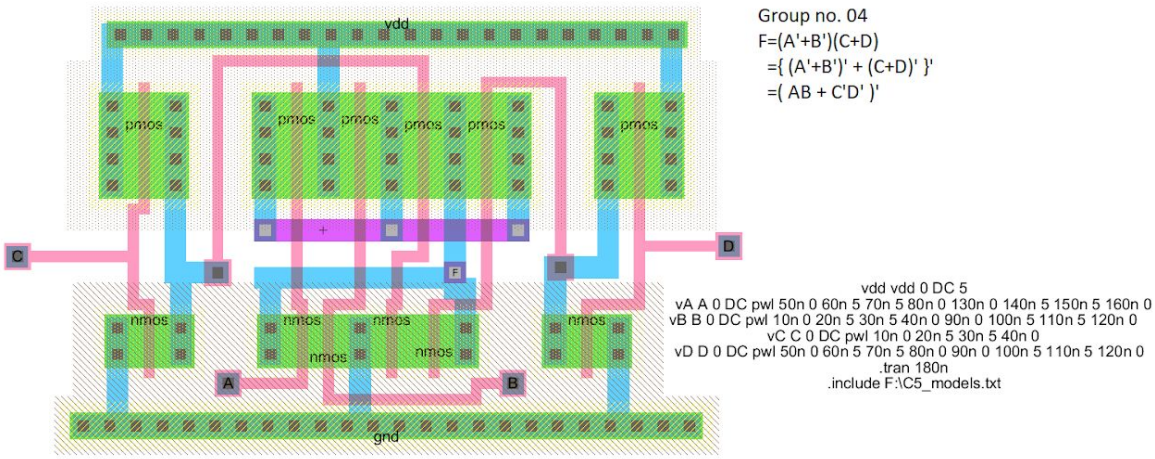


5. Schematic Circuit



12 transistors used.

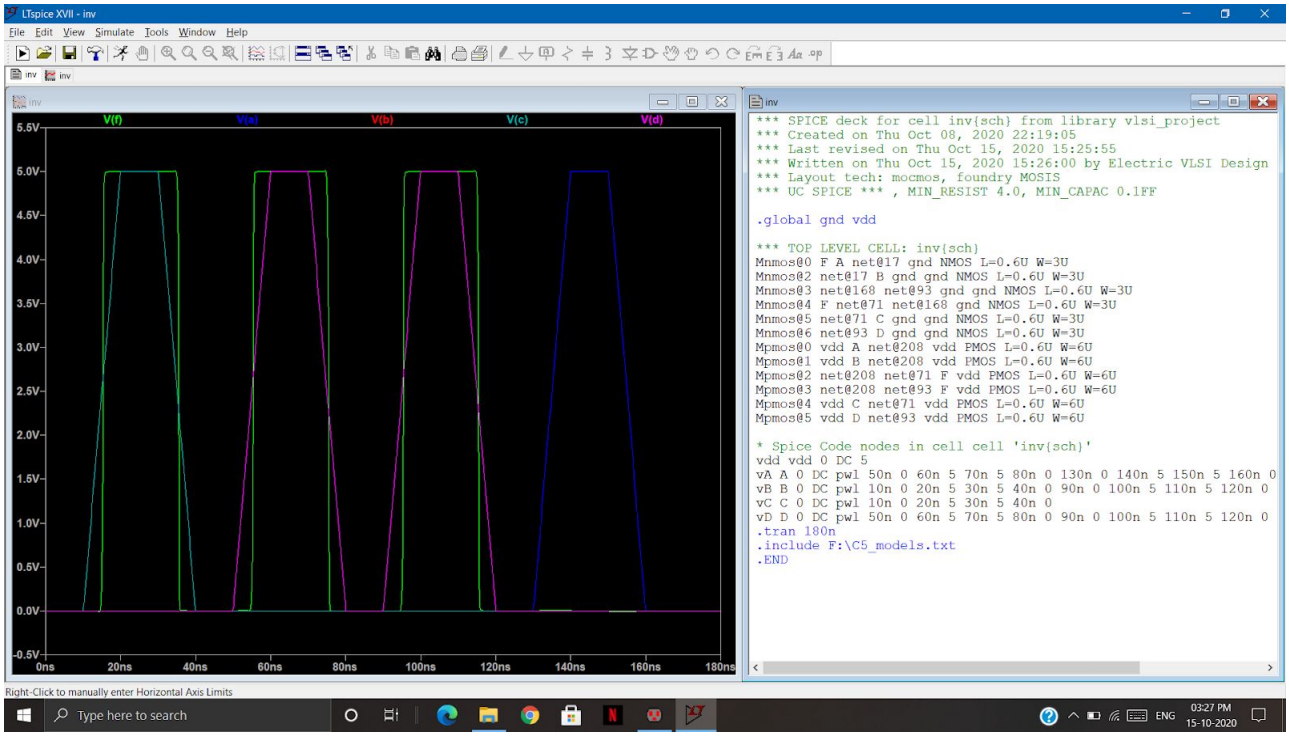
6. Layout Circuit



7. Simulation Results

CASE	A	B	C	D	F
1.	0	0	0	0	0
2.	0	1	1	0	1
3.	1	0	0	1	1
4.	0	1	0	1	1
5.	1	0	0	0	0

- *For schematic:*


LTspice XVII - inv
File Edit View Simulate Tools Window Help
V(f) V(a) V(b) V(c) V(d)
5.5V 5.0V 4.5V 4.0V 3.5V 3.0V 2.5V 2.0V 1.5V 1.0V 0.5V 0.0V -0.5V
0ns 20ns 40ns 60ns 80ns 100ns 120ns 140ns 160ns 180ns
Right-Click to manually enter Horizontal Axis Limits
*** SPICE deck for cell inv{sch} from library vlsi_project
*** Created on Thu Oct 08, 2020 22:19:05
*** Last revised on Thu Oct 15, 2020 15:25:55
*** Written on Thu Oct 15, 2020 15:26:00 by Electric VLSI Design
*** Layout tech: mocmos, foundry MOSIS
*** UC SPICE *** , MIN_RESIST 4.0, MIN_CAPAC 0.1FF
.global gnd vdd
*** TOP LEVEL CELL: inv{sch}
Mnmos@0 F A net@17 gnd NMOS L=0.6U W=3U
Mnmos@2 net@17 B gnd gnd NMOS L=0.6U W=3U
Mnmos@3 net@168 net@93 gnd gnd NMOS L=0.6U W=3U
Mnmos@4 F net@71 net@168 gnd NMOS L=0.6U W=3U
Mnmos@5 net@71 C gnd gnd NMOS L=0.6U W=3U
Mnmos@6 net@93 D gnd gnd NMOS L=0.6U W=3U
Mpmos@0 vdd A net@208 vdd PMOS L=0.6U W=6U
Mpmos@1 vdd B net@208 vdd PMOS L=0.6U W=6U
Mpmos@2 net@208 net@71 F vdd PMOS L=0.6U W=6U
Mpmos@3 net@208 net@93 F vdd PMOS L=0.6U W=6U
Mpmos@4 vdd C net@71 vdd PMOS L=0.6U W=6U
Mpmos@5 vdd D net@93 vdd PMOS L=0.6U W=6U
* Spice Code nodes in cell cell 'inv{sch}'
vdd vdd 0 DC 5
vA A 0 DC pwl 50n 0 60n 5 70n 5 80n 0 130n 0 140n 5 150n 5 160n 0
vB B 0 DC pwl 10n 0 20n 5 30n 5 40n 0 90n 0 100n 5 110n 5 120n 0
vC C 0 DC pwl 10n 0 20n 5 30n 5 40n 0
vD D 0 DC pwl 50n 0 60n 5 70n 5 80n 0 90n 0 100n 5 110n 5 120n 0
.tran 180n
.include F:\C5_models.txt
.END
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ENG
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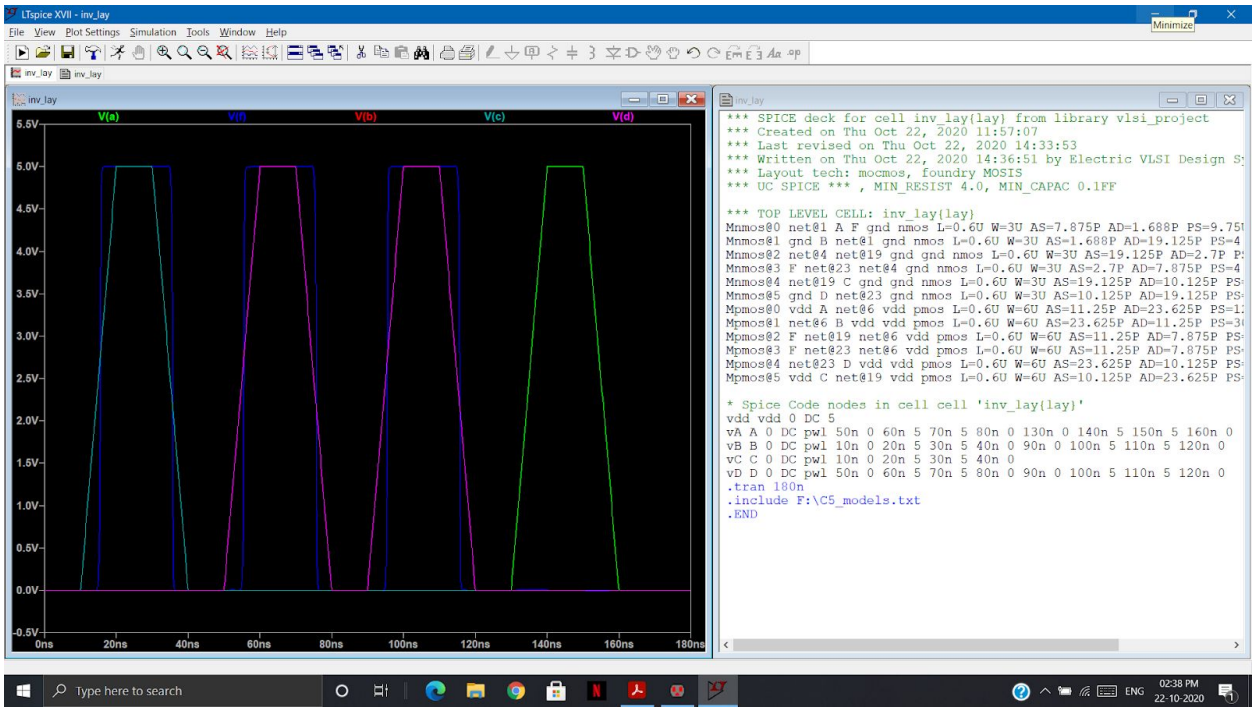
15-10-2020

- *For layout:*


LTspice XVII - inv_lay
File View Plot Settings Simulation Tools Window Help
Minimize
V(a) V(f) V(b) V(c) V(d)
5.5V 5.0V 4.5V 4.0V 3.5V 3.0V 2.5V 2.0V 1.5V 1.0V 0.5V 0.0V -0.5V
0ns 20ns 40ns 60ns 80ns 100ns 120ns 140ns 160ns 180ns
*** SPICE deck for cell inv_lay{lay} from library vlsi_project
*** Created on Thu Oct 22, 2020 11:57:07
*** Last revised on Thu Oct 22, 2020 14:33:53
*** Written on Thu Oct 22, 2020 14:36:51 by Electric VLSI Design
*** Layout tech: mocmos, foundry MOSIS
*** UC SPICE *** , MIN_RESIST 4.0, MIN_CAPAC 0.1FF
*** TOP LEVEL CELL: inv_lay{lay}
Mnmos@0 net@1 A F gnd nmos L=0.6U W=3U AS=7.875P AD=1.688P PS=9.75
Mnmos@1 gnd B net@1 gnd nmos L=0.6U W=3U AS=1.688P AD=19.125P PS=4
Mnmos@2 net@4 net@19 gnd gnd nmos L=0.6U W=3U AS=19.125P AD=2.7P P
Mnmos@3 F net@23 net@4 gnd nmos L=0.6U W=3U AS=2.7P AD=7.875P PS=4
Mnmos@4 net@19 C gnd gnd nmos L=0.6U W=3U AS=19.125P AD=10.125P PS
Mnmos@5 gnd D net@23 gnd nmos L=0.6U W=3U AS=10.125P AD=19.125P PS
Mpmos@0 vdd A net@6 vdd pmos L=0.6U W=6U AS=11.25P AD=23.625P PS=1
Mpmos@1 net@6 B vdd vdd pmos L=0.6U W=6U AS=23.625P AD=11.25P PS=3
Mpmos@2 F net@19 net@6 vdd pmos L=0.6U W=6U AS=11.25P AD=7.875P PS
Mpmos@3 F net@23 net@6 vdd pmos L=0.6U W=6U AS=11.25P AD=7.875P PS
Mpmos@4 net@23 D vdd vdd pmos L=0.6U W=6U AS=23.625P AD=10.125P PS
Mpmos@5 vdd C net@19 vdd pmos L=0.6U W=6U AS=10.125P AD=23.625P PS
* Spice Code nodes in cell cell 'inv_lay{lay}'
vdd vdd 0 DC 5
vA A 0 DC pwl 50n 0 60n 5 70n 5 80n 0 130n 0 140n 5 150n 5 160n 0
vB B 0 DC pwl 10n 0 20n 5 30n 5 40n 0 90n 0 100n 5 110n 5 120n 0
vC C 0 DC pwl 10n 0 20n 5 30n 5 40n 0
vD D 0 DC pwl 50n 0 60n 5 70n 5 80n 0 90n 0 100n 5 110n 5 120n 0
.tran 180n
.include F:\C5_models.txt
.END
Type here to search
ENG
02:38 PM
22-10-2020

8. References

- Baker, R. Jacob. “Electric VlSI Tutorials from CMOSedu.com”. *CMOSedu,* http://cmosedu.com/videos/electric/electric_videos.htm
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- Rubin, Steven M. “Electric User's Manual, version 9.07”. *Staticfreesoft,* https://www.staticfreesoft.com/jmanual/