Lab 6: Design and Characterization of a Flip-Flop

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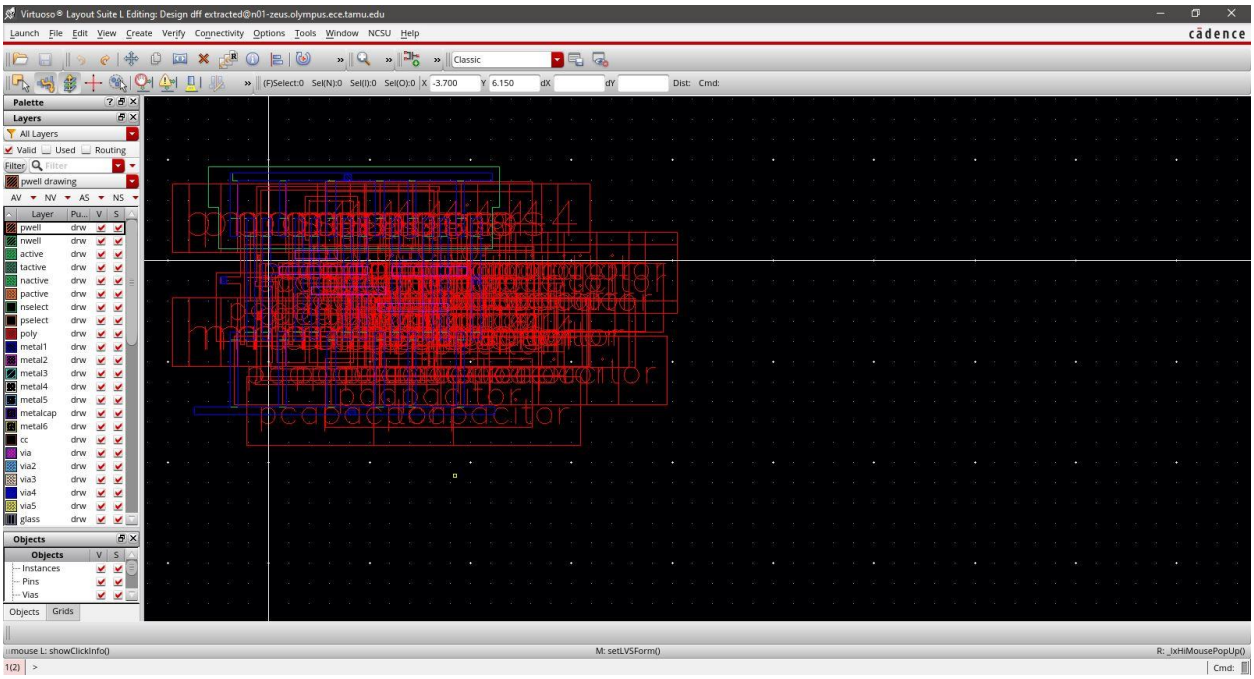
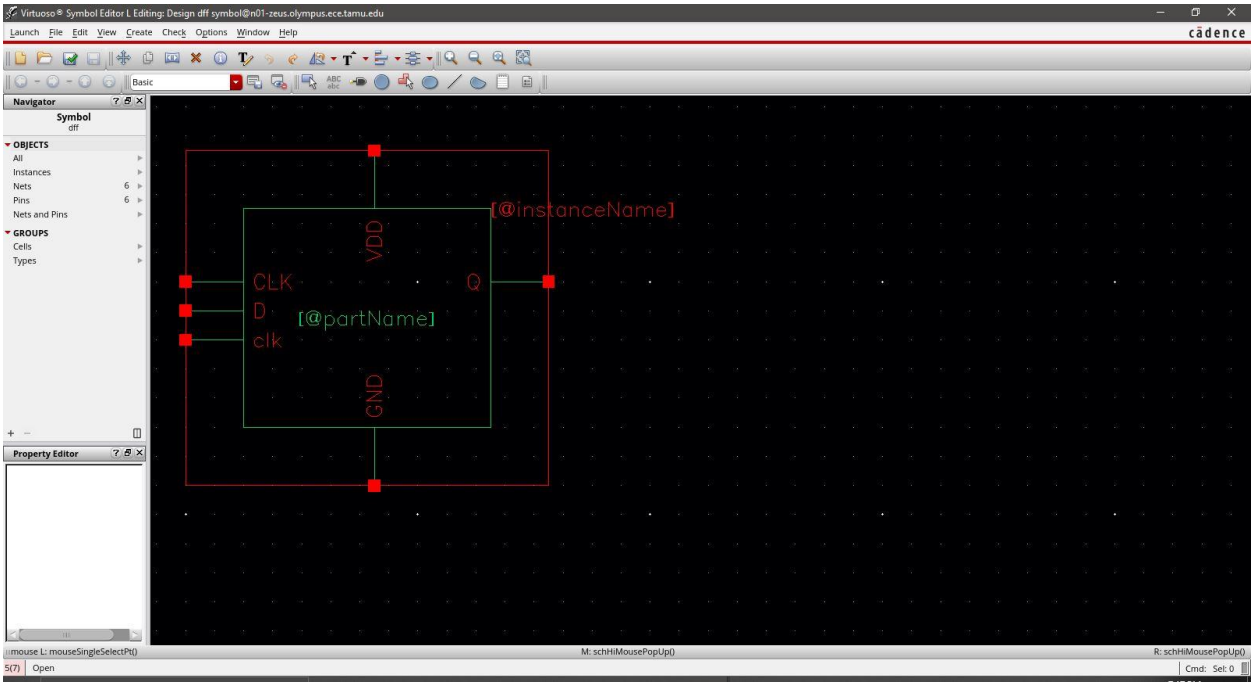
Introduction:

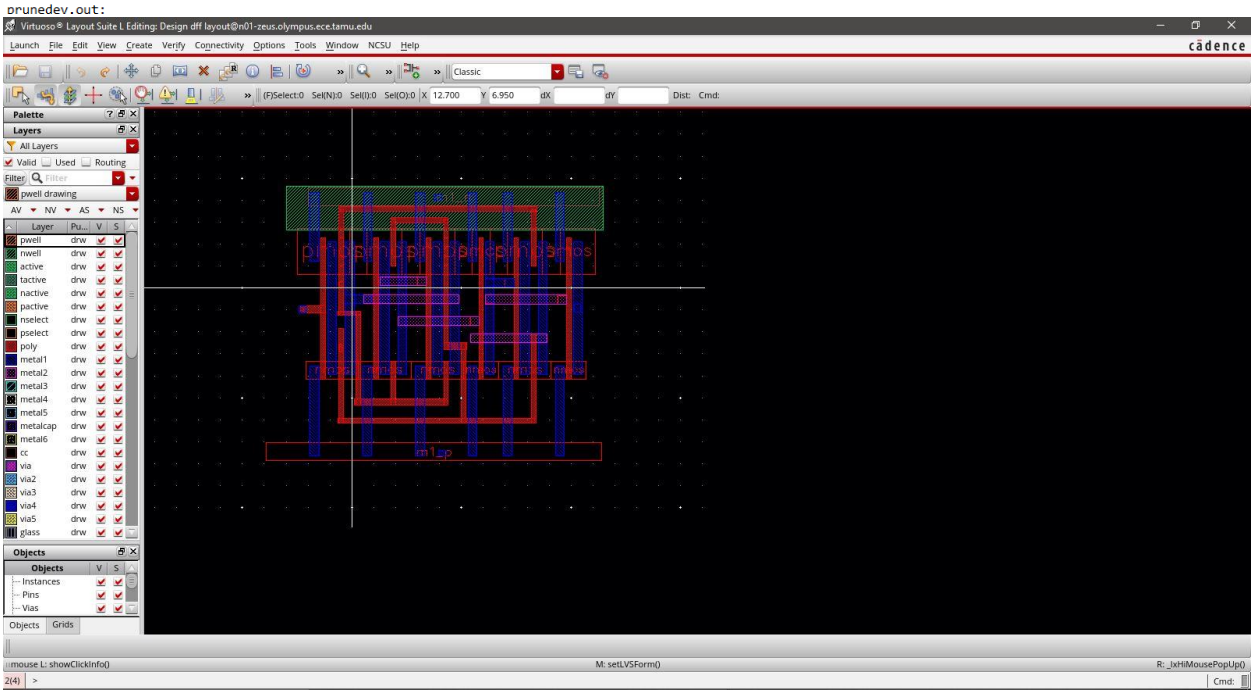
After completing the design of a single combinational stage of the design, you will next design the basic sequential element that will be used in the design, i.e., the Flip-Flop (FF). In this lab you will be required to design Flip-Flop and also characterize its delay, input capacitance and its setup and hold time.

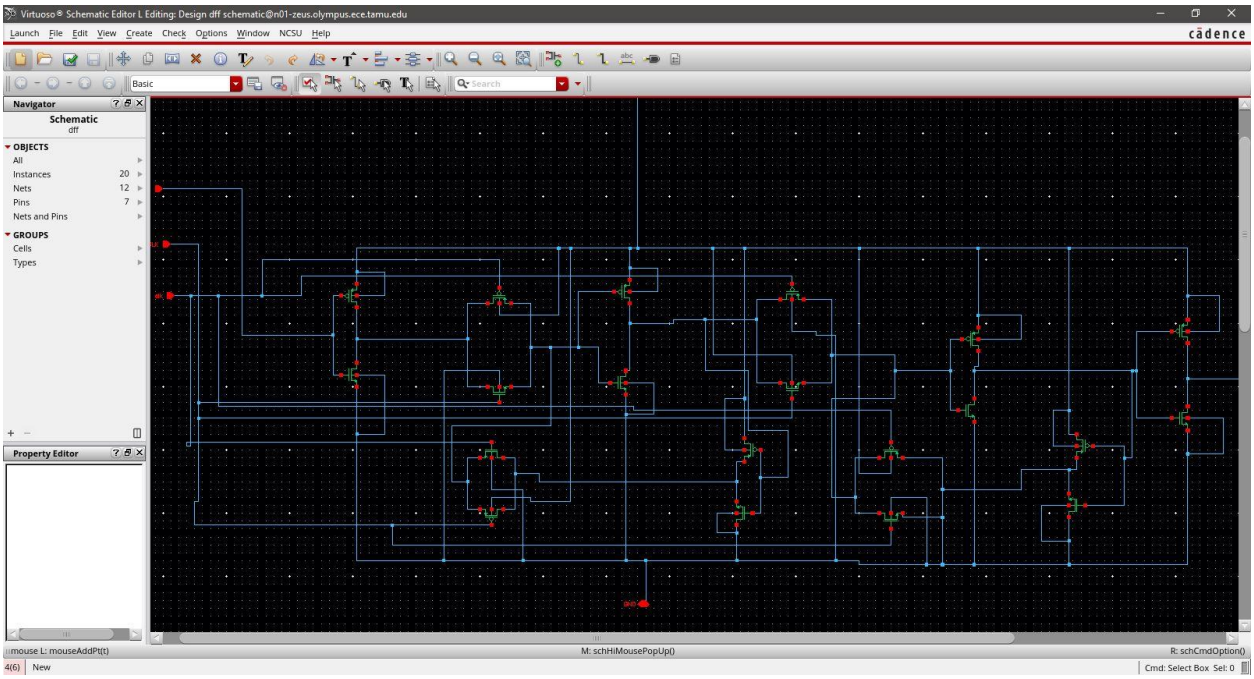
Results:

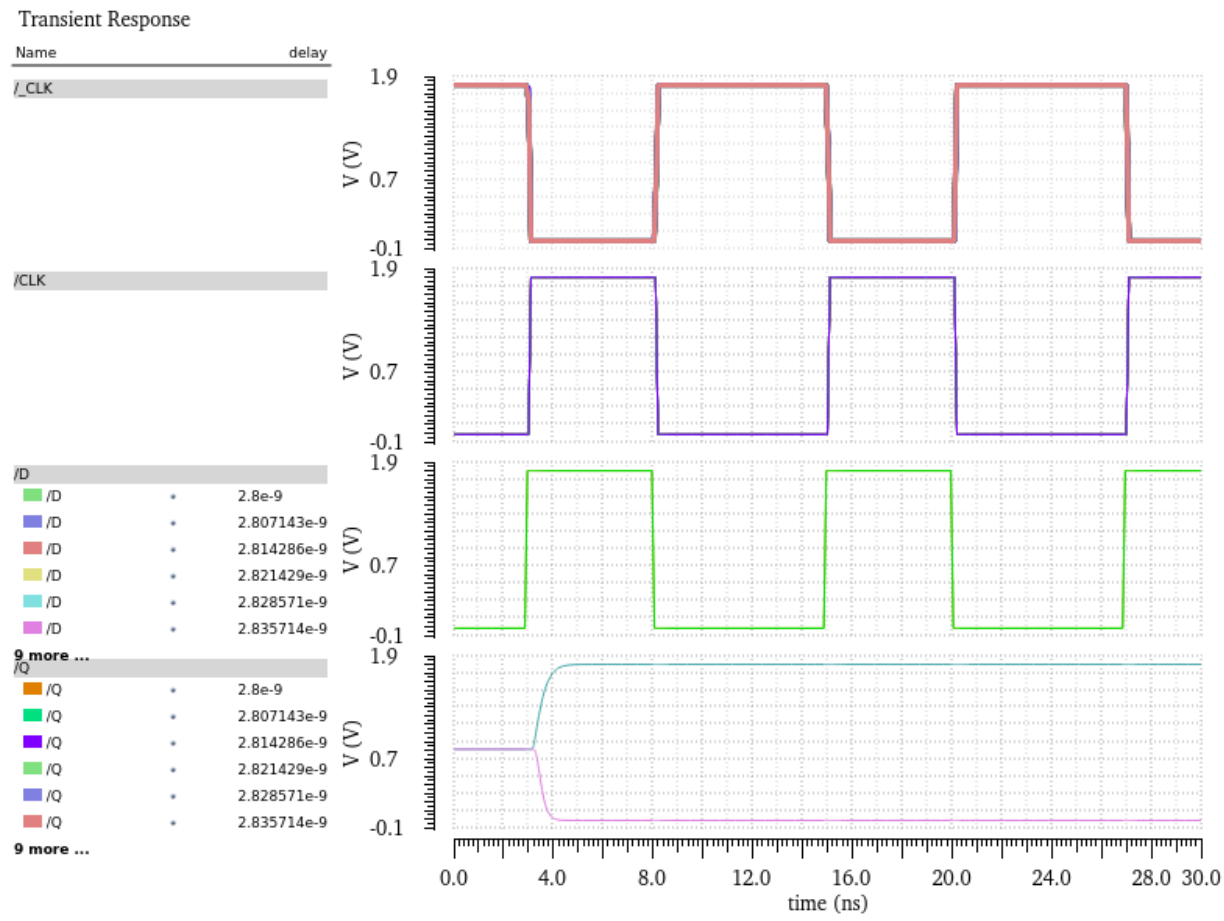

Virtuoso® Layout Suite L Editing: Design dff extracted@n01-zeus.olympus.ece.tamu.edu
Launch File Edit View Create Verify Connectivity Options Tools Window NCSU Help
cadence
Palette
Layers
All Layers
Valid Used Routing
pwell drawing
Layer Pu... V S
pwell drw
nwell drw
active drw
tactive drw
nactive drw
pactive drw
nselect drw
pselect drw
poly drw
metal1 drw
metal2 drw
metal3 drw
metal4 drw
metal5 drw
metalcap drw
metal6 drw
cc drw
via drw
via2 drw
via3 drw
via4 drw
via5 drw
glass drw
Objects
Instances
Pins
Vias
Objects Grids
mouse L: showClickInfo()
M: setLVSForm()
R: _lxHiMousePopUp()
Cmd:

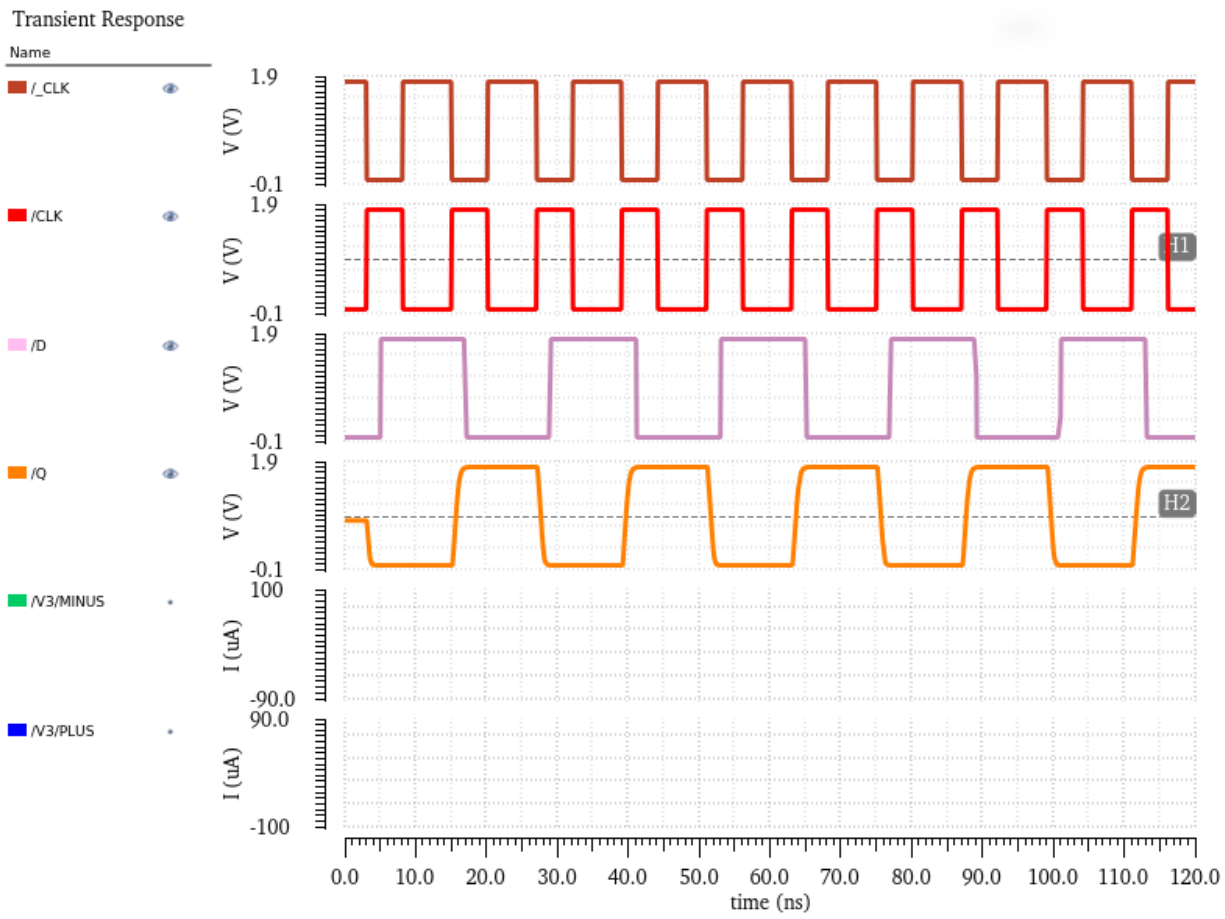

Virtuoso® Symbol Editor L Editing: Design dff symbol@n01-zeus.olympus.ece.tamu.edu
Launch File Edit View Create Check Options Window Help
cadence
Navigator
Symbol
dff
OBJECTS
All
Instances
Nets 6
Pins 6
Nets and Pins
GROUPS
Cells
Types
Property Editor
[@instanceName]
VDD
CLK
D
clk
[@partName]
Q
GND
mouse L: mouseSingleSelectPt()
M: schHiMousePopUp()
R: schHiMousePopUp()
Open
Cmd: Sel: 0

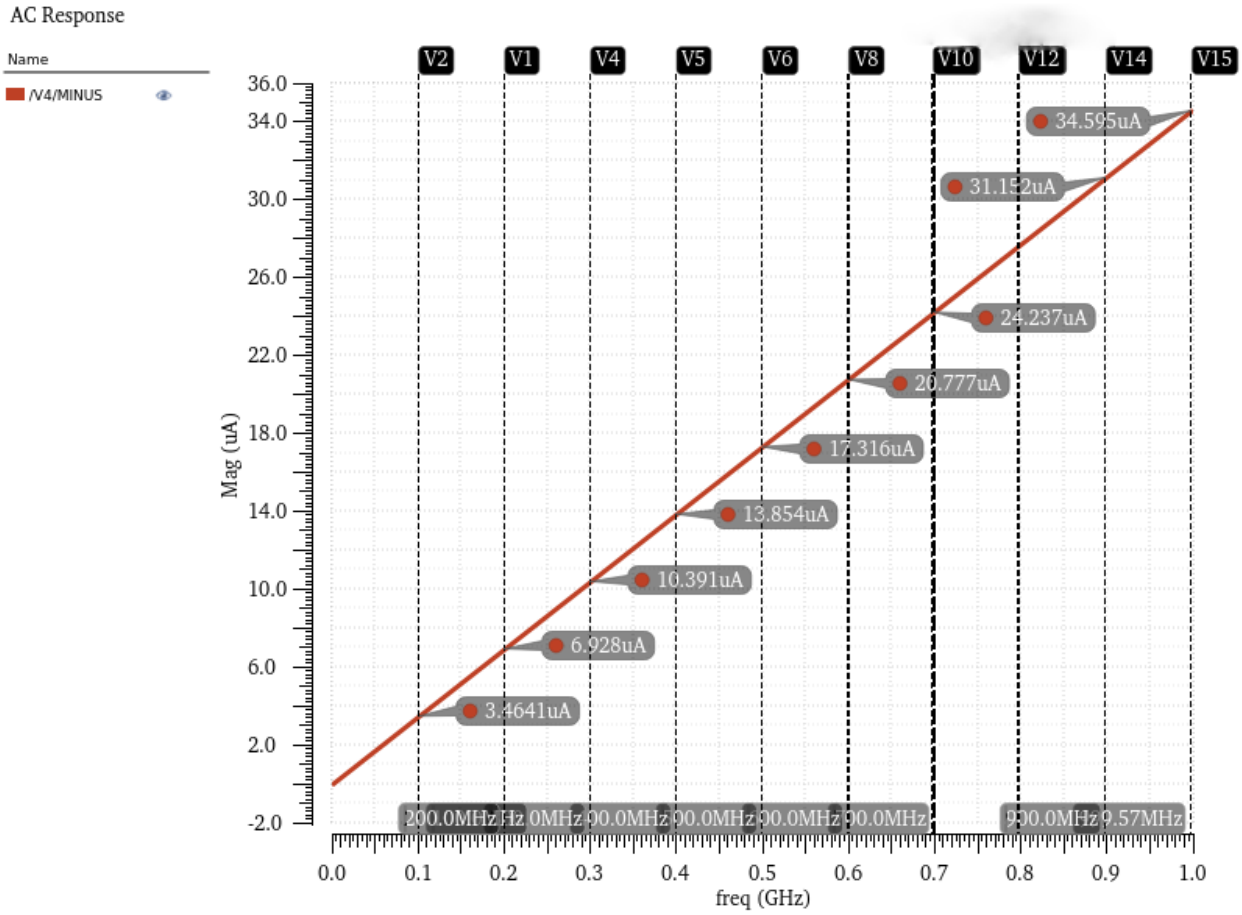
```
Devices in the netlist but not in the rules:
        pcapacitor pmos nmos

The net-lists match.

                              layout  schematic
                                instances
        un-matched                0       0
        rewired                   0       0
        size errors               0       0
        pruned                    0       0
        active                   20      20
        total                    20      20

                                  nets
        un-matched                0       0
        merged                    0       0
        pruned                    0       0
        active                   13      13
        total                    13      13

                                terminals
        un-matched                0       0
        matched but
        different type            2       2
        total                     6       6


Probe files from /home/ugrads/s/seakid/cadence/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:
? Terminal CLK's type in the schematic: inputOutput, in the layout: input
? Terminal _CLK's type in the schematic: inputOutput, in the layout: input

prunenet.out:

prunedev.out:
```




Virtuoso® Schematic Editor L Editing: Design dff schematic@n01-zeus.olympus.ece.tamu.edu
Launch File Edit View Create Check Options Window NCSU Help
cadence
Navigator
Schematic
dff
OBJECTS
All
Instances 20
Nets 12
Pins 7
Nets and Pins
GROUPS
Cells
Types
Property Editor
mouse L: mouseAddPt(t)
M: schHiMousePopUp()
R: schCmdOption()
4(6) New
Cmd: Select Box Sel: 0


Transient Response
Name
delay
/_CLK
/CLK
/D
/D 2.8e-9
/D 2.807143e-9
/D 2.814286e-9
/D 2.821429e-9
/D 2.828571e-9
/D 2.835714e-9
9 more ...
/Q
/Q 2.8e-9
/Q 2.807143e-9
/Q 2.814286e-9
/Q 2.821429e-9
/Q 2.828571e-9
/Q 2.835714e-9
9 more ...
1.9
0.7
-0.1
V (V)
0.0
4.0
8.0
12.0
16.0
20.0
24.0
28.0
30.0
time (ns)


Transient Response
Name
/_CLK
/CLK
/D
/Q
/V3/MINUS
/V3/PLUS
1.9
-0.1
V (V)
H1
H2
100
-90.0
I (uA)
90.0
-100
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
110.0
120.0
time (ns)


AC Response
Name
/V4/MINUS
V2
V1
V4
V5
V6
V8
V10
V12
V14
V15
34.595uA
31.152uA
24.237uA
20.777uA
17.316uA
13.854uA
10.391uA
6.928uA
3.4641uA
Mag (uA)
freq (GHz)