Lab 2: Cadence Custom Layout:

Design Rules, Extraction and Verification

Connor Murphy

ECEN454-504

TA Sina

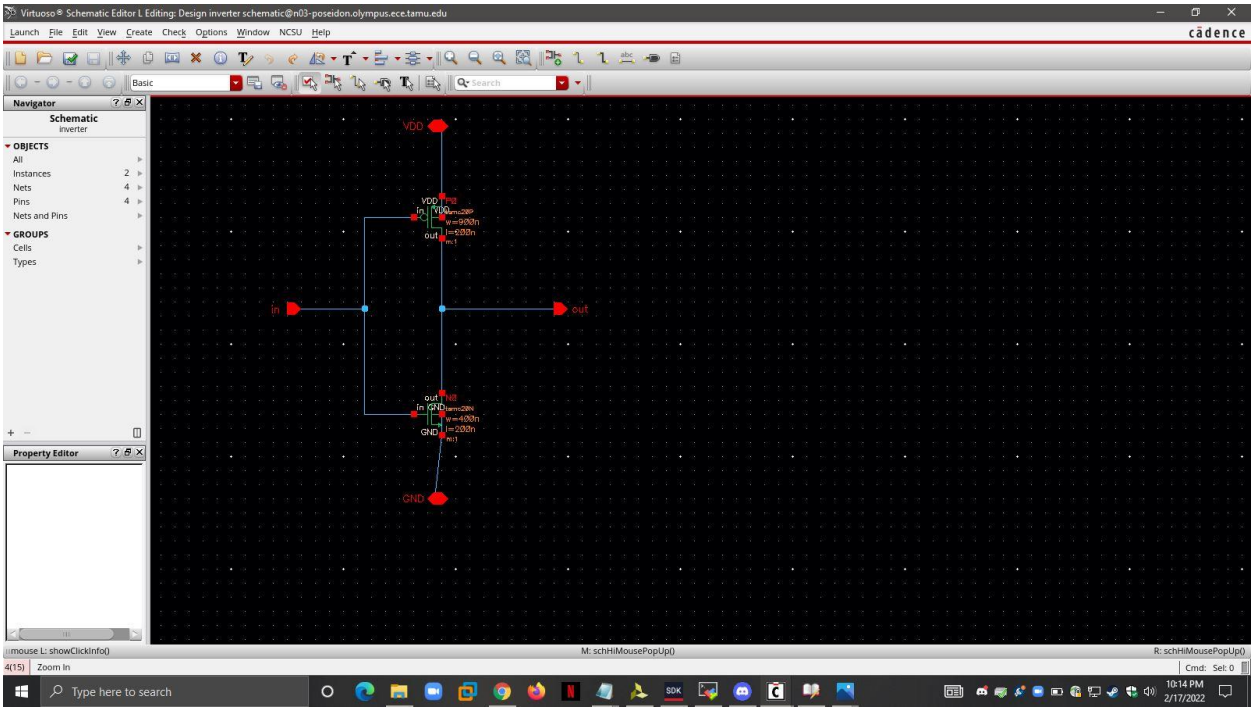
2/17/2022

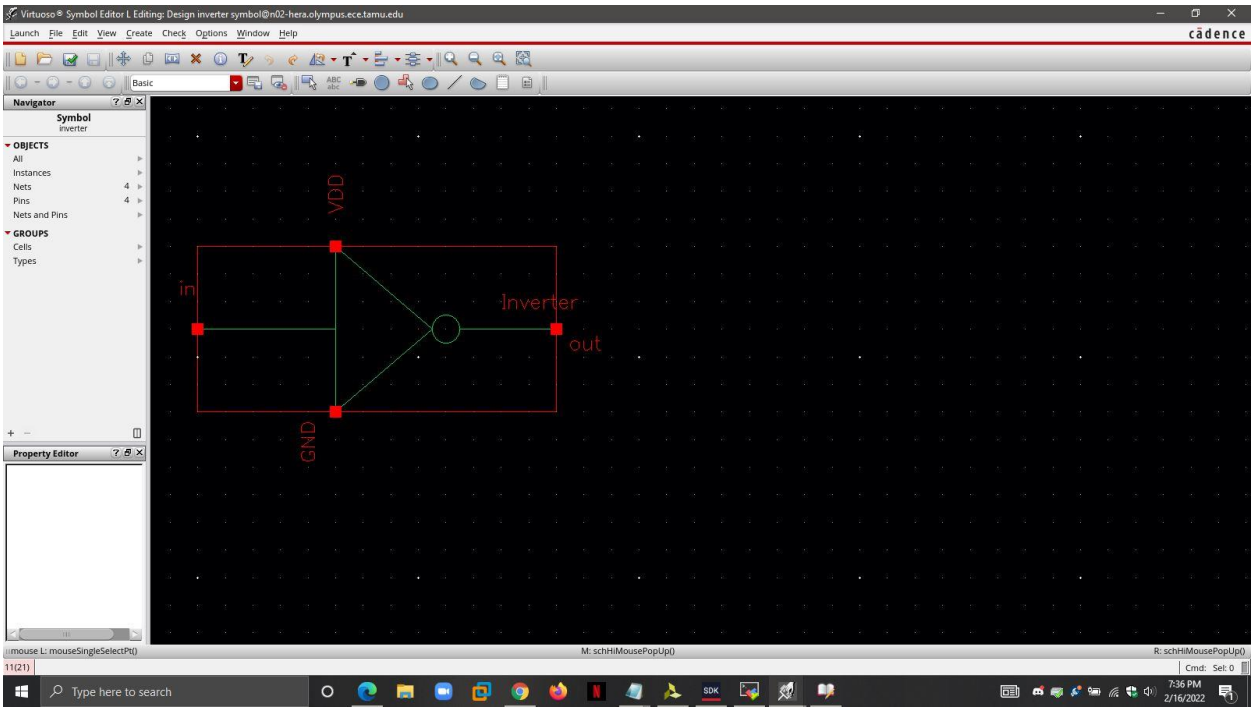
Introduction:

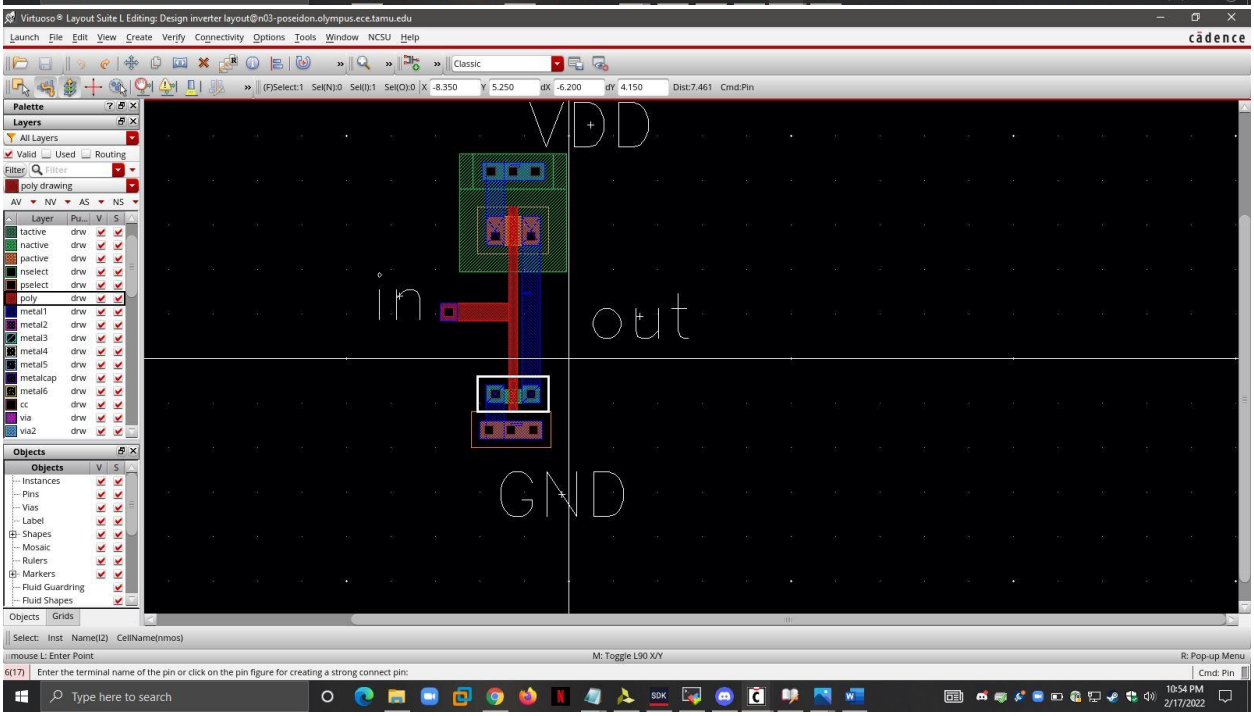
In this lab you will create the physical layout of all the logic gates (Inverter, NAND2, and XOR2) that you used in the previous labs. This lab manual contains instructions to draw the schematic and layout of a basic inverter circuit. You will also perform extraction of the layout parameters and verifying if the layout drawn is equivalent to the schematic (of the corresponding gate) through an LVS (Layout versus schematic) check. You would have to implement the same for the other required gates. Make sure you have attached the “NCSU_TechLib_tsmc02” technology file to your library before you begin the lab. This technology will use design rules based on the 0.2 µm technology from TSMC. This means that the smallest feature size that can be implemented is 0.2 µm. All the layout dimensions would be in terms of “λ” which is equal to half the feature size (0.1 pm in this case).

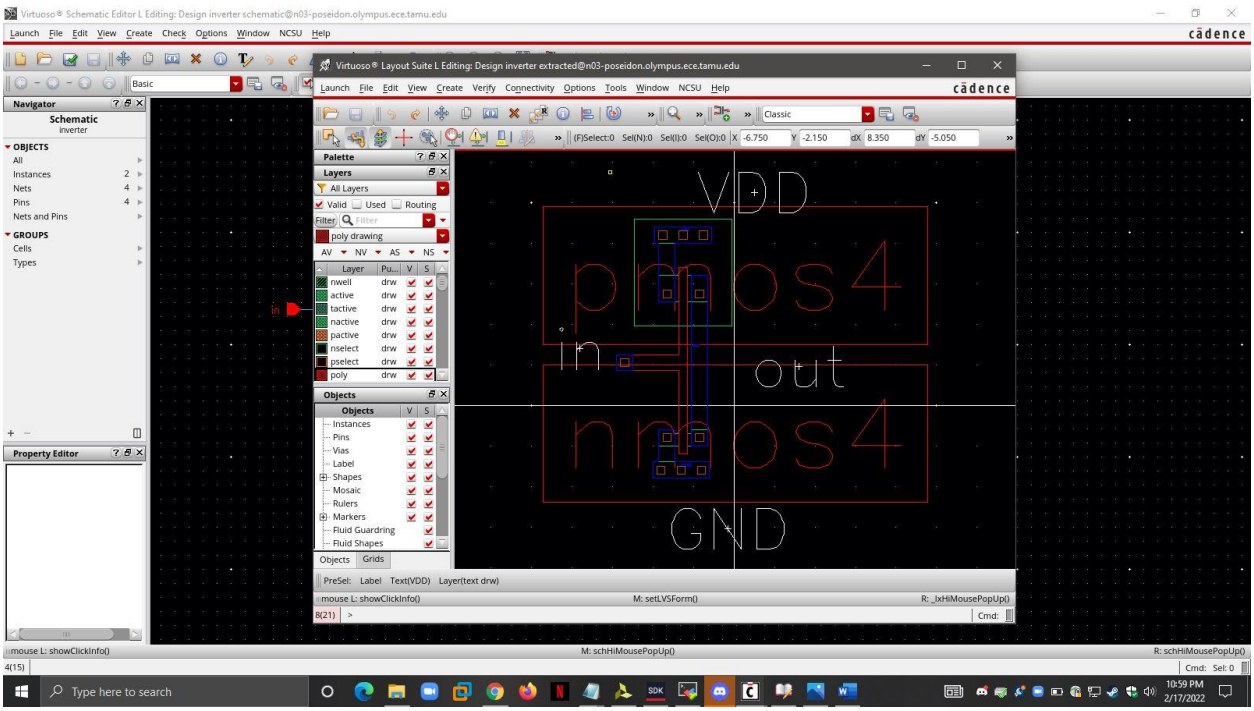
Results:

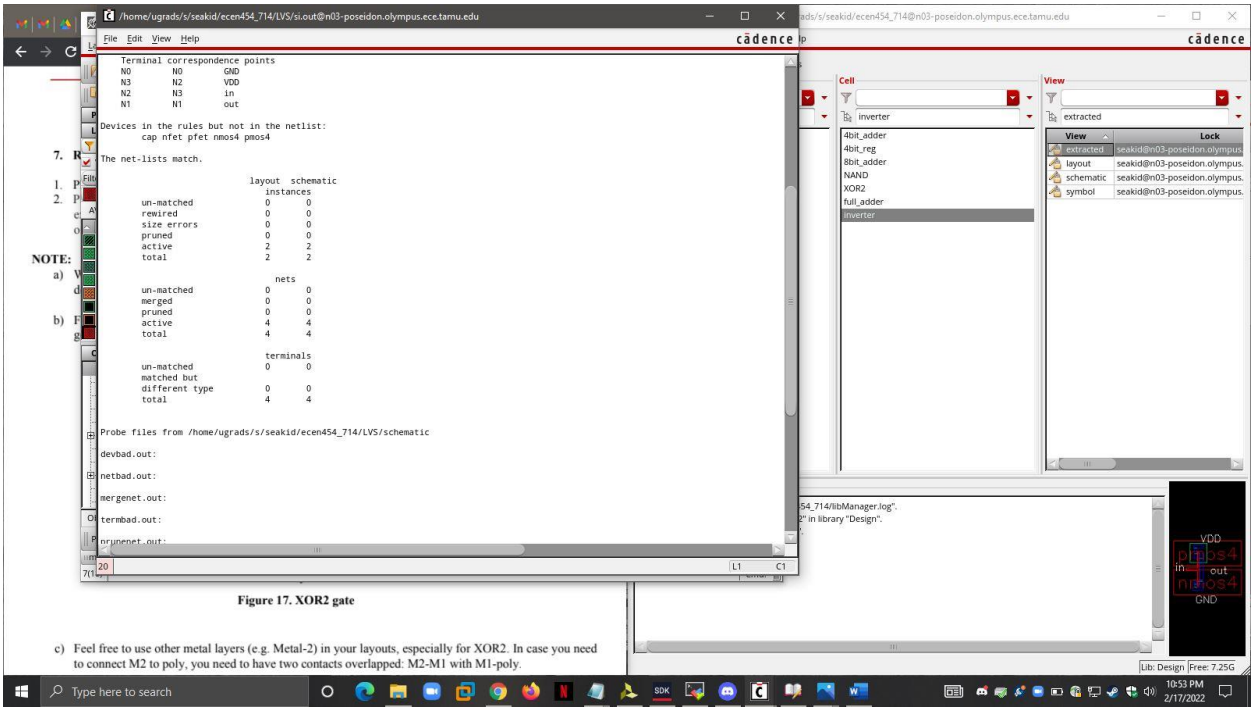
Inverter



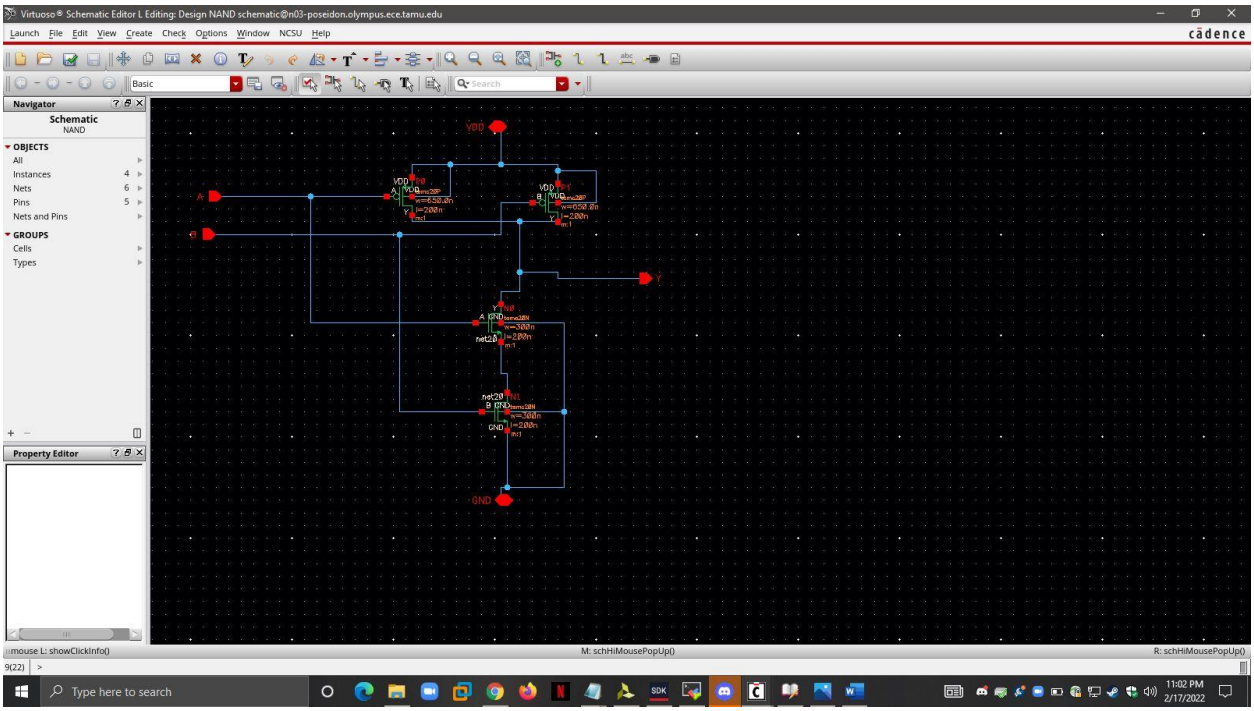

Virtuoso® Symbol Editor L Editing: Design inverter symbol@n02-hera.olympus.ece.tamu.edu
Launch File Edit View Create Check Options Window Help
cadence
Navigator
Symbol
inverter
OBJECTS
All
Instances
Nets 4
Pins 4
Nets and Pins
GROUPS
Cells
Types
Property Editor
VDD
in
Inverter
out
GND
mouse L: mouseSingleSelectPt()
M: schHiMousePopUp()
R: schHiMousePopUp()
11(21)
Cmd: Sel: 0
Type here to search
7:36 PM
2/16/2022

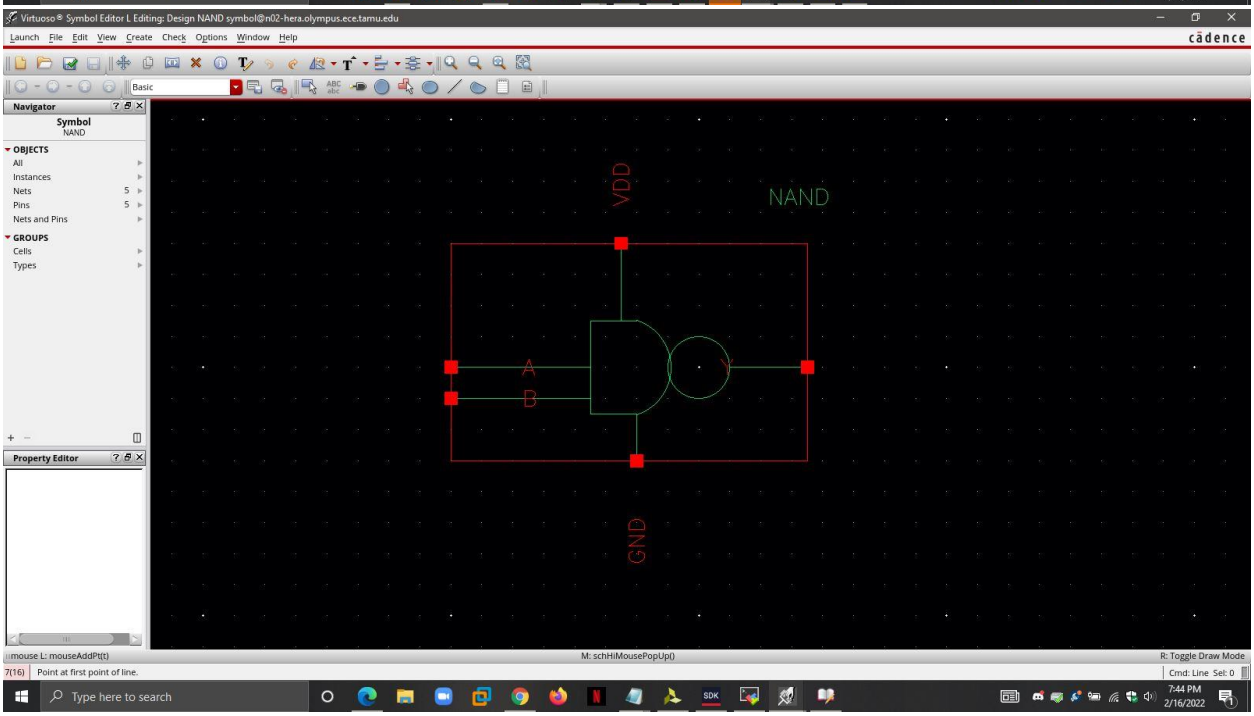

Virtuoso® Layout Suite L Editing: Design inverter layout@n03-poseidon.olympus.ece.tamu.edu
Launch File Edit View Create Verify Connectivity Options Tools Window NCSU Help
cadence
Palette
Layers
All Layers
Valid Used Routing
poly drawing
Objects
VDD
in
out
GND
Select: Inst Name(I2) CellName(nmos)
mouse L: Enter Point
M: Toggle L90 X/Y
R: Pop-up Menu
6(17)
Enter the terminal name of the pin or click on the pin figure for creating a strong connect pin:
Cmd: Pin
Type here to search
10:54 PM
2/17/2022

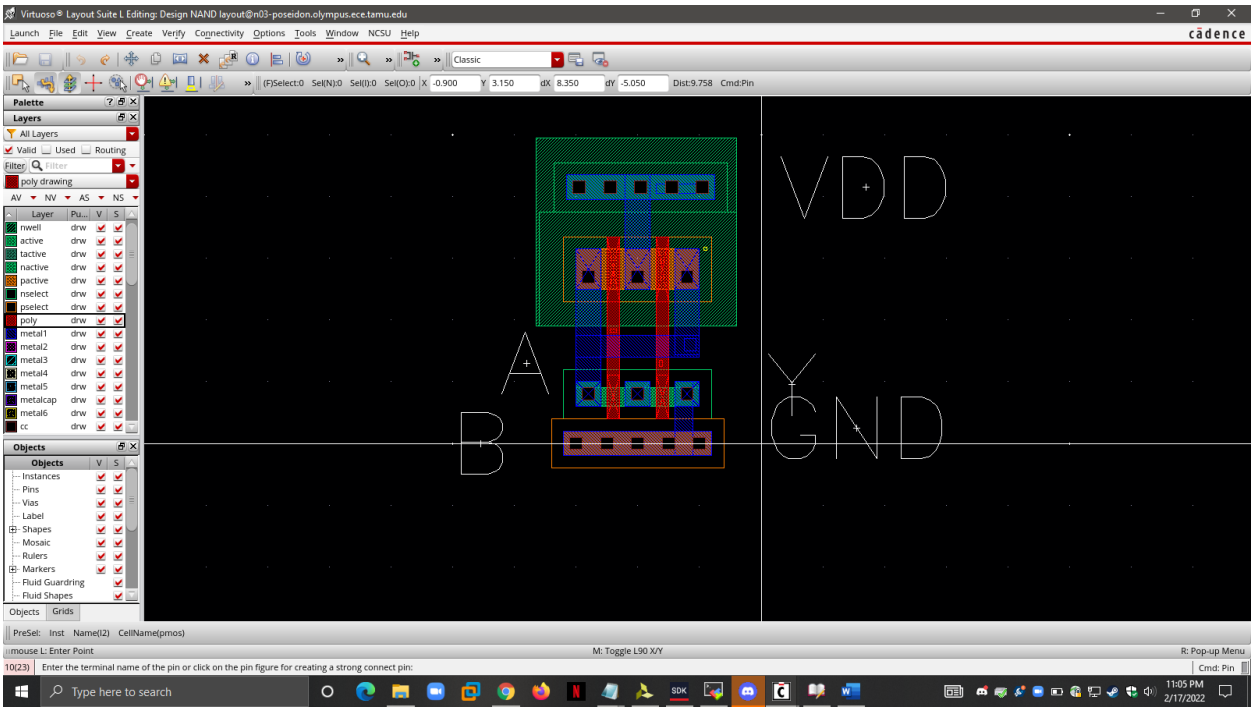

VDD
pmos4
in
out
nmos4
GND

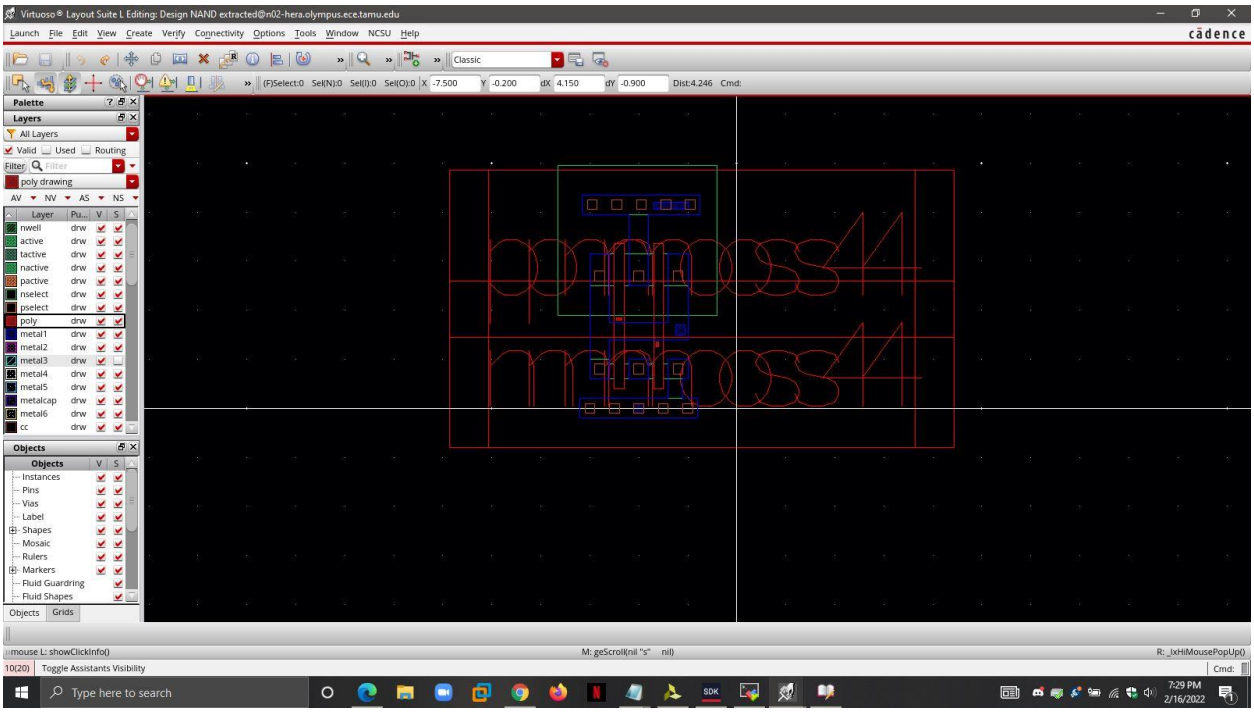

Terminal correspondence points
N0 N0 GND
N3 N2 VDD
N2 N3 in
N1 N1 out
Devices in the rules but not in the netlist:
cap nfet pfet nmos4 pmos4
The net-lists match.
layout schematic
instances
un-matched 0 0
rewired 0 0
size errors 0 0
pruned 0 0
active 2 2
total 2 2
nets
un-matched 0 0
merged 0 0
pruned 0 0
active 4 4
total 4 4
terminals
un-matched 0 0
matched but
different type 0 0
total 4 4
Probe files from /home/ugrads/s/seakid/ecen454_714/LVS/schematic
devbad.out:
netbad.out:
mergenet.out:
termbad.out:
prunenet.out:
Figure 17. XOR2 gate
c) Feel free to use other metal layers (e.g. Metal-2) in your layouts, especially for XOR2. In case you need to connect M2 to poly, you need to have two contacts overlapped: M2-M1 with M1-poly.

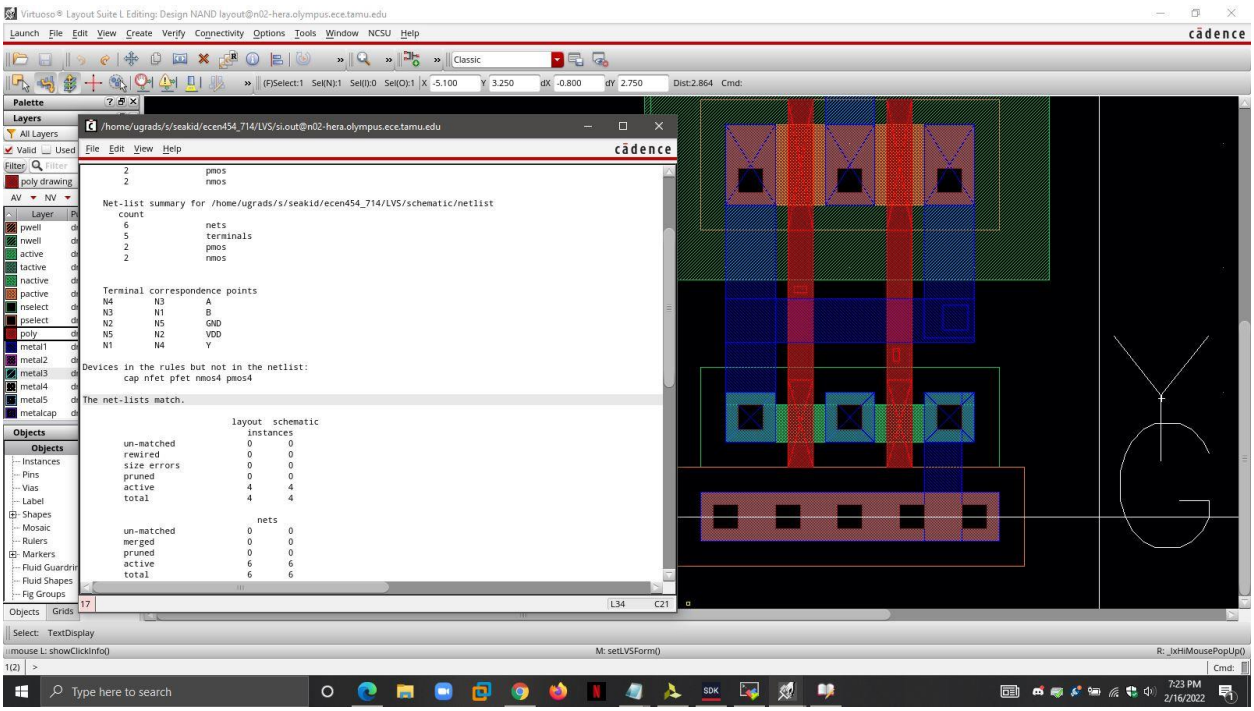
NAND Gate:


Virtuoso® Schematic Editor L Editing: Design NAND schematic@n03-poseidon.olympus.ece.tamu.edu
Launch File Edit View Create Check Options Window NCSU Help
cadence
Navigator
Schematic
NAND
OBJECTS
All
Instances 4
Nets 6
Pins 5
Nets and Pins
GROUPS
Cells
Types
Property Editor
VDD
GND
A
B
Y
net20
mouse L: showClickInfo()
M: schHiMousePopUp()
R: schHiMousePopUp()
Type here to search
11:02 PM
2/17/2022

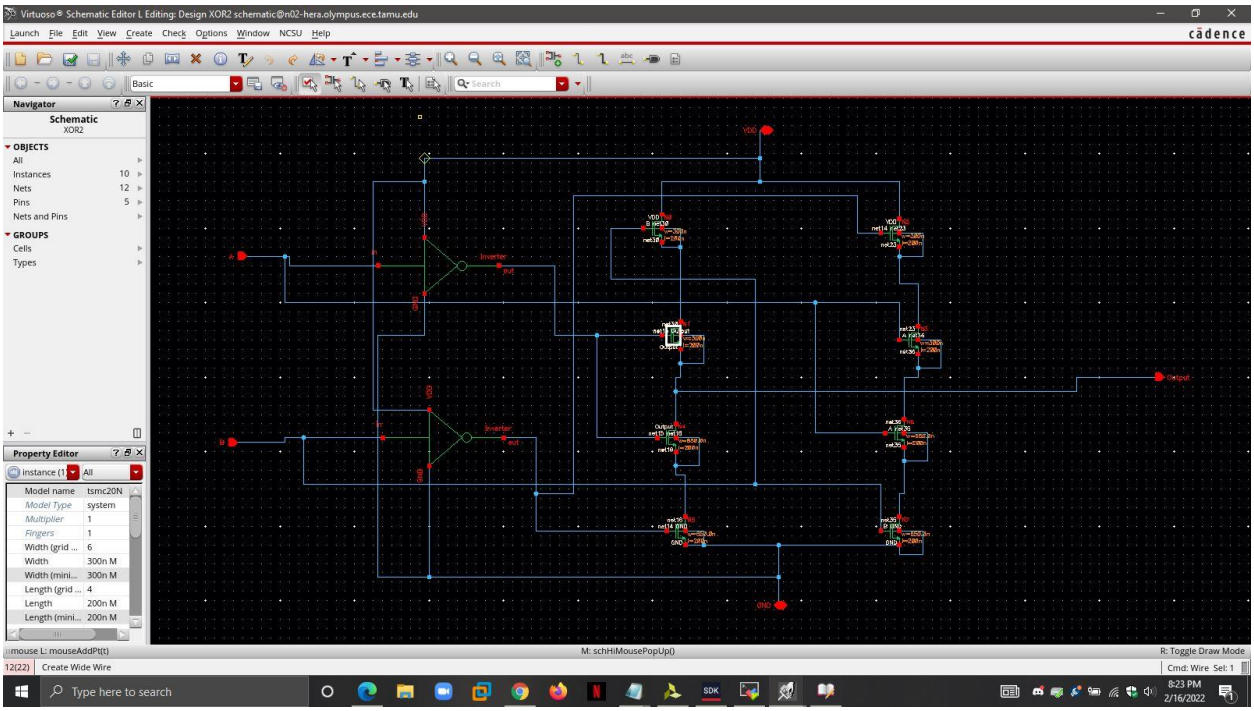

Virtuoso® Symbol Editor L Editing: Design NAND symbol@n02-hera.olympus.ece.tamu.edu
Launch File Edit View Create Check Options Window Help
cadence
Navigator
Symbol
NAND
OBJECTS
All
Instances
Nets 5
Pins 5
Nets and Pins
GROUPS
Cells
Types
Property Editor
VDD
NAND
A
B
Y
GND
mouse L: mouseAddPt(t)
M: schHiMousePopUp()
R: Toggle Draw Mode
Point at first point of line.
Cmd: Line Sel: 0
Type here to search
7:44 PM
2/16/2022

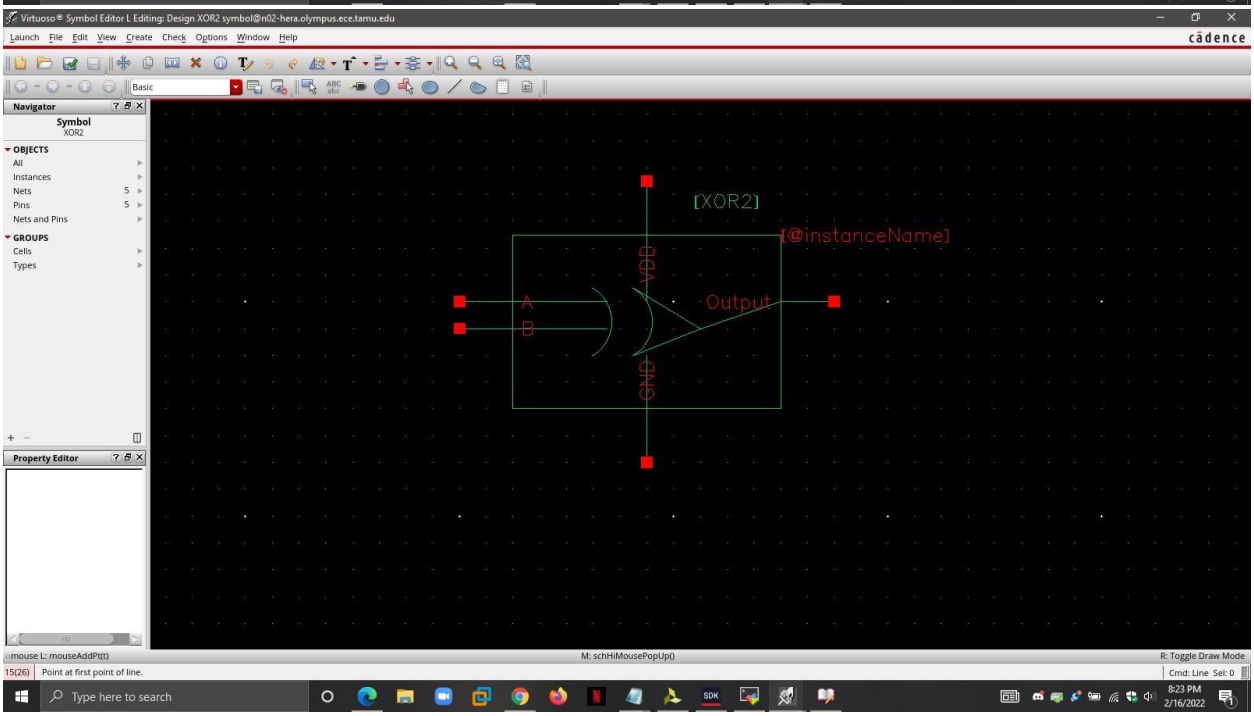

Virtuoso® Layout Suite L Editing: Design NAND layout@n03-poseidon.olympus.ece.tamu.edu
VDD
A
B
Y
GND
Type here to search
11:05 PM
2/17/2022

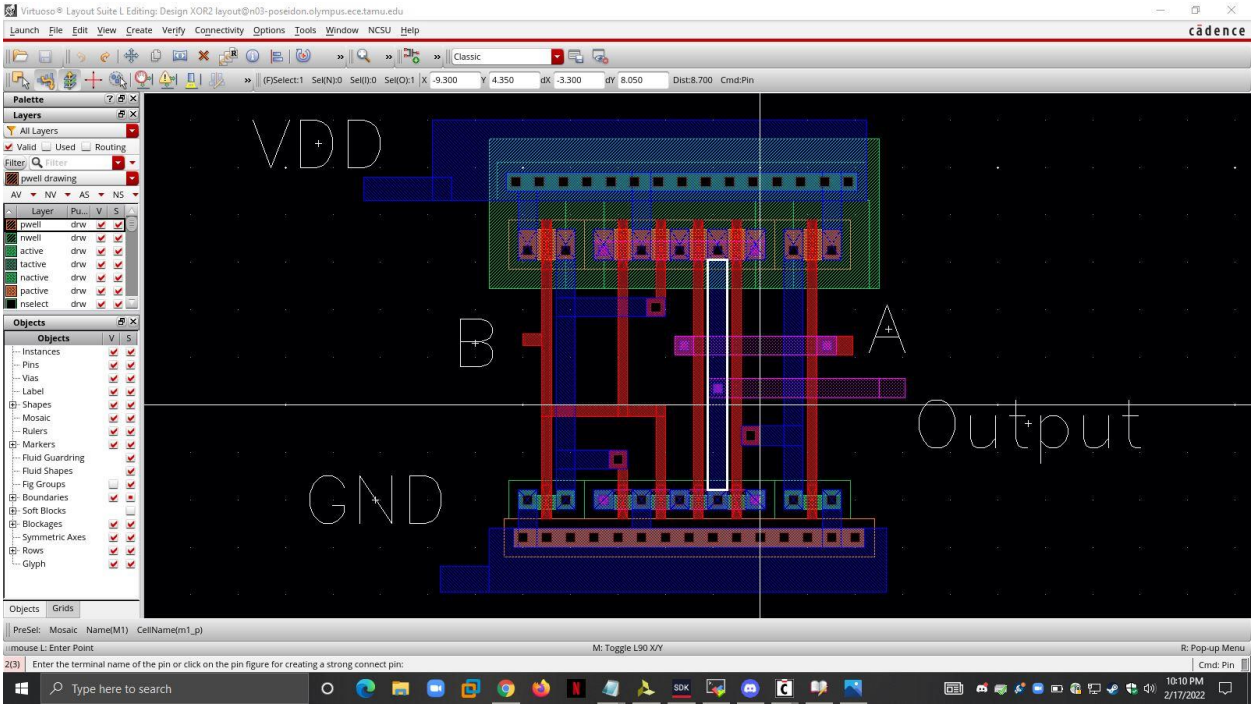

Virtuoso® Layout Suite L Editing: Design NAND extracted@n02-hera.olympus.ece.tamu.edu
pmos_4
nmos_4
Type here to search
7:29 PM
2/16/2022

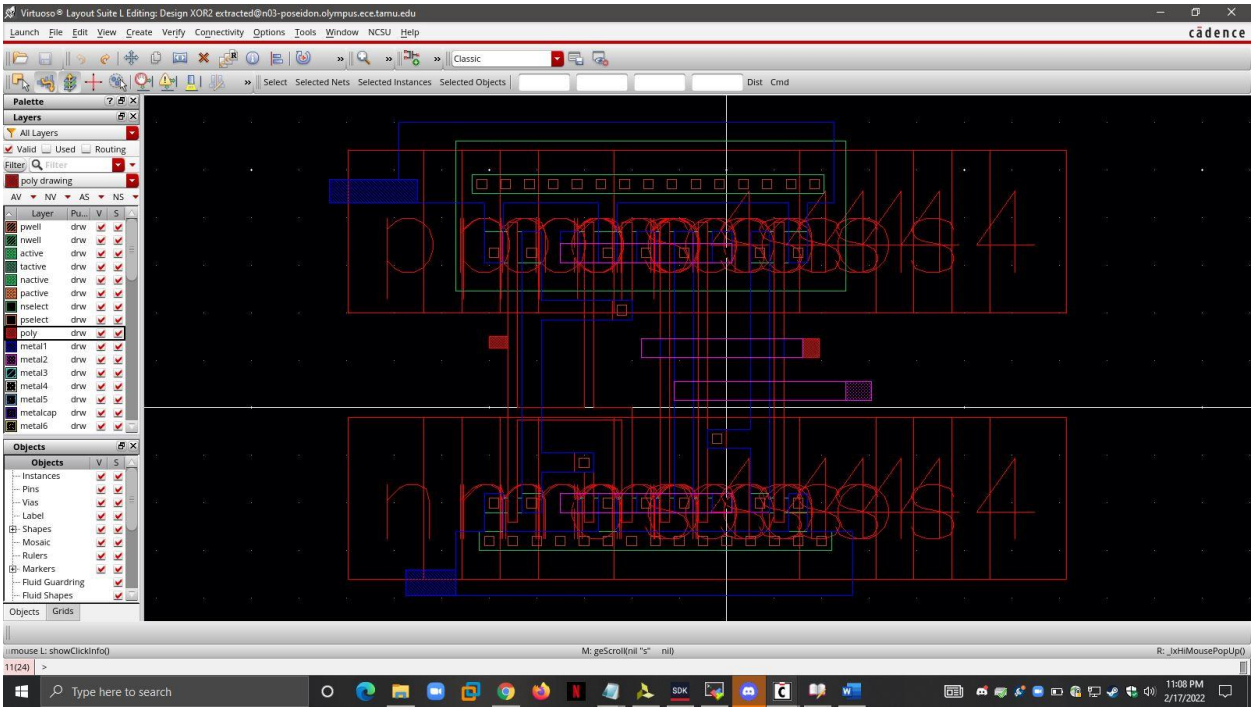

Virtuoso® Layout Suite L Editing: Design NAND layout@n02-hera.olympus.ece.tamu.edu
/home/ugrads/s/seakid/ecen454_714/LVS/si.out@n02-hera.olympus.ece.tamu.edu
2 pmos
2 nmos
Net-list summary for /home/ugrads/s/seakid/ecen454_714/LVS/schematic/netlist
count
6 nets
5 terminals
2 pmos
2 nmos
Terminal correspondence points
N4 N3 A
N3 N1 B
N2 N5 GND
N5 N2 VDD
N1 N4 Y
Devices in the rules but not in the netlist:
cap nfet pfet nmos4 pmos4
The net-lists match.
layout schematic
instances
un-matched 0 0
rewired 0 0
size errors 0 0
pruned 0 0
active 4 4
total 4 4
nets
un-matched 0 0
merged 0 0
pruned 0 0
active 6 6
total 6 6
Type here to search
7:23 PM
2/16/2022

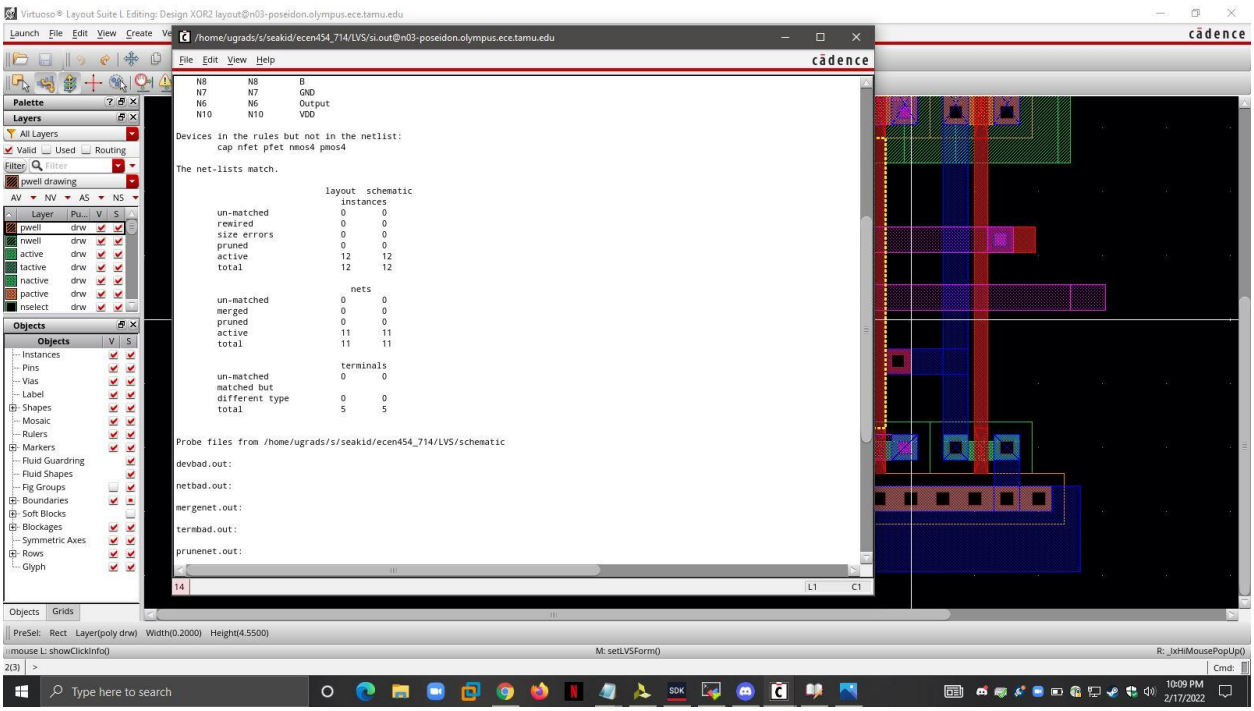
XOR2 Gate:


Virtuoso® Schematic Editor L Editing: Design XOR2 schematic@n02-hera.olympus.ece.tamu.edu
Launch File Edit View Create Check Options Window NCSU Help
cadence
Navigator
Schematic
XOR2
OBJECTS
All
Instances 10
Nets 12
Pins 5
Nets and Pins
GROUPS
Cells
Types
Property Editor
Model name tsmc20N
Model Type system
Multiplier 1
Fingers 1
Width (grid ... 6
Width 300n M
Length (grid ... 4
Length 200n M
VDD
GND
Output
Inverter
mouse L: mouseAddPt(t)
M: schHiMousePopUp()
R: Toggle Draw Mode
12(22) Create Wide Wire
Cmd: Wire Sel: 1
Type here to search
8:23 PM
2/16/2022


Virtuoso® Symbol Editor L Editing: Design XOR2 symbol@n02-hera.olympus.ece.tamu.edu
Launch File Edit View Create Check Options Window Help
cadence
Navigator
Symbol
XOR2
OBJECTS
All
Instances
Nets 5
Pins 5
Nets and Pins
GROUPS
Cells
Types
Property Editor
[XOR2]
[@instanceName]
VDD
GND
A
B
Output
mouse L: mouseAddPt(t)
M: schHiMousePopUp()
R: Toggle Draw Mode
15(26) Point at first point of line.
Cmd: Line Sel: 0
Type here to search
8:23 PM
2/16/2022


VDD
B
A
Output
GND




/home/ugrads/s/seakid/ecen454_714/LVS/si.out@n03-poseidon.olympus.ece.tamu.edu
File Edit View Help
cadence
N8 N8 B
N7 N7 GND
N6 N6 Output
N10 N10 VDD
Devices in the rules but not in the netlist:
cap nfet pfet nmos4 pmos4
The net-lists match.
layout schematic
instances
un-matched 0 0
rewired 0 0
size errors 0 0
pruned 0 0
active 12 12
total 12 12
nets
un-matched 0 0
merged 0 0
pruned 0 0
active 11 11
total 11 11
terminals
un-matched 0 0
matched but
different type 0 0
total 5 5
Probe files from /home/ugrads/s/seakid/ecen454_714/LVS/schematic
devbad.out:
netbad.out:
mergenet.out:
termbad.out:
prunenet.out:
Palette
Layers
All Layers
Valid Used Routing
pwell drawing
Objects
Instances
Pins
Vias
Label
Shapes
Mosaic
Rulers
Markers
Fluid Guardring
Fluid Shapes
Fig Groups
Boundaries
Soft Blocks
Blockages
Symmetric Axes
Rows
Glyph
Objects Grids
PreSel: Rect Layer(poly drw) Width(0.2000) Height(4.5500)
M: setLVSForm()
Cmd:
Type here to search
10:09 PM
2/17/2022