

Lab 1: Introduction to Cadence Schematic Capture & Simulation

Connor Murphy

TA: Sina

ECEN 454- 507

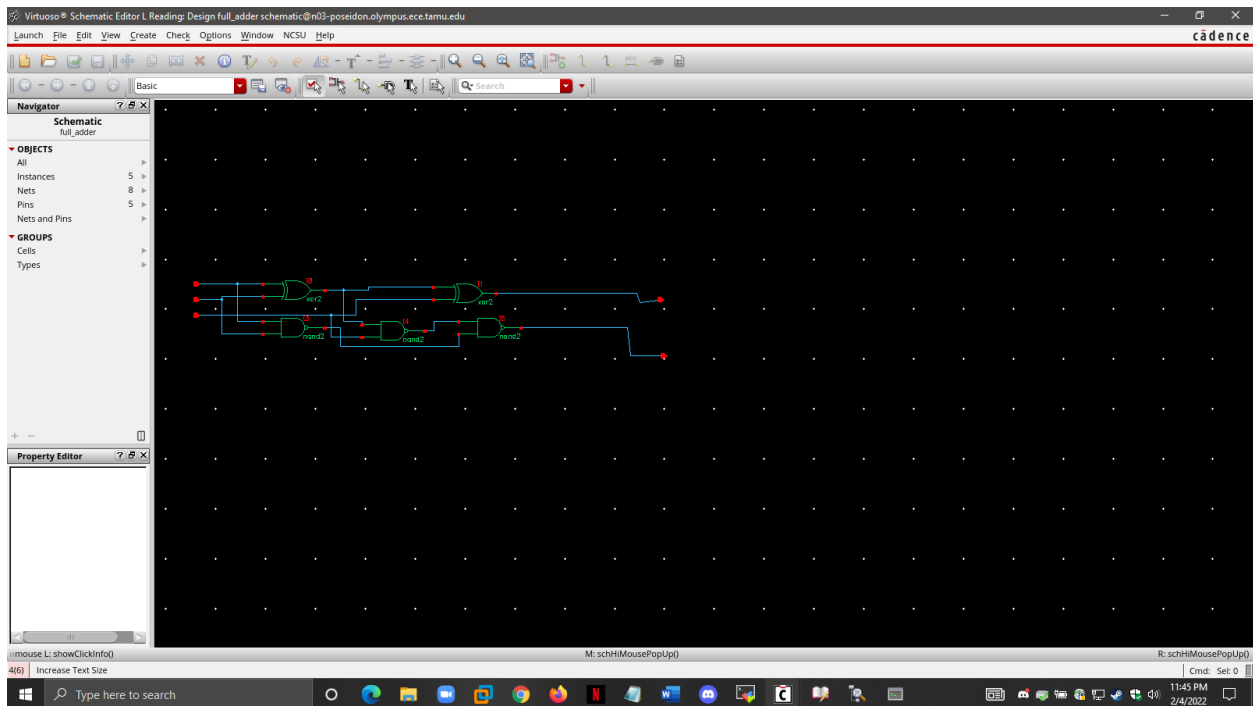
2/2/2022

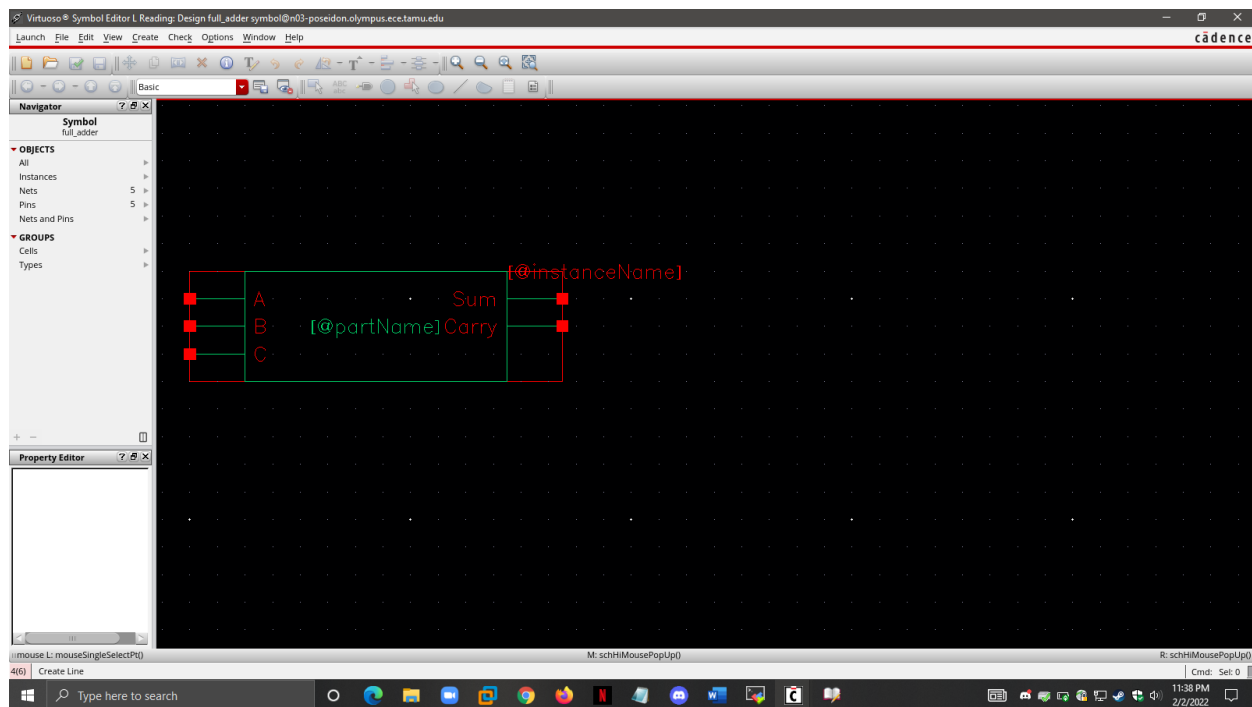
Introduction:

We will now begin the design by implementing the logic design of the 8-bit Pipelined adder. The following sections introduce you to the procedures to use Cadence for schematic capture and simulation which you will use to implement the required logic design.

Results:

Full adder:





```

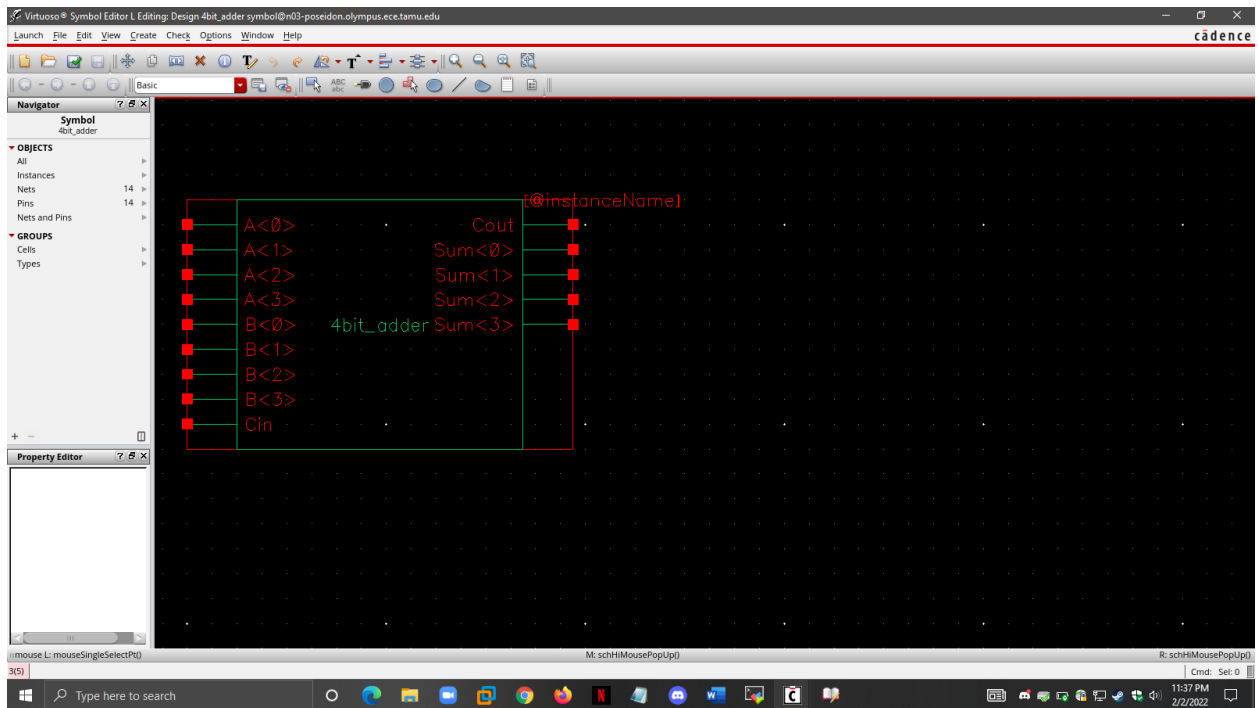
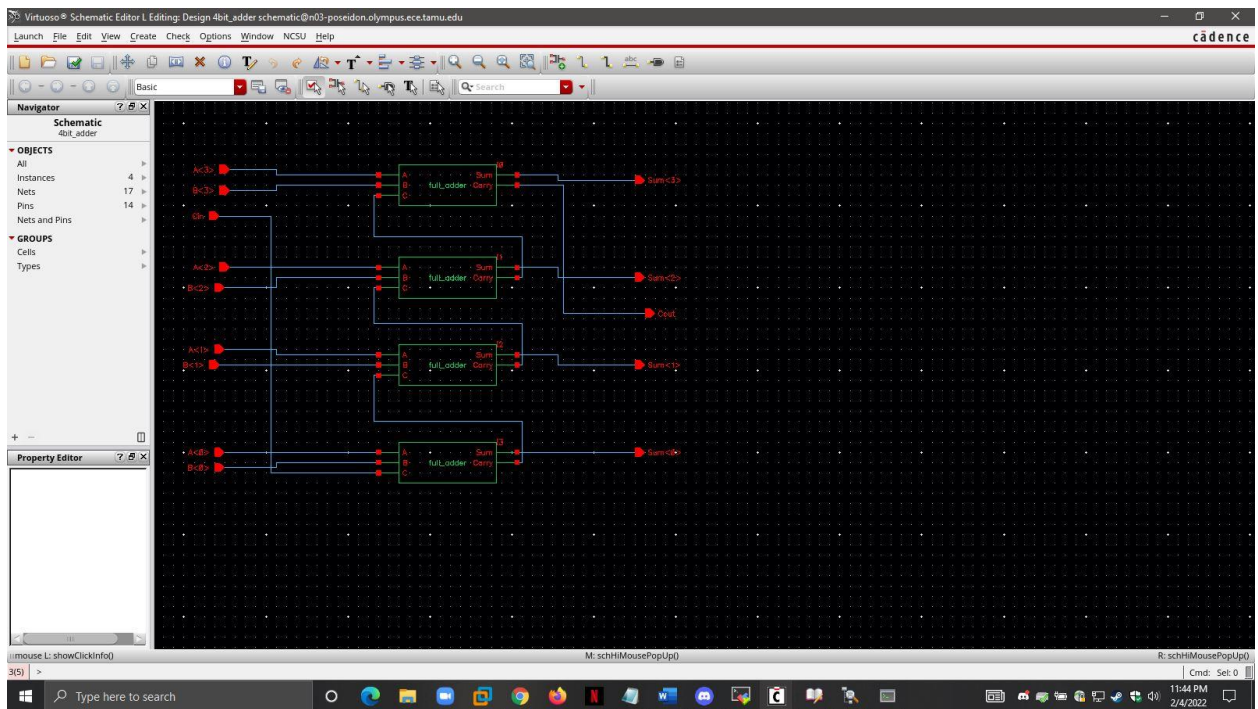
simout - Notepad
File Edit Format View Help
[TOOL: ncxlmode 15.20-s077: Started on Jan 28, 2022 at 17:53:34 CST
ncxlmode
+delay_mode_path
+typdelays
-1
simout.tmp
/home/ugrads/s/seakid/ecen454_714/full_adder_run1/testfixture.template
-f /home/ugrads/s/seakid/ecen454_714/full_adder_run1/verilog.infiles
/opt/coe/ncsu/ncsu-cdk-1.6.0.beta/11b/NCSU_Digital_Parts/nand2/functional/verilog.v
/opt/coe/ncsu/ncsu-cdk-1.6.0.beta/11b/NCSU_Digital_Parts/xor2/functional/verilog.v
ihnl/cds0/netlist
+nostdout
+nocopyright
+ncvlogargs+ " -neverwarn -nostdout -nocopyright "
+ncelabargs+ " -neg_tchk -nonotifier -sdf_NOCheck_celltype -access + " -pulse_e 100 -pulse_r 100 -neverwarn -timescale 1ns/1ns -nostdout -nocopyright"
+ncsimargs+ " -neverwarn -nocopyright -gui -input /home/ugrads/s/seakid/ecen454_714/full_adder_run1/.simtmpNCCmd "
+mpsession+virtuosol1263
+mpshost+n02-hera.olympus.ece.tamu.edu

-----
Relinquished control to SimVision...
ncsim>
ncsim> source /opt/coe/cadence/INCISIVE152/tools/inca/files/ncsimc
ncsim> database -open shmWave -shm -default -into shm.db
Created default SHM database shmWave
ncsim> probe -create -shm test -all -depth 1
Created probe 1
ncsim> run
0 A=0, B=0, C=0, SUM=0, CARRY=0
50 A=0, B=0, C=1, SUM=1, CARRY=0
100 A=0, B=1, C=0, SUM=1, CARRY=0
150 A=0, B=1, C=1, SUM=0, CARRY=1
200 A=1, B=0, C=0, SUM=1, CARRY=0
250 A=1, B=0, C=1, SUM=0, CARRY=1
300 A=1, B=1, C=0, SUM=0, CARRY=1
350 A=1, B=1, C=1, SUM=1, CARRY=1

ncsim> run
ncsim> run
ncsim> run
ncsim>

```

4bit Adder:



[illegible]

