

# Lab 5: Design & Simulation of 4-bit adder

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TA Sina

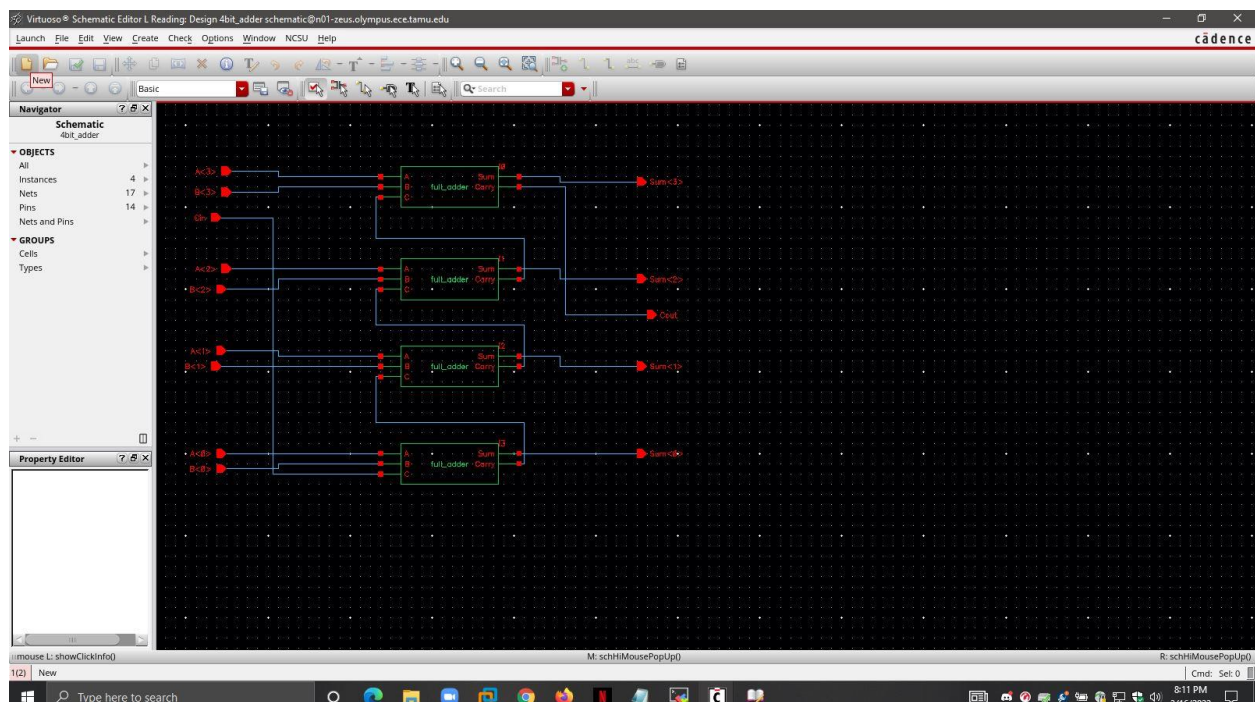
ECEN 454-504

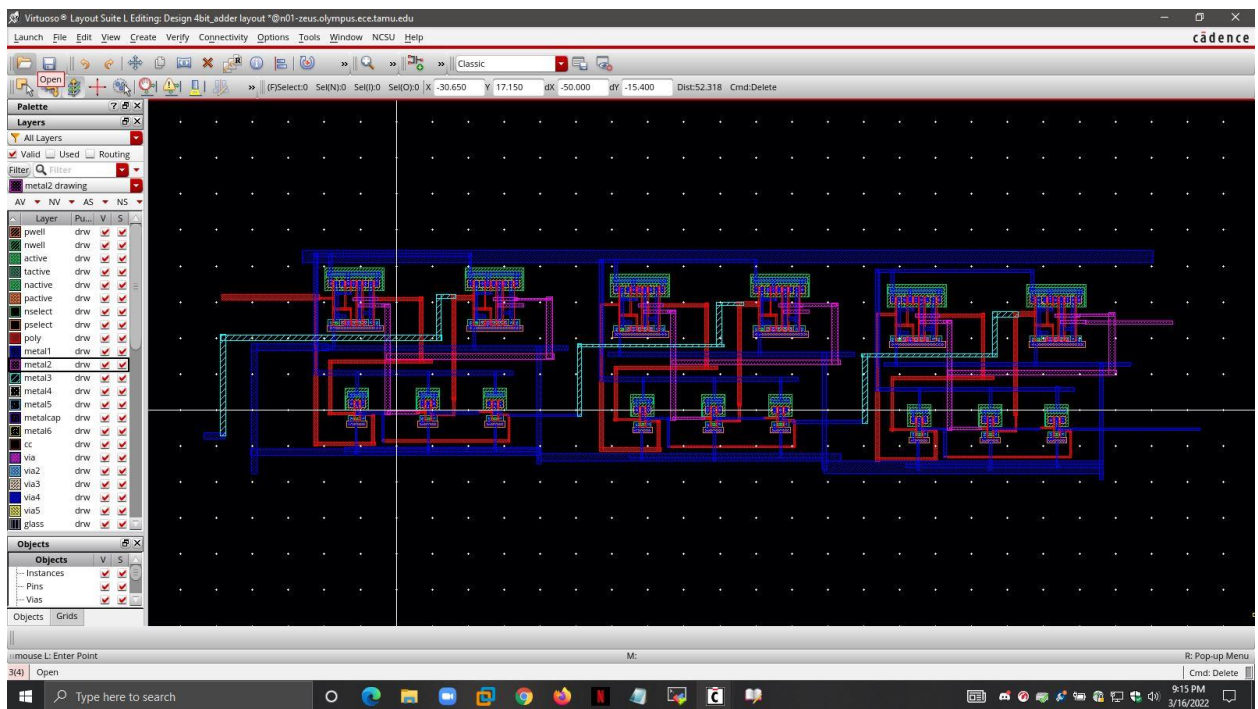
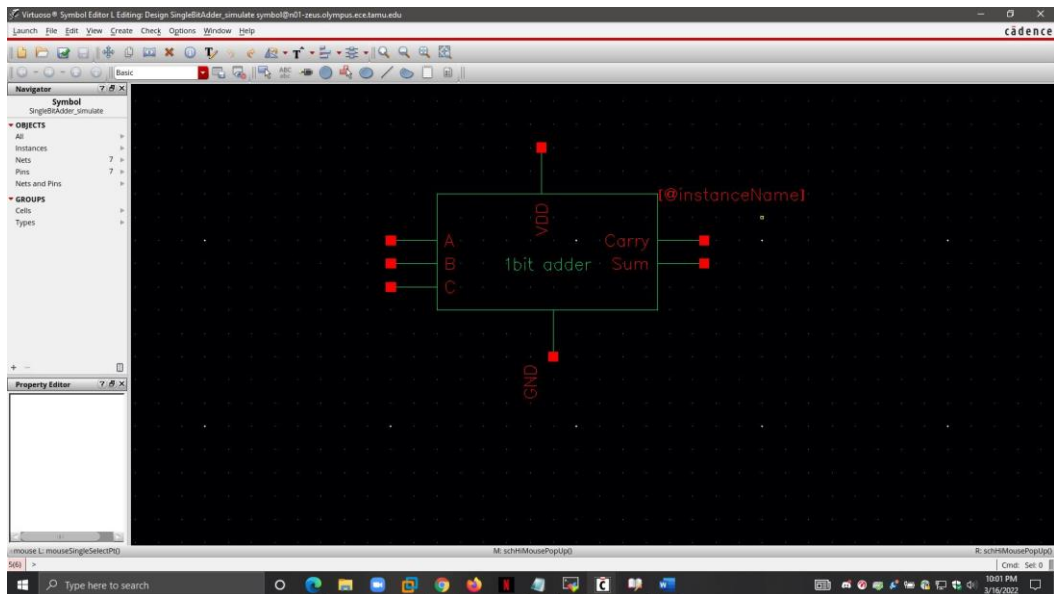
3/16/2022

## Introduction:

In this lab you will be designing the 4-bit adder circuit which will form one stage of the combinational logic required to build the complete 8-bit pipelined adder.

## Results:

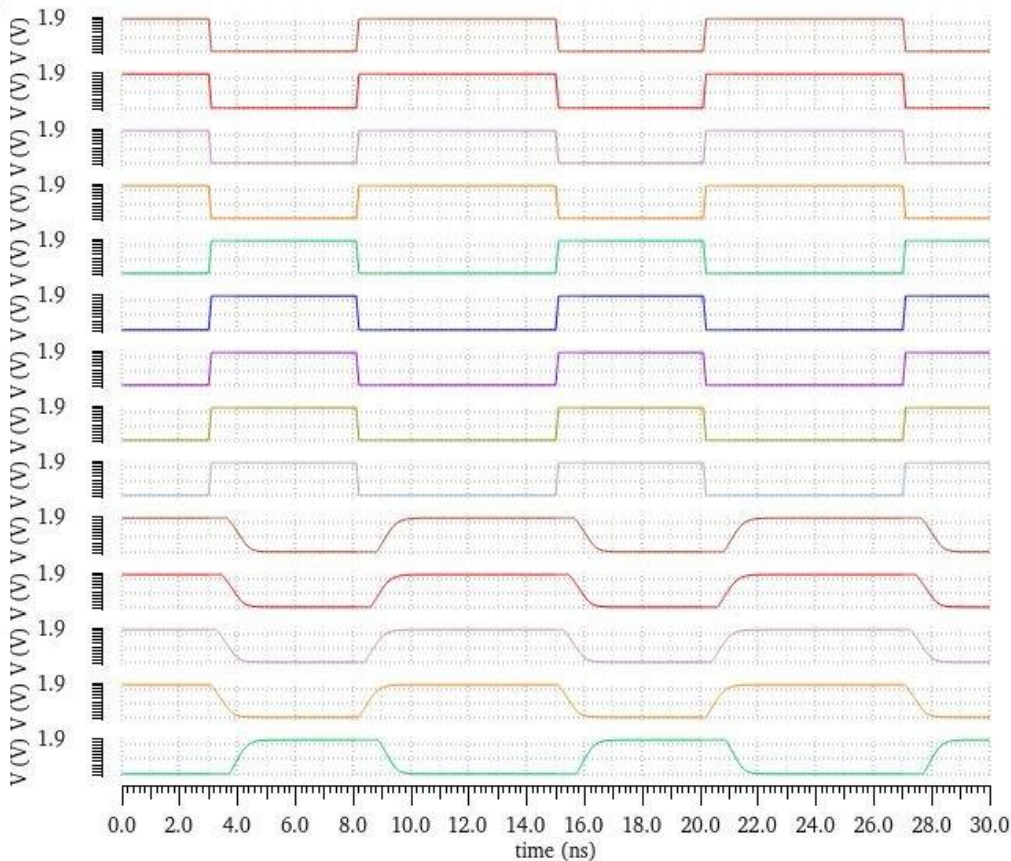




Transient Response

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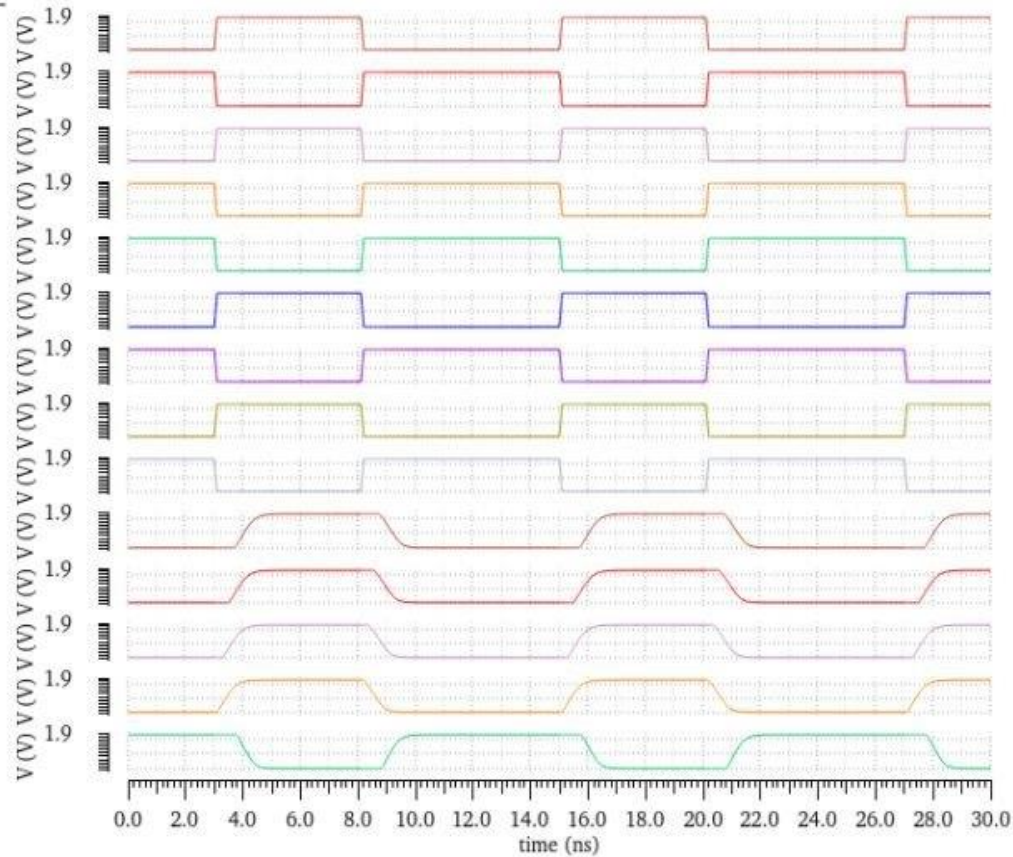
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# Transient Response

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# Transient Response

