Lab 3: Cell Characterization using Spectre

Connor Murphy

TA Sina

ECEN454-504

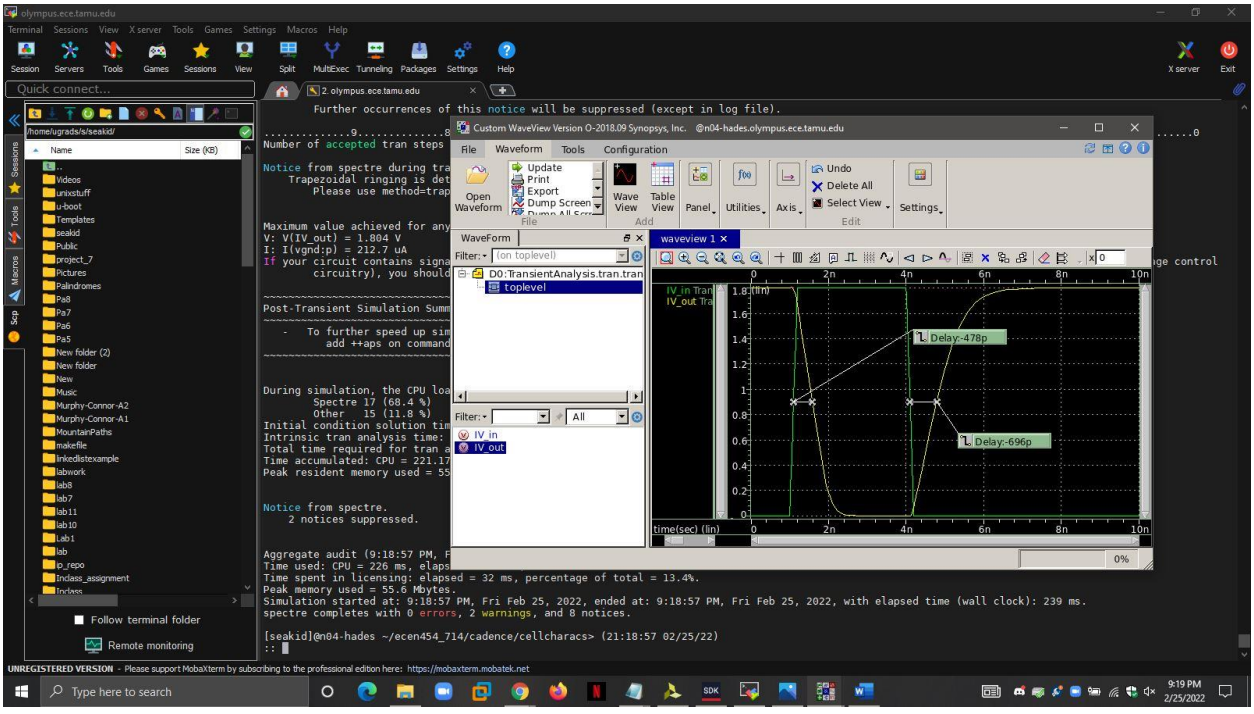
2/25/2022

Introduction:

In this lab session you will be required to characterize the standard cells that you have used in the design of the pipelined adder so far. Although cell characterization includes a wide number of parameters such as propagation delay, power, area, timing constraints in the case of sequential elements, input capacitance and global parameters like PVT(Process, Voltage, Temperature), corner selection, etc. In this lab you will be dealing only with the propagation delay and input capacitance of a standard cell by performing circuit simulations at the transistor level.

Results:

Inverter:

1. 

2.

inverter - Notepad

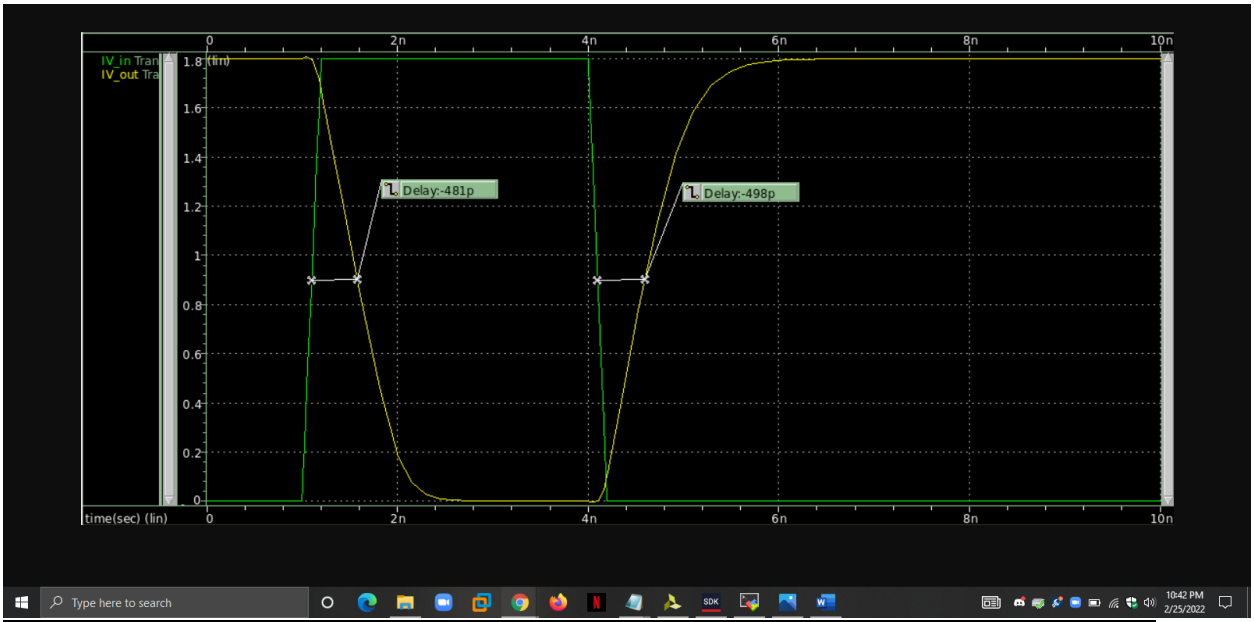
File Edit Format View Help

```
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "~/ecen454_714/cadence/cellcharacs/model18.spi"
include "~/ecen454_714/cadence/cellcharacs/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

vpwl (IV_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

X1 (IV_in IV_out vdd gnd) IV wp=0.6u lp=0.2u wn=0.3u ln=0.2u

R1 (IV_out 1) resistor r=1
C1 (1 0) capacitor c=100f

TransientAnalysis tran start=0 stop=10ns step=1ps
save IV_in IV_out
```

Ln 12, Col 36 100% Windows (CRLF) UTF-8

Type here to search 9:17 PM 2/25/2022

3.

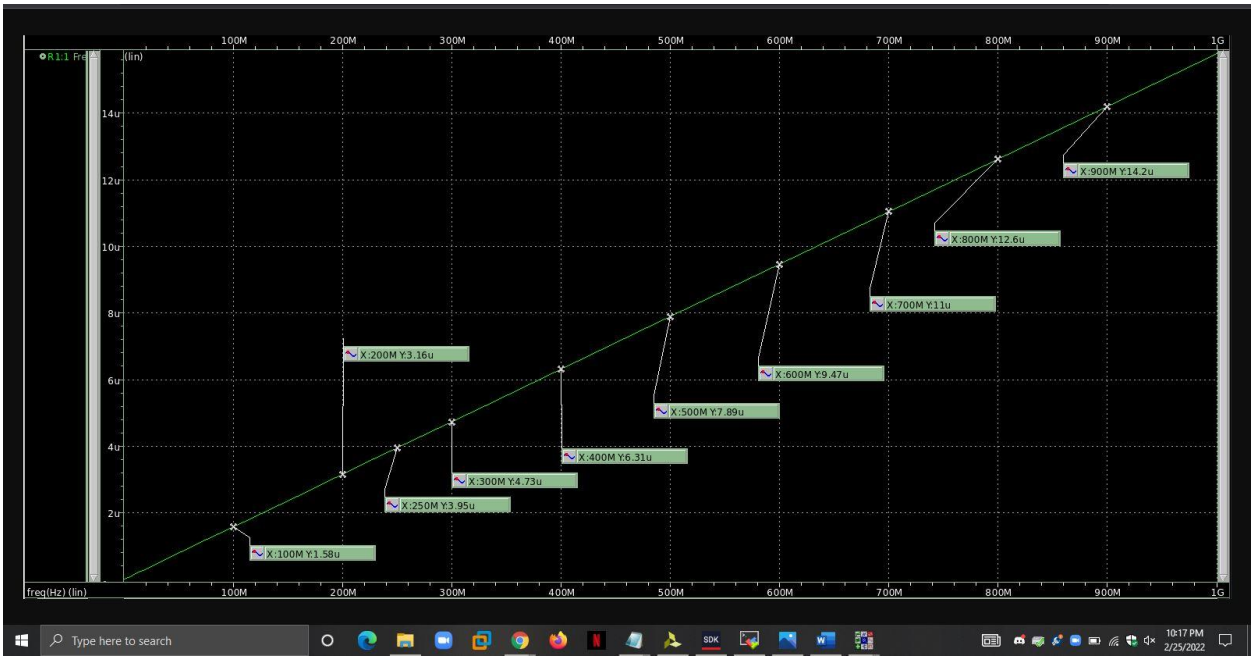


Type here to search 10:42 PM 2/25/2022

Capacitance values	Falling Delay	Rising Delay	Error: (Difference of delays/falling delay)
100p	-481p	-498p	3.534%
20p	-131p	-144p	9.92%
25	-153p	-166p	8.49%
30	-175p	-188p	7.42%

35	-197p	-210p	6.59%
40	-219p	-232p	5.93%
45	-240p	-255p	6.25%
50	-262p	-276p	5.34%
55	-284p	-297p	4.57%
60	-306p	-321p	4.90%
65	-329p	-325p	4.86%
70	-351p	-368p	4.84%
75	-373p	-389p	4.28%
80	-393p	-410p	4.32%

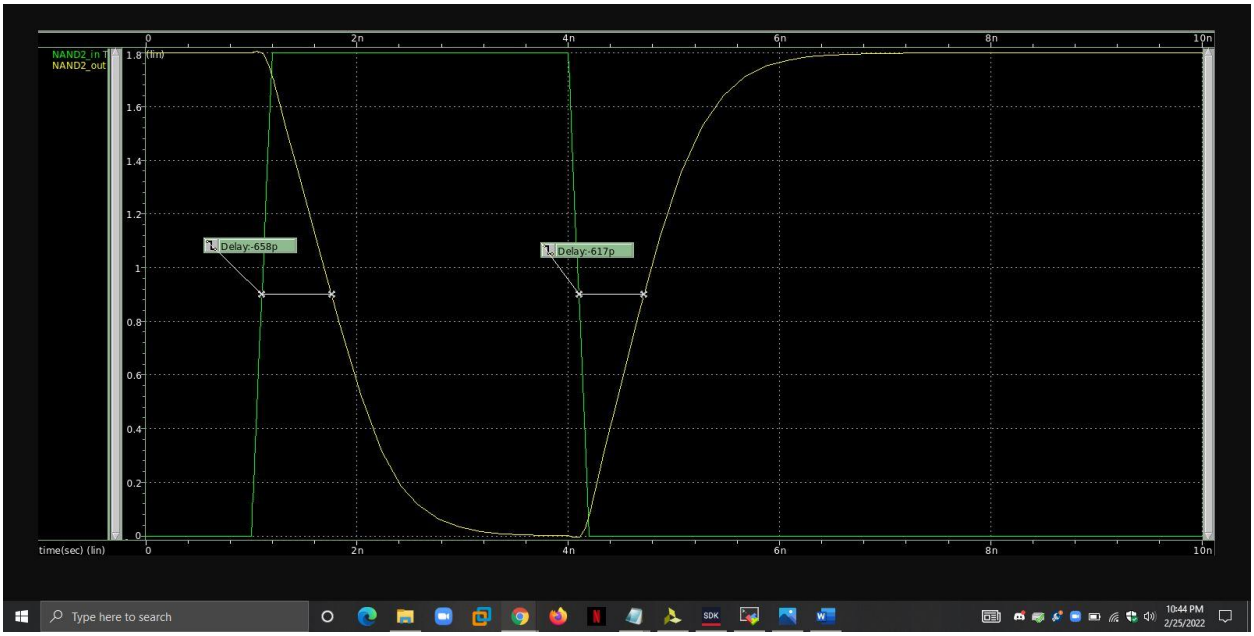
4.



Sink capacitance:

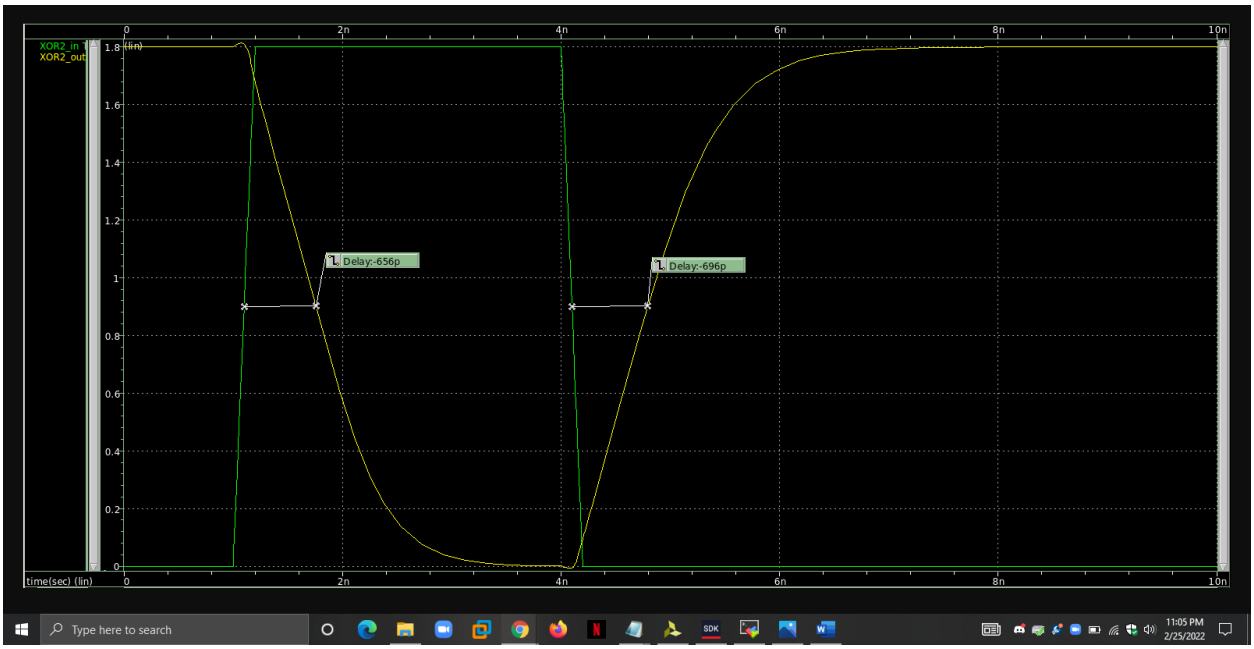
Frequency(MHz)	Ifrequency(uA)	Capacitance(fF)
100	1.58	2.515
200	3.16	2.515
250	3.95	2.515
300	4.73	2.509
400	6.31	2.511
500	7.89	2.511
600	9.47	2.512
700	11.0	2.501
800	12.6	2.507

900	14.2	2.511
Sink Capacitance: 2.511fF		

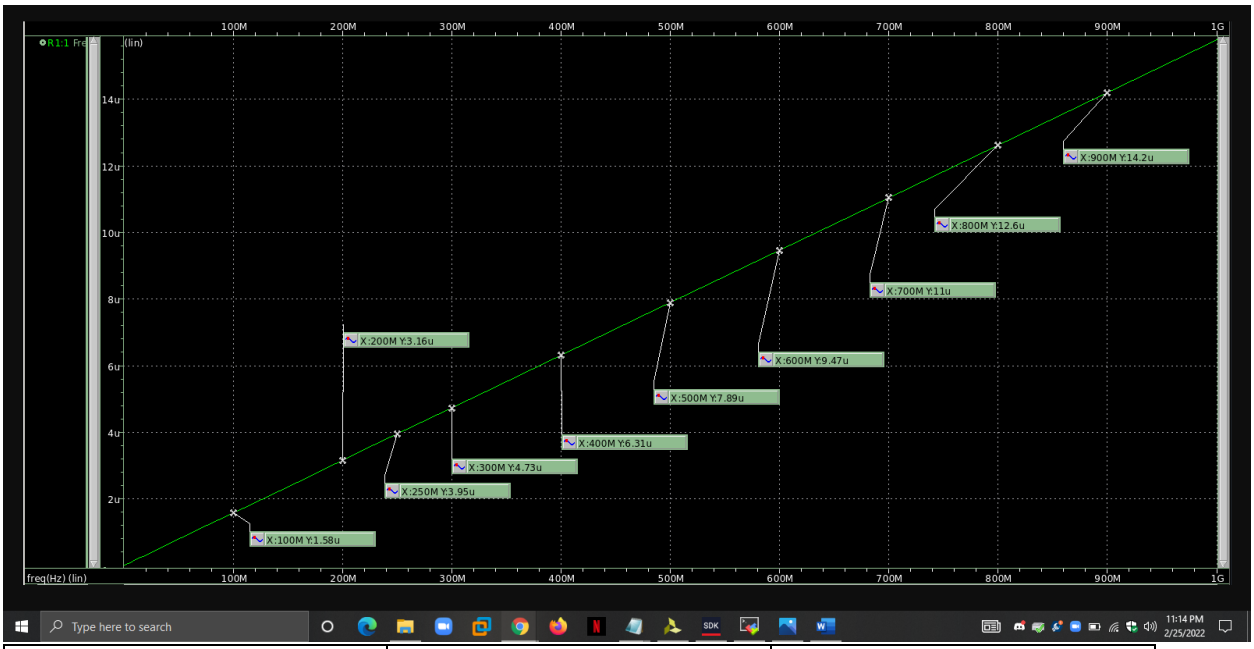


Capacitance values(fF)	Rising Delay	Falling Delay	Error: (Difference of delays/falling delay)
1	-38.6p	-54.9p	42.23%
5	-74.8p	-87.2p	16.58%
10	-109p	-116p	6.42%
20	-170p	-172p	1.18%
25	-200p	-200p	0.00%
30	-232p	-227p	2.20%
40	-293p	-284p	3.17%
50	-353p	-341p	3.52%
60	-416p	-395p	5.32%
70	-476p	-451p	5.54%
75	-506p	-478p	5.86%
80	-535p	-505p	6.14%
85	-567p	-535p	5.98%
90	-598p	-562p	6.41%
100	-658p	-617p	6.65%

XOR:

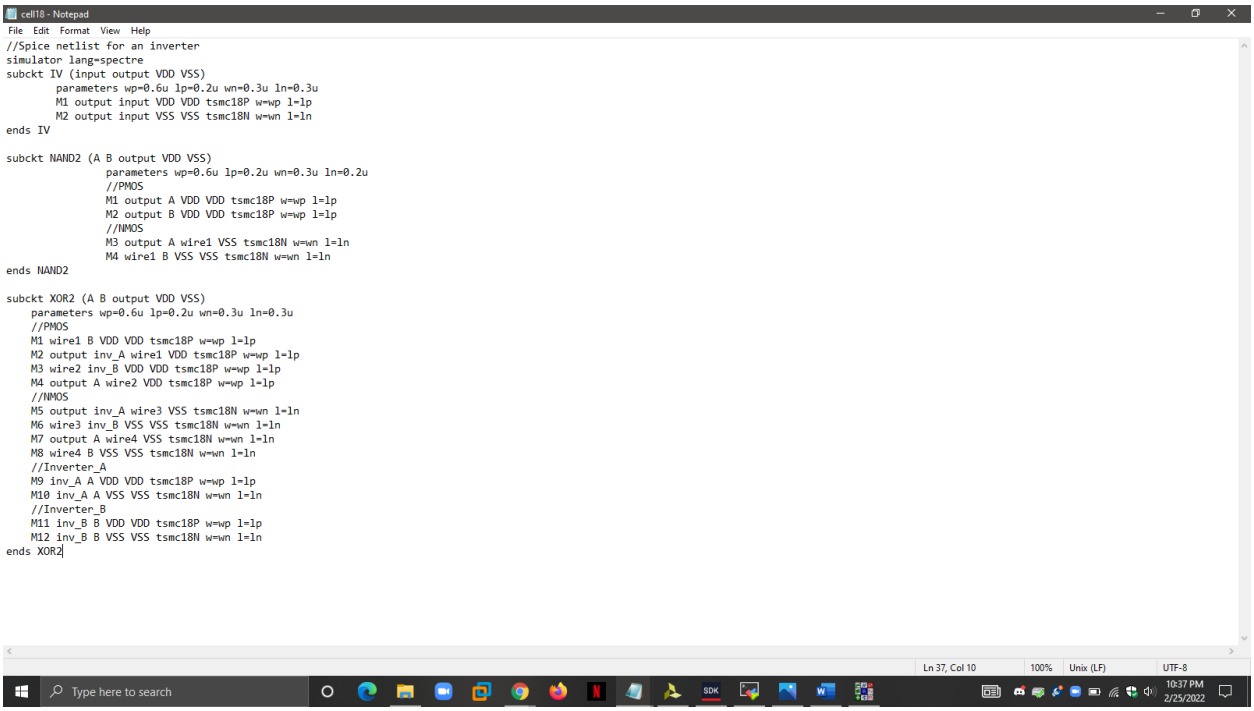


Capacitance values(fF)	Rising Delay	Falling Delay	Error: (Difference of delays/falling delay)
1	-41.3p	-51.3p	24.21%
5	-70.4p	-81.7p	16.05%
10	-103p	-117p	13.59%
20	-166p	-182p	9.64%
25	-197p	-214p	8.63%
30	-228p	-247p	8.33%
40	-290p	-311p	7.24%
50	-351p	-374p	6.55%
60	-412p	-441p	7.40%
70	-473p	-503p	6.34%
75	-504p	-537p	6.55%
80	-535p	-569p	6.36%
85	-566p	-599p	5.83%
90	-596p	-633p	6.21%
100	-656p	-696p	6.10%



Frequency(MHz)	Ifrequency(uA)	Capacitance(fF)
100	4.89	7.783
200	9.77	7.775
250	12.2	7.767
300	14.7	7.799
400	19.5	7.759
500	24.4	7.653
600	29.3	7.764
700	34.2	7.771
800	39.0	7.7789
900	43.9	7.775
Sink Capacitance: 7.772fF		

5.


cell18 - Notepad
File Edit Format View Help
//Spice netlist for an inverter
simulator lang=spectre
subckt IV (input output VDD VSS)
parameters wp=0.6u lp=0.2u wn=0.3u ln=0.3u
M1 output input VDD VDD tsmc18P w=wp l=lp
M2 output input VSS VSS tsmc18N w=wn l=ln
ends IV
subckt NAND2 (A B output VDD VSS)
parameters wp=0.6u lp=0.2u wn=0.3u ln=0.2u
//PMOS
M1 output A VDD VDD tsmc18P w=wp l=lp
M2 output B VDD VDD tsmc18P w=wp l=lp
//NMOS
M3 output A wire1 VSS tsmc18N w=wn l=ln
M4 wire1 B VSS VSS tsmc18N w=wn l=ln
ends NAND2
subckt XOR2 (A B output VDD VSS)
parameters wp=0.6u lp=0.2u wn=0.3u ln=0.3u
//PMOS
M1 wire1 B VDD VDD tsmc18P w=wp l=lp
M2 output inv_A wire1 VDD tsmc18P w=wp l=lp
M3 wire2 inv_B VDD VDD tsmc18P w=wp l=lp
M4 output A wire2 VDD tsmc18P w=wp l=lp
//NMOS
M5 output inv_A wire3 VSS tsmc18N w=wn l=ln
M6 wire3 inv_B VSS VSS tsmc18N w=wn l=ln
M7 output A wire4 VSS tsmc18N w=wn l=ln
M8 wire4 B VSS VSS tsmc18N w=wn l=ln
//Inverter_A
M9 inv_A A VDD VDD tsmc18P w=wp l=lp
M10 inv_A A VSS VSS tsmc18N w=wn l=ln
//Inverter_B
M11 inv_B B VDD VDD tsmc18P w=wp l=lp
M12 inv_B B VSS VSS tsmc18N w=wn l=ln
ends XOR2
Ln 37, Col 10
100%
Unix (LF)
UTF-8
Type here to search
10:37 PM
2/25/2022