Lab 9: Optimization using Logical Effort

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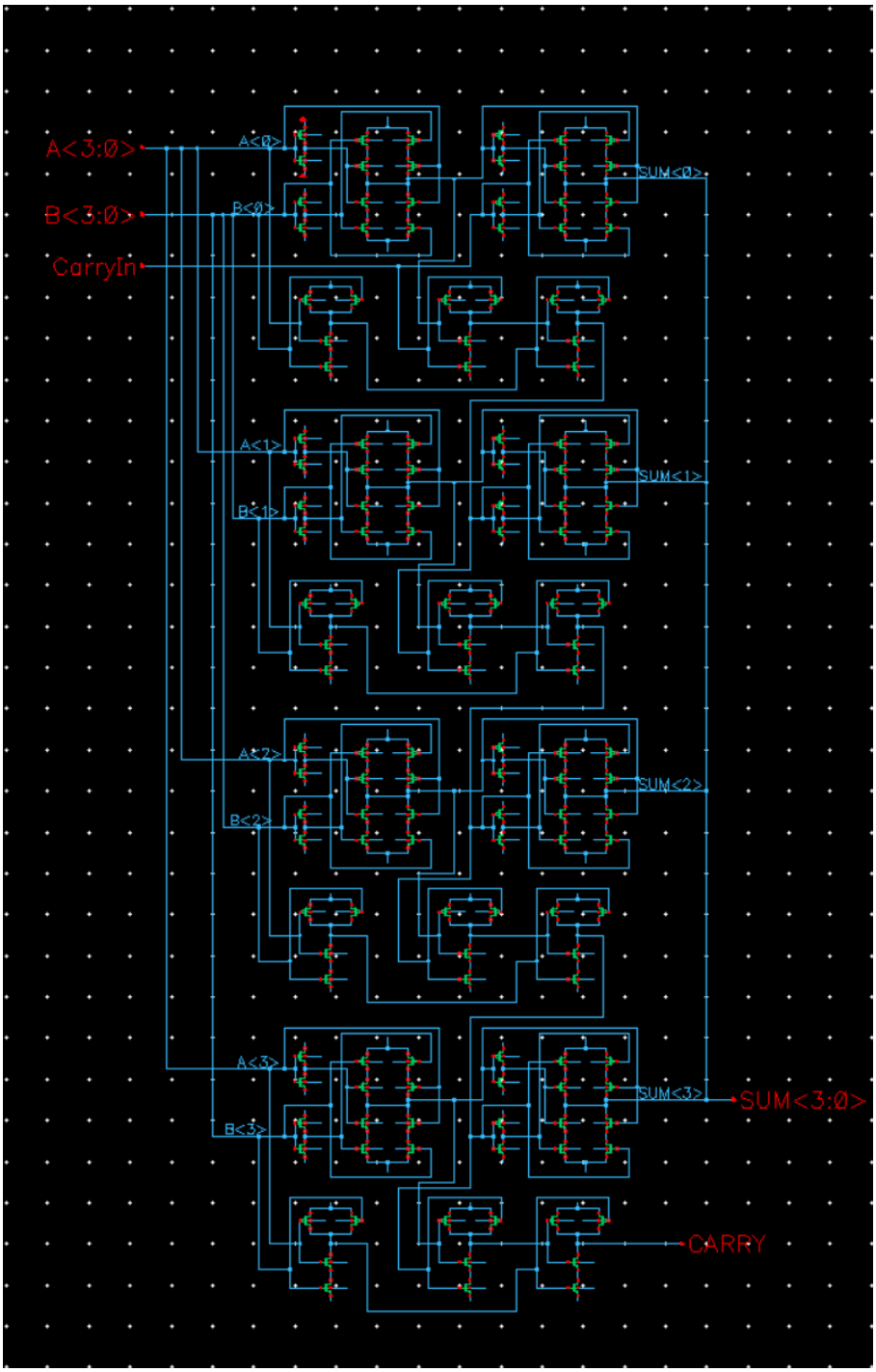
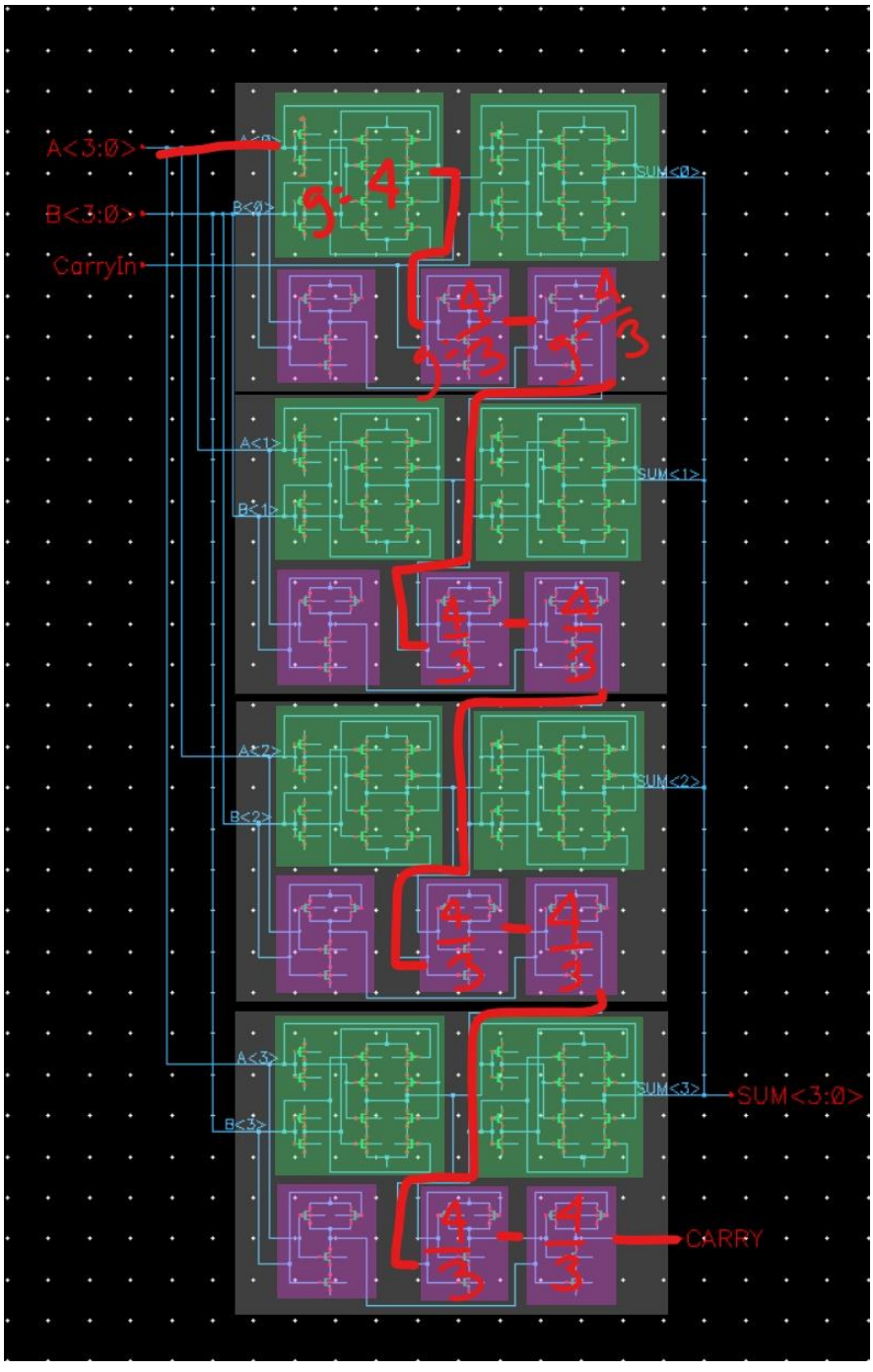
Introduction:

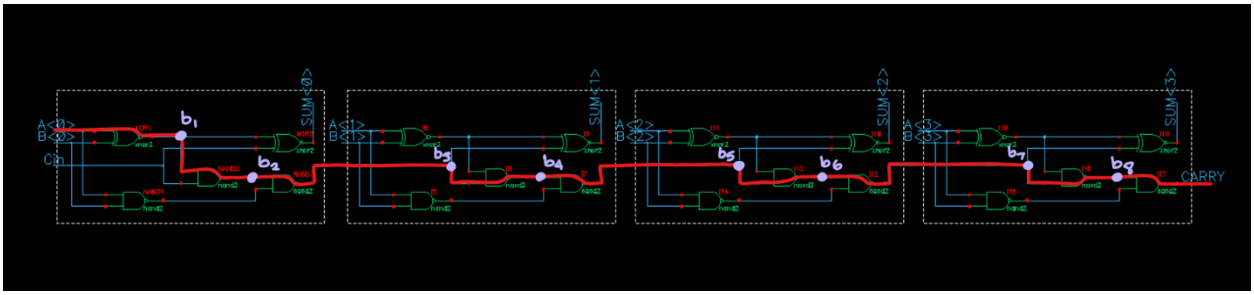
In this lab you have to identify the critical path in your design (4 bit adder), and reduce the delay of this path by determining the optimal number of devices and sizes of the gates that lie along this path. You have to use the Logical Effort and Gate sizing techniques you learn in the course.

Results:

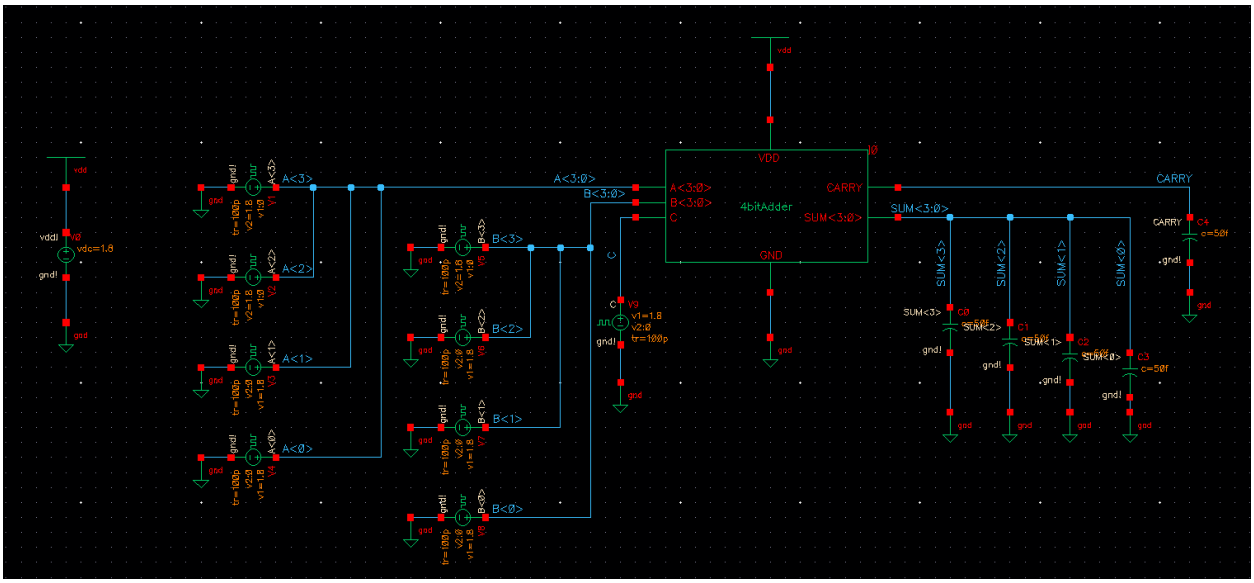
4-bit adder transistors:


A<3:0>
B<3:0>
CarryIn
A<0>
B<0>
SUM<0>
A<1>
B<1>
SUM<1>
A<2>
B<2>
SUM<2>
A<3>
B<3>
SUM<3>
SUM<3:0>
CARRY

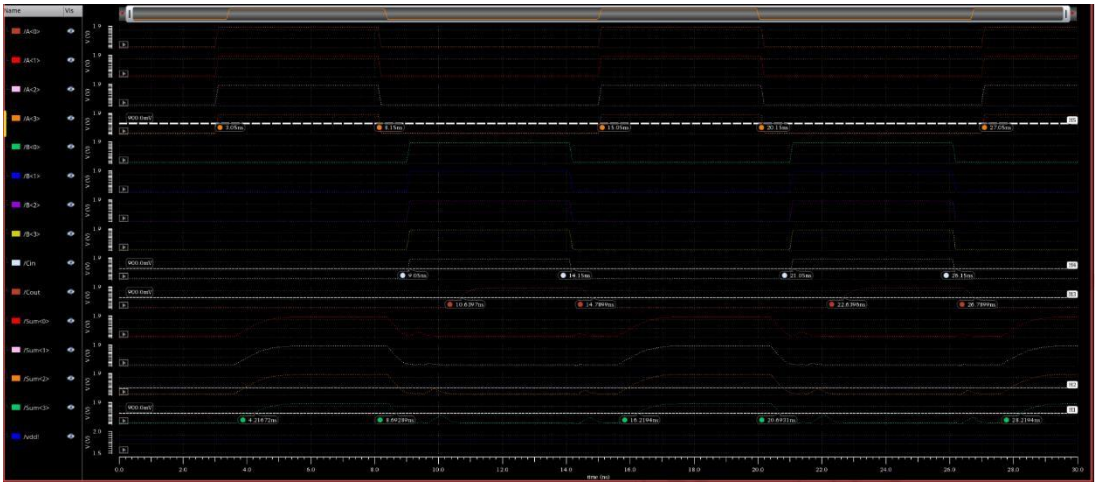

A<3:0>
B<3:0>
CarryIn
A<0>
B<0>
SUM<0>
A<1>
B<1>
SUM<1>
A<2>
B<2>
SUM<2>
A<3>
B<3>
SUM<3>
SUM<3:0>
CARRY


A<0>
B<0>
Cin
SUM<0>
b1
b2
A<1>
B<1>
SUM<1>
b3
b4
A<2>
B<2>
SUM<2>
b5
b6
A<3>
B<3>
SUM<3>
b7
b8
CARRY

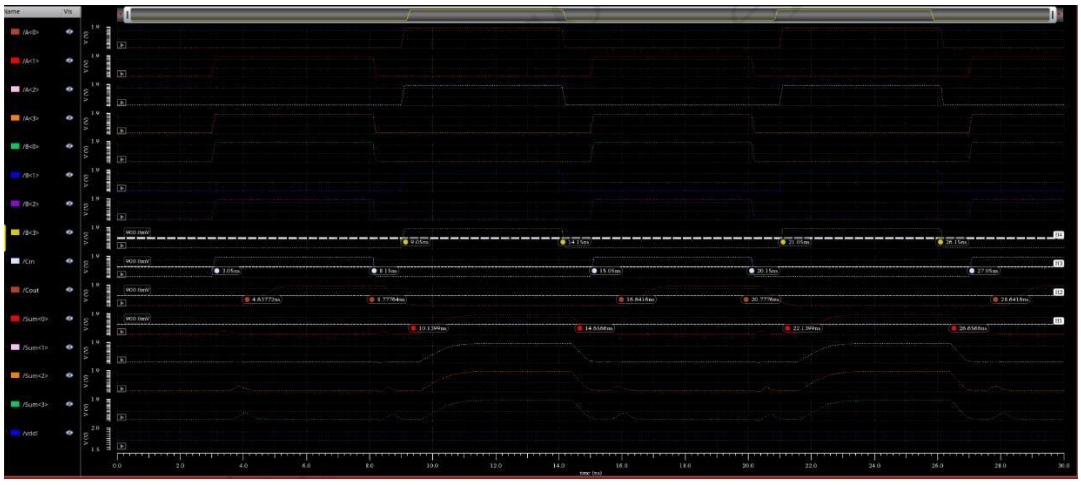
Schematic:


vdd
vdd!
gnd!
gnd
vdc=1.8
A<3>
A<2>
A<1>
A<0>
B<3>
B<2>
B<1>
B<0>
A<3:0>
B<3:0>
C
VDD
A<3:0>
B<3:0>
C
4bitAdder
CARRY
SUM<3:0>
GND
SUM<3:0>
SUM<3>
SUM<2>
SUM<1>
SUM<0>
CARRY
C0
C1
C2
C3
C4
c=50f

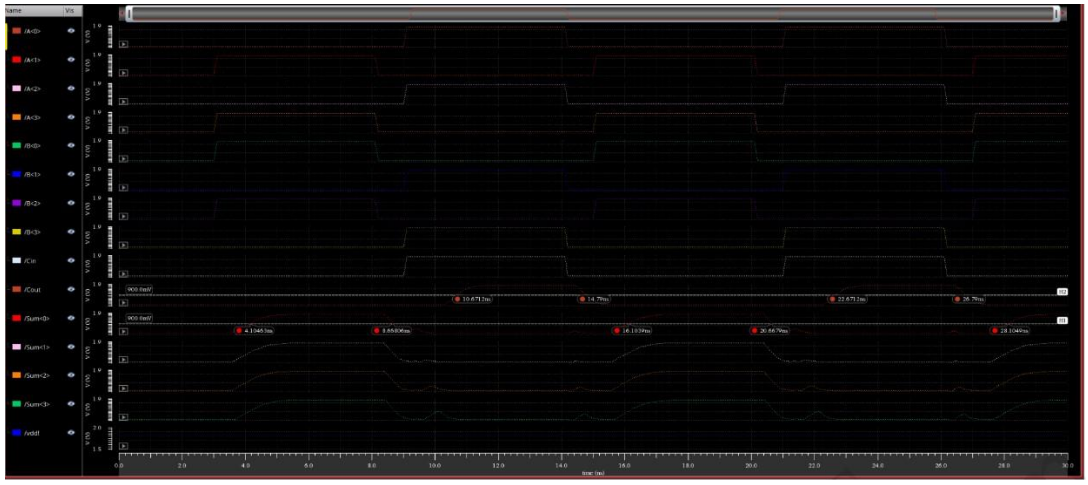
A=0000 B=1111 Cin=1



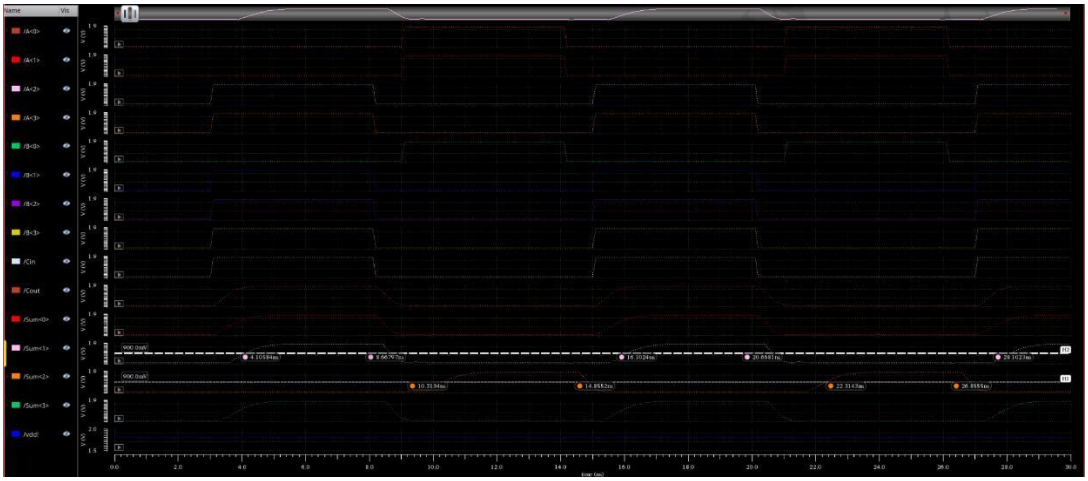
: A=1010 B=0101 Cin=0



A=1010 B=0101 Cin=1



A=1100 B=1000 Cin=0



input	**output**	**Non optimized time (ns)**	Optimized time **(ns)**
A: 0000 **B: 1111** **Cin: 1**	Cout S<0> S<1> S<2> S<3>	1.63 1.102 1.102 1.104 1.104	1.5870 1.1335 1.1335 1.1462 1.1462

A: 1010 **B: 0101** **Cin: 0**	Cout S<0> S<1> S<2> S<3>	1.6893 1.114 1.101 1.124 1.124	1.5877 1.0899 1.0910 1.0899 1.0905
A: 1010 **B: 0101** **Cin: 1**	Cout S<0> S<1> S<2> S<3>	1.1218 1.1017 1.1147 1.1017 1.1147	1.621 1.0899 1.0546 1.0899 1.0546
A: 1100 **B: 1000** **Cin: 0**	Cout S<0> S<1> S<2> S<3>	0.5264 0.7937 1.155 1.105 1.4959	0.4952 1.0546 1.0852 1.0758 1.0985

Case	**Non-Optimized power (µW)**	**Optimized power (µW)**
A: 0000 **B: 1111** **Cin: 1**	-190.8	-157.5
A: 1010 **B: 0101** **Cin: 0**	-191.7	-159.3
A: 1010 **B: 0101** **Cin: 1**	-192.2	-157.1
A: 1100 **B: 1000** **Cin: 0**	-127.1	-109.5

	Non-Optimized	Optimized
Area (μ^2m^2)	11.86	12.602