Semiconductor Materials for Ultra High Frequency Transistors

Pongpak Techagumthorn
Physical Sciences Division
Univ. of Washington Bothell
Bothell, USA
pongpakt@uw.edu

***Abstract*—Our modern day world is ever more reliant on connected devices. Inside every one of these devices there is a microprocessor inside. Currently the overwhelming majority of these microprocessors are constructed from silicon. As technology progresses we require ever faster processors. We are at a point now where we are reaching the limits of what silicon can provide. Scientists and engineers have turned to new semiconductor materials to overcome these limits. One such semiconductor material is Indium Gallium Phosphide (InGaP).**

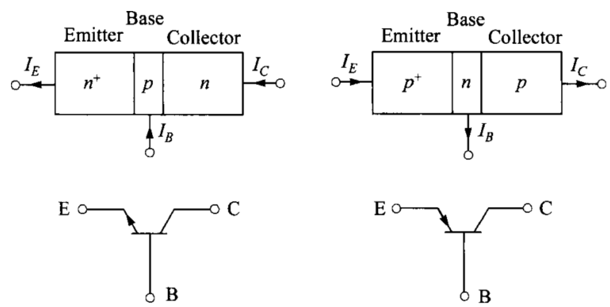
This project aims to compare ultra-high frequency (0.3 - 3 GHz) characteristics of Silicon and Indium Gallium Phosphide in an LTSpice environment. For the transistor model we will be using the hybrid-*pi* equivalent circuit transistor model. On the silicon side of things we will be simulating the general purpose 2N3904 NPN transistor. For the InGaP transistor we will be looking at the ERA-50SM+ device. Before simulating a complex device such as the ERA-50SM+ we started with small scale common emitter and common collector amplifier circuits. After running or small scale simulations we realized that the hybrid-*pi* model was inadequate for our tests. Due to time constraints we were not able to come to a consensus for our research question.

***Index Terms*—Transistors, Semiconductors, Silicon, InGaP, LTSpice**

I. Introduction

A. Background

EVERYWHERE we look more and more of our devices are being connected to the internet, from our phones and computers to our cars and even our kitchen appliances. These so called "smart devices" are made to accomplish a myriad of tasks but share one thing in common, they all have some sort of microprocessor inside them to control what they do. Looking back at the history of microprocessors, and the transistors that provided their building blocks, the prevailing semiconductor material used within these devices has been silicon. The earliest transistors were constructed from germanium due to the ease of production at a high purity monocrystalline form [1]. In the early 1950s a way to produce monocrystalline silicon was developed and since then the industry has largely switched over to silicon. From the onset of transistor technology scientists knew that silicon would be superior to germanium for transistors [2]. The larger band gap in silicon made silicon-based transistors more reliable and less susceptible to random noise from internal and external sources [1], [2]. The earliest, and most basic, transistors were bipolar junction transistors (BJTs). These BJT devices consist of three semiconductor regions of alternating positive-negative-positive (PNP) or negative-positive-negative (npn) doping, shown in fig. [3]. The two junctions allow small base input currents to control much higher currents between the collector and emitter [3]. This allows BJTs to function as either a swicth or an amplifier [4].



(a) NPN (b) PNP

Fig. 1: Simplified internal construction, nomenclatures, and symbols of (a) NPN and (b) PNP transistors
Source: Adapted from [3]

In the past decade we have gotten closer and closer to the limits of silicon BJTs, especially in ultra high and extremely high frequency applications that operate in the order of 1 – 100 GHz (10^9 Hz – 10^{11} Hz) [5]. One solution that scientists and engineers have tuned to is the use of newer semiconductor materials. These new materials have electrical properties that are more suited for ultra high (UHF) to extremely high frequency (EHF) applications and beyond [6]. Some new semiconductor materials that have already been implemented to address these limitations include Indium and Gallium based semiconductor materials [5].

An example of a device that makes use of Indium based transistors, specifically Indium Gallium Phosphide (InGaP), is Kenichiro Aoki and Takahisa Mitsui's classic tabletop direct speed of light measurement lab [7].The lab uses a very high speed laser pulse and a detector to directly measure the speed of light, seen in fig. 2 . Inside the pulse circuit there is an ERA-50SM+ wide band monolithic amplifier that supports signals from DC up to 2 GHz [8]. This amplifier uses a pair of NPN

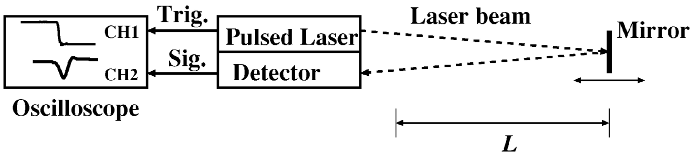


Fig. 2: Block diagram of the Aoki and Mitsui speed of light lab. The ERA-50SM+ device is part of the Pulsed Laser circuitry
Source: [7]

InGaP heterojunction bipolar transistors (HBT) in a Darlington pair, seen in fig. 3. HBTs function on the same principle as BJTs but instead of having the same semiconductor material at the 2 outer

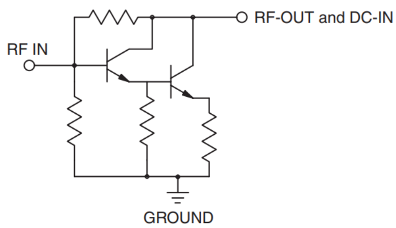


Fig. 3: Simplified internal schematic of the ERA-50SM+ wide band monolithic amplifier
Source: [8]

Another solution that scientists and engineers use to overcome the limits of silicon BJTs is using faster switching transistor technologies. Technologies such as Field Effect Transistors (FET) are much better suited for these frequencies [5]. For this paper we choose to focus only on differing semiconductor materials in junction transistors, a superset of BJTs and HBTs, since the ERA-50SM+ device exclusively uses this type of transistor.

B. Purpose

The goal of this project is to run simulations on InGaP HBTs and silicon BJTs and within an LTSpice environment to determine the more suitable semiconductor material for ultra high frequency applications. Additionally we will also determine suitable applications for each semiconductor material and the intrinsic electrical properties that make one semiconductor more suitable for ultra high frequency applications over another.

II. Methods

A. Evaluation Methods

To evaluate the performance of the InGaP HBTs in comparison to standard silicon BJTs we will be simulating the ERA-50SM+ internal circuit from fig. 3 within the manufacturer prescribed evaluation circuit, shown in fig. 4. For the ERA-50SM+ device in fig. 4 we will be constructing the internal circuitry as shown in fig. 3 with both silicon and InGaP parameters

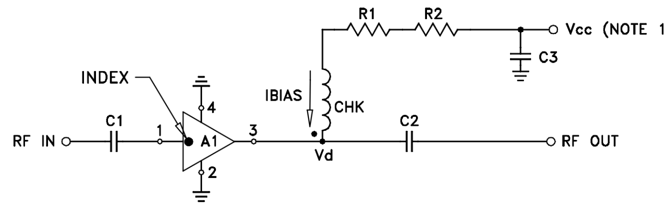
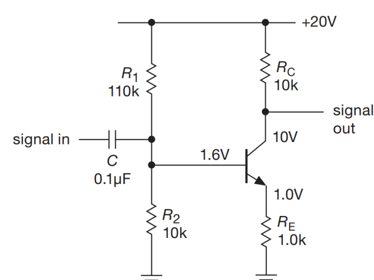


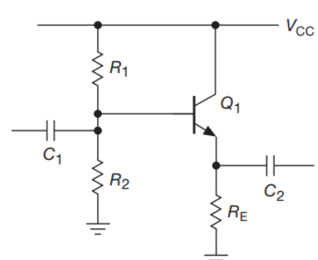
Fig. 4: ERA-50SM+ evaluation circuit as prescribed by the manufacturer
Source: [8]

Before simulating the entire ERA-50SM+ device in the prescribed evaluation circuit, fig. 4 we will first simulate each type of transistor within simple circuits. We will compare the simple circuit results to manufacturer provided performance metrics to verify that the simulated components matches expected real world performance. For the silicon BJT model we will be simulating the 2N3904 NPN BJT with parameters from KEC Semiconductor Corp [9]. For the InGaP HBT model we will be determining parameters from literature [10], [11] as we do not know the specific parameters for the HBTs within the ERA-50SM+ device.

For the simple circuit testing we will be using basic common emitter and common collector transistor amplifier circuits, fig. 5a and 5b respectively. The common emitter amplifier configuration produces a simple voltage amplification circuit and the common collector circuit produces a simple current amplification circuit



(a) Common Emitter



(b) Common Collector

Fig. 5: Simple NPN amplifier circuits
Source: [4]

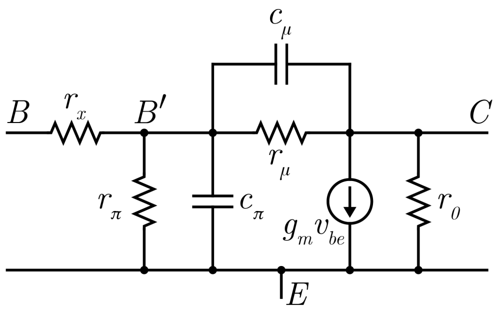


Fig. 6: Hybrid-π equivalent circuit model for NPN transistors

B. Hybrid-π Model

To model the transistor devices we will be using the hybrid-π equivalent circuit model, shown in fig. 6. The hybrid-π model was chosen since its parameters are easily calculated from information provided in component datasheets and its relative accuracy in modeling junction transistor behavior across low and high frequencies [12], [13]. This model is able to function across a wide range of frequencies since it takes into account both basic parameters and parasitic electrical properties of junction transistors [12]. The basic parameters needed for a simple hybrid-π model are the input resistance r_π, output resistance r_0, and the transconductance $g_m v_{be}$ [13]. These three parameters are adequate for dc and low frequency simulations but for higher frequency simulations we need to add addition parasitic elements. The base-emitter capacitance c_π, spreading resistance r_x, feedback resistance r_μ, and interelectrode capacitance c_μ compensate for high frequency effects within the stricture of the transistor [12].

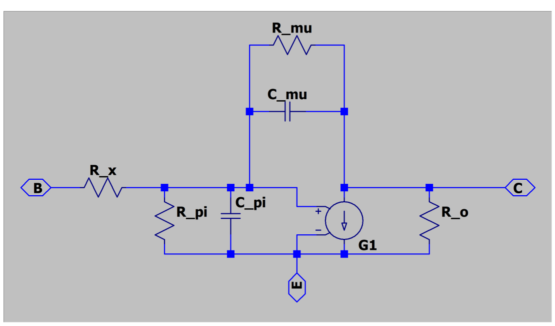


Fig. 7: Hybrid-π model in LTSpice

III. Analysis

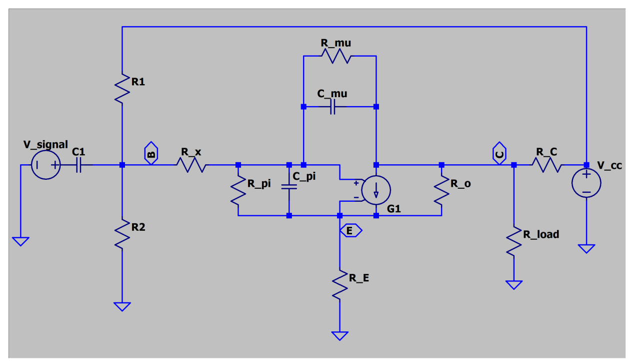
A. LTSpice Models

We used SPICE (Simulation Program with Integrated Circuit Emphasis) software to run our simulations, specifically the LTSpice distribution by Analog Devices. The simulation setup in LTSpice consists of graphically laying out a circuit, assigning values to the components, configuring simulation parameters, and running the simulation. fig. 7 shows the hybrid-π model from fig. 6 set up in LTSpice. This model is not quite complete enough to run a simulation since the values of each component has not been assigned yet and there are no power and signal related components.

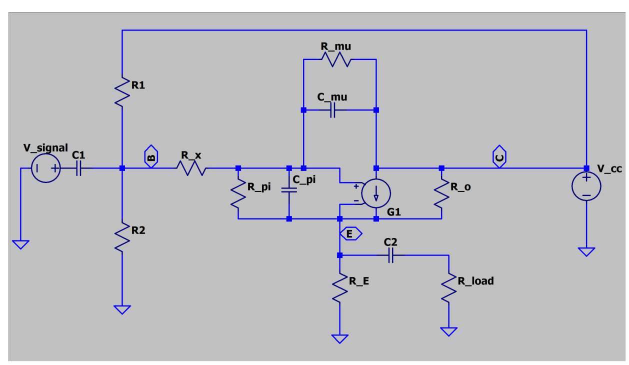
TABLE I: Calculated parameters for hybrid-π models

Parameter	Si	InGaP	Unit
g_m	3.894×10^{-2}	1.073×10^{-2}	℧
r_x	580	53	Ω
r_π	6420	2609	Ω
c_π	1.666×10^{-11}	1.148×10^{-14}	F
r_μ	15.12×10^{6}	11.01	Ω
c_μ	4×10^{-12}	3.5×10^{-15}	F
r_0	2.522×10^{5}	10.93	Ω

1) Hybrid-π model parameters: To determine the values for each component we used calculations outlined by Malik [13] and Ramanan [14] with a combination of transistor h-parameters provided by manufacturer datasheets for the 2N3904 [9], and transistor t-parameters found in literature for the InGaP HBT [10]. Table I lists the parameters that were calculated for the Si and InGaP hybrid-π model. Worked out calculations for these parameters are given in Appendixes A and B



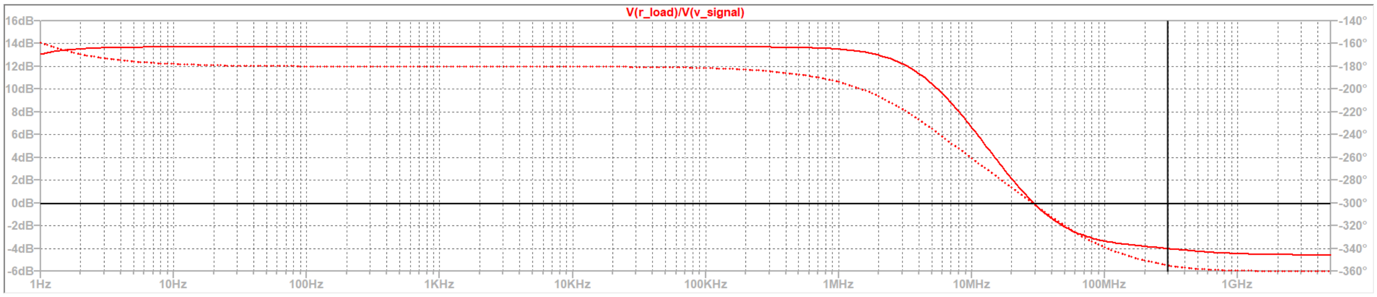
(a) Common Emitter



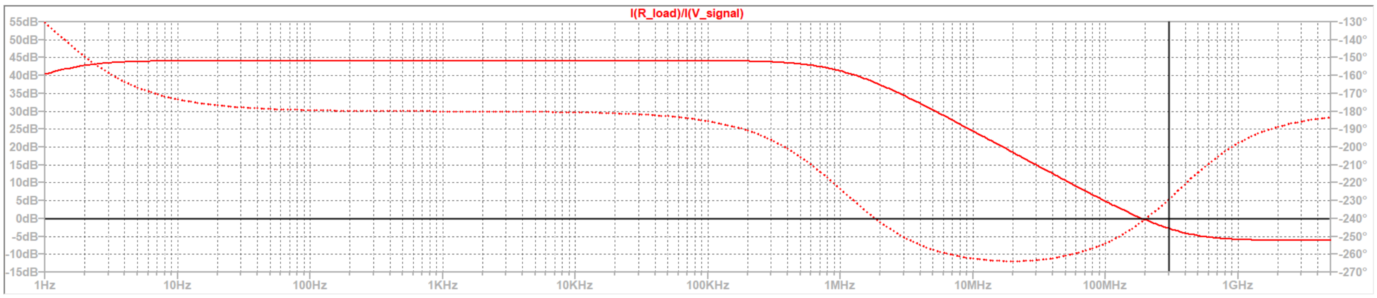
(b) Common Collector

Fig. 8: Simple NPN amplifier circuits in LTSpice

2) Simple Amplifier Circuits: Before we could use these parameters in the full test circuits, fig. 3 and 4, we ran the BJT/HBT models in simple amplifier circuits to ensure that they exhibit expected behavior. For this testing we are using common collector ans common emitter amplifier circuits, fig. 5b and 5a from above. We then transferred the schematics



(a) Common Emitter Amplifier Results for Silicon. The vertical axis represents the voltage gain



(b) Common Collector Amplifier Results for Silicon. The vertical axis represents the current gain

Fig. 9: Simple Amplifier Circuit Results for Silicon. The Vertical axis is the relative gain between the input signal and output load. The horizontal axis is the frequency. The bold black lines represent the 0 dB gain line in the vertical and the specified unity gain point in the horizontal.

into LTSpice, fig. 8a and 8b, and determined the values for the external resistors, capacitors, and voltage sources. The parameters for the external were calculated from Horowitz [4]. For $V_{cc} = 10V$ the external capacitor and resistor values were: $R_1 = 88k\Omega, R_2 = 110k\Omega, R_E = 5k\Omega, R_{Load} = 50\Omega, C_1 = 47\mu F, C_2 = 470\mu F$. For our first simulation run we set the V_{signal} AC input to have an amplitude $0.1V$, a sufficiently low amplitude to stay within a small signal model. We then ran an sinusoidal AC sweep between 1 Hz and 5 GHz (5×10^9 Hz) to verify that we were seeing positive current/voltage gains and that the unity gain frequencies, where the gain should be 0 dB, is close to the frequencies specified in the literature or datasheets.

IV. Results

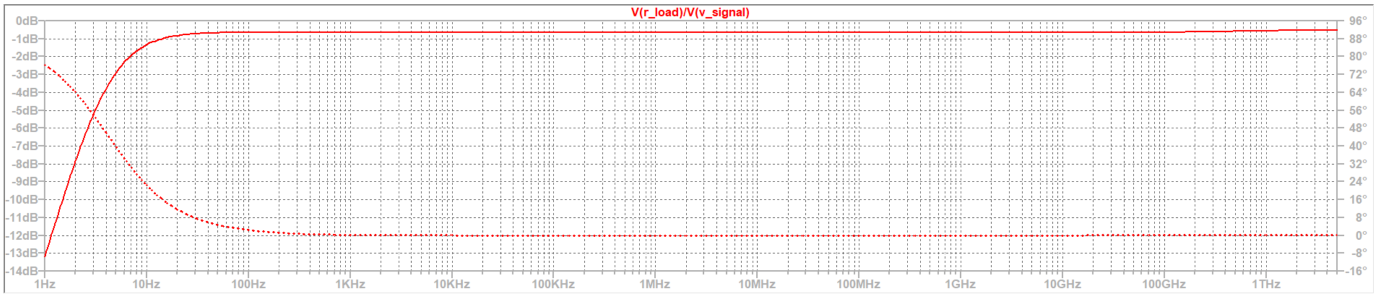
A. Common Emitter and Common Collector Amplifier Simulations

The silicon common emitter and common collector amplifier AC sweep results are shown in fig. 9a and 9b. The results looked very promising at first. The common collector simulation had good level of gain and slowly ramped down to the unity gain which was close to the specified value of 300 MHz. The common emitter simulation also showed decent levels of gain but missed the unity gain mark by an order of magnitude. The silicon simulation results came out promising so we proceeded to the InGaP simulation.

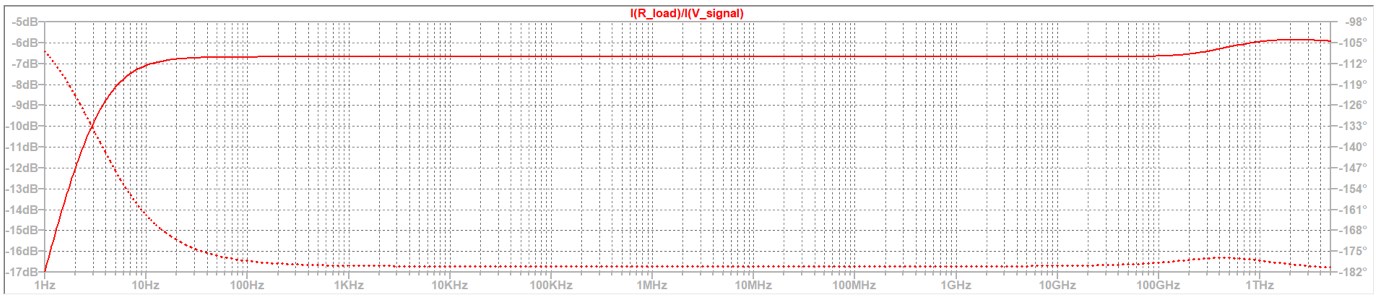
The InGaP common collector and common emitter simulation results are shown in fig. 10a and 10b. Unfortunately the results for this set of simulations was much less promising. We tried modifying the external component values, the input signal amplitude but we still ended up with negative gains, or attenuations, in our InGaP simulation. Since this model should be showing at least a positive gain we ran additional simulations to determine if our model was adequate for the simulations we are planning to run.

1) DC Analysis: For our additional test to verify our model we chose to run some basic DC analysis simulations, specifically an analysis to characterize the current-voltage curve of the transistor model. For our InGaP model we expect the curve to resemble that of fig. 11. fig. 11 shows the current at the collector, I_C, relative to the voltage between the collector and emitter, V_{CE}, of the junction transistor. The several curves represents increasing input currents at the base, I_B, of the transistor in 10 μA steps. This plot shows that at very low collector-emitter voltages there is very little current gain but as the voltage increases the gain between the current at the base and collector increases until a certain voltage, called the saturation voltage, where the collector current stays relatively constant with increasing collector-emitter voltage. This type of behavior is exhibited by all junction based transistors [3].

When we ran a DC analysis on the InGaP model to characterize it's current-voltage curve were given the result seen in fig. 12. We can see that the model does show a steady rise in the collector current, I_C plotted on the vertical axis, as the collector emitter voltage increases. Where this model fell short is that there is no transition, at a saturation voltage,



(a) Common Emitter Amplifier Results for InGaP. The vertical axis represents the voltage gain



(b) Common Collector Amplifier Results for InGaP. The vertical axis represents the current gain

Fig. 10: Simple Amplifier Circuit Results for Silicon. The Vertical axis is the relative gain between the input signal and output load. The horizontal axis is the frequency. As you can see both gains are in the negative region.

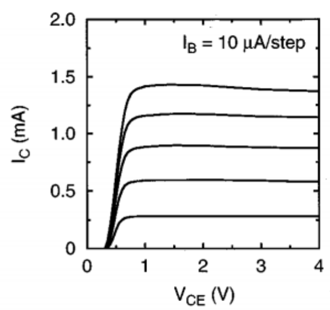


Fig. 11: The characteristic current-voltage curve of an InGaP HBT transistor. Notice how the collector current I_C plateaus after around 0.5 - 0.6 V_{CE}.
Source: [10]

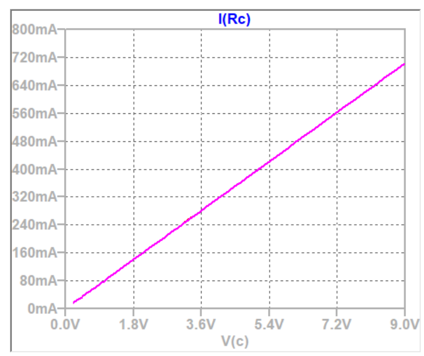


Fig. 12: DC simulation of the hybrid-π InGaP model does not follow the plateau that is to be expected with an junction transistor

from the steady increase in the collector current to a plateau in the collector current. From this result the hybrid-π model seems to be inadequate for the series of tests we had planned to carry out.

V. Conclusion

Even though we were not able to reach a consensus on the performance of Silicon and InGaP junction transistors we were able to discover shortcomings in the popular hybrid-π equivalent circuit transistor model and paved the groundwork for future research with models that more accurately predict the behavior of junction transistors.

A. Limitations

The biggest limitation that we had in this project was our choice of using the hybrid-π model for our simulations. This model works on the assumption that the junction transistor is purely a current amplifier device. In reality a junction transistor can be used as a current amplification device, but more importantly, it is a device constructed from a pair of junctions between positively and negatively doped semiconductor material [3]. This gives it properties such as the current-voltage curve and saturation voltage we saw from from fig. 11. With this limitation we were not able to simulate the circuits we originally planned. Another limitation that we had in this project is that we only chose to model a single type of silicon

BJT rather than sample a wide range to pick one that could possibly perform the best at ultra high frequencies. We were also limited in this project by the fact that we were not able to find a specific InGaP HBT part that had a nicely formatted datasheet and specifications we could calculate our parameters with. Instead we had to rely on research literature where the data was not as centralized. This meant that the data that we gathered may not be a very fair comparison with InGaP HBTs in general or match very closely with the InGaP HBTs inside the ERA-50SM+ device.

B. Future Work

Some possible paths that could be taken for future work include developing a better simulation model to more accurately model the behavior of a junction transistor, taking a wider sample of silicon BJTs to find more ultra high speed optimized types, and doing deeper research into InGaP HBTs to come up with a better set of parameters. Developing a better simulation model for junction transistors will increase the accuracy of our results to the real world behavior of junction transistors. Simulating a broader range of silicon transistors and digging deeper into InGaP transistor parameters will provide fairer comparison between the two materials.

Appendix A
Calculations for Silicon Hybrid-π Model

Table A1 shows the data we gathered for the 2N3904 Silicon BJT parameters from KEC Semiconductor [9].

TABLE A1: Data gathered from KEC 3904 datasheet Compiled from [9]

Parameter	Value
f_T Unity Gain Frequency	300×10^6 Hz
I_C Collector Current at h-parameter test condition	10V
h_{ie} Input Impedance	$7 \times 10^3 \Omega$
h_{re} Voltage Feedback Ratio	4.25×10^{-4}
$beta = h_{fe}$ Small-Signal Current Gain	250
h_{oe} Collector Output Admittance	$20.5 \times 10^{-6}\mho$
$C_{ob} = C_{\mu}$ Collector Output Capacitance	4×10^{-12} F

The following calculations use equations collected from [13].

To calculate the transconductance, g_m, we need the collector current at the h-parameter test condition, I_C, and the thermal voltage, V_T.

$$\begin{aligned} V_T &= \frac{kT}{q} \\ V_T &= \frac{1.38 \times 10^{-28} \times 298.15}{1.602 \times 10^{-19}} \\ V_T &= 0.02568V = 25.68mV \end{aligned} \tag{1}$$

where k is the Boltzmann Constant, T is the temperature in kelvin, and q is the charge of an electron

$$\begin{aligned} g_m &= \frac{I_C}{V_T} \\ g_m &= \frac{1 \times 10^{-3}}{0.02568} \\ g_m &= 0.03894 \end{aligned} \tag{2}$$

To calculate the input resistance, r_π, we need the transconductance, g_m, and the small-signal current gain, $\beta = h_{fe}$.

$$\begin{aligned} r_\pi &= \frac{\beta}{g_m} \\ r_\pi &= \frac{250}{0.03894} \\ r_\pi &= 6420 \end{aligned} \tag{3}$$

To calculate the feedback resistance, r_μ, we need the input resistance, r_π, and the voltage feedback ratio, h_{re}.

$$\begin{aligned} r_\mu &= \frac{r_\pi}{h_{re}} \\ r_\mu &= \frac{6420}{4.25 \times 10^{-4}} \\ r_\mu &= 15.12 \times 10^6 \end{aligned} \tag{4}$$

To calculate the output resistance, r_0, we need the collector output admittance, h_{oe}, small-signal current gain, $\beta = h_{fe}$, and the feedback resistance, r_μ.

$$\begin{aligned} r_0 &= \left(h_{oe} - \frac{\beta}{r_\mu}\right)^{-1} \\ r_0 &= \left(20.5 \times 10^{-6} - \frac{250}{15.12 \times 10^6}\right)^{-1} \\ r_0 &= 2.522 \times 10^5 \end{aligned} \tag{5}$$

To calculate the spreading resistance, r_x, we need the input impedance, h_{ie}, and the input resistance, r_π.

$$\begin{aligned} r_x &= h_{ie} - r_\pi \\ r_x &= 7 \times 10^3 - 6420 \\ r_x &= 580 \end{aligned} \tag{6}$$

To interelectrode capacitance, c_π, we need the transconductance, g_m, the unity gain frequency, f_T, and the Collector Output Capacitance, c_μ.

$$\begin{aligned} c_\pi &= \frac{g_m}{2\pi f_T} - c_\mu \\ c_\pi &= \frac{0.03894}{2\pi 300 \times 10^6} - 4 \times 10^{-12} \\ c_\pi &= 1.666 \times 10^{-11} \end{aligned} \tag{7}$$

TABLE A2: Data gathered from T. Oka et al. Compiled from [10]

Parameter	Value
f_T Unity Gain Frequency	114×10^9 Hz
h_{fe} Small-Signal Current Gain	28
r_e Emitter Resistance	90Ω
$r_b = r_x$ Base Resistance	53Ω
r_c Collector Resistance	11Ω
C_μ Collector Capacitance	3.5×10^{-15} F

APPENDIX B
CALCULATIONS FOR InGaP HYBRID-π MODEL

Table A2 shows the data we gathered for the InGaP parameters from T. Oka et al. [10].

Since the parameter we gathered are in t-parameter format we have to first convert them to h-parameters then to the values for a hybrid-π model

The following calculations use equations collected from Ramanan [14].

To find our t-parameter α value we need the small signal current gain, h_{fe}.

$$\begin{aligned} h_{fe} &= \frac{\alpha}{1-\alpha} \\ 28 &= \frac{\alpha}{1-\alpha} \\ 28(1-\alpha) &= \alpha \\ 28 &= 29\alpha \\ \alpha &= 0.9665 \end{aligned} \tag{8}$$

To find the input impedance, h_{ie}, we need the α value, the emitter resistance, r_e, and the base resistance r_b.

$$\begin{aligned} h_{ie} &= \frac{r_e}{1-\alpha} + r_b \\ h_{ie} &= \frac{90}{1-0.9655} + 53 \\ h_{ie} &= 2662 \end{aligned} \tag{9}$$

To find the voltage feedback ratio, h_{re}, we need the α value, the emitter resistance, r_e, and the collector resistance, r_c.

$$\begin{aligned} h_{re} &= \frac{r_e}{(1-\alpha)\, r_c} \\ h_{re} &= \frac{90}{(1-0.9655)\, 11} \\ h_{re} &= 237 \end{aligned} \tag{10}$$

To find the collector output admittance, h_{oe}, we need the α value and the collector resistance r_c

$$\begin{aligned} h_{oe} &= \frac{1}{(1-\alpha)\, r_c} \\ h_{oe} &= \frac{1}{(1-0.9655)\, 11} h_{oe} \quad = 2.635 \end{aligned} \tag{11}$$

To find the transconductance, g_m, we need the small-signal current gain, h_{fe}, the input impedance, h_{ie}, and the base resistance, $r_b = r_x$.

$$\begin{aligned} g_m &= \frac{h_{fe}}{h_{ie} - rx} \\ g_m &= \frac{28}{2662 - 53} \\ g_m &= 0.01073 \end{aligned} \tag{12}$$

To calculate the input resistance, r_π, we need the input impedance, h_{ie}, and the base resistance, $r_b = r_x$.

$$\begin{aligned} r_\pi &= h_{ie} - r_x \\ r_\pi &= 2662 - 53 \\ r_\pi &= 2609 \end{aligned} \tag{13}$$

To calculate the feedback resistance, r_μ, we need the input impedance, h_{ie}, the base resistance, $r_b = r_x$, and the voltage feedback ratio, h_{re}.

$$\begin{aligned} r_\mu &= \frac{h_{ie} - r_x}{h_{re}} \\ r_\mu &= \frac{2662 - 53}{237} \\ r_\mu &= 11.01 \end{aligned} \tag{14}$$

To calculate the output resistance, r_0, we need the collector output admittance, h_{oe}, small-signal current gain, h_{fe}, the input impedance, h_{ie}, the voltage feedback ratio, h_{re}, and the base resistance, $r_b = r_x$.

$$\begin{aligned} r_0 &= \left(h_{oe} - \frac{h_{fe} h_{re}}{h_{ie} - r_x}\right)^{-1} \\ r_0 &= \left(2.635 - \frac{(28)(237)}{2662 - 53}\right)^{-1} \\ r_0 &= 10.93 \end{aligned} \tag{15}$$

ACKNOWLEDGMENT

The author would like to thank Dr. S. Ramachandran for all the guidance and support for this project. The author would also like to thank Dr. M. Gliboff and the UW Bothell physics class of 2021 for their support as well.

REFERENCES

[1] J. Early, "Out to murray hill to play: an early history of transistors," *IEEE Transactions on Electron Devices*, vol. 48, no. 11, pp. 2468–2472, 2001. [Online]. Available: https://doi.org/10.1109/16.960369

[2] T. Jenkins, "A brief history of ... semiconductors," *Physics Education*, vol. 40, no. 5, pp. 430–439, Sep. 2005. [Online]. Available: https://doi.org/10.1088/0031-9120/40/5/002

[3] S. M. Sze and K. K. Ng, *Physics of semiconductor devices*, 3rd ed. Hoboken, N.J: Wiley-Interscience, 2007.

[4] P. Horowitz, *The art of electronics*, 3rd ed. New York, NY: Cambridge University Press, 2015.

[5] F. Schwierz and J. J. Liou, "RF transistors: Recent developments and roadmap toward terahertz applications," *Solid-State Electronics*, vol. 51, no. 8, pp. 1079–1091, Aug. 2007. [Online]. Available: https://doi.org/10.1016/j.sse.2007.05.020

[6] R. W. Keyes, "Physical limits of silicon transistors and circuits," *Reports on Progress in Physics*, vol. 68, no. 12, pp. 2701–2746, Sep. 2005. [Online]. Available: https://doi.org/10.1088/0034-4885/68/12/r01

[7] K. Aoki and T. Mitsui, "A tabletop experiment for the direct measurement of the speed of light," *American Journal of Physics*, vol. 76, no. 9, pp. 812–815, Sep. 2008. [Online]. Available: https://doi.org/10.1119/1.2919743

[8] Mini-Circuits, *ERA-50SM+ Surface Mount Monolithic Amplifier*, 191031, 2020., rev. P.

[9] KEC Semiconductor, *2N3904 Epitaxial Planar NPN Transistor*, 2002., rev. 1.

[10] T. Oka, K. Hirata, H. Suzuki, K. Ouchi, H. Uchiyama, T. Taniguchi, K. Mochizuki, and T. Nakamura, "High-speed small-scale InGaP/GaAs HBT technology and its application to integrated circuits," *IEEE Transactions on Electron Devices*, vol. 48, no. 11, pp. 2625–2630, 2001. [Online]. Available: https://doi.org/10.1109/16.960388

[11] T. Low, T. Shirley, C. Hutchinson, G. Essilfie, W. Whiteley, B. Yeats, and D. D'Avanzo, "InGaP HBT technology for RF and microwave instrumentation," *Solid-State Electronics*, vol. 43, no. 8, pp. 1437–1444, Aug. 1999. [Online]. Available: https://doi.org/10.1016/s0038-1101(99)00086-6

[12] B. K. Sharma and P. Purkait, "The hybrid-pi model: Some discrepencies and the suggested universal model," *IETE Journal of Research*, vol. 35, no. 1, pp. 1–7, Jan. 1989. [Online]. Available: https://doi.org/10.1080/03772063.1989.11436780

[13] N. Malik, "Determining SPICE parameter values for BJTs," *IEEE Transactions on Education*, vol. 33, no. 4, pp. 366–368, 1990. [Online]. Available: https://doi.org/10.1109/13.61094

[14] K. V. Ramanan, *Functional Electronics*. New Delhi: Tata McGraw-Hill, 1985.