Questions on I2C:

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| --- | --- | --- | --- | --- | --- | --- | --- |
| Sl.No | Topic | Subtopic | Questions | | 1 | 2 | 3 |
| 1 | Multi master | Arbitration | |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | |  | Data on | T1 | T2 | T3 | T4 | T5 | T6 | T7 | T8 | … | … | … | | Master 1 | SDA | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | … | … | … | | Master2 | SDA | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | … | … | … | | Master 3 | SDA | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | … | … | … | | Master4 | SDA | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | … | … | … |   In the above scenario, if the all the master starts to transfer the client address, at the same point in time, who will win the bus arbitration \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_  and who will lose the bus arbitration 1st : \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_  and who will lose the next. \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ | |  |  | x |
| 2 |  | Clock Sync | |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | |  | Data on | T1 | T2 | T3 | T4 | T5 | T6 | T7 | T8 | … | … | … | | Master 1 | SCL | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | … | … | … | | Master2 | SCL | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | … | … | … | | Master 3 | SCL | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | … | … | … | | Master 4 | SCL | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | … | … | … | | Final Clock line status |  |  |  |  |  |  |  |  |  |  |  |  |   In the above scenario, each Master has different clock :   1. Is it possible to have multiple master working with different clock speed (Yes/No) 2. If “No” : Skip the below question. 3. If “Yes” : Fill the final clock line in the above table. | |  |  | X |
| 3. | Single master | SDA synchronization | If master is sending data at a high rate than the speed at which the client can process the data.  Then how the slaves inform the master to slow down. ………………………………………….. | | x |  |  |
| 4 |  | SDA synchronization | In the below example, if the slave needs 2 clock time after it receives every 4 bits of data, how does the clock and data line look like.  Without stretching:   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | |  | Data on | T1 | T2 | T3 | T4 | T5 | T6 | T7 | T8 | T9 | T10 | T11 | T12 | T13 | T14 | T15 | T16 | | Master 1 | SDA | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |  |  |  |  | | Master1 | SCL | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |  |  |  |  |   With stretching:   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | x | Data on | T1 | T2 | T3 | T4 | T5 | T6 | T7 | T8 | T9 | T10 | T11 | T12 | T13 | T14 | T15 | T16 | | Master 1 | SDA | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |  |  |  |  | | Master1 | SCL | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |  |  |  |  | | |  |  | x |
| 5 |  | Clock Stretching | How long the slave can hold the line low? | | x |  |  |
| 6 | General |  | Is I2C half-duplex or full duplex | | x |  |  |
|  |  |  | Is I2C synchronous or Asynchronous | | x |  |  |
|  |  |  | A bus line oscillates 10 times per second. For each oscillation one bit can be transmitted.  For this bus line:   1. What is the bit rate of the bus? ………………. 2. What is the data rate of the bus?......................... 3. What is the baud rate?.......................... | |  | x |  |
| 7 | I2C Facts |  | Pick the mode against each data rate of the I2C bus   * 100 kbit/s : * 1 Mbit/s: * Mbit/s: * 1.4 Mbit/s: | 1. Fast Mode 2. Fast mode plus 3. High Speed mode 4. No Such mode | x |  |  |
| 8 | General |  | Find the error in the bus w.r.t the data transfer:   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | |  | Data on | T1 | T2 | T3 | T4 | T5 | T6 | T7 | T8 | T9 | T10 | T11 | T12 | T13 | T14 | T15 | T16 | | Master 1 | SDA | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | | Master1 | SCL | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | | |  |  | x |
| 9 | General |  | Fine the error in the bus w.r.t to data transfer:   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | |  | Data on | T1 | T2 | T3 | T4 | T5 | T6 | T7 | T8 | T9 | T10 | T11 | T12 | T13 | T14 | T15 | T16 | | Master 1 | SDA | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | | Master1 | SCL | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | | |  |  | x |
| 10 | Error |  | In case of normal data transfer, if NAC is sent after the data, then the master will…   1. The master will send a stop bit. 2. Try to resent the data in the subsequent bit of data transfer 3. The master will send a stop bit followed with address | |  | x |  |
| 11 | Repeated Start |  | In case of repeated start, if NAC is sent after the data, then the master will…   1. The master will send a stop bit. 2. Try to resent the data in the subsequent bit of data transfer 3. The master will send a stop bit followed with address | |  | x |  |
| 12 |  |  | In case of repeated start, if ACK is sent after the data and further data is available for sending. The bit following the ACK will be:   1. Start bit followed with data 2. Start bit followed with Address 3. Stop bit followed with start bit and address 4. Stop bit followed with start bit and data | |  | x |  |
| 13 |  |  | Ultra-fast mode data rate is ……… | | x |  |  |
| 14 |  |  | 1. Can I2C slave start the data communication with Master (Yes/No)…….. 2. If “Yes” skip the below question 3. If “No” what is the best possible way by with a key board slave connected on I2C line can communicate the key press event to Master?    1. Master can do a continuous polling.    2. Slave change its mode from Slave to Master and starts to communicate    3. Slave can raise an interrupt to Master | |  | x |  |
| 15 |  |  | I2C can work in   1. I2C is Multiple master and multiple slave 2. Multiple slave and Single Master 3. Multiple Master and single Slave 4. One master and One Slave | |  | x |  |
| 16 |  |  | In Idle mode :   1. SCL and SDA, remain high 2. SCL and SDA, remains low 3. SCL remains low and SDA remains high 4. SCL oscillate and SDA remains low | |  | x |  |
| 17 |  |  | Given the below condition at what time period will the 1st, 2nd , 3rd and 4th data be transmitted and what data bit will be transmitted:  1st bit : Time period ……….data transmitted ……….  2nd bit : Time period ……….data transmitted ……….  3rd bit : Time period ……….data transmitted ……….  4th bit : Time period ……….data transmitted ……….   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | |  | Data on | d1 | d2 | d3 | d4 | d5 | d6 | d7 | T8 | d9 | d  10 | d  11 | d  12 | d  13 | d  14 | d  15 | d  16 | | Master 1 | SDA | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | … | … | … |  |  |  |  |  | | Master2 | SDA | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | … | … | … |  |  |  |  |  | | Master 3 | SDA | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | … | … | … |  |  |  |  |  | | Master4 | SDA | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | … | … | … |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | |  | Data on | T1 | T2 | T3 | T4 | T5 | T6 | T7 | T8 | T9 | T  10 | T  11 | T  12 | T  13 | T  14 | T  15 | T  16 | | Master 1 | SCL | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | | Master2 | SCL | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | | Master 3 | SCL | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | | Master4 | SCL | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   Note : d1->1st data, d2->2nd data …. | |  |  | X |
| 18 |  |  | How many slave can be addressed in 7 bit addressing mode of I2C…………………… | | x |  |  |
| 19 |  |  | To extend address more 10 bit addressing is used, can the I2C slaves connected in single bus has mix of both 10bit and 7 bit addressing ( Yes, No)……………..   1. If “No”, Skip the below question 2. If “Yes” how the 7bit and 10bit slave is addressed 3. After the start condition, a leading '00001' introduces 4. Before the Start condition, a leading '00001' introduces 5. After the start condition, a leading '11110' introduces 6. Before the start condition, a leading '11110' introduces | |  |  |  |
| 20 |  |  | In some applications different I2C reference voltages are used for different ICs, Sometimes it is necessary to have all of them sharing the same bus. To be able to recognize what a logical zero and logical one is, a…………………………….. is necessary. | |  |  |  |