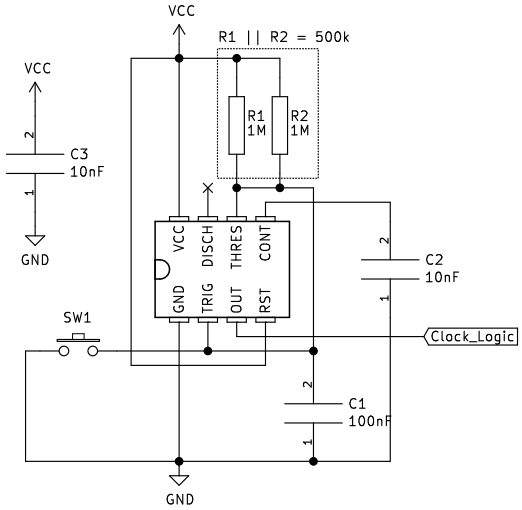

Theory of Operation:

When SW1 is open, C1 will charge through R1 and R2 which act in parallel to provide an equivalent resistance of 500kΩ.
The resistance of R1||R2, paired with the 100nF capacitance of C1, charges C1 to 66% of Vcc in about 50ms, at which point the threshold comparater will trigger and the 555 output will be held in a low state (The values I chose for this RC circuit are based on the compnent values which come with the 8-Bit Breadboard Computer kit, as well as what timing felt best in my own testing while maintaining good debounce properties. They are ultimately arbitrary, and I'd encourage you to experiment with values on your own).

When SW1 is depressed, a direct path is created between C1 and GND causing C1 to discharge practically instantaneously, dropping the voltage on the TRIG pin below 33% of Vcc and latching the 555 output to a high state while SW1 remains held.
If the button contact is intermittent, the 555 output will not return to low unless the THRES voltage is allowed to return to 66% of Vcc which should only happen when SW1 is intentionally released and 40ms are allowed to pass with SW1 open.

The DISCH pin is not utilized in this circuit and should not be connected to anything.

The CONT pin's purpose is to adjust the voltages at which the THRES and TRIG pins latch the 555's internal SR latch.
Becuase we do not want to use this feature, we place C2 between CONT and GROUND to resist voltage variations on this pin from outside interferences.

The RESET pin is tied to Vcc in order to avoid being accidentally triggered.

C3 provides power smoothing to the Vcc and GND rails which results in much cleaner state transitions on the 555 output.

Sheet: /		
File: 555 debounce.sch		
Title: Monostable 555 Switch Debouncer		
Size: A4	Date: 2021-05-29	**Rev: 1**
KiCad E.D.A. kicad (5.1.10-0-10_14)		Id: 1/1