VIT
Vellore Institute of Technology

School of Computer Science and Engineering

Fall Semester 2024-25

Continuous Assessment Test - I, August 2024

SLOT:E1+TE1

Programme Name & Branch: M.Tech (MIC,MID)

Course Name & Code: Advanced Computer Architecture, CSI3021

Class Number (s): VL2024250101933, 1951, 3605, 1957

Faculty Name (s): THIRUNAVUKKARASAN M , SREETHAR S, NARMALLI JAYAKRISHNA, SURESH A

Exam Duration: 90 Min. **Maximum Marks: 50**

Answer ALL questions (5 x 10 = 50 Marks)

Q. No.	Question	Max Marks
1.	a) Distinguish between typical RISC and CISC processor architectures (5 Marks) b) Consider a processor with a clock rate of 800 Mhz running a given set of instructions Calculate the Effective CPI, MIPS rate and Execution time. (5 Marks)	10
2.	Draw and label a typical single cycle Datapath block diagram. Explain its components and the sequence of operations using an example instruction	10
3.	Explain how Tomasulo's algorithm can be enhanced to enable hardware-based speculation. Highlight the key techniques and modifications required for this extension.	10
4.	a) Compare and contrast static scheduling and dynamic scheduling. (5 Marks) b) Explain the significance of register renaming in processor architecture (5 Marks)	10
5.	Evaluate the primary components of the VMIPS instruction set architecture and explain the fundamental aspects of vector architecture. Include a neat block diagram to illustrate the basic vector architecture.	10

Instruction Count (Millions)	Cycle per Instruction
8	1
4	3
2	4
4	3