

# **Linear Integrated Circuits**

## **Second Edition**

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## **Second Edition**

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# **Foreword**

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It gives me immense pleasure in introducing the second edition of the book Linear Integrated Circuits, authored by Prof. S. Salivahanan, Principal, SSN College of Engineering, Chennai, and Prof. V S Kanchana Bhaaskaran, Professor & Dean of the School of Electronics Engineering, VIT University, Chennai. I have known the authors, Prof. Salivahanan and Prof. Kanchana, as dedicated academics who have been serving the cause of teaching and research.

The subject of Linear Integrated Circuits finds applications in all branches of engineering. Since the physical world is essentially linear or analog in nature, it is imperative that the students and faculty of many specialty fields have an exhaustive knowledge in the area of linear integrated circuit design. The authors with their rich teaching experience and knowledge have uncovered various topics in simple and lucid language interspersed with illustrative examples and exercises. Furthermore, the mode of presentation is set to enhance the interest of the readers towards self-study and designing realistic circuits.

I am confident that this book shall fill the void felt by the academia for a good textbook on the subject of Linear Integrated Circuits. Making the copies of this book available in the libraries of all universities, colleges and polytechnics will certainly help in enriching them. I strongly recommend this book to every Electronics, Electrical, Instrumentation, Computer Science, Information and Communication Engineering student, and wish the authors a grand success.

**G Viswanathan**  
*Chancellor*  
*VIT University*



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# Preface

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The monolithic operational amplifier has become an important building block of linear integrated circuits and applications. The objective of this book is to offer the reader proficiency in the analysis and design of circuits including analog signal processing using linear ICs.

## Target Audience

The book hopes to serve the purpose of a text to the engineering students of degree, AMIE, graduate IETE and diploma courses and a useful reference to those preparing for competitive examinations such as GATE, UPSC, etc. In addition, it will meet the pressing need of those enthusiastic readers who wish to acquire a sound knowledge and understanding of the principles of linear integrated circuits. Further, the book will assist the practical analog IC designer with the selection of appropriate devices and circuit configurations. The text is presented in a simple and lucid manner with the theoretical, analytical and application aspects of ICs.

## Salient Features

- Detailed description of the components of integrated circuits from the applications perspective
- Focus on internal circuitry to develop practical know-how
- Coverage of Fiber Optic ICs and Optocouplers unique to the book
- Exposure to ORCAD PSpice with specific design problems
- **New to this edition**—Negative Feedback op-amps, Diode, Zener diode and LED Tester Circuits, Generalised Impedance converter, Biquad Filter and KRC Filter.
- Refreshed pedagogy:
  - Diagrams: 550
  - Solved Examples: 106
  - Review Questions: 729
  - PSpice Examples: 14

## Chapter Organization

The book comprises 14 chapters. **Chapter 1** discusses the various processes involved in monolithic integrated circuit fabrication, beginning with wafer preparation and culminating in encapsulation of the IC. The text also unfolds the devising of bipolar and MOS transistors, various diodes, passive components such as resistors and capacitors, transformation of an electronic circuit into equivalent monolithic form, and thin- and thick-film technologies.

In **Chapter 2**, the basic circuit configurations for linear ICs, such as current sources, voltage sources and references, various differential amplifier configurations using BJT, JFET and MOSFET are discussed.

**Chapter 3** dwells upon the characteristics of operational amplifiers. The popularly used op-amp 741 is introduced. The dc and ac performance characteristics, frequency-compensation methods, noise

characteristics, open-loop and closed-loop configurations, characteristics of differential amplifiers and typical manufacturers' specifications are provided.

**Chapter 4** unfolds the linear applications of op-amps, namely, scale changer, voltage follower, instrumentation amplifier, ac amplifiers, integrator and differentiator, log and antilog amplifiers concluding with the use of linear ICs for analog computation with typical examples.

In **Chapter 5**, non-linear circuit applications using op-amps originating with comparators, developing into Schmitt trigger and various other applications employing comparators such as, the rectifiers, peak detectors, sample-and-hold circuits, clippers, clampers, and diode, Zener diode and LED testers have been elaborated. The analog switches used for sample-and-hold circuits are also discussed in this chapter.

**Chapter 6** uncovers the active filter design using linear ICs. First-order and second-order low-pass and high-pass filter designs, filter approximations, band-pass and band-reject filters, all-pass and state variable filters, impedance converters, impedance gyration, switched capacitor integrators, the theory and design of various filter responses are uncovered.

**Chapter 7** discusses the sinusoidal, square, triangular and sawtooth waveform generation circuits using op-amps, and the widely used function generator ICs such as 8038 and the timer IC 555 with elaborate discussion on their various modes of operation. Typical application circuits using IC 555 are presented.

In **Chapter 8**, the fundamental principles of linear voltage regulation, three-terminal fixed voltage regulators, variable voltage regulators and their designs for high-current capability followed by the over-current protection circuitries, theory of switched mode regulation and switched mode power supplies are covered in detail.

**Chapter 9** presents the various methods of obtaining analog multiplication, theory of Gilbert Cell and variable transconductance-based four-quadrant multipliers, multiplier ICs and their practical applications.

**Chapter 10** demonstrates the theory of phase-locked loop (PLL) encompassing the phase detector circuit, voltage-controlled oscillator circuit, voltage-controlled oscillator IC, closed-loop analysis of PLL, the typical monolithic PLL IC 565 and its various application circuits.

In **Chapter 11**, the sampling theorem, the fundamentals of A/D and D/A conversion techniques, the circuit arrangements of various conversion methodologies, sigma delta conversion techniques and the widely used ICs for A/D and D/A conversion are dealt with in detail. **Chapter 12** presents the special function ICs meant for voltage and frequency conversions, tuned amplification, power amplification, video amplification, fibre optic circuits, opto-couplers, isolation amplifiers and compander integrated circuits. Insights into the ICs available for voltage and frequency conversions, function generator IC are also provided.

**Chapter 13** deals with advanced operational amplifier structures using CMOS, BiFET, BiMOS and JFET and their analyses. Programmable transconductance amplifiers and their applications have also been discussed.

**Chapter 14** provides a practice with simulation examples using PSpice for the linear integrated circuits discussed in the text. The readers can familiarize themselves with the nuances of programming using PSpice using the example simulations included in the chapter.

All the topics have been illustrated with lucid diagrams for easy understanding. Equal emphasis has been laid on mathematical derivations and their physical interpretations and inferences. Illustrative examples are discussed to emphasize the concepts and typical applications. Summary, review questions and exercises have been included at the end of each chapter with a view to help the readers augment their understanding of the subject and to encourage further reading.

## Acknowledgements

We sincerely thank the managements of SSN College of Engineering, Chennai, and VIT University, Chennai, for the constant encouragement, and for providing the necessary facilities for the completion of this project.

We express our deep gratitude to Dr G Viswanathan, Chancellor, VIT University, for writing the foreword to this book. We thank our colleagues for their useful comments, which have improved the book considerably. We are thankful to Mr R Gopalakrishnan for word processing the manuscript. Our special thanks to Ms Saambhavi Baskaran who spent her precious time on proofreading the second edition contents.

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Professor S Salivahanan is immensely thankful to his wife, Mrs Kalavathy, and sons, Santhosh Kanna and Subadesh Kanna, for their spirit of self-denial and enormous patience during the preparation of the revised edition. Professor Kanchana Bhaaskaran expresses her heartfelt thanks to her husband, Mr Baskaran, and daughters, Madhangi and Saambhavi, for their spirit of self-denial and enormous patience during the preparation of the second edition of this book.

Readers are welcome to give constructive suggestions for the improvement of the book.

**S Salivahanan**  
**V S Kanchana Bhaaskaran**

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# Integrated Circuit Fabrication

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1

## 1.1 INTRODUCTION

Integrated circuit (IC) is the outcome of continued improvements in the characteristics and miniaturisation of solid-state devices and components. When solid-state devices such as transistors and diodes were invented, they replaced vacuum tubes. Similarly, a new generation of solid-state electronics, i.e. integrated circuits, is replacing the discrete components like resistors, capacitors, diodes, transistors, FETs etc. In a discrete circuit, the components are separable, whereas the components of integrated circuit are inseparable. Most of the ICs are silicon chips with devices such as transistors, resistors and capacitors fabricated in them. A single silicon chip can contain a few devices or many thousands of devices. Large and complex circuits can be reduced to a small size by IC technology.

The following are the advantages of ICs over discrete components.

- (i) Small size (around  $10^{12}$  transistors per die)
- (ii) Improved performance (more complex circuits may be used)
- (iii) Low cost
- (iv) High reliability and ruggedness
- (v) Low power consumption
- (vi) Less vulnerability to parameter variations
- (vii) Easy troubleshooting by replacement
- (viii) Simpler design of systems
- (ix) Standard packaging
- (x) Increased operating speed (due to the absence of parasitic capacitance effect)
- (xi) Less weight and portable
- (xii) Battery operated systems due to low power supply requirement

The limitations of integrated circuits are as follows:

1. As IC is small in size, it is unable to dissipate large amount of power. Increase in current may produce enough heat which may destroy the device.
2. At present, coils, inductors and transformers cannot be produced in IC form.

**Classification of ICs** IC technology has been advancing rapidly, increasing the complexity and functionality of the circuits fabricated. This necessitates the need for categorising ICs based on their complexity levels as shown in Table 1.1.

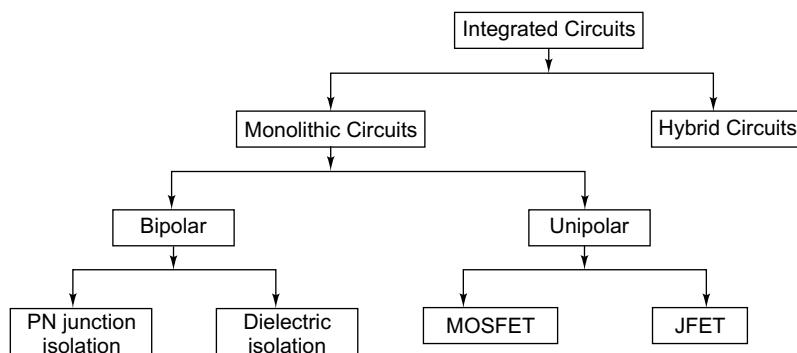
**Table 1.1 Classification of ICs**

Type of IC	No. of Gates	No. of Transistors
Small Scale Integration (SSI)	3–30 per chip approx.	100
Medium Scale Integration (MSI)	30–300 per chip approx.	100–1,000
Large Scale Integration (LSI)	300–3,000 per chip approx.	1,000–20,000
Very Large Scale Integration (VLSI)	More than 3,000 per chip	20,000–10,00,000
Ultra Large Scale Integration (ULSI)	—	$10^6$ – $10^7$
Giant Scale Integration (GSI)	—	More than $10^7$

The area for SSI chip is 1 sq.mm (1600 sq.mil) and for LSI chip it is 1 sq.cm (1,60,000 sq.mil).

The ICs can be classified as shown in Fig. 1.1. On the basis of fabrication process used, ICs can be classified as *monolithic* circuits and *hybrid* circuits. The word *monolithic* means *single stone*, and as the name implies, the entire circuit is fabricated on a single chip of semiconductor. In monolithic integrated circuits, the components like transistors, diodes, resistors and capacitors are formed simultaneously by diffusion process steps. Then the process of metallisation is used in interconnecting these components to form the required circuit. The dielectric or *PN* junction is used to provide electrical isolation in monolithic ICs. The monolithic circuit technology is ideal for applications requiring identical characteristics of components in very large quantities. Therefore, they cost less and provide a higher order of reliability.

A hybrid circuit contains individual component parts attached to a ceramic substrate. The components are interconnected by the use of either metallisation patterns or bonding wires. The hybrid circuits improve the circuit performance, since passive component values can be trimmed to precision at higher values. This technology is more suitable to custom-designed circuits of small volume fabrications. Hybrid ICs are categorised as *thin film* and *thick film*, based on the method used to form the resistors, capacitors, and related interconnections on the substrate.

**Fig. 1.1 Classification of ICs**

Based on the active devices used, ICs can be classified as bipolar (using BJT) and unipolar (FET). Depending on the isolation technique employed to separate the individual components in the ICs, the bipolar ICs may further be classified as (i) *PN* junction isolation and (ii) dielectric isolation. On the basis of the type of field effect generation in the FET devices, the unipolar ICs may further be classified as JFET and MOSFET.

The ICs can more relevantly be classified as (i) linear or analog ICs, (ii) digital ICs and (iii) mixed signal ICs based on the type and combinations of signals they process. The classification is made based on the treatment of the *signal*. An analog signal is the one that is defined over a continuous range of time, while, the digital signal is the one that is defined only at discrete points of time, by discrete values of amplitude. The linear ICs such as op-amps, voltage regulators, voltage comparators and timers are related to all the design phases of electronics in which signals are represented by continuous or analog quantities. The digital ICs such as logic gates, flip-flops, counters, digital clock chips, calculator chips, memory chips and microprocessors deal with discrete quantities. In a digital IC, the information is represented by binary digits and involves logic and memory. The mixed signal ICs involve both the analog and digital signal processing.

## 1.2 MANUFACTURING PROCESSES OF MONOLITHIC ICs

The basic processes used to fabricate monolithic circuits using silicon planar technology can be categorised as follows:

- (i) Silicon wafer preparation
- (ii) Epitaxial growth
- (iii) Oxidation
- (iv) Photolithography
- (v) Diffusion
- (vi) Metallisation
- (vii) Circuit probing
- (viii) Scribing and separating into chips
- (ix) Mounting and packaging
- (x) Encapsulation

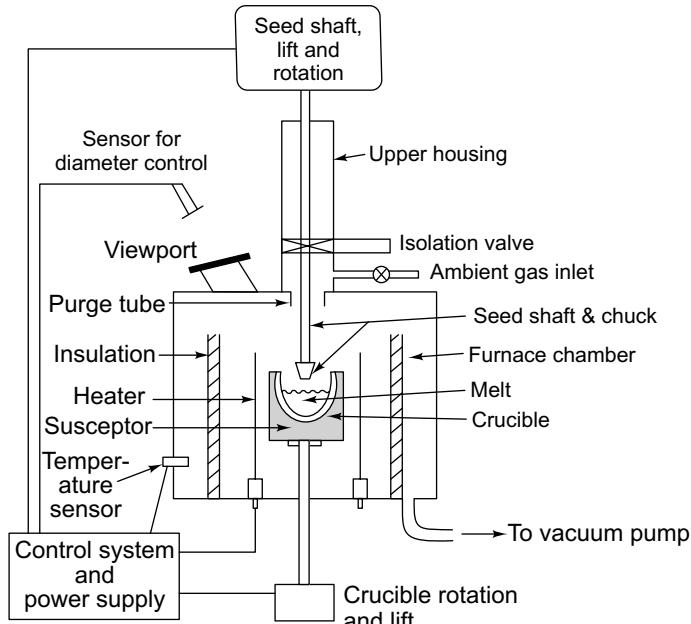
### 1.2.1 Silicon Wafer Preparation

The starting material for integrated circuits is a slice of single crystal silicon, which is normally the Metallurgical Grade Silicon (MGS). By the use of Chemical Vapour Deposition techniques (CVD) and hydrogen reduction method, the Electronic Grade Silicon (EGS) is obtained. The EGS is a polycrystalline material of high purity and it is used as the raw material for the preparation of single crystal silicon.

The processes of obtaining EGS from MGS are (i) reaction with  $HCl$  as given by  $Si + 3HCl \rightarrow SiHCl_3 + H_2$  thus forming trichlorosilane and (ii) hydrogen reduction of trichlorosilane as represented by  $2SiHCl_3 + 2H_2 \rightarrow 2Si + 6HCl$ . The EGS has very small impurity level and is a polycrystalline material. This is converted to purer and defect free single crystal by Czochralski technique or Bridgeman technique. The former method is used for growing single crystals and the latter method is used for growing gallium arsenide crystals.

**Crystal growth** The Czochralski technique for growing crystals was developed by Czochralski. The crystal growth apparatus consisting of the *Czochralski puller* used in this technique is shown in Fig. 1.2. The Czochralski puller consists of a quartz crucible. The polycrystalline EGS along with an appropriate amount of dopant impurities is placed in the quartz crucible. The material is then heated to a temperature that is slightly in excess of the silicon melting point of  $1420^{\circ}C$ . A small single-crystal rod of silicon called a *seed crystal* is then dipped into the silicon melt. The conduction of heat, up the *seed crystal* will produce a reduction in the temperature of the melt in the area of contact with the seed crystal to slightly below the silicon melting point. This will make the silicon to freeze onto the end of

the seed crystal, and as the seed crystal is slowly pulled up and out of the melt, it will pull with it a solidified mass of silicon that will be a crystallographic continuation of the seed crystal. Both the seed crystal and the crucible are rotated in opposite directions during the crystal pulling process in order to produce the crystalline silicon ingots of circular cross section. The ingots are then cut into slices, about a millimetre thick and the surface is polished to give a smooth, highly flat region.

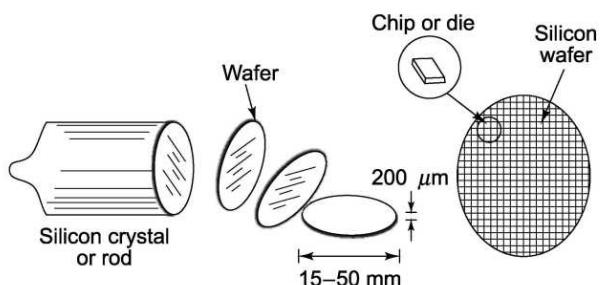


**Fig. 1.2** Czochralski silicon crystal growing apparatus

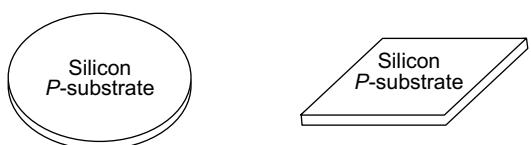
*P*-type (or *N*-type) impurities are added with the melt to give the required semiconducting characteristics to the final silicon *ingots* (bars) obtained from the crystal growth process. The doping elements are normally identified in parts per billion. The *P*-type silicon bar is cut into thin slices called wafers as shown in Fig. 1.3. These wafers are polished to mirror finish and they serve as the base or substrate for hundreds of ICs. The enlarged views of circular and rectangular *P*-type silicon wafers are shown in Fig. 1.4.

## 1.2.2 Epitaxial Growth

*Epitaxy* means growing a single crystal silicon structure upon an original silicon substrate, such that the new structure is essentially a molecular extension of the original substrate.



**Fig. 1.3** Silicon wafer preparation



**Fig. 1.4** Enlarged views of circular and rectangular *P*-type silicon substrates

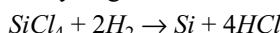
Thus the structure of the grown epitaxial layer will be a continuation of the single crystal substrate. There is a distinct difference between epitaxy and crystal growing technique. In epitaxy, a thin film of single crystal silicon is grown from a vapour phase upon an existing single crystal of the same material, whereas in crystal growing technique, a single crystal is grown from the liquid phase. Epitaxy layers can be closely controlled for their size and resistivity.

Growth of epitaxial layer makes it possible to control the doping profile in a device structure. The epitaxy layer is generally free from oxygen and carbon. Most of the integrated circuit structure is formed in the epitaxy layer, the rest of the slice acting purely as a supporting plane.

Epitaxy apparatus is very similar to the oxide growth arrangement. RF heating coils are normally used and silicon wafers are stacked in a graphite boat, which may be coated with quartz to prevent the graphite from contaminating the silicon. The apparatus used for the epitaxial growth is shown in Fig. 1.5.

Initially, the slices are heated to about  $1200^{\circ}\text{C}$ , and mixture of pure hydrogen and hydrochloric acid vapour is passed over them to etch away any oxide or impurities which may exist on the surface of the silicon.  $\text{HCl}$  vapour is then cut-off and hydrogen gas bubbled through  $\text{SiCl}_4$  kept in a bubbler is allowed. When this reaches the hot silicon,  $\text{SiCl}_4$  dissociates and silicon atoms are deposited on the slice, where they rapidly establish themselves as part of the original crystal structure. It is essential to saturate the tube with  $\text{SiCl}_4$  vapour to ensure a uniform layer thickness over the whole slice. There are a number of different chemical reactions that can be used for the deposition of epitaxial layers.

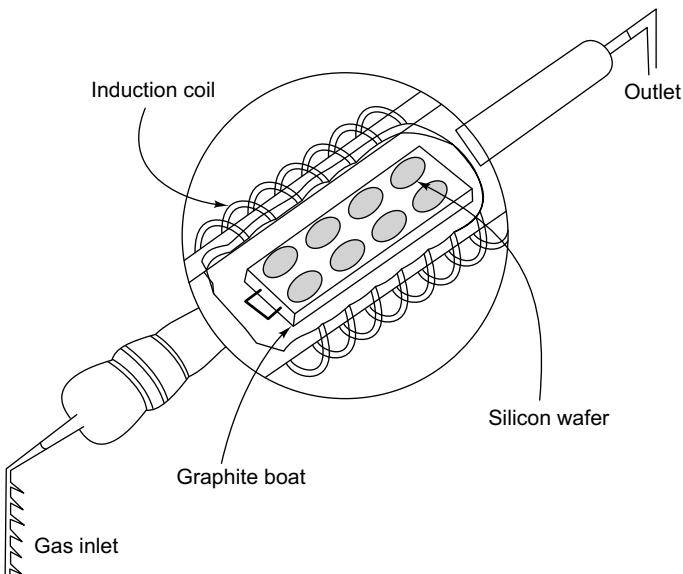
The overall reaction can be classified as hydrogen reduction of a gas.



When the hydrogen reduction of  $\text{SiCl}_4$  takes place, the reaction gives rise to free silicon atoms. Atoms from the gas phase skid along the surface of the growing epitaxial film until they find correct position in the lattice structure before becoming fastened into the growing structure. The epitaxy layer may be doped with *P* or *N*-type impurities by introducing these dopants with the required concentration, into the vapour stream.

Four silicon sources can be used for growing epitaxial silicon. These are silicon tetrachloride ( $\text{SiCl}_4$ ), dichlorosilane ( $\text{SiH}_2\text{Cl}_2$ ), trichlorosilane ( $\text{SiHCl}_3$ ) and silane ( $\text{SiH}_4$ ). Silicon tetrachloride has been the most studied and has obtained the widest industrial use.

The usual sources of dopants are hydrides of phosphorus, boron or arsenic. Generally, diborane ( $\text{B}_2\text{H}_6$ ) is used for *P*-type doping and phosphine ( $\text{PH}_3$ ) for *N*-type doping. Doping levels in epitaxial layers rarely exceed  $10^{17}$  atoms/ $\text{cm}^3$ . The epitaxy layer is about  $10\text{--}15\ \mu\text{m}$  in depth and has a resistivity, which varies in the region, around  $10\ \Omega\cdot\text{cm}$ .

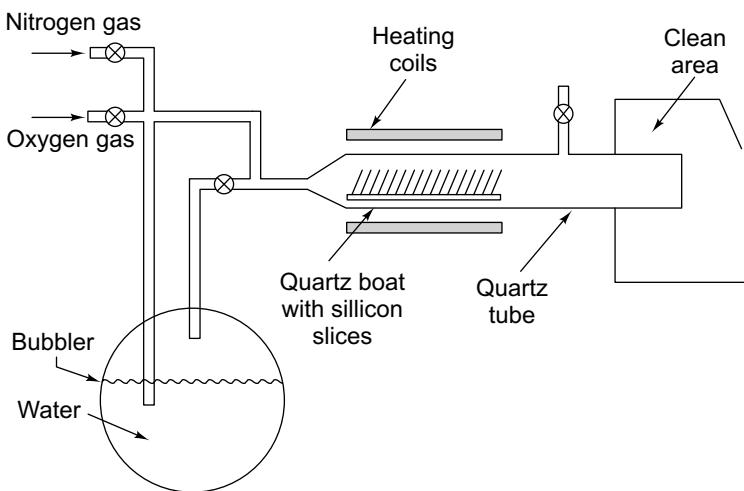


**Fig. 1.5** Epitaxy apparatus

### 1.2.3 Oxidation

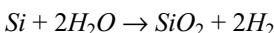
Silicon dioxide is formed by exposing the wafer to an oxygen environment at a high temperature for a controlled duration and removed from the surface of the silicon slice many times during the manufacture of an integrated circuit. This process is called *thermal oxidation* because high temperature is used to grow the oxide layer. The layer of silicon dioxide serves two important purposes.

- $SiO_2$  is an extremely hard protective coating. Hence, it is used for surface passivation and is unaffected by moisture, reagents except hydrofluoric acid and other atmospheric contaminants.
  - It acts as a diffusion mask permitting selective diffusions into silicon wafer through the windows etched in the oxide. It is also used for insulating the metal interconnections from the silicon.
- Figure 1.6 shows a typical arrangement of the apparatus used for oxidation.



**Fig. 1.6** Oxidation apparatus

The silicon wafers are kept in a quartz boat and placed in a quartz tube. The tube is heated to a temperature of 1000 to 1200°C with the use of heating coils. Care is taken for maintaining a uniform temperature along the length of the tube. The wafer is exposed to a gas containing  $O_2$  or  $H_2O$  or both. Silicon dioxide layer is formed on the surface of the silicon wafer by thermal oxidation as given by the process



A thickness of 0.02 to 2  $\mu m$  is normally grown. The thickness of the oxide layer is governed by time, temperature and the moisture content. The colour of the silicon surface changes with thickness of the oxide layer due to the shift in the wavelength of the reflected light, and it is an indication of the layer thickness.

### 1.2.4 Photolithography

The process of photolithography makes it possible to produce microscopically small circuit and device patterns on  $Si$  wafers. Its prime use in integrated circuit manufacturing is to selectively remove the oxide from the silicon slice. The openings where the  $SiO_2$  layer is removed are called as *windows* and through these windows, the diffusions are allowed to take place. The windows are produced by the process of photolithography. This process enables the fabrication of extremely small circuits and devices, numbering as many as millions of components on silicon wafers of less than 1  $cm^2$  area.

The photographic process involves the following processes.

**Resist coating** The first step in photolithography is the application of the photoresist. The photoresist is a light sensitive emulsion, which when exposed to ultraviolet radiation and curing becomes resistant to chemical corrosion. The silicon wafer is held firm in a vacuum chuck and a drop of photoresist is applied at the centre of the oxide layer. The wafer is then rotated at a speed of 5000 rpm. This spin makes the photoresist to uniformly spread as a thin coating over the oxide layer. Hence, this process is also called *spin coating*.

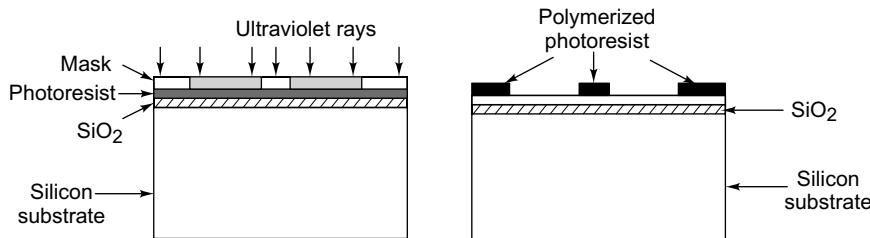
**Prebaking of photoresist** The silicon wafers coated with photoresist are then baked in an oven at a temperature of 100°C. This prebaking is necessary to harden the photoresist coat.

**Mask transfer** The next step in the process of photolithography is the aligning of the photomask over the silicon wafer. The photomask indicates the location of the windows in the oxide layer where the  $SiO_2$  layer is to be removed. Thus, a photomask is a photographic plate in which the windows are represented by an opaque area and the remaining regions are made transparent. The photomask is placed over the photoresist-coated silicon wafer. The photomasks can be aligned well over the wafer using a mask aligner.

**Resist development** The entire setup is then exposed to ultraviolet radiation. The photoresist under the transparent region of the mask becomes polymerised. These polymerised portions become tougher and they are insoluble in the developer solution. This type of photoresist is called *negative photoresist*. With a *positive photoresist*, the exposed region becomes depolymerised and is readily soluble in the developer solution.

**Selective removal or etching** After UV exposure, the mask is removed and the wafer is developed using a suitable chemical like *trichloroethylene*. This results in the removal of the photoresist film where windows are required. After developing, *curing* is done to the wafer, and this makes the polymerised area resistant to corrosion.

After developing and curing, the silicon wafer is again baked in the oven at 150°C for about 20 minutes. The chip is then dipped in an etching solution of diluted hydrofluoric acid which removes the oxide layer that is not protected by the polymerised photoresist. The hydrofluoric acid etches the  $SiO_2$  but will not remove the underlying silicon or the photoresist layer to any appreciable extent. The wafers are kept dipped in the etching solution for a sufficiently long time allowing the complete removal of  $SiO_2$  in the areas of the wafer that are not covered by the photoresist. The resultant pattern on the  $SiO_2$  layer, after etching, is a pattern of openings or windows which is same as the pattern on the photomask. Through these openings, *N* or *P*-type impurities are diffused in various steps of IC fabrication. After diffusion of impurities, the resist mask is removed using sulphuric acid and by means of a mechanical abrasion process. The process of photolithography is illustrated in Fig. 1.7.



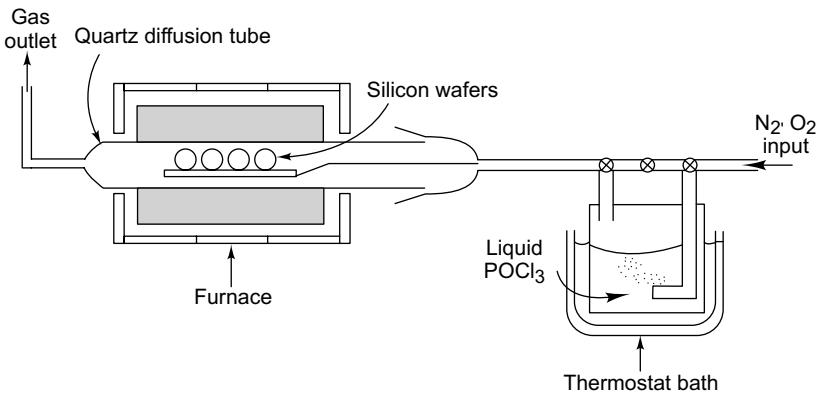
**Fig. 1.7** Photolithographic process

### 1.2.5 Diffusion

This is an important process in the fabrication of monolithic ICs. During epitaxial growth, the full epitaxy layer is doped by a closely controlled amount of impurity. On the other hand, the diffusion process enables selective areas to be doped to the required levels. The process of junction formation, i.e. generation of *P* and *N*-type areas is typically accomplished by the process of allowing the appropriate dopant or impurities to diffuse at a high temperature. It is normally carried out in a furnace similar to that used in thermal oxidation process, by placing the wafers inside it and allowing an inert gas containing the desired dopant passing through it in the temperature environment of 800–1200°C.

*P*-type semiconductor is obtained by diffusion of boron in the form of solid, liquid or gaseous source and *N*-type semiconductor is obtained by diffusion of solid, liquid or gaseous source of arsenic or phosphorus into silicon. The compounds such as boron oxide ( $B_2O_3$ ) and boron chloride ( $BCl_3$ ) are used for boron, and phosphorus pentaoxide ( $P_2O_5$ ) and phosphorus oxychloride ( $POCl_3$ ) are used as sources of phosphorus. The carrier gas such as dry oxygen or nitrogen is normally used for exposing the impurity to the diffusant at high temperatures. The depth of diffusion depends on the time allowed for diffusion and it normally extends to two hours. The diffusion profile is determined by a number of factors, namely, solid solubility, diffusion temperature, diffusion time and surface cleanliness.

The diffusion apparatus is shown in Fig. 1.8. The diffusion process uses a high temperature furnace which has a flat temperature profile over its useful length. A quartz boat containing the cleaned wafers is kept in the hot zone of the furnace. The hot zone temperature is maintained close to the melting point of silicon, i.e. 1200°C, and at this temperature, the silicon atoms are highly mobile. The impurity atoms freely move through the silicon lattice. By the process of substitution, the impurity atoms replace the silicon atoms, going from a region of higher concentration to that of lower concentration.



**Fig. 1.8** Diffusion apparatus

Substitutional diffusion takes place at high temperature conditions, when several atoms in the semiconductor move out of their lattice site leaving vacancies, into which, the impurity atoms can move in. This substitutional diffusion mechanism is applicable for most of the common diffusion processes, such as those with boron, phosphorus and arsenic. Moreover, these dopant atoms are too big to fit into the interstices. Hence, they are made to substitute in the vacancies created by silicon atoms.

**Solid solubility** It is defined as the maximum concentration of impurity which can be dissolved in the solid diffusant. The amount of dopant impurities is decided by the dopant profile required and the solid solubility of the diffusant. For example, the solid solubility of phosphorus in silicon is

$10^{21}$  atoms/cm<sup>3</sup> and the density of pure silicon is  $10^{21}$  atoms/cm<sup>3</sup>. Therefore, the pure silicon diffusant can accept phosphorus atoms only to about 2% of silicon's density.

**Diffusion temperature** At higher temperatures, the diffused impurity atoms acquire higher thermal energy and thereby, higher velocity. The impurities with higher velocities can diffuse much further into the diffusant. It is found that the *diffusion coefficient* critically depends upon temperature. Therefore, the temperature profile of the diffusion apparatus must have closely controlled flat temperature response over the entire length of its hot zone.

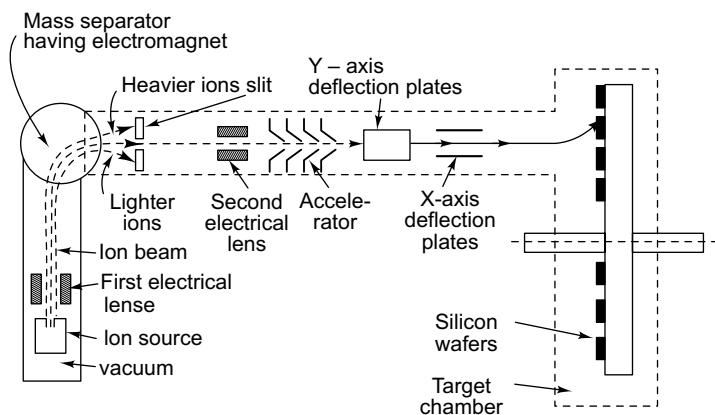
**Diffusion time** The time duration of diffusion process determines the junction depth. For Gaussian distribution profile, the net concentration will decrease due to impurity compensation, and it can approach zero with increasing diffusion time lengths.

**Surface cleanliness** The silicon surface must be prevented against contaminants during diffusion, which may interfere seriously with the uniformity of the diffusion profile. The crystal defects such as *dislocation* or *stacking faults* may produce localised impurity concentration. This results in the degradation of junction characteristics. Hence, the silicon crystals must be made highly perfect.

## 1.2.6 Ion Implantation

It is the process by which the ions of a particular impurity or dopant material are accelerated by an electric field to a very high velocity and physically implant or lodge the dopant within the semiconductor material. This is an alternate to the deposition diffusion process discussed earlier and it is used to produce a shallow surface region of dopant atoms with the average depth of penetration varying between 0.1 to  $0.6 \mu\text{m}$  depending on the velocity and the angle at which the ions strike the silicon wafer. The ions can typically be implanted off-axis from the wafer such that they experience collision with lattice atoms, thereby avoiding undesirable channelling of ions penetrating deeper into the silicon. The ion implantation can also be channelled through the silicon dioxide layer itself that changes the implant direction before the atoms enter the silicon.

The typical ion implantation system is shown in Fig.1.9. A gas containing the desired impurity is ionised inside an ion source. The ions are generated and directed from the source in a diverging beam and they are focused before passing through a mass separator that directs only the ions of the desired dopant through a narrow aperture. A second lens focuses this beam, which is then passed through an accelerator that imparts the required energy for striking at the target and become implanted in the silicon wafer. The voltage levels used for acceleration may be in the range of 20 kV to 250 kV. Since the ion beam is small, they are scanned uniformly across the



**Fig. 1.9** Ion implantation system

wafers with the use of an electro-static field over the surface of the wafer in the target chamber. Repeated scanning provides exceptionally uniform doping in the wafer. The target chamber is commonly provided with automatic wafer handling facilities for speeding the process of implanting many wafers per hour. The impurity range in the semiconductor may vary from a few hundred angstroms to around one micrometre and the distribution of impurity is approximately Gaussian.

The distribution of the implanted ions as a function of distance  $x$  from the silicon surface into the substrate is normally expressed as  $N(x)$ . That is,

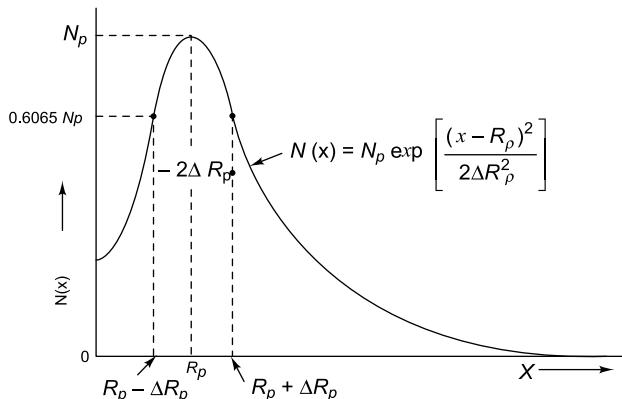
$$N(x) = N_p \exp \left[ -\frac{(x - R_p)^2}{2\Delta R_p^2} \right]$$

where  $R_p$  is the projected range of implantation

$\Delta R_p$  is the standard deviation of the projected range and

$N_p$  is the implanted ions peak concentration

The ion implantation impurity profile is shown in Fig. 1.10.



**Fig. 1.10** Impurity profile of ion implantation

The peak of implanted ion concentration is related to the implantation dosage  $Q$  by the relation

$$N_p = \frac{Q}{\sqrt{2\pi}\Delta R_p} = 0.4 \frac{Q}{\Delta R_p}$$

The implantation dosage  $Q$  is the number of implanted ions per unit of surface area. This process has the following advantages:

- (i) Accurate control over doping to within  $\pm 5\%$
- (ii) Very good reproducibility
- (iii) Predictable threshold voltage of mass devices
- (iv) Precise resistance values
- (v) A room temperature process

The limitations are:

- (i) Annealing at higher temperature is required for avoiding the crystal damage
- (ii) The possibility of dopant implanting through various layers of wafer

Hence, it is important that non-exposure to contaminants during and after the implantation process is taken care of.

The ion implantation process can also cause damage to the semiconductor crystal lattice that leaves many of the implanted ions electrically inactive. This could be set right by the process of annealing in which the temperature of the semiconductor is increased to around  $800^{\circ}\text{C}$  after the implantation process for allowing the ions to move into electrically active locations in the semiconductor crystal lattice. Laser beam and electron beam annealing are also employed, wherein only the surface region of the wafer is heated and recrystallised.

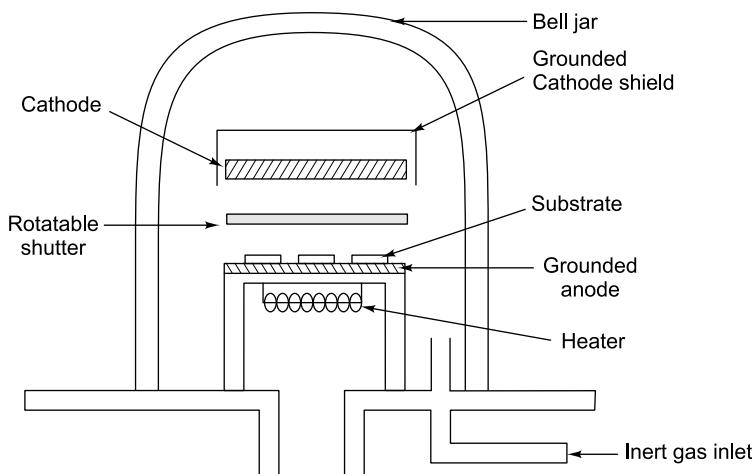
Buried conductors are typical examples, where the ion implantation of high energy type is employed. These are used when the latch-up is to be avoided in CMOS fabrication and low resistive collector regions are required in BJT fabrication.

### 1.2.7 Metallisation

Metallisation is the final step in the wafer manufacturing process. During the manufacture of integrated circuits, it is necessary to deposit a thin layer of metal on the silicon, for instance, to form aluminium interconnections. This process produces a thin-film metal layer that serves as the *conductor pattern* for the interconnection of various components on the chip. Metallisation is also used to produce bonding pads around the periphery of the chip to produce metallised areas for the bonding of wire leads from the package to the chip.

The metal films are formed by various methods such as chemical vapour deposition (CVD) and physical vapour deposition (PVD).

The arrangement of metallisation process using *vacuum deposition technique* is shown in Fig. 1.11. The silicon wafers are placed face down around the bell jar, with the source of metal in the centre. The vacuum pressure is lowered to below  $5 \times 10^{-6}$  Torr before the metal deposition commences. The silicon is then heated to a temperatures range of 100 to  $300^{\circ}\text{C}$ , which causes the deposited metal to chemically react with the silicon dioxide and adhere to the wafer surface. Upward evaporation is also used to prevent impurities, which may be generated by the heat source, from falling onto the wafers. The metal film is normally of  $1 \mu\text{m}$  thickness. The thickness can be monitored by including a quartz crystal oscillator in the vacuum, whose frequency can be set with the amount of metal to be deposited on its surface.



**Fig. 1.11** Arrangement for vacuum deposition

After evaporation, the wafers are heated at about  $1500^{\circ}\text{C}$  in an inert-gaseous (e.g. nitrogen) atmosphere. This causes the metal to alloy well with the silicon surface so that low resistance is achieved in the interface between the two. This is referred to as a *low ohmic contact* joint.

### 1.2.8 Circuit Probing

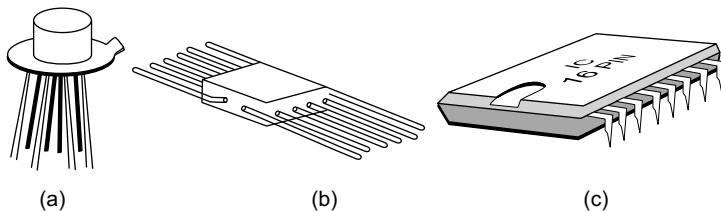
The performance of each of the integrated circuit fabricated on the wafer is checked electrically by placing probes on the bonding pads of the ICs. Faulty chips are identified and discarded after scribing and separating the individual chips from the wafer.

### 1.2.9 Scribing and Separating into Chips

The wafer, in which hundreds of ICs are fabricated, is broken into individual chips by scribing with a diamond-tipped tool.

### 1.2.10 Mounting and Packaging

The individual chip cannot be directly handled because it is very small and brittle. Hence, it is soldered to a gold plated header with which leads have already been connected. Some of the standard packages available are top-hat (TO) package, flat package and dual-in-line plastic package shown in Fig. 1.12(a), (b) and (c) respectively.



**Fig. 1.12** (a) Top-hat (TO) package (b) Flat package (c) Dual-in-line plastic package

### 1.2.11 Encapsulation

Encapsulation of an IC is essential to protect it against mechanical and chemical damage while in use. The encapsulation is done by placing a cap over the circuit and sealing it in an inert atmosphere.

## 1.3 CONSTRUCTION OF A MONOLITHIC BIPOLAR TRANSISTOR

The fabrication of a monolithic transistor includes the following steps.

- (i) Epitaxial growth
- (ii) Oxidation
- (iii) Photolithography
- (iv) Isolation diffusion
- (v) Base diffusion
- (vi) Emitter diffusion
- (vii) Contact mask
- (viii) Aluminium metallization
- (ix) Passivation

The letters *P* and *N* in the figures refer to the type of doping, and a minus (−) or plus (+) with *P* and *N* indicates lighter or heavier doping respectively.

### 1.3.1 Epitaxial Growth

The first step in the transistor fabrication is creation of the collector region. We normally require a low resistivity path for the collector current. This is due to the fact that, the collector contact is normally taken at the top, thus increasing the collector series resistance and the  $V_{CE(Sat)}$  of the device. The higher collector resistance is reduced by a process called *buried layer* as shown in Fig. 1.13. In this arrangement, a heavily doped  $N^+$  region is sandwiched between the  $N$ -type epitaxial layer and  $P$ -type substrate. This buried  $N^+$  layer provides a low resistance path in the active collector region to the collector contact C. In effect, the buried layer provides a low resistance shunt path for the flow of current.

For fabricating an *NPN* transistor, we begin with a  $P$ -type silicon substrate having a resistivity of typically  $1\Omega\text{-cm}$ , corresponding to an acceptor ion concentration of  $1.4 \times 10^{15}$  atoms/cm $^3$ . An oxide mask with the necessary pattern for buried layer diffusion is prepared. This is followed by masking and etching the oxide in the buried layer mask.

The  $N$ -type buried layer is now diffused into the substrate. A slow-diffusing material such as arsenic or antimony is used, so that the buried layer will *stay-put* during subsequent diffusions. The junction depth is typically a few microns, with sheet resistivity of around  $20\ \Omega$  per square.

Then, an epitaxial layer of lightly doped  $N$ -silicon is grown on the  $P$ -type substrate by placing the wafer in the furnace at  $1200^\circ\text{C}$  and introducing a gas containing phosphorus (donor impurity). The resulting structure is shown in Fig. 1.13.

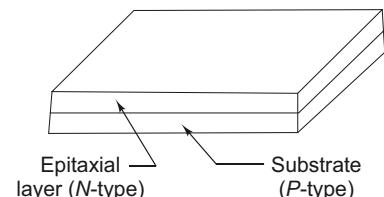
The subsequent diffusions are done in this epitaxial layer. All active and passive components are formed on the thin  $N$ -type epitaxial layer grown over the  $P$ -type substrate. Obtaining an epitaxial layer of the proper thickness and doping with high crystal quality is perhaps the most formidable challenge in bipolar device processing.

### 1.3.2 Oxidation

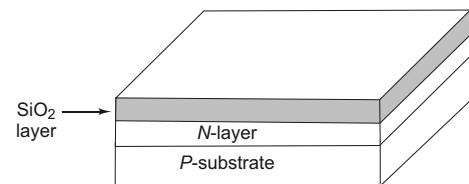
As shown in Fig. 1.14, a thin layer of silicon dioxide ( $\text{SiO}_2$ ) is grown over the  $N$ -type layer by exposing the silicon wafer to an oxygen atmosphere at about  $1000^\circ\text{C}$ .

### 1.3.3 Photolithography

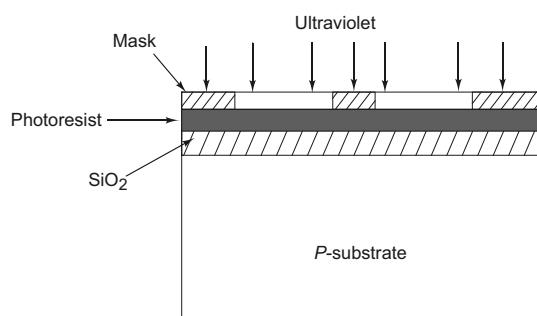
The prime use of photolithography in IC manufacturing is to selectively etch or remove the  $\text{SiO}_2$  layer. As shown in Fig. 1.15(a), the surface of the oxide is first covered with a thin uniform layer of photosensitive emulsion (Photoresist). The mask, a black and white negative of the required pattern, is placed over the structure. When exposed to ultraviolet light, the photoresist under the transparent region of the mask becomes polymerised. The mask is then removed and the wafer is treated chemically that removes the unexposed portions of the photoresist film. The polymerised region is cured so that it becomes



**Fig. 1.13** Epitaxial growth



**Fig. 1.14** Oxidation



**Fig. 1.15** (a) Masking and exposure to ultraviolet radiation

resistant to corrosion. Then the chip is dipped in an etching solution of hydrofluoric acid which removes the oxide layer not protected by the polymerised photoresist. This creates openings in the  $SiO_2$  layer through which  $P$ -type or  $N$ -type impurities can be diffused using the isolation diffusion process as shown in Fig. 1.15(b). After diffusion of impurities, the polymerised photoresist is removed with sulphuric acid and by a mechanical abrasion process.

### 1.3.4 Isolation Diffusion

The integrated circuit contains many devices. Since a number of devices are to be fabricated on the same IC chip, it becomes necessary to provide good isolation between various components and their interconnections.

The most important techniques for isolation are:

- (i)  $PN$  junction isolation
- (ii) Dielectric isolation

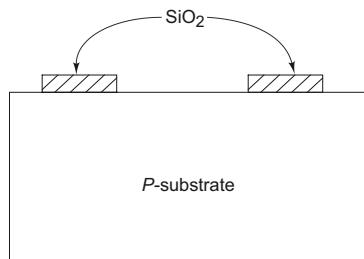
In  $PN$  junction isolation technique, the  $P^+$  type impurities are selectively diffused into the  $N$ -type epitaxial layer so that it touches the  $P$ -type substrate at the bottom. This method generates  $N$ -type isolation regions surrounded by  $P$ -type moats. If the  $P$  substrate is held at the most negative potential, the diodes will become reverse-biased, thus providing isolation between these islands. The individual components are fabricated inside these islands. This method is very economical, and is the most commonly used isolation method for general purpose integrated circuits.

In dielectric isolation method, a layer of solid dielectric such as silicon dioxide or ruby surrounds each component and this dielectric provides isolation. The isolation is both physical and electrical. This method is very expensive due to additional processing steps needed and this is mostly used for fabricating ICs required for special applications in military and aerospace.

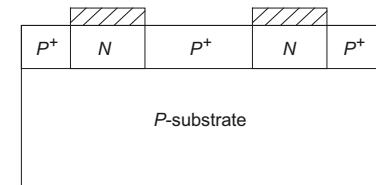
The  $PN$  junction isolation diffusion method is shown in Fig. 1.16. The process takes place in a furnace using boron source. The diffusion depth must be at least equal to the epitaxial thickness in order to obtain complete isolation. Poor isolation results in device failures as all transistors might get shorted together. The  $N$ -type island shown in Fig. 1.16 forms the collector region of the  $NPN$  transistor. The heavily doped  $P$ -type regions marked  $P^+$  are the isolation regions for the active and passive components that will be formed in the various  $N$ -type islands of the epitaxial layer.

### 1.3.5 Base Diffusion

Formation of the base is a critical step in the construction of a bipolar transistor. The base must be aligned so that, during diffusion, it does not come into contact with either the isolation region or the buried layer. Frequently, the base diffusion step is also used in parallel to fabricate diffused resistors for the circuit. The value of these resistors depends on the diffusion conditions and the width of the opening made during etching. The base width influences the transistor parameters very strongly. Therefore, the base junction depth and resistivity must be tightly controlled. The base sheet resistivity should be fairly high ( $200\text{--}500 \Omega$  per square) so that the base does not inject carriers into the emitter. For  $NPN$  transistor, the



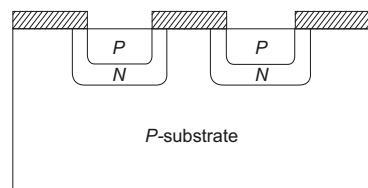
**Fig. 1.15 (b)** Selective openings in the  $SiO_2$  layer



**Fig. 1.16** Isolation diffusion

base is diffused in a furnace using a boron source. The diffusion process is done in two steps, predeposition of dopants at  $900^{\circ}\text{C}$  and driving them in at about  $1200^{\circ}\text{C}$ . The drive-in is done in an oxidising ambience, so that oxide is grown over the base region for subsequent fabrication steps.

Figure 1.17 shows the *P*-type base region of the transistor diffused in the *N*-type island (collector region) using photolithography and isolation diffusion processes.



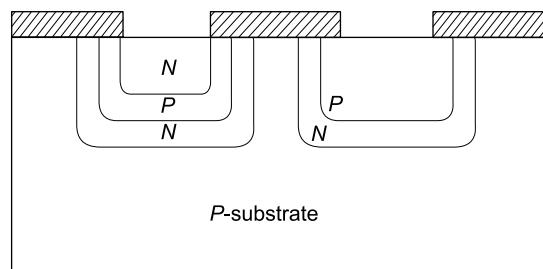
**Fig. 1.17** Base diffusion

### 1.3.6 Emitter Diffusion

Emitter diffusion is the final step in the fabrication of the transistor. The emitter opening must lie wholly within the base. Emitter masking not only opens windows for the emitter, but also for the contact point, which provides a low-resistivity *ohmic contact* path for the emitter terminal.

The emitter diffusion is normally a heavy *N*-type diffusion, producing low-resistivity layer that can inject charge easily into the base. A phosphorus source is commonly used so that the diffusion time is shortened and the previous diffusion layers do not diffuse further. The emitter is diffused into the base, so that the emitter junction depth very closely approaches the base junction depth. The active base is then a *P*-region between these two junctions, which can be made very narrow by adjusting the emitter diffusion time. Various diffusion and drive-in cycles can be used to fabricate the emitter. The resistivity of the emitter is usually not too critical.

The *N*-type emitter region of the transistor diffused into the *P*-type base region is shown in Fig. 1.18. However, this is not needed to fabricate a resistor where the resistivity of the *P*-type base region itself will serve the purpose. In this way, an *NPN* transistor and a resistor are fabricated simultaneously.

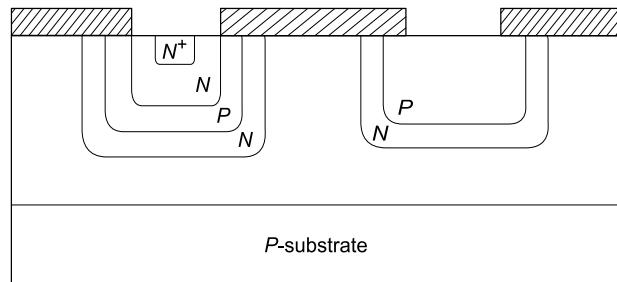


**Fig. 1.18** Emitter diffusion

### 1.3.7 Contact Mask

After the fabrication of emitter, windows are etched into the *N*-type regions where contacts are to be made for collector and emitter terminals. Heavily concentrated phosphorus  $\text{N}^+$  dopant is diffused into these regions simultaneously.

The reason for the use of heavy  $\text{N}^+$  diffusion is explained as follows: Aluminium, being a good conductor used for interconnection, is a *P*-type of impurity when used with silicon. Therefore, it can produce an unwanted diode or rectifying contact with the lightly doped *N*-material. Introducing a high concentration of  $\text{N}^+$  dopant causes the *Si* lattice at the surface *semi-metallic*. Thus, the  $\text{N}^+$  layer makes a very good ohmic contact with the Aluminium layer. Figure 1.19 shows the pre-ohmic etch pattern used to get a good metal ohmic (non-rectifying) contact with the diffused region. This is done by the oxidation, photolithography and isolation diffusion processes.



**Fig. 1.19** Pre-ohmic etch

### 1.3.8 Metallisation

The IC chip is now complete with the active and passive devices, and the metal leads are to be formed for making connections with the terminals of the devices. Aluminium is deposited over the entire wafer by vacuum deposition. The thickness for single layer metal is fraction of a  $\mu\text{m}$ . Metallisation is carried out by evaporating aluminium over the entire surface and then selectively etching away aluminium to leave behind the desired interconnection and bonding pads as shown in Fig. 1.20.

Metallisation is done for making interconnection between the various components fabricated in an IC and providing bonding pads around the circumference of the IC chip for later connection of wires.

### 1.3.9 Passivation

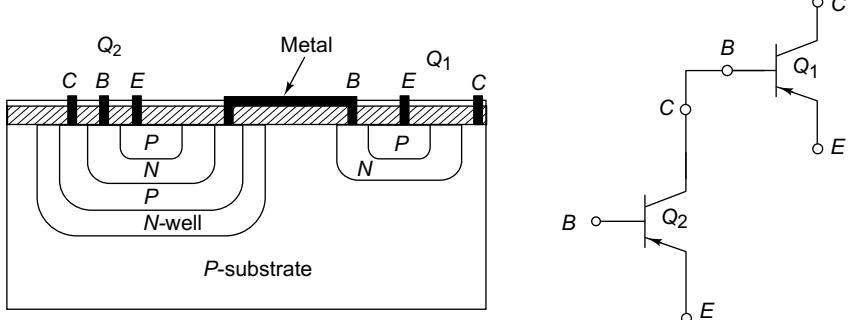
Metallisation is followed by passivation, in which an insulating and protective layer is deposited over the whole device. This protects it against mechanical and chemical damage during subsequent processing steps. Doped or undoped silicon oxide or silicon nitride, or some combination of them, are usually chosen for passivation of layers. The layer is deposited by chemical vapour deposition (CVD) technique at a temperature low enough not to harm the metallisation.

## 1.4 PNP TRANSISTORS

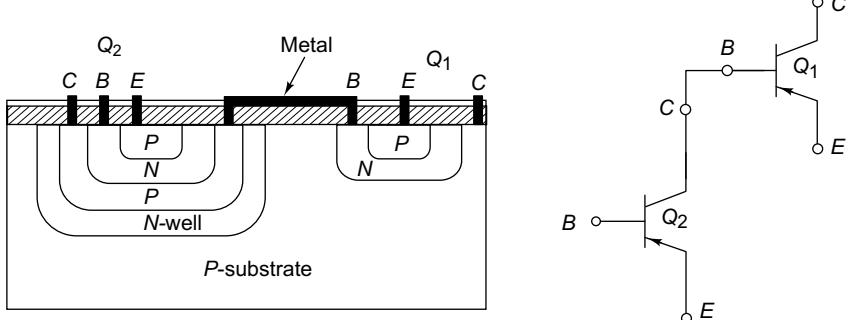
The integrated *PNP* transistors are fabricated in one of the following three structures.

- (i) Substrate or vertical *PNP*
- (ii) Lateral or horizontal *PNP*
- (iii) Triple diffused *PNP*

**Substrate or vertical *PNP*** The *P*-substrate of the IC is used as the collector, the *N*-epitaxial layer is used as the base and the next *P*-diffusion is used as the emitter region of the *PNP* transistor. The structure of a vertical monolithic *PNP* transistor  $Q_1$  is shown in Fig. 1.21. The base region of an *NPN* transistor structure can be formed in parallel with the emitter region of the *PNP* transistor.



**Fig. 1.20** Metallisation (*NPN* transistor)



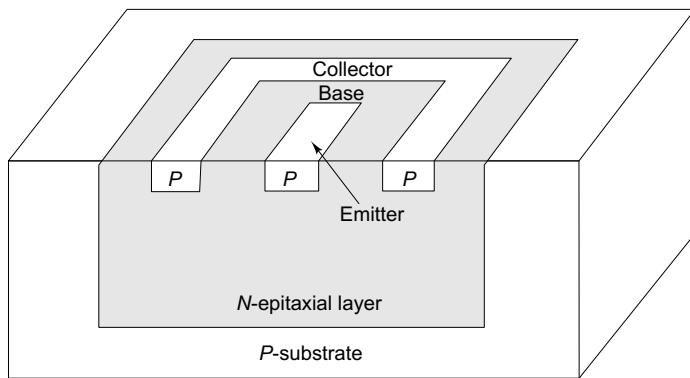
**Fig. 1.21** Vertical and triple diffused monolithic *PNP* transistors

This method of fabrication has the disadvantage of having its collector held at a fixed negative potential. This is due to the fact that the *P*-substrate of the IC is always held at a negative potential normally for providing good isolation between the circuit components and the substrate.

**Triple diffused PNP** This type of *PNP* transistor is formed by including an additional diffusion process over the standard *NPN* transistor processing steps. This is called as triple diffusion process, because it involves an additional diffusion of *P*-region in the second *N*-diffusion region of a *NPN* transistor. The structure of the triple diffused monolithic *PNP* transistor  $Q_2$  is also shown in Fig. 1.21.

This has the limitation of requiring additional fabrication steps and sophisticated fabrication assemblies.

**Lateral or horizontal PNP** This is the most commonly used form of integrated *PNP* transistor fabrication method. This has the advantage that it can be fabricated simultaneously with the processing steps of an *NPN* transistor and therefore it requires no additional masking and diffusion steps. The *N*-type epitaxial layer is used as the base of the *PNP* transistor. During the *P*-type base diffusion process of *NPN* transistor, two parallel *P*-regions are formed which make the emitter and collector regions of the horizontal *PNP* transistor. This arrangement is shown in Fig. 1.22.

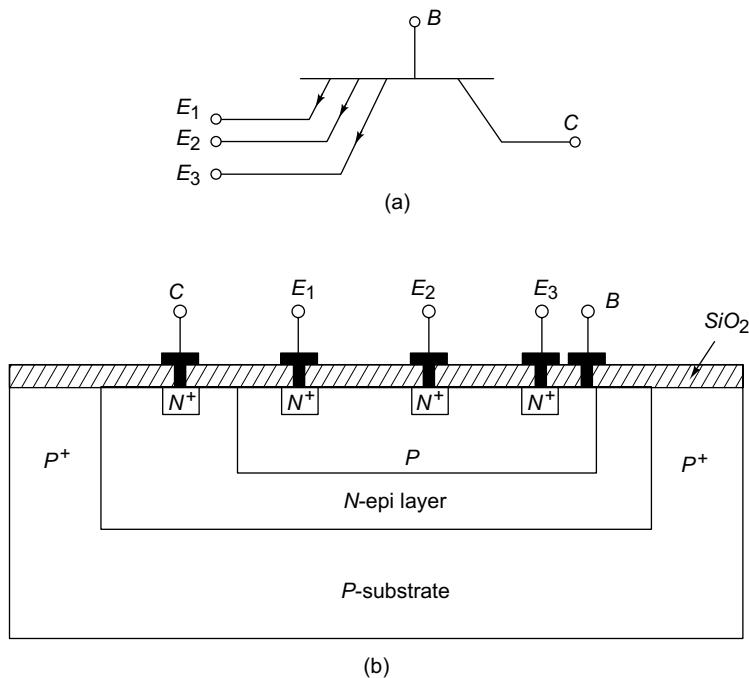


**Fig. 1.22** A lateral monolithic *PNP* transistor

**Comparison of monolithic *NPN* and *PNP* transistors** Normally, the *NPN* transistor is preferred in monolithic circuits due to the following reasons:

- (i) The vertical *PNP* transistor must have his collector held at a fixed negative voltage.
- (ii) The lateral *PNP* transistor has very wide base region and has the limitation due to the lateral diffusion of *P*-type impurities into the *N*-type base region. This makes the photographic mask making, alignment and etching processes very difficult. This reduces the current gain of lateral *PNP* transistors as low as 1.5 to 30 as against 50 to 300 for a monolithic *NPN* transistor.
- (iii) The collector region is formed prior to the formation of base and emitter diffusion. During the later diffusion steps, the collector impurities diffuse on either side of the defined collector junction. Since the *N*-type impurities have smaller diffusion constant compared to *P*-type impurities, the *N*-type collector performs better than the *P*-type collector. This makes the *NPN* transistor preferable for monolithic fabrication due to the easier process control.

**Transistor with multiple emitters** The applications such as transistor-transistor logic (TTL) require multiple emitters. Figure 1.23 shows the cross-sectional view of three  $N^+$  emitter regions diffused in three places inside the *P*-type base. This arrangement saves the chip area and enhances the component density of the IC.



**Fig. 1.23** A Multi-emitter transistor (a) Cross-sectional view and (b) Symbol

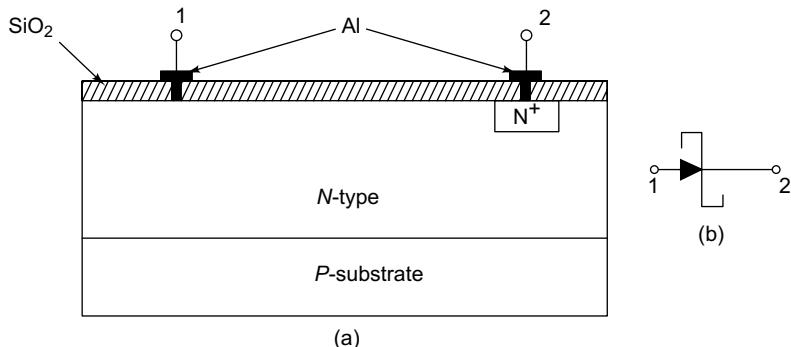
## 1.5 SCHOTTKY BARRIER DIODE

The metal contacts are required to be ohmic and no  $PN$  junctions to be formed between the metal and silicon layers. The  $N^+$  diffusion region serves the purpose of generating ohmic contacts. On the other hand, if aluminium is deposited directly on the  $N$ -type silicon, then a metal-semiconductor diode can be said to be formed. Such a metal semiconductor diode junction exhibits the same type of  $V-I$  characteristics as that of an ordinary  $PN$  junction.

The cross-sectional view and symbol of a Schottky barrier diode are shown in Fig. 1.24(a) and (b) respectively. Contact 1 shown in Fig. 1.24(a) is a Schottky barrier and the contact 2 is an ohmic contact. The contact potential between the semiconductor and the metal generates a barrier for the flow of conducting electrons from semiconductor to metal. When the junction is forward biased, this barrier is lowered and the electron flow is allowed from semiconductor to metal, where the electrons are in large quantities.

The majority carriers carry the conduction current in the Schottky diode whereas in the  $PN$  junction diode, minority carriers carry the conduction current and it incurs an appreciable time delay from ON state to OFF state. This is due to the fact that the minority carriers stored in the junction have to be totally removed.

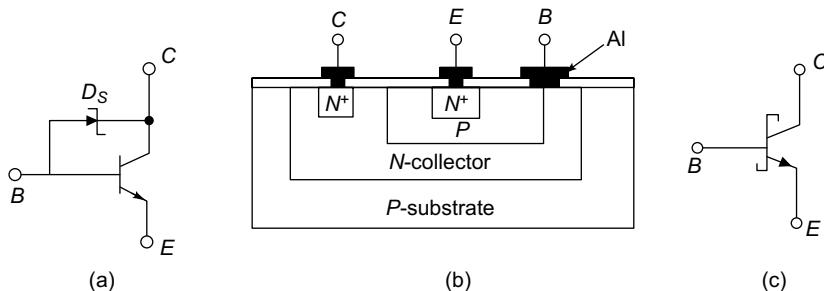
This characteristic puts the Schottky barrier diode at an advantage since it exhibits negligible storage time to flow the electron from  $N$ -type silicon into aluminium almost right at the contact surface, where they mix with the free electrons. The other advantage of this type of diode is that it has less forward voltage (approximately 0.4V). Thus, it can be used for clamping and detection in high frequency applications and microwave integrated circuits.



**Fig. 1.24** Schottky barrier diode (a) Cross-sectional view and (b) Symbol

## 1.6 SCHOTTKY TRANSISTOR

The cross-sectional view of a transistor employing a Schottky barrier diode clamped between its base and collector regions is shown in Fig. 1.25(a). The equivalent circuit and the symbolic representation of the Schottky transistor are shown in Fig. 1.25(b) and (c) respectively. The Schottky diode is formed by allowing aluminium metallisation for the base lead which makes contact with the  $N$ -type collector region also as shown in Fig. 1.25(a).



**Fig. 1.25** Schottky transistor (a) Cross-sectional view, (b) Equivalent circuit and (c) Symbol

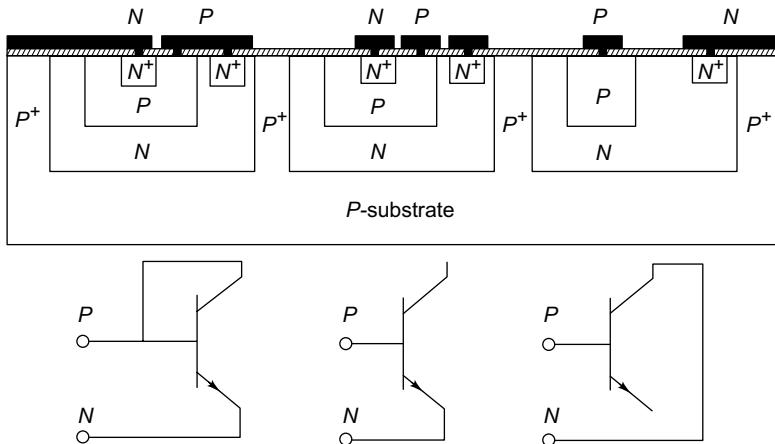
When the base current is increased to saturate the transistor, the voltage at the collector  $C$  reduces and this makes the diode  $D_S$  conduct. The base to collector voltage reduces to 0.4 V, which is less than the *cut-in* voltage of a silicon base-collector junction. Therefore, the transistor does not get saturated.

## 1.7 MONOLITHIC DIODES

The diodes used in integrated circuits are made using transistor structures in one of the five possible connections. The three most popular structures are shown in Fig. 1.26. The diode is obtained from a transistor structure using one of the following structures.

- (i) The emitter-base diode, with the collector short-circuited to the base
- (ii) The emitter-base diode, with the collector open
- (iii) The collector-base diode, with the emitter open-circuited.

The choice of the diode structure depends on the performance and application desired. Collector-base diodes have higher collector-base voltage breaking rating, and they are suitable for common-cathode diode arrays diffused within a single isolation island. The emitter-base diffusion is very popular for the fabrication of diodes, provided the reverse-voltage requirement of the circuit does not exceed the lower base-emitter breakdown voltage.



**Fig. 1.26** Popular structures for monolithic diodes

## 1.8 INTEGRATED RESISTORS

A resistor in a monolithic integrated circuit is obtained by utilising the bulk resistivity of the diffused volume of semiconductor region. The commonly used methods for fabricating integrated resistors are (i) diffused, (ii) epitaxial, (iii) pinched and (iv) thin film techniques.

**Diffused resistor** The diffused resistor is formed in any one of the isolated regions of epitaxial layer during base or emitter diffusion processes. This type of resistor fabrication is very economical as it runs in parallel to the bipolar transistor fabrication. The *N*-type emitter diffusion and *P*-type base diffusion are commonly used to realise the monolithic resistor.

The diffused resistor has a severe limitation in that, only small valued resistors can be fabricated. The surface geometry such as the length, width and the diffused impurity profile determine the resistance value. The commonly used parameter for defining this resistance is called the *sheet resistance*. It is defined as the resistance in ohms/square offered by the diffused area.

In the monolithic resistor, the resistance value is expressed by

$$R = R_s \frac{l}{w}$$

where  $R$  = resistance offered (in ohms)

$R_s$  = sheet resistance of the particular fabrication process step involved (in ohms/square\*)

$l$  = length of the diffused area and

$w$  = width of the diffused area

(\* For example 1 square = 1 mil  $\times$  1 mil; 1 mil = 1 milli inch = 25.4  $\mu\text{m}$ )

The sheet resistance of the base and emitter diffusion is 200  $\Omega$ /square and 2.2 ohm/square respectively.

For example, an emitter-diffused strip of 2mil wide and 20mil long will offer a resistance of  $22\ \Omega$ . For higher values of resistances, the diffusion region can be formed in a zig-zag fashion resulting in larger effective length. The polysilicon layer can also be used for resistor realisation.

### Example 1.1

Assume that the sheet resistance of P-type diffusion is  $200\ \Omega/\text{square}$ . Design a  $5\ k\Omega$  diffused resistor.

**Solution** Given the sheet resistance  $R_s = 200\ \Omega/\text{square}$ .

$$\text{Then the resistance } R = 5\ k\Omega = R_s \frac{l}{w} = 200 \times \frac{l}{w}$$

$$\text{Therefore, } \frac{l}{w} = \frac{R}{R_s} = \frac{5000}{200} = 25.$$

So, a  $5\ k\Omega$  resistor can be fabricated by using a pattern of  $25\ \text{mil} \times 1\ \text{mil}$ .

### Example 1.2

Given the sheet resistance of polysilicon layer as  $30\ \Omega/\text{square}$ , design a  $1\ k\Omega$  resistor.

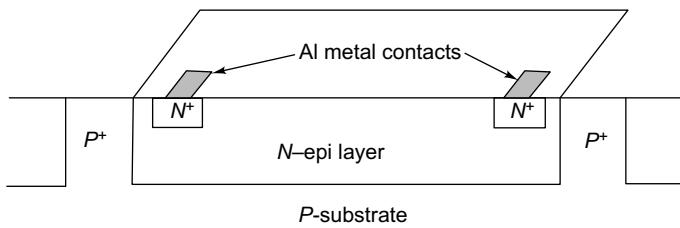
**Solution** Given the sheet resistance  $R_s = 30\ \Omega/\text{square}$ .

$$\text{Then the resistance } R = 1\ k\Omega = R_s \frac{l}{w} = 30 \times \frac{l}{w}$$

$$\text{Therefore, } \frac{l}{w} = \frac{R}{R_s} = \frac{1000}{30} = \frac{100}{3}.$$

So, a  $1\ k\Omega$  resistor can be fabricated by using a pattern of  $100\ \text{mil} \times 3\ \text{mil}$  in the polysilicon layer.

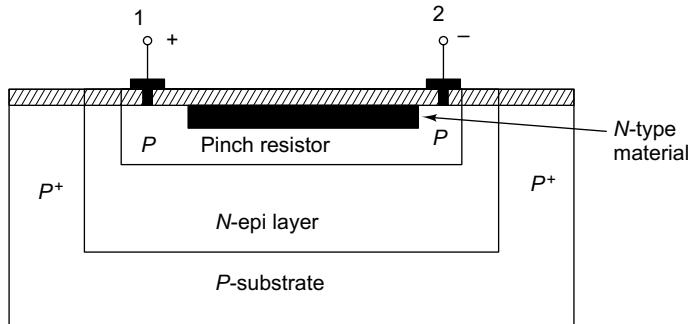
**Epitaxial resistor** The N-epitaxial layer can be used for realising large resistance values. Figure 1.27 shows the cross-sectional view of the epitaxial resistor formed in the epitaxial layer between the two  $N^+$  aluminium metal contacts.



**Fig. 1.27** Structure of an epitaxial resistor

**Pinched resistor** The sheet resistance offered by the diffusion regions can be increased by narrowing down its effective cross-sectional area. This type of resistance is normally achieved in the base region. Figure 1.28 shows a pinched base diffused resistor. It can offer resistances of the order of mega ohms in a comparatively smaller area. In the structure shown, no current can flow in the N-type material since the diode realised at contact 2 is biased in the reversed direction. Only very small reverse saturation current can flow in the N-region. Therefore, by forming this N-region in the base diffusion, the conduction

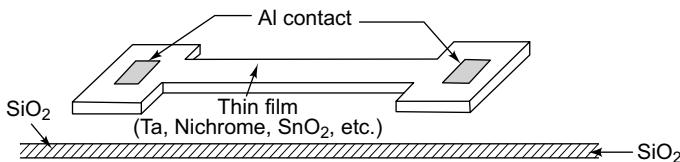
path for the current has been reduced or pinched. Therefore, the resistance between the contact 1 and 2 increases as the width narrows down and hence it acts as a *pinched resistor*.



**Fig. 1.28** Cross-sectional view of a pinched resistor

**Thin film resistor** The thin film deposition technique can also be used for the fabrication of monolithic resistors. A very thin metallic film of thickness less than  $1\text{ }\mu\text{m}$  is deposited on the silicon dioxide layer by vapour deposition techniques. Normally, Nichrome ( $NiCr$ ) is used for this process. Desired geometry is achieved using masked etching processes to obtain suitable value of resistors. Ohmic contacts are made using aluminium metallisation as discussed in the earlier sections.

The cross-sectional view of a thin film resistor is shown in Fig. 1.29. Sheet resistances of 40 to  $400\text{ }\Omega/\text{square}$  can be easily obtained in this method and thus  $20\text{ k}\Omega$  to  $50\text{ k}\Omega$  values are very practical.



**Fig. 1.29** Cross-sectional view of a thin film resistor

The advantages of thin film resistors are as follows:

- (i) They have smaller parasitic components which makes their high frequency behaviour good.
- (ii) The thin film resistor values can be very minutely controlled using laser trimming.
- (iii) They have low temperature coefficient of resistance and this makes them more stable.

The thin film resistor can be obtained by the use of Tantalum deposited over silicon dioxide layer. The main disadvantage of thin film resistor is that its fabrication requires additional processing steps.

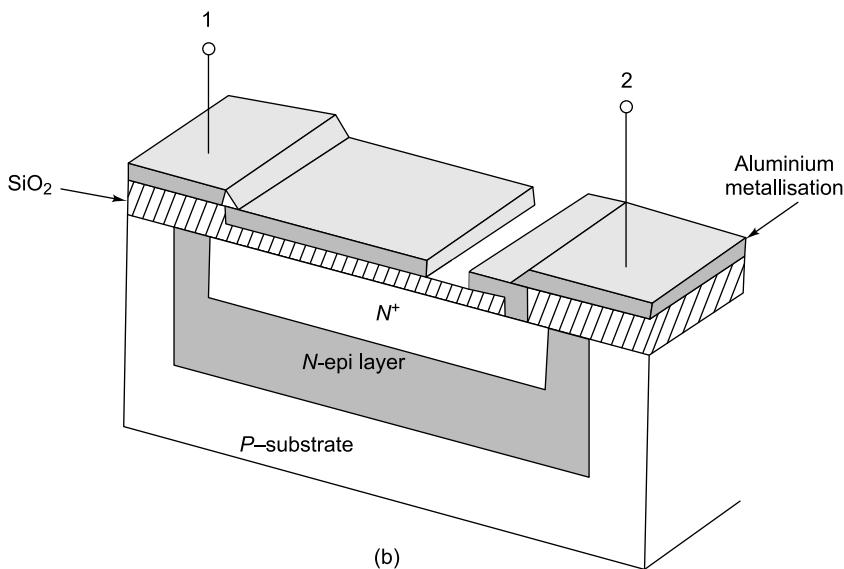
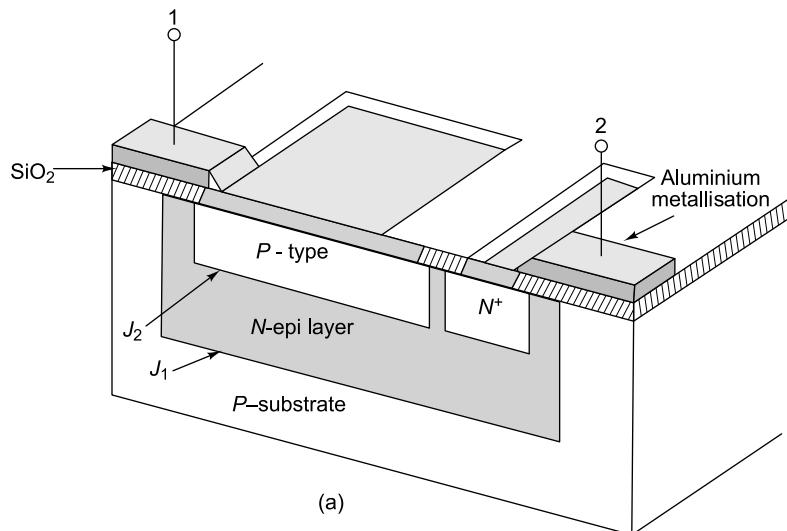
## 1.9 MONOLITHIC CAPACITORS

Monolithic capacitors are not frequently used in integrated circuits since they are limited in the range of values obtained and their performance. There are, however, two types available, the junction capacitor and the thin film capacitor as shown in Fig. 1.30. The junction capacitor is a reverse biased  $PN$  junction formed by the collector-base or emitter-base diffusion of the transistor. The capacitance is proportional to the area of the junction and inversely proportional to the depletion thickness.

$C \propto A$ , where  $A$  is the area of the junction and

$C \propto T^{-1}$ , where  $T$  is the thickness of the depletion layer

The capacitance value thus obtainable can be around  $1.2 \text{ nF/mm}^2$



**Fig. 1.30** Cross-section of (a) Monolithic junction capacitor, (b) Thin-film capacitor

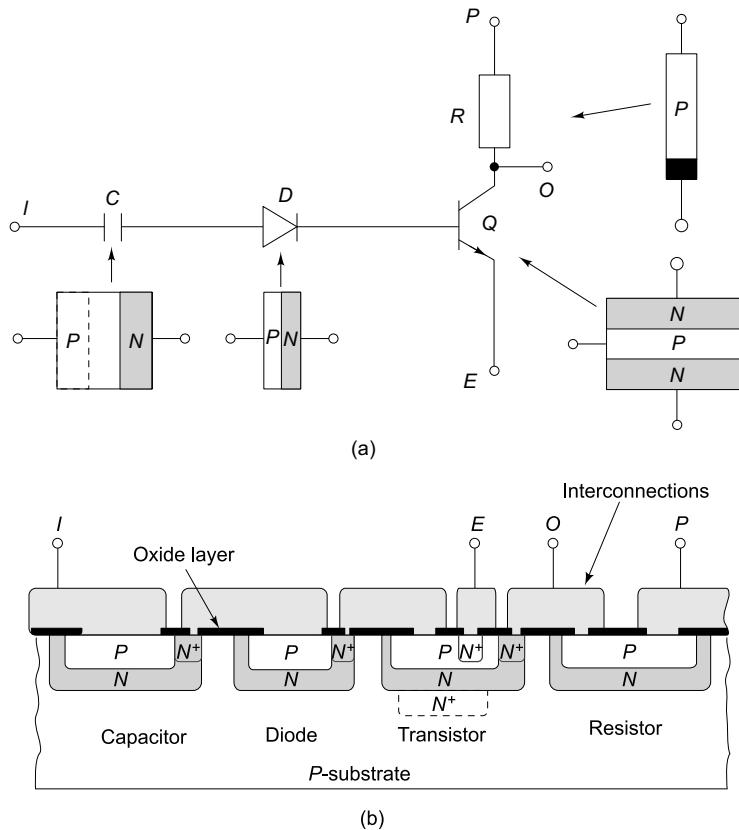
The thin-film or metal oxide silicon capacitor uses a thin layer of silicon dioxide as the dielectric. One plate is the connecting metal and the other is a heavily doped layer of silicon, which is formed during the emitter diffusion. This capacitor has a lower leakage current and is non-directional, since emitter plate can be biased positively. The capacitance value of this method can be varied between  $0.3$  and  $0.8 \text{ nF/mm}^2$ .

## 1.10 MONOLITHIC INDUCTORS

No satisfactory integrated inductors exist. If high  $Q$  inductors with inductance of values larger than  $5 \mu\text{H}$  are required, they are usually supplied by a wound inductor which is connected externally to the chip. Therefore, the use of inductors is normally avoided when integrated circuits are used.

## 1.11 TRANSFORMATION OF A HYPOTHETICAL ELECTRONIC CIRCUIT INTO MONOLITHIC FORM

Figure 1.31 shows a hypothetical electronic circuit and the possible monolithic integrated circuit realisation.



**Fig. 1.31** (a) Hypothetical electronic circuit and (b) Possible IC realisation

## 1.12 FABRICATION OF FIELD EFFECT TRANSISTORS

The FET is a device in which the flow of current through the conducting region is controlled by an electric field and hence the name Field Effect Transistor (FET). As current conduction is only by majority carriers, FET is said to be a unipolar device.

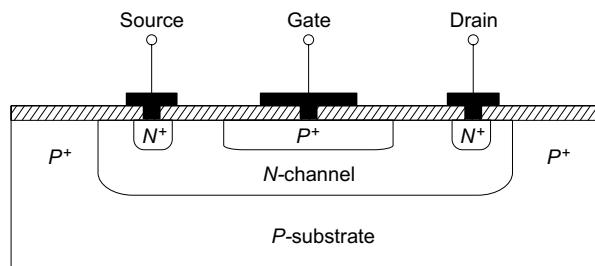
Based on the construction, the Field Effect Transistors are classified into two types, namely, (i) Junction Field Effect Transistor (JFET) and (ii) Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) or Insulated Gate FET (IGFET) or Metal Oxide Silicon Transistor (MOST).

Depending upon the majority carriers, JFET has been classified into two types, namely, (i) *N*-channel JFET with electrons as the majority carriers, and (ii) *P*-channel JFET with holes as the majority carriers.

The fabrication of monolithic *N*-channel JFET and MOSFET, and the Complementary Metal-Oxide-Semiconductor (CMOS) are discussed in the following sections.

### 1.12.1 Junction Field Effect Transistor (JFET)

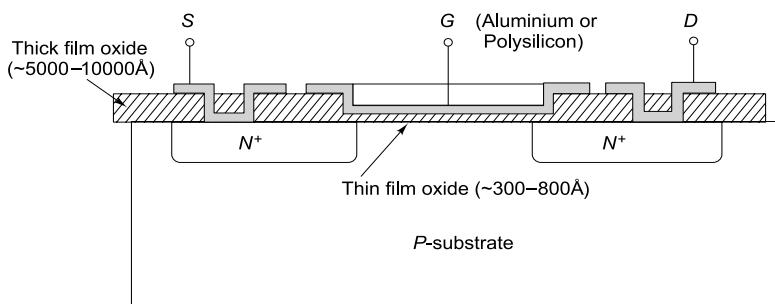
The structural arrangement of an *N*-channel JFET is depicted in Fig. 1.32. The processing steps as followed for *NPN* and *PNP* transistors are used for JFET fabrication also. The epitaxial layer of the monolithic IC forms the *N*-channel of the JFET. The  $P^+$  gate structure is formed in the *N*-channel by diffusion process or ion-implantation procedure. The drain and source connections are made through the ohmic contact regions as shown in Fig. 1.32. The ohmic regions are diffusion regions with  $N^+$  regions of higher doping concentration. They provide good ohmic contacts which are only *resistive* in nature and are not *rectifying*.



**Fig. 1.32** *N*-channel monolithic JFET

### 1.12.2 Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET)

The two types of MOSFET devices, namely, the enhancement type and depletion type can be fabricated in IC Technology. The cross-sectional view of an *N*-channel enhancement MOSFET is shown in Fig. 1.33. The substrate forms the channel of the MOS transistor. The metallic or polysilicon gate  $G$  is grown over an insulating  $SiO_2$  layer. This is formed by oxidation process and it is normally 300–800 Å with extremely high resistances of the order of  $10^{10}$  to  $10^{15} \Omega$ .



**Fig. 1.33** *N*-channel monolithic MOSFET

The threshold voltage  $V_T$  of a MOSFET is determined by the gate material, insulation material and its thickness, substrate doping and other process conditions such as impurities in the silicon-insulator surface. The typical  $V_T$  of 350 nm process technology is 0.7 V for PMOS and 0.5 V for NMOS devices.

The superior masking properties of Silicon Nitride ( $Si_3N_4$ ) make this material an effective dielectric for use in monolithic MOSFET fabrication. The dielectric constant of  $Si_3N_4$  is 7.5 as compared to 4.0 of

$\text{SiO}_2$ . This higher value of dielectric constant reduces the threshold voltage  $V_T$ . This makes low voltage and low power circuit designs possible using ICs.

Normally, aluminium is used as the gate electrode material. The polycrystalline silicon or polysilicon doped with phosphorous is conductive and it replaces the aluminium gate in recent monolithic fabrication processes. Since the polycrystalline silicon is grown over the silicon dioxide insulator material, it is commonly called polysilicon.

The polysilicon gate structure facilitates self-alignment of the gate with the source and drain. The gate electrode is formed earlier than the source and drain diffusions in the fabrication process. This is followed by  $N^+$  dopant diffusions in the source and drain regions. The process of self-alignment avoids any masking errors and eliminates any additional capacitance.

This structure has the advantage that the isolation island is not required because the drain terminal in an NMOS device is held positive with respect to the source that is tied to the substrate and the current flows only along the channel between the drain D and the source S.

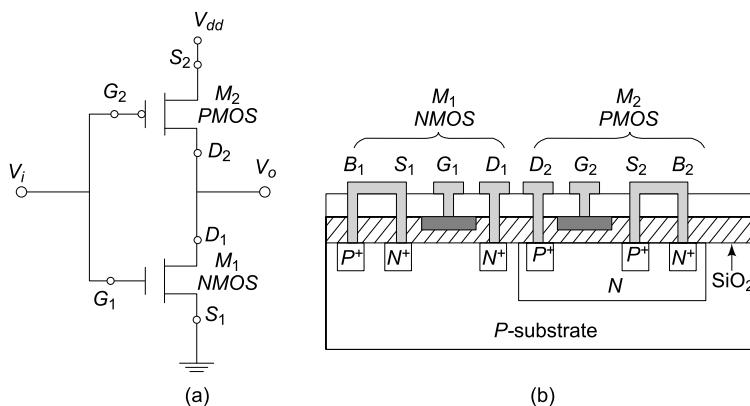
In BJT, the isolation diffusion occupies a large part of chip area. It is possible to get a higher packaging density with the MOSFET technology, which is 20 times more than that of BJT IC.

Silicon Nitride ( $\text{Si}_3\text{N}_4$ ) has excellent masking properties as compared to  $\text{SiO}_2$ . Therefore, an  $\text{Si}_3\text{N}_4$  layer is sandwiched between two  $\text{SiO}_2$  layers. This prevents the impurities from penetrating through the  $\text{SiO}_2$  layer. This structure also reduces the threshold voltage of the transistor, thus making it possible to operate at low voltage levels.

### 1.12.3 Complementary MOSFET (CMOS)

The NMOS and PMOS enhancement devices can be fabricated on the same silicon chip. These devices are called complementary MOSFETs and are abbreviated as CMOS. The four important CMOS process technologies are (i)  $N$ -well process, (ii)  $P$ -well process, (iii) Twin-tub process, and (iv) Silicon-on-Insulator (SoI) process.

In the  $N$ -well process, an  $N$ -type well or tub is diffused in the  $P$ -type substrate. The PMOS transistor  $M_2$  is fabricated within this well. The  $N$ -well region acts as the substrate for the PMOS transistor. Two additional steps are therefore required in the fabrication of PMOS transistor  $M_2$  in comparison with the NMOS transistor  $M_1$ . The additional processing steps are the formation of  $N$ -region and the ion-implantation step of  $P$ -type source and drain regions. A typical CMOS inverter circuit and the cross-sectional view of the  $N$ -well CMOS structure is shown in Fig. 1.34(a) and (b) respectively.



**Fig.1.34** (a) CMOS inverter circuit (b) Cross-sectional view of CMOS IC

The *P*-well processes were the commonly used forms of CMOS fabrication and the process steps are similar to *N*-well process except that the *P*-well diffusions are formed for fabricating NMOS devices. The *P*-well processes are preferred in situations where the characteristics of PMOS and NMOS devices are to be more balanced.

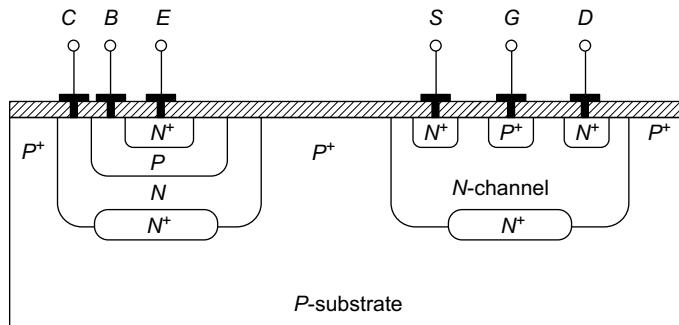
The twin-tub CMOS process employs both *N*-well and *P*-well diffusion regions for fabricating PMOS and NMOS devices respectively in the wells. Therefore, individual optimisation for the PMOS and NMOS through the control of  $V_T$  at other characteristics can be achieved.

The emerging process of SoI technology achieves closer packing of PMOS and NMOS transistors and it avoids such problems as latchup and lower parasitic capacitances. In this process, a thin layer of single crystal silicon is epitaxially grown over an insulator such as sapphire or magnesium aluminate spinel. The SoI can also be grown on  $SiO_2$  which in turn is grown on silicon material. This is a very popular structure in recent years.

#### 1.12.4 BiFET Devices

A specialised transistor device is required for applications involving low input bias current level, typically less than  $1nA$ . Since the bipolar transistor usually has low input impedance, it needs larger drive current. To overcome this drawback, the high input impedance characteristics of FET can be utilised. But the FET circuit normally has lower overall voltage gain than a similar BJT-based circuit. In such a situation, the circuit based on a combination of the two technologies, with FET amplifier circuit forming the input stage, and the BJT stage following it provides the designer with the inherent advantages of both the type of devices. Such a combination of Bipolar Junction Transistor and Field Effect Transistor is called a BiFET device. This BiFET device provides very high input impedance as well as high voltage gain of the order of  $10^3$ .

The fabrication of this device generally requires the addition of one or more masking steps to the basic fabrication process of integrated circuits. A typical structural arrangement of an *NPN* transistor and a JFET is shown in Fig. 1.35.



**Fig. 1.35** Structural arrangement of a JFET and BJT Structure

### 1.13 THIN-AND THICK-FILM TECHNOLOGY

Film ICs are broadly classified as thick film and thin film circuits. Thin films are the ones whose thickness vary from 50 to 20000 Å and the thick films have thickness that vary between 125000 and 625000 Å. However, the thickness of the film is not a critical tool for classifying, but the technology for fabricating the film classifies whether the film is thin film or thick film.

Only passive components like resistors and capacitors can be fabricated using film technology. Conventional film circuits are made by depositing film capacitors and resistors on a non-conducting substrate like glass or ceramic, and pre-fabricated active components are added to the film structure.

### 1.13.1 Thin-Film Fabrication

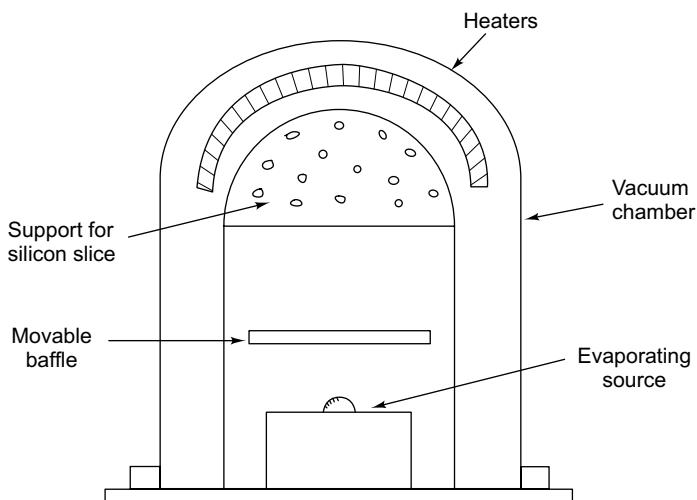
Thin films provide greater precision in component values. Thin film deposition can be done using any of the following methods.

- (i) Vacuum evaporation
- (ii) Plating technique
- (iii) Sputtering
- (iv) Screening

*Vacuum evaporation* technique has already been discussed in Sections 1.2.7 and 1.3.8. The technique is same as depositing thin metallic layer for interconnections.

Two types of plating techniques are widely in use, viz. *electroplating* and *electroless plating*. Electroplating is a process of coating an object with one or more layers of metals. In thin film fabrication, the substrate (acting as cathode) and the metal (acting as anode) are dipped in an electrolytic solution. When a proper voltage is connected across the substrate and the metal, the metal ions from the anode get deposited on the substrate. Electroless plating involves reducing a metal ion in a solution to free metal and depositing the same as a coating over the substrate without the use of an electric current.

*Sputtering* uses a system that is identical to that used for vacuum evaporation. The process of sputtering is carried out at a very low pressure. The source material to be deposited on the substrate is subjected to heavy bombardment by the ions of a heavy inert gas, viz. argon. These ions are accelerated by making the source material as the cathode of the dc glow discharge. The atoms are given out from the cathode, they migrate away from the cathode through a low pressure inert gas and finally land on the substrate. The high energy possessed by the particles, while landing on the substrate results in a uniform coating over the substrate with good crystal structure and adhesion. The main parts of a sputtering system are shown in Fig. 1.36.



**Fig. 1.36** Sputtering apparatus

A dc potential of about 3kV is applied between the cathode and the anode, which produces a glow discharge from the cathode that fills the inter-electrode space completely.

The *screening* process uses screen from very fine silk threads and mounted on aluminium frames. The screen is coated with a photo-sensitive emulsion and a mask of desired pattern is kept on it. Then the screen is exposed to light and developed. The screen becomes clear wherever thin film is to be deposited on the substrate and blocked by the photoresist elsewhere. The screen is then placed on the substrate and the components are deposited by driving a squeegee across the patterned screen at a constant rate. The squeegee forces the metal in the paste form through the openings on the screen. The deposited film is developed by firing it in a furnace where the temperature varies from 500 to 1000°C. The firing process vapourises the organic binders in the film and the remaining material fuses with the substrate.

The following are the major advantages of thin film circuits.

- (i) Good high frequency package density
- (ii) High component package density
- (iii) Resistors can be trimmed to precision
- (iv) Simple processing techniques

The thin film hybrid circuits are used in microwave ICs. Since precision resistors can be fabricated, these ICs are more suitable for ladder type D/A converters.

### 1.13.2 Thick-Film Fabrication

Thick film technology can be used to fabricate high density circuits containing resistors, conductors and capacitors at low cost. Active components can be added to form a fully functional hybrid circuit. Thick film circuits are finding a wide range of applications in areas where size and high-frequency requirements are considered important.

The technique used for depositing thick films over substrate involves (i) Screen printing and (ii) Substrate firing. The screen printing and the substrate firing processes are essentially the same as that of thin film deposition except that the screen used for thick film deposition is woven from stainless steel wires. The processing equipment for thick film circuits is relatively inexpensive and easy to use. Thin film technology provides greater precision in manufacturing but is more costly than thick film technology.

The following are the advantages of thick film hybrid circuits.

- (i) Low fabrication cost
- (ii) Good high frequency response
- (iii) Very low tolerance because of trimming
- (iv) Highly stable and reliable over a long run
- (v) Simple fabrication steps

The thick film circuits are used in automobile electronic circuits, digital watches and electronic toys and also in telecommunication circuits and computers.

## 1.14 RECENT TRENDS IN IC TECHNOLOGY

Process technology has progressed, and increasingly more complex chips are constantly increasing. For high speed and low noise applications, bipolar technology is preferred. Since the heat dissipation in bipolar circuits is comparatively large, elaborate heat dissipation capabilities are required. The MOS technology is becoming popular due to the high component density that can be achieved. Originally, PMOS devices were used but now NMOS technology is predominant due to high-speed performance.

The CMOS technology leads the NMOS with its extremely low static power dissipation. The feature size of the devices is also decreasing rapidly. In 1990s the minimum feature size for CMOS was 0.5  $\mu\text{m}$ , which reduced to 0.12  $\mu\text{m}$  in the year 2002 and it is predicted that 35nm devices will be available

for production by 2010. Gallium Arsenide (GaAs) technology is also advancing and this semiconductor material is found suitable for military and aerospace applications. They exhibit better performance characteristics than silicon, due to its higher carrier mobility.

The electron-beam photolithographic techniques lost its place due to increasingly lower feature sizes of the devices and X-rays are in use exclusively. New techniques such as Extreme Ultraviolet (EUV) lithography and electron beam lithography such as Scattering with Angular Limitation Projection Electron-Beam Lithography (SCALPEL) are being used for sub-micron size devices. The interconnections inside the chip start demanding more attention and research. They move from aluminium to copper, and optical interconnections may soon arrive.

The IC design engineers develop and use advanced Electronic Design Automation (EDA) tools that can aid in the fabrication of ICs. Such Computer Aided Design (CAD) tools are being used for the full flow of IC fabrication processes, from high level synthesis of system, logic synthesis, circuit optimisation, layout simulation, design verifications and to final testing.

An emerging technology is the BiCMOS which makes use of the advantages of both bipolar and CMOS devices on the same chip. These devices are capable of driving much higher loads, faster as compared to CMOS, at the cost of higher fabrication costs. The silicon-on-insulation technology enables easy integration of analog and digital circuits in the form of *mixed signal circuits*, using a novel substrate technology. It shows better performance characteristics against cross-talk. The integrated circuit technology has made possible the evolution of low-power displays and faster and denser memory packages.

Packaging technology has improved greatly from the earlier Dual-in-line-packages (DIP) for ICs with number of pins less than 64. Pin-through-hole (PTH), surface-mounted technology (SMT), Pin-Grid Array (PGA) packages with higher pin count and better power dissipation characteristics, Ball-Grid Arrays (BGA) to reduce parasitics for higher performance chips, Quad-Flat Packs (QFP) with very high pin counts (up to 500) are becoming popular in recent years. Multi-Chip Modules (MCM) are being fabricated for very high performance requirements with multiple chips assembled on a common substrate placed in a single package. This arrangement makes the critical interconnections among the chips possible within the package.

## SUMMARY

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- ❑ Integrated circuit is miniaturised solid-state devices and components fabricated on a single crystal of silicon.
- ❑ An IC has several advantages, such as improved performance, reliability and ruggedness, low power operation and lower cost.
- ❑ ICs can be classified into SSI, MSI, LSI, VLSI, ULSI and GSI based on device density, and analog and digital based on the types of signals they process.
- ❑ The basic processes in monolithic IC fabrication are
  - Wafer preparation
  - Epitaxial growth
  - Oxidation
  - Photolithography
  - Diffusion
  - Metallisation
  - Circuit probing
  - Mounting and packaging and
  - Encapsulation
- ❑ Various isolation process techniques involved in IC fabrication are PN-junction and dielectric isolation techniques.
- ❑ The typical fabrication processes also include Schottky barrier devices.
- ❑ Resistor fabrication in ICs are in the epitaxial region, base region and by the process of thin film technology.

- Generation of capacitors of value 0.3 to 0.8 nF/mm<sup>2</sup> are possible in IC Technology.
- FET devices occupy less area and consume low power. Fabrication of BJT and FET devices, use of silicon nitride for efficient masking, low threshold voltage operation, fabrication of NMOS and PMOS devices on the same chip and BiFET devices with very high input impedance and high voltage gain of the order of 10<sup>3</sup> are possible.
- A glimpse into the recent IC technology trends show
  - The CMOS technology leading the NMOS with its extremely low static power dissipation.
  - The feature size of the devices decreasing rapidly, with 0.5 μm in 1990s, 0.12 μm in the year 2002 and it is presently 35nm devices that are available for production in 2010.
  - Gallium Arsenide (GaAs) technology exhibiting better performance characteristics than silicon, due to its higher carrier mobility.
  - The electron-beam photolithographic techniques losing its place due to increasingly lower feature sizes of the devices.
  - New techniques such as Extreme Ultraviolet (EUV) lithography and electron beam lithography such as SCattering with Angular Limitation Projection Electron-Beam Lithography (SCALPEL) being used for sub-micron size devices.
  - The interconnections inside the chip demanding more attention and research, which move from aluminium to copper, and optical interconnections may soon arrive.
  - IC design engineers developing and using advanced Electronic Design Automation (EDA) tools in the fabrication of ICs and dealing with the full IC fabrication.
  - BiCMOS making use of the advantages of both bipolar and CMOS devices on the same chip.
  - Silicon-on-insulation technology enabling easy integration of analog and digital circuits called mixed signal circuits.
  - Improved packaging technology.
  - Transition from Pin-Through-Hole (PTH), Pin-Grid Array (PGA) packages, Ball-Grid Arrays (BGA), Quad-Flat Packs (QFP) and to Multi-Chip Modules (MCM)

## REVIEW QUESTIONS

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1. What is meant by an Integrated Circuit? Why is it preferred over discrete circuits?
2. What are the advantages of an IC over discrete components?
3. List the limitations of ICs.
4. Classify the ICs in terms of function, device and technology.
5. Compare the features of monolithic and hybrid technologies.
6. What are the dimensions of a typical integrated circuit?
7. What are the different types of packaging of ICs?
8. List the steps involved in the manufacturing process of an IC.
9. What is meant by an epitaxial layer?
10. What is the difference between epitaxial and crystal growing techniques?
11. Explain the process of epitaxial growth in the fabrication of ICs.
12. Why is an oxide layer grown before diffusion? Explain the purpose served by SiO<sub>2</sub> layer during different steps of fabrication.
13. What is doping? Explain its use in brief.
14. What are the normally used dopants for N and P type diffusions?
15. Define isolation. What are the isolation techniques normally used? Explain.
16. Explain the following processes in the monolithic IC technology. (i) Epitaxial growth, (ii) Isolation by diffusion.
17. Explain the process of diffusion.
18. Explain the P-type base diffusion process in the monolithic IC transistor fabrication.
19. What is meant by photolithography in IC fabrication and how is it carried out?
20. Why is prebaking of silicon wafer required in the photolithography process?
21. Why is the negative photoresist called so?
22. What is a positive photoresist? Compare it with a negative photoresist.
23. What are the methods of metal deposition process? Explain vacuum deposition process.

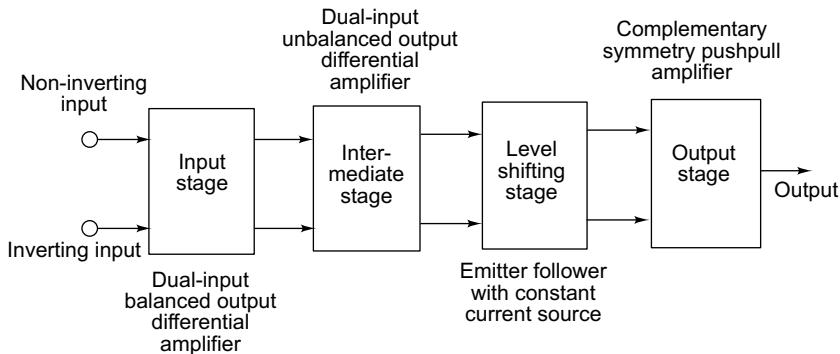
24. Describe with proper diagrams, the steps involved in the fabrication of an IC transistor.
25. Describe briefly the process of buried layer diffusion.
26. Explain why buried layer is needed in the collector region.
27. Define ohmic contact. Why is it important?
28. How is electrical isolation achieved among the different components fabricated in the IC? Explain.
29. Explain clearly the following terms related to the fabrication of monolithic integrated circuit:
  - a. Diffusion
  - b. Photolithography
  - c. Metallisation
30. Explain the different methods of fabrication of *PNP* transistor.
31. What are triple diffused *PNP* transistors?
32. Differentiate lateral *PNP* transistor from vertical *PNP* transistor.
33. Why are *NPN* transistors preferred over *PNP* transistors in ICs?
34. Why is passivation needed in an IC?
35. Why are the transistors modified as diodes in IC diode fabrication? Draw the different diode configurations obtainable from transistor structure. Which configuration is generally used? Why?
36. Draw the popular structures of monolithic diodes and explain them.
37. Describe the fabrication of Schottky barrier diode. What are its applications?
38. What are the advantages of Schottky barrier diode over a junction diode?
39. Explain the use of Schottky barrier diode in the structure of a Schottky transistor.
40. Write notes on integration of resistors and capacitors in an IC.
41. How are the integrated resistors obtained in monolithic integrated circuits?
42. What are the types of resistors fabricated in ICs? Comment on the choice of the type with respect to the resistance values.
43. Define sheet resistance. Comment on its unit.
44. How are capacitors fabricated in ICs?
45. What are the two types of capacitors that can be fabricated in an IC?
46. Draw the cross-sectional view of a junction capacitor and explain the processing steps.
47. Draw the cross-section of an *N*-channel MOSFET.
48. Draw the cross-section of a CMOS transistor. Explain the fabrication steps involved.
49. What is polysilicon? Why is it called so?
50. Describe briefly the use of polysilicon as a gate material.
51. Draw the cross-sectional view of a thin film capacitor and explain the processing steps. Comment on the factors determining the capacitance values.
52. Explain why inductors are difficult to be fabricated in ICs.
53. What are the metals normally used for metallisation?
54. Explain the steps involved in aluminium metallisation.
55. What are the fabrication constraints in monolithic IC technology?
56. Draw a typical circuit using transistors and resistors, and explain the fabrication steps for the same with necessary diagrams.
57. Write notes on BiFET technology. What are its main advantages?
58. What are the characteristics of thin film technology?
59. Describe thin film technology with relevant diagrams.
60. Explain the various techniques used in fabricating thin film and thick film circuits.
61. Describe briefly the steps involved in the fabrication of MOS ICs with suitable diagrams.
62. What are SoI and MCM?
63. Describe the current status of IC technology.
64. Define the terms (a) Sputtering, (b) Multiemitter transistor, (c) Pinched resistor, and (d) Oxidation
65. Given the sheet resistance of *N*-type diffusion is  $100 \Omega/\text{square}$ . Design a  $1 \text{k}\Omega$  diffused resistor.
66. Given the sheet resistance of polysilicon layer as  $20 \Omega/\text{square}$ , design a  $2 \text{k}\Omega$  resistor.

# Circuit Configurations for Linear ICs

2

## 2.1 INTRODUCTION

The integrated circuit technology makes it possible to realise a large number of virtually identical transistors and the device characteristics can be matched to within 1% of compatibility or less. Such an ability to build devices with nearly identical characteristics has led to the development of special circuit techniques for use in the operational amplifier (abbreviated *op-amp*), which is a fundamental building block of analog circuit design. The op-amp is a direct-coupled high-gain amplifier to which the feedback is externally connected to control its overall response characteristics. As it is mainly used to perform many linear operations as well as some non-linear functions, it is often called the *analog* or *linear integrated circuit*. The name *operational amplifier* comes from the application of this type of amplifier for specific electronic circuit functions or operations such as summation, scaling, differentiation and integration, and in analog computers.



**Fig. 2.1** Basic block diagram of operational amplifiers

Figure 2.1 shows the general block diagram of a typical op-amp. The major blocks are differential amplifiers, intermediate stages of differential, or dual input and single output amplifiers, dc level shift circuits and output stages. The operational amplifier is basically a differential amplifier and its function is to amplify the difference between the two input signals. The dc current source is a fundamental circuit component used to provide bias to the BJT and MOS op-amp circuits to improve their performance by providing a high voltage gain at low supply voltages. The circuits that can yield a precise voltage or current, which is independent of external influences, such as power supply and temperature variations are called *voltage references* and *current references*. The dual circuit of the current source, namely, the voltage source, voltage references and bandgap references are used to reduce supply sensitivity. This chapter explores the

current mirror and current sources, voltage sources and voltage references, bandgap voltage references and the differential amplifiers using BJT and FET devices with passive and active loads.

This chapter also provides a transition between the integrated circuit building blocks and the monolithic integrated circuits such as operational amplifiers. The specific and more detailed study of the stages of the op-amp will be made in Chapter 3.

## 2.2 CURRENT SOURCES

A current mirror is a circuit whose output current is a replica of the current sent at its input terminal. An ideal constant current source is an electric circuit that supplies a constant current to the load that is independent of the voltage across the load. In other words, the current is maintained constant irrespective of load conditions. The current mirrors are used for designing floating current sources also.

The constant current sources are widely used in analog integrated circuits as biasing elements and load devices for amplifier stages. These circuits make use of the fact that when the transistor operates in the active region of operation, the collector current will be relatively independent of the collector voltage. The current mirrors are more economical than resistors in terms of the die area required to provide bias currents of very small values for the circuits used in op-amps.

The large signal current characteristics of an ideal current source are shown in Fig. 2.2, compared against its practical characteristics. The most important characteristic of the current source is the variation in the current delivered by the current source with change in voltage at the output terminal. The output current of the current source increases slightly with respect to increase in voltage within the voltage compliance range. The small signal output resistance or the *dynamic output resistance* of the current source denotes this feature of the current source. The slope of the curve shown in Fig. 2.2 in the voltage compliance range is given by

$$\text{Slope} = \frac{\Delta I_o}{\Delta V_o} = g_m = \frac{1}{r_o}$$

where  $g_m$  is the dynamic output conductance and  $r_o$  is the *small-signal* or *dynamic output resistance* of the current source. The values of  $g_m$  and  $r_o$  for an ideal current source are

$$g_m = 0 \text{ and } r_o = \infty$$

For a basic current source, we can have

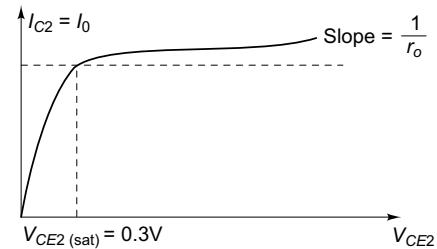
$$g_m = \frac{\Delta I_o}{\Delta V_o} = \frac{I_o}{V_A} = \frac{1}{r_o}$$

where  $V_A$  is the Early voltage whose typical value is in the range of 50 to 100, corresponding to  $r_o$  of range 50 k $\Omega$  to 100 k $\Omega$  for  $I_C = 1$  mA.

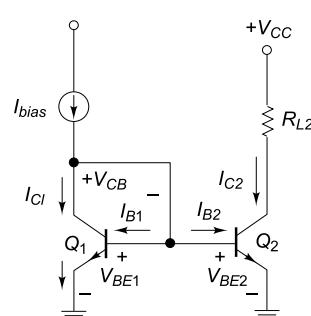
The term *reference* is used since the current and voltage values have more precision and better stability than that commonly obtained from a source.

### 2.2.1 Current Mirror

Figure 2.3 shows the circuit arrangement of a current mirror. The transistors  $Q_1$  and  $Q_2$  are assumed identical. The bases of the



**Fig. 2.2** Ideal output current characteristics of a current source



**Fig. 2.3** Current mirror circuit

transistors are tied together and the emitters are grounded. Therefore, the two transistors have exactly the same base-to-emitter voltages, i.e.  $V_{BE1} = V_{BE2}$ .

It can be observed that  $Q_1$  is a diode-connected transistor, with its collector shorted to base, such that  $V_{CB} = 0$ . When a current  $I_{C1}$  is forced to pass-through in the direction shown,  $Q_1$  is biased ON and since  $V_{CB} = 0$ , the transistor  $Q_1$  is operating in the active region.

The voltages  $V_{BE1}$  and  $V_{BE2}$  being equal,  $Q_2$  will also be in the active region and the collector currents of the two transistors will be approximately equal, so that  $I_{C1} = I_{C2}$ . Hence, the circuit shown in Fig. 2.3 is called as a *current mirror*. The current flowing through the left part of the circuit produces a mirror image of current in the right side. This principle forms the basis of most of the current source circuits and the active loads using current source circuits.

## 2.2.2 Basic Current Source Circuit

Figure 2.4 shows the simplest form of a constant current source circuit. The transistor  $Q_1$  is diode-connected with collector shorted to base. Therefore, the collector-base junction is maintained at zero bias, and the transistor operates in the active mode of operation. As indicated in the previous section, we assume identical transistors, and we also neglect the junction leakage currents. Collector of transistor  $Q_1$  is connected to  $+V_{CC}$  through a resistance  $R$ , and the collector resistance of  $Q_1$  is assumed infinite.

We can understand from Fig. 2.4 that the base-emitter voltages  $V_{BE1}$  and  $V_{BE2}$  of the two transistors are equal. Hence, their collector currents are also equal.

That is,

$$I_{C1} = I_{C2}$$

From Fig. 2.4,

$$I_{ref} = I_{C1} + I_{B1} + I_{B2}$$

Assuming  $I_{C1} = I_{C2} = I_C$  and  $I_{B1} = I_{B2}$

$$I_{ref} = I_C + 2I_B$$

Since  $\frac{I_C}{I_B} = \beta$ ,

$$I_{ref} = I_C + 2\frac{I_C}{\beta} = I_C \left(1 + \frac{2}{\beta}\right)$$

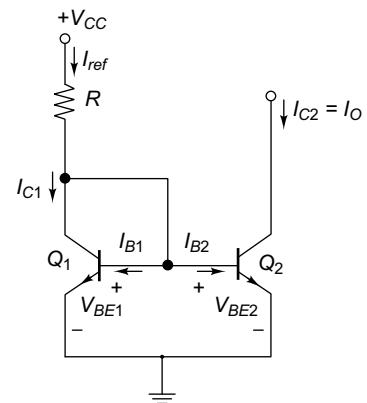
When the current gain  $\beta$  is large with a typical value of 100,

$$I_{C2} = I_o \cong I_{ref} = \frac{V_{CC} - V_{BE(ON)}}{R}$$

As a result, we can write  $I_C = I_{C1} = I_{C2} = \frac{I_{ref}}{\left(1 + \frac{2}{\beta}\right)} = \frac{\beta}{\beta + 2} \left( \frac{V_{CC} - V_{BE(ON)}}{R} \right)$  (2.1)

where

$$I_{ref} = \frac{V_{CC} - V_{BE(ON)}}{R}$$



**Fig. 2.4** Simple current source

Thus, it can be seen that for identical transistors  $Q_1$  and  $Q_2$ , the output current  $I_{C2}$  equals  $I_{ref}$ . If the devices  $Q_1$  and  $Q_2$  are not identical and have different emitter areas, the current  $I_S$  describing the transfer characteristic of the transistor in the active region can be different. The currents  $I_{C1}$  and  $I_{C2}$  will then have a constant ratio, as decided by the emitter ratios. Therefore, any desired output current  $I_{C2}$  can be obtained from the current source. For currents of ratio more than 5, large die area is required.

Figure 2.5(a) shows the output characteristics of a practical constant current source compared with that of an ideal current source.

The small signal output resistance of the current source represented by  $r_o$  is shown in Fig. 2.5(b) for an ideal and actual constant current source. The slope  $g_m$  represents the dynamic output conductance and  $r_o$  is the dynamic output resistance. For an ideal current source  $g_m = 0$  and  $r_o = \infty$ .

Therefore, for the constant current source, we have

$$g_m = \frac{1}{r_o} = \frac{dI_o}{dV_o} = \frac{1}{r_{ce}}$$

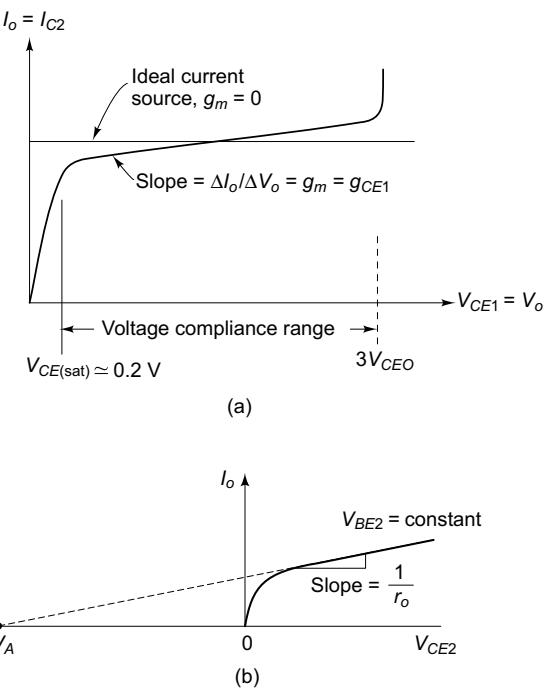
Figure 2.5(b) shows the characteristics of  $I_o$  versus  $V_{CE2}$  for a constant base-to-emitter voltage. The ratio of the load current  $I_o$  to the reference current  $I_{ref}$ , considering the Early effect is given by

$$\frac{I_o}{I_{ref}} = \frac{1}{\left(1 + \frac{2}{\beta}\right)} \times \frac{\left(1 + \frac{V_{CE2}}{V_A}\right)}{\left(1 + \frac{V_{CE1}}{V_A}\right)}$$

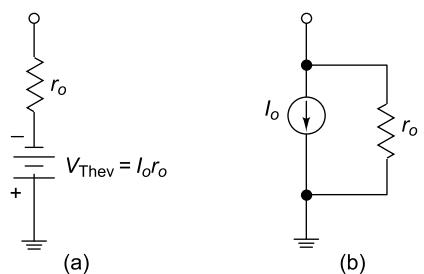
where the term  $\left(1 + \frac{2}{\beta}\right)$  stands for the finite gain.

The Thevenin's and Norton's equivalent circuit diagrams of the constant current source are shown in Figs. 2.6(a) and (b) respectively. The Thevenin's voltage remains a constant value independent of the current  $I_o$ .

$$V_{Th} = I_o r_o = I_{C2} r_{o2} = I_{C2} \frac{V_A}{I_{C2}} = V_A$$



**Fig. 2.5** (a) Current source output characteristics  
(b) Constant current source output characteristics showing Early voltage



**Fig. 2.6** Current source:  
(a) Thevenin's equivalent circuit  
(b) Norton's equivalent circuit representations

where  $r_{o2}$  is the small signal output resistance of the transistor. Therefore, the open circuit voltage is equal to  $V_A$ , the Early voltage for the simple current source.

### Example 2.1

Design a current source of Fig. 2.4 to provide an output current of  $100 \mu A$ . Assume  $V_{CC} = 5 V$ ,  $V_{BE(ON)} = 0.6 V$ ,  $\beta = 150$  and Early voltage  $V_A \approx \infty$ .

**Solution** The reference current is given by

$$I_{ref} = I_o \left(1 + \frac{2}{\beta}\right) = 100 \times 10^{-6} \left(1 + \frac{2}{150}\right) = 101.33 \mu A$$

The resistance  $R$  can be found from the equation

$$R = \frac{V_{CC} - V_{BE}}{I_{ref}} = \frac{5 - 0.6}{101.33 \times 10^{-6}} = 43.42 \text{ k}\Omega$$

It can be noted that the reference current and the load current are within 1.5% of each other in the two-transistor current source. Therefore, for most of the applications, we can assume  $I_{ref} \approx I_o$ .

### Example 2.2

Assuming identical transistors with  $V_{BE} = 0.7 V$ , determine the voltage  $V_o$  for the circuit shown in Fig. 2.7.

**Solution**

$$I_{ref} = \frac{V_{CC} - V_{BE}}{R_{C1}} = \frac{12 - 0.7}{1 \times 10^3} = 11.3 \text{ mA}$$

With  $I_o = I_{ref}$  (current mirror), the voltage at  $V_o$  is

$$V_o = V_{CC} - R_{C2} I_o = 12 - 330 \times 11.3 \times 10^{-3} = 8.271 \text{ V}$$

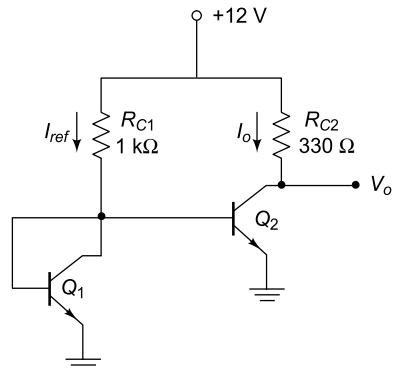


Fig. 2.7

### Example 2.3

Determine the output current  $I$  for the current source given in Fig. 2.8. Assume  $h_{FE}$  of the transistor is very high and  $V_{BE} = 0.6 V$ .

**Solution** Given  $h_{FE}$  is large,  $V_{BE} = 0.6 V$  and  $V_Z = 4.7 V$

Using KVL around emitter base loop of transistor through Zener diode with  $V_Z = 4.7 V$  and assuming negligible base current,

$$V_Z = V_{BE} + V_{RE}$$

$$4.7 = 0.6 + I \times 1 \times 10^3$$

$$\text{Therefore, } I = \frac{4.1}{1 \times 10^3} = 4.1 \text{ mA}$$

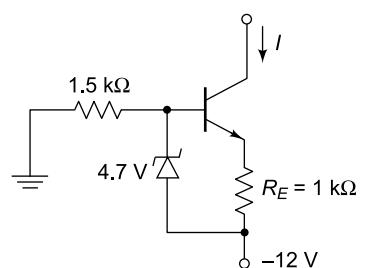


Fig. 2.8

### 2.2.3 Widlar Current Source

The operational amplifiers require very small input current. Therefore, the emitter-coupled pair of transistors at the input are needed to be biased at very low current, with the collector currents of the order of  $5\ \mu\text{A}$ . Realising such circuits using simple current sources are difficult. If we assume that the reference current is  $50\ \mu\text{A}$  and the emitter area ratio is  $1:10$  for  $Q_2:Q_1$ , then the circuit achieves an output current  $I_{C2}$  of  $5\ \mu\text{A}$ . Hence, a very large value of resistance must be connected with the power supply  $V_{CC}$  which will occupy a very large die area.

The Widlar current source is designed for current values of very low magnitude. This circuit shown in Fig. 2.9 employs moderate value of resistors. The transistors  $Q_1$  and  $Q_2$  operate at different values of  $V_{BE}$  due to the presence of resistor  $R_2$  in the emitter circuit of  $Q_2$ . Due to the resistor  $R_2$ , it can be observed that,

$$V_{BE2} < V_{BE1} \text{ and hence, } I_{C2} < I_{C1}$$

The reference current  $I_{ref}$  is determined by  $Q_1$ ,  $R_1$  and  $V_{CC}$ . The resistance  $R_2$  and  $I_{ref}$  decide the value of  $I_{C2}$ . Applying Kirchhoff's voltage law for the emitter-base loop of  $Q_1$  and  $Q_2$ , and assuming the Early voltage  $V_A$  is infinite and the base currents  $I_{B1}$  and  $I_{B2}$  are negligible due to high  $\beta$  of the transistors, we have

$$V_{BE1} - V_{BE2} - I_{C2}R_2 = 0$$

That is,

$$V_T \ln \frac{I_{C1}}{I_{S1}} - V_T \ln \frac{I_{C2}}{I_{S2}} - I_{C2}R_2 = 0$$

where  $I_{S1}$  and  $I_{S2}$  are the reverse saturation currents of transistors  $Q_1$  and  $Q_2$  respectively. The  $I_{S1}$  and  $I_{S2}$  are assumed constant in the forward active region.

Assuming  $I_{S1} = I_{S2}$ , the above equation can be reduced to

$$V_T \ln \left( \frac{I_{C1}}{I_{C2}} \right) = I_{C2}R_2$$

Therefore,

$$R_2 = \frac{V_T}{I_{C2}} \ln \left( \frac{I_{C1}}{I_{C2}} \right) \quad (2.2)$$

For practical design purposes, the values of  $I_{C1}$  and  $I_{C2}$  are usually known, and the value of  $R_2$  is calculated to achieve the desired value of  $I_{C2}$ .

Analysing the circuit of Fig. 2.9 for non-negligible base currents, we have

$$I_{C1} = \alpha I_{S1} e^{V_{BE1}/V_T}$$

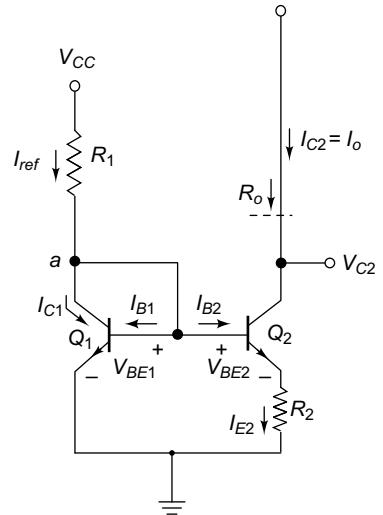
and

$$I_{C2} = \alpha I_{S2} e^{V_{BE2}/V_T}$$

Using the above two equations,  $\frac{I_{C1}}{I_{C2}} = e^{(V_{BE1} - V_{BE2})/V_T}$ , since  $I_{S1} = I_{S2}$  for matched transistors.

Taking natural logarithm for the above equation, we get

$$V_{BE1} = V_{BE2} + V_T \ln \left( \frac{I_{C1}}{I_{C2}} \right)$$



**Fig. 2.9** Widlar current source

are negligible due to high  $\beta$  of the

From Fig. 2.9, we observe that

$$V_{BE1} = V_{BE2} + (I_{B2} + I_{C2}) R_2$$

or,

$$V_{BE1} - V_{BE2} = \left( \frac{1}{\beta_2} + 1 \right) I_{C2} R_2$$

Therefore,

$$R_2 = \frac{V_T}{\left( 1 + \frac{1}{\beta_2} \right) I_{C2}} \ln \frac{I_{C1}}{I_{C2}}$$

Writing Kirchhoff's current law at the node  $a$ , we get

$$\begin{aligned} I_{ref} &= I_{C1} + I_{B1} + I_{B2} \\ &= I_{C1} \left( 1 + \frac{1}{\beta_1} \right) + \frac{I_{C2}}{\beta_2} \end{aligned}$$

Assuming matched transistors,  $\beta_1 = \beta_2 = \beta$ . By *matched transistors*, we mean that their respective parameter values such as  $I_S$ ,  $\beta$ ,  $V_A$  etc. are the same.

For the Widlar current source, the output current  $I_o = I_{C2} \ll I_{C1}$ . Therefore, neglecting  $I_{C2}/\beta$  in the previous equation, we get

$$I_{ref} \approx I_{C1} \left( 1 + \frac{1}{\beta} \right)$$

and

$$I_{C1} = I_{ref} \left( \frac{\beta}{1 + \beta} \right)$$

We know that  $I_{ref} = \frac{V_{CC} - V_{BE1}}{R_l}$ . When  $\beta \gg 1$ ,  $I_o = I_{C2} = I_{ref}$ .

The output resistance of the Widlar current source is  $R_o = r_o \left( 1 + \frac{I_{C2} R_2}{V_T} \right)$ . Thus, the value of  $R_o$  is

much larger than  $r_o$ , and it depends on  $I_{C2} R_2$ , which is the dc voltage drop across  $R_2$ . Larger the drop across  $R_2$ , higher is the resistance  $R_o$ .

The ratio of the maximum to minimum value of collector current obtained by this method is around 10 and the fabrication procedures limit the ratio.

## Example 2.4

For the circuit in Fig. 2.9, assume  $V_{CC} = 20$  V,  $R_l = 19.3$  k $\Omega$  and  $V_{BE(ON)} = 0.7$  V. Find the value of  $R_2$  required to produce a current  $I_{C2}$  of  $5\mu A$ .

### Solution

$$I_{C1} = \frac{V_{CC} - V_{BE1}}{R_l} = \frac{20 - 0.7}{19.3 \times 10^3} = 1 \text{ mA}$$

$$R_2 = \frac{V_T}{\left( 1 + \frac{1}{\beta} \right) I_{C2}} \ln \frac{I_{C1}}{I_{C2}}$$

$$\approx \frac{V_T}{I_{C2}} \ln \frac{I_{C1}}{I_{C2}}, \text{ since } \left(1 + \frac{1}{\beta}\right) \approx 1$$

Therefore,  $R_2 = \frac{26 \times 10^{-3}}{5 \times 10^{-6}} \ln \frac{1 \times 10^{-3}}{5 \times 10^{-6}} = 27.55 \text{ k}\Omega$

### 2.2.4 Multiple Current Source

The diode-resistor combination of a simple current source or a current mirror which establishes current  $I_{ref}$  can be employed for supplying more than a single load or to bias multiple amplifier stages using one reference current. Such a circuit is called a *current repeater* or a *multiple current source*. The circuit of a multiple current source is shown in Fig. 2.10. Here, the base terminals of the BJTs are extended through the transistors for simplifying the drawing. The reference current  $I_{ref}$  is supplied by the diode-connected transistor

$Q$  for establishing the emitter-base reference voltage  $V_{EB}$ . The  $V_{EB}$  thus generated is used for biasing the transistors  $Q_1$  through  $Q_3$ . The transistors  $Q_1$ ,  $Q_2$  and  $Q_3$  can have different emitter areas in comparison to the reference transistor. Different values of  $I_{C1}$ ,  $I_{C2}$  and  $I_{C3}$  can be obtained by correspondingly scaling the emitter areas of  $Q_1$ ,  $Q_2$  and  $Q_3$ .

In Fig. 2.10, assuming equal emitter areas, the collector currents of the various transistors are given by  $I_{C1} = I_{C2} = I_{C3} \equiv I_{ref}$

At the collector node  $a$  of transistor  $Q$ ,  $I_{ref} = I_B + I_C + NI_B$  where  $N$  is the number of multiple current sources. If there are three identical transistors  $Q_1$ ,  $Q_2$  and  $Q_3$ , we have  $N = 3$ . Therefore,

$$I_{ref} = I_C + (1 + 3)I_B = I_C + \left(\frac{1 + 3}{\beta}\right)I_C$$

When  $N$  number of such multiple current sources are required, we have

$$\begin{aligned} I_{ref} &= I_C + \left(\frac{1 + N}{\beta}\right)I_C \\ &= I_C \left(1 + \left(\frac{1 + N}{\beta}\right)\right) \end{aligned}$$

Therefore,  $I_C = I_{ref} \times \frac{\beta}{\beta + N + 1}$ .

### Example 2.5

For the circuit shown in Fig. 2.10, assume  $\beta = 100$ ,  $R = 20 \text{ k}\Omega$ ,  $V_{CC} = 5 \text{ V}$  and  $V_{BE} = 0.6 \text{ V}$ . Determine the values of  $I_{C1}$ ,  $I_{C2}$  and  $I_{C3}$ .

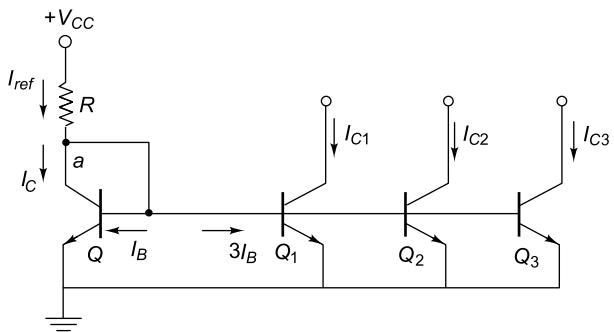


Fig. 2.10 Multiple current source

### Solution

$$I_{ref} = \frac{5 - 0.6}{20 \times 10^3} = 0.22 \text{ mA}$$

At node  $a$  shown in Fig. 2.10, we have

$$I_{ref} = I_C + 4I_B = I_C \left(1 + \frac{4}{\beta}\right)$$

Therefore,  $I_{C1} = I_{C2} = I_{C3} = I_{ref} \times \frac{\beta}{(\beta + N + 1)}$

$$= 0.22 \times 10^{-3} \left(\frac{100}{100 + 3 + 1}\right) = 0.212 \text{ mA}$$

### 2.2.5 Wilson Current Source

The Wilson current source shown in Fig. 2.11 is designed for achieving much higher resistances than the output resistance  $r_o$  of the simple current source. The circuit achieves a Thevenin's voltage much larger than the Early voltage. An additional transistor  $Q_3$  is connected to form a negative feedback path, which increases the output resistance. This configuration also achieves first-order cancellation of base currents and this makes the ratio of output current to the reference current less sensitive to  $\beta$ . An output current  $I_o = I_{ref}$  and the Wilson current source exhibits a very high output resistance.

The cancellation of finite base currents can be explained as follows:

Since  $V_{BE1} = V_{BE2}$ ,  $I_{C1} = I_{C2}$  and  $I_{B1} = I_{B2} = I_B$ . Assuming that  $I_{C2} = I_2$  and all base currents are equal to  $I_B$ , Fig. 2.11 gives

$$I_{ref} = I_{C1} + I_B \quad (2.3)$$

At node  $b$ ,  $I_{E3} = I_{C2} + 2I_B \quad (2.4)$

$$I_{E3} = I_{C3} + I_B \quad (2.5)$$

We know that for the transistor pair  $Q_1$  and  $Q_2$

$$I_{C1} = I_{C2}$$

Combining Eqs. (2.4) and (2.5), we get

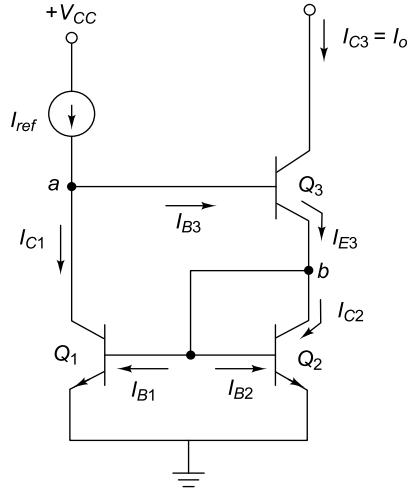
$$\begin{aligned} I_{C3} &= I_{E3} - I_B = I_{C2} + 2I_B - I_B = I_{C2} + I_B \\ &= I_{C1} + I_B \end{aligned} \quad (2.6)$$

From Eqs. (2.3) and (2.6), we get

$$I_{ref} = I_{C3}$$

Hence, the effect of finite base currents stands cancelled.

For the dc analysis of the circuit, assume  $V_A = \infty$  and identical transistors are employed. The emitter current  $I_{E3}$  of  $Q_3$  is the sum of the collector current  $I_{C2}$  of  $Q_2$  and the base currents of  $Q_1$  and  $Q_2$ .



**Fig. 2.11** Wilson current source

Therefore, we have

$$\begin{aligned} I_{E3} &= I_{C2} + 2I_B \\ &= I_{C2} + 2 \frac{I_{C2}}{\beta} = I_{C2} \left(1 + \frac{2}{\beta}\right) \end{aligned}$$

The collector current  $I_{C3}$  of  $Q_3$  is

$$\begin{aligned} I_{C3} &= \alpha I_{E3} \\ &= I_{C2} \left(1 + \frac{2}{\beta}\right) \left(\frac{\beta}{1+\beta}\right) \end{aligned}$$

where

$$\alpha = \frac{\beta}{1+\beta}$$

Rearranging, we get

$$I_{C2} = I_{C3} \left[ \frac{1}{\left(1 + \frac{2}{\beta}\right)\left(\frac{\beta}{1+\beta}\right)} \right] \quad (2.7)$$

From Eq. (2.3), we have

$$I_{C1} = I_{ref} - \frac{I_{C3}}{\beta} \quad (2.8)$$

For the current mirror formed by  $Q_1$  and  $Q_2$ , we have  $I_{C1} = I_{C2}$ .

Therefore, equating Eqs. (2.7) and (2.8), we get

$$I_{C3} = I_{ref} \left(1 - \frac{2}{\beta^2 + 2\beta + 2}\right)$$

Hence, it is observed that the output current  $I_{C3}$  and the reference current  $I_{ref}$  differ by a factor of  $\frac{2}{\beta^2 + 2\beta + 2}$  only, as against  $\frac{2}{\beta}$  obtainable with a simple constant current source. The difference between the two and three-transistor current-source circuits is the output resistance  $R_o$ . In the Wilson current source, the output resistance  $R_o$  looking into the collector of  $Q_3$  is  $R_o \approx \beta r_{o3}/2$  which is  $\beta/2$  times larger than that of either the two-transistor source or the basic three-transistor current source, and Thevenin's voltage of  $V_{Thev} \approx \beta V_A/2$ . In Wilson current source, the change in bias current  $I_o$  with a change in collector voltage is small.

The Widlar current source is useful for applications involving small output currents whereas the Wilson current source is preferable for achieving higher output resistance and lower sensitivity to transistor base currents.

## 2.3 CURRENT SOURCES INDEPENDENT OF SUPPLY VOLTAGE VARIATION

The simple current source of Fig. 2.4 has its output current decided by  $V_{CC}$  as shown in Eq. (2.1) and  $I_o$  varies directly proportional to the change in  $V_{CC}$ . One performance metric to define this aspect of the bias-circuit is the *fractional change in the output current that results from a given fractional change in supply voltage* denoted by  $S_{V_{CC}}^{I_o}$ .

For the simple current source, the *figure of merit* is unity, since

$$S_{V_{CC}}^{I_o} = \frac{\Delta I_o / I_o}{\Delta V_{CC} / V_{CC}} = \frac{V_{CC}}{I_o} \frac{\partial I_o}{\partial V_{CC}} \quad (2.9)$$

Therefore, using Eqn. (2.1),

$$\begin{aligned} S_{V_{CC}}^{I_o} &= \frac{V_{CC}}{I_o} \frac{\partial}{\partial V_{CC}} \left[ \frac{\beta}{\beta + 2} \times \frac{V_{CC} - V_{BE}}{R} \right] \\ &= \frac{V_{CC}}{I_o} \times \frac{1}{R} \\ &= \frac{V_{CC}}{R} \times \frac{R}{V_{CC} - V_{BE}} \approx 1 \end{aligned}$$

### 2.3.1 Widlar Current Source

The Widlar current source shown in Fig. 2.9 is proved efficient with better power supply insensitivity due to the presence of the emitter resistor  $R_2$ , that gives an approximate logarithmic dependence of output current on supply voltage. The dependence characteristics of the Widlar current source are indicated in Fig. 2.12 against a simple current source.

### 2.3.2 Power Supply Independent Bias Circuit

Figure 2.13 shows the circuit arrangement of a Widlar current source which has a greater degree of power supply voltage independence. This circuit consists of a Widlar current source combined with a standard current mirror. The current mirror formed by the *PNP* transistor forces the currents on the two sides of the reference to be equal, i.e.  $I_{C1} = I_{C2}$ .

As an example, consider the emitter area ratio of the Widlar source is 20. This condition is satisfied by choosing the operating point as defined by

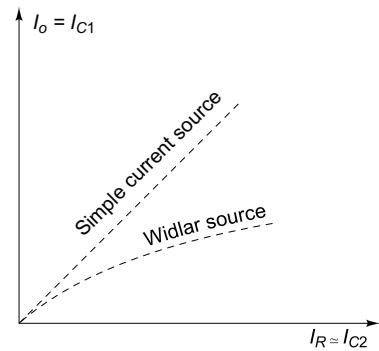
$$I_{C2} = \frac{V_T}{R_E} \ln 20 = \frac{0.0749V}{R_E}$$

This represents that a voltage of approximately 75 mV is developed across resistor  $R_E$  which is independent of the power supply voltages. Therefore, the resistor  $R_E$  can be chosen as per the requirement of the operating current.

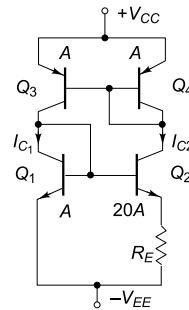
This circuit has the additional advantage of providing a wider range of current mirror values achieved by various emitter area ratios in the design of the circuit shown in Fig. 2.13.

A point of contention though, is that for practical values of  $I_{C1}$  and  $R_E$ , it is found that the output current  $I_{C1}$  is not adequately independent of changes in power supply.

The analog and mixed signal circuits demand much higher degree of stability against  $V_{CC}$ . This is achieved by making  $I_{C1}$  dependent on any voltage other than the supply voltage. For example, the current  $I_{C1}$  can be made to be dependent on the base-emitter junction voltage  $V_{BE}$ , thermal voltage  $V_T (= kT/q)$ , or the breakdown voltage of a reverse-biased emitter-base junction. However, the first two voltages are temperature dependent, and the third one has the disadvantage that a minimum power supply of 7 V



**Fig. 2.12** Comparison of the dependence of  $I_o$  on supply voltage for the simple and Widlar current sources



**Fig. 2.13** Power supply independent bias circuit

or 8V is required. This is necessary since the standard ICs contain *NPN* transistors with emitter-base breakdown voltages of around 6V. Further, the breakdown of such *PN* junction inflicts large amount of noise in the ICs.

### 2.3.3 Bipolar Transistor Current Sources using $V_{BE}$ and $V_T$ Based Reference

A bipolar transistor current source using  $V_{BE}$  based reference is shown in Fig. 2.14. This circuit structure is similar to that of a Wilson current source with the diode-connected transistor replaced with a resistor  $R_1$ .

Neglecting the base currents, the output current  $I_o = I_{E2} \approx I_{C2}$ , which is the current flowing through  $R_2$ . Resistor  $R_2$  has a voltage of one base-emitter drop across it, and the output current is made proportional to this base-emitter voltage  $V_{BE}$ . Then, neglecting base currents, we get

$$I_o = \frac{V_{BE1}}{R_2} = \frac{V_T}{R_2} \ln \frac{I_R}{I_{S_1}} \quad (2.10)$$

This circuit is also not fully guaranteed against supply voltage changes, due to the fact that the collector current of  $Q_1$  is proportional to  $V_{CC}$ , the base emitter voltage of  $Q_1$  can change slightly with power supply voltage variations. This poses problem for devices whose base currents are derived from a resistor connected to the supply terminal. Therefore, some improved circuit structures use the output current of the current source itself feedback as reference.

A current source employing thermal voltage  $V_T$  as a standard, that is almost completely independent of the supply voltage is shown in Fig. 2.15. For analysis, assuming that all the transistors are identical, and  $R_1 = R_3$  so that  $I_1 = I_3$  we have  $I_3$  and  $I_2$  related by

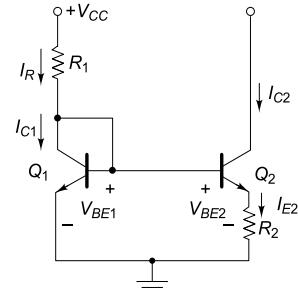
$$\frac{I_2}{I_3} = \exp\left(\frac{I_3 R_3}{V_T}\right)$$

As shown in Fig. 2.15, the ratio of  $I_5$  to  $I_6$  is set by the ratio of  $R_6$  to  $R_5$  using the relation  $\frac{I_5}{I_6} = \frac{R_6}{R_5}$ . Since the base currents are small compared to the collector and emitter currents, we can consider  $I_2 = I_5$  and  $I_3 = I_6$ .

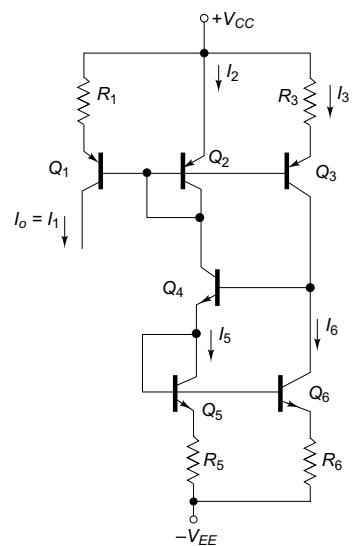
$$\text{Therefore, } \frac{I_2}{I_3} = \exp\left(\frac{I_3 R_3}{V_T}\right) = \frac{I_5}{I_6} = \frac{R_6}{R_5}$$

Upon solving Eq. (2.11) for  $I_3$ , we get

$$I_o = I_1 = I_3 = \frac{V_T}{R_3} \ln \frac{R_6}{R_5} \quad (2.12)$$



**Fig. 2.14** A current source independent of supply voltage



**Fig. 2.15** Current source employing thermal voltage  $V_T$  as a standard

Equation (2.12) shows that, the output current of the current source is independent of the supply voltage. To have an accurate current ratio  $I_5/I_6$ , the emitter areas of  $Q_5$  and  $Q_6$  should be scaled such that the two transistors will have equal current densities with equal  $V_{BE}$  drops.

Choosing a current ratio of  $I_5/I_6 = 2$ , so that the ratio  $R_6/R_5 = 2$  and using Eq. (2.12), we have

$$I_o = I_1 = \frac{V_T}{R_3} \ln 2 \quad (2.13)$$

To cite an example, considering that the desired current  $I_o = 1 \mu\text{A}$ , the value of  $R_3 = R_1$  is found to be

$$R_1 = R_3 = \frac{26\text{mV}}{1\mu\text{A}} \ln 2 = 17.3 \text{ k}\Omega$$

Thus, a very small current has been obtained using only a very moderate resistance value. It is possible to eliminate  $R_5$  and  $R_6$  from the circuit, if the active area of  $Q_5$  and  $Q_6$  are properly scaled. Then, the ratio  $I_5/I_6$  will be determined entirely by the transistor active area ratio as represented by  $I_5/I_6 = A_5/A_6$ . Then, the output current is given by

$$I_o = I_1 = I_3 = \frac{V_T}{R_1} \ln \frac{A_5}{A_6} \quad (2.14)$$

The above equation shows that, though the current source is independent of supply voltage, it requires a minimum value of supply voltage for its operation. The circuit is also characterised by a constant current output over a very wide range of supply voltages, and it exhibits an ability to operate with supply voltage as low as 1.6V and current levels of the order of  $\mu\text{A}$  with only moderate resistance values. These characteristics enable this type of current source very suitable for low power operational amplifier.

### 2.3.4 Temperature Dependence

The bias circuits discussed above are independent of power supply. However, they are temperature dependent, and the variation of the output current with respect to temperature expressed as the *fractional change in output current per degree centigrade of temperature variation* is called the *temperature coefficient*  $TC_F$ . It is expressed as

$$TC_F = \frac{1}{I_o} \times \frac{\partial I_o}{\partial T} \quad (2.15)$$

For the current source using  $V_{BE}$  as reference shown in Fig. 2.14 and using Eq. (2.10),

$$TC_F = \frac{1}{V_{BE_1}} \times \frac{\partial V_T}{\partial T} - \frac{1}{R_2} \frac{\partial R_2}{\partial T} \quad (2.16)$$

Equation (2.16) shows that the temperature dependence of  $I_o$  is related to the difference between the positive temperature coefficient of resistance and the negative temperature coefficient of the base-emitter junction. This makes the effective  $TC_F$  very large for the current source using  $V_{BE}$  as reference of Fig. 2.14.

The current source employing thermal voltage  $V_T$  as a standard is shown in Fig. 2.15. Similarly, the temperature coefficient  $TC_F$  of Eq. (2.13) can be obtained by using Eq. (2.15) as

$$TC_F = \frac{1}{V_T} \times \frac{\partial V_T}{\partial T} - \frac{1}{R_3} \frac{\partial R_3}{\partial T} \quad (2.17)$$

From Eq. (2.17), we can find that the circuit of Fig. 2.15 produces a much smaller temperature coefficient of the output current, because of the fact that, the fractional sensitivities of both  $V_T$  and the diffused resistor  $R_3$  are positive and tend to cancel each other.

To summarise the above, we find that, the reference circuits using  $V_{BE}$  and  $V_T$  have rather high value of temperature coefficient of output current, and out of the two reference circuits, the use of  $V_T$  is considerably better. This difficulty in reference circuits using  $V_{BE}$  and  $V_T$  can be overcome by using the Zener diode reference and the bandgap reference design approaches, which are usually termed *voltage references*.

## 2.4 FET CURRENT SOURCES

The Field-Effect Transistor ICs are biased with current sources in the same manner as for bipolar transistor ICs. The relationship between the reference and load currents for MOSFET and JFET current sources and their output impedance are discussed in this section.

### 2.4.1 Basic Two-transistor MOSFET Current Source

A basic two transistor NMOS current source is shown in Fig. 2.16. The drain and gate terminals of the enhancement-mode transistor  $M_1$  are interconnected. This biases the transistor  $M_1$  in the saturation region.

Assuming a simple MOS model with its *channel length modulation parameter*  $\lambda$  considered zero, the reference current is given by

$$I_{ref} = k_{n1}(V_{GS} - V_{Th1})^2 \quad (2.18)$$

where  $V_{GS}$  is the gate-to-source voltage of the transistor and  $V_{Th1}$  is the threshold voltage of the transistor and  $k_{n1}$  is the process transconductance parameter.

Solving for  $V_{GS}$  gives

$$V_{GS} = V_{Th1} + \sqrt{\frac{I_{ref}}{k_{n1}}} \quad (2.19)$$

The transistor  $M_2$  is always biased in the saturation region so that its drain current is independent of the drain-to-source voltage  $V_{DS}$ .

The load current is then given by

$$I_{D2} = I_o = k_{n2} \left[ \sqrt{\frac{I_{ref}}{k_{n1}}} + V_{Th1} - V_{Th2} \right]^2 \quad (2.20)$$

If the transistors  $M_1$  and  $M_2$  are identical, then  $V_{Th1} = V_{Th2}$  and  $k_{n1} = k_{n2}$ . Then, the current  $I_o$  becomes

$$I_o = I_{ref} \quad (2.21)$$

There is no gate current in MOSFETs  $M_1$  and  $M_2$ . Since the two transistors are matched, the load current  $I_o$  is identical to the reference current  $I_{ref}$ .

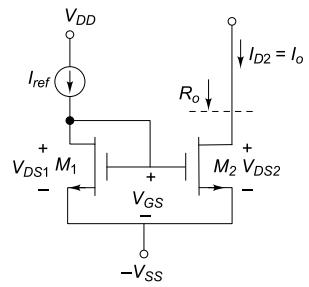
The stability of the load current against  $V_{DS}$  is an important design consideration in many applications. The load and reference currents of the two MOS devices can be expressed as given by

$$I_o = k_{n2}(V_{GS} - V_{Th2})^2 \quad (2.22)$$

and

$$I_{ref} = k_{n1}(V_{GS} - V_{Th1})^2 \quad (2.23)$$

Since the transistors  $M_1$  and  $M_2$  are fabricated on the same monolithic integrated circuit, all the physical parameters, such as  $V_{Th}$ ,  $\mu_n$ ,  $C_{ox}$  and  $\mu$  are essentially the same for both the devices.



**Fig. 2.16** Basic two-transistor MOSFET current source

Therefore, using Eqs. (2.22) and (2.23), we have the ratio of  $I_o$  to  $I_{ref}$  as given by

$$\frac{I_o}{I_{ref}} = \frac{(W/L)_2}{(W/L)_1} \quad (2.24)$$

where  $W/L$  is the width to length ratio of the transistor concerned.

Equation (2.24) shows that the ratio  $I_o/I_{ref}$  is a function of the aspect ratio of the transistors. In the advanced circuit design, the *channel length modulation parameter*  $\lambda$  is also considered. The stability of the load current can be described in terms of the output resistance as given by

$$\frac{dI_o}{dV_{DS2}} = \frac{1}{r_o} \quad (2.25)$$

where  $r_o$  is the output resistance of the transistor. The MOSFET current sources require a large output resistance for good stability.

The reference current in current source circuits using BJTs is generally determined by the bias voltages and a resistor. The MOSFET acts like a resistor, and hence, the reference current in MOSFET current mirrors is usually generated using MOSFET connected as shown in Fig. 2.17. The transistors  $M_1$  and  $M_3$  are connected in series. Therefore, we have

$$k_{n1}(V_{GS1} - V_{Th1})^2 = k_{n3}(V_{GS3} - V_{Th3})^2 \quad (2.26)$$

Assuming that the parameters  $V_{Th}$ ,  $\mu_n$  and  $C_{ox}$  are identical for all the transistors, Eq. (2.26) can be written as

$$V_{GS1} = \sqrt{\frac{(W/L)_3}{(W/L)_1}} V_{GS3} + \left(1 - \sqrt{\frac{(W/L)_3}{(W/L)_1}}\right) V_{Th} \quad (2.27)$$

From the circuit, we see that

$$V_{GS1} + V_{GS3} = V_{DD} - V_{SS} \quad (2.28)$$

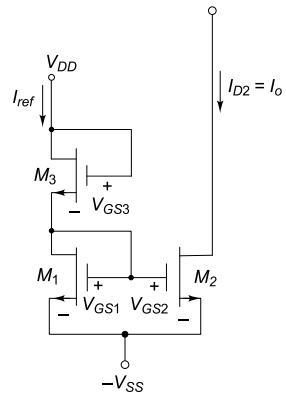
Therefore, using Eqs. (2.27) and (2.28), we get

$$V_{GS1} = V_{GS2} = \frac{\sqrt{\frac{(W/L)_3}{(W/L)_1}}}{1 + \sqrt{\frac{(W/L)_3}{(W/L)_1}}} (V_{DD} - V_{SS}) + \frac{\left(1 - \sqrt{\frac{(W/L)_3}{(W/L)_1}}\right) V_{Th}}{1 + \sqrt{\frac{(W/L)_3}{(W/L)_1}}} \quad (2.29)$$

The load current  $I_o$  in terms of the aspect ratio and process parameters is given by

$$I_o = \left(\frac{W}{L}\right)_2 \left(\frac{1}{2} \mu_n C_{ox}\right) (V_{GS} - V_{Th})^2 \quad (2.30)$$

As the aspect ratio ( $W/L$ ) of the transistors can be controlled, the MOSFET current source is very efficient.



**Fig. 2.17** MOSFET current source

## Example 2.6

Design a current source using MOSFETs for  $I_{ref} = 0.25 \text{ mA}$  and  $I_o = 0.2 \text{ mA}$ . Assume  $k_n = \frac{1}{2}\mu_n C_{ox} = 20 \mu\text{A/V}^2$ ,  $V_{Th} = 1 \text{ V}$ ,  $V_{GS2} = 1.752 \text{ V}$  and  $\lambda = 0$ . Also assume  $V_{DD} = 5 \text{ V}$  and  $V_{SS} = 0 \text{ V}$ .

**Solution** Given  $I_{ref} = 0.25 \text{ mA}$  and  $I_o = 0.2 \text{ mA}$ ,  $V_{DD} = 5 \text{ V}$  and  $V_{SS} = 0 \text{ V}$ .

$$k_n = \frac{1}{2}\mu_n C_{ox} = 20 \mu\text{A/V}^2, V_{Th} = 1 \text{ V}, V_{GS2} = 1.752 \text{ V}, \text{ and } \lambda = 0$$

Using Eq. (2.30), we have

$$\left(\frac{W}{L}\right)_2 = \frac{I_o}{\left(\frac{1}{2}\mu_n C_{ox}\right)(V_{GS2} - V_{Th})^2} = \frac{0.2 \times 10^{-3}}{(20 \times 10^{-6})(1.752 - 1)^2} = 17.7$$

It can be observed that the transistor  $M_2$  is biased in the saturation region since

$$V_{DS} > V_{DS(\text{sat})} = V_{GS2} - V_{Th} = 1.752 - 1 = 0.752 \text{ V}$$

$$\text{The reference current } I_{ref} = I_o = \left(\frac{W}{L}\right)_1 \left(\frac{1}{2}\mu_n C_{ox}\right) (V_{GS1} = V_{Th})^2$$

Assuming  $V_{GS1} = V_{GS2}$ , we get

$$\left(\frac{W}{L}\right)_1 = \frac{I_{ref}}{\left(\frac{1}{2}\mu_n C_{ox}\right)(V_{GS2} - V_{Th})^2} = \frac{0.25 \times 10^{-3}}{(20 \times 10^{-6})(1.752 - 1)^2} = 22.1$$

The value of  $V_{GS3}$  is given by

$$V_{GS3} = V_{DD} - V_{SS} - V_{GS1} = 5 - 0 - 1.752 = 3.248 \text{ V}$$

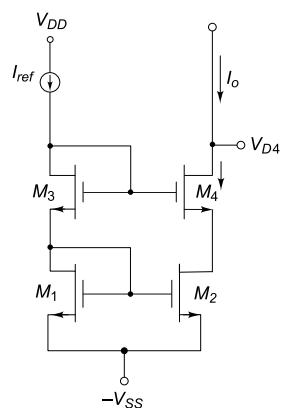
Since  $I_{ref} = k_{n3} (V_{GS3} - V_{Th})^2$ , we have

$$\left(\frac{W}{L}\right)_3 = \frac{I_{ref}}{\left(\frac{1}{2}\mu_n C_{ox}\right)(V_{GS3} - V_{Th})^2} = \frac{0.25 \times 10^{-3}}{(20 \times 10^{-6})(3.248 - 1)^2} = 2.47$$

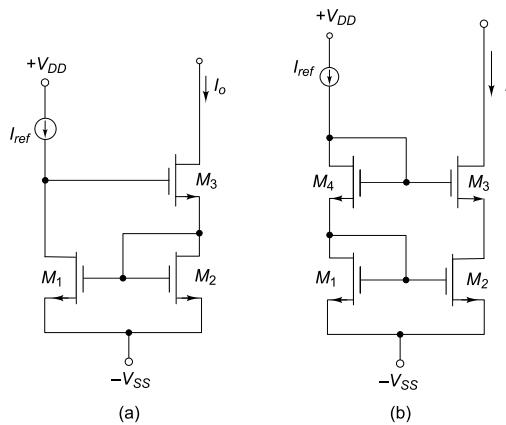
### 2.4.2 Multi-MOSFET Current-Source Circuits

In the current source circuits using MOSFETs, the output resistance denotes the stability against the changes in the output voltage. This output resistance can be enhanced by the circuit shown in Fig. 2.18, which is called a *cascode current mirror*. The reference current is generated by introducing another MOSFET in the reference branch of the circuit. Then, assuming that all the transistors are identical, we achieve  $I_o = I_{ref}$ .

Figures 2.19(a) and (b) show two other multi-MOSFET current sources. The circuit of Fig. 2.19(a) is the *Wilson current source* where the  $V_{DS}$  values of  $M_1$  and  $M_2$  are unequal. The channel length coefficient  $\lambda$  of the transistor is not assumed to be zero for the circuit of Fig. 2.19(a). Hence, the ratio  $I_o/I_{ref}$  is different from that defined by the aspect ratios.



**Fig. 2.18** MOSFET cascode current mirror



**Fig. 2.19** (a) MOSFET Wilson current source  
(b) Modified MOSFET Wilson current source

This problem is eliminated in the modified version of Wilson current source shown in Fig. 2.19(b). It includes transistor  $M_4$  with its gate tied to the drain. For a constant reference current  $I_{ref}$ , the drain-to-source voltages of  $M_1$  and  $M_2$  are maintained constant. The primary advantage of these circuits is their high value of output resistance, and this helps in better stabilisation of the load current.

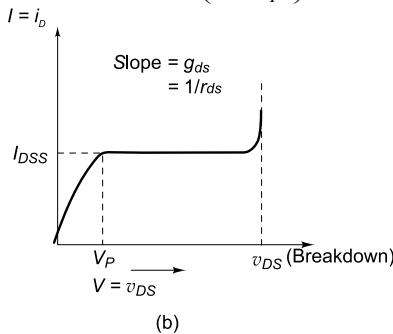
### 2.4.3 JFET Current Sources

Current sources using JFETs make fundamental elements in JFET ICs. The basic method of designing a current source is to interconnect the gate and source terminals of a depletion-mode N-channel JFET as shown in Fig. 2.20. The device remains biased in its saturation region, when the following condition represented by Eq. (2.31) is satisfied. Figure 2.21 shows the  $V$ - $I$  characteristic of the JFET current source. It is basically the  $I_{DS}$  versus  $V_{DS}$  characteristic of the JFET, when  $V_{GS} = 0$ .

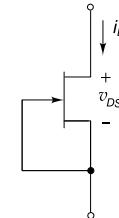
$$v_{DS} \geq v_{DS(sat)} = v_{GS} - V_p = |V_p| \quad (2.31)$$

Assuming non-zero  $\lambda$  factor, the current in the saturation region is given by

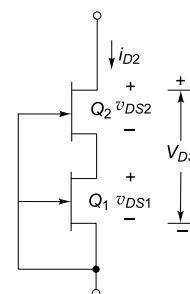
$$I_D = I_{DS} \left( 1 + \frac{V_{GS}}{V_p} \right)^2 (1 + \lambda v_{DS}) = I_{DS} (1 + \lambda v_{DS}) \quad (2.32)$$



**Fig. 2.21** V-I characteristics of JFET current source



**Fig. 2.20** Current source using depletion mode JFET



**Fig. 2.22** JFET cascode current source

The output resistance looking into the drain terminal is obtained using Eq. (2.32). Hence,

$$\frac{1}{r_o} = \frac{di_D}{dv_{DS}} = \lambda I_{DS} \quad (2.33)$$

This expression for the output resistance of a JFET current source is similar to that of a MOSFET current source discussed in previous section.

The output resistance of a JFET current source can be enhanced by the use of a cascode configuration of JFETs. Figure 2.22 shows a simple JFET cascode current source with two *N*-channel depletion-mode devices.

#### 2.4.4 MOSFET Current Sources Relatively Independent of Supply Voltage

Figure 2.23 shows a MOSFET current source which has its output current relatively independent of the supply voltage. The output current  $I_o$  derived from the circuit is given by

$$I_o = I_{D2} = V_{GS1}/R_1$$

and  $I_1$  is given by

$$I_1 = \frac{V_{DD} - V_{SS} - V_{GS2} - V_{GS1}}{R_1} \quad (2.34)$$

Since we normally have  $V_{DD} - V_{SS} \gg V_{GS}$ , Eq. (2.34) can be simplified as

$$I_1 = \frac{V_{DD} - V_{SS}}{R_1} \quad (2.35)$$

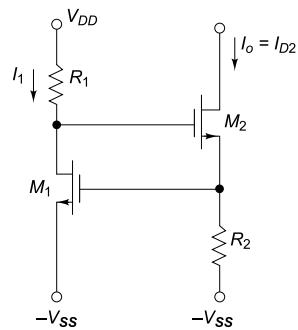
A number of MOS bias circuit designs can be designed, that closely follow the BJT circuit approaches discussed so far. To achieve supply independence, the MOS bias circuit may employ a reference other than the supply voltage  $V_{DD}$ . The possible references are as follows:

- (i) Threshold voltage  $V_{Th}$
- (ii) The difference between the threshold voltages of dissimilar devices  $\Delta V_{Th}$
- (iii) The base-emitter voltage  $V_{BE}$  of the parasitic bipolar transistor in CMOS technology
- (iv) Thermal voltage  $V_T$  and
- (v) The bandgap voltage  $V_{GO}$  of silicon ( $=1.205$  V)

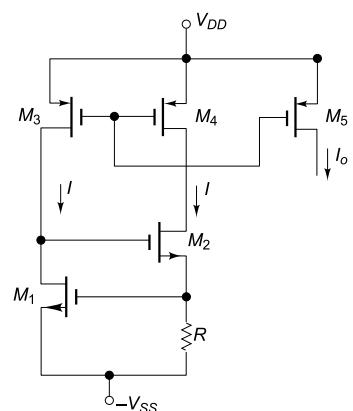
A Zener diode reference is also available in CMOS technology but it is not frequently utilised due to its relatively high breakdown voltage level required.

#### 2.4.5 Current Source using Threshold Reference

Figure 2.24 shows a current source circuit using self-biased threshold reference bias. In this circuit, the feedback achieved through  $M_2$ ,  $M_3$  and  $M_4$  forces equal current to flow in transistor  $M_1$ , the same as what is flowing through resistor  $R$ . Considering the channel length modulation and body effects negligible, and



**Fig. 2.23** MOSFET current source relatively independent of power supply



**Fig. 2.24** Self-biased  $V_{Th}$  referenced current-source

assuming low bias current and large W/L ratio for the MOS devices, the bias current  $I$  is given by

$$I = \frac{V_{Th}}{R} \quad (2.36)$$

Threshold reference biasing is found useful in some applications, however, with the following drawbacks:

- (i) The  $V_{Th}$  in a MOS process cannot be controlled effectively due to stringent process parameter conditions. The typical value of  $V_{Th}$  is in the range of 0.4 V to 0.8 V.
- (ii) Threshold voltage of NMOS transistor displays a negative temperature coefficient ( $TC$ ) of about  $-2\text{mV}/^\circ\text{C}$ , whereas the diffused resistors display a substantial positive temperature coefficient value that results in the output current having a large negative temperature coefficient.

A second technique using the  $V_{Th}$  for reference is to employ the difference between the threshold voltage of two MOSFETs of same type with different channel implants and hence different threshold voltages. The main advantage of this technique is that the temperature coefficients of the two threshold voltages cancel to first order and this technique is employed to realise precision voltage references.

#### 2.4.6 Self-Bias Current Source using $V_{BE}$ Reference

A self-bias current source using  $V_{BE}$  as a reference is shown in Fig. 2.25. The transistor  $Q_1$  is the parasitic *PNP* device inherently formed in the *P*-type *bulk* or *substrate* of the CMOS structure. The parasitic *NPN* device can be used in case of *N*-bulk CMOS technology. The feedback circuit formed by  $M_1$ ,  $M_2$ ,  $M_3$  and  $M_4$  forces the current in transistor  $Q_1$  to be the same as that flowing in resistor  $R$ . Therefore, the operating point must satisfy the following equation.

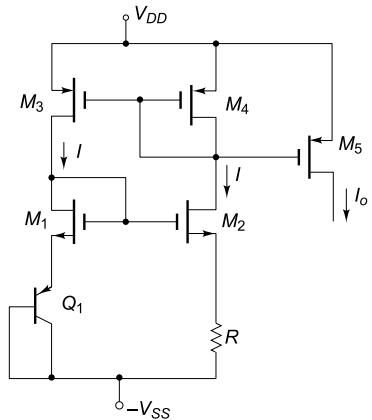
$$IR = V_T \ln \frac{I}{I_S} \quad (2.37)$$

Then, Eq. (2.37) can also be expressed as

$$I = \frac{V_{BE_1}}{R} \quad (2.38)$$

This self-bias current source circuit has the advantage that normally  $V_{BE}$  is a parameter which is relatively well-controlled. However, it exhibits a negative temperature coefficient ( $TC$ ) of about  $-2\text{mV}/^\circ\text{C}$ . This factor combined with the strong positive  $TC$  of the diffused and polysilicon resistors obtainable in linear ICs results in a strong negative  $TC$  in the resulting bias current.

The current sources employing threshold voltage  $V_{Th}$  as a reference can also be implemented, which offers much smaller  $TC$  of the output current than the  $V_{BE}$  reference. Its primary advantage lies in the fact that the positive  $TC$  of  $V_T$  in combination with the positive  $TC$  of the resistor tends to cancel each other resulting in a relatively temperature independent output current.



**Fig. 2.25** CMOS self-bias current source using  $V_{BE}$  as reference

## 2.5 CURRENT SOURCES AS ACTIVE LOADS

The current source can be used as an active load in both analog and digital ICs. The active load realised using current source in place of the passive load (i.e. a resistor) in the collector arm of differential amplifier makes it possible to achieve high voltage gain without requiring large power supply voltage. The active load so achieved is basically  $r_o$  of a *PNP* transistor. The active loads using the current sources for differential amplifier configurations are discussed in Sec. 2.11.

## 2.6 VOLTAGE SOURCES

A voltage source is a circuit that produces an output voltage  $V_o$ , which is independent of the load driven by the voltage source, or the output current supplied to the load. The voltage source is the circuit dual of the constant current source.

A number of IC applications require a voltage reference point with very low ac impedance and a stable dc voltage that is not affected by power supply and temperature variations. There are two methods which can be used to produce a voltage source, namely,

- using the impedance transforming properties of the transistor, which in turn determines the current gain of the transistor, and
- using an amplifier with negative feedback.

### 2.6.1 Voltage Source Circuit using Impedance Transformation

The voltage source circuit using the impedance transforming property of the transistor is shown in Fig. 2.26. The source voltage  $V_S$  drives the base of the transistor through a series resistance  $R_S$  and the output is taken across the emitter. From the circuit, the output ac resistance looking into emitter is given by

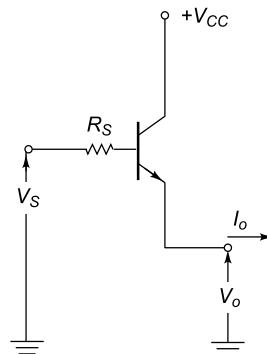
$$\frac{dV_o}{dI_o} = R_o = \frac{R_S}{\beta + 1} + r_{eb} \quad (2.39)$$

Here,  $r_{eb}$  is the internal resistance between emitter and base of the transistor.

With values as high as 100 for  $\beta$ ,  $R_S$  is transformed to a value of

$\frac{R_S}{\beta + 1}$ . It is to be noted that, Eq. (2.39) is applicable only for small changes in the output current.

The load regulation parameter indicates the changes in  $V_o$  resulting from large changes in output current  $I_o$ . Reduction in  $V_o$  occurs as  $I_o$  goes from *no-load* current to *full-load* current and this factor determines the output impedance of the voltage source.



**Fig. 2.26** Voltage source circuit using the impedance transformation

### 2.6.2 Emitter-Follower or Common-Collector Type Voltage Source

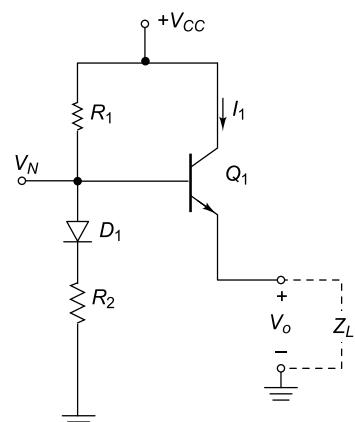
Figure 2.27 shows an emitter-follower or common-collector type voltage source. This voltage source is suitable for the differential gain stage used in op-amps. This circuit has the advantages of

- producing low ac impedance, and
- resulting in effective decoupling of adjacent gain stages.

The low output impedance of the common-collector stage simulates a low impedance voltage source with an output voltage level of  $V_o$  represented by

$$V_o \equiv V_{CC} \left( \frac{R_2}{R_1 + R_2} \right)$$

The diode  $D_1$  is used for offsetting the effect of dc value  $V_{BE}$  across the  $E-B$  junction of transistor, and for compensating the temperature dependence of  $V_{BE}$  drop of  $Q_1$ . The load  $Z_L$  shown in dotted line represents the circuit biased by the current through  $Q_1$ .



**Fig. 2.27** Voltage source using common-collector stage

The impedance  $R_o$  looking into the emitter of  $Q_1$  derived from the hybrid  $\pi$  model is given by

$$R_o \approx \frac{V_T}{I_1} + \frac{R_1 R_2}{\beta(R_1 + R_2)}$$

### 2.6.3 Voltage Source using Temperature Compensated Avalanche Diode

The voltage source using Fig. 2.27 has the limitations of its vulnerability for changes in bias voltage  $V_N$  and the output voltage  $V_o$  with respect to changes in supply voltage  $V_{CC}$ . This is overcome in the voltage source circuit using the breakdown voltage of the base-emitter junction shown in Fig. 2.28.

The emitter-follower stage of Fig. 2.27 is eliminated in this circuit, since the impedance seen looking into the bias terminal  $N$  is very low. The current source  $I_1$  is normally simulated by a resistor connected between  $V_{CC}$  and node  $N$ . Then, the output voltage level  $V_o$  at node  $N$  is given by

$$V_o = V_B + V_{BE}$$

where  $V_B$  is the breakdown voltage of diode  $D_B$  and  $V_{BE}$  is the diode drop across  $D_1$ . The breakdown diode  $D_B$  is normally realised using the base-emitter junction of the transistor. The diode  $D_1$  provides partial compensation for the positive temperature coefficient effect of  $V_B$ . In a monolithic IC structure,  $D_B$  and  $D_1$  can be conveniently realised as a single transistor with two individual emitters as shown in Fig. 2.29.

The structure consists of composite connection of two transistors which are diode-connected back-to-back. Since the transistors have their base and collector terminals common, they can be designed as a single transistor with two emitters.

The output resistance  $R_o$  looking into the output terminal in Fig. 2.28 is given by

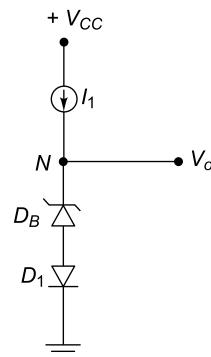
$$R_o = R_B + \frac{V_T}{I_1}$$

where  $R_B$  and  $V_T/I_1$  are the ac resistances of the base-emitter resistance of diode  $D_B$  and  $D_1$  respectively. Typically  $R_B$  is in the range of  $40\ \Omega$  to  $100\ \Omega$ , and  $V_o$  is in the range of  $6.5\text{ V}$  to  $9\text{ V}$ .

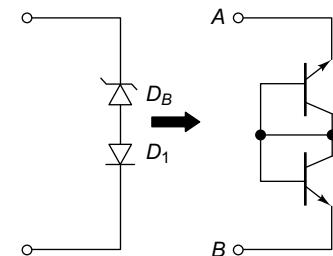
### 2.6.4 Voltage Source using $V_{BE}$ as a Reference

The output stage of op-amp requires stabilised bias voltage source, which can be obtained using a forward-biased diode-connected transistor.

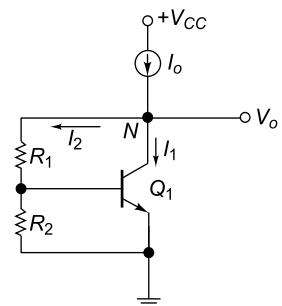
The forward voltage drop for such a connection is approximately  $0.7\text{ V}$ , and it changes slightly with current. When a voltage level greater than  $0.7\text{ V}$  is needed, several diodes can be connected in series, which can offer integral multiples of  $0.7\text{ V}$ . Alternately, Fig. 2.30 shows a



**Fig. 2.28** Voltage source using the breakdown voltage of the base-emitter junction



**Fig. 2.29** Temperature compensated avalanche diode



**Fig. 2.30**  $V_{BE}$  Multiplier circuit

multiplier circuit, which can offer voltage levels, that need not be integral multiples of 0.7 V. The drop across  $R_2$  equals  $V_{BE}$  drop of  $Q_1$ . Considering negligible base current for  $Q_1$ , current through  $R_2$  is the same as that flowing through  $R_1$ . Therefore, the output voltage  $V_o$  can be expressed as

$$V_o = I_2(R_1 + R_2) = \frac{V_{BE}}{R_2}(R_1 + R_2) = V_{BE} \left( \frac{R_1}{R_2} + 1 \right) \quad (2.40)$$

Hence, the voltage  $V_o$  can be any multiple of  $V_{BE}$  by properly selecting the resistors  $R_1$  and  $R_2$ . Due to the shunt feedback provided by  $R_1$ , the transistor current  $I_1$  automatically adjusts itself, towards maintaining  $I_2$  and  $V_o$  relatively independent of the changes in supply voltage.

The ac output resistance of the circuit  $R_o$  is given by,

$$R_o = \frac{dV_o}{dI_o} \cong \frac{R_1 + R_2}{1 + g_m R_2}$$

$$\text{When } g_m R_2 \gg 1, \text{ we have } R_o = \frac{R_1 + R_2}{R_2} \cdot \frac{1}{g_m} \quad (2.41)$$

Using Eq. (2.40), we have

$$\frac{V_o}{V_{BE}} = \frac{R_1 + R_2}{R_2}$$

Therefore,

$$R_o = \frac{V_o}{V_{BE}} \frac{1}{g_m} = \frac{V_o}{V_{BE}} \frac{V_1}{I_C}$$

## 2.7 VOLTAGE REFERENCES

The circuit that is primarily designed for providing a constant voltage independent of changes in temperature is called a *voltage reference*. The most important characteristic of a voltage reference is the *temperature co-efficient of the output reference voltage*  $TC_R$ , and it is expressed as

$$TC_R = \frac{dV_R}{dT}$$

The desirable properties of a voltage reference are:

- (i) reference voltage must be independent of any temperature change
- (ii) reference voltage must have good *power supply rejection* which is as independent of the supply voltage as possible
- (iii) output voltage must be as independent of the loading of output current as possible, or in other words, the circuit should have low output impedance

The *voltage reference circuit* is used to bias the *voltage source circuit*, and the combination can be called as the *voltage regulator*. The basic design strategy is producing a zero  $TC_R$  at a given temperature, and thereby achieving good thermal stability. Temperature stability of the order of 100 ppm/ $^{\circ}\text{C}$  is typically expected.

### 2.7.1 Voltage Reference Circuit using Temperature Compensation Scheme

The voltage reference circuit using basic temperature compensation scheme is shown in Fig. 2.31. This design utilises the close thermal coupling achievable among the monolithic components and this technique compensates the known thermal drifts by introducing an opposing and compensating drift source of equal magnitude.

A constant current  $I$  is supplied to the avalanche diode  $D_B$  and it provides a bias voltage of  $V_B$  to the base of  $Q_1$ . The temperature dependence of the  $V_{BE}$  drop across  $Q_1$  and those across  $D_1$  and  $D_2$  results in respective temperature coefficients. Hence, with the use of resistors  $R_1$  and  $R_2$  with tapping across them at point  $N$  compensates for the temperature drifts in the base-emitter loop of  $Q_1$ . This results in generating a voltage reference  $V_R$  with nominally zero temperature coefficient.

Applying Kirchhoff's current law at node  $N$  of Fig. 2.31, we get

$$\frac{V_B - V_{BE(Q_1)} - V_{BE(D_1)} - V_R}{R_1} = \frac{V_R - V_{BE(D_2)}}{R_2} \quad (2.42)$$

Assuming matched transistors,

$$V_{BE(Q_1)} = V_{BE(D_1)} = V_{BE(D_2)} = V_{BE}$$

Then, Eq. (2.42) can be expressed as

$$\frac{V_B - 2V_{BE} - V_R}{R_1} = \frac{V_R - V_{BE}}{R_2}$$

Therefore, the voltage level  $V_R$  is given by

$$V_R = \frac{R_2 V_B + V_{BE} (R_1 - 2R_2)}{R_1 + R_2} \quad (2.43)$$

Differentiating  $V_B$  and  $V_{BE}$  in Eq. (2.43) partially with respect to temperature, we get

$$0 = \frac{R_2}{R_1 + R_2} \frac{\partial V_B}{\partial T} + \left[ \frac{(R_1 - 2R_2)}{R_1 + R_2} \right] \frac{\partial V_{BE}}{\partial T}$$

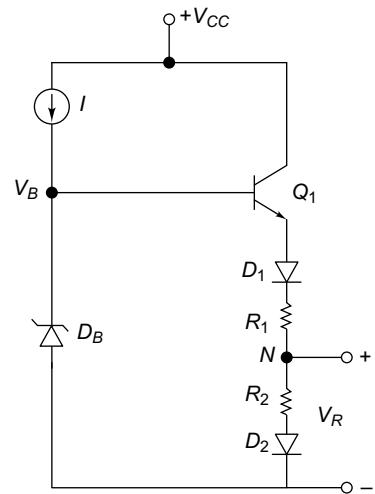
That is,

$$\frac{2R_2 - R_1}{R_2} = \frac{\partial V_B / \partial T}{\partial V_{BE} / \partial T} \quad (2.44)$$

Therefore, it can be inferred that Eq. (2.44) is to be satisfied for obtaining zero temperature coefficient.

### 2.7.2 Voltage Reference Circuit using Avalanche Diode Reference

A voltage reference can be implemented using the *breakdown phenomenon* that occurs in the reverse-biased condition of a heavily doped  $PN$  junction. The *Zener* breakdown is the main mechanism for



**Fig. 2.31** Voltage reference circuit using temperature compensation scheme

junctions, which breakdown at a voltage of 5V or less. For integrated transistors, the base-emitter breakdown voltage falls in the range of 6 to 8V. Therefore, the breakdown in the junctions of the integrated transistor is primarily due to *avalanche* multiplication. The avalanche breakdown voltage  $V_B$  of a transistor incurs a positive temperature coefficient, typically in the range of 2 mV/ $^{\circ}$ C to 5 mV/ $^{\circ}$ C.

Figure 2.32 depicts a current reference circuit using avalanche diode reference. The base bias for transistor  $Q_1$  is provided through resistor  $R_1$  and it also provides the dc current needed to bias  $D_B$ ,  $D_1$  and  $D_2$ .

The voltage at the base of  $Q_1$  is equal to the Zener voltage  $V_B$  added with two diode drops due to  $D_1$  and  $D_2$ . The voltage across  $R_2$  is equal to the voltage at the base of  $Q_1$  less the sum of the base-emitter voltages of  $Q_1$  and  $Q_2$ . Hence, the voltage across  $R_2$  is approximately equal to that across  $D_B = V_B$ . Since  $Q_2$  and  $Q_3$  act as a current mirror circuit, current  $I_o$  equals the current through  $R_2$ .

Therefore,

$$I_o \approx \frac{V_B}{R_2} \quad (2.45)$$

Equation (2.45) shows that, the output current  $I_o$  has low temperature coefficient, if the temperature coefficient of  $R_2$  is low, such as that produced by a diffused resistor in IC fabrication.

The zero temperature coefficient for output current can be achieved, if diodes are added in series with  $R_2$ , so that, they can compensate for the temperature variation of  $R_2$  and  $V_B$ . The temperature compensated avalanche diode reference source circuit is shown in Fig. 2.33. The transistor  $Q_4$  and  $Q_5$  form an active load current mirror circuit. The base voltage of  $Q_1$  is the voltage  $V_B$  across Zener  $D_B$ .

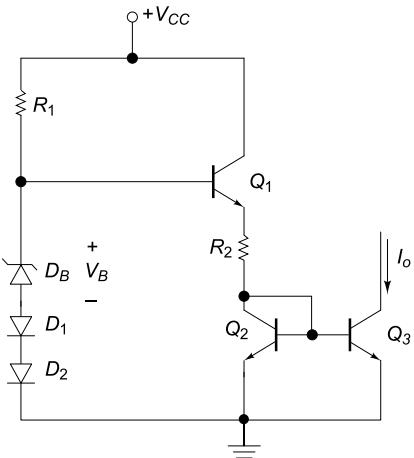
Then,  $V_B = (V_{BE} \times n) + V_{BE}$  across  $Q_1 + V_{BE}$  across  $Q_2 + \text{drop across } R_2$ . Here,  $n$  is the number of diodes.

It can be expressed as

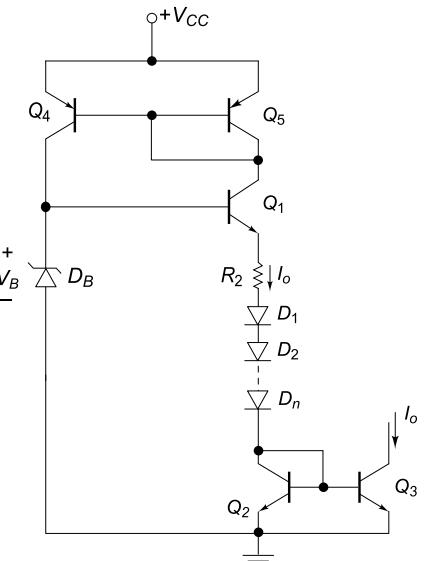
$$V_B = (n + 2)V_{BE} + I_o \times R_2 \quad (2.46)$$

Differentiating Eq. (2.46) for  $V_B$ ,  $I_o \times R_2$  and  $V_{BE}$  partially, with respect to temperature  $T$ , we get

$$\frac{\partial V_B}{\partial T} = (n + 2) \frac{\partial V_{BE}}{\partial T} + R_2 \frac{\partial I_o}{\partial T} + I_o \frac{\partial R_2}{\partial T} \quad (2.47)$$



**Fig. 2.32** Voltage reference using avalanche diode reference



**Fig. 2.33** Temperature compensated avalanche diode reference source

Dividing Eq. (2.47) throughout by  $I_o R_2$ , we get

$$\frac{1}{I_o R_2} \frac{\partial V_B}{\partial T} = \frac{(n+2)}{I_o R_2} \frac{\partial V_{BE}}{\partial T} + \frac{1}{I_o} \frac{\partial I_o}{\partial T} + \frac{1}{R_2} \frac{\partial R_2}{\partial T}.$$

Therefore, zero temperature coefficient of  $I_o$  can be obtained, if the following condition is satisfied.

That is,

$$\frac{1}{I_o} \frac{\partial I_o}{\partial T} = 0 = \frac{1}{R_2 I_o} \left[ \frac{\partial V_B}{\partial T} - (n+2) \frac{\partial V_{BE}}{\partial T} \right] - \frac{1}{R_2} \frac{\partial R_2}{\partial T} \quad (2.48)$$

## 2.8 BANDGAP VOLTAGE REFERENCE

The temperature compensated avalanche diodes were used for the voltage references discussed in the previous section. The lowest available voltage temperature compensated avalanche diode is 6.2 V. When the supply voltage is 6 V or less, the reference voltage is developed from the highly predictable base-emitter voltage  $V_{BE}$  of the transistors. In its simplest form, the reference developed is equal to the energy bandgap voltage  $V_{GO}$  of the semiconductor material, which is 1.205V for silicon. This eases the minimum input voltage limitation on operating voltage, and the output voltage is also well determined and predictable in an IC.

A typical energy bandgap voltage reference circuit is shown in Fig. 2.34. The transistor  $Q_1$  with its base connected to the collector operates with a relatively high current density. The current density of  $Q_2$  is 10 times lower, and  $\Delta V_{BE}$  between the transistors  $Q_1$  and  $Q_2$  appears across resistor  $R_2$ . If the transistors have high current gain  $\beta$ , then the voltage drop across  $R_2$  will be proportional to  $\Delta V_{BE}$ . Transistor  $Q_3$  is a gain regulator stage with the output voltage  $V_R$  equal to its emitter-base voltage plus the drop across  $R_2$ . The emitter-base voltage  $V_{BE}$  of  $Q_3$  has a negative temperature coefficient, while the  $\Delta V_{BE}$  drop across  $R_2$  has a positive temperature coefficient.

The voltage  $V_R$  from the circuit is given by

$$V_R = V_{BE3} + I_2 R_2 \quad (2.49)$$

Assuming all transistors are identical, we have

$$I_o = I_2 e^{\Delta V_{BE} / V_T} = I_2 e^{\left( \frac{V_{BE1} - V_{BE2}}{V_T} \right)} = I_2 e^{\left( \frac{I_2 R_3}{V_T} \right)} \quad (2.50)$$

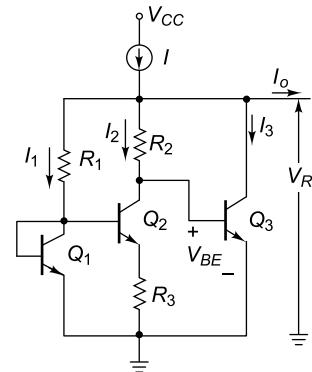
or,

$$I_2 R_3 = V_T \ln \frac{I_1}{I_2} \quad (2.51)$$

Neglecting the base current of  $Q_2$ , we have  $I_{E2} = I_{C2}$

That is, using Eq. (2.51), we get

$$I_2 R_2 = \frac{I_2 R_3}{R_3} R_2 = \frac{R_2}{R_3} V_T \ln \frac{I_1}{I_2} \quad (2.52)$$



**Fig. 2.34** Energy bandgap voltage reference circuit

Substituting Eq. (2.52) in Eq. (2.49), we get

$$V_R = V_{BE3} + \frac{R_2}{R_3} V_T \ln \frac{I_1}{I_2} \quad (2.53)$$

The first term  $V_{BE3}$  has a negative  $TC$  and the second term has a positive  $TC$  due to  $V_T = kT/q$ . Thus, by suitably selecting the ratios of  $R_2/R_3$  and  $I_1/I_2$ , it becomes possible to get a resultant temperature coefficient of zero. Differentiating Eq. (2.53) with respect to  $T$  for obtaining the  $TC$  of  $V_R$  gives us

$$TC_{V(\text{ref})} = \frac{dV_R}{dT} = \frac{dV_{BE3}}{dT} + \frac{R_2}{R_3} \frac{k}{q} \ln \frac{I_1}{I_2} \quad (2.54)$$

The resistors  $R_2$  and  $R_3$  normally have similar characteristics due to their close proximity and identical fabrication process conditions. This makes the ratio  $R_2/R_3$  relatively independent of temperature.

Considering the basic silicon diode theory of PN-junction, the forward bias voltage  $V_D = V_T \ln \left( \frac{I_D}{I_S} \right)$  where  $V_T$  is the thermal voltage as given by  $V_T = \frac{kT}{q}$  and  $I_S$  represent the saturation current given by

$I_S = BT^3 \exp \frac{-V_{GO}}{V_T}$  where  $k$  is the Boltzmann's constant of  $1.381 \times 10^{-23}$ ,  $q$  is the charge of  $1.602 \times 10^{-19}\text{C}$ ,  $T$  is the absolute temperature,  $V_{GO}$  is the bandgap voltage which is 1.2V for silicon, and  $B$  is a proportionality constant. The temperature coefficient ( $TC$ ) of thermal voltage is  $TC(V_T) = \frac{\partial}{\partial T} \left( \frac{kT}{q} \right) = \frac{k}{q}$ . The  $TC$  of junction voltage  $V_D$  at a given  $I_D$  is

$$\begin{aligned} TC_{VD} &= \frac{\partial V_D}{\partial T} = \frac{\partial V_T}{\partial T} \ln \left( \frac{I_D}{I_S} \right) + V_T \frac{\partial}{\partial T} \left( \ln \left( \frac{I_D}{I_S} \right) \right) \\ &= \frac{k}{q} \ln \frac{I_D}{I_S} + V_T \frac{\partial}{\partial T} \left( -\ln \left( T^3 \exp \frac{-V_{GO}}{V_T} \right) \right) \\ &= \frac{V_D}{T} + V_T \frac{\partial}{\partial T} \left[ -\left( 3 \ln T - \frac{V_{GO}}{V_T} \right) \right] \end{aligned}$$

Therefore, the temperature coefficient of  $V_{BE}$  is given by

$$TC(V_{BE}) = \frac{V_D}{T} - \frac{3k}{q} - \frac{V_{GO}}{T}$$

The  $TC$  for the  $V_{BE}$  drop can be obtained as given by,

$$TC_{V(BE)} = \frac{dV_{BE}}{dT} = \frac{V_{BE} - (V_{GO} + 3V_T)}{T} \quad (2.55)$$

Assuming  $V_{GO} = 1.205\text{V}$  (a more precise value),  $V_{BE} = 0.65\text{ V}$  and  $V_T = 26\text{ mV}$ ,

$$TC_{V(BE)} = \frac{dV_{BE}}{dT} = -2.1\text{ mV/}^\circ\text{C}$$

Substituting Eq. (2.55) in Eq. (2.54) to find the condition for a zero temperature coefficient, we get

$$TC_{V(\text{ref})} = \frac{dV_R}{dT} = \frac{V_{BE} - (V_{GO} + 3V_T)}{T} + \frac{R_2}{R_3} \frac{k}{q} \ln \frac{I_1}{I_2} \quad (2.56)$$

We require  $TC_{V(\text{ref})} = 0$ .

Therefore, equating the RHS of Eq. (2.56) to zero gives,

$$V_{BE} = V_{GO} + 3V_T - \frac{R_2}{R_3} V_T \ln \frac{I_1}{I_2} \quad (2.57)$$

Substituting Eq. (2.57) for  $V_{BE}$  in Eq. (2.53) gives us,

$$V_R = V_{GO} + 3V_T = 1.205 + 3 \times 26 \times 10^{-3} = 1.283\text{ V at } 300^\circ\text{C}$$

It shows that the bandgap reference source, while operating under zero  $TC_{V(\text{ref})}$  condition, gives an output voltage of  $1.283\text{V}$  and it also shows that the energy bandgap value  $V_{GO} = 1.205\text{ V}$  (for silicon) determines  $V_R$ .

A high input impedance buffer circuit may be inserted between the voltage reference and the load to be driven for reducing the output resistance of bandgap reference. The circuit also provides good degree of power supply rejection.

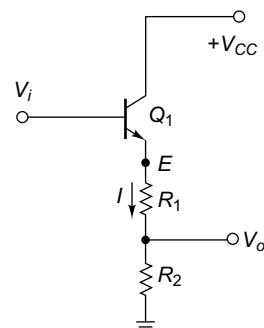
The IC type LM113 uses a bandgap reference of  $1.2\text{ V}$  and its voltage changes by  $0.5\%$  with temperature, and this chip finds use in regulator applications for voltages less than  $6\text{ V}$ . Laser trimmed thin-film of resistors for  $R_2$  and  $R_3$  also provide minimum  $TC$  of the order of a few  $\mu\text{V/}^\circ\text{C}$ .

## 2.9 DC LEVEL SHIFT STAGES

Fabrication of large value coupling capacitors, such as those needed for dc coupling in broadband amplifiers are not easy to be fabricated in IC technology. The *NPN* common-emitter gain stage always produces dc level that is higher than the dc level at the input.

When a number of gain stages are cascaded for larger gain values, the dc level at the output rapidly builds up reaching the supply voltages. This results in poor linearity and amplitude limitation, or clipping of output voltage swing. This problem can be overcome by using a *level shift stage* between each of the gain stages so that the output dc level is shifted towards the negative supply. This circuit also helps in preventing inter-stage loading effects with its inherent characteristics of high input impedance and relatively low output impedance values.

A typical dc level shift stage used in op-amp design is shown in Fig. 2.35, employing a common collector stage to buffer the input signal. This provides an easier means of shifting the input level  $V_i$  to a more negative dc level  $V_o$ .



**Fig. 2.35** A typical level shift stage circuit

To obtain the output value  $V_o$ , consider a current  $I$  flowing through the emitter branch of  $Q_1$  and it is given by

$$I = \frac{V_E}{R_1 + R_2}$$

where  $V_E$  is the voltage at the emitter of  $Q_1$  at node  $E$ .

Therefore, the output voltage  $V_o = \frac{V_E}{R_1 + R_2} \times R_2$

Here,

$$V_E = V_i - V_{BE1}$$

Hence, we have

$$V_o = \frac{(V_i - V_{BE2})R_2}{(R_1 + R_2)}$$

This form of level shift circuit has a main drawback. The ac gain of the circuit starts reducing as  $R_2$  is decreased for improving the net dc level shift. Moreover, its output impedance is also comparatively high. This limitation makes the level shift stage using avalanche diode an attractive alternative circuit for shifting the dc level. It is shown in Fig. 2.36.

For this circuit, the net dc level shift is given by

$$V_i - V_o = V_{BE} + V_B$$

where  $V_B$  is the breakdown voltage of the avalanche diode  $D_B$ . This circuit may not be suitable for low level ac signals, because of the excess noise generated by the diode  $D_B$ . Further, the value of  $V_B$  obtainable in ICs is limited. However, the voltage gain for the stage is nearly unity if the bulk resistance of  $D_B$  is made negligible as compared with  $R$ .

Another circuit for dc level shift applications is shown in Fig. 2.37. The transistor  $Q_2$  connected with resistors  $R_1$  and  $R_2$  form a  $V_{BE}$  multiplier circuit. Therefore, the voltage between nodes  $E$  and  $F$  is given by

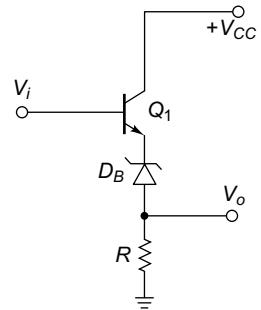
$$V_{EF} = V_{BE} \left( \frac{R_2 + R_1}{R_2} \right) = V_{BE} \left( 1 + \frac{R_1}{R_2} \right)$$

But, we understand from Fig. 2.37 that

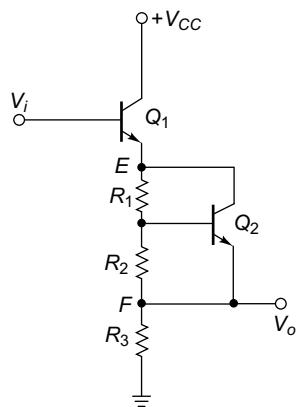
$$V_o = V_i - (V_{BE} + V_{EF})$$

$$\text{Therefore, } V_o = V_i - \left[ V_{BE} + V_{BE} \left( 1 + \frac{R_1}{R_2} \right) \right]$$

$$\text{or } V_i - V_o = V_{BE} (2 + R_1/R_2)$$



**Fig. 2.36** Level shift stage using Avalanche diode



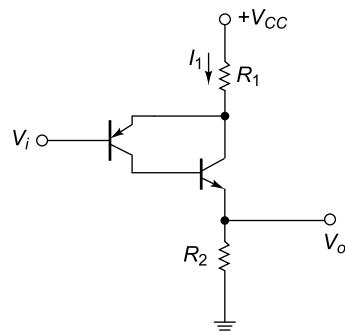
**Fig. 2.37** DC level shift circuit configuration

Figure 2.38 shows another level shifter configuration using a *lateral PNP* and *vertical NPN* transistor configuration. The output dc voltage obtained by the level shift circuit is given by

$$V_o = \frac{R_2}{R_1} (V_{CC} - V_{BE} - V_i)$$

where  $V_{BE}$  is base to emitter voltage of the composite *PNP-NPN* transistor connection. The ac voltage gain of the circuit is given by

$$A_v \equiv -\frac{R_2}{R_1}$$



**Fig. 2.38** DC level stage using *PNP-NPN* transistor arrangement

## 2.10 DIFFERENTIAL AMPLIFIERS

The function of a differential amplifier is to amplify the difference between two signals. The need for differential amplifier arises in many physical measurements where response from dc to many MHz of frequency is required. This forms the basic input stage of an integrated amplifier.

The basic differential amplifier has the following important properties of

- (i) excellent stability
- (ii) high versatility and
- (iii) high immunity to interference signals.

The differential amplifier as a building block of the op-amp has the advantages of

- (i) lower cost
- (ii) easier fabrication as IC component and
- (iii) closely matched components

Figure 2.39 shows the basic block diagram of a differential amplifier, with two input terminals and one output terminal.

The output signal of the differential amplifier is proportional to the difference between the two input signals.

That is,

$$v_o = A_{dm} (v_1 - v_2)$$

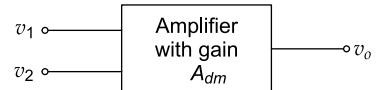
If  $v_1 = v_2$ , then the output voltage is zero. A non-zero output voltage  $v_o$  is obtained when  $v_1$  and  $v_2$  are not equal. The *difference mode* input voltage is defined as

$$v_{dm} = v_1 - v_2$$

and the *common mode* input voltage is defined as

$$v_{cm} = \frac{(v_1 + v_2)}{2}$$

These equations show that if  $v_1 = v_2$ , then the differential mode input signal is zero and common mode input signal is  $v_{cm} = v_1 = v_2$ . For example, if  $v_1 = +20 \mu V$  and  $v_2 = -20 \mu V$ , then the differential mode voltage is  $v_{id} = +40 \mu V$  and the common voltage  $v_{cm} = 0$ . However, if  $v_1 = 120 \mu V$  and  $v_2 = 80 \mu V$ , then the differential mode input signal is still  $v_{dm} = +40 \mu V$ , but the common mode input signal is  $v_{cm} = 100 \mu V$ . For both the sets of input voltages, the output voltage of an ideal differential amplifier would be exactly the same. However, in practice the common mode input signal affects the output. In the design of differential amplifier, the main aim is to minimise the effect of common mode input signal.

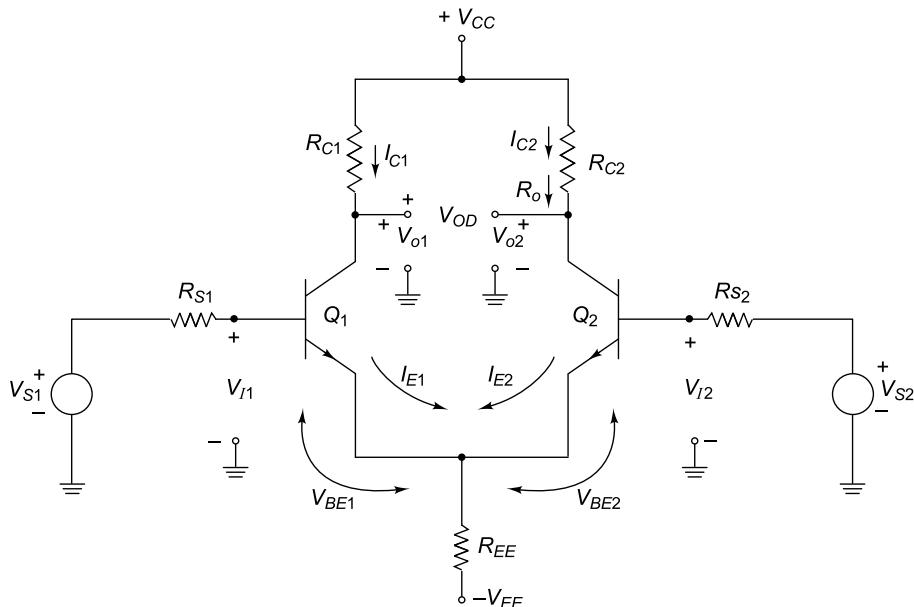


**Fig. 2.39** Block diagram of differential amplifier

### 2.10.1 Differential Amplifiers using BJT

The differential amplifiers using BJT are broadly classified into two types, namely, (i) differential BJT amplifier with resistive loading and (ii) differential BJT amplifier with active loading.

The emitter-coupled or source coupled differential amplifier forms the input stage of most analog ICs. The emitter-coupled differential amplifier circuit is shown in Fig. 2.40. It is important to note that the performance of a differential amplifier depends on the ideal matching characteristics of the transistor pair  $Q_1$  and  $Q_2$ .



**Fig. 2.40** Circuit diagram of emitter-coupled differential amplifier

The amplifier uses both a positive power supply  $+V_{CC}$  and a negative power supply  $-V_{EE}$ . Though in practical situations, the power supplies are equal in magnitude, it need not be the case always. It is to be mentioned that these amplifiers operate at dc, because appropriate dc level shifting could be obtained without the use of coupling capacitors.

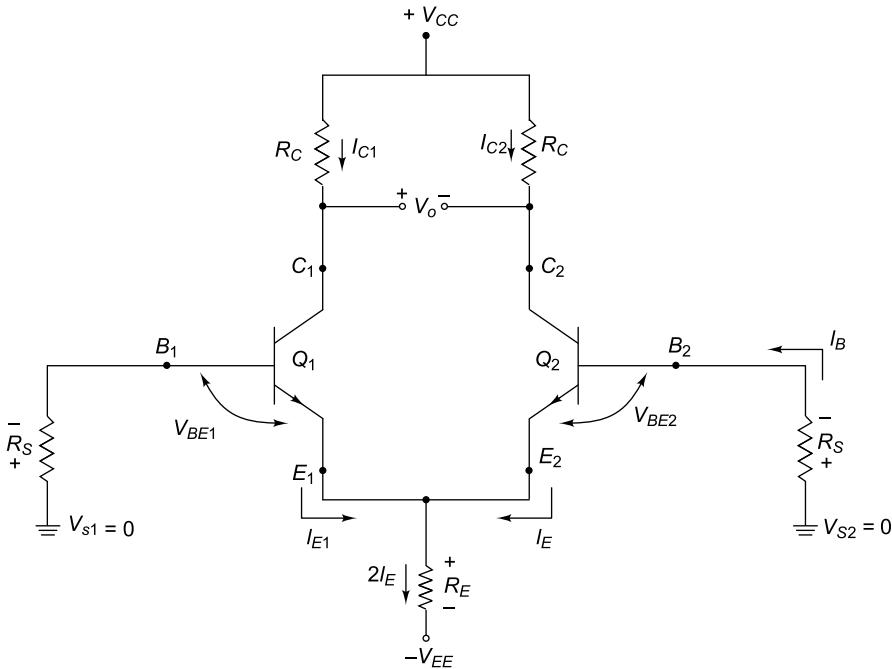
**dc analysis of an emitter-coupled pair** The dc analysis begins with the assumption that  $Q_1$  and  $Q_2$  are ideally matched, and the mismatching effects will be considered later. Also let us consider  $\beta \gg 1$  so that

$$I_{E1} \approx I_{C1} \text{ and } -I_{E2} \approx I_{C2}$$

and hence,

$$V_{I1} = V_{BE1} - V_{BE2} + V_{I2}$$

In the dc analysis, the operating point values, i.e.  $V_{CQ}$  and  $V_{CEQ}$  can be obtained for  $Q_1$  and  $Q_2$ . The dc equivalent circuit can be derived by making ac inputs zero as shown in Fig. 2.41.



**Fig. 2.41** Differential amplifier using BJT

For matched or identical transistor pairs, we have

- $R_E = R_{E1} \parallel R_{E2}$ , since  $R_{E1} = R_{E2}$
- $R_{C1} = R_{C2} = R_C$
- $|V_{CC}| = |V_{EE}|$

For a symmetrical circuit with matched transistors,  $I_{C1Q} = I_{C2Q}$  and  $V_{C1E1Q} = V_{C2E2Q}$ . Hence, the operating point  $I_{CQ}$  and  $V_{CEQ}$  for any one of the two transistors can be found out.

Consider Fig. 2.41 for the dc analysis. Applying KVL to base-emitter loop of  $Q$ , we get

$$I_B R_S + V_{BE} + 2I_E R_E = V_{EE}$$

As  $\beta = \frac{I_C}{I_B}$  for common emitter configuration and  $I_C \approx I_E$ ,  $\beta = \frac{I_E}{I_B}$ .

Therefore,  $\frac{I_E}{\beta} R_S + V_{BE} + 2I_E R_E = V_{EE}$

$$I_E \left[ \frac{R_S}{\beta} + 2R_E \right] = V_{EE} - V_{BE}$$

$$I_E = \frac{V_{EE} - V_{BE}}{\left( \frac{R_S}{\beta} + 2R_E \right)}$$

In practical conditions,  $\frac{R_S}{\beta} \ll 2R_E$ . Therefore,

$$I_E = \frac{V_{EE} - V_{BE}}{2R_E}$$

From the above equation, it can be inferred that

- (i) For a known value of  $V_{EE}$ , the emitter current of  $Q_1$  and  $Q_2$  are determined by  $R_E$
- (ii) The emitter current  $I_E$  is independent of  $R_C$  when  $I_E \gg I_C$

Neglecting drop across and applying KVL to the collector-base loop, we get

$$V_C = V_{CC} - I_C R_C$$

and

$$\begin{aligned} V_{CE} &= V_C - V_E \\ &= V_{CC} - I_C R_C - V_E \end{aligned}$$

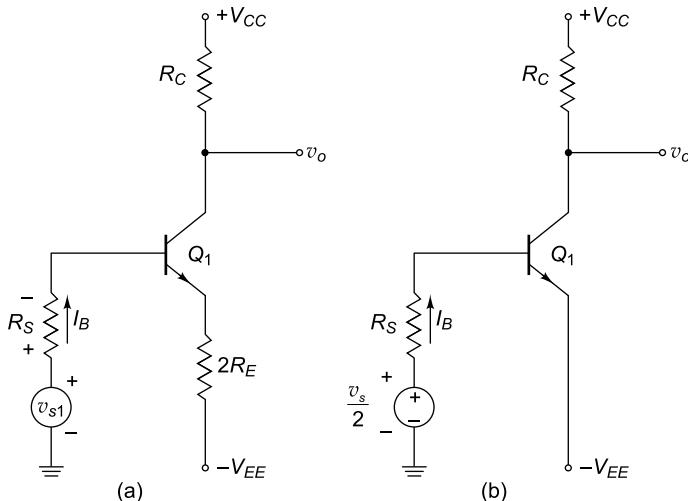
But  $V_E = -V_{BE}$  (voltage at the emitter of  $Q_1$ ).

Thus,

$$V_{CE} = V_{CC} - I_C R_C + V_{BE}$$

The above equation gives  $V_{CEQ} = V_{CE}$  when  $I_E \approx I_C = I_{CQ}$ , for the given values of  $V_{CC}$  and  $V_{EE}$ .

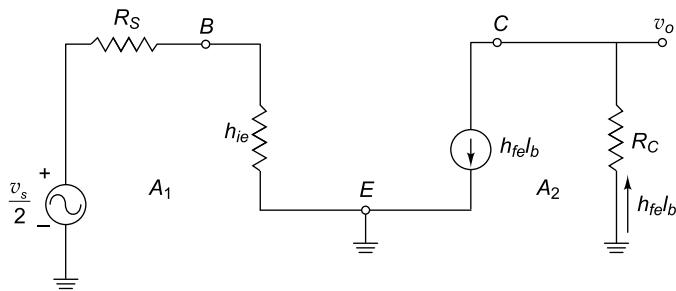
**ac analysis of an emitter-coupled pair** The symmetrical circuit split into two equivalent circuits as shown in Fig. 2.42 will be suitable for ac analysis of an emitter-coupled pair.



**Fig. 2.42** Emitter-coupled pair (a) for  $A_{cm}$  analysis and (b) for  $A_{dm}$  analysis

The differential gain  $A_{dm}$ , common mode gain  $A_{cm}$ , input resistance  $R_i$  and output resistance  $R_o$  can be obtained using the  $h$ -parameter model of the transistors.

**Differential mode gain ( $A_{dm}$ )** For the analysis, assume that the two input signals have a magnitude of  $v_s/2$  and differ from each other by  $180^\circ$  phase shift as shown in Fig. 2.42(b). In Fig. 2.42(a), since  $I_{E1} = I_{E2}$  and they are out of phase by  $180^\circ$ , they cancel each other. The ac equivalent circuit of Fig. 2.42(b) is shown in Fig. 2.43 and a similar structure may be realised for  $Q_2$  also.



**Fig. 2.43** Approximate hybrid model neglecting  $h_{oe}$

Applying KVL to the input loop  $A_1$ , we get

$$I_b(R_s + h_{ie}) = \frac{v_s}{2}$$

$$I_b = \frac{v_s}{2(R_s + h_{ie})}$$

Applying KVL to loop  $A_2$ , the output voltage is

$$v_o = -h_{fe} I_b R_C$$

Therefore,

$$v_o = -h_{fe} R_C \frac{v_s}{2(R_s + h_{ie})}$$

$$\frac{v_o}{v_s} = \frac{-h_{fe} R_C}{2(R_s + h_{ie})}$$

It should be noted that the minus sign in the above equation indicates  $180^\circ$  phase difference between input and output. As the magnitude of the input signals are equal, viz.  $\left(\frac{v_s}{2}\right)$  and are out of phase by  $180^\circ$ , we have

$$v_{id} = \frac{v_s}{2} - \left(-\frac{v_s}{2}\right) = v_s$$

Therefore,

$$A_{dm} = \frac{v_o}{v_{id}} = \frac{v_o}{v_s} = \frac{-h_{fe} R_C}{2(R_s + h_{ie})} \quad (2.58)$$

where  $v_s$  is the differential input voltage.

When the output of a differential amplifier is measured with reference to the ground point, it is called unbalanced output. However,  $A_{dm}$  for a balanced case can be derived by considering the balanced output across the two collectors of  $Q_1$  and  $Q_2$ , which are assumed to be perfectly matched.  $A_{dm}$  for such a condition is twice the value of  $A_{dm}$  obtained for an unbalanced output. Therefore,

$$A_{dm} = \frac{-2h_{fe} R_C}{2(R_s + h_{ie})} = \frac{-h_{fe} R_C}{(R_s + h_{ie})} \quad (2.59)$$

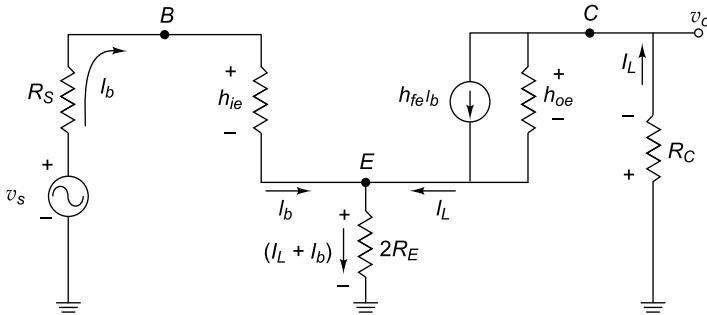
**Common mode gain ( $A_{cm}$ )** For common mode analysis, consider that the input signals have the same magnitude  $v_s$  and are in phase.

Therefore,

$$v_{ic} = \frac{v_1 + v_2}{2} = \frac{v_s + v_s}{2} = v_s \quad (2.60)$$

We know that  $v_o = A_{cm}v_s$ . Hence,  $A_{cm} = \frac{v_o}{v_s}$

Unlike the previous case, the emitter current is considered for the analysis. The current through  $R_E$  is  $2I_E$ . The emitter resistance is assumed to be  $2R_E$  and emitter current to be  $I_E$  instead of  $2I_E$  as shown in Fig. 2.42(a). The appropriate hybrid model is shown in Fig. 2.44.



**Fig. 2.44** Approximate hybrid model

Current through  $R_C = I_L$  (Load Current)

Effective emitter resistance =  $2R_E$

Current through emitter resistance =  $I_L + I_b$

Current through  $h_{oe}$  =  $(I_L - h_{fe}I_b)$

Applying Kirchhoff's voltage law to the input side,

$$I_b R_s + I_b h_{ie} + 2R_E(I_L + I_b) = v_s$$

Therefore,

$$v_s = I_b(R_s + h_{ie} + 2R_E) + I_L(2R_E)$$

and

$$v_o = -I_L R_C$$

As in dc analysis, let us now apply KVL to output loop.

$$I_L R_C + 2R_E(I_L + I_b) + \frac{(I_L - h_{fe}I_b)}{h_{oe}} = 0$$

That is,

$$I_L R_C + 2R_E I_L + 2R_E I_b + \frac{I_L}{h_{oe}} - \frac{h_{fe} I_b}{h_{oe}} = 0$$

Therefore,

$$I_b \left[ 2R_E - \frac{h_{fe}}{h_{oe}} \right] + I_L \left[ R_C + 2R_E + \frac{1}{h_{oe}} \right] = 0$$

That is,

$$I_L \left[ R_C + 2R_E + \frac{1}{h_{oe}} \right] = -I_b \left[ 2R_E - \frac{h_{fe}}{h_{oe}} \right]$$

$$\text{That is, } \frac{I_L}{I_b} = \frac{\left[ \frac{h_{fe}}{h_{oe}} - 2R_E \right]}{\left[ R_C + 2R_E + \frac{1}{h_{oe}} \right]}$$

$$= \frac{h_{fe} - 2R_E h_{oe}}{1 + h_{oe}(2R_E + R_C)}$$

$$\text{Therefore, } I_b = \frac{I_L [1 + h_{oe}(2R_E + R_C)]}{h_{fe} - 2R_E h_{oe}}$$

$$\text{That is, } v_s = \frac{I_L [1 + h_{oe}(2R_E + R_C)](R_s + h_{ie} + 2R_E)}{[h_{fe} - 2R_E h_{oe}]} + I_L(2R_E)$$

$$\frac{v_s}{I_L} = \frac{[1 + h_{oe}(2R_E + R_C)](R_s + h_{ie} + 2R_E)}{[h_{fe} - 2R_E h_{oe}]} + 2R_E$$

$$= \frac{[1 + h_{oe}(2R_E + R_C)](R_s + h_{ie} + 2R_E) + 2R_E(h_{fe} - 2R_E h_{oe})}{[h_{fe} - 2R_E h_{oe}]}$$

Simplifying the above equation, we get

$$\frac{v_s}{I_L} = \frac{h_{oe}R_C[R_s + h_{ie} + 2R_E] + 2R_E(1 + h_{fe}) + R_s(1 + 2R_E h_{oe}) + h_{ie}(1 + 2R_E h_{oe})}{(h_{fe} - 2R_E h_{oe})}$$

Rearranging the last two terms in the numerator, we get

$$\frac{v_s}{I_L} = \frac{h_{oe}R_C(R_s + R_s + h_{ie}) + 2R_E(1 + h_{fe}) + (R_s + h_{ie})(1 + 2R_E h_{oe})}{[h_{fe} - 2R_E h_{oe}]} \quad (2.61)$$

In practical cases,  $h_{oe}R_C \ll 1$ .

$$\frac{v_s}{I_L} = \frac{2R_E(1 + h_{fe}) + (R_s + h_{ie}) + (1 + 2R_E h_{oe})}{(h_{fe} - 2R_E h_{oe})}$$

$$\begin{aligned} \text{Therefore, } A_{cm} &= \frac{v_o}{v_s} = -\frac{I_L R_C}{v_s} \\ &= \frac{-(h_{fe} - 2R_E h_{oe}) R_C}{2R_E(1 + h_{fe}) + (R_s + h_{ie})(1 + 2R_E h_{oe})} \\ &= \frac{R_C(2R_E h_{oe} - h_{fe})}{2R_E(1 + h_{fe}) + (R_s + h_{ie})(1 + 2R_E h_{oe})} \end{aligned} \quad (2.62)$$

As shown in Fig. 2.43,  $h_{oe}$  is generally neglected in practical designs.

Therefore,

$$A_{cm} = \frac{-R_C h_{fe}}{R_s + h_{ie} + 2R_E (1 + h_{fe})} \quad (2.63)$$

Hence, unlike  $A_{dm}$ ,  $A_{cm}$  is the same for both balanced and unbalanced outputs.

**Common Mode Rejection Ratio (CMRR)** The differential amplifier is set to be operating in common mode configuration when the same voltage is applied to both the inputs, i.e.  $v_1 = v_2$ . One of the main requirements of the differential amplifier is to cancel or reject the noise signal that appears as a common input signal in both the input terminals of the differential amplifier. Hence a figure of merit called the Common Mode Rejection Ratio (CMRR) is introduced to define the ability of a differential amplifier to reject the common-mode input signal. The CMRR is defined as the ratio of the differential voltage gain  $A_{dm}$  to common-mode voltage gain  $A_{cm}$  and is generally expressed in terms of decibels. Therefore,

$$CMRR = 20 \log_{10} \left| \frac{A_{dm}}{A_{cm}} \right| \text{dB} \quad (2.64)$$

where  $A_{dm}$  is the differential-mode voltage gain and  $A_{cm}$  is the common-mode voltage gain. For an ideal differential amplifier,  $A_{cm} = 0$  and hence  $CMRR = \infty$ . In practical cases, since  $A_{dm} \gg A_{cm}$ , CMRR is high, though finite. Therefore,

$$\begin{aligned} v_o &= A_{dm}v_{id} + A_{cm}v_{ic} \\ &= A_{dm}v_{id} \left[ 1 + \frac{A_{cm}v_{ic}}{A_{dm}v_{id}} \right] \\ &= A_{dm}v_{id} \left[ 1 + \frac{1}{(A_{dm}/A_{cm})} \frac{v_{ic}}{v_{id}} \right] \\ v_o &= A_{dm}v_{id} \left[ 1 + \frac{1}{CMRR} \frac{v_{ic}}{v_{id}} \right] \end{aligned}$$

where CMRR is not expressed in dB. As  $CMRR \rightarrow \infty$ , the output voltage becomes

$$v_o = A_{dm}v_{id}$$

Here the common mode voltage is nullified to a greater extent. For a balanced case, substituting the results of  $A_{dm}$  and  $A_{cm}$ , we get

$$CMRR = 20 \log_{10} \left| \frac{R_s + h_{ie} + 2R_E (1 + h_{fe})}{R_s + h_{ie}} \right| \text{dB}$$

and for an unbalanced output,

$$CMRR = 20 \log_{10} \left| \frac{R_s + h_{ie} + 2R_E (1 + h_{fe})}{2(R_s + h_{ie})} \right| \text{dB}$$

**Input impedance  $R_i$**  The input impedance  $R_i$  is defined as the equivalent resistance existing between any one of the inputs and the ground, when the other input is grounded.

From Fig. 2.44,

$$R_i = \frac{v_s}{I_b} \quad (2.65)$$

For a single input,

$$R_i = R_s + h_{ie}$$

For dual input circuits,

$$R_i = 2(R_s + h_{ie}) \quad (2.66)$$

This input resistance is not dependent on whether the output is balanced or unbalanced.

**Output impedance  $R_o$**  The output impedance  $R_o$  is defined as the equivalent resistance existing between any one of the outputs and ground. Therefore, from Fig. 2.42, it is found that  $R_o = R_C$ . The common-mode gain decreases as  $R_o$  increases. Hence, the CMRR increases as  $R_o$  increases.

## Example 2.7

A differential amplifier has (i) CMRR=1000 and (ii) CMRR = 10000. The first set of inputs is  $v_1 = +100 \mu V$  and  $v_2 = -100 \mu V$ . The second set of inputs is  $v_1 = 1100 \mu V$  and  $v_2 = 900 \mu V$ . Calculate the percentage difference in output voltage obtained for the two sets of input voltages and also comment on this.

**Solution** In the first set,

$$v_{id} = v_1 - v_2 = [100 - (-100)] \mu V = 200 \mu V$$

$$v_{cm} = (1/2)(v_1 + v_2) = (1/2)[100 + (-100)] \mu V = 0$$

$$\begin{aligned} v_o &= A_{dm} v_{id} \left[ 1 + \frac{1}{CMRR} \frac{v_{ic}}{v_{id}} \right] \\ &= A_{dm} 200 \times 10^{-6} \left[ 1 + \frac{1}{1000} \frac{0}{200} \right] = 200 A_{dm} \mu V \end{aligned}$$

In the second set,

$$v_{id} = v_1 - v_2 = 1100 \mu V - 900 \mu V = 200 \mu V \quad (2.67)$$

$$v_{ic} = \frac{1}{2}(v_1 + v_2) = \frac{1}{2}(1100 + 900) \mu V = 1000 \mu V$$

$$\begin{aligned} \text{Hence, } v_o &= A_{dm} v_{id} \left[ 1 + \frac{1}{CMRR} \frac{v_{ic}}{v_{id}} \right] \\ &= A_{dm} 200 \times 10^{-6} \left[ 1 + \frac{1}{1000} \frac{1000}{200} \right] = 201 A_{dm} \mu V \end{aligned} \quad (2.68)$$

Comparing Eqs. (2.67) and (2.68), the output voltages for the two sets of input signals result in 0.5% difference.

Though the difference voltage  $v_{id} = 200 \mu V$  in both the cases, the output is not the same and hence the effect of common mode voltage  $v_{ic}$  has the same influence on the output voltage and it decreases with increase in CMRR.

When CMRR = 10000, a similar analysis as that of case (1) gives

$$v_o = 200 \times 10^{-6} A_{dm} \left( 1 + \frac{1}{10,000} \frac{1000}{200} \right) = 200.1 A_{dm} \mu V$$

Set 2—Same as case (1)

Here the output voltages differ by 0.05%. Hence, as the CMRR increases, the difference between the output voltages decreases.

### Example 2.8

Find the Q-point  $V_C$  and  $I_B$  for the differential amplifier shown in Fig. 2.45. Assume  $\beta = 100$ .

**Solution** The emitter current can be found by writing a loop equation starting at the base of  $Q_1$ .

$$V_{BE} + 2I_E R_E - V_{EE} = 0$$

$$I_E = \frac{V_{EE} - V_{BE}}{2R_E} = \frac{(15 - 0.7)}{2(65 \times 10^3)} = 110 \mu A$$

$$I_C = \alpha I_E = \frac{100}{101} I_E = \frac{100}{101} \times 110 \times 10^{-6} = 108.9 \mu A$$

$$I_B = \frac{I_C}{\beta} = \frac{108.9 \times 10^{-6}}{100} = 1.089 \mu A$$

$$V_C = V_{CC} - I_C R_C = 15 - (108.9 \times 10^{-6} \times 65 \times 10^3) = 7.922 V$$

$$V_{CE} = V_C - V_E = 7.922 - (-0.7) = 8.622 V$$

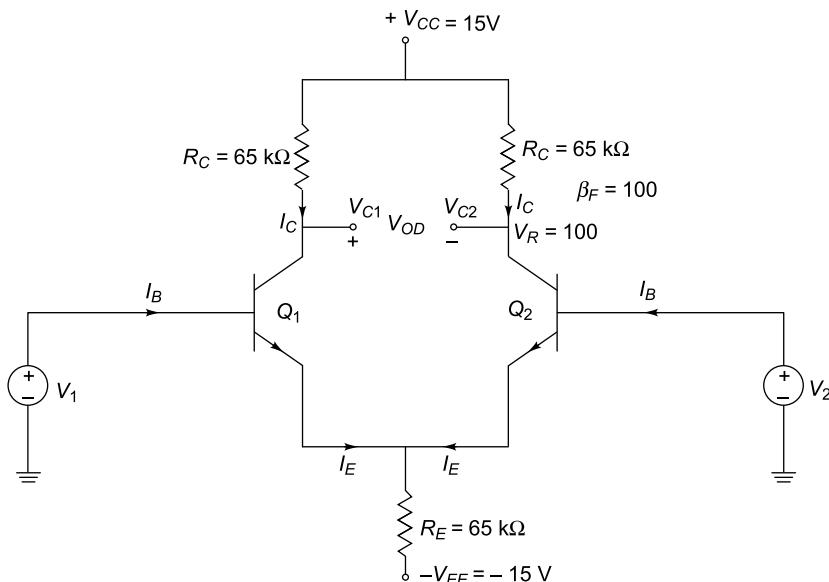


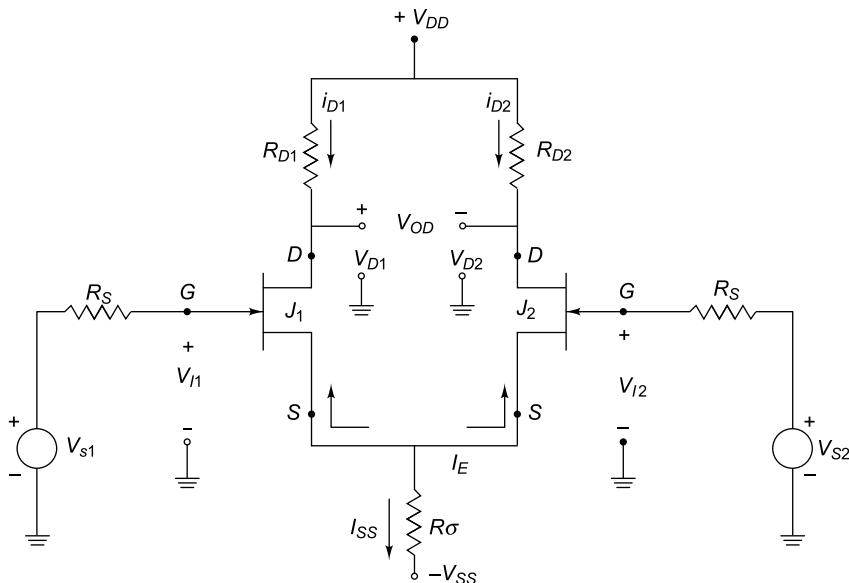
Fig. 2.45

Both the transistors of the differential amplifier are biased at the Q-point ( $108.9 \mu\text{A}$ ,  $8.622 \text{ V}$ ) with  $I_B = 1.089 \mu\text{A}$  and  $V_C = 7.922 \text{ V}$ . As  $V_{EE} \gg V_{BE}$ ,  $I_E$  can be approximated by  $I_E \approx \frac{V_{EE}}{2R_F} = \frac{15}{2 \times 65 \times 10^3} = 115.38 \mu\text{A}$ .

### 2.10.2 JFET Differential Amplifier

The JFET differential amplifier with resistive loading is considered below for the ac and dc analysis because JFET differential amplifier with active loading is quite complex. MOSFETs are widely used in the input stages of the differential amplifiers for better stability.

**JFET source-coupled pair: dc analysis** The source-coupled differential amplifier is shown in Fig. 2.46. The circuit is initially studied for its dc operation, which will be extended for the study of small signal model. Here  $J_1$  and  $J_2$  are assumed identical with matched drain resistors.



**Fig. 2.46** Source coupled differential amplifier

Considering the input loop, we get

$$V_{I1} = V_{GS1} - V_{GS2} + V_{I2}$$

We know that

$$V_{GS} = V_P \left( 1 - \sqrt{\frac{I_D}{I_{DSS}}} \right)$$

where  $I_D$  is the drain current,  $I_{DS}$  is the saturation drain current and  $I_{DSS}$  is the value of  $I_{DS}$  when  $V_{DG} = 0$  and  $V_P$  is the pinch-off voltage. The input differential voltage is

$$V_D = V_{D1} - V_{D2}$$

Considering  $J_1$  and  $J_2$  to be ideal,

$$V_{P1} = V_{P2}$$

and

$$I_{SS} = I_{D1} + I_{D2}$$

By mathematical analysis of the above equations, we get

$$I_{D1} = \frac{I_{SS}}{2} \left[ 1 - \frac{V_{ID}}{V_P} \sqrt{2 \left( \frac{I_{DSS}}{I_{SS}} \right) - \left( \frac{V_{ID}}{V_P} \right)^2 \left( \frac{I_{DSS}}{I_{SS}} \right)^2} \right]$$

$$\text{and } I_{D2} = \frac{I_{SS}}{2} \left[ 1 + \frac{V_{ID}}{V_P} \sqrt{2 \left( \frac{I_{DSS}}{I_{SS}} \right) - \left( \frac{V_{ID}}{V_P} \right)^2 \left( \frac{I_{DSS}}{I_{SS}} \right)^2} \right]$$

The above equations are graphed in Fig. 2.47 for the case  $I_{SS} = I_{DSS}$

$$\text{or } I_D = I_{DSS}/2.$$

These transfer functions resemble the corresponding result for the bipolar based differential amplifier with the linear region around  $V_{ID} = 0$  much wider for the JFET. However the JFET differential amplifier can handle much larger input signals than its bipolar counterpart, which is an important advantage.

From Fig. 2.46 we get the drain output voltage as

$$V_{D1} = V_{DD} - I_{D1} R_D$$

and

$$V_{D2} = V_{DD} - I_{D2} R_D$$

When  $R_{D1} = R_{D2} = R_D$ , the output differential voltage is given by

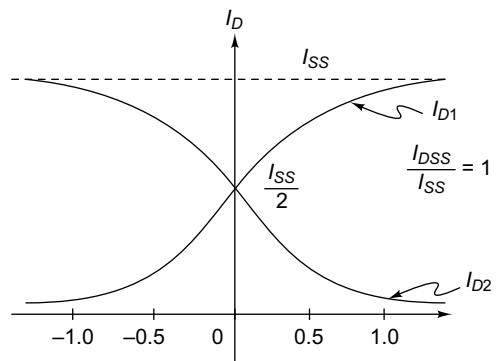
$$V_{OD} = (V_{DD} - I_{D1} R_D) - (V_{DD} - I_{D2} R_D) = -I_{D1} R_D + I_{D2} R_D$$

$$\text{Therefore, } V_{OD} = \frac{I_{SS} R_D V_{ID}}{V_P} \sqrt{2 \left( \frac{I_{DSS}}{I_{SS}} \right) - \left( \frac{V_{ID}}{V_P} \right)^2 \left( \frac{I_{DSS}}{I_{SS}} \right)^2}$$

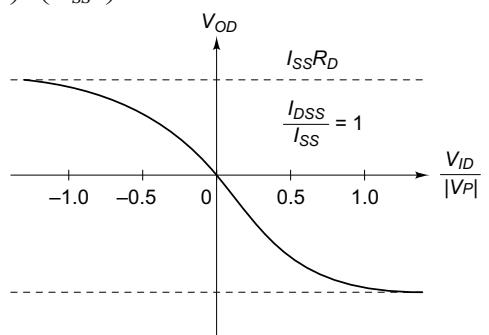
Again the output differential voltage is shown to be a function of the input differential voltage, and this is plotted in Fig. 2.48. For small  $V_{ID}$ , the transfer function is approximately linear.

The differential mode voltage gain is found by differentiating the above equation with respect to  $V_{ID}$  and letting  $V_{ID} = 0$ ,

$$A_{dm} = \left. \frac{dV_{OD}}{dV_{ID}} \right|_{V_{ID}=0} = \frac{I_{SS} R_D}{V_P} \sqrt{\frac{2 I_{DSS}}{I_{SS}}}$$



**Fig. 2.47** Source-coupled pair drain current as a function of the differential input voltage  $I_{SS} = I_{DSS}$



**Fig. 2.48** Differential output voltage of a common source amplifier as a function of the differential input voltage ( $I_{SS} = I_{DSS}$ )

$$\text{and } A_D = \frac{R_D}{V_P} \sqrt{2I_{SS}I_{DSS}}$$

At  $V_{ID} = 0$ ,  $I_{SS} = 2I_D$  (refer to Fig. 2.48) and since  $g_m = \frac{2}{V_P} \sqrt{I_D I_{DSS}}$ , we get

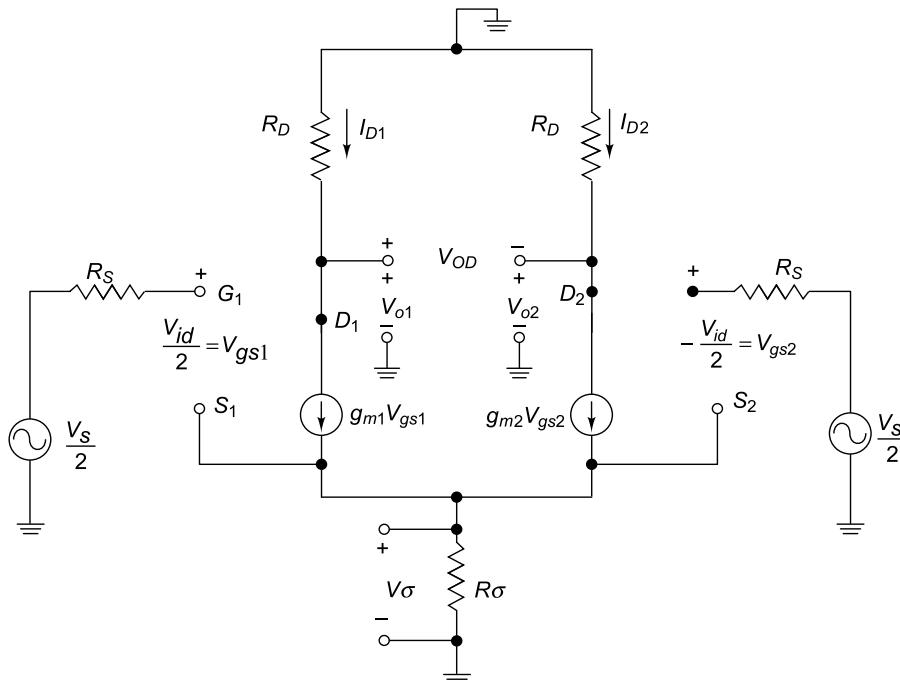
$$A_{dm} = -g_m R_D \quad (2.69)$$

This is the same as the voltage gain of a single ended common source amplifier, which means that there is zero dc voltage offset supplied as input to the next stage.

**JFET common-source amplifier—ac analysis** The small signal models for both BJT and FET based differential amplifiers are modelled using voltage-controlled current generators. However, the transconductance and output resistance have different physical basis and are computed differently. It should be noted that the FET input resistance is essentially infinite, but the manipulation of the model is the same.

Figure 2.49 shows the small signal representation of the JFET source-coupled amplifier. By applying a differential input voltage, the circuit can be simplified as shown in Fig. 2.50. However, the analysis part remains the same as that of BJT.

$$\text{Here, from Figs. 2.49 and 2.50, } A_{dm} = V_{od}/V_{id} = -g_m (R_D \parallel r_d)$$



**Fig. 2.49** Small signal mode with differential input

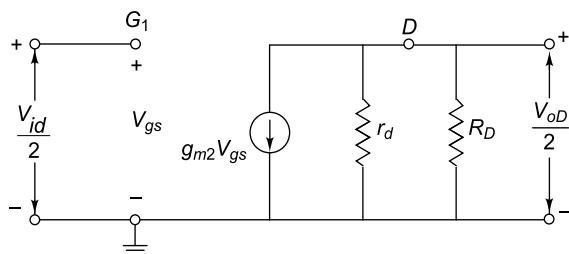


Fig. 2.50 Differential mode half-circuit model

### 2.10.3 Differential Amplifier using MOSFET

Figure 2.51 shows the basic circuit arrangement of a MOSFET differential pair, and the matched transistors \$M\_1\$ and \$M\_2\$ form the differential pair. Let us assume for analysis that \$M\_1\$ and \$M\_2\$ are always biased in the saturation region of their operation. They are biased with a constant current source \$I\_{SS}\$ as shown in Fig. 2.51. The differential amplifier uses the drain resistors \$R\_D\$ for load, though in practice, active loads are more common.

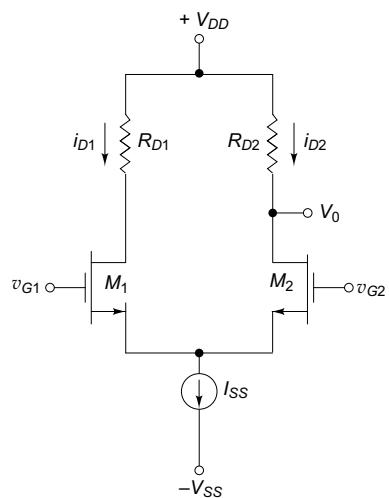


Fig. 2.51 Basic MOSFET differential pair configuration

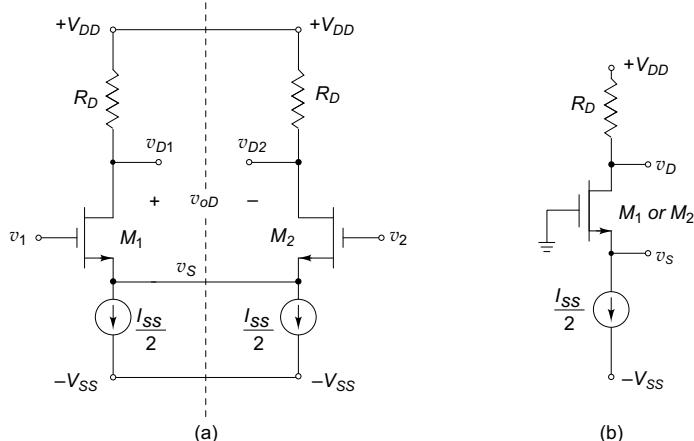
**dc transfer characteristics** The dc analysis of the MOSFET differential pair can be made using the circuit in Fig. 2.52(a) which is redrawn in symmetrical form. If the connections on the line of symmetry are replaced with open circuits and the two input voltages are set to zero, then the half-circuit needed for dc analysis is obtained as shown in Fig. 2.52(b). It is assumed that the output resistances of \$M\_1\$ and \$M\_2\$ are negligible and the two resistors are matched. Then, we have

$$I_{D1} = k_n (V_{GS1} - V_{Th})^2$$

and

$$I_{D2} = k_n (V_{GS2} - V_{Th})^2$$

Using Fig. 2.52(b) we know that the source current for the NMOS transistor is half of the bias current \$I\_{SS}\$.

Fig. 2.52 (a) MOSFET differential amplifier symmetric circuit representation  
(b) Half-circuit for dc analysis

That is,

$$I_{DS} = \frac{I_{SS}}{2}$$

The standard drain current formula for the transistor is given by

$$I_{DS} = \frac{k_n}{2} (v_{GS} - V_{Th})^2 \quad (2.70)$$

From the above equation, we get

$$V_{GS} = V_{Th} + \sqrt{\frac{2I_{DS}}{k_n}} = V_{Th} + \sqrt{\frac{I_{SS}}{k_n}}$$

The voltage at the source terminal is  $V_S = -V_{GS}$ . The voltages at the drain terminals  $V_{D1}$  and  $V_{D2}$  are given by

$$V_{D1} = V_{D2} = V_{DD} - I_{DS}R_D$$

and the output voltage across the terminals  $V_{D1}$  and  $V_{D2}$  is  $V_o = 0$ . Then, drain to source voltage is expressed by

$$V_{DS} = V_{DD} - I_{DS}R_D + V_{GS} \quad (2.71)$$

**ac analysis** Figures 2.53(a) and (b) show the differential mode and common mode half circuits obtained for the differential amplifier. In the differential mode circuit shown in Fig. 2.53(a) the source terminal of the MOSFETs represent a virtual ground. For the common mode circuit, the current source model is obtained as twice the small signal output resistance, which is the finite output resistance of the current source.

**differential mode input signal** The differential mode half circuit is a common source amplifier. The output voltages are given by

$$v_{d1} = -g_m R_D \frac{v_{id}}{2}$$

$$v_{d2} = +g_m R_D \frac{v_{id}}{2}$$

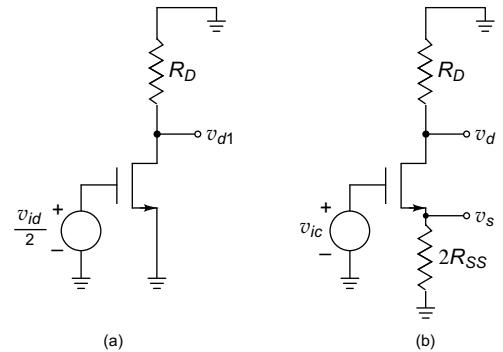
$$v_{od} = -g_m R_D v_{id}$$

The differential mode gain is

$$A_{dd} = \left. \frac{v_{od}}{v_{id}} \right|_{v_{ic}=0} = -\frac{g_m R_D v_{id}}{v_{id}} = -g_m R_D$$

A single ended output between any one of the drains and ground gives a gain of  $A_{dd}/2$ . Then, gain of the single ended output is

$$A_{dd1} = \left. \frac{v_{d1}}{v_{id}} \right|_{v_{ic}=0} = -\frac{g_m R_D}{2} = -\frac{A_{dd}}{2}$$



**Fig. 2.53** Half circuits for (a) Common-mode analysis, and (b) Differential mode analysis

$$A_{dd2} = \left. \frac{v_{d2}}{v_{id}} \right|_{v_{ic}=0} = +\frac{g_m R_D}{2} = +\frac{A_{dd}}{2}$$

The differential mode input resistance is given by  $R_{ID} = \infty$  and the differential mode output resistance is  $R_{OD} = 2R_D$ .

**Common-mode input signals** The common-mode half-circuit of Fig. 2.53(b) is the same as an inverting amplifier and its source resistance is  $2R_{SS}$

Then,  $v_{d1} = v_{d2} = \frac{-g_m R_D}{1 + 2g_m R_{SS}} v_{ic}$

The signal voltage at the source is given by

$$v_s = \frac{2g_m R_{SS}}{1 + 2g_m R_{SS}} v_{ic} \equiv v_{ic}$$

The common-mode voltage is applied to the circuit. Hence, the differential output voltage is zero.

$$v_{od} = v_{d1} - v_{d2} = 0$$

Therefore, common-mode conversion gain also is zero.

That is,  $A_{cd} = \frac{v_{od}}{v_{ic}} = 0$

When the output is taken across one of the drains, then the gain  $A_{cd}$  is given by

$$A_{cd} = \frac{v_{d1}}{v_{ic}} = \frac{-g_m R_D}{1 + 2g_m R_{SS}} \approx -\frac{R_D}{2R_{SS}} \quad (2.72)$$

The input current is zero and the common mode resistance  $R_{cm} = \infty$ .

**Common-mode rejection ratio (CMRR)** For common mode input signal, the output voltage of the differential amplifier is zero. Hence the CMRR is infinite. However, if a single ended output is taken from one of the drains, then the CMRR is given by

$$CMRR = \left| \frac{A_{dd}}{A_{cd}} \right| = \left| \frac{\frac{-g_m R_D}{2}}{-\frac{R_D}{2R_{SS}}} \right| = g_m R_{SS} \quad (2.73)$$

## 2.11 DIFFERENTIAL AMPLIFIERS WITH ACTIVE LOADS

Differential amplifiers are designed with active loads to increase the differential mode voltage gain.

The open circuit voltage gain of an op-amp is needed to be as large as possible. This is achieved by cascading the gain stages which increases the phase shift and the amplifier also becomes vulnerable to oscillations. The gain can be increased by using large values of collector resistance.

For such a circuit, the voltage gain is given by

$$A_{dm} = -g_m R_C = -\frac{I_C R_C}{V_T}$$

To increase the gain the  $I_C R_C$  product must be made very large. However, there are limitations in IC fabrication such as

- (i) a large value of resistance needs a large chip area
- (ii) for large  $R_C$ , the quiescent drop across the resistor increases and a large power supply will be required to maintain a given operating current
- (iii) large monolithic resistor introduces large parasitic capacitances which limits the frequency response of the amplifier
- (iv) for linear operation of the differential pair, the devices should not be allowed to enter into saturation. This limits the maximum input voltage that can be applied to the bases of transistors  $Q_1$  and  $Q_2$ , the base-collector junction must be allowed to become forward-biased by more than

0.5 V. The large value of load resistance produces a large dc voltage drop  $\left(\frac{I_{EE}}{2}\right)R_C$ , so that the collector voltage will be  $V_C = V_{CC} - \left(\frac{I_{EE}}{2}\right)R_C$  and it will be substantially less than the supply voltage  $V_{CC}$ . This will reduce the input voltage range of the differential amplifier.

Due to the reasons cited above, an active load is preferred in the differential amplifier configurations.

### 2.11.1 BJT Differential Amplifiers using Active Loads

A simple active load circuit for a differential amplifier is the current mirror active load as shown in Fig. 2.54. The active load comprises transistors  $Q_3$  and  $Q_4$  with the transistor  $Q_3$  connected as a diode with its base and collector shorted. The circuit is shown to drive a load  $R_L$ .

When an ac input voltage is applied to the differential amplifier, the various currents of the circuit are given by

$$I_{C4} = I_{C3} = I_{C1} = (g_m V_{id})/2$$

where  $I_{C4} = I_{C3}$  due to current mirror action. Here,  $I_{C2}$  is given by

$$I_{C2} = -(g_m V_{id})/2$$

We know that the load current  $I_L$  entering the next stage is

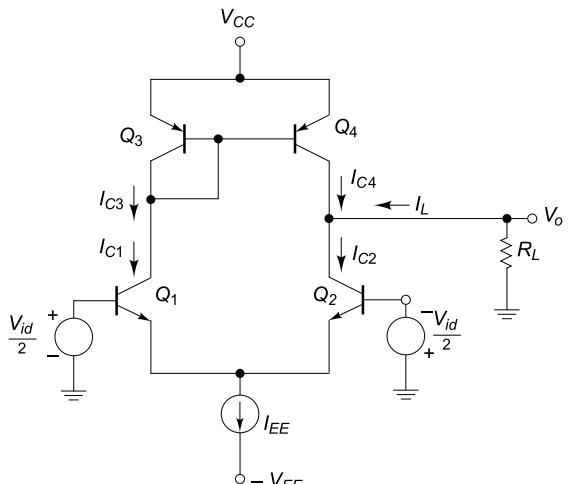
$$I_L = I_{C2} - I_{C4}$$

Therefore,

$$I_L = -(g_m V_{id})/2 - (g_m V_{id})/2 = -g_m V_{id}$$

Then, the output voltage from the differential amplifier is given by

$$V_o = -I_L R_L = -(-g_m V_{id}) R_L = g_m R_L V_{id}$$



**Fig. 2.54** Bipolar differential amplifier with current mirror active load

The ac voltage gain of the circuit is given by

$$A_V = \frac{V_o}{V_{id}} = \frac{(g_m R_L V_{id})}{V_{id}} = g_m R_L \quad (2.74)$$

The differential amplifier can amplify the differential input signals and it provides single-ended output with a ground reference since the load  $R_L$  is connected to only one output terminal. This is made possible by the use of the current mirror active load.

The output resistance  $R_o$  of the circuit is that offered by the parallel combination of transistors  $Q_2$  (*NPN*) and  $Q_4$  (*PNP*). It is given by

$$R_o = r_{o2} || r_{o4} \quad (2.75)$$

### Analysis of BJT Differential Amplifier with Active Load

Assuming  $V_{id}/2 = 0$  for transistor  $Q_1$  and  $Q_2$  and  $\beta = \infty$ , then the bias current  $I_{EE}$  is divided equally between  $Q_1$  and  $Q_2$ , and hence,  $I_{C1} = I_{C2} = I_{EE}/2$ . The current  $I_{C1}$  supplied by  $Q_3$  is mirrored as  $I_{C4}$  at the output of transistor  $Q_4$ .

Therefore,  $I_{C3} = I_{C4} = I_{EE}$  and the dc current in the collector of  $Q_4$  is exactly the current needed to satisfy  $Q_2$ .

When  $\beta$  is very large and  $V_{EC4} = V_{EC3} = V_{BE}$ , the *current mirror ratio* becomes exactly unity. Then, the differential amplifier is completely balanced, and the output voltage is  $V_o = V_{CC} - V_{BE}$ .

**Q-points** The collector currents of all the transistors are equal. That is,  $I_{C1} = I_{C2} = I_{C3} = I_{C4} = \frac{I_{EE}}{2}$ . The collector-emitter voltages of  $Q_1$  and  $Q_2$  are given by

$$V_{CE1} = V_{CE2} = V_C - V_E = (V_{CC} - V_{EB}) - (-V_{EB}) \approx V_{CC}$$

The collector-emitter voltages of  $Q_3$  and  $Q_4$  are given by,

$$V_{CE3} = V_{EC4} = V_{EB}$$

The input offset voltage  $V_{OS}$  of the differential amplifier arises from the mismatches in the input devices  $Q_1$ ,  $Q_2$  and load devices  $Q_3$ ,  $Q_4$  and from the base currents of the load devices.

An approximate expression for  $V_{OS}$  is given by

$$V_{OS} \cong V_T \left( \frac{\Delta I_{SP}}{I_{SP}} - \frac{\Delta I_{SN}}{I_{SN}} + \frac{2}{\beta} \right) \quad (2.76)$$

where  $\beta$  represents the gain of *PNP* transistor and it is assumed that

$$\Delta I_{SP} = I_{S3} - I_{S4}$$

$$I_{SP} = \left( \frac{I_{S3} + I_{S4}}{2} \right)$$

$$\Delta I_{SN} = I_{S1} - I_{S2}$$

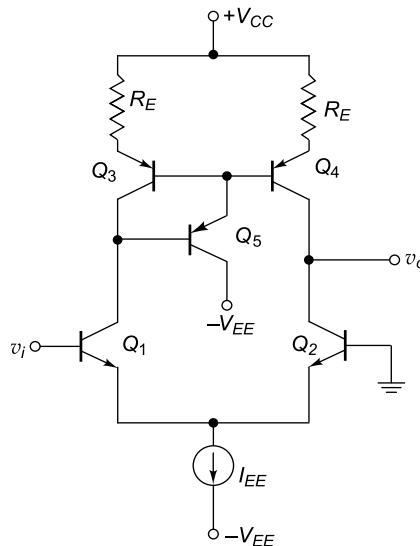
and

$$I_{SN} = \left( \frac{I_{S1} + I_{S2}}{2} \right)$$

Assuming a worst case value of  $\pm 4\%$  for  $\frac{\Delta I_S}{I_S}$  and  $\beta$  of 20,

$$V_{OS} = V_T (0.04 + 0.04 + 0.1) = 26 \times 10^{-3} \times 0.18 \cong 4.68 \text{ mV} \quad (2.77)$$

Equation (2.77) shows that, the offset is higher than that of a resistive loaded differential amplifier. This can be reduced by the use of emitter resistors for  $Q_3$  and  $Q_4$ , and a transistor  $Q_5$  in the current mirror load as shown in Fig. 2.55.

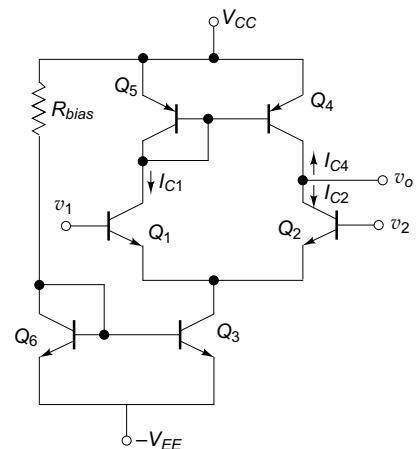


**Fig. 2.55** Improved differential circuit using active load

**CMRR of the differential amplifier using active load** The differential amplifier using active load provides high voltage gain to the differential input signal and a single-ended output that is referenced to the ground is obtained. The differential amplifier which provides conversion for a differential signal to a single-ended signal is necessary in differential input and single-ended output amplifiers. The op-amp is one such circuit.

Figure 2.56 shows the differential-to-single-ended conversion circuit. The changes in the common-mode signal of input cause change in the bias current  $I_{EE}$ , due to the finite output resistance of the bias current source. This induces a change in  $I_{C2}$  and an identical change in  $I_{C1}$ . The change in  $I_{C1}$  will then produce a change in the PNP load devices, and thereby a change in  $I_{C4}$ , which is the collector current  $Q_4$ . The current  $I_{C4}$  is in such a direction as to cancel the change in  $I_{C2}$ . As a result of this, any common-mode input does not cause a change in output.

The voltage gain of the differential amplifier is independent of the quiescent current  $I_{EE}$ . This makes it possible to use very small value of  $I_{EE}$  as low as  $20 \mu\text{A}$ , while still maintaining a large voltage gain. Small value of  $I_{EE}$  is preferred, since it results in a small value of bias current and a large value for the input resistance. A limitation in choosing a small  $I_{EE}$  is, however, the fact that, it will result in a poor frequency response of the amplifier.



**Fig. 2.56** Differential to single ended conversion with active load

When a small value of bias current is required, the best approach is to use a JFET or MOSFET differential amplifier that is operated at comparatively higher values of  $I_{EE}$ .

**Differential mode signal analysis** The ac analysis of the differential amplifier can be made using the circuit model shown in Fig. 2.57. The differential input transistor pair produces equal and opposite currents whose amplitude is given by  $g_{m2}v_{id}/2$  at the collectors of  $Q_1$  and  $Q_2$ . The collector current  $i_{C1}$  is fed by the transistor  $Q_3$  and it is mirrored at the output of  $Q_4$ . Therefore, the total current  $i_o$  flowing through the load resistor  $R_L$  is given by

$$i_o = 2 \frac{g_{m2}v_{id}}{2} = g_{m2}v_{id}$$

Then, the output voltage is

$$v_o = i_o R_L = (g_{m2}R_L)v_{id}$$

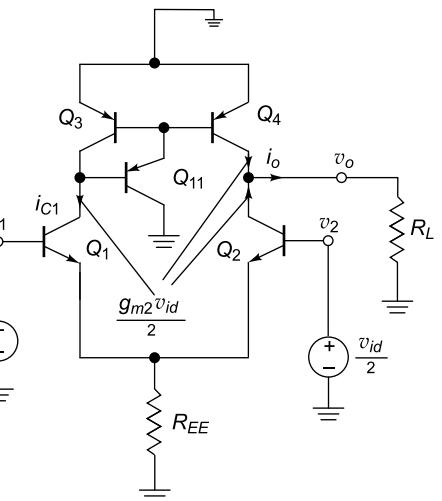
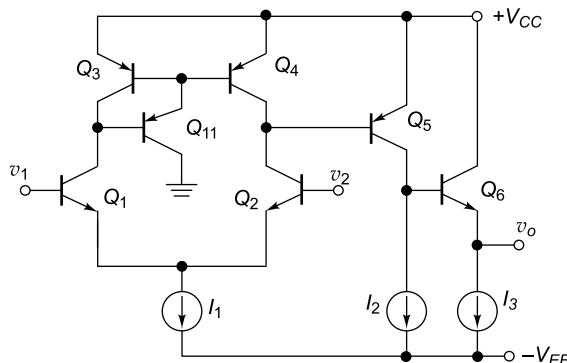
and the differential mode gain  $A_{dd}$  of the differential amplifier is given by

$$A_{dd} = \frac{v_o}{v_{id}} = g_{m2}R_L \quad (2.78)$$

This current mirror provides a single-ended output which has a voltage equal to the maximum gain of the common emitter amplifier.

The power of the current mirror can be increased by including additional common collector stages at the output of the differential input stage. A bipolar differential amplifier structure with additional stages is shown in Fig. 2.58. The resistance at the output of the differential stage is now given by the parallel combination of transistors  $Q_2$  and  $Q_4$  and the input resistance is offered by  $Q_5$ . Then, the equivalent resistance is expressed by

$$R_{eq} = r_{o2} \parallel r_{o4} \parallel r_{i5} \approx r_{i5}$$



**Fig. 2.57** BJT differential amplifier with differential mode input

**Fig. 2.58** BJT differential amplifier with additional output stages

The gain of the differential stage then becomes

$$A_{dm} = g_{m2} R_{eq} = g_{m2} r_{i5} = \beta_{o5} \frac{I_{C2}}{I_{C5}} \quad (2.79)$$

**Bipolar differential amplifier with common mode input signals** Figure 2.59 shows the bipolar differential amplifier applied with a common mode input signal. The common mode input signal induces a common mode current  $i_{ic}$  in each of the differential transistor pair  $Q_1$  and  $Q_2$ . The common current  $i_{ic}$  is given by

$$i_{ic} = \frac{g_{m2}}{1 + 2g_{m2}R_{EE}} v_{ic} \approx \frac{v_{ic}}{2R_{EE}}$$

The current flow through the transistor  $Q_1$  is supplied by the reference current of transistor  $Q_3$ . This current is replicated or mirrored in the transistor  $Q_4$  and it produces exactly the same current needed at the collector of  $Q_2$ . Therefore, the output current and hence the output voltage and common mode conversion gain  $A_{cd}$  are all zero.

However, for an actual amplifier, the common mode gain is determined by small imbalances generated in the bipolar transistor fabrication and the overall asymmetry in the amplifier. One of the main factors is due to the current gain defect in the active load, and it can be minimised through the use of buffered current mirror using the transistor  $Q_5$  as shown in Fig. 2.59.

## 2.11.2 MOSFET Differential Amplifiers using Active Loads

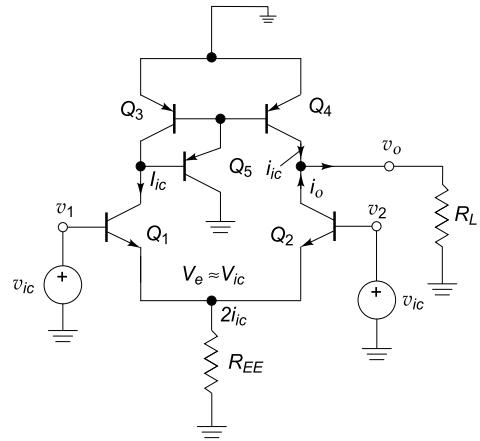
Figure 2.60 shows a MOSFET differential amplifier with an active load using P-MOSFET devices. The transistors  $M_1$  and  $M_2$  are the NMOS devices forming the differential pair biased with the current  $I_{SS}$ . The transistors  $M_3$  and  $M_4$  are P Channel devices configured as a current mirror and they act as the load devices. The single-ended output is taken from the common-drain junction of  $M_2$  and  $M_4$ . When a common-mode voltage of  $v_1 = v_2 = v_{cm}$  is applied to the circuit, the current  $I_{SS}$  divides evenly between  $M_1$  and  $M_2$ . Therefore, the drain currents are given by

$$i_{D1} = i_{D2} = I_{SS}/2$$

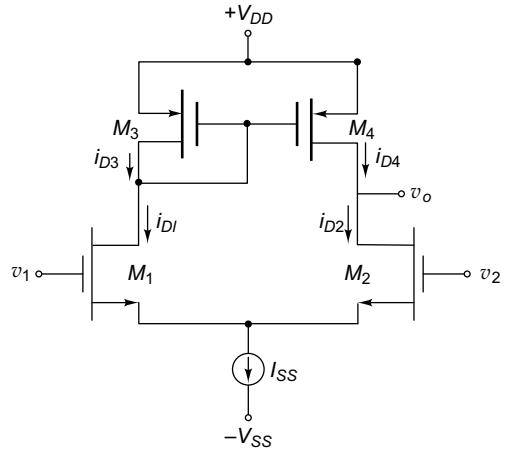
Since there are no gate currents,

$$i_{D3} = i_{D1} \text{ and } i_{D4} = i_{D2}$$

A single-ended output is taken from the drain junction of  $M_2$  and  $M_4$ . When a common-mode signal of  $v_1 = v_2$  is applied to the circuit, the current  $I_{SS}$  divides equally between  $M_1$  and  $M_2$ . Then, the drain currents are  $i_{D1} = i_{D2} = I_{SS}/2$ . Since the gate currents are zero,  $i_{D3} = i_{D1}$  and  $i_{D4} = i_{D2}$ . When a small differential mode input voltage of value  $v_{id} = v_1 - v_2$  is applied, then the drain currents are given by



**Fig. 2.59** BJT differential amplifier with common-mode input



**Fig. 2.60** MOSFET differential amplifiers using active loads

$$i_{D1} = \frac{i_{SS}}{2} + i_D \text{ and } i_{D2} = \frac{i_{SS}}{2} - i_D \quad (2.80)$$

Then, the current mirror formed by  $M_3$  and  $M_4$  mirrors the current as given by

$$i_{D4} = i_{D3} = \frac{i_{SS}}{2} + i_D$$

Figure 2.61 shows the ac equivalent circuit with active load marked with the signal currents. The current  $i_{D2}$  is shown negative as given in Eq. (2.80).

Figure 2.62(a) shows the small signal equivalent circuit at the drain junction of  $M_2$  and  $M_4$ . When the output of a MOSFET is connected to the gate of another MOSFET which is equivalent to infinite impedance for low frequency signals, the output terminal is effectively an open circuit. Therefore, the circuit can be rearranged with a common point joining the signal currents as shown in Fig. 2.62(b). Therefore,

$$v_o = 2 \left( \frac{g_m v_d}{2} \right) (r_{o2} \| r_{o4})$$

The small signal differential mode voltage gain is given by

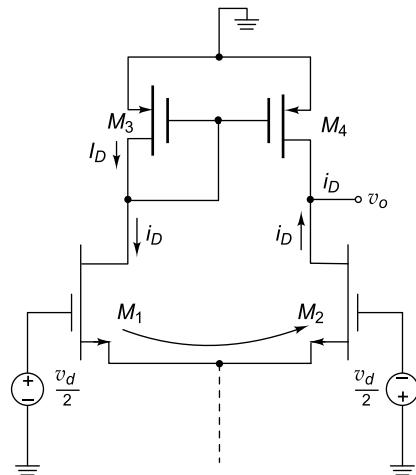
$$A_{dm} = \frac{v_o}{v_{id}} = g_m (r_{o2} \| r_{o4})$$

or

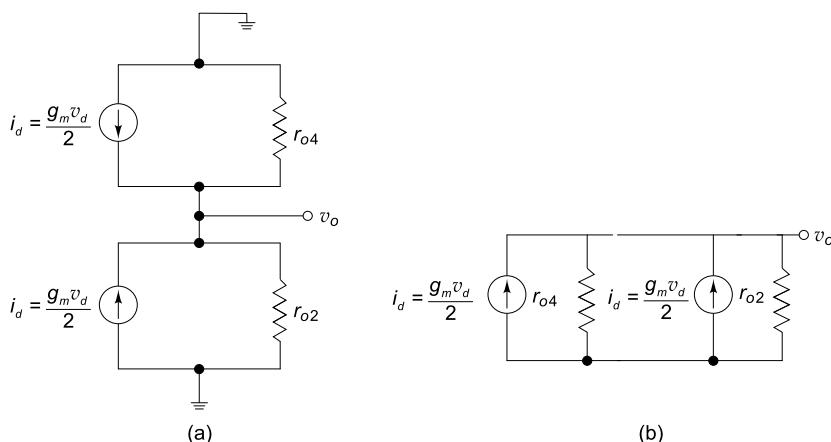
$$A_{dm} = \frac{g_m}{\left( \frac{1}{r_{o2}} + \frac{1}{r_{o4}} \right)} = \frac{g_m}{g_{o2} + g_{o4}}$$

where

$$g_m = 2\sqrt{k_n I_D} = \sqrt{2k_n I_{SS}}$$



**Fig. 2.61** AC equivalent circuit of MOSFET differential amplifier with active load



**Fig. 2.62** (a) Small signal equivalent circuit and (b) Rearranged equivalent circuit

## Example 2.9

Find the *Q*-point for the MOSFETs in the differential amplifier shown in Fig. 2.63 with  $V_{DD} = -V_{SS} = 12$  V,  $I_{SS} = 175 \mu A$ ,  $R_D = 65 k\Omega$ ,  $k_n = 3 mA/V^2$  and  $V_{Th} = 1V$ . What is the maximum  $V_{ic}$  for which  $M_1$  remains saturated?

### Solution

$$I_{DS} = \frac{I_{SS}}{2} = \frac{175}{2} \mu A = 87.5 \mu A$$

$$V_{GS} = V_{Th} + \sqrt{\frac{I_{SS}}{k_n}} = 1 + \sqrt{\frac{175 \times 10^{-6}}{3 \times 10^{-3}}} = 1.242 \text{ V}$$

$$V_{DS} = V_{DD} - I_{DS}R_D + V_{GS}$$

$$= 12 - (87.5 \times 10^{-6})(65 \times 10^3) + 1.242 = 7.55 \text{ V}$$

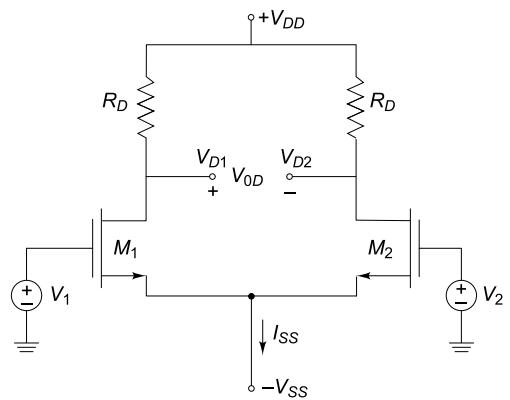
Since  $V_{GS} - V_{Th} = 0.242$  V, the necessary saturation condition of MOSFET, which is given by  $(V_{DS} = 7.55 \text{ V}) \geq 0.242 \text{ V}$  is satisfied. Both the transistors of the differential amplifier are biased at the *Q*-point of (87.5  $\mu$ A, 7.55 V).

Requirement of saturation for  $M_1$  for nonzero  $V_{ic}$  necessitates

$$V_{GD} = V_{ic} - (V_{DD} - I_{DS}R_D) \leq V_{Th}$$

$$\begin{aligned} V_{ic} &\leq V_{DD} - I_{DS}R_D + V_{Th} \\ &= 12 - (87.5 \times 10^{-6})(65 \times 10^3) + 1 = 7.31 \text{ V} \end{aligned}$$

Therefore,  $V_{ic} \leq 7.31 \text{ V}$ .



**Fig. 2.63**

## SUMMARY

- The major blocks of operational amplifiers are differential amplifier, intermediate gain stage(s), dc level shifters and output stages.
- The basic current source is the two-transistor current mirror used as an active load, due to its high ac resistance. The dynamic output conductance is  $g_m = \frac{\Delta I_o}{\Delta V_o} = \frac{I_o}{V_A} = \frac{1}{r_o}$  where  $V_A$  is the Early voltage. The reference and load currents are within 1.5% of each other in simple current source.
- Widlar current source has improved current source characteristics with capability to feed current values down to 5  $\mu$ A. It uses a reference current as given by  $I_{ref} \approx I_{C1} \left(1 + \frac{1}{\beta}\right)$  resulting in  $I_{C1} = I_{ref} \left(\frac{\beta}{1 + \beta}\right)$ .
- The simple current mirror can be used for supplying more than a single load. Such a circuit is called a current repeater or multiple current source and the reference current is  $I_{ref} = I_C + \left(1 + \frac{N}{\beta}\right) I_C$ . The ratio

of the maximum to minimum value of collector current obtained by this method is around 10 and the fabrication processes limit the ratio.

- Wilson current source achieves higher resistance than the output resistance  $r_o$  of simple current source and it has much larger Thevenin's voltage than the Early voltage. For the Wilson current source,

$$I_{C3} = I_{ref} \left( 1 - \frac{2}{\beta^2 + 2\beta + 2} \right).$$

- Widlar current source is useful for small output currents and Wilson current source is preferable for higher output resistance and lower sensitivity to transistor base currents. The latter has a greater degree of supply independence and wider ranges of current mirror values are obtainable by selecting emitter area ratios.
- The Widlar and Wilson current sources are more stable against variations in  $\beta$ .
- The performance metric to define the dependence of current on power supply is denoted by  $S_{V_{CC}}^{I_o}$  and it is the fractional change in the output current that results from a given fractional change in supply voltage

$$\text{and } S_{V_{CC}}^{I_o} = \frac{V_{CC}}{R} \times \frac{R}{V_{CC} - V_{BE}} \approx 1.$$

- The variation of the output current with respect to temperature expressed as the fractional change in output current per degree centigrade of temperature variation is called the temperature coefficient  $TC_F$  and it is  $TC_F = \frac{1}{I_o} \times \frac{\partial I_o}{\partial T}$ .
- The current source employing thermal voltage  $V_T$  has the temperature coefficient  $TC_F = \frac{1}{V_T} \times \frac{\partial V_T}{\partial T} - \frac{1}{R_3} \frac{\partial R_3}{\partial T}$ .
- The reference circuits using  $V_{BE}$  and  $V_T$  have high value of temperature coefficient of output current. This difficulty can be overcome by using the Zener diode as a reference and the bandgap reference design.
- The basic two transistor NMOS current source has the load current  $I_o$  defined by

$$I_o = \left( \frac{W}{L} \right) \left( \frac{1}{2} \mu_n C_{ox} \right) (V_{GS2} - V_{Th})^2.$$

- The MOSFET current sources require a large output resistance for good stability. This output resistance can be enhanced by the use of cascode current mirror.
- Current sources using JFETs are fundamental elements in JFET ICs and the output resistance looking into the drain terminal is  $\frac{1}{r_o} = \frac{di_D}{dv_{DS}} = \lambda I_{DS}$ .
- Power supply independence can be achieved by the use of threshold voltage  $V_{Th}$ , the difference between the threshold voltages of dissimilar devices  $\Delta V_{Th}$ , the base-emitter voltage  $V_{BE}$  of the parasitic bipolar transistor in CMOS technology, thermal voltage  $V_T$  or the bandgap voltage  $V_{GO}$  of silicon (=1.205V).
- Current source circuit using self-biased threshold reference bias has  $I = \frac{V_{Th}}{R}$  with the limitations of
  - $V_{Th}$  cannot be controlled effectively and typical  $V_{Th}$  is in the range of 0.4V to 0.8V
  - $V_{Th}$  displays a negative temperature coefficient ( $TC$ ) of about  $-2mV/^{\circ}C$ , whereas the diffused resistors have positive temperature coefficient that results in output current having a large negative temperature coefficient
- The current source employing  $V_{Th}$  reference offers much smaller  $TC$  of the output current than the  $V_{BE}$  reference. Its primary advantage is that the positive  $TC$  of  $V_T$  in combination with the positive  $TC$  of the resistor tends to cancel each other resulting in a relatively temperature independent output current.
- Normally  $V_{BE}$  is a parameter that is relatively well-controlled. However, it exhibits a negative temperature coefficient ( $TC$ ) of about  $-2mV/^{\circ}C$ . This factor combined with the strong positive  $TC$  of the diffused and polysilicon resistors result in a strong negative  $TC$  in the resulting bias current.

- ❑ Voltage source produces an output voltage  $V_o$ , which is independent of the load driven by the voltage source, or the output current supplied to the load and it is the circuit dual of the constant current source.
- ❑ Two methods used to produce a voltage source are

- Using impedance transforming properties of the transistor, which in turn determines the current gain of the transistor
- Using an amplifier with negative feedback

- ❑ Emitter-follower or common-collector type voltage source is suitable for the differential gain stage used in op-amps and it has the advantages of producing low ac impedance resulting in effective decoupling of adjacent gain stages.
- ❑ Voltage source using the breakdown voltage of the base-emitter junction overcomes the limitations of the vulnerability for changes in bias voltage  $V_N$  and the output voltage  $V_o$  with respect to changes in supply voltage  $V_{CC}$ . The output resistance  $R_o$  looking into the output terminal is  $R_o = R_B + \frac{V_T}{I_1}$  where  $R_B$  and

$V_T/I_1$  are the ac resistances of the base-emitter resistance of diode  $D_B$  and diode  $D_1$  respectively. Typical value of  $V_o$  is in the range of 6.5 V to 9 V.

- ❑ Stabilised bias voltage source can be obtained using a forward-biased diode-connected transistor whose ac output resistance is  $R_o \approx \frac{V_o}{V_{BE}} \frac{1}{g_m} = \frac{V_o}{V_{BE}} \frac{V_I}{I_C}$ .

- ❑ The most important characteristic of a voltage reference is the temperature co-efficient of the output reference voltage  $TC_R$  expressed as  $TC_R = \frac{dV_R}{dT}$ .

- ❑ The desirable properties of a voltage reference are:

  - it must be independent of any temperature change
  - it must have good power supply rejection
  - output voltage must be independent of the loading of output current

- ❑ The voltage reference circuit biases the voltage source circuit, and the combination can be called as the voltage regulator. The basic design strategy of a voltage reference circuit is producing a zero  $TC_R$  at a given temperature, and thereby achieving good thermal stability. Temperature stability of the order of 100 ppm/ $^{\circ}\text{C}$  is typically expected.

- ❑ Voltage reference circuit using temperature compensation scheme uses the close thermal coupling achievable in monolithic IC design and this compensates the known thermal drifts by introducing an opposing and compensating drift source of equal magnitude.

- ❑ Voltage Reference Circuit using Avalanche Diode Reference uses the breakdown phenomenon of a heavily doped  $PN$  junction. The breakdown in the junctions of the integrated transistor is mainly due to avalanche multiplication and the avalanche breakdown voltage  $V_B$  incurs a positive temperature coefficient, typically in the range of 2 mV/ $^{\circ}\text{C}$  to 5 mV/ $^{\circ}\text{C}$ . Zero temperature coefficient of  $I_o$  is obtained by satisfying

$$\frac{1}{I_o} \frac{\partial I_o}{\partial T} = 0 = \frac{1}{R_2 I_o} \left[ \frac{\partial V_B}{\partial T} - (n+2) \frac{\partial V_{BE}}{\partial T} \right] - \frac{1}{R_2} \frac{\partial R_2}{\partial T}. \quad \text{The lowest voltage temperature compensated}$$

avalanche diode is 6.2 V. When the supply voltage is 6 V or less, the reference voltage is developed from the energy bandgap voltage  $V_{GO}$  of the semiconductor material, which is 1.205 V for silicon. Condition for

$$\text{a zero temperature coefficient is obtained by satisfying the condition } TC_{V(BE)} = \frac{dV_R}{dT} = \frac{V_{BE} - (V_{GO} + 3V_T)}{T} +$$

$$\frac{R_2}{R_3} \frac{k}{q} \ln \frac{I_1}{I_2}$$

The bandgap reference source, operating under zero  $TC_{V(\text{ref})}$ , gives an output voltage of 1.283 V the energy bandgap value  $V_{GO} = 1.205$  V (for silicon) determines  $V_R$ .

- M113 uses a bandgap reference of 1.2V and its voltage changes by 0.5% with temperature. Laser trimmed thin-film of resistors provide minimum  $TC$  of the order of a few  $\mu\text{V}/^\circ\text{C}$ .
- Level shift stages are needed when a number of gain stages are cascaded for larger gain values which result in shifting of the output dc level towards the negative supply. Level shift stages avoid poor linearity and amplitude limitation or clipping of output voltage swing. They also help in preventing inter-stage loading effects with its inherent characteristics of high input impedance and relatively low output impedance values.
- The differential amplifier amplifies the difference between two signals and this forms the basic input stage of an integrated amplifier. The main aim in its design is to minimise the effect of common mode input signal.
- The important properties of differential amplifier are:
  - Excellent stability
  - High versatility
  - High immunity to interference signals
- The differential amplifier which is one of the building blocks of op-amp has the advantages of lower cost and easier fabrication as a closely matched IC component.
- Differential amplifier amplifies the difference between two input signals and it can be biased using emitter bias or a constant current source.
- The bipolar and MOSFET differential amplifier using active load present higher differential-mode voltage gain, with the bipolar differential amplifier exhibiting a larger voltage gain than the later, and the later possessing an advantage of infinite input impedance at low frequencies over the former.
- The Common Mode Rejection Ratio (CMRR) is a *figure of merit* and it indicates the ability of the differential amplifier in rejecting the common-mode input signal. CMRR is defined as the ratio of the differential voltage gain  $A_{dm}$  to common-mode voltage gain  $A_{cm}$  and is generally expressed in terms of decibels as given by  $CMRR = 20 \log_{10} \left| \frac{A_{dm}}{A_{cm}} \right| dB$  where  $A_{dm}$  is the differential-mode voltage gain and  $A_{cm}$  is the common-mode voltage gain.
- For an ideal differential amplifier,  $A_{cm} = 0$  and  $CMRR = \infty$ . In practical cases, since  $A_{dm} \gg A_{cm}$ , CMRR is high though finite.
- The input impedance  $R_i$  is the equivalent resistance existing between any one of the inputs and the ground when the other input is grounded and it is given by  $R_i = 2(R_s + h_{ie})$ .
- The output impedance  $R_o$  is the equivalent resistance existing between any one of the outputs and ground. The CMRR increases as  $R_o$  increases.
- MOSFETs are widely used in the input stages of the differential amplifiers for their better stability characteristics.
- The differential mode voltage gain of the JFET source-coupled amplifier is given by

$$A_{dm} = V_{od} / V_{id} = -g_m (R_D \parallel r_d).$$

- Common-Mode Rejection Ratio (CMRR) of MOSFET differential amplifier is

$$CMRR = \left| \frac{A_{dd1}}{A_{cd}} \right| = \left| \frac{\frac{-g_m R_D}{2}}{-\frac{R_D}{2R_{SS}}} \right| = g_m R_{SS}.$$

- The differential amplifier using active load provides high voltage gain to the differential input signal.

- When the output of a MOSFET is connected to the gate of another MOSFET, it is equivalent to infinite impedance for low frequency signals and the output terminal is effectively an open circuit.

## REVIEW QUESTIONS

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1. What are the basic building blocks of an op-amp?
2. List some important circuit configurations used in linear ICs.
3. Draw the ideal output current characteristics of a current source and explain.
4. What is a current mirror and why is it called so?
5. What are the advantages and applications of a current source?
6. What is the use and advantage of an active load?
7. Why is the current mirror circuit used in differential amplifier stages?
8. Draw a circuit for a constant current source and explain its operation.
9. Draw the output characteristics of a practical current source and comment on the shape of the waveform.
10. Draw the Thevenin's and Norton's equivalent circuit representations of a current source. Explain the parameters involved.
11. Design a current source of Fig. 2.4 to provide an output current of  $200 \mu\text{A}$ . Assume  $V_{CC} = 12 \text{ V}$ ,  $V_{BE(ON)} = 0.7 \text{ V}$ ,  $\beta = 200$ . Assume Early voltage  $V_A$  is  $\infty$ .
12. Explain the operation of a Widlar current source with a neat diagram.
13. For Widlar current source assume that  $V_{CC} = 12 \text{ V}$ ,  $R_1 = 15 \text{ k}\Omega$  and  $V_{BE(ON)} = 0.7 \text{ V}$  Find the value of  $R_2$  to be connected to produce a current  $I_{C2}$  of  $10 \mu\text{A}$ .
14. Draw the circuit of a multiple current source and explain its operation.
15. For the circuit shown in Fig. 2.8, assume  $R_1 = 10 \text{ k}\Omega$ ,  $\beta = 200$ ,  $V_{CC} = 12 \text{ V}$  and  $V_{BE} = 0.65 \text{ V}$ . Determine the values of  $I_{C1}$ ,  $I_{C2}$  and  $I_{C3}$ .
16. Explain the Wilson current source with a neat circuit diagram.
17. Discuss the operation of a multiple output transistor current source.
18. What is the effect of supply voltage variations on the current sources?
19. Define a performance metric to represent the effect of supply voltage variation on the current source.
20. Why is the Widlar source said to have good power supply insensitivity? Justify.
21. Draw the circuit of power supply independent bias circuit using the Widlar source.
22. Explain BJT current sources using  $V_{BE}$  and  $V_T$  based references.
23. How is the thermal voltage  $V_T$  used as a standard? Explain.
24. Comment on the temperature dependent characteristics of current source.
25. Explain the operation of a current source using FETs with a neat diagram.
26. Explain the operation of MOSFET cascode current mirror with the circuit diagram.
27. Explain the Wilson current source using MOSFET.
28. Design a current source using MOSFETs for  $I_{ref} = 0.2 \text{ mA}$  and  $I_o = 0.18 \text{ mA}$ . Assume  $k_n = \frac{1}{2} \mu_n C_{ox} = 40 \mu\text{A/V}^2$ ,  $V_{TH} = 0.5 \text{ V}$ ,  $V_{GS2} = 1.5 \text{ V}$  and  $\lambda = 0$ . Also assume  $V_{DD} = 6 \text{ V}$  and  $V_{SS} = 0 \text{ V}$ .
29. Explain the operation of JFET cascode current source.
30. Explain the operation of a MOSFET current source which is relatively independent of power supply.
31. Explain a current source using threshold reference.
32. Explain a self-biased current source using  $V_{BE}$  as reference.
33. Explain the operation of current mirror circuit in dual input, balanced output differential amplifier circuit.
34. What are voltage references?
35. Define bandgap reference.
36. Explain the operation of voltage source using temperature compensated Avalanche diode.
37. What is the concept of the use of a voltage reference?
38. Define the temperature coefficient of the output reference voltage.

39. Explain a voltage reference circuit using Avalanche diode reference with a neat circuit diagram.
40. With a circuit diagram, explain how dc level shifting operation is performed.
41. What is a level shifter? Why is it needed?
42. What is a level translator circuit? Why is it used with the cascaded differential amplifier stages?
43. What is the main advantage of constant current bias over emitter bias?
44. What is a differential amplifier?
45. Draw the circuit of any one type of differential amplifier. Derive the expression for differential voltage gain.
46. Draw the circuit diagram of an emitter-coupled differential amplifier and explain the operation.
47. Perform dc analysis and ac analysis of an emitter-coupled pair.
48. Draw a circuit diagram and explain the operation of JFET differential amplifier with zero constant current bias.
49. State and explain common-mode rejection ratio (CMRR).
50. Define the terms common-mode gain and differential mode gain.
51. Explain the operation of a JFET differential amplifier.
52. Perform the ac and dc analysis of JFET differential amplifier.
53. Explain the operation of a MOSFET differential amplifier.
54. Perform the ac and dc analysis of MOSFET differential amplifier.
55. Discuss the operation of a BJT based active load using neat sketch.
56. Discuss the operation of an active load using JFET with a neat circuit diagram.
57. Discuss the operation of an active load using MOSFET with a neat circuit diagram.
58. What is the main advantage of an active load?
59. Draw the circuit of a MOSFET cascode current source and discuss the advantages of this design.
60. What is meant by matched transistors?
61. Sketch the circuit of a MOSFET differential amplifier with active load and explain the operation of the circuit.
62. Explain how a differential mode output signal is generated in a differential amplifier.
63. Explain how a common mode output signal is generated in a differential amplifier.
64. Define CMRR. What is its ideal value?
65. Draw the dc transfer characteristics of a BJT differential amplifier and comment on it.
66. Define common mode and differential mode input voltages.
67. Draw the half circuit models for an emitter-coupled differential amplifier and explain.
68. Find the  $Q$ -point  $V_C$  and  $I_B$  for the differential amplifier shown in Fig. 2.45. Assume  $\beta = 200$ .
69. A differential amplifier has (i)  $\text{CMRR} = 1000$  and (ii)  $\text{CMRR} = 10000$ . The first set of inputs is  $v_1 = +200 \mu\text{V}$  and  $v_2 = -200 \mu\text{V}$ . The second set of inputs is  $v_1 = 1200 \mu\text{V}$  and  $v_2 = 800 \mu\text{V}$ . Compare the levels of output voltages obtained for the two sets of input voltages and comment on the performance of differential amplifier based on the results.
70. Find the  $Q$ -point for the MOSFETs in the differential amplifier shown in Fig. 2.63 with  $V_{DD} = -V_{SS} = 10\text{V}$ ,  $I_{ss} = 150 \mu\text{A}$ ,  $R_D = 60 \text{k}\Omega$ ,  $K_n = 570 \mu\text{A}/V^2$  and  $V_{Th} = 0.5 \text{ V}$ . What is the maximum  $V_{IC}$  for which  $M_1$  remains saturated?
71. Assume for the bandgap voltage reference circuit shown in Fig. 2.34,  $I_1 = I_3 = 0.25 \text{ mA}$ ,  $I_2 = 0.25 I_1$ ,  $I_S = 2 \times 10^{-15} \text{ A}$  for the transistor and temperature is  $27^\circ\text{C}$ . Design the bandgap voltage reference circuit.

# Operational Amplifier Characteristics

3

## 3.1 INTRODUCTION

An operational amplifier, commonly called op-amp, is a three stage circuit, namely, the input stage, gain stage and output stage. This op-amp is available as an integrated circuit. The input stage is a differential amplifier, the gain stage provides additional voltage gain with necessary dc level shifting and the output stage provides current gain and low output impedance. A feedback capacitor is often included in the second stage to provide frequency compensation. The op-amp is a multiple terminal and internally compensated device, which was conceived as an integrated circuit in the year 1966. The op-amp amplifies only the difference between two input signals and generates a single output.

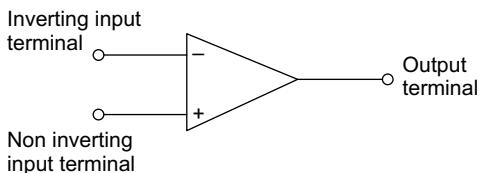
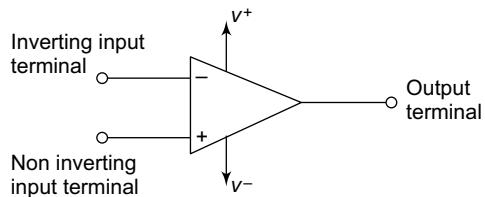
A common user finds it easy to design the circuits, taking into consideration the entire performance characteristics of the op-amps simply by the selection of external components that are connected to it. The main advantage of an op-amp is that it can be used to perform a large number of mathematical operations, or to generate a number of circuit functions by applying a passive feedback around the amplifier.

The op-amps are used extensively in electronic systems such as audio and radio communication, medical electronics, instrumentation, and in mathematical computations of addition, subtraction, multiplication, integration and differentiation, logarithmic and antilogarithmic operations and in many signal processing applications.

In the previous chapter, the important circuit configurations of linear ICs and the basic concepts of their design and analysis have been discussed. This chapter combines basic circuit configurations to form larger analog circuits, culminating in the form of integrated circuit, and further explores the study of a general op-amp and its design.

The IC 741 is a widely used all-bipolar general purpose op-amp. The characteristics of ideal and practical op-amps, internal circuit diagram and operation of the circuits, dc and ac performance characteristics and the interpretation of the data sheet of the op-amp 741 are presented in this chapter.

**Circuit symbol of an operational amplifier** The circuit schematic of an op-amp is in the form of a triangle as shown in Fig. 3.1. The device has two input terminals and one output terminal. The terminal marked  $(-)$  is called the *inverting input* terminal and the terminal marked  $(+)$  is identified as the *non-inverting input* terminal. Figure 3.2 shows the op-amp with positive voltage supply  $V^+$  and a negative voltage supply  $V^-$  terminals.

**Fig. 3.1** Op-amp circuit symbol**Fig. 3.2** Op-amp circuit symbol with positive and negative voltage supply terminals

## 3.2 IDEAL OPERATIONAL AMPLIFIER

The *ideal* operational amplifier is a differential input and single-ended output device. The equivalent circuit and the transfer characteristics of an ideal op-amp are shown in Fig. 3.3(a) and (b). The input impedance of the ideal op-amp is infinite and it means that the input current is zero. The output terminal of the op-amp acts as the output of an ideal voltage source which means that its small signal output impedance is zero. As shown in Fig. 3.3(a),  $A$  represents the differential gain of the op-amp and the output voltage  $v_o$  is given by

$$v_o = A(v_1 - v_2) \quad (3.1)$$

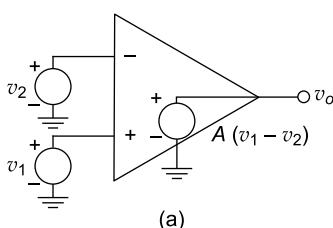
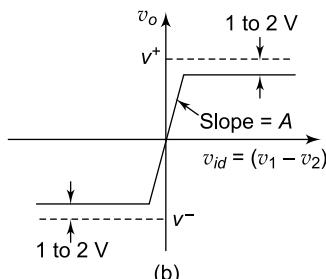
where  $v_1$  is the input at the non-inverting input terminal and  $v_2$  is the input at the inverting input terminal.

Equation (3.1) identifies that the output is in phase with  $v_1$  and out of phase with  $v_2$ . The transfer characteristics of an op-amp are shown in Fig. 3.3(b).

The ideal op-amp produces an output in response only to the difference between the input signals  $v_1$  and  $v_2$ . Thus, it maintains an ideal zero output signal for  $v_1 = v_2$ . When  $(v_1 - v_2) \neq 0$ , there exists a *common-mode input signal*, in response to which the ideal op-amp produces a zero output signal. This characteristic is called the *common-mode rejection*.

The op-amp consists of transistors biased in the active region with the voltages  $V^+$  (or  $+V_{CC}$ ) and  $V^-$  (or  $-V_{EE}$ ). Therefore, the output voltage is limited by the output voltage levels. When the output voltage  $v_o$  reaches  $V^+$ , it saturates and is nearly equal to  $V^+$ . Similarly when the output voltage  $v_o$  approaches  $V^-$ , it saturates at a voltage nearly equal to  $V^-$ . The difference between the positive saturation level and positive supply voltage and the difference between the negative saturation level and the negative supply voltage is approximately 1 to 2 V as shown in Fig. 3.3(b). This concept is discussed in detail in Sec. 3.3.

The ideal op-amp identifies the difference between two input signals that are applied at the inverting and non-inverting input terminals and amplifies the difference so obtained to produce an output signal. The output voltage is the voltage at the output terminal measured with respect to ground.

**Fig. 3.3** Ideal op-amp: (a) Equivalent circuit (b) Transfer characteristics

The characteristics of an ideal op-amp are as follows:

- (i) Infinite input resistance,  $R_i = \infty$
- (ii) Zero output resistance,  $R_o = 0$
- (iii) Infinite voltage gain,  $A_v = \infty$
- (iv) Infinite bandwidth,  $BW = \infty$
- (v) Infinite common-mode rejection ratio,  $CMRR = \infty$
- (vi) Infinite slew rate,  $SR = \infty$
- (vii) Zero offset, i.e. when  $v_1 = v_2$ ,  $v_o = 0$
- (viii) Characteristics do not drift with temperature

It can be observed that

- (i) An ideal op-amp allows zero current to enter into its input terminals, i.e.  $i_1 = i_2 = 0$ . Due to infinite input impedance, any signal with source impedance can drive the op-amp without getting inflicted with any loading effect.
- (ii) The gain of the ideal op-amp is infinite. Hence, the voltage between the inverting and non-inverting terminals is essentially zero for a finite output voltage.
- (iii) The output voltage  $v_o$  is independent of the output current drawn from the op-amp, since  $R_o = 0$ . This means that the output can drive an infinite number of output devices of any impedance value.

If the input impedance is high and output impedance is low with respect to the feedback impedances connected externally, and if the voltage gain is sufficiently high, then the resulting amplifier performance becomes solely determined by the external feedback components.

### 3.3 PRACTICAL OPERATIONAL AMPLIFIER

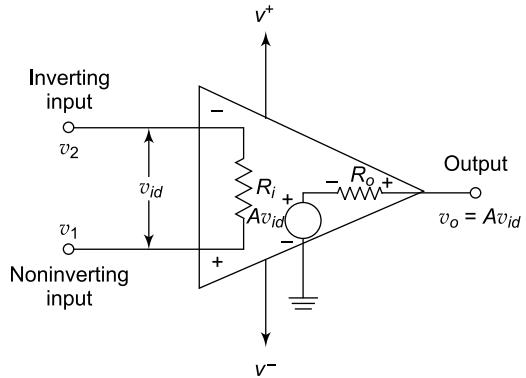
A physical op-amp is not ideal. The equivalent circuit of a practical op-amp is shown in Fig. 3.4. The equivalent circuit is useful in analyzing the operating principles of op-amps and in observing the effects of feedback.

For the practical op-amp, the open-loop gain  $A \neq \infty$ , the input resistance  $R_i \neq \infty$  and the output resistance  $R_o \neq 0$ . It can be observed from Fig. 3.4 that the output is a voltage controlled voltage source with  $A v_{id}$  of equivalent Thevenin's voltage source and  $R_o$  of Thevenin's equivalent resistance looking back into the output terminal of the op-amp. The output voltage is given by

$$v_o = A v_{id} = A(v_1 - v_2) \quad (3.2)$$

where  $A$  is the large-signal voltage gain and  $v_{id}$  is the difference between the input voltages  $v_1$  and  $v_2$ .

From the equation above, it is evident that the op-amp amplifies the difference between the two input voltages and it does not amplify the input voltages themselves. The output voltage is directly proportional to the algebraic difference between the two input voltages. The polarity of the output voltage depends on the polarity of the difference between the input voltages.



**Fig. 3.4** Equivalent circuit of a practical op-amp

The use of an op-amp is greatly enhanced by the negative feedback. The feedback helps in avoiding saturation of the output and the circuit operates in a linear manner.

**Output saturation** The dual supply voltages  $V^+$  and  $V^-$  set the upper and lower bounds on the output characteristic of the op-amp. The input-output voltage transfer characteristics of Fig. 3.3(b) show the regions of operation and approximate model of op-amp in the respective regions.

- (i) In the linear region, the curve is approximately a straight line and its slope indicates the open-loop gain  $A$ . When  $A$  is very large, the curve becomes steeper, and nearly aligns itself with the vertical axis. For a voltage of  $v_{id} = 1 \mu\text{V}$  and  $A = 2 \times 10^5$ ,  $v_o = A \times v_{id} = 2 \times 10^5 \times 1 \times 10^{-6} = 0.2 \text{ V}$ . Hence, the op-amp is modelled with a dependent source of value  $Av_{id}$  as shown in Fig. 3.4.
- (ii) As  $v_{id}$  increases,  $v_o$  rises proportionally, until a point is reached when the internal transistors saturate that causes the characteristics to flatten out. This region is called the *positive saturation region* and in this region,  $v_o$  no longer depends on  $v_{id}$ . Then, the op-amp behaves as an independent source of value  $+V_{sat}$ . Similarly, the *negative saturation* occurs when  $v_{id}$  rises in the negative direction resulting in the op-amp acting as an independent source of value  $-V_{sat}$ .

For bipolar op-amps, such as IC 741,  $+V_{sat}$  and  $-V_{sat}$  are typically  $\pm 13 \text{ V}$  which is about  $2 \text{ V}$  below  $V_{CC}$  and  $V_{EE}$ , of value  $\pm 15 \text{ V}$ . When the op-amp is used with negative feedback, the operation must be confined within the linear region of operation.

## 3.4 GENERAL OPERATIONAL AMPLIFIER

An operational amplifier generally consists of three stages, namely, (i) a differential amplifier, (ii) additional amplifier stages to provide the required voltage gain and dc level shifting, and (iii) an emitter-follower or source-follower output stage to provide current gain and low output resistance.

A low-frequency or dc gain of approximately  $10^4$  is desired for a general purpose op-amp and hence, the use of active load is preferred in the internal circuitry of op-amp. The output voltage is required to be at ground, when the differential input voltage is zero, and this necessitates the use of dual polarity supply voltage. Since the output resistance of an op-amp is required to be low, a complementary push-pull emitter-follower or source-follower output stage is employed. Moreover, as the input bias currents are to be very small of the order of picoamperes, an FET input stage is normally preferred. Figure 3.5 shows a general op-amp circuit using JFET input devices.

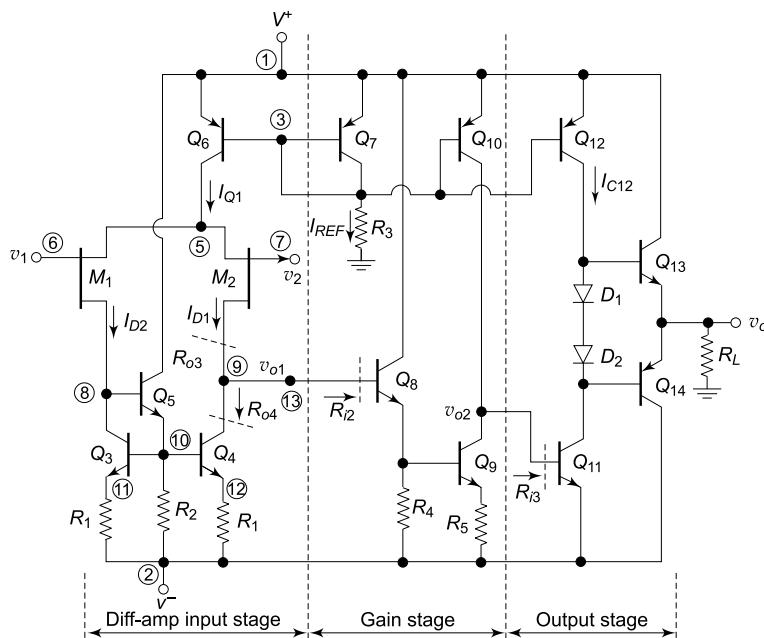
### 3.4.1 Input Stage

The input differential amplifier stage uses *p*-channel JFETs  $M_1$  and  $M_2$ . It employs a three-transistor active load formed by  $Q_3$ ,  $Q_4$  and  $Q_5$ . The bias current for the stage is provided by a two-transistor current source using *PNP* transistors  $Q_6$  and  $Q_7$ . Resistor  $R_1$  increases the output resistance seen looking into the collector of  $Q_4$  as indicated by  $R_{o4}$ . This is necessary to provide bias current stability against the transistor parameter variations. Resistor  $R_2$  establishes a definite bias current through  $Q_5$ . A single ended output is taken out at the collector of  $Q_4$ .

MOSFETs are used in place of JFETs, with additional devices in the circuit to prevent any damage for the gate oxide due to electrostatic discharges.

### 3.4.2 Gain Stage

The second stage or the gain stage uses Darlington transistor pair formed by  $Q_8$  and  $Q_9$  as shown in Fig. 3.5. The transistor  $Q_8$  is connected as an emitter follower, providing large input resistance. Therefore, it minimises the loading effect on the input differential amplifier stage.



**Fig. 3.5** General op-amp circuit

The transistor Q<sub>9</sub> provides an additional gain and Q<sub>10</sub> acts as an active load for this stage. The current mirror formed by Q<sub>7</sub> and Q<sub>12</sub> establishes the bias current for Q<sub>9</sub>. The  $V_{BE}$  drop across Q<sub>9</sub> and drop across R<sub>5</sub> constitute the voltage drop across R<sub>4</sub>, and this voltage sets the current through Q<sub>8</sub>. It can be set to a small value, such that the base current of Q<sub>8</sub> also is very less.

### 3.4.3 Output Stage

The final stage of the op-amp is a class AB complementary push-pull output stage. Q<sub>11</sub> is an emitter follower, providing a large input resistance for minimising the loading effects on the gain stage. Bias current for Q<sub>11</sub> is provided by the current mirror formed by Q<sub>7</sub> and Q<sub>12</sub>, through the diodes D<sub>1</sub> and D<sub>2</sub>, and this establishes the quiescent current through Q<sub>13</sub> and Q<sub>14</sub> for minimising the cross-over distortion. Transistors can also be used in place of the two diodes.

The overall voltage gain  $A_v$  of the op-amp is the product of voltage gains of each stage as given by

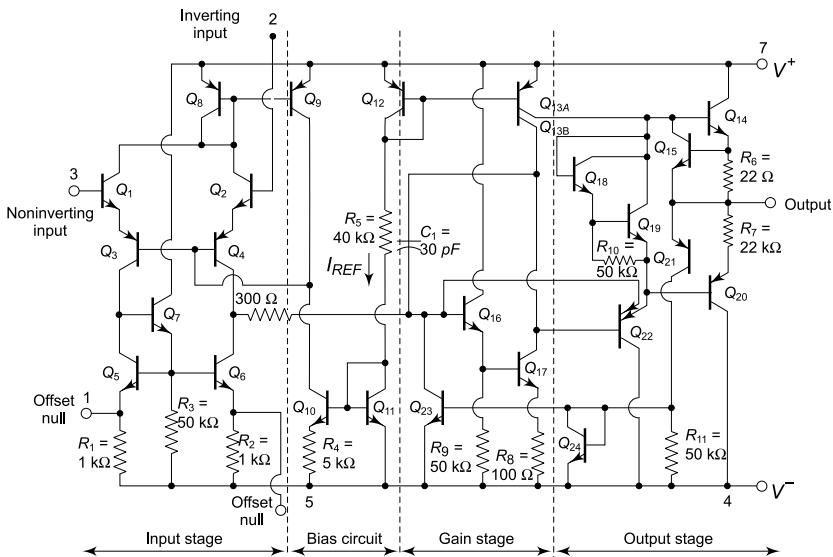
$$A_v = |A_d| |A_2| |A_3|$$

where  $A_d$  is the gain of the differential amplifier stage,  $A_2$  is the gain of the second gain stage and  $A_3$  is the gain of the output stage.

## 3.5 IC 741 BIPOLAR OPERATIONAL AMPLIFIER

The IC 741 produced since 1966 by several manufacturers is a widely used general purpose operational amplifier. Figure 3.6 shows the equivalent circuit of the 741 op-amp, divided into various individual stages. As discussed for the general op-amp structure, the circuit consists of three stages.

- (i) The input differential amplifier
- (ii) The gain stage
- (iii) The output stage



**Fig. 3.6** Op-amp 741 equivalent circuit

A bias circuit is used to establish the bias current for whole of the circuit in the IC. The op-amp is supplied with positive and negative supply voltages of value  $\pm 15$  V, and the supply voltages as low as  $\pm 5$  V can also be used.

### 3.5.1 Bias Circuit

The reference bias current  $I_{REF}$  for the 741 circuit is established by the bias circuit consisting of two diode-connected transistors  $Q_{11}$  and  $Q_{12}$  and resistor  $R_5$ . The Widlar current source formed by  $Q_{11}$ ,  $Q_{10}$  and  $R_4$  provide bias current for the differential amplifier stage at the collector of  $Q_{10}$ . Transistors  $Q_8$  and  $Q_9$  form another current mirror providing bias current for the differential amplifier. The reference bias current  $I_{REF}$  also provides mirrored and proportional current at the collector of the *double-collector lateral PNP* transistor  $Q_{13}$ . The transistor  $Q_{13}$  and  $Q_{12}$  thus form a two-output current mirror with  $Q_{13A}$  providing bias current for output stage and  $Q_{13B}$  providing bias current for  $Q_{17}$ . The transistors  $Q_{18}$  and  $Q_{19}$  provide dc bias for the output stage formed by  $Q_{14}$  and  $Q_{20}$  and they establish two  $V_{BE}$  drops of potential difference between the bases of  $Q_{14}$  and  $Q_{18}$ .

### 3.5.2 Input Stage

The input differential amplifier stage consists of transistors  $Q_1$  through  $Q_7$ , with biasing provided by  $Q_8$  through  $Q_{12}$ . The transistors  $Q_1$  and  $Q_2$  form emitter-followers contributing to high differential input resistance, and whose output currents are inputs to the common base amplifier using  $Q_3$  and  $Q_4$  which offers a large voltage gain.

The transistors  $Q_5$ ,  $Q_6$  and  $Q_7$  along with resistors  $R_1$ ,  $R_2$  and  $R_3$  form the active load for input stage. The single-ended output is available at the collector of  $Q_6$ . The two null terminals in the input stage facilitate the null adjustment. The lateral *PNP* transistors  $Q_3$  and  $Q_4$  provide additional protection against voltage breakdown conditions. The emitter-base junction of *NPN* transistors breakdown at about 7V whereas the *PNP* transistors  $Q_3$  and  $Q_4$  have higher emitter-base breakdown voltages of about 50 V. Therefore, placing *PNP* transistors in series with *NPN* transistors provide protection against accidental shorting of supply voltages to the input terminals.

### 3.5.3 Gain Stage

The second or the gain stage consists of transistors  $Q_{16}$  and  $Q_{17}$ , with  $Q_{16}$  acting as an emitter-follower for achieving high input resistance. The transistor  $Q_{17}$  operates in common emitter configuration with its collector voltage applied as input to the output stage. Level shifting is done for this signal at this stage.

Internal compensation through Miller compensation technique is achieved using the feedback capacitor  $C_1$  connected between the output and input terminals of the gain stage.

### 3.5.4 Output Stage

The output stage is a class *AB* circuit consisting of complementary emitter follower transistor pair  $Q_{14}$  and  $Q_{20}$ . Hence, they provide an effective low output resistance and current gain.

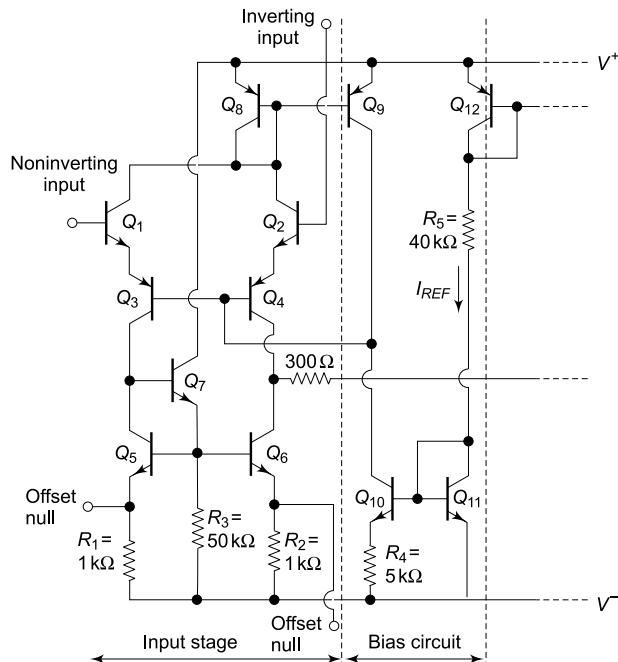
The output of the gain stage is connected at the base of  $Q_{22}$ , which is connected as an emitter-follower providing a very high input resistance, and it offers no appreciable loading effect on the gain stage. It is biased by transistor  $Q_{13A}$  which also drives  $Q_{18}$  and  $Q_{19}$ , that are used for establishing a quiescent bias current in the output transistors  $Q_{14}$  and  $Q_{20}$ .

### 3.5.5 DC Analysis of IC 741

To perform dc analysis, both the inverting and non-inverting input terminals are assumed to be at ground potential and supply voltages of  $\pm 15V$  are supplied to the op-amp.

**Bias circuit and input stage** The bias circuit and input differential amplifier stage of 741 are shown in Fig. 3.7. The reference current  $I_{REF}$  is given by

$$I_{REF} = \frac{V^+ - V_{EB12} - V_{BE11} - V^-}{R_5}$$



**Fig. 3.7** Input stage with bias circuit

where  $V_{EB12}$  and  $V_{BE11}$  are the base-emitter voltages of  $Q_{12}$  and  $Q_{11}$ . The transistors  $Q_{11}$  and  $Q_{10}$  with  $R_4$  form a Widlar current source, whose output current  $I_{C10}$  is determined using the relation as given by

$$I_{C10}R_4 = V_T \ln\left(\frac{I_{REF}}{I_{C10}}\right)$$

where  $V_T$  is the thermal voltage.

Neglecting the base currents, we have

$$I_{C8} = I_{C9} = I_{C10}$$

Then, the quiescent collector currents in transistors  $Q_1$  through  $Q_4$  are equal and they are given by

$$I_{C1} = I_{C2} = I_{C3} = I_{C4} = \frac{I_{C10}}{2}$$

Assuming exactly balanced dc currents in the input stage, the dc voltages at the collector of  $Q_5$  and  $Q_6$  are exactly the same. Therefore, it can be represented as

$$V_{C6} = V_{C5} = V_{BE7} + V_{BE6} + I_{C6}R_2 + V^-$$

Thus, the dc level shifts through the op-amp.

The current gain  $\beta_p$  of  $PNP$  transistors  $Q_3$ ,  $Q_4$ ,  $Q_8$  and  $Q_9$  are relatively small, and hence, their base currents are not negligible. Figure 3.8 shows the detailed circuit of input stage of op-amp with the current components indicated. The base currents of  $NPN$  transistors  $Q_1$  and  $Q_2$  are assumed small and negligible. The current  $I_{C10}$  forms the base currents of  $Q_3$  and  $Q_4$ , which in turn establish their emitter currents marked  $I$  in Fig. 3.8.

The collector current of  $Q_8$  is given by

$$2I = I_{C8} + \frac{2I_{C9}}{\beta_p}$$

Since  $I_{C9} = I_{C8}$  in the current mirror, we can write

$$2I = I_{C9} \left(1 + \frac{2}{\beta_p}\right)$$

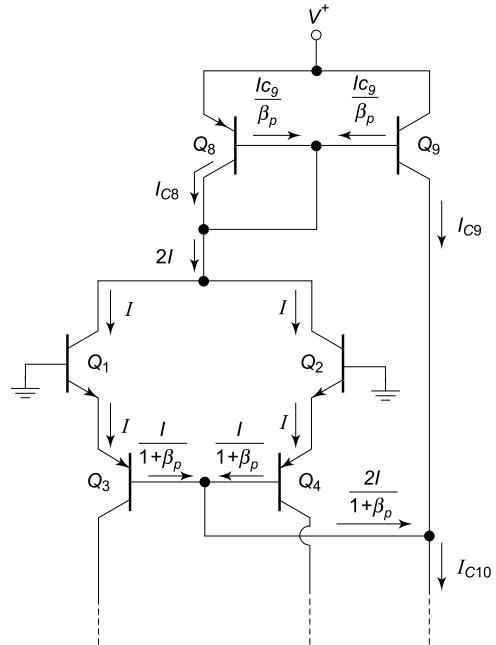
$$\text{Therefore, } I_{C9} = \frac{2I}{1 + \frac{2}{\beta_p}} \quad (3.3)$$

$$\text{Then, } I_{C10} = I_{C9} + \frac{2I}{1 + \beta_p}$$

Using Eq. (3.3), we can write the equation above as given by

$$I_{C10} = \frac{2I}{1 + \frac{2}{\beta_p}} + \frac{2I}{1 + \beta_p} = 2I \left[ \frac{\beta_p^2 + 2\beta_p + 2}{\beta_p^2 + 3\beta_p + 2} \right] \quad (3.4)$$

Assuming the base currents of  $NPN$  transistors  $Q_1$  and  $Q_2$  are negligible, the current  $I \equiv \frac{I_{C10}}{2}$ .



**Fig. 3.8** Detailed circuit of input stage

**Gain stage** The gain stage along with a part of the bias circuit showing  $I_{REF}$  is shown in Fig. 3.9.

The transistors  $Q_{12}$  and  $Q_{13}$  form a current mirror. The current  $I_{C13B}$  is provided with a scale factor of 0.75 as given by

$$I_{C13B} = 0.75 I_{REF} \quad (3.5)$$

From Fig. 3.9, the emitter current of  $Q_{16}$  is given by

$$I_{E16} \cong I_{C16}$$

$$= I_{B17} + \frac{(I_{E17} \times R_8) + V_{BE17}}{R_9} \quad (3.6)$$

considering that base current of  $Q_{16}$  is negligible.

**Output stage** Figure 3.10 shows the basic output stage of op-amp 741 operating in class *AB* mode. The current source  $Q_{13A}$  supplies a current of  $0.25 I_{REF}$ , to the combination of  $Q_{18}$ ,  $Q_{19}$  and  $R_{10}$ . Assuming the base currents are negligible,  $I_{C13A}$  is given by

$$I_{C13A} = 0.25 I_{REF} = I_{Bias} \quad (3.7)$$

Neglecting the base current once again, the collector current of  $Q_{22}$  equals  $0.25 I_{REF}$  of  $I_{Bias}$ . The collector current of  $Q_{18}$  is then

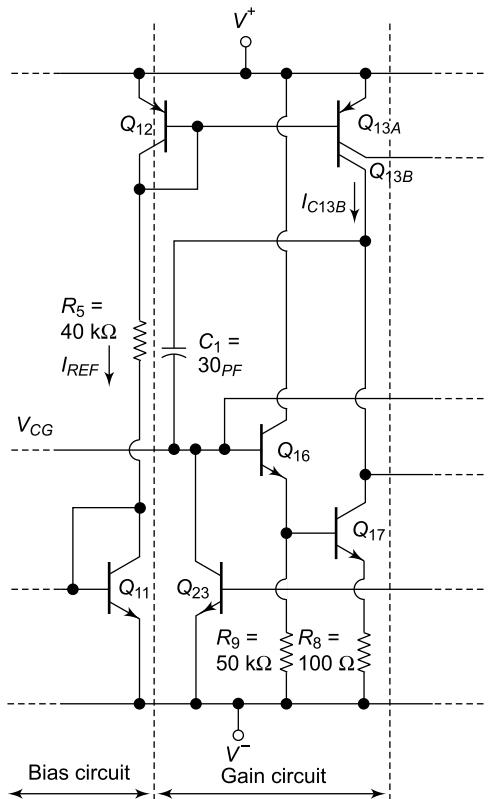
$$I_{C18} \cong \frac{V_{BE19}}{R_{10}}$$

Therefore, we have

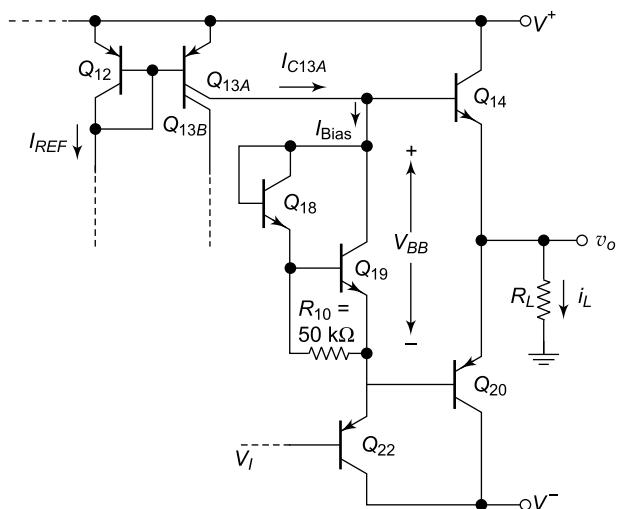
$$I_{C19} = I_{Bias} - I_{C18}$$

### 3.5.6 Short-Circuit Protection

The op-amp 741 contains a number of transistors that are OFF during its normal operation. When the output terminal gets shorted to the ground accidentally, while keeping a positive output voltage due to a certain input signal, a large current will get induced in the output transistor  $Q_{14}$ . This can produce heat and cause burnout of the transistor. Therefore, when the current in  $Q_{14}$  reaches 20 mA, the voltage drop across  $R_6$  becomes  $27 \Omega \times 20 \text{ mA} = 540 \text{ mV}$ , which biases the transistor  $Q_{15}$  into conduction.

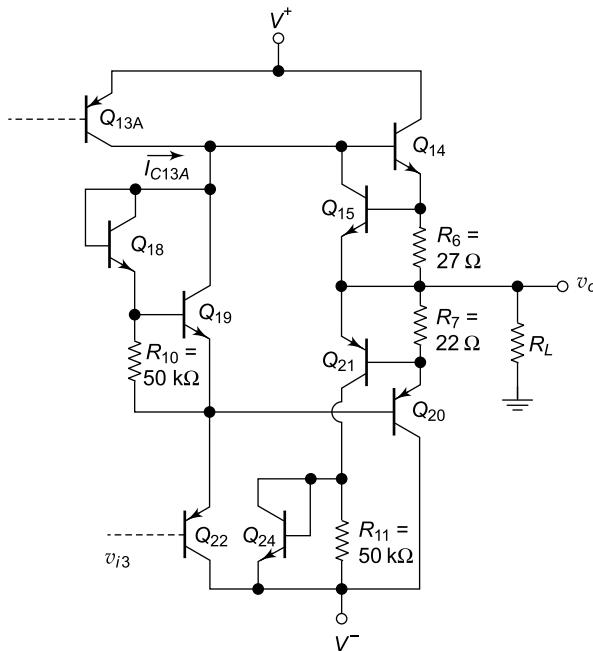


**Fig. 3.9** Gain stage of op-amp 741



**Fig. 3.10** Output stage of op-amp

Then, the excess current is shunted through the collector of  $Q_{15}$ . The circuit of the output stage with short-circuit protection is shown in Fig. 3.11.



**Fig. 3.11** Short-circuit protection in IC 741 op-amp

Similarly, the maximum current in  $Q_{20}$  is limited by  $R_7$ ,  $Q_{21}$  and  $Q_{24}$ . When the current flow increases, the drop across  $R_7$  becomes sufficient to turn the transistor  $Q_{21}$  ON and the transistor  $Q_{21}$  and  $Q_{24}$  shunt the excess current away from the transistor  $Q_{20}$ , thus protecting the output transistor.

### **Example 3.1**

Find the reference current  $I_{REF}$  for the circuit shown in Fig. 3.7, assuming  $V^+ = 15 V$ ,  $V^- = -15 V$  and  $V_{BE11} = V_{BE12} = 0.7 V$ .

**Solution** Given  $V^+ = 15V$ ,  $V^- = -15V$  and  $V_{BE11} = V_{BE12} = 0.7V$

From Fig. 3.7,  $R_5 = 40 \text{ k}\Omega$

$$\text{Therefore, } I_{REF} = \frac{V^+ - V_{BE12} - V_{BE11} - (-V^-)}{R_5}$$

$$= \frac{15 - 0.7 - 0.7 - (-15)}{40 \times 10^3} = 0.715 \text{ mA}$$

### **Example 3.2**

Determine the bias currents in the gain stage of the op-amp shown in Fig. 3.9.

**Solution** Assuming  $I_{REF}$  to be 0.715 mA, the collector current  $I_{C17}$  of  $Q_{17}$  is given by,

$$I_{C17} = I_{C13B}$$

Since

$$I_{C13B} = 0.75I_{REF},$$

$$I_{C13B} = I_{C17} \approx I_{E17} = 0.75 \times 0.715 \times 10^{-3} = 0.536 \text{ mA}$$

Using Eq. (3.6),

$$\begin{aligned} I_{C16} &\cong I_{E16} = I_{B17} + \frac{I_{E17}R_8 + V_{BE17}}{R_9} \\ &= \frac{I_{C17}}{\beta} + \frac{I_{E17}R_8 + V_{BE17}}{R_9} \end{aligned}$$

Assuming  $\beta = 150$  and  $V_{BE17} = 0.7 \text{ V}$  for NPN transistor,

$$I_{C16} \cong \frac{0.536 \times 10^{-3}}{150} + \frac{0.536 \times 10^{-3} \times 100 + 0.7}{50 \times 10^3} = 15.1 \mu\text{A}$$

### Example 3.3

Determine the bias current in the output stage of Fig. 3.10 assuming  $I_{REF} = 0.715 \text{ mA}$ ,  $V_{BE} = 0.7 \text{ V}$  and the saturation current for  $Q_{18}$  and  $Q_{19}$  are  $I_{S18} = I_{S19} = 10^{-14} \text{ A}$  and  $I_{S14} = I_{S20} = 2 \times 10^{-14} \text{ A}$ . Assume that the base currents are negligible.

**Solution** Given  $I_{REF} = 0.715 \text{ mA}$

Thus,

$$I_{C13A} = 0.25 \times I_{REF} = 0.25 \times 0.715 \times 10^{-3} = 0.179 \text{ mA}$$

Assuming

$V_{BE19} = 0.7 \text{ V}$ , the current through  $R_{10}$  is given by

$$I_{R10} = \frac{V_{BE19}}{R_{10}} = \frac{0.7}{50 \times 10^3} = 0.014 \text{ mA}$$

Therefore,

$$I_{C19} \cong I_{E19} = I_{C13A} - I_{R10} = 0.179 - 0.014 = 0.165 \text{ mA}$$

Then,  $V_{BE19}$  can be calculated as

$$V_{BE19} = V_T \ln \left[ \frac{I_{C19}}{I_S} \right] = 26 \times 10^{-3} \times \ln \left( \frac{0.165 \times 10^{-3}}{10^{-14}} \right) = 0.612 \text{ V}$$

Assuming

$$\beta = 200,$$

$$I_{B19} = \frac{I_{C19}}{\beta} = \frac{0.165 \times 10^{-3}}{200} = 0.825 \mu\text{A}$$

$$I_{C18} \cong I_{E18} = I_{R10} + I_{B19} = (14 + 0.825) \mu\text{A} = 14.825 \mu\text{A}$$

$$V_{BE18} = V_T \ln \left( \frac{I_{C18}}{I_S} \right) = 26 \times 10^{-3} \ln \left( \frac{14.825 \times 10^{-6}}{10^{-14}} \right) = 0.549 \text{ V}$$

Therefore,

$$V_{BB} = V_{BE18} + V_{BE19} = 0.549 + 0.612 = 1.161 \text{ V}$$

Transistors  $Q_{14}$  and  $Q_{20}$  are identical with  $\frac{V_{BB}}{2}$  across their base-emitter junction.

$$I_{C14} = I_{C20} = I_S e^{\frac{V_{BB}}{2} \frac{1}{V_T}} = 2 \times 10^{-14} \times e^{\frac{1.161}{2} \frac{1}{0.026}} = 99.42 \mu\text{A}$$

### 3.5.7 Small Signal Analysis

**Input stage** Figure 3.12 shows the ac equivalent circuit of the input stage. The differential voltage is  $v_{id}$  between the two input terminals. The constant current biasing provides infinite impedance at the bases of  $Q_3$  and  $Q_4$ .  $R_{eff1}$  is the effective resistance offered by the active load, with  $R_{i2}$  acting as the input resistance of the gain stage. The small-signal differential voltage gain is given by

$$A_d = \frac{v_{o1}}{v_{id}} = -g_m (r_{o4} \parallel R_{eff1} \parallel R_{i2}) = -\frac{I_{CQ}}{V_T} (r_{o4} \parallel R_{eff1} \parallel R_{i2}) \quad (3.8)$$

where  $I_{CQ}$  represents the quiescent collector current in transistors  $Q_1, Q_2, Q_3$  and  $Q_4$ ,  $r_{o4}$  is the resistance of  $Q_4$  looking into its collector. The minus sign denotes the change in signal polarity.

The effective resistance of active load is  $R_{eff1} = r_{o6}(1 + g_{m6}(R_2 \parallel r_{\pi6}))$  which is the resistance of the Widlar current source.

Input resistance  $R_{i2}$  of the current stage is given by

$$R_{i2} = r_{\pi16} + (1 + \beta_n)R'_E$$

where  $r_{\pi16}$  is the resistance through hybrid  $\pi$  model of  $Q_{16}$ , and  $R'_E$  is the effective resistance  $Q_{16}$  given by

$$R'_E = R_9 \parallel (r_{\pi17} + (1 + \beta_n)R_8) \quad (3.9)$$

**Gain stage** Figure 3.13 shows the ac equivalent circuit of gain stage of 741 op-amp. The resistance  $R_{eff2}$  is the effective resistance of active load.  $R_{i3}$  indicates the resistance offered by the output stage and  $R_{i2}$  is the input resistance of the gain stage.

To find the small-signal voltage gain, the input base current of  $Q_{16}$  is

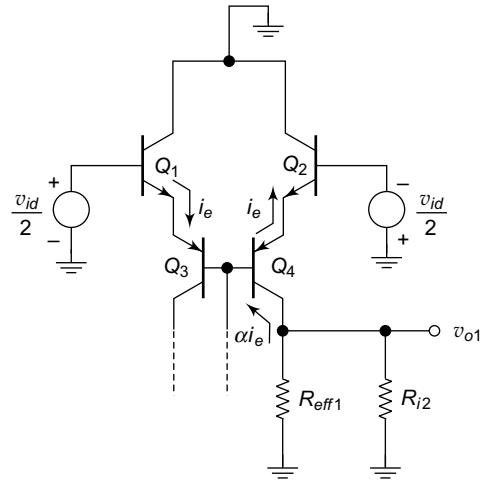
$$i_{b16} = \frac{v_{o1}}{R_{i2}}$$

$$i_{b17} = \frac{R_9}{R_9 + (r_{\pi17} + (1 + \beta_n)R_8)} \times i_{e16}$$

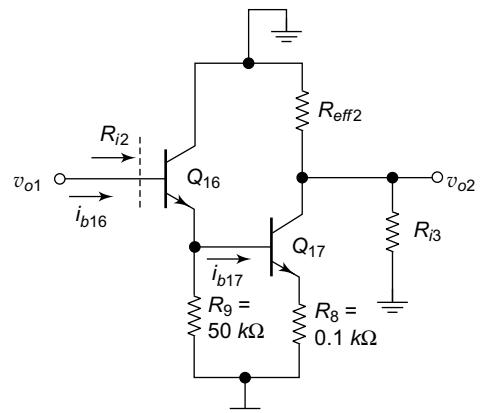
Then,  $v_{o2} = -i_{c17} \times (R_{eff2} \parallel R_{i3})$

Using the three equations above, we get

$$A_{v2} = \frac{v_{o2}}{v_{o1}} = -\beta_n \frac{(1 + \beta_n)R_9 (R_{eff2} \parallel R_{i3} \parallel R_{o17})}{R_{i2} (R_9 + (r_{\pi17} + (1 + \beta_n)R_8))}$$



**Fig. 3.12** The ac equivalent circuit of input stage



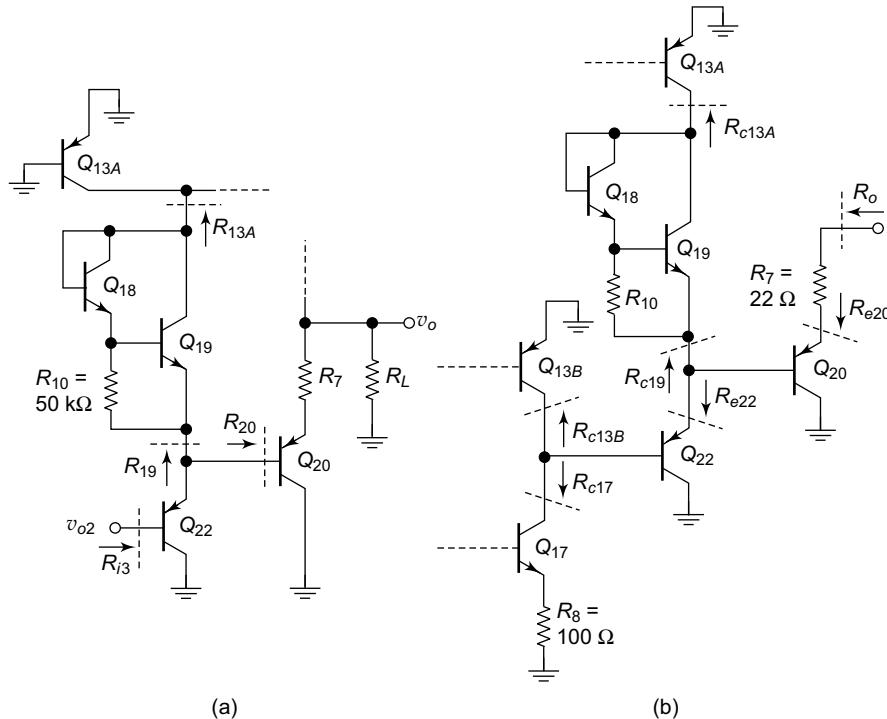
**Fig. 3.13** The ac equivalent circuit of gain stage

The effective resistance of the active load is the resistance seen into the collector of  $Q_{13B}$ , that is given by

$$R_{eff2} = r_{o13B} = \frac{V_A}{I_{C13B}}$$

Figure 3.14(a) shows the ac equivalent circuit to determine the input resistance of the output stage. Consider that the *PNP* output transistor  $Q_{20}$  is active, the *NPN* output transistor  $Q_{14}$  is cut-off and the resistor  $R_L$  is the load. Transistor  $Q_{22}$  acts as an emitter-follower and the input resistance is given by

$$R_{i3} = r_{\pi22} + (1 + \beta_p) [R_{19} \| R_{20}]$$



**Fig. 3.14** The ac equivalent circuit of the output stage of op-amp 741 for calculating (a) input resistance, and (b) output resistance

The resistance  $R_{19}$  is the series combination of resistances seen looking into the emitters of  $Q_{18}$  and  $Q_{19}$  and collector of  $Q_{13A}$ . The emitter resistances are small, compared with that of  $Q_{13A}$ . Hence, we have

$$R_{19} \equiv R_{13A} = r_{o13A} = \frac{V_A}{I_{C13A}}$$

The output transistor  $Q_{20}$  is also an emitter-follower. Therefore,

$$R_{20} = r_{\pi20} + (1 + \beta_p)R_L,$$

considering that the resistor  $R_L$  is larger than  $R_7$ .

**Overall gain** The overall voltage gain is the product of the individual gain factors, or we can write

$$A_v = A_d A_{v2} A_{v3} \quad (3.10)$$

where  $A_{v3}$  is the voltage gain of the output stage. Typical voltage gain for the 741 op-amp is in the range of 200,000.

**Output resistance** The output resistance can be determined using the ac equivalent circuit shown in Fig. 3.14(b). Assuming the output transistor  $Q_{20}$  is conducting and  $Q_{14}$  is cut-off, the output resistance is given by

$$R_o = R_7 + R_{e20}$$

$$\text{where } R_{e20} = \frac{r_{\pi20} + R_{e22} \| R_{c19}}{(1 + \beta_p)},$$

in which  $R_{c19} \cong R_{c13A}$  and the resistor  $R_{e22}$  is given by

$$R_{e22} = \frac{r_{\pi22} + R_{c17} \| R_{c13B}}{(1 + \beta_p)}, \quad R_{c13B} = r_{o13B},$$

and

$$R_{c17} = r_{o17} [1 + g_{m17} (R_8 \| r_{\pi17})].$$

The output resistance of the op-amp can be determined by combining all the resistance terms.

### 3.5.8 Frequency Response

The 741 op-amp is internally frequency-compensated using the Miller compensation technique by introducing a dominant low-frequency pole. Applying Miller's theorem, the effective input capacitance of the second gain stage is

$$C_i = C_1 (1 + |A_{v2}|) \quad (3.11)$$

The dominant low-frequency pole is given by

$$f_1 = \frac{1}{2\pi R_{eq} C_i}$$

where  $R_{eq}$  is the equivalent resistance between the second stage input node and ground. It is given by

$$R_{eq} = R_{o1} \| R_{i2}$$

where  $R_{i2}$  is the input resistance of the gain stage and  $R_{o1}$  is the output resistance of the differential amplifier stage. Using Fig. 3.12, we observe that

$$R_{o1} = R_{eff1} \| r_{o4}$$

The unity gain-bandwidth is given by

$$f_T = A_o f_1 \quad (3.12)$$

Typical unity gain-bandwidth value for the 741 op-amp is 1 MHz. If the frequencies of the other poles of the 741 op-amp are greater than 1.9 MHz, the phase margin is 90 degrees. This phase margin guarantees that any closed-loop amplifier circuit using op-amp 741 remain stable for any feedback transfer function.

## 3.6 DC PERFORMANCE CHARACTERISTICS OF OP-AMP

An ideal operational amplifier draws no current from the signal source and its response is independent of the temperature variations. However, a practical op-amp gets affected by the environmental and process parameter variations. The current is indeed, taken from the source into the input of op-amp and the two inputs respond differently to the input voltage and current. This happens due to the inherent mismatch among the transistors.

Therefore, the non-ideal dc characteristics of the op-amp are

- |                                |                           |
|--------------------------------|---------------------------|
| (i) Input bias current         | (ii) Input offset current |
| (iii) Input offset voltage and | (iv) Thermal drift        |

### 3.6.1 Input Bias Current

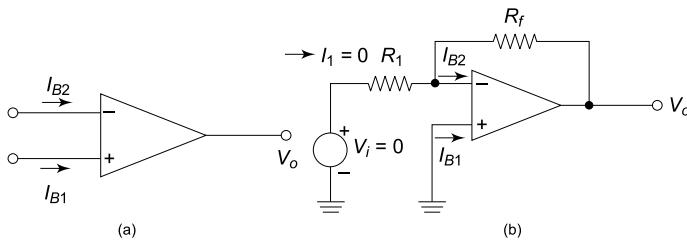
The input bias current is the average of the currents that flow into the inverting and non-inverting input terminals of an op-amp. The input bias current affects all applications of op-amps. For the op-amp to function, it is necessary to supply a small current, of the order of picoamperes for op-amps with FET inputs and microamperes for junction transistor type inputs. When the lower input bias currents are achieved, the possible imbalances in the circuit will be minimised. The 741 has an input bias current of 80 nA.

The input of the op-amp is a differential amplifier comprising either BJT or FET. In both the cases, the input transistors are biased into their linear regions of operation by inducing current into the bases of BJTs or supplying voltages to the gates of FETs with the use of external circuitry. It is assumed that no current is drawn into the input terminals of an ideal op-amp. However, a small value of dc current does enter the input terminals to bias the input transistors. Figure 3.15(a) shows the currents  $I_{B1}$  and  $I_{B2}$  entering the input terminals of the op-amp. Though both the transistors are identical, the two currents  $I_{B1}$  and  $I_{B2}$  are not exactly equal. This is due to the internal imbalances created during the fabrication process. Therefore, the manufacturers specify the input bias current  $I_B$  as the average of the two base currents of the differential amplifier constituting the input stage of the op-amp. The input bias current  $I_B$  is given by

$$I_B = \frac{I_{B1} + I_{B2}}{2} \quad (3.13)$$

where  $I_{B1}$  is the dc bias current entering the non-inverting input and  $I_{B2}$  is the dc bias current entering the inverting input

Figure 3.15(a) shows that both the inputs are grounded, thus maintaining zero input voltage to the op-amp. It may be noted that the op-amp is to be powered by the dual voltage power supply, which is normally  $\pm 15$  V.



**Fig. 3.15** (a) Input bias currents (b) Inverting amplifier with bias currents

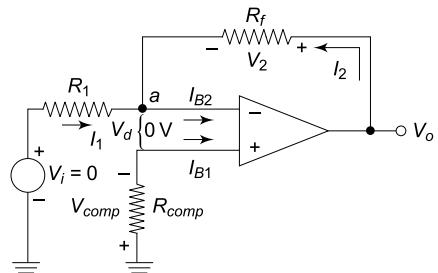
The basic inverting amplifier with the base currents  $I_{B1}$  and  $I_{B2}$  and the input voltage  $V_i = 0$  is shown in Fig. 3.15(b). The non-inverting input terminal of the op-amp is grounded. For this circuit, the output voltage  $V_o$  must be 0 V. However, the output voltage is found to be offset by a value of

$$V_o = I_{B2}R_f$$

Assuming a 741 op-amp with 500 nA of bias current (from datasheets), for  $R_f = 1 \text{ M}\Omega$ , the output becomes

$$V_o = 500 \times 10^{-9} \times 1 \times 10^6 = 500 \text{ mV}$$

This indicates that for applications involving 500 mA of input current, this offset voltage is utterly unacceptable. This offset effect can be compensated by the use of a compensation resistor  $R_{comp}$  connected as shown in Fig. 3.15(c).



**Fig. 3.15** (c) Bias current compensation

The compensation resistor  $R_{comp}$  is introduced in the non-inverting terminal path to ground. The current  $I_{B1}$  flowing through the compensating resistor  $R_{comp}$  develops a voltage  $V_{comp}$  across it. Then applying Kirchhoff's voltage law for the input circuit, we get

$$\begin{aligned} -V_{comp} + 0 + V_2 - V_o &= 0 \\ \text{or} \quad V_o &= V_2 - V_{comp} \end{aligned} \quad (3.14)$$

Choosing the proper value of  $R_{comp}$  to get  $V_2 = V_{comp}$  cancels the offset effect, thus making the output  $V_o = 0$ . The value of  $R_{comp}$  is calculated as shown below.

$$R_{comp} = \frac{V_2}{I_{B2}}$$

and

$$I_{B1} = \frac{V_{comp}}{R_{comp}}$$

At node  $a$ , with its voltage equal to  $-V_{comp}$  as shown in Fig. 3.15(c), we get

$$I_1 = \frac{V_{comp}}{R_l}$$

and

$$I_2 = \frac{V_2}{R_f} \quad (3.15)$$

For offset compensation, we know  $V_o$  must be zero for  $V_i = 0$ . That is, using Eq. (3.14),

we must have  $V_2 = V_{comp}$  and using Eq. (3.15), we get  $I_2 = \frac{V_{comp}}{R_f}$ .

The Kirchhoff's current law at node  $a$  offers

$$I_{B2} = I_2 + I_1 = \frac{V_{comp}}{R_f} + \frac{V_{comp}}{R_l} = V_{comp} \left( \frac{R_l + R_f}{R_l R_f} \right) \quad (3.16)$$

Assuming that  $I_{B1} = I_{B2}$ , and using  $I_{B1} = \frac{V_{comp}}{R_{comp}}$ , we get

$$V_{comp} \left( \frac{R_l + R_f}{R_l R_f} \right) = \frac{V_{comp}}{R_{comp}}$$

$$\text{or} \quad R_{comp} = \frac{R_l R_f}{R_l + R_f} = R_l \parallel R_f \quad (3.17)$$

Equation (3.17) shows that the compensating resistor  $R_{comp}$  must be equal to the parallel combination of input and feedback resistors  $R_l$  and  $R_f$  connected at the inverting input terminal of the op-amp.

### 3.6.2 Input Offset Current

The circuit of Fig. 3.15(a) achieves bias current compensation, when the bias currents are equal, i.e. when  $I_{B1} = I_{B2}$ . However, the input transistors cannot be made identical, and there always exists a small difference between the bias currents  $I_{B1}$  and  $I_{B2}$ .

The difference in magnitude between  $I_{B1}$  and  $I_{B2}$  is called *input offset current*  $I_{OS}$ .

$$I_{OS} = |I_{B1}| - |I_{B2}| \quad (3.18)$$

The manufacturers specify  $I_{OS}$  for a circuit when the output  $V_o$  is zero and temperature is 25°C.  $I_{OS}$  is typically less than 25% of  $I_B$  for the average input bias current. It is 200nA for BJT op-amp and 10pA for FET op-amp.

To find the effect of  $I_{OS}$  on  $V_o$ , referring to Fig. 3.15(c), and assuming  $V_i = 0$ , we get

$$V_{comp} = I_{B1} \times R_{comp}$$

and

$$I_1 = \frac{V_{comp}}{R_1}$$

Applying the two equations and using Kirchhoff's current law at node  $a$  gives,

$$I_2 = I_{B2} - I_1 = I_{B2} - \left( I_{B1} \frac{R_{comp}}{R_1} \right) \quad (3.19)$$

Figure 3.15(c) shows,

$$\begin{aligned} V_o &= I_2 R_f - V_{comp} \\ &= I_2 R_f - I_{B1} R_{comp} \end{aligned}$$

Substituting Eq. (3.19) in the above equation, we get

$$V_o = \left( I_{B2} - I_{B1} \frac{R_{comp}}{R_1} \right) R_f - I_{B1} R_{comp} \quad (3.20)$$

Using Eq. (3.17) for  $R_{comp}$  and simplifying Eq. (3.20) we get,

$$V_o = R_f (I_{B2} - I_{B1})$$

Therefore,

$$V_o = R_f I_{OS} \quad (3.21)$$

Equation (3.21) shows that the output voltage due to offset current  $I_{OS}$  is dependent on the feedback resistor  $R_f$ , and it can be a positive or negative dc voltage with respect to ground. Since, normally  $I_{OS} \ll I_B$ , the output offset caused by  $I_{OS}$  is much smaller than that caused by  $I_B$ .

### Example 3.4

Assume that an op-amp has  $I_{B1} = 400 \text{ nA}$  and  $I_{B2} = 300 \text{ nA}$ . Determine the average bias current  $I_B$  and the offset current  $I_{OS}$ .

**Solution** The average bias current is

$$\begin{aligned} I_B &= \frac{I_{B1} + I_{B2}}{2} \\ &= \frac{(400 + 300) \times 10^{-9}}{2} = 350 \text{ nA} \end{aligned}$$

The offset current is given by

$$\begin{aligned} I_{OS} &= I_{B1} - I_{B2} \\ &= (400 - 300) \times 10^{-9} = 100 \text{ nA} \end{aligned}$$

### Example 3.5

Assume for Fig. 3.15(c),  $I_{OS} = 400 \text{ nA}$ ,  $R_f = 100 \text{ k}\Omega$  and  $R_l = 1 \text{ k}\Omega$ . Determine the maximum output offset voltage.

**Solution** Given  $I_{OS} = 400 \text{ nA}$ ,  $R_f = 100 \text{ k}\Omega$  and  $R_l = 1 \text{ k}\Omega$

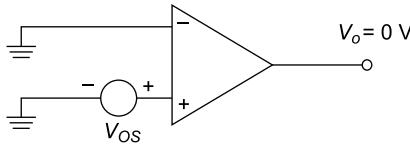
The maximum output offset voltage is

$$V_o = R_f I_{OS} = 100 \times 10^3 \times 400 \times 10^{-9} = 40 \text{ mV}$$

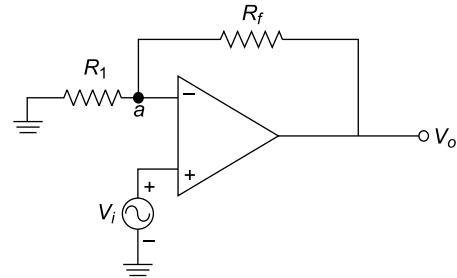
### 3.6.3 Input Offset Voltage

Input offset voltage  $V_{OS}$  is the differential input voltage that exists between the inverting and non-inverting input terminals of an op-amp. In other words, this can be defined as the voltage that is to be applied between the two input terminals for making the output voltage zero.

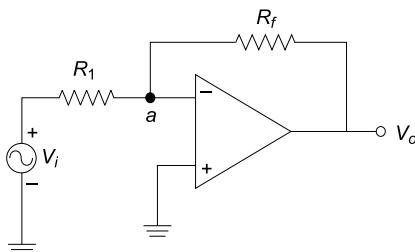
The input offset voltage  $V_{OS}$  is inadvertently introduced due to process imbalances such as mismatches in the output transistors and active load resistors. Figure 3.16(a) shows the op-amp with input offset voltage  $V_{OS}$  applied at the non-inverting terminal.



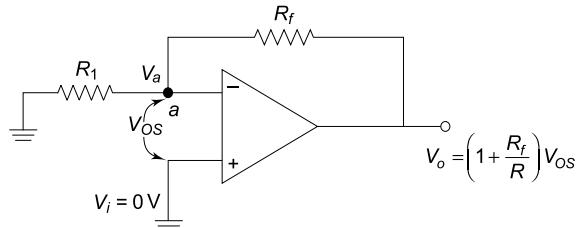
**Fig. 3.16 (a)** Op-amp with input offset voltage



**Fig. 3.16 (b)** Non-inverting amplifier



**Fig. 3.16 (c)** Inverting amplifier



**Fig. 3.16 (d)** Equivalent circuit for  $V_i = 0 \text{ V}$

Considering the non-inverting and inverting amplifier shown in Fig. 3.16(b) and (c), we have at the node  $a$ ,

$$V_a = V_o \left( \frac{R_1}{R_1 + R_f} \right)$$

or

$$V_o = \left( \frac{R_1 + R_f}{R_1} \right) V_a = \left( 1 + \frac{R_f}{R_1} \right) V_a \quad (3.22)$$

We know  $V_{OS} = (V_i - V_a)$  and with  $V_i = 0$ ,

$$V_{OS} = |(0 - V_a)| = V_a$$

or

$$V_o = \left(1 + \frac{R_f}{R_l}\right) V_{OS} \quad (3.23)$$

Therefore, Eq. (3.23) gives the effective output offset voltage in a closed-loop inverting and non-inverting configuration of op-amp.

### 3.6.4 Total Output Offset Voltage

The total output offset voltage  $V_{OT}$  can be due to either the input bias current or the input offset voltage, and also, it can be either positive or negative with respect to ground. Then, considering that both these output voltages are of same polarity, the maximum output offset voltage will be

$$V_{OT} = \left(1 + \frac{R_f}{R_l}\right) V_{OS} + R_f I_B \quad (3.24)$$

However, when  $R_{comp}$  is connected in the circuit, then the total output offset voltage will be

$$V_{OT} = \left(1 + \frac{R_f}{R_l}\right) V_{OS} + R_f I_{OS} \quad (3.25)$$

Since  $I_{OS} < I_B$ , it can be seen that the use of  $R_{comp}$  ensures a reduction in the output offset voltage generated due to bias current.

### Example 3.6

Assume that  $R_f = 10 k\Omega$ ,  $R_l = 2 k\Omega$ , input offset voltage  $V_{OS} = 5 mV$ , input offset current  $I_{OS} = 50 nA(\max)$  and input bias current  $I_B = 200 nA(\max)$  at  $T_A = 25^\circ C$ . Determine the maximum output offset voltage for circuit in Fig. 3.15 with  $R_{comp}$ .

**Solution** Using Eq. (3.24), the total output offset voltage without the compensating resistor  $R_{comp}$  is

$$\begin{aligned} V_{OT} &= \left(1 + \frac{R_f}{R_l}\right) V_{OS} + R_f I_B \\ &= \left(1 + \frac{10 \times 10^3}{2 \times 10^3}\right) 5 \times 10^{-3} + 10 \times 10^3 \times 200 \times 10^{-9} = 32 \text{ mV} \end{aligned}$$

When  $R_{comp}$  is used, using Eq. (3.25), the maximum output offset voltage is

$$\begin{aligned} V_{OT} &= \left(1 + \frac{R_f}{R_l}\right) V_{OS} + R_f I_{OS} \\ &= \left(1 + \frac{10 \times 10^3}{2 \times 10^3}\right) 5 \times 10^{-3} + 10 \times 10^3 \times 50 \times 10^{-9} = 30.5 \text{ mV} \end{aligned}$$

It is obvious that the output offset voltage due to input offset voltage is a more serious problem than the input bias current or input offset current.

### 3.6.5 Offset Voltage Compensation

The two methods of achieving offset voltage compensation are (i) op-amp with *offset null terminals* and (ii) providing an externally connected *offset compensation network*.

Figure 3.17(a) shows the circuit for offset null compensation for IC  $\mu$ A741. The offset compensation is achieved by the use of offset compensation pins made available by the manufacturers.

A 10 k $\Omega$  trimming potentiometer is connected between the offset null pins 1 and 5 and the variable terminal of the potentiometer is connected to the negative supply pin 4. The position of the variable terminal is so adjusted that the output voltage is zero or *nulled*, when both the input voltages are zero.

#### Nulling procedure

- Connect the circuit by including the compensating resistor  $R_{comp}$  and the voltage offset null circuit of Fig. 3.17(a)
- Make all generator (source) signals zero
- Connect the load to the output and turn the circuit ON
- Connect a dc voltmeter or an oscilloscope across the load to measure  $V_o$
- Vary the offset voltage adjustment trimming potentiometer until  $V_o$  becomes zero

Figures 3.17(b) and (c) show the compensation circuits for inverting and non-inverting amplifier circuits, when no offset null pins are provided by the manufacturer.

The resistive voltage divider formed by  $R_3$  and  $R_4$  in combination with potentiometer  $R_2$  form the external offset compensation network for canceling the

effects of  $V_{OS}$ . The input offset voltage is given by  $V_{OS}$

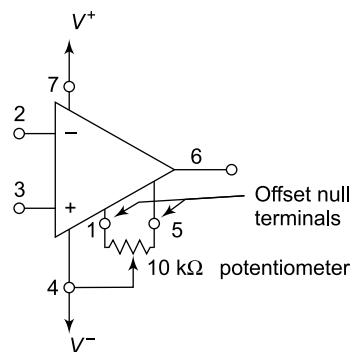
$$= \pm V \left( \frac{R_4}{R_3 + R_4} \right). \text{ When } R_4 \ll R_3, \text{ the compensating}$$

voltage applied at the non-inverting terminal can be of the order of millivolts, that forms the normal range of offset voltage values.

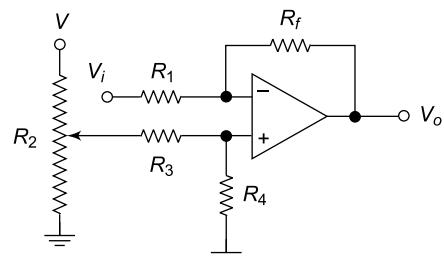
Figure 3.17(c) shows the compensation circuit for a non-inverting amplifier. It uses a potential divider formed by  $R_3$  and  $R_4$  along with potentiometer  $R_2$ . The input offset voltage is given by

$$V_{OS} = \pm V \left( \frac{R_4}{R_4 + R_3} \right)$$

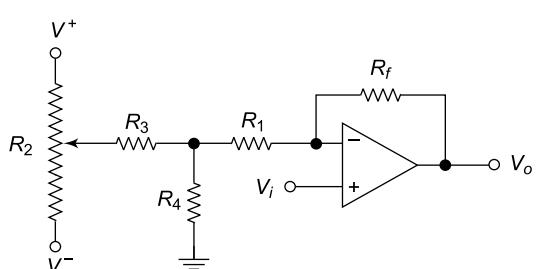
Normally, the typical value of  $R_4$  is 100 $\Omega$ , whereas  $R_3$  is around 100 k $\Omega$ . Assuming  $\pm 15$  V for supply voltages, the compensation voltage introduced is in the range of  $-15$  mV to  $+15$  mV.



**Fig. 3.17 (a)** Offset compensation circuit for  $\mu$ A741



**Fig. 3.17 (b)** Offset voltage compensation for an inverting amplifier



**Fig. 3.17 (c)** Offset voltage compensation for a non-inverting amplifier

Therefore, the gain of the amplifier can be approximated as given by

$$A_v = \frac{V_o}{V_i} = 1 + \frac{R_f}{R_l + R_4} \text{ since } R_4 \ll R_3.$$

### 3.6.6 Thermal Drift

It was assumed so far that the parameters  $V_{OS}$ ,  $I_B$  and  $I_{OS}$  are constant for a given op-amp. However, in practice, the following operating conditions pose a great challenge to these parameters:

- (i) Change in temperature  $\Delta T$
- (ii) Change in supply voltage and
- (iii) Change in time

The change in temperature causes the most serious variation in the values of  $V_{OS}$ ,  $I_B$  and  $I_{OS}$ . The term *thermal drift* is used to identify such changes and it is defined as the average rate of change of input offset voltage per unit change in temperature. It is denoted by  $\frac{\Delta V_{OS}}{\Delta T}$  with the unit  $\mu\text{V}/^\circ\text{C}$ . Similarly, the thermal drift in the input offset current is defined by  $\frac{\Delta I_{OS}}{\Delta T}$  with the unit ( $\text{pA}/^\circ\text{C}$ ) and thermal drift of the input bias current is defined by  $\frac{\Delta I_B}{\Delta T}$  with the unit of ( $\text{pA}/^\circ\text{C}$ ).

The thermal drift is not a constant value, and it is not uniform over a specified temperature range. Thus, a circuit effectively nulled at  $25^\circ\text{C}$  may not remain nulled at a higher temperature, say  $35^\circ\text{C}$ . Manufacturers specify either an average or maximum drift for two temperature limits and a plot of drift Vs temperature indicating the performance characteristics of op-amp.

### Example 3.7

---

An op-amp has the drift specifications as given below:

$$\frac{\Delta V_{OS}}{\Delta T} = 30 \mu\text{V}/^\circ\text{C}$$

$$\frac{\Delta I_{OS}}{\Delta T} = 0.2 \text{ nA}/^\circ\text{C}$$

$$R_f = 1 \text{ M}\Omega \text{ and } R_l = 100 \text{ k}\Omega$$

Assume that the output  $V_o = 0$  after nulling at  $25^\circ\text{C}$ . If the temperature is raised to  $75^\circ\text{C}$ , determine the maximum change in output voltage due to (a) drift in  $V_{OS}$  and (b) drift in  $I_{OS}$ .

**Solution** (a) The change in  $V_{OS}$  is given by

$$\pm 30 \mu\text{V}/^\circ\text{C} \times (75 - 25)^\circ\text{C} = 30 \times 10^{-6} \times 50 = \pm 1.5 \text{ mV}$$

Then, using Eq. 3.13, we get the error voltage in the output due to  $V_{OS}$  as given by

$$\begin{aligned} V_o &= V_{OS} \left( 1 + \frac{R_f}{R_l} \right) \\ &= \pm 1.5 \times 10^{-3} \left( 1 + \frac{1 \times 10^6}{100 \times 10^3} \right) = \pm 16.5 \text{ mV} \end{aligned}$$

(b) Change in  $I_{OS}$  is given by

$$\Delta I_{OS} = \pm 0.2 \times 10^{-9} / ^\circ C \times 50^\circ C = \pm 10 \text{ nA}$$

Change in  $V_o$  due to change in  $I_{OS}$  is

$$\Delta V_{OS} = \pm 10 \text{ nA} \times R_f = \pm 10 \times 10^{-9} \times 1 \times 10^6 = \pm 10 \text{ mV}$$

The changes in  $V_o$  caused by variation due to  $V_{OS}$  and  $I_{OS}$  can either add to or subtract from one another. Hence, the worst case drift is given by

$$+16.5 \text{ mV} + 10 \text{ mV} = 26.5 \text{ mV}$$

$$\text{or } -16.5 \text{ mV} - 10 \text{ mV} = -26.5 \text{ mV}$$

### 3.6.7 Power Supply Rejection Ratio (PSRR) or Supply Voltage Rejection Ratio (SVRR)

The internal circuitry of an op-amp is very sensitive to variations in supply voltages. Hence, the power supply used for the op-amp is preferred to have low noise and good regulation characteristics. This sensitivity is indicated by the *maximum offset voltage versus supply voltage*. The reciprocal of sensitivity is defined as the Power Supply Rejection Ratio (PSRR) or Supply Voltage Rejection Ratio (SVRR).

This parameter is normally expressed using *Power Supply Rejection* (PSR) value, which is expressed logarithmically as

$$PSR = 20 \log_{10} (PSRR)$$

Assuming that an op-amp has 10  $\mu\text{V}$  per Volt of offset change, this would result in a PSRR of

$$\frac{1 \text{ V}}{10 \mu\text{V}} = 10^5 \text{ and PSR of } 20 \log_{10} 10^5 = 100 \text{ dB.}$$

#### Example 3.8

Consider an op-amp with PSR of 90 dB. When the op-amp is operated with a power supply, whose peak-to-peak supply voltage ripple is of 0.5 V magnitude, find out the effect of ripple at the output of op-amp.

#### Solution

$$PSRR = \text{Antilog } \frac{PSR}{20} = \text{Antilog } \frac{90}{20} = 33333.33$$

The output ripple voltage is given by

$$V_{o,\text{ripple}} = \frac{V_{\text{in,ripple}}}{PSRR} = \frac{0.5 \text{ V}}{33333.33} = 15 \mu\text{V} \text{ (peak-to-peak)}$$

### 3.7 AC PERFORMANCE CHARACTERISTICS OF OP-AMP

When an op-amp is used in a circuit for amplifying only ac signal, the first design consideration is that of identifying whether the ac output voltage will be *small signal* (less than about IV peak) or *large signal* (more than about IV peak).

When only ac output signal is present, the primary design consideration is determined by *noise* and *frequency response*. On the other hand, when large ac output signal is aimed at in the design, then the slew rate *limiting* characteristics of op-amp decides whether distortion will be introduced by the op-amp that may further limit the frequency response.

Therefore, the ac response characteristics to be studied are:

- (i) Frequency response
- (ii) Bandwidth and
- (iii) Slew rate

### 3.7.1 Frequency Response

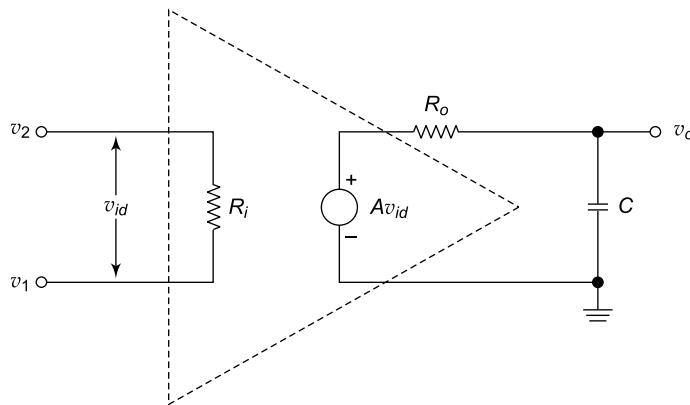
The gain of the op-amp is assumed a constant for dc and very low frequencies of operation. However, it is observed in practice that the gain is a complex number and a function of frequency. At a given frequency, the gain  $A$  has a certain magnitude and a phase angle.

Any change in operating frequency causes variation in gain magnitude and phase angle. Therefore, *frequency response* is defined as the manner in which, the gain of the op-amp responds to different frequencies. The frequency response plot shows the magnitude of gain Vs frequency, and it is provided in the data sheet of op-amp.

Ideally, an op-amp is expected to have an infinite bandwidth. If the open-loop gain is specified as a particular value, it must remain the same throughout the audio and high radio frequency ranges. However, the gain of a practical op-amp decreases or *rolls-off* at higher frequencies. The decreasing gain of the op-amp can be attributed to a capacitive component included in the equivalent circuit of the op-amp. Two major sources can be considered responsible for this capacitive component.

- (i) The physical characteristics of semiconductor devices, such as BJTs and FETs which inherently contain junction capacitors. The junction capacitors are very small, of the order of picofarads and they act as open-circuits at low frequencies and as reactive paths at higher frequencies. As the frequency increases, the reactance decreases.
- (ii) The internal construction of the op-amp with transistors, resistors and capacitors integrated on the same *substrate* introduce parasitic or stray capacitances, wherever two conducting paths are found separated by insulator, which, in effect, creates a capacitor.

The combined effect of these capacitances reduces the gain of op-amp at high frequencies. The high frequency model of an op-amp with only one break frequency and all the capacitor effects represented by a single capacitor  $C$  is shown in Fig. 3.18.



**Fig. 3.18** High frequency model of an op-amp with a single corner frequency

### 3.7.2 Open-loop Gain as a Function of Frequency

Figure 3.18 is the modified version of Fig. 3.4 with a capacitor  $C$  at the output. Using the voltage divider rule, we have

$$v_o = \left( \frac{1/j\omega C}{R_o + 1/j\omega C} \right) A_o v_{id}$$

Therefore, the open-loop gain  $A$  is given by

$$A = \frac{v_o}{v_{id}} = \frac{A_0}{1 + j\omega R_o C}$$

Substituting  $f_1 = \frac{1}{2\pi R_o C}$ , we have

$$A = \frac{A_0}{1 + j(f/f_1)} \quad (3.26)$$

where  $A$  is the open-loop voltage gain as a function of frequency and  $f_1$  is the break frequency or the dominant-pole frequency of the op-amp and  $A_0$  is the voltage gain of the op-amp at 0 Hz (dc) or the low frequency open-loop gain.

Equation (3.26) indicates that the open-loop gain  $A$  is a complex quantity dependent on operating frequency.

The magnitude of open-loop gain is

$$= \frac{A_0}{\sqrt{1 + (f/f_1)^2}} \quad (3.27)$$

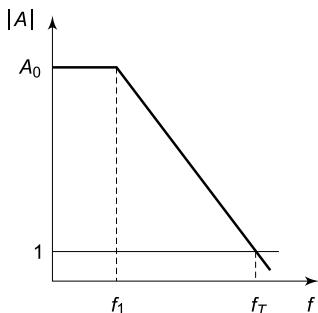
and phase angle is

$$\phi(f) = -\tan^{-1}(f/f_1) \quad (3.28)$$

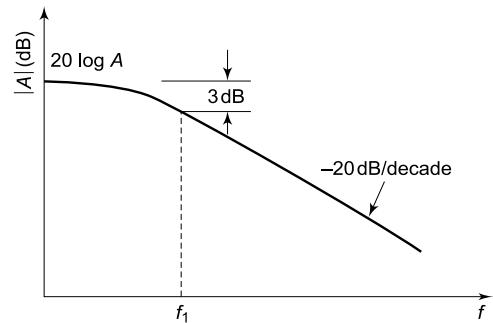
Equations (3.27) and (3.28) can be used to plot the magnitude vs frequency and phase angle vs frequency curves respectively as shown in Fig. 3.19(a), (b) and (c) where Fig. 3.19(a) shows the Bode plot open-loop gain magnitude and Fig. 3.19(b) shows the open-loop gain magnitude characteristics on a semi-log scale. Fig. 3.19(c) shows the phase characteristic with single break frequency.

The following observations can be made from Figs. 3.19(a) and (b).

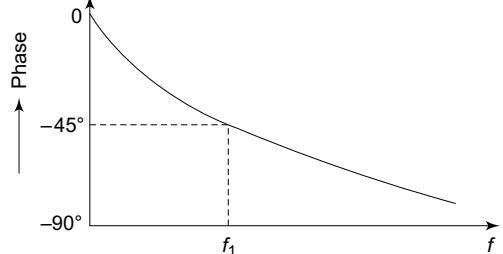
- (i) The open-loop gain  $A$  is approximately constant from 0 Hz to break frequency  $f_1$ .
- (ii) When  $f = f_1$ , the gain  $A$  is 3 dB down from its value at 0 Hz. Hence, the break frequency is called  $-3 \text{ dB}$  frequency or *corner frequency*.
- (iii) For  $f > f_1$ , the open-loop gain rolls-off at a rate of  $-20 \text{ dB/decade}$  or  $-6 \text{ dB/octave}$ .
- (iv) At a particular input frequency  $f_T$  shown, the open-loop gain  $A$  is unity, or gain in dB is zero. This is called the *unity gain-bandwidth*, small-signal bandwidth and unity gain cross-over frequency. The unity gain-bandwidth of IC 741C is approximately 1 MHz.
- (v) From Fig. 3.19(c), the phase angle is zero at  $f = 0$ , and at  $f = f_1$ , the phase angle is  $-45^\circ$  (lagging) and at infinite frequency, the phase angle is  $-90^\circ$ .



**Fig. 3.19 (a)** Bode plot open-loop gain magnitude



**Fig. 3.19 (b)** Open-loop gain (log magnitude)



**Fig. 3.19 (c)** Phase characteristics with single break frequency

This indicates that a maximum of  $90^\circ$  phase shift between the input and output voltages can occur in an op-amp with a single capacitor.

The voltage transfer function for a single stage is expressed by

$$\begin{aligned} A &= \frac{A_0}{1 + j(f/f_1)} = \frac{A_0}{1 + j(\omega/\omega_1)} \\ &= \frac{A_0 \omega_1}{j\omega + \omega_1} = \frac{A_0 \omega_1}{s + \omega_1} \end{aligned}$$

However, a practical op-amp has a number of stages and each stage contributes for a capacitive component. Therefore, due to a number of  $RC$  pole pairs, there will be an equal number of different corner frequencies. Therefore, the transfer function of an op-amp with three break frequencies can be written as

$$A = \frac{A_0}{\left(1 + j\frac{f}{f_1}\right)\left(1 + j\frac{f}{f_2}\right)\left(1 + j\frac{f}{f_3}\right)} \quad (3.29)$$

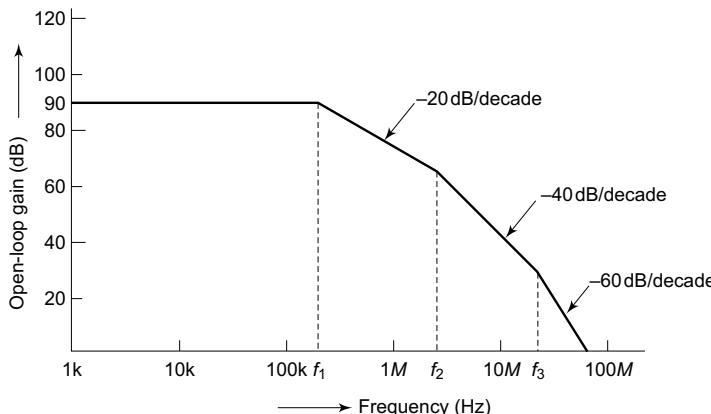
where  $0 < f_1 < f_2 < f_3$ .

It can also be written as

$$A = \frac{A_0 \omega_1 \omega_2 \omega_3}{(s + \omega_1)(s + \omega_2)(s + \omega_3)}$$

where  $0 < \omega_1 < \omega_2 < \omega_3$ .

Figure 3.20 shows the typical op-amp straight line approximation of open-loop gain vs frequency in logarithmic scale.



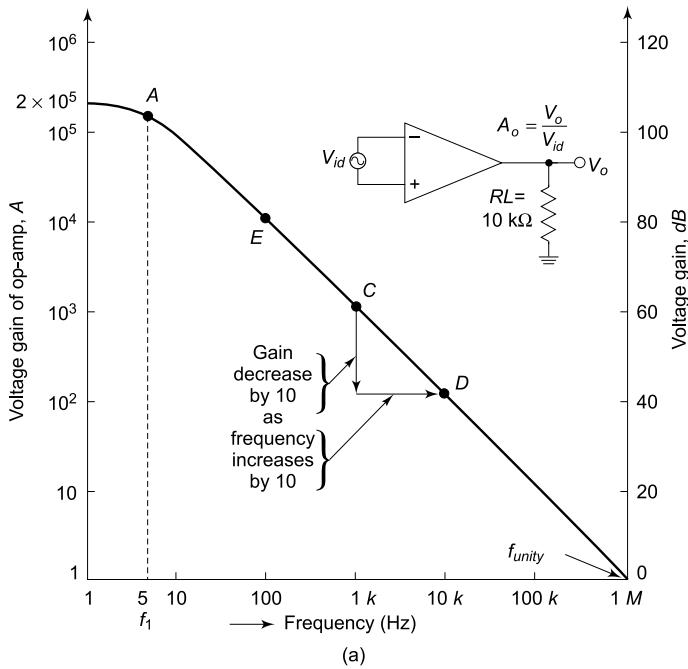
**Fig. 3.20** Open-loop gain vs frequency curve

The first break frequency occurs at 200 kHz and frequency response is flat at 90 dB. The gain drops from 90 dB to 70 dB for the frequency range from 200 kHz to 2 MHz at  $-20$  dB/decade or  $-6$  dB/octave rate. As frequency increases, the cascading effect of  $RC$  pairs or poles takes effect and correspondingly, the roll-off rate increases successively by  $-20$  dB/decade at each of the corner frequencies. For the frequency range from 2 MHz to 20 MHz, the roll-off rate is  $-40$  dB/decade or  $-12$  dB/octave. Each pole pair also introduces a phase lag at a maximum of  $-90^\circ$ .

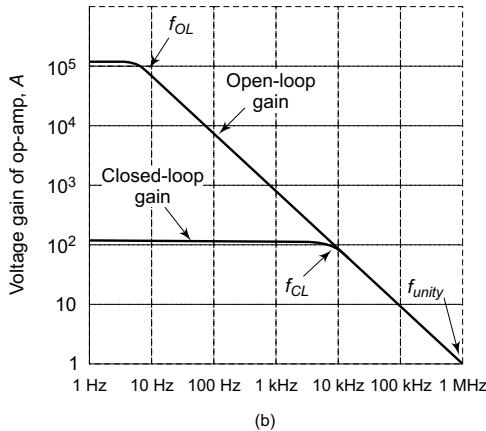
Figure 3.21(a) shows the open-loop voltage gain vs frequency for a 741 op-amp. The open-loop gain has a maximum value of 200,000. When the operating frequency increases to 5 Hz, the open-loop

gain is down to 0.707 of its maximum value. The gain keeps dropping off with increasing frequency. After the upper cut-off frequency  $f_i$ , the gain drops by 20 dB/decade. The unity-gain frequency is the frequency where the open-loop gain has decreased to unity. In Fig. 3.21(a),  $f_{unity}$  equals 1 MHz.

The closed-loop gain curve shown in Fig. 3.21(b) represents the closed-loop response of an op-amp against the open-loop gain. It can be seen that the open-loop gain decreases continuously until it approaches the value of closed-loop gain. Then, the closed-loop gain starts to decrease and at  $f_{CL}$ , the closed-loop gain is down to 0.707 of its maximum value. Thereafter, both the curves superimpose and decrease to unity at  $f_{unity}$ .



(a)



(b)

**Fig. 3.21** (a) Open-loop voltage gain vs frequency response for IC 741  
 (b) Closed-loop and open-loop gain responses

If the feedback resistors are changed, the closed-loop gain will change to a new value and so will the closed-loop cut-off frequency. Since the gain-bandwidth product is constant, the closed-loop curve superimposes on the open-loop curve beyond cut-off frequency.

The specification sheets normally present

- manufacturer's plot of *open-loop gain A* versus *frequency*, with the point  $f_{\text{unity}}$  indicating the frequency where  $A = 1$
- specification called *transient response time (unity gain)*, which is typically  $0.25 \mu\text{s}$  and  $0.8 \mu\text{s}$  at maximum for 741 op-amp. The bandwidth  $BW$  is determined from the rise time specification by using the relation

$$BW = \frac{0.35}{\text{Rise time}}$$

- the product of the open-loop gain  $A$  of the op-amp and the frequency of operation  $f$  provides the bandwidth  $BW$ . For example, given  $A = 100$  at a frequency of  $15 \text{ kHz}$ , the bandwidth is given by

$$BW = A \times f$$

That is,

$$BW = 15 \times 10^3 \times 100 = 1.5 \text{ MHz}$$

The op-amp and a few resistors form an amplifier, and the frequency response depends on the frequency response of the op-amp. The voltage gain of the op-amp decreases at high frequencies. This is due to the parasitic junction capacitance and minority-carrier charge storage in devices making up the circuit. This aspect of op-amp is characterized by the gain-bandwidth product, which is the bandwidth of the op-amp when the voltage gain is unity. Equivalent terms for gain-bandwidth product are closed-loop bandwidth, unity gain-bandwidth and small-signal bandwidth. For general purpose op-amps, the gain-bandwidth product is in the range of 1 to 20 MHz. The *small signal unity gain-bandwidth* characteristic is an important parameter of an op-amp. For an op-amp with a single break frequency  $f_1$ , the gain-bandwidth product is constant and it can be written as

$$\text{UGB} = A_0 f_1$$

where  $A_0$  is the open-loop dc voltage gain and

$f_1$  is the break frequency of the op-amp

A typical data sheet presents the unity gain-bandwidth (UGB) instead of the corner frequency  $f_1$ , and  $f_1$  can be calculated using the equation

$$f_1 = \frac{\text{UGB}}{A_0} \quad (3.30)$$

### Example 3.9

The frequency response of IC 741C is shown in Fig. 3.22. Determine the gain that can be used to have a maximally flat response at  $1 \text{ kHz}$ .

**Solution** Referring to the frequency response plot, the  $1\text{kHz}$  point is projected vertically to the curve as shown in Fig. 3.22. Reading the corresponding value of gain gives  $+60 \text{ dB}$ , i.e. a gain of 1000.

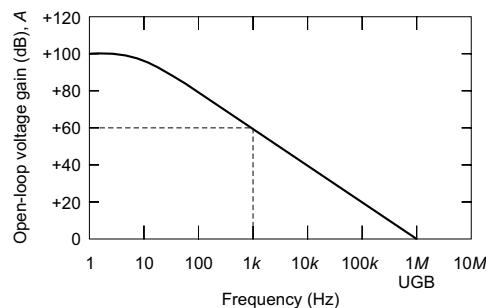


Fig. 3.22

**Example 3.10**

An op-amp has a rise time of  $0.7 \mu\text{s}$ . Determine the small signal or unity gain-bandwidth.

**Solution** Given rise time =  $0.7 \mu\text{s}$

$$\text{Therefore, bandwidth } BW = \frac{0.35}{\text{Rise time}} = \frac{0.35}{0.7 \times 10^{-6}} = 500 \text{ kHz}$$

**3.7.3 Bandwidth with Feedback**

The bandwidth of an amplifier is defined as the range of frequencies within which the gain remains constant. The gain-bandwidth product of an op-amp is always constant. The gain of an op-amp and its bandwidth are inversely proportional to one another. The bandwidth of an op-amp can be increased by providing feedback signal to its input. Consider the following statement. The product of closed-loop gain  $A_v$  and closed-loop bandwidth  $BW_{CL}$  is same as the product of open-loop gain and open-loop bandwidth. That is,

$$A_v \times BW_{CL} = A_0 \times BW_{OL} \quad (3.31)$$

The op-amp 741 has an open-loop gain of 200,000 and a bandwidth of about 5 Hz. Therefore, the product of its open-loop gain and bandwidth is

$$A_0 \times BW_{OL} = 200,000 \times 5 = 1 \text{ MHz.}$$

The open-loop gain-bandwidth product of the 741 is 1 MHz. For any values of  $R_1$  and  $R_f$ , the product of closed-loop gain and closed-loop bandwidth must equal the open-loop gain-bandwidth product, i.e. for 741, the closed-loop gain-bandwidth product must be 1 MHz.

**Example 3.11**

An op-amp has a unity gain-bandwidth of 1.5 MHz. For a signal of frequency 2 kHz, what is the open-loop dc voltage gain?

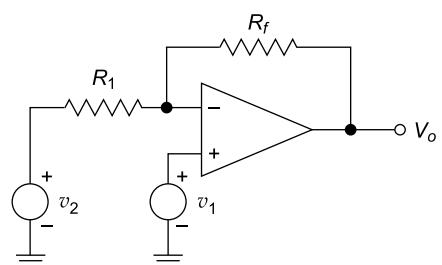
**Solution** Given UGB = 1.5 MHz and  $f_1 = 2 \text{ kHz}$ .

$$\text{The open-loop dc voltage gain, } A_0 = \frac{\text{UGB}}{f_1} = \frac{1.5 \times 10^6}{2 \times 10^3} = 750$$

**3.7.4 Closed-loop Frequency Response**

The op-amp is generally used in a closed-loop configuration. The open-loop gain  $A$  is maintained constant only up to the first corner frequency  $f_1$ , which is the maximum useful frequency of the open-loop op-amp. Hence, the bandwidth of the op-amp is very small. Ideally, we expect the bandwidth of an amplifier to be infinite, so that the gain remains constant at all frequencies. Therefore, a negative feedback can be used to make the op-amp versatile as shown in Fig. 3.23.

It uses a resistor feedback network forming a non-inverting amplifier for input  $v_2 = 0$  and an inverting amplifier for input  $v_1 = 0$ .



**Fig. 3.23** Feedback in op-amp

The closed-loop transfer function can be written as

$$A_v = \frac{A_0}{1 + A_0\beta} \quad (3.32)$$

where  $A_0$  is the open-loop voltage gain and  $\beta$  is the feedback ratio. When the denominator  $(1 + A_0\beta) = 0$ , the circuit becomes unstable that leads to sustained oscillation.

Rearranging, we get the loop-gain as given by

$$-A_0\beta = 1$$

Here,  $A_0\beta$  is a complex quantity, and the magnitude is given by

$$|A_0\beta| = 1 \quad (3.33)$$

and phase condition is

$$\boxed{|A_0\beta| = 0 \text{ (or integral multiple of } 2\pi)}$$

or

$$\boxed{|A_0\beta| = \pi \text{ (or odd multiple of } \pi)}$$

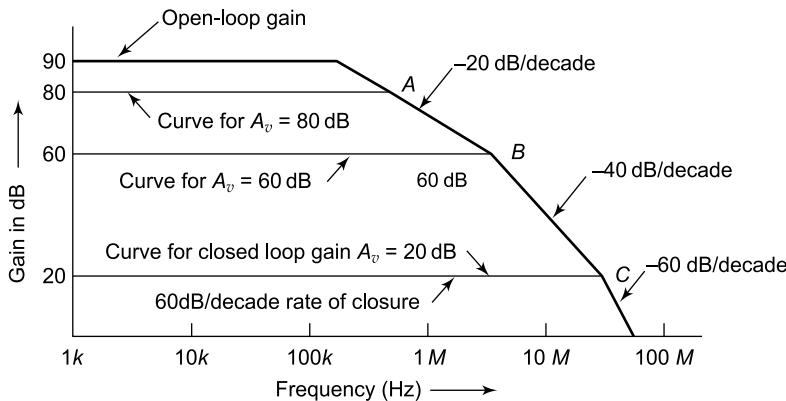
Here,  $\beta$  is a constant if only resistive components are used, and hence, they do not provide any phase shift. Using Eq. (3.32), when  $(1 + A_0\beta) < 0$ ,  $A\beta < 0$  or  $A\beta$  is negative, instability or unbounded output may result.

Then,

$$A_v > A_0$$

The performance of the circuit at high frequencies and low frequencies can be explained using Fig. 3.24.

At high frequencies, due to each corner frequency, a phase shift of maximum  $-90^\circ$  may result in the open-loop gain  $A_0$  shown as a darker line. The maximum phase shift for two corner frequencies can be  $-180^\circ$ . Therefore, at high frequencies, for some value of  $\beta$ ,  $|A_0\beta|$  may become unity and total phase shift around the loop may be made zero. Then, the amplifier may start oscillating, and instability will set in. At low frequency, additional phase shift is zero. Hence,  $A_0\beta > 0$ . This makes the closed-loop gain  $A_v < A_0$  and the system becomes stable. Figure 3.24 shows the effect of feedback on open-loop gain with three corner frequencies and hence three  $RC$  pole pairs.



**Fig. 3.24** Effect of feedback on open-loop gain Vs frequency characteristics

Assuming a closed-loop gain of 80 dB is required, projecting the point horizontally to intersect on the open-loop response curve at point *A* shows a closed-loop bandwidth of around 600 kHz. The  $-20$  dB/decade rate of closure at *A* results in a maximum of  $-90^\circ$  phase shift. If feedback resistors are chosen for 60 dB (or 1000) gain, the bandwidth is 3.5 MHz as shown in Fig. 3.24. The 60 dB projection intersects

the open-loop curve at  $-40$  dB/decade rate of closure, and the maximum phase shift obtainable is  $(-90^\circ - 90^\circ) = -180^\circ$ . Hence, the circuit may be unstable. Similarly, a closed-loop gain of  $-20$  dB results in a maximum of  $-270^\circ$  phase shift creating instability.

The transfer function of an op-amp with three corner frequencies is given by

$$A = \frac{A_0 \omega_1 \omega_2 \omega_3}{(s + \omega_1)(s + \omega_2)(s + \omega_3)}$$

where  $0 < \omega_1 < \omega_2 < \omega_3$ . The poles of the open-loop transfer function are at  $\omega_1$ ,  $\omega_2$  and  $\omega_3$ .

The poles of the closed-loop transfer function are given by the use of the equation  $1 + A\beta = 0$

That is,

$$1 + \frac{\beta A_0 \omega_1 \omega_2 \omega_3}{(s + \omega_1)(s + \omega_2)(s + \omega_3)} = 0$$

## 3.8 FREQUENCY COMPENSATION

When wider bandwidth and limited closed-loop gain are required, suitable compensation techniques are employed. The two types of compensation techniques used in practice are

- (i) External frequency compensation and
- (ii) Internal frequency compensation

### 3.8.1 External Frequency Compensation

The compensating network is connected externally to the op-amp for modifying the response suiting the requirements. The compensating network alters the response so that  $-20$  dB/decade of roll-off rate is achieved over a broad range of frequency.

The commonly used external compensation methods are

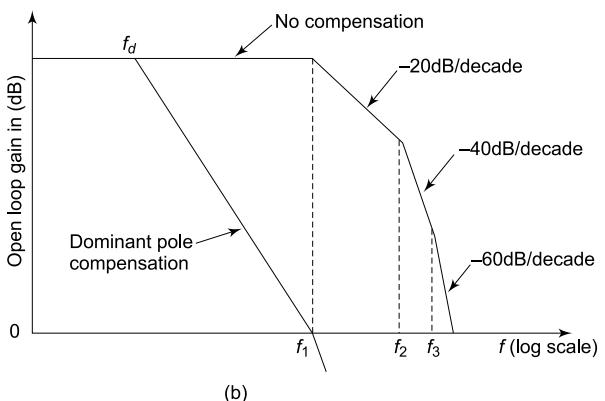
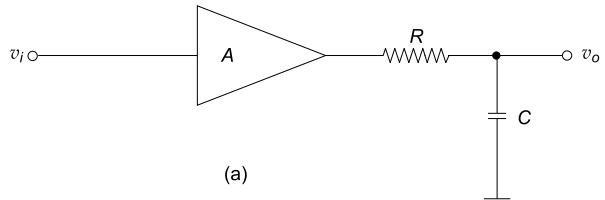
- (i) Dominant-Pole compensation
- (ii) Pole-Zero (lag) compensation
- (iii) Miller effect compensation

**Dominant-pole compensation** Assume  $A$  is the uncompensated transfer function of an open-loop op-amp, whose transfer function is given by

$$A = \frac{A_0 \omega_1 \omega_2 \omega_3}{(s + \omega_1)(s + \omega_2)(s + \omega_3)} \quad (3.34)$$

where  $0 < \omega_1 < \omega_2 < \omega_3$ .

Figure 3.25(a) shows a dominant-pole compensation network by adding an  $RC$  network in series with an op-amp, or it can be achieved by connecting a capacitor  $C$  at a suitable high resistance node with respect to ground.



**Fig. 3.25** (a) Dominant-pole compensation  
(b) Gain Vs frequency characteristics for dominant pole compensation

Then, the compensated transfer function  $A'$  after compensation is given by

$$A' = \frac{v_o}{v_i} = A_0 \left( \frac{\frac{1}{j\omega C}}{R + \frac{1}{j\omega C}} \right) = \frac{A_0}{1 + j(f/f_d)}$$

where  $f_d = \frac{1}{2\pi RC}$  is the break frequency of the compensating network. Using Eq. (3.34), we get the compensated transfer function as

$$A' = \frac{A_0}{\left(1 + j\frac{f}{f_d}\right)\left(1 + j\frac{f}{f_1}\right)\left(1 + j\frac{f}{f_2}\right)\left(1 + j\frac{f}{f_3}\right)}$$

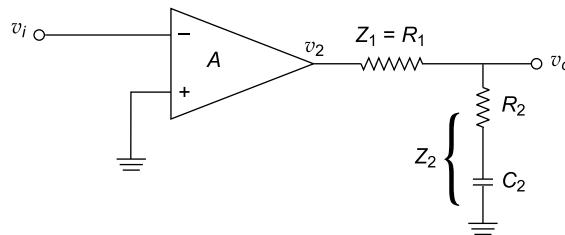
where  $f_d < f_1 < f_2 < f_3$ .

The capacitance  $C$  is selected such that, the modified loop gain drops down to 0 dB with a roll-off rate as given by 20 dB/decade at a frequency, where the poles of the uncompensated system transfer function  $A$  contributes negligible phase shift. Normally, the break frequency  $f_d = \frac{\omega_d}{2\pi}$  is selected so that, the transfer function  $A'$  passes through 0 dB at the pole  $f_1$  of  $A$ . The uncompensated and compensated magnitude plots are shown in Fig. 3.25(b).

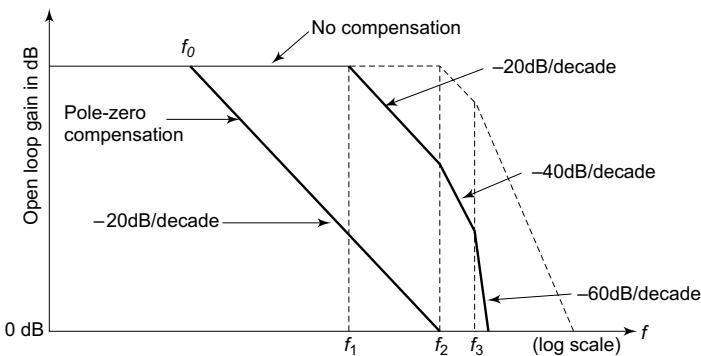
The main disadvantage of this compensation technique is that, the bandwidth of the op-amp circuit reduces drastically from  $f_1$  to  $f_d$  as shown in Fig. 3.25(b). However, the advantage derived from this method is the improved noise immunity of the system, since the noise components outside the reduced bandwidth are eliminated.

**Pole-zero compensation** In this method, both a pole and a zero are added to the uncompensated transfer function  $A$ . Figure 3.26(a) shows the circuit arrangement of the pole-zero compensation method. The zero is added at a higher frequency than the pole. The transfer function of the compensation network is given by

$$\frac{v_o}{v_2} = \frac{Z_2}{Z_1 + Z_2} = \frac{\frac{R_2 + \frac{1}{jX_{C2}}}{R_1 + R_2 + \frac{1}{jX_{C2}}}}{1}$$



**Fig. 3.26 (a)** Pole-zero compensation



**Fig. 3.26 (b) Its open-loop Vs frequency response**

where  $Z_1 = R_1$  and  $Z_2 = R_2 + \frac{1}{j\omega C_2}$ .

That gives

$$\frac{v_o}{v_2} = \frac{1 + j\omega R_2 C_2}{1 + j\omega(R_1 + R_2)C_2} = \frac{1 + \left(j\frac{f}{f_1}\right)}{1 + \left(j\frac{f}{f_0}\right)}$$

where

$$f_1 = \frac{1}{2\pi R_2 C_2}$$

and

$$f_0 = \frac{1}{2\pi(R_1 + R_2)C_2}$$

The compensating network introduces a zero at the first corner frequency  $f_1$  of uncompensated transfer function represented by  $A'$ , which cancels the effect of pole at  $f_1$ . The pole of the compensation network at  $f_0$  given as  $\frac{\omega_0}{2\pi}$  is selected such that the compensated transfer function  $A'$  passes through 0 dB at the second corner frequency  $f_2$  shown in the uncompensated transfer function  $A$  of Eq. (3.29). This is shown in Fig. 3.26(b) graphically by having  $A'$  passing through 0 dB at frequency  $f_2$  with a slope of  $-20$  dB/decade. The overall transfer function of the amplifier with compensation network is given by

$$A' = \frac{v_o}{v_i} = \frac{v_o}{v_2} \times \frac{v_2}{v_i} = \frac{\left(1 + j\frac{f}{f_1}\right)}{\left(1 + j\frac{f}{f_0}\right)} \times \frac{A_0}{\left(1 + j\frac{f}{f_1}\right)\left(1 + j\frac{f}{f_2}\right)\left(1 + j\frac{f}{f_3}\right)}$$

Therefore,

$$A' = \frac{A_0}{\left(1 + j\frac{f}{f_0}\right)\left(1 + j\frac{f}{f_2}\right)\left(1 + j\frac{f}{f_3}\right)} \quad (3.35)$$

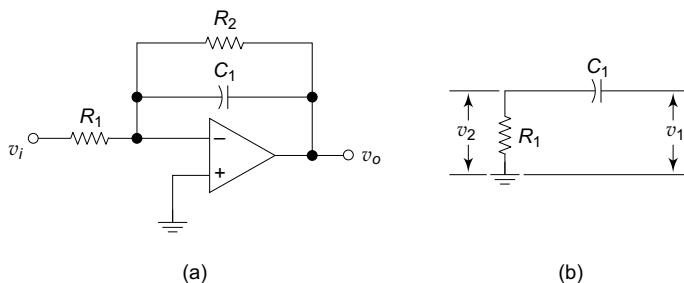
where  $0 < f_0 < f_2 < f_3$ .

A comparison of the compensating techniques using dominant pole and pole-zero methods can be made using Fig. 3.25(b) and Fig. 3.26(b). The dominant pole is selected such that the compensated transfer function passes through 0 dB at  $f_1$ , which is the first pole of the uncompensated function, whereas the zero is chosen

at  $f_1$  and pole is selected at  $f_2$ . Therefore, the compensated transfer function passes through 0 dB at the second pole  $f_2$  of the uncompensated transfer function in the pole-zero compensation technique.

Therefore, the resultant advantage is the improved bandwidth of value  $(f_2 - f_1)$ . Since the size of the compensation capacitance is large, forbidding the integration of capacitor with the op-amp, normally standard IC op-amps have external pins provided to facilitate the external component connection. This drawback is eliminated in Miller effect compensation method, which employs the Miller effect.

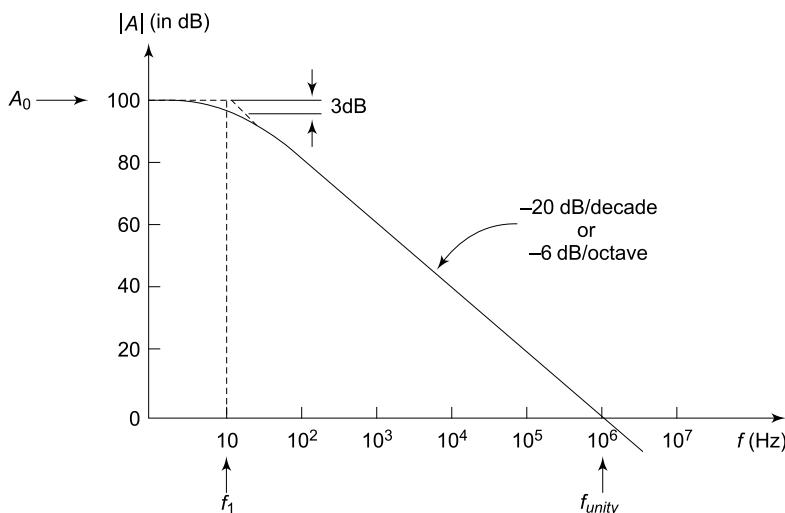
**Miller effect compensation** Figure 3.27(a) shows the op-amp inverting amplifier with capacitor  $C_1$  connected in parallel with the feedback resistor  $R_2$ . The combination of  $C_1$  and  $R_1$  behaves as phase-lead network in the feedback loop of op-amp as shown in Fig. 3.27(b). Thus,  $C_1$  and  $R_1$  introduce a phase lead to cancel some amount of phase lag in the loop.



**Fig. 3.27** Miller effect compensation: (a) Inverting amplifier with Miller capacitor  
(b) Phase lead network of the compensated op-amp

### 3.8.2 Internal Frequency Compensation

Broad bandwidth may not be the only criterion required in some applications like instrumentation. In such cases, internally compensated op-amps called *compensated op-amps* can be employed. They are found to be stable regardless of the value of closed-loop gain and without any external compensation methods. The frequency response of  $\mu$ A741 op-amp which is internally compensated is reproduced in Fig. 3.28.



**Fig. 3.28** Frequency response of  $\mu$ A741 op-amp

The op-amp 741 internally contains a capacitance of 30 pF that shunts off the signal current at higher frequencies, leading to decrease in output signal. This internal compensating capacitor causes the open-loop gain to roll-off at  $-20$  dB/decade rate that assures a stable characteristic for the circuit.

The op-amp 741 has a gain-bandwidth ( $GBW$ ) product of 1 MHz. This represents that the product of gain and frequency at any point on the open-loop gain Vs frequency curve is 1MHz. If the op-amp is connected for a gain of 60 dB, or  $10^3$ , then the bandwidth obtainable is 1 kHz. For a gain of 10, the bandwidth increases to 100 kHz.

Note that the gain bandwidth product is also identified normally as  $GBP$ .

Some of the internally compensated op-amps are LM741, LM107 and LM112 from National Semiconductor, MC1558 from Motorola and  $\mu$ A741 from Fairchild.

### 3.8.3 Slew Rate

Slew rate is an important parameter which limits the bandwidth for large signals and it indicates how fast its output voltage can change. It is defined as the maximum rate of change of output voltage realised by a step input voltage, and it is usually specified in units of  $V/\mu s$ . The slew rate of the op-amp is related to its frequency response. The op-amps with wide bandwidth have better slew rates. Slew rate limiting affects all amplifiers where capacitance on internal nodes, or as part of the external load, has to be charged and discharged as voltage levels vary.

The general purpose op-amps such as the 741 have a maximum slew rate of  $0.5 V/\mu s$ , which means that the output voltage can change at a maximum of  $0.5 V$  in  $1 \mu s$ . The slew rate is usually specified at unity gain and no-load, and it improves with higher closed-loop gain and dc supply voltage.

**Cause of slew rate limiting** The slew rate is determined by a number of factors such as the amplifier gain, compensating capacitors and the change in polarity of output voltage. It is also a function of temperature and the slew rate generally reduces due to rise in temperature.

The capacitor within or outside the op-amp is required to prevent oscillation and this capacitor restricts the response of op-amp to a rapidly changing input signal. The rate at which the voltage across the capacitor  $V_c$  increases is given by  $\frac{dv_c}{dt} = \frac{I}{C}$  where  $I$  is the current furnished by the internal circuit. This means that the op-amp must have either a higher current or a small compensation capacitor. For example, the IC 741 can provide  $15 \mu A$  of maximum current to its internal  $30 \text{ pF}$  capacitor. That is,

$$\text{Slew rate} = \frac{\text{Output voltage change}}{\text{Time}} = \frac{dv_c}{dt} \Big|_{\max} = \frac{I_{\max}}{C} = \frac{15 \mu A}{30 \text{ pF}} = 0.5 V/\mu s$$

Therefore, slew rates of value more than  $100 V/\mu s$  are called as *high-speed* op-amps and slew rates greater than  $100 V/\mu s$  are available for special applications such as video systems.

**Slew rate limiting of sine-wave** The slew rate limits the speed of response of all the large signal wave-shapes. Figure 3.29 shows  $v_i$  as a large amplitude, high frequency sine-wave with a peak amplitude of  $V_m$ .

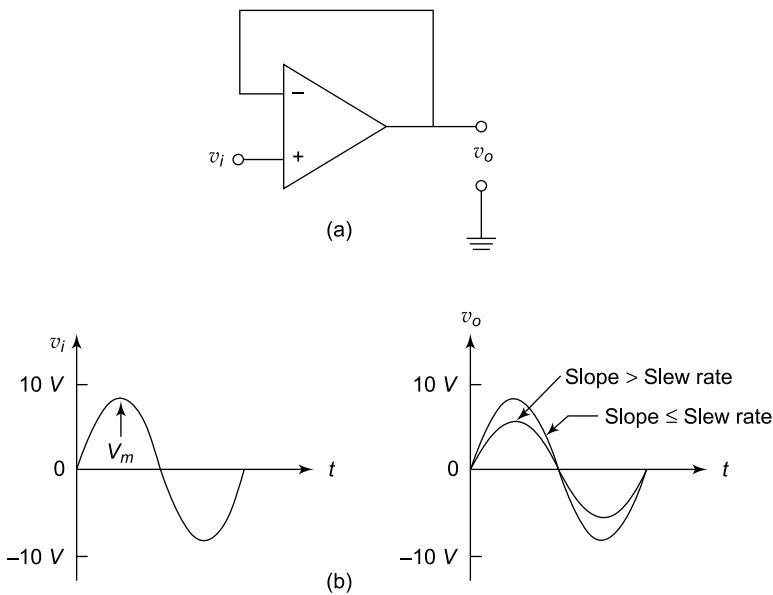
$$v_i = V_m \sin \omega t$$

Therefore, the output

$$v_o = V_m \sin \omega t$$

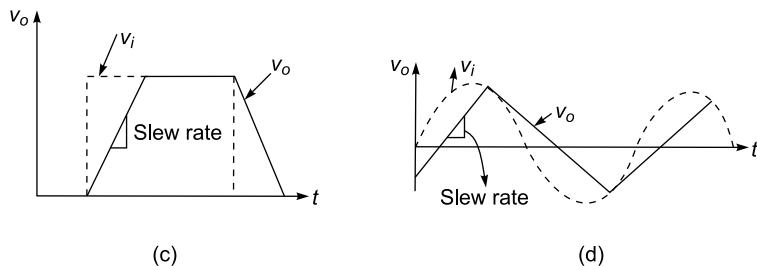
The rate of change of output is given by

$$\frac{dv_o}{dt} = V_m \omega \cos \omega t$$



**Fig. 3.29** Slew rate limiting of sine wave: (a) Voltage follower (b) Input and output waveforms

The effect of slew rate limiting on a pulse input and a sine wave input is shown in Fig. 3.29(c) and (d).



**Fig. 3.29** Effect of slew rate limiting: (c) pulse input and output (d) Sinusoidal input and output

The maximum rate of change of the output occurs when  $\cos \omega t = 1$ .

That is,

$$\text{slew rate} = \frac{dv_o}{dt} \Big|_{\max} = V_m \omega$$

or,

$$\text{slew rate, } SR = 2\pi f V_m \text{ V/s} \quad (3.36)$$

The maximum frequency  $f_{\max}$  at which an undistorted output voltage with a peak value  $V_m$  can be obtained is determined by

$$f_{\max} = \frac{\text{Slew rate}}{2\pi V_m} \quad (3.37)$$

The maximum peak sinusoidal output voltage  $V_{m(\max)}$  that can be obtained at a frequency of  $f$  is given by

$$V_{m(\max)} = \frac{\text{Slew rate}}{2\pi f} \quad (3.38)$$

**Full power bandwidth** The effect of slew rate limiting is the resulting distortion in the output signal, when the op-amp circuit is operated beyond its slew-rate capabilities. This is illustrated through examples 3.12 to 3.18.

To cite using an example and elaborate, consider a sinusoidal input  $v_i$  of Fig. 3.29(b). If the slew rate is high enough, the output would be  $v_o = V_m \sin 2\pi ft$ . The rate change of output,  $\frac{dv_o}{dt} = 2\pi f V_m \cos 2\pi ft$ .

Here, the peak amplitude is  $2\pi f V_m$ . To realize an undistorted output, the slew rate must be equal to or greater than  $\left(\frac{dv_o}{dt}\right)_{\max}$ , i.e.,  $2\pi f V_m \leq \text{slew rate}$ , or  $f V_m \leq \frac{\text{slew rate}}{2\pi}$ . This shows that there is a tradeoff

existing between frequency  $f$  and amplitude  $V_m$ . In other words, the  $V_m$  must be sufficiently small, to operate at higher frequencies. To operate the IC 741 at its full small-signal bandwidth of 1 MHz as a voltage follower, the maximum amplitude of  $V_m$  can be  $(0.5 \text{ V/ms})/(2\pi \times 1 \text{ MHz}) \cong 80 \text{ mV}$ . Hence, the specification *Full Power Bandwidth (FPB)* of an op-amp is defined as the maximum frequency at which the op-amp can produce an undistorted output, with the maximum possible amplitude. Thus,

$FPB = \frac{\text{slew rate}}{2\pi V_{sat}}$ , where  $\pm V_{sat}$  is the saturation voltage of op-amp chosen.

### Example 3.12

Assume that an op-amp 741 connected as a unit gain inverting amplifier is applied with an input change of 10 V. Determine the time taken for the output to change by 10 V.

**Solution** Given, output voltage change = 10 V

For the op-amp 741, slew rate = 0.5 V/ $\mu$ s

We know that, Slew rate =  $\frac{\text{Output voltage change}}{\text{Time}}$

$$\begin{aligned} \text{Therefore, Time} &= \frac{\text{Output voltage change}}{\text{Slew rate}} = \frac{10 \text{ V}}{0.5 \text{ V}/\mu\text{s}} \\ &= 20 \mu\text{s} \end{aligned}$$

### Example 3.13

Assuming slew rate for 741 is 0.5 V/ $\mu$ s, what is the maximum undistorted sine-wave that can be obtained for (a) 12V peak and (b) 2V peak?

**Solution** Given the slew rate for 741 is 0.5 V/ $\mu$ s.

(a) For the sine-wave of 12 V peak,

$$f_{\max} = \frac{\text{Slew rate}}{2\pi V_m} = \frac{0.5 \text{ V}/\mu\text{s}}{2\pi \times 12 \text{ V}} = \frac{0.5}{2\pi \times 12 \times 10^{-6}} = 6.63 \text{ kHz}$$

(b) For the sine-wave of 2V peak,

$$f_{\max} = \frac{0.5 \text{ V}/\mu\text{s}}{2\pi \times 2 \text{ V}} = \frac{0.5}{2\pi \times 2 \times 10^{-6}} = 39.8 \text{ kHz}$$

### Example 3.14

IC 741 is used as an inverting amplifier with a gain of 100. The voltage gain Vs frequency characteristic is flat up to 10 kHz. Determine the maximum peak-to-peak input signal that can be applied without any distortion to the output.

**Solution** Slew rate of op-amp 741 = 0.5 V/μs

Using Eq. (3.38),

$$\begin{aligned}V_{m(\max)} &= \frac{\text{Slew rate}}{2\pi f} \\&= \frac{0.5 \text{ V}/\mu\text{s}}{2\pi \times 10 \text{ kHz}} = \frac{0.5}{2\pi \times 10 \times 10^3 \times 10^{-6}} = 7.96 \text{ V}\end{aligned}$$

### Example 3.15

Assuming the slew rate of op-amp is 0.5 V/μs, justify whether it is possible to amplify a square-wave of peak-to-peak value 500 mV, with a rise time of 4 μs or less, to a peak-to-peak amplitude of 5 V.

**Solution** The output voltage is greater than 1V.

Therefore, the required slew rate =  $\frac{dV}{dt}$ .

The rise time is defined as the time needed for 10% to 90% of output transition.

Therefore, the voltage swing value of 10% to 90% is

$$(0.9 - 0.1) 5 \text{ V} = 4 \text{ V}.$$

$$\text{Then, the slew rate required} = \frac{4 \text{ V}}{4 \mu\text{s}} = \frac{4}{4 \times 10^{-6}} = 1 \text{ V}/\mu\text{s}.$$

Since the slew rate of op-amp 741 as given in the datasheet is 0.5 V/μs which is too slow when compared to the required slew rate of 1 V/μs, it is not possible to use op-amp 741 to amplify the given square wave.

### Example 3.16

The output voltage of a certain op-amp circuit changes by 20 V in 4 μs. What is its slew rate?

$$\text{Solution} \quad \text{The slew rate} = \frac{dV_o}{dt} = \frac{20 \text{ V}}{4 \mu\text{s}} = 5 \text{ V}/\mu\text{s}$$

### Example 3.17

The 741C is used as an inverting amplifier with a gain of 50. The sinusoidal input signal has a variable frequency and maximum amplitude of 20 mV peak. What is the maximum frequency of the input at which the output will be undistorted? Assume that the amplifier is initially nulled.

**Solution** The 741C has a typical slew rate of 0.5 V/μs. Using Eq. (3.36), the slew rate is

$$SR = \frac{2\pi f V_m}{10^6} = \frac{0.5 \text{ V}}{\mu\text{s}}$$

$$\text{The maximum output voltage } V_m = A V_{id}$$

$$= 50 \times 20 \times 10^{-3} = 1 \text{ V (peak)}$$

The maximum frequency of the input for which undistorted output is obtained is given by

$$\begin{aligned}f_{\max} &= \frac{SR}{2\pi V_m} \times 10^6 \\&= \frac{0.5}{2\pi \times 1} \times 10^6 = 79.6 \text{ kHz}\end{aligned}$$

### **Example 3.18**

An inverting amplifier using the 741C must have a flat response up to 40 kHz. The gain of the amplifier is 10. What maximum peak-to-peak input signal can be applied without distorting the output?

**Solution** The 741C has a typical slew rate of 0.5 V/ $\mu$ s. Using Eq. (3.36), the slew rate is

$$SR = \frac{2\pi f V_m}{10^6} = 0.5 \text{ V}/\mu\text{s}$$

$$\begin{aligned}\text{The maximum output voltage } V_m &= \frac{SR \times 10^6}{2\pi f} \\&= \frac{0.5 \times 10^6}{2\pi \times 40 \times 10^3} = 1.99 \text{ V peak} \\&= 3.98 \text{ V (peak-to-peak)}\end{aligned}$$

The maximum peak-to-peak input voltage for undistorted output is

$$V_{id} = \frac{V_m}{A} = \frac{3.98}{10} = 0.398 \text{ V (peak-to-peak)}$$

## **3.9 NOISE**

Noise is a major source of interference and it is the undesired electrical signal present on the desired signal output in the electronic systems consisting of discrete and integrated circuits. Any unwanted signal can be called noise and it is random in nature and therefore difficult to be analysed.

Drift and offset can be considered as noise of very low frequency. The noise source can be categorised into

- (i) Internal or self-induced
- (ii) External or man-made

The internal noise may be caused by random voltage of ac signals, switching of other circuit nodes and the resulting currents generated within conductors, and active and passive devices. The amount of noise induced in a given circuit is determined by the rate of change of current and voltage, frequency of operation, and the type of coupling existing between two circuits.

The external noise sources are electrical devices and their controls. For example, rotating machinery, spark plugs in automobile, voltage regulators, air conditioner and lightings generate noise. Natural phenomena such as lightning may also be an external noise source.

**Noise in op-amp circuits** The common types of noise factors associated with op-amps are

- (i) Thermal noise
- (ii) Shot noise
- (iii)  $1/f$  noise or flicker noise and
- (iv) Burst noise or popcorn noise

The *thermal noise* increases with rise in temperature, and it is the result of random motion of charge carriers in a resistance. The *shot noise* is induced due to the discrete nature of current flow in devices. The *flicker noise* or  $1/f$  noise increases with decrease in frequency. The popcorn noise results from a sudden change in input bias current, usually at frequencies less than 100 Hz, which is caused due to imperfect semiconductor surface conditions.

These various sources combine to form a net cumulative noise that can be broadly categorised as (i) white noise and (ii) flicker noise based on their frequency distribution. White noise has its frequency spectrum constant over a very wide bandwidth. Flicker noise follows a  $(1/f)$  frequency variation and it is usually negligible above 1 kHz or so.

The actual noise is a random process with erratic behaviour as illustrated in Fig. 3.30. The internal noise model of an op-amp, using a noise voltage source  $v_{ni}$ , at the non-inverting input is shown in Fig. 3.31.

The *rms* noise voltage at the output of the op-amp is given by

$$v_{no} = k_n v_{ni}$$

where  $k_n$  is the noise gain value of op-amp. The noise voltage is amplified in the same manner of, how the offset voltage is amplified. Thus, the *noise voltage gain* of non-inverting amplifier is given by

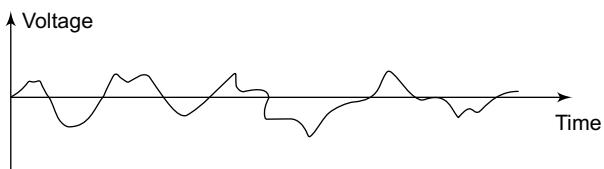
$$\text{Noise gain} = k_n = 1 + \frac{R_f}{R_1}$$

The noise voltage will be in  $\mu\text{V}$  or  $\text{nV}$  (*rms*) for different values of source resistances over a particular frequency range. The op-amp 741 has a  $2\mu\text{V}$  of *total noise* over a frequency band of 10 Hz to 10 kHz, and for source resistor  $R_1$  of value between  $100\ \Omega$  and  $20\ \Omega$ . For larger values of  $R_1$ , the noise voltage increases. Therefore,  $R_1$  is normally limited to  $20\text{ k}\Omega$  to minimise noise in the output.

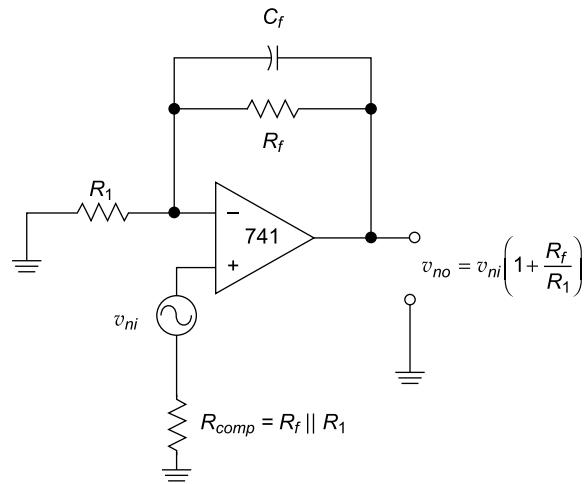
The steps to be taken to minimise the errors in output voltage due to noise are

- Avoid large values of  $R_f$  and  $R_1$  and select  $R_1 < 20\text{ k}\Omega$
- Place a small capacitor of value  $3\text{ pF}$  across  $R_f$  to shunt it for high noise frequencies
- Not necessary to connect any capacitor across  $R_1$ , since at high frequencies, the  $R_1C$  combination will generate a smaller impedance and the gain will tend to increase with frequency which will further aggravate the noise effect

To reduce the effect of electrical noise on ICs, several schemes have been commonly used. Physical shielding of the ICs and associated wiring help to prevent external electromagnetic radiation from introducing noise into the internal circuitry. Special buffering and filtering circuits can be used between the electronic circuits and signal leads. To provide a path for any extraneous radio frequency (*RF*) signals, all linear IC power supply terminals should generally be bypassed to ground. The breadboard layout should be such that the bypass capacitors are as close to the IC terminals as possible. Internal noise



**Fig. 3.30** Random noise wave form



**Fig. 3.31** Op-amp noise model

generation can be reduced by keeping input and output lead lengths as short as practically feasible. One common junction point should be used near the IC for all ground connections. In a high electrical noise environment, use of an IC with a high degree of noise immunity will minimise the amount of special care needed for proper circuit operation.

### Example 3.19

Consider the non-inverting amplifier shown in Fig. 3.31 with  $R_f = 10 \text{ k}\Omega$  and  $R_i = 100 \Omega$ . Also assume that the broadband noise characteristics of the op-amp indicates input rms noise  $v_{ni} = 1 \mu\text{V}$ . Estimate the noise gain of the circuit and output noise level in the bandwidth of 10 Hz to 1 kHz.

**Solution** Given input noise voltage,  $v_{ni} = 1 \mu\text{V}$  (rms)

$$\text{Noise gain } k_n \text{ of the circuit} = 1 + \frac{R_f}{R_i} = 1 + \frac{10 \times 10^3}{100} = 101$$

$$\text{The output noise voltage, } v_{no} = v_{ni} \left( 1 + \frac{R_f}{R_i} \right) = 1 \times 10^{-6} \times 101 = 101 \mu\text{V (rms)}$$

## 3.10 OPEN-LOOP OP-AMP CONFIGURATIONS

The term *open-loop* indicates that no feedback in any form is fed to the input from the output. When connected in open-loop, the op-amp functions as a very high gain amplifier. There are three open-loop configurations of op-amp, namely,

- (i) Differential amplifier
- (ii) Inverting amplifier and
- (iii) Non-inverting amplifier

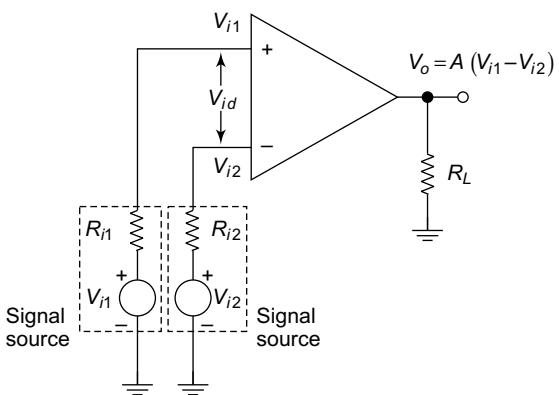
The above classification is made based on the number of inputs used and the terminal to which the input is applied. The op-amp amplifies both ac and dc input signals. Thus, the input signals can be either ac or dc voltages.

### 3.10.1 Open-loop Differential Amplifier

In this configuration, the inputs are applied to both the inverting and the non-inverting input terminals of the op-amp and it amplifies the difference between the two input voltages. Figure 3.32 shows the open-loop differential amplifier configuration.

The input voltages are represented by  $V_{i1}$  and  $V_{i2}$ . The source resistances  $R_{i1}$  and  $R_{i2}$  are negligibly small in comparison with the very high input resistance offered by the op-amp, and thus the voltage drop across these source resistances is assumed to be zero. The output voltage  $V_o$  is given by

$$V_o = A(V_{i1} - V_{i2}) \quad (3.39)$$



**Fig. 3.32** Open-loop differential amplifier

where  $A$  is the large-signal voltage gain. Thus, the output voltage is equal to the voltage gain  $A$  times the difference between the two input voltages. This is the reason why this configuration is called a *differential amplifier*. In open-loop configurations, the large-signal voltage gain  $A$  is also called *open-loop gain A*.

### 3.10.2 Inverting Amplifier

In this configuration, the input signal is applied to the inverting input terminal of the op-amp and the non-inverting input terminal is connected to the ground. Figure 3.33 shows the circuit of an open-loop inverting amplifier.

The output voltage is  $180^\circ$  out-of-phase with respect to the input and hence, the output voltage  $V_o$  is given by

$$V_o = -AV_i$$

Thus, in an inverting amplifier, the input signal is amplified by the open-loop gain  $A$  and is phase-shifted by  $180^\circ$ .

### 3.10.3 Non-inverting Amplifier

Figure 3.34 shows the open-loop non-inverting amplifier. The input signal is applied to the non-inverting input terminal of the op-amp and the inverting input terminal is connected to the ground.

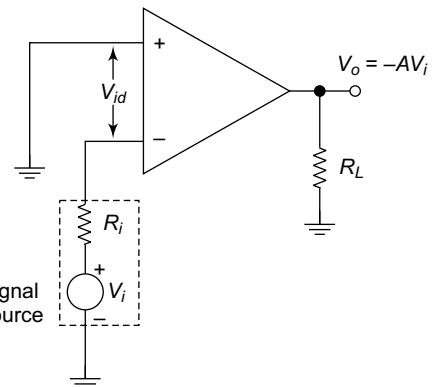
The input signal is amplified by the open-loop gain  $A$  and the output is in-phase with the input signal.

$$V_o = AV_i$$

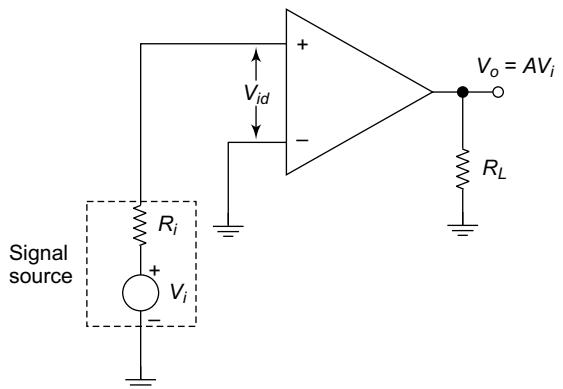
In all the above open-loop configurations, only very small values of input voltages can be applied. Even for voltage levels slightly greater than zero, the output is driven into saturation, which is observed from the ideal transfer characteristics of op-amp shown in Fig. 3.3(b). Thus, when operated in the open-loop configuration, the output of the op-amp is either in negative or positive saturation, or switches between positive and negative saturation levels. This prevents the use of open-loop configurations of op-amps in linear applications.

### 3.10.4 Limitations of Open-loop Op-amp Configurations

Firstly, in the open-loop configurations, clipping of the output waveform can occur when the output voltage exceeds the saturation level of op-amp. This is due to the very high open-loop gain of the op-amp. This feature actually makes it possible to amplify very low frequency signal of the order of microvolts or even less, and the amplification can be achieved accurately without any distortion. However, signals of such magnitudes are susceptible to noise and the amplification for those applications is almost impossible to obtain in the laboratory.



**Fig. 3.33** Open-loop inverting amplifier



**Fig. 3.34** Open-loop non-inverting amplifier

Secondly, the open-loop gain of the op-amp is not a constant and it varies with changing temperature and variations in power supply. Also, the bandwidth of most of the open-loop op-amps is negligibly small. This makes the open-loop configuration of op-amp unsuitable for ac applications. The open-loop bandwidth of the widely used IC 741 is approximately 5 Hz. But in almost all ac applications, the bandwidth requirement is much larger than this.

For the reasons stated, the open-loop op-amp is generally not used in linear applications. However, the open-loop op-amp configurations find use in certain non-linear applications such as comparators, square-wave generators and astable multivibrators.

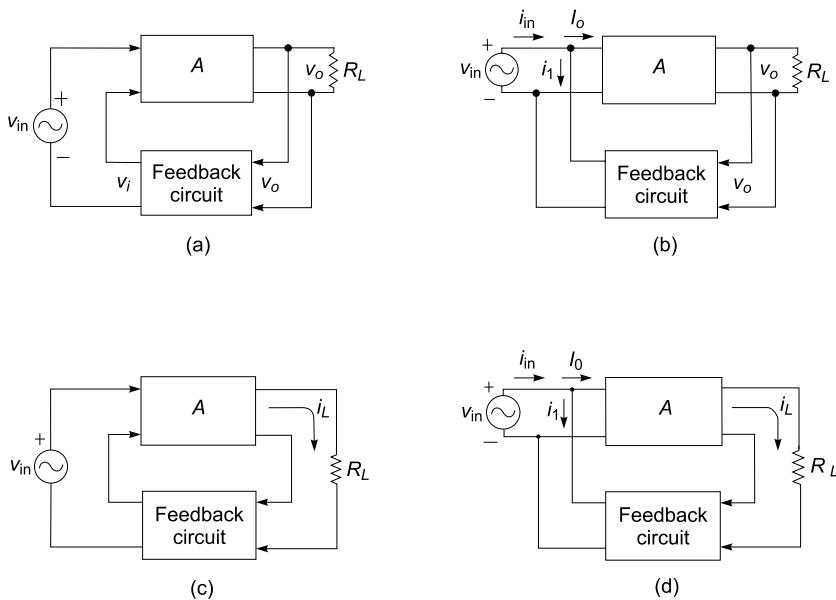
### 3.11 CLOSED-LOOP OP-AMP CONFIGURATIONS

The op-amp can be effectively utilised in linear applications by providing a feedback from the output to the input, either directly or through another network. If the signal feedback is out-of-phase by  $180^\circ$  with respect to the input, then the feedback is referred to as *negative feedback* or *degenerative feedback*. Conversely, if the feedback signal is in-phase with that at the input, then the feedback is referred to as *positive feedback* or *regenerative feedback*.

The op-amps when used as a closed-loop amplifier may employ either active devices, passive components, or the combination of both. The intended application of the circuits decides the selection of components. In any case, the closed-loop amplifier can be represented by the use of two functional blocks, one depicting the op-amp and the other showing the feedback circuit block.

The main configurations of these circuits are decided by two factors, namely, (i) whether voltage or current is feedback to the input from the output, and (ii) whether the feedback signal is connected in series or parallel.

The four different basic types of configurations using an amplifier  $A$  and feedback circuit are shown in Fig. 3.35.

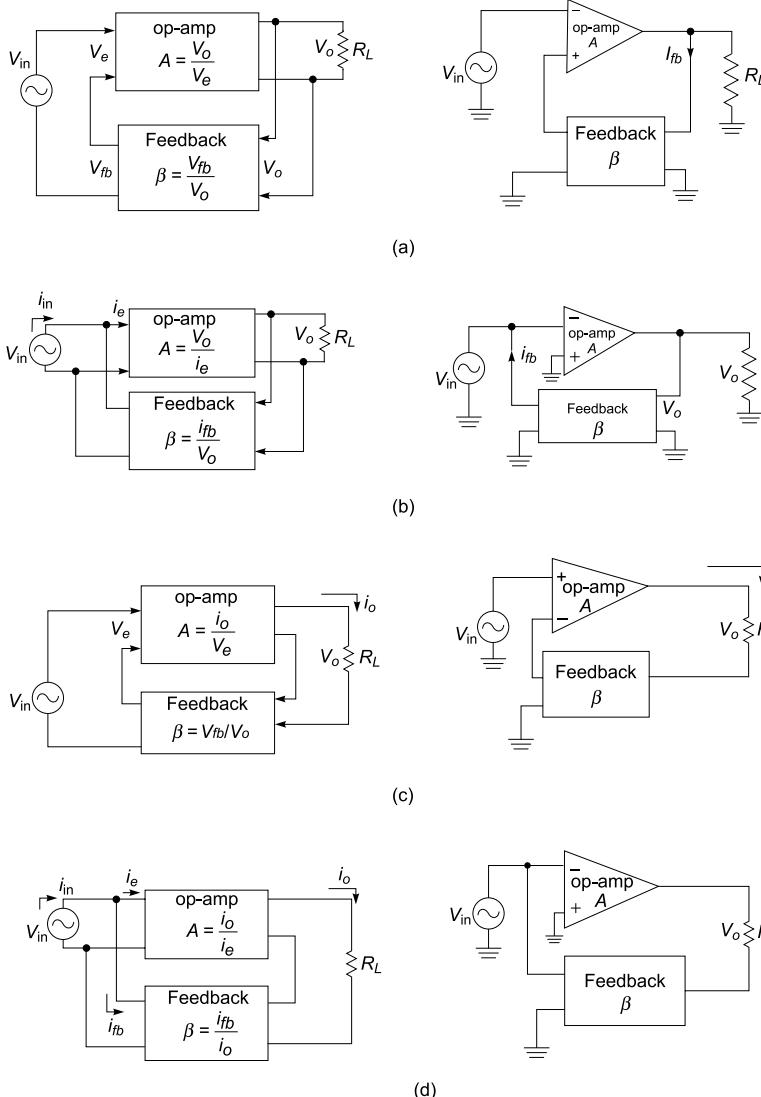


**Fig. 3.35** Four types of feedback configurations: (a) Voltage-series, (b) Voltage shunt  
(c) Current series (d) Current shunt

Figures 3.35(a) and (b) illustrate the voltage output across load resistor feedback to the input in voltage series and voltage-shunt feedback respectively. Figures 3.35(c) and (d) show that the output current  $i_L$  flowing through the load resistor is applied as input through the feedback circuit in series and parallel respectively.

The most commonly employed configurations are the voltage-series and voltage-shunt feedback types. The following sections discuss *the voltage-shunt or the inverting amplifier* and *the voltage-series or the non-inverting amplifier* circuits using op-amps.

An op-amp that uses feedback is called a closed-loop amplifier. The most commonly used closed-loop amplifier configurations are (i) Inverting amplifier (voltage-shunt feedback) and (ii) Non-inverting amplifier (voltage-series feedback).



**Fig. 3.36** Four types of feedback configurations for op-amps: (a) Voltage-series (b) Voltage-shunt (c) Current-series (d) Current-shunt

### 3.11.1 Inverting Amplifier

The inverting amplifier is shown in Fig. 3.37(a), and its alternate circuit arrangement is shown in Fig. 3.37(b), with the circuit redrawn in a different way to illustrate how the voltage shunt feedback is achieved. The input signal drives the inverting input of the op-amp through resistor  $R_1$ .

The op-amp has an open-loop gain of  $A$ , so that the output signal is much larger than the error voltage. Because of the phase inversion, the output signal is  $180^\circ$  out-of-phase with the input signal. This means that the feedback signal opposes the input signal and the feedback is *negative* or *degenerative*.

**Virtual ground** A *virtual ground* is a ground which acts *like* a ground. It may not have physical connection to ground. This property of an ideal op-amp indicates that the inverting and non-inverting terminals of the op-amp are at the same potential. The non-inverting input is grounded for the inverting amplifier circuit. This means that the inverting input of the op-amp is also at ground potential. Therefore, a virtual ground is a point that is at the fixed ground potential (0 V), though it is not practically connected to the actual ground or common terminal of the circuit.

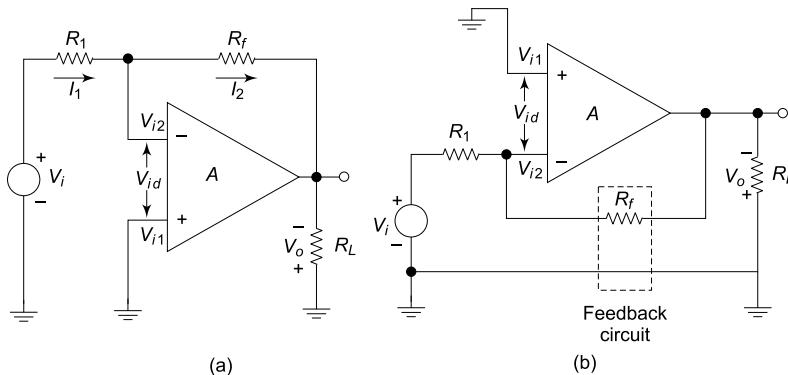
The open-loop gain of an op-amp is extremely high, typically 200,000 for a 741. For example, when the output voltage is 10 V, the input differential voltage  $V_{id}$  is given by

$$V_{id} = \frac{V_o}{A} = \frac{10}{200,000} = 0.05 \text{ mV}$$

Furthermore, the open-loop input impedance of a 741 is around  $2 \text{ M}\Omega$ . Therefore, for an input differential voltage of 0.05 mV, the input current is only

$$I_i = \frac{V_{id}}{R_i} = \frac{0.05 \text{ mV}}{2 \text{ M}\Omega} = 0.25 \text{ nA}$$

Since the input current is so small compared to all other signal currents, it can be approximated as zero. For any input voltage applied at the inverting input, the input differential voltage  $V_{id}$  is negligibly small and the input current is ideally zero. Hence, the inverting input of Fig. 3.37(a) acts as a virtual ground. The term *virtual ground* signifies a point whose voltage with respect to ground is zero, and yet no current can flow into it.



**Fig. 3.37** Closed-loop inverting amplifier

The expression for the closed-loop voltage gain of an inverting amplifier can be obtained from Fig. 3.37(a). Since the inverting input is at virtual ground, the input impedance is the resistance between the inverting input terminal and the ground. That is,  $Z_i = R_1$ . Therefore, all of the input voltage appears across  $R_1$  and it sets up a current through  $R_1$  that equals

$$I_1 = \frac{V_i}{R_1} \quad (3.40)$$

This current must flow through  $R_f$ , because the virtual ground accepts negligible current. The left end of  $R_f$  is ideally grounded, and hence the output voltage appears wholly across it. Therefore,

$$V_o = -I_2 R_f = -\frac{R_f}{R_1} V_i \quad (3.41)$$

The closed-loop voltage gain  $A_v$  is given by

$$A_v = \frac{V_o}{V_i} = \frac{-R_f}{R_1} \quad (3.42)$$

The input impedance can be set by selecting the input resistor  $R_1$ . Moreover, the above equation shows that the gain of the inverting amplifier is set by selecting a ratio of feedback resistor  $R_f$  to the input resistor  $R_1$ . The ratio  $R_f/R_1$  can be set to any value less than or greater than unity. This feature of the gain equation makes the inverting amplifier with feedback very popular and it lends this configuration to a majority of applications.

### Example 3.20

For the inverting amplifier of Fig. 3.35(a),  $R_f = 10 \text{ k}\Omega$  and  $R_1 = 1 \text{ k}\Omega$ . Determine the closed-loop voltage gain  $A_v$ .

**Solution** The closed-loop voltage gain is

$$\begin{aligned} A_v &= -\frac{R_f}{R_1} \\ &= -\frac{10}{1} = -10 \end{aligned}$$

The gain is 10 and the negative sign indicates the inverting mode or  $180^\circ$  phase-shift obtained at the output with respect to the input.

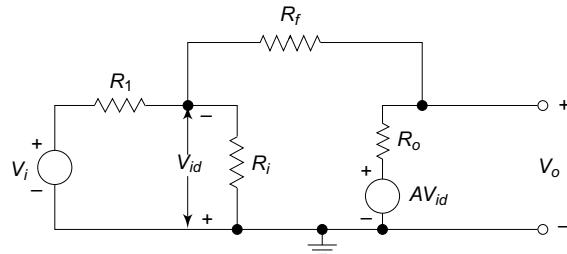
#### Practical considerations

- (i) Setting the input impedance  $R_1$  to be too high will pose problems for the bias current, and it is usually restricted to  $10 \text{ k}\Omega$ .
- (ii) The gain cannot be set very high due to the upper limit set by the gain-bandwidth ( $GBW = A_v \times f$ ) product. The  $A_v$  is normally below 100.
- (iii) The peak output of the op-amp is limited by the power supply voltages, and it is about 2 V less than supply, beyond which, the op-amp enters into saturation.
- (iv) The output current may not be short-circuit limited, and heavy loads may damage the op-amp. When short-circuit protection is provided, a heavy load may drastically distort the output voltage.

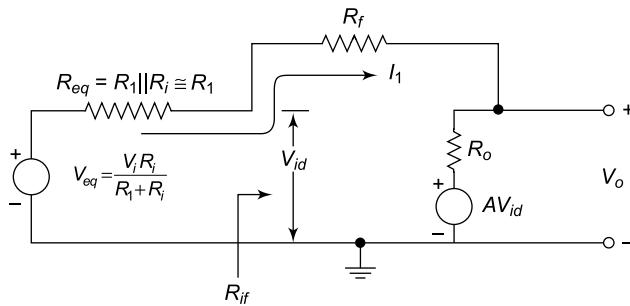
### 3.11.2 Practical Inverting Amplifier

The practical inverting amplifier has finite value of input resistance and input current, its open voltage gain  $A_0$  is less than infinity and its output resistance  $R_o$  is not zero, as against the ideal inverting amplifier with infinite input resistance, infinite open-loop voltage gain and zero output resistance respectively.

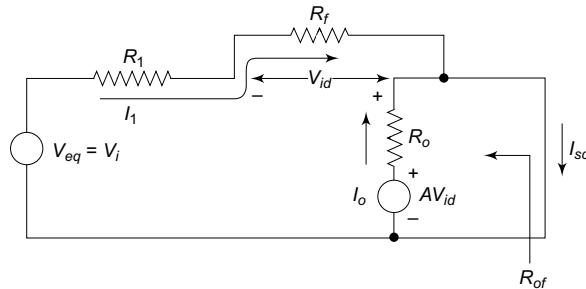
Figure 3.38(a) shows the low frequency equivalent circuit model of a practical inverting amplifier. This circuit can be simplified using the Thevenin's equivalent circuit shown in Fig. 3.38(b). The signal source  $V_i$  and the resistors  $R_1$  and  $R_i$  are replaced by their Thevenin's equivalent values. The closed-loop gain  $A_v$  and the input impedance  $R_{if}$  are calculated as follows.



**Fig. 3.38 (a)** Equivalent circuit of a practical inverting amplifier



**Fig. 3.38 (b)** Thevenin's equivalent circuit



**Fig. 3.38 (c)** Equivalent circuit to determine  $R_o$

The input impedance of the op-amp is normally much larger than the input resistance  $R_1$ . Therefore, we can assume  $V_{eq} \approx V_i$  and  $R_{eq} \approx R_1$ . From Fig. 3.38(b), we get

$$V_o = I_1 R_o + A V_{id} \quad (3.43)$$

and

$$V_{id} + I_1 R_f + V_o = 0 \quad (3.44)$$

Substituting the value of  $V_{id}$  from Eq. (3.44) in Eq. (3.43), we get

$$V_o (1 + A) = I_1 (R_o - A R_f) \quad (3.45)$$

Also using the Kirchhoff's voltage law, we get

$$V_i = I_1(R_1 + R_f) + V_o \quad (3.46)$$

Substituting the value of  $I$  derived from Eq. (3.45) in Eq. (3.46) and obtaining the closed-loop gain  $A_v$ , we get

$$A_v = \frac{V_o}{V_i} = \frac{R_o - AR_f}{R_o + R_f + R_l(1+A)} \quad (3.47)$$

It can be observed from Eq. (3.47) that when  $A \gg 1$ ,  $R_o$  is negligibly small and the product  $AR_1 \gg R_o + R_f$ , the closed-loop gain is given by

$$A_v \approx -\frac{R_f}{R_l}$$

which is of the same form as given in Eq. (3.42) for an ideal inverter.

**Input resistance  $R_{if}$**  From Fig. 3.36(b), we get

$$R_{if} = \frac{V_{id}}{I_1}$$

Using Kirchhoff's voltage law, we get,

$$V_{id} + I_1(R_f + R_o) + AV_{id} = 0$$

which can be simplified for  $R_{if}$  as

$$R_{if} = \frac{V_{id}}{I_1} = \frac{R_f + R_o}{1 + A} \quad (3.48)$$

**Output resistance  $R_{of}$**  Figure 3.38(c) shows the equivalent circuit to determine  $R_{of}$ . The output impedance  $R_{of}$  without the load resistance factor  $R_L$  is calculated from the open circuit output voltage  $V_{oc}$  and the short circuit output current  $I_{sc}$ . From Fig. 3.38(c), when the output is short circuited, we get

$$I_1 = \frac{V_i - 0}{R_l + R_f} \quad (3.49)$$

and

$$I_o = \frac{AV_{id}}{R_o} \quad (3.50)$$

We know that

$$V_{id} = -I_1 R_f$$

Therefore,

$$I_o = \frac{AI_1 R_f}{R_o} \quad (3.51)$$

The short-circuit current is

$$I_{sc} = I_1 + I_o = V_i \frac{(R_o - AR_f)}{R_o(R_l + R_f)} \quad (3.52)$$

The output resistance  $R_{of} = \frac{V_{oc}}{I_{sc}}$  and the closed-loop gain  $A_v = \frac{V_{oc}}{V_i}$ .

Therefore,

$$R_{of} = \frac{A_v V_i}{V_i \left[ \frac{(R_o - AR_f)}{R_o(R_l + R_f)} \right]} \quad (3.53)$$

Substituting the value of  $A_v$  from Eq. (3.47), we get

$$\begin{aligned} R_{of} &= \frac{R_o(R_l + R_f)}{R_o + R_f + R_l(1 + A)} \\ &= \frac{\frac{R_o(R_l + R_f)}{R_o + R_l + R_f}}{1 + \frac{R_l A}{R_o + R_l + R_f}} \end{aligned} \quad (3.54)$$

In the above equation, the numerator contains the term  $R_o || (R_l + R_f)$  and it is smaller than  $R_o$ . The output resistance  $R_{of}$  is therefore always smaller than  $R_o$  and from Eq. (3.54) for  $A_v \rightarrow \infty$ , the output resistance  $R_{of} \rightarrow 0$ .

### 3.11.3 Non-inverting Amplifier

The non-inverting amplifier with input signal applied to the non-inverting input and the output voltage feedback to the inverting input, i.e. in voltage-series mode is shown in Fig. 3.39(a). Figure 3.39(b) represents the simplified circuit arrangement as usually followed. The op-amp provides an internal gain  $A$ . The external resistors  $R_1$  and  $R_f$  form the feedback voltage divider circuit with an attenuation factor of  $\beta$ . Since the feedback voltage is at the inverting input, it opposes the input voltage at the non-inverting input terminal, and hence, the feedback is negative or degenerative.

The differential voltage  $V_{id}$  at the input of the op-amp is zero, because node  $a$  is at the same voltage as that of the non-inverting input terminal. As shown in Fig. 3.39(a),  $R_f$  and  $R_1$  form a potential divider. Therefore,

$$V_i = \frac{R_1}{R_1 + R_f} \times V_o \quad (3.55)$$

since no current flows into the op-amp.

$$\text{Equation (3.55) can be written as } \frac{V_o}{V_i} = \frac{R_1 + R_f}{R_1} = 1 + \frac{R_f}{R_1}.$$

Hence, the voltage gain for the non-inverting amplifier is given by

$$A_v = \frac{V_o}{V_i} = 1 + \frac{R_f}{R_1}$$

Using the alternate circuit arrangement shown in Fig. 3.39(b), the feedback factor of the feedback voltage divider network is

$$\beta = \frac{R_1}{R_1 + R_f} \quad (3.56)$$

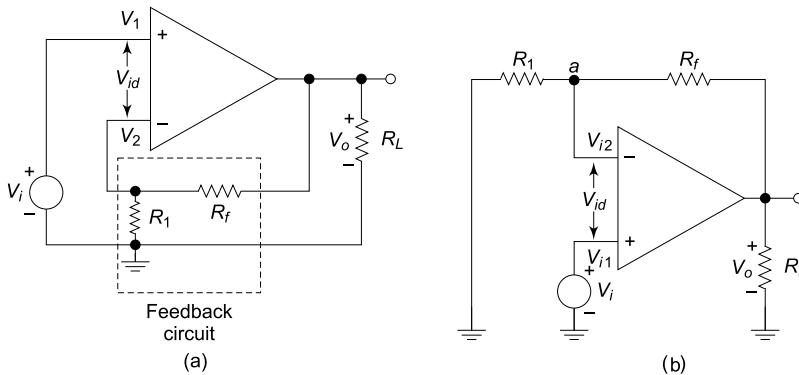
Therefore, the closed-loop gain is

$$A_v = \frac{1}{\beta} = \frac{R_1 + R_f}{R_1} \quad (3.57)$$

$$= 1 + \frac{R_f}{R_1} \quad (3.58)$$

From the above equation, it can be observed that the closed-loop gain is always greater than one and it depends on the ratio of the feedback resistors. If precision resistors are used in the feedback network, a precise value of closed-loop gain can be achieved. The closed-loop gain does not drift with temperature changes or op-amp replacements.

The input resistance of the op-amp is extremely large (approximately infinity), since the op-amp draws negligible current from the input signal.



**Fig. 3.39** (a) Its alternate circuit arrangement (b) Closed-loop non-inverting amplifier

### Example 3.21

The variable resistance varies from zero to  $100\text{ k}\Omega$ . Find out the maximum and the minimum closed-loop voltage gain.

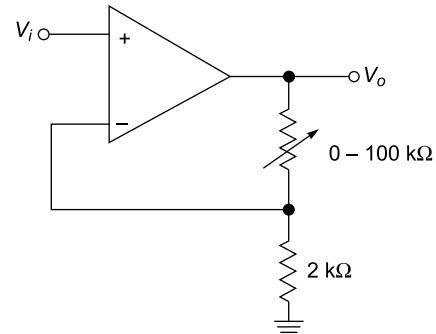
**Solution** Given circuit is a non-inverting amplifier.

$$\text{Therefore, } A_{Vf} = 1 + \frac{R_f}{R_1}$$

$$\text{Here } R_f = 0 - 100\text{ k}\Omega \quad \text{and} \quad R_1 = 2\text{ k}\Omega$$

$$\text{When } R_f = 0, A_{Vf} = 1 + \frac{0}{2 \times 10^3} = 1$$

$$\text{When } R_f = 100\text{ k}\Omega, A_{Vf} = 1 + \frac{100}{2 \times 10^3} = 51$$



**Fig. 3.40**

### Example 3.22

Design a non-inverting amplifier circuit which is capable of providing a voltage gain of 15. Assume ideal op-amp and resistances used should not exceed  $30\text{ k}\Omega$ .

**Solution**  $A_{CL} = 15$

$$A_{CL} = 1 + \frac{R_f}{R_1}$$

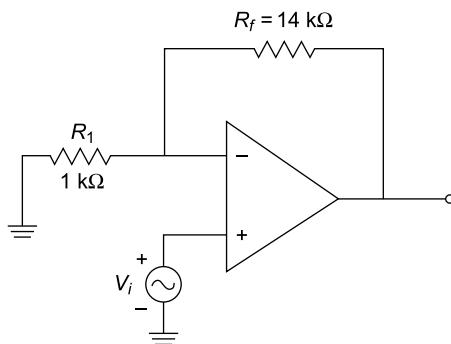
$$\begin{aligned} \text{i.e.} \quad 15 &= 1 + \frac{R_f}{R_1} \\ \frac{R_f}{R_1} &= 14 \end{aligned}$$

i.e.

$$R_f = 14R_1$$

Select  $R_1 = 1 \text{ k}\Omega$ , i.e.  $R_f = 14 \text{ k}\Omega$

The designed circuit is shown in Fig. E3.41



**Fig. 3.41**

### Example 3.23

For the non-inverting amplifier of Fig. 3.39,  $R_1 = 1 \text{ k}\Omega$  and  $R_f = 10 \text{ k}\Omega$ . Determine the closed-loop voltage gain of the amplifier and the feedback factor  $\beta$ .

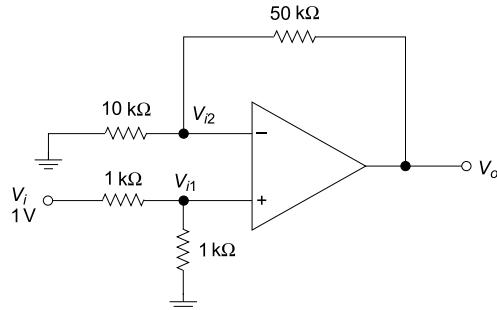
**Solution** The closed-loop voltage gain  $A_v = 1 + \frac{R_f}{R_1}$

$$= 1 + \frac{10 \times 10^3}{1 \times 10^3} = 11$$

$$\begin{aligned} \text{The feedback factor } \beta &= \frac{R_f}{R_1 + R_f} \\ &= \frac{1 \times 10^3}{1 \times 10^3 + 10 \times 10^3} = 0.091 \end{aligned}$$

### Example 3.24

Determine the output voltage  $V_o$  for the non-inverting amplifier circuit shown in Fig. 3.42(a).



**Fig. 3.42(a)**

**Solution** This non-inverting amplifier will amplify  $V_{i1}$  by  $1 + \frac{R_f}{R_l}$  and not  $V_i$ . Since the op-amp input current is zero, a part of the circuit is as shown in Fig. 3.42(b).

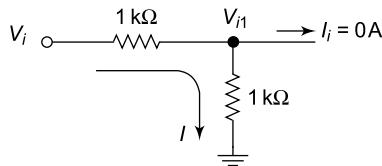


Fig. 3.42(b)

Therefore,

$$I = \frac{1}{1 \times 10^3 + 1 \times 10^3} = 0.5 \text{ mA}$$

and

$$V_{i1} = I \times (1 \times 10^3) = 0.5 \times 10^{-3} \times 10^3 = 0.5 \text{ V}$$

Therefore,

$$V_o = \left(1 + \frac{R_f}{R_l}\right) V_{i1} = \left(1 + \frac{50 \times 10^3}{10 \times 10^3}\right) 0.5 = 3 \text{ V}$$

### Example 3.25

For a non-inverting amplifier shown in Fig. 3.43, determine (a)  $A_v$  (b)  $V_o$  (c)  $I_L$  and (d)  $I_o$ .

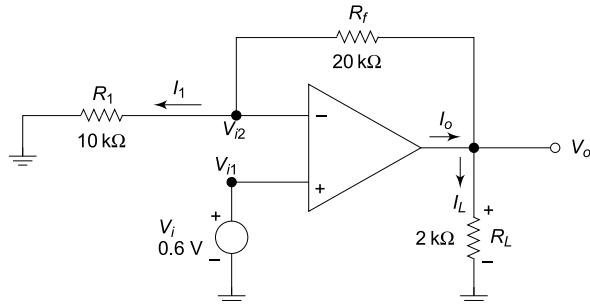


Fig. 3.43

**Solution** The potential of the non-inverting input terminal is  $V_i$ .

Therefore,

$$V_{i2} = V_{i1} = V_i = 0.6 \text{ V}$$

$$I_1 = \frac{V_{i2}}{R_1} = \frac{V_i}{R_1} = \frac{0.6}{10 \times 10^3} = 60 \mu\text{A}$$

Since the input current into op-amp is zero, the current can flow only through  $R_f$ .

$$(a) \quad A_v = 1 + \frac{R_f}{R_1} = 1 + \frac{20}{10} = 3$$

$$(b) \quad V_o = A_v V_i = 3 \times 0.6 = 1.8 \text{ V}$$

$$(c) I_L = \frac{V_o}{R_L} = \frac{1.8}{2 \times 10^3} = 0.9 \text{ mA}$$

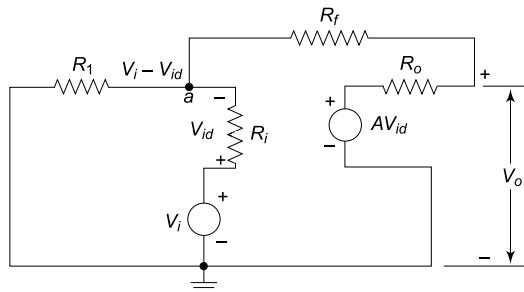
(d) Applying Kirchhoff's current law at the output node,

$$I_o = I_1 + I_L = 60 \times 10^{-6} + 0.9 \times 10^{-3} = 0.96 \text{ mA}$$

The current  $I_o$  flows from op-amp towards output terminal.

### 3.11.4 Practical Non-inverting Amplifier

The equivalent circuit of a non-inverting amplifier using the low frequency model is shown in Fig. 3.44. Using Kirchhoff's current law at node  $a$ ,



**Fig. 3.44** Equivalent circuit of a non-inverting amplifier using low frequency model

$$(V_i - V_{id})Y_1 - V_{id}Y_i + (V_i - V_{id} - V_o)Y_f = 0$$

That is,

$$-(Y_1 + Y_i + Y_f)V_{id} + (Y_1 + Y_f)V_i = Y_f V_o \quad (3.59)$$

Similarly Kirchhoff's current law at the output node gives,

$$(V_i - V_{id} - V_o)Y_f + (AV_{id} - V_o)Y_o = 0$$

That gives

$$-(Y_f - AY_o)V_{id} + Y_f V_i = (Y_f + Y_o)V_o \quad (3.60)$$

Using Eqs. (3.59) and (3.60) for  $V_o/V_i$ , we get

$$A_v = \frac{V_o}{V_i} = \frac{AY_o(Y_1 + Y_f) + Y_f Y_i}{(A+1)Y_o Y_f + (Y_1 + Y_i)(Y_f + Y_o)} \quad (3.61)$$

When the open-loop gain  $A$  approaches infinity, Eq. (3.61) becomes

$$\frac{AY_o(Y_1 + Y_f)}{AY_o Y_f} = \frac{Y_1 + Y_f}{Y_f} = 1 + \frac{Y_1}{Y_f}$$

It can be written as  $A_v = 1 + \frac{R_f}{R_i}$ , and it may be noted that it is of the form as given in Eq. (3.58).

### 3.11.5 AC Amplifiers using Op-Amp

The op-amp can fundamentally amplify both the ac and dc signals. The dc amplifier produces an output in response to changes in dc input signals. When the ac response of the op-amp is required with high and low frequency limits, or when the signal contains a dc offset, it becomes necessary to use an ac amplifier along with a coupling capacitor between any two stages. The coupling capacitor is allowed to

block the dc signals and to interrupt the bias current paths to the op-amp input terminals with the use of additional bias resistors. It sets the low frequency cut-off value  $f_L$  which is given by

$$f_L = \frac{1}{2\pi C_i (R_{iN} + R_o)}$$

where  $C_i$  is the coupling capacitance

$R_{iN}$  is the ac input resistance of the next stage

and  $R_o$  is the ac output resistance of the source stage

Since the capacitor has high impedance at low frequencies, the coupling capacitors must be selected based on the desired lower cut-off frequency ( $f_L$ ). As a thumb rule, the impedance of coupling capacitor at  $f_L$  is normally fixed to be one-tenth of the resistance connected in series. Moreover, the largest capacitor connected in the circuit is normally assumed to determine  $f_L$  and in such a case, the capacitive impedance is made equal to that of the resistance connected in series. In this section, some ac amplifier configurations using op-amp are discussed.

### ac voltage follower (capacitor-coupled circuit)

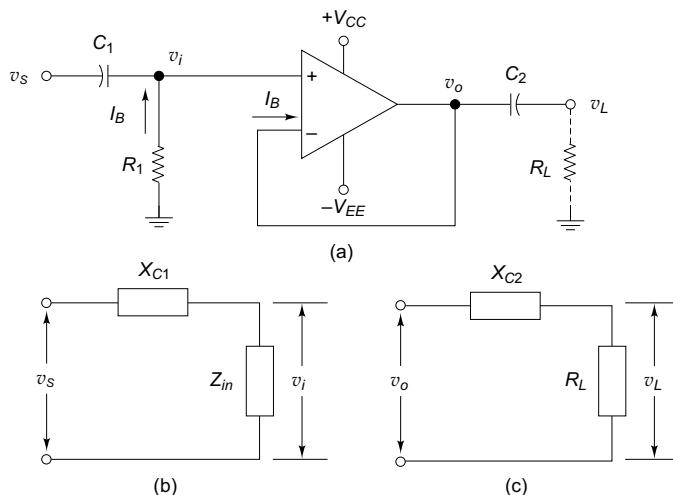
Figure 3.45(a) shows the ac voltage follower using capacitor coupling. The noninverting terminal of the op-amp is grounded through the resistor  $R_1$  to provide a path for input bias current. The capacitor values are selected by the relationships given by

$$X_{C1} = Z_{in}/10 \text{ and } X_{C2} = R_L \text{ at } f_L$$

The design of the capacitor-coupled voltage follower involves the selection of  $R_1$  and  $C_2$ . Larger values of resistors are normally used for achieving minimum circuit power dissipation and minimum current requirement from the power supply. Smaller values of capacitors are preferred for their smaller physical size and less cost. For a BJT op-amp such as IC 741, a maximum value of  $R_1$  for a bipolar op-amp is determined as given by  $0.1 V_{BE}/I_B$  where  $V_{BE}$  is the base-emitter junction cut-in voltage and  $I_B$  is the base current.

For the voltage follower circuit in Fig. 3.45(a), the input impedance  $Z_{in}$  is given by

$$Z_{in} = R_1$$



**Fig. 3.45** (a) Capacitor-coupled voltage follower circuit (b) The signal voltage divided across  $X_{C1}$  and  $Z_{in}$ , (c) The output voltage divided across  $X_{C2}$  and  $R_L$

The values of load resistor  $R_L$  is normally lower than  $R_1$ . The value of capacitor is inversely proportional to the resistance connected in series with it. Hence  $C_2$  is usually larger than  $C_1$ . At lower 3dB frequency  $f_L$ , the impedance of  $C_1$  must be much less than  $Z_{in}$ , so that the division of signal across  $X_{C1}$  and  $Z_{in}$  is avoided. The connection is shown in Fig. 3.45(b). Here  $C_1$  will have no effect on the lower 3dB frequency. Thus,  $C_1$  is calculated as given by

$$X_{C1} = (Z_{in}/10) \text{ at } f_L$$

$$\text{Therefore, } C_1 = \frac{1}{2\pi f_L (R_1/10)}$$

As shown in Fig. 3.45(c), the load voltage  $v_L$  as given by

$$v_L = \frac{v_o \times R_L}{\sqrt{R_L^2 + X_{C2}^2}}$$

where  $v_o$  is the circuit output voltage.

When  $X_{C2} = R_L$ , we have

$$v_L = \frac{v_o \times R_L}{\sqrt{2R_L^2}} = \frac{v_o}{\sqrt{2}} = 0.707 v_o$$

$$0.707 v_o = v_o - 3\text{dB}$$

In other words, the lower 3dB frequency  $f_L$ , of the circuit occurs when  $X_{C2} = R_L$ . Therefore,  $C_2$  is determined by

$$X_{C2} = R_L \text{ at } f_L$$

$$\text{or } C_2 = \frac{1}{2\pi f_L R_L}$$

While selecting standard values of components, it is always the usual practice to choose a larger standard size for achieving the capacitive impedances that are slightly less than those what is theoretically calculated.

For situations where  $R_1$  is smaller than  $R_L$ ,  $C_1$  can be of higher value than  $C_2$ . Then,  $C_1$  is set for determining the lower 3dB frequency by making  $X_{C1} = R_1$  at  $f_L$ . At the output,  $X_{C2} = R_L/10$  at  $f_L$ .

### Example 3.26

Using a 741 op-amp, design a capacitor-coupled voltage follower with a lower cut-off frequency of 50 Hz and a load resistance of  $R_L = 3.3 \text{ k}\Omega$ . Assume  $I_{B(\max)} = 500 \text{ nA}$ .

**Solution** Given  $f_L = 50 \text{ Hz}$ ,  $R_L = 3.3 \text{ k}\Omega$  and  $I_{B(\max)} = 500 \text{ nA}$

$$\text{We know that, } R_{l(\max)} = \frac{0.1V_{BE}}{I_{B(\max)}} = \frac{0.1 \times 0.7}{500 \text{ nA}} \approx 140 \text{ k}\Omega$$

$$X_{C1} = (Z_{in}/10) \text{ at } f_L$$

Here

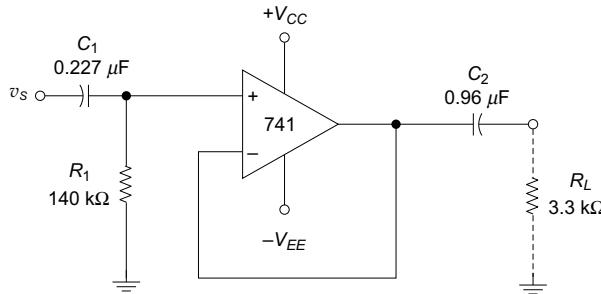
$$Z_{in} = R_l \text{ at } f_L$$

$$\text{Therefore, } C_1 = \frac{1}{2\pi f_L (R_l/100)} = \frac{1}{2\pi \times 50 \times (140 \times 10^3 / 10)} = 0.227 \mu\text{F}$$

We know that  $X_{C2} = R_L$  at  $f_L$

$$\text{Therefore, } C_2 = \frac{1}{2\pi f_L R_L} = \frac{1}{2\pi \times 50 \times 3.3 \times 10^3} = 0.96 \mu\text{F}$$

The supply voltages will be  $\pm 9\text{V}$  to  $\pm 18\text{V}$ . The circuit diagram of the bipolar op-amp is shown in Fig. 3.46.

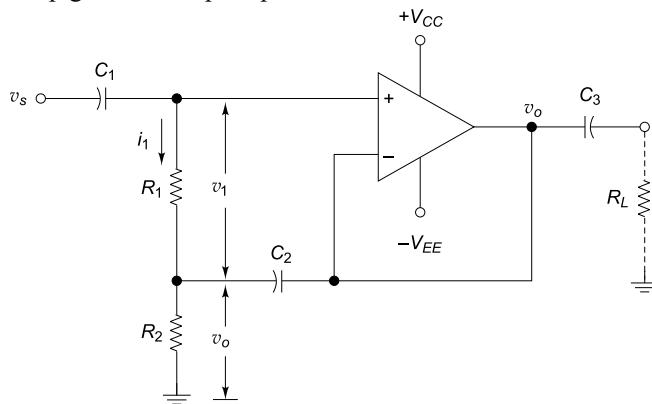


**Fig. 3.46** Capacitor-coupled voltage follower using a bipolar op-amp

**high Input impedance ac voltage follower** The input impedance of the capacitor-coupled voltage follower is decided by the value of resistor  $R_1$  shown in Fig. 3.45(a). The resistor  $R_1$  is required to provide a path for input bias current which results in much smaller input impedance. This input impedance is less than that of the direct-coupled voltage follower. Fig. 3.47 shows an alternative *bootstrapped* circuit configuration by which, the input impedance of the capacitor-coupled voltage follower can be appreciably increased. The capacitor  $C_2$  couples the output of the op-amp to the junction of resistors  $R_1$  and  $R_2$ . The input is applied to the top of  $R_1$  through the capacitor  $C_1$  and the output is applied to the bottom of  $R_1$  through the capacitor  $C_2$ . Here  $C_2$  forms a short circuit for ac, and this makes the output  $v_o$  available across  $R_2$ . Then, the voltage across  $R_1$  is given by

$$v_1 = v_s - v_o = v_s - M v_1$$

where  $M$  is the open loop gain of the op-amp.



**Fig. 3.47** High input impedance capacitor-coupled voltage follower

Rearranging, we have  $v_1(1 + M) = v_s$

$$\text{i.e. } v_1 = \frac{v_s}{(1 + M)}$$

Then,

$$i_1 = \frac{v_1}{R_1} = \frac{v_s}{(1+M)R_1}$$

Input resistance

$$Z_{in} = \frac{v_s}{i_1}$$

or

$$Z_{in} = (1+M)R_1$$

The above equation shows that the circuit acquires a very high input impedance. For example, with an open loop gain of  $10^5$  and a  $33\text{k}\Omega$  resistor for  $R_1$ , the circuit input impedance would become

$$Z_{in} = 10^5 \times 33\text{k}\Omega = 3.3 \times 10^9 \Omega$$

The extremely high input impedance is unrealisable, taking into consideration the stray capacitance which are always present. If the stray capacitance ( $C_S$ ) between the circuit input and ground is assumed to be  $4\text{ pF}$ , the impedance of  $C_S$  at  $2\text{ kHz}$  is

$$X_{CS} = \frac{1}{2\pi f C} = \frac{1}{2\pi \times 2 \times 10^3 \times 4 \times 10^{-12}} = 19.9 \text{ M}\Omega$$

Since this is smaller than the input impedance  $Z_{in}$ , the effective input impedance of a high  $Z_{in}$  voltage follower is normally much less.

Normally, the design of a high input impedance capacitor-coupled voltage follower involves the selection of a single resistor  $R_{1(\max)}$  using the equation

$$R_{1(\max)} = Z_{in} = R_1$$

Then  $R_{1(\max)}$  is split into two equal resistors  $R_1$  and  $R_2$ . For ensuring that the feedback voltage remains nearly 100% of the output voltage at the lowest operating frequency, the required feedback capacitor  $C_2$ , is then calculated as given by

$$X_{C2} = \frac{R_2}{10} \text{ at } f_L$$

The output capacitor is also used to set the lower 3dB frequency point for the high-input impedance voltage follower using

$$X_{C3} = R_L \text{ at } f_L$$

The impedance of input capacitor  $C_1$  can be determined using  $X_{C1} = Z_{in}/10$  at  $f_L$ . However, the actual input impedance is affected by stray capacitance. Moreover, selecting  $C_1$  of much higher value than the possible stray capacitance can result in a peaking effect in the frequency response of the circuit. Therefore, a rule-of-thumb is normally followed to select  $X_{C1} \approx R_1/10$  at  $f_L$  with  $R_1 = R_2$ ,  $X_{C1} = X_{C2}$  and  $C_1 = C_2$ .

In the circuit of Fig. 3.47, a resistor is included in series with the op-amp inverting input terminal to equalise the  $I_B R_B$  voltage drops. However, this is not necessary when the output is capacitor-coupled. When used, the resistor must be equal to  $(R_1 + R_2)$  which is connected between the inverting input terminal and the junction of  $C_2$  and the output of op-amp. In other words, it must not be in series with  $C_2$ .

### Example 3.27

Using the circuit of Fig. 3.47, design a high input impedance capacitor coupled voltage follower and determine its minimum input impedance. Assume  $f_L = 50\text{ Hz}$ ,  $R_L = 3.3\text{k}\Omega$ ,  $I_{B(\max)} = 500\text{nA}$  and  $V_{BE} = 0.6\text{ V}$ .

#### Solution

$$(R_1 + R_2) = R_{1(\max)} = \frac{0.1V_{BE}}{I_{B(\max)}} = \frac{0.1 \times 0.6}{500 \times 10^{-9}} \approx 120\text{k}\Omega$$

$$R_1 = R_2 = \frac{120 \times 10^3}{2} = 60 \text{ k}\Omega$$

We know that  $X_{C3} = R_L$  at  $f_L$

$$\text{Therefore, } C_3 = \frac{1}{2\pi f_L R_L} = \frac{1}{2\pi \times 50 \times 3.3 \times 10^3} = 0.96 \mu\text{F} \approx 1 \mu\text{F}$$

We know that  $X_{C2} = \frac{R_2}{10}$  at  $f_L$

$$\begin{aligned} \text{Therefore, } C_2 &= \frac{1}{2\pi f_L (R_2/10)} = \frac{1}{2\pi \times 50 \times (56 \times 10^3 / 10)} \\ &= 0.57 \mu\text{F} \approx 0.6 \mu\text{F} \end{aligned}$$

i.e.  $C_1 = C_2 = 0.6 \mu\text{F}$

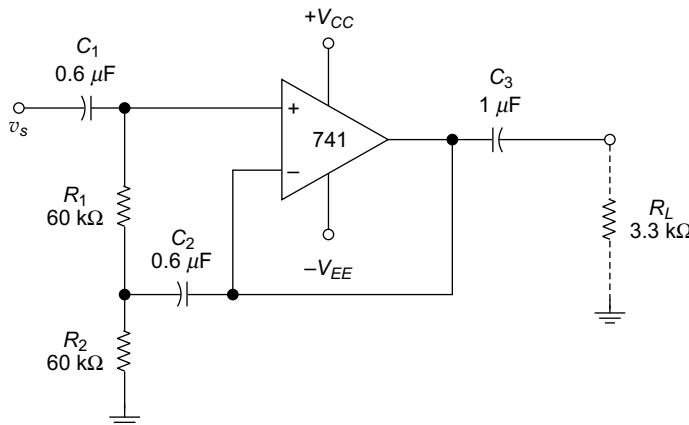
The input impedance  $Z_{in} = (1 + M)R_1$

Further, the 741 data sheet shows that

$M_{(min)} = 50000$

Thus,  $Z_{in(min)} = (1 + 50000) \times 56 \times 10^3 = 2800 \text{ M}\Omega$

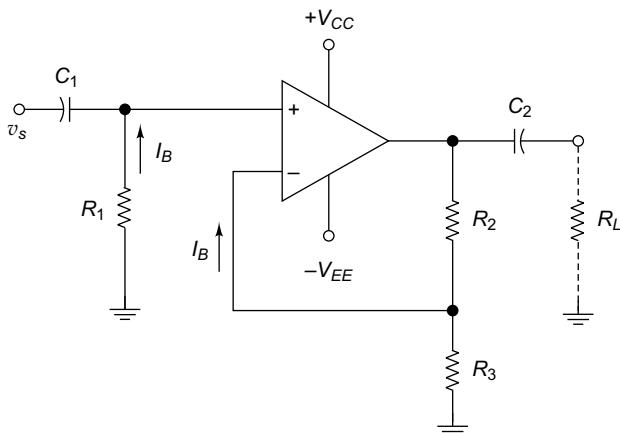
The circuit schematic obtained is shown in Fig. 3.48.



**Fig. 3.48** High input impedance capacitor-coupled voltage follower

**ac non-inverting amplifier** When the input of noninverting amplifier is needed to be capacitor-coupled, the noninverting input terminal should be grounded through a resistor for providing a path for the input bias current. The circuit arrangement is shown in Fig. 3.49. The resistor  $R_1$  is made equal to  $R_2 \parallel R_3$ . The dc offset is not important when the output is capacitor-coupled.

The input impedance  $Z_{in} = R_1$  for the capacitor-coupled non-inverting amplifier. Resistors  $R_2$  and  $R_3$  in Fig. 3.49 are calculated by the same method as that of the direct-coupled circuit. The capacitors are selected in the same manner as for capacitor-coupled voltage follower.

**Fig. 3.49** Capacitor-coupled non-inverting amplifier

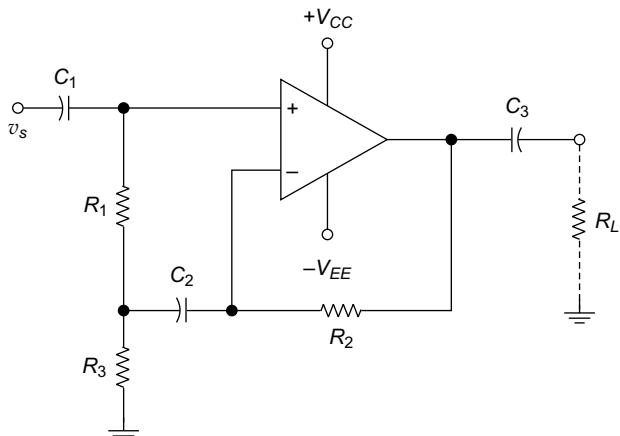
**High input impedance ac non-inverting amplifier** The input impedance of the noninverting amplifier shown in Fig. 3.50 is improved in the same manner as for the high  $Z_{in}$  voltage follower circuit. The voltage divided by a factor  $\beta$  is fed back from the output to the input through the components  $R_2$ ,  $C_2$  and  $R_3$ .

Hence,

$$\beta = R_3 / (R_2 + R_3)$$

and

$$Z_{in} = (1 + M\beta) R_1$$

**Fig. 3.50** High input impedance AC non-inverting amplifier

The resistances  $R_2$  and  $R_3$  for the high input impedance ( $Z_{in}$ ) circuit in Fig. 3.46 are calculated using the same method as that of the direct-coupled noninverting amplifier. Then, for equal  $I_B R_B$  voltage drops, we have

$$(R_1 + R_3) = R_2$$

and this usually yields

$$R_1 \approx R_2$$

Alternatively, for the highest input impedance when the  $I_B R_B$  voltage drops are unequal,

$$(R_1 + R_3) = R_{(\max)} = \frac{0.1 V_{BE}}{I_{B(\max)}}$$

The capacitances can be calculated as for the high  $Z_{in}$  voltage follower. An alternative method for a circuit with a variable load is to use  $C_2$  to determine the lower 3dB frequency. When  $C_2$  is connected in the circuit, the voltage gain becomes

$$A_v = \frac{R_2 + R_3 - jX_{C2}}{R_3 - jX_{C2}}$$

When  $X_{C2} \leq (R_2 + R_3)$ ,

$$A_v \approx \frac{R_2 + R_3}{\sqrt{R_3^2 + X_{C2}^2}}$$

For

$$X_{C2} = R_3$$

$$A_v = \frac{R_2 + R_3}{R_3} \times \frac{1}{\sqrt{2}}$$

Here,  $A_v$  is 3 dB below the normal mid-frequency gain of  $(R_2 + R_3)/R_3$ . Thus, for calculating the value of  $C_2$  to determine  $f_L$ ,

$$X_{C2} = R_3 \text{ at } f_L$$

It is observed that the assumption of  $X_{C2} \ll (R_2 + R_3)$  is valid only when  $X_{C2} = R_3$  and  $R_3 \ll R_2$ . This is the case only when the circuit has appreciable voltage gain.

When  $C_2$  is used to decide the lower cut-off frequency of the circuit,  $C_3$  should not have any effect on the lower 3dB frequency. Then the capacitance of  $C_3$  is selected as any other coupling capacitor, to have an impedance at  $f_L$  which is equal to one-tenth of the minimum resistance in series with  $C_3$ .

### Example 3.28

Design a high input impedance capacitor-coupled noninverting amplifier using the IC LF353 BIFET op-amp for a lower cut-off frequency of 100 Hz. The input and output voltages are 10 mV and 3 V respectively, and the minimum load resistance is 15 kΩ.

#### Solution

$$A_v = \frac{v_o}{v_i} = \frac{3}{10 \times 10^{-3}} = 300$$

Letting  $R_2 = 1 \text{ M}\Omega$  for a BIFET op-amp, we get

$$A_v = \frac{R_2 + R_3}{R_3}$$

$$\text{Therefore } R_3 = \frac{R_2}{A_v - 1} = \frac{1 \times 10^6}{300 - 1} \approx 3.3 \text{ k}\Omega$$

$$R_1 = R_2 - R_3 = 1 \times 10^6 - 3.3 \times 10^3 \approx 1 \text{ M}\Omega$$

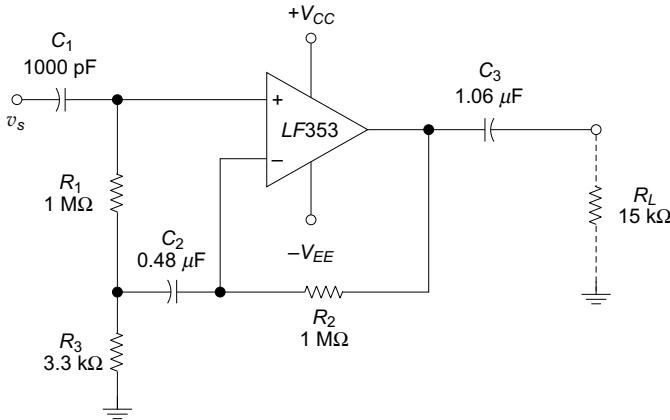
We know that  $X_{C2} = R_3$  at  $f_L$

$$\text{Therefore, } C_2 = \frac{1}{2\pi f_L R_3} = \frac{1}{2\pi \times 100 \times 3.3 \times 10^3} = 0.48 \mu\text{F}$$

Assume  $C_1 = 1000 \text{ pF}$

$$C_3 = \frac{1}{2\pi f_L (R_L/10)} = \frac{1}{2\pi \times 100 \times (15 \times 10^3 / 10)} = 1.06 \mu\text{F}$$

The circuit diagram of high input impedance capacitor-coupled non-inverting amplifier is shown in Fig. 3.51.

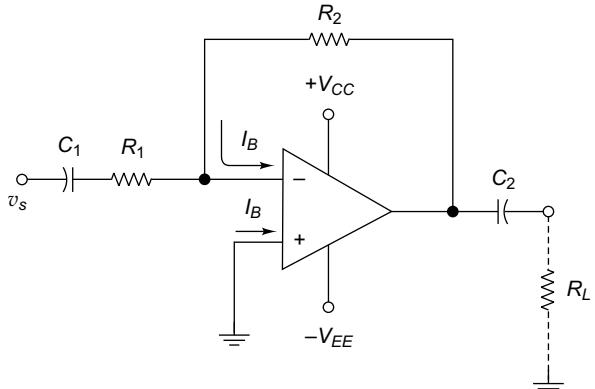


**Fig. 3.51** High input impedance capacitor-coupled non-inverting amplifier circuit

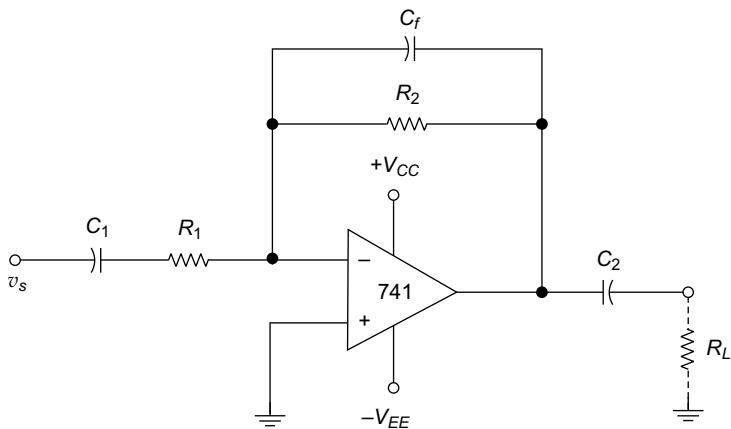
**ac inverting amplifier** Figure 3.52 shows a capacitor-coupled inverting amplifier. The bias current flows through resistor  $R_2$  to the op-amp inverting input terminal. Therefore, the coupling capacitor  $C_1$  does not interrupt the bias current. There is no resistor connected in series with the noninverting input terminal, since the small dc offset is negligible with the capacitor-coupled output.

Here, the resistances are determined as in the case of a simple direct-coupled inverting amplifier circuit. Then  $C_1$  is determined by  $X_{C1} = R_1/10$  at  $f_L$ , and  $C_2$  is determined by  $X_{C2} = R_L$  at  $f_L$ , as in the case of a capacitor-coupled noninverting amplifier.

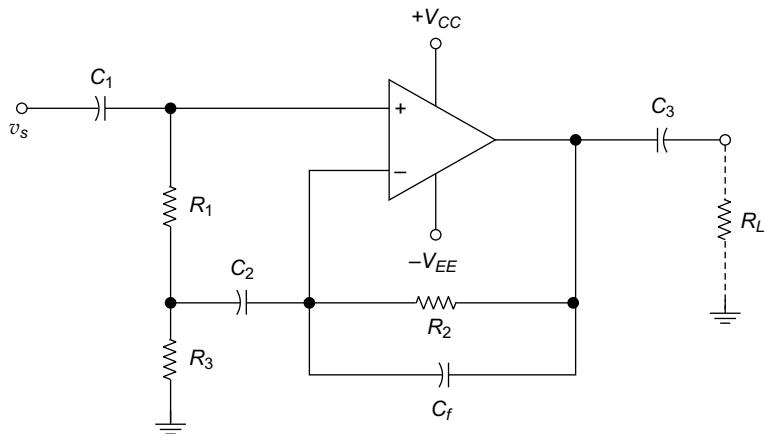
The upper cut-off frequency of the signal is processed depending on the selection of the op-amp. In some cases, the upper cut-off frequency may be higher than what is required. For example, when only low frequency signals are to be amplified, the higher frequency ambient noise voltages are to be avoided. Then, the voltage gain can be made to fall-off just above the highest desired signal frequency. The usual procedure is to connect a feedback capacitor  $C_f$  from the op-amp output to the inverting input terminal as shown in Fig. 3.53 (a) and (b).



**Fig. 3.52** Capacitor-coupled inverting amplifier



**Fig. 3.53 (a)** Inverting amplifier with feedback capacitor



**Fig. 3.53 (b)** Non-inverting amplifier with feedback capacitor

Using the general theory of an inverting amplifier, we get the voltage gain as

$$A_v = \frac{R_2 \| X_{Cf}}{R_1}$$

Therefore,

$$A_v = \frac{1}{R_1 \sqrt{\left(1/R_2\right)^2 + \left(1 + X_{Cf}\right)^2}}$$

Assuming \$X\_{Cf} = R\_2\$, the gain can be written as

$$A_v = \frac{1}{\sqrt{2}} \left( \frac{R_2}{R_1} \right)$$

Here, \$A\_v\$ is 3dB below the normal voltage gain of \$R\_2/R\_1\$. Thus, the upper cut-off frequency for the circuit can be set at the desired frequency (\$f\_H\$).

The upper cut-off frequency of a non-inverting amplifier can also be set as shown in Fig. 3.53(b).

It must be noted that this method of setting the upper cut-off frequency is applicable only when the op-amp is supposed to have a much greater cut-off frequency.

### Example 3.29

Design a capacitor coupled inverting amplifier of Fig. 3.53(a) to have a signal frequency range of 20 Hz to 2 kHz. For a load resistance of  $300 \Omega$ , determine the capacitor values required. Assume  $R_1 = 1.5 \text{ k}\Omega$  and  $R_2 = 56 \text{ k}\Omega$

**Solution** Given  $f_L = 20 \text{ Hz}$ ,  $f_H = 2 \text{ kHz}$ ,  $R_L = 300 \Omega$ ,  $R_1 = 1.5 \text{ k}\Omega$  and  $R_2 = 56 \text{ k}\Omega$

We know that  $X_{C1} = Z_{in}/10$  at  $f_L$

$$\text{Therefore, } C_1 = \frac{1}{2\pi f_L (R_1/100)} = \frac{1}{2\pi \times 20 \times (1.5 \times 10^3 / 10)} = 53 \mu\text{F}$$

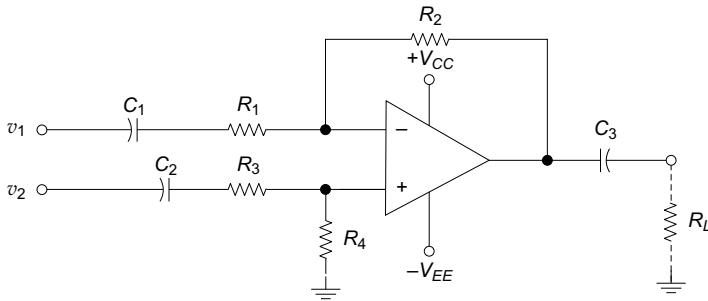
We have  $X_{C2} = R_L$  at  $f_L$ .

$$\text{Therefore, } C_2 = \frac{1}{2\pi f_L R_L} = \frac{1}{2\pi \times 20 \times 300} = 27 \mu\text{F}$$

We know that,  $X_{Cf} = R_2$  at  $f_H$ .

$$\text{Hence, } C_f = \frac{1}{2\pi f_H R_2} = \frac{1}{2\pi \times 2 \times 10^3 \times 56 \times 10^3} = 1421 \text{ pF}$$

**ac difference amplifier** The capacitor-coupled difference amplifier circuit can be constructed as shown in Fig. 3.54. The values of resistors and capacitors are calculated in the same way as for a direct-coupled circuit. At frequency  $f_L$ , the input capacitors  $C_1$  and  $C_2$  are determined from the impedance available at each input terminal and  $X_{C3}$  is made equal to  $R_L$ .



**Fig. 3.54** Capacitor-coupled difference amplifier

That is,

$$X_{C1} = R_1/10,$$

$$X_{C2} = (R_3 + R_4)/10,$$

and

$$X_{C3} = R_L$$

Here, the voltage gain can be rolled-off at the required upper cut-off frequency. For the difference amplifier, the capacitors are connected across resistors  $R_2$  and  $R_4$  with each one at the required cut-off frequency.

**ac voltage follower using a single-polarity power supply** Since the capacitors block the dc bias voltages at input and output, capacitor-coupled op-amp circuits for AC applications can be operated with a single-polarity supply voltage as shown in Fig. 3.55(a). A minimum supply voltage of twice the normal operating voltage of a dual polarity supply is used. As shown in the figure, the potential divider formed by  $R_1$  and  $R_2$  sets the bias voltage at the noninverting input terminal, i.e.,  $V_{CC}/2$ . Thus, the dc levels of the output and the inverting input are at  $V_{CC}/2$ . For instance, while using an 18V supply, the positive supply terminal is +9V with respect to the bias level at input and output terminals, and the negative supply terminal is -9V with respect to these input and output terminals.

The resistors forming the potential divider are calculated by choosing a current  $I_2$  that is much larger than input bias current of the op-amp. The input impedance of the circuit is given by

$$Z_{in} = R_1 \parallel R_2$$

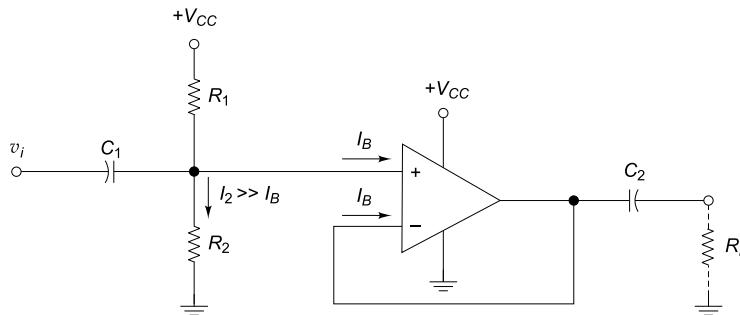
Thus,

$$X_{C1} = (R_1 \parallel R_2)/10 \text{ at } f_L$$

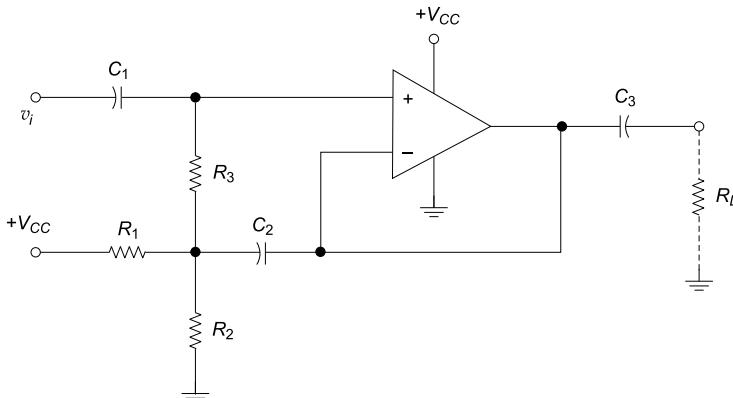
and

$$X_{C2} = R_L \text{ at } f_L$$

Figure 3.55(b) shows the circuit diagram of a capacitor-coupled voltage follower using a single polarity supply for high input impedance applications. The potential divider  $R_1$  and  $R_2$  sets the bias voltage at  $V_{CC}/2$ . Resistor  $R_3$  is included in the circuit, so that its bottom terminal can be pushed up and down with the use of feedback obtained through  $C_2$ . Hence, this arrangement offers an input impedance of  $(1 + M)R_3$ . The resistance in series with capacitor  $C_2$  is  $R_1 \parallel R_2$ , since the top terminal of  $R_1$  is ac grounded through  $V_{CC}$ . Hence,  $C_2$  is determined from  $X_{C2} = (R_1 \parallel R_2)/10$  at  $f_L$ .

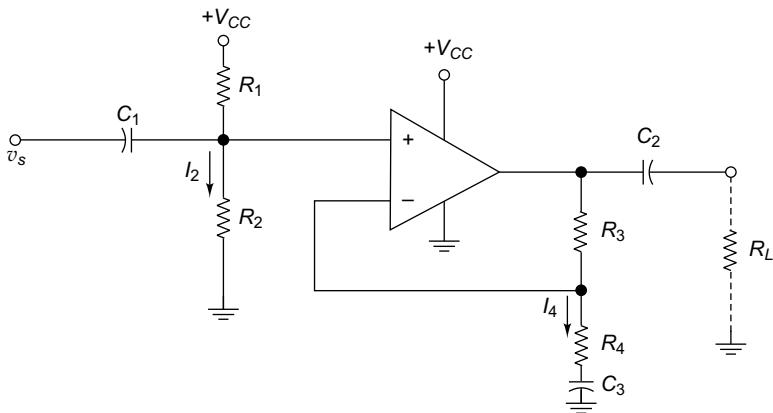


**Fig. 3.55 (a)** Capacitor-coupled voltage follower circuit using single polarity supply

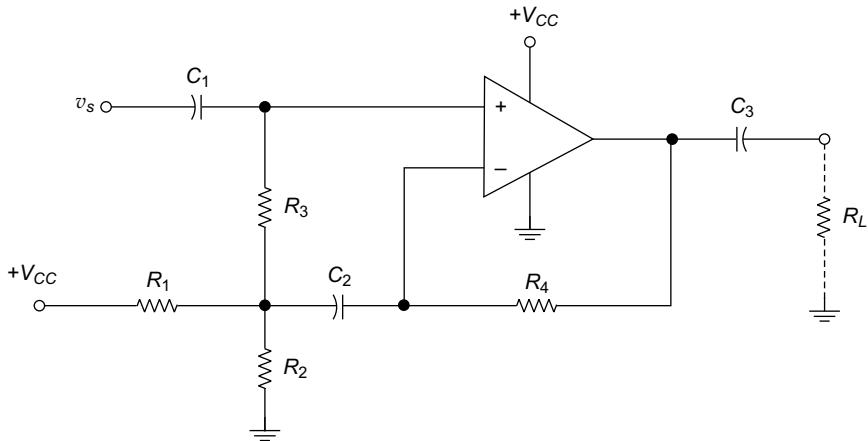


**Fig. 3.55 (b)** High input impedance capacitor-coupled voltage follower circuit using single polarity supply

**ac non-inverting amplifier using a single-polarity power supply** The capacitor-coupled noninverting amplifier circuit using a single polarity supply is shown in Fig. 3.56(a). The potential divider formed by  $R_1$  and  $R_2$  biases the op-amp noninverting input terminal at  $V_{CC}/2$ . This positive dc level is intentionally inserted, so that the output can swing in both the positive and negative directions. The bottom of resistor  $R_4$  is capacitor-coupled to ground through capacitor  $C_3$ . When this point is directly grounded, the dc voltage at the op-amp output terminal will be  $A_v \times V_{CC}/2$ . The output gets saturated at approximately  $(V_{CC} - 1\text{V})$ . The circuit will behave like a dc voltage follower with  $C_3$  and  $R_3$  connecting the inverting input terminal to the output. For dc voltages, the dc voltage level at the output terminal of the op-amp is then equal to that at the noninverting input terminal, namely,  $V_{CC}/2$ . For ac voltages,  $C_3$  behaves as a short circuit and hence the ac output voltage becomes  $v_o = v_i(R_3 + R_4)/R_4$ .



**Fig. 3.56 (a)** Capacitor-coupled non-inverting amplifier circuit using single polarity supply



**Fig. 3.56 (b)** High input impedance capacitor-coupled noninverting amplifier circuit using single polarity supply

The values of components  $C_1, C_2, R_1$  and  $R_2$  are determined as discussed earlier for the voltage follower. The resistors  $R_3$  and  $R_4$  are calculated in the usual way as that of a noninverting amplifier.

Capacitor  $C_3$  should be selected to have an impedance value which is appreciably less than  $R_4$  at the lower 3dB frequency of the circuit. Thus, it can be set as  $X_{C3} = R_4/10$  at  $f_L$ . Capacitor  $C_3$  can also be determined based on the lower cut-off frequency requirement of the circuit. This method is preferable while operating the circuit with variable load. Then,  $X_{C3} = R_4$  at  $f_L$ , and  $X_{C2} = R_{L(min)}/10$  at  $f_L$ .

### Example 3.30

---

Using a 741 op-amp, design a capacitor-coupled noninverting amplifier circuit to operate with a +24V supply. The voltage gain is 100, output amplitude is 6 V and lower cut-off frequency is to be 100 Hz to drive a minimum load resistance is 5.6 k $\Omega$ .

**Solution** We know that  $I_2 \gg I_{B(max)}$ , where  $I_{B(max)}$  for 741 op-amp is 500 nA

$$\text{Assuming } I_2 = 100 \times I_{B(max)} = 100 \times 500 \times 10^{-9} = 50 \mu\text{A}$$

$$R_1 = R_2 = \frac{V_{CC}/2}{I_2} = \frac{24/2}{50 \times 10^{-6}} = 240 \text{ k}\Omega$$

$$v_i = \frac{v_o}{A_v} = \frac{6}{100} = 60 \text{ mV}$$

$$I_4 \gg I_{B(max)}$$

$$\text{We know that } I_4 = 100 \times I_{B(max)} = 100 \times 500 \times 10^{-9} = 50 \mu\text{A}$$

$$R_4 = \frac{v_i}{I_4} = \frac{60 \times 10^{-3}}{50 \times 10^{-6}} = 1.2 \text{ k}\Omega$$

$$(R_3 + R_4) = \frac{v_o}{I_4} = \frac{6}{50 \times 10^{-6}} = 120 \text{ k}\Omega$$

$$R_3 = (R_3 + R_4) - R_4 = 120 \text{ k}\Omega - 1.2 \text{ k}\Omega = 118.8 \text{ k}\Omega$$

$$\text{We know that } X_{C1} = Z_{in}/10 \text{ at } f_L$$

$$\begin{aligned} \text{Therefore, } C_1 &= \frac{1}{2\pi f_L (R_1 \parallel R_2)/10} \\ &= \frac{1}{2\pi \times 100 \times (240 \times 10^3 \parallel 240 \times 10^3)/10} = 0.1326 \mu\text{F} \end{aligned}$$

$$C_2 = \frac{1}{2\pi f_L R_L/10} = \frac{1}{2\pi \times 100 \times (5.6 \times 10^3/10)} = 2.84 \mu\text{F}$$

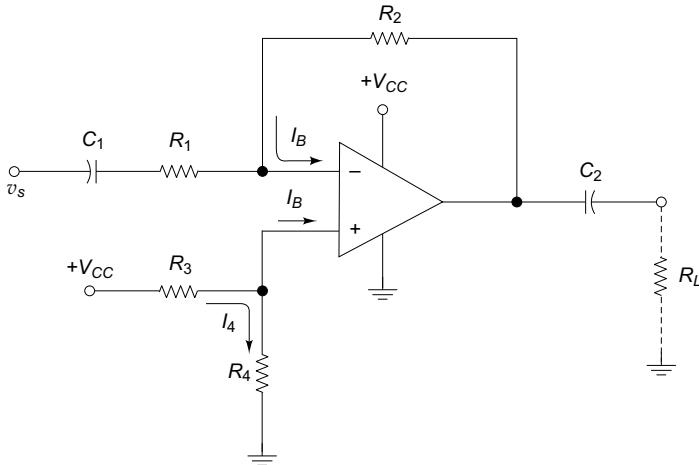
$$C_3 = \frac{1}{2\pi f_L R_4} = \frac{1}{2\pi \times 100 \times 1.2 \times 10^3} = 1.326 \mu\text{F}$$

**ac inverting amplifier using a single polarity supply** Figure 3.57 shows the circuit diagram of an inverting amplifier using a single polarity supply. The potential divider  $R_3$  and  $R_4$  sets the noninverting input terminal at  $V_{CC}/2$ . This positive dc voltage level is intentionally inserted, so that the output can swing in both the positive and negative directions. The dc voltage level of the output and the inverting input

terminal will also be  $V_{CC}/2$ . The values of  $R_3$  and  $R_4$  for potential divider are selected by initially fixing a current  $I_4$  which is much larger than the current  $I_B$  flowing out of the potential divider. Then, we have

$$R_3 = R_4 = \frac{V_{CC}/2}{I_4}$$

The ac output voltage is given by  $v_o = -v_i(R_2/R_1)$ . The op-amp output is the ac riding on a dc level of  $+V_{CC}/2$ . The output coupling capacitor  $C_2$  blocks this dc voltage and the resulting waveform is a pure ac.



**Fig. 3.57** AC inverting amplifier using a single-polarity supply

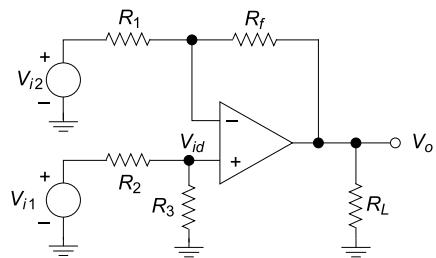
## 3.12 DIFFERENTIAL AMPLIFIER

The differential amplifier, also called *difference amplifier*, can be constructed using a single op-amp or two op-amps with constant or variable gain in closed-loop configuration.

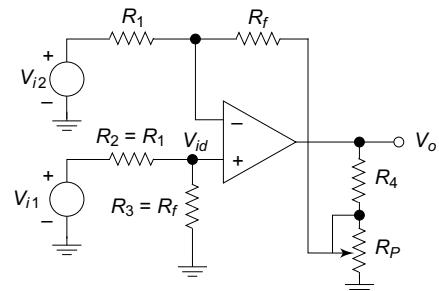
### 3.12.1 Differential Amplifier with Single Op-amp

The basic op-amp can be used as a differential amplifier as shown in Fig. 3.58(a). To analyse the operation of the circuit, assume that all resistors are equal of value  $R$ . The output voltage can be determined by using the superposition principle. It is assumed for analysis that,  $R_1 = R_2 = R_3 = R_f = R$ . Then, if  $V_{il} = 0$  or grounded, then the output voltage  $V_{o2}$  will be due to the input voltage  $V_{i2}$  alone. Hence, the circuit shown in Fig. 3.58(a) becomes an inverting amplifier with the output voltage as given by

$$V_{o2} = -[V_{i2}/2](1 + R/R) = -V_{i2}$$



**Fig. 3.58 (a)** Differential amplifier



**Fig. 3.58 (b)** Differential amplifier with variable gain

Similarly, if  $V_{i2}=0$ , then the output voltage  $V_{o1}$  will be due to  $V_{i1}$  alone. Hence the circuit becomes a non-inverting amplifier and the output voltage is given by

$$V_{o1} = \frac{V_{i1}}{2} \left( 1 + \frac{R_f}{R} \right) = V_{i1} \quad (3.62)$$

Now, considering that both the inputs are applied, the output voltage  $V_o$  is

$$V_o = V_{o1} + V_{o2} = V_{i1} - V_{i2} \quad (3.63)$$

Thus, the output voltage is proportional to the difference between the two input voltages. Hence, it acts as a *difference amplifier* and is also called *differential amplifier*. If the resistors are selected such that  $R_f \neq (R_1 \neq R_2 \neq R_3)$ , then the output voltage  $V_o$  is expressed by

$$V_o = \left( 1 + \frac{R_f}{R} \right) \left( \frac{R_3}{R_3 + R_2} \right) V_{i1} - \frac{R_f}{R} V_{i2} \quad (3.64)$$

By changing the input resistors individually, difference amplifier for different strengths of input signals can be realized.

Figure 3.58(b) shows the differential amplifier circuit with variable gain. This circuit has  $R_1 = R_2$ ,  $R_f = R_4$  and the potentiometer  $R_p = R_4$ . Hence, based on the position of the variable terminal in  $R_p$ , the voltage gain can be correspondingly varied.

**Difference-mode gain and common-mode gain** For Eq. (3.64), if  $R_f = R$  and  $V_{i2} = V_{i1}$ , then the output voltage  $V_o = 0$ . This means that the signal common to both the inputs compensate each other and produces no effective output voltage. This characteristic is true for an ideal op-amp based difference amplifier. However, a practical op-amp exhibits a small response to the common mode values of the input voltages also. The output voltage depends on the difference  $V_{id}$  between the input signals and it also depends on the common mode signal  $V_{cm}$ . This common mode signal  $V_{cm}$  is defined as

$$V_{cm} = \frac{V_{i1} + V_{i2}}{2} \quad (3.65)$$

Though the differential amplifier is symmetric, because of the mismatch between the circuit components, the gain at the output in response to the positive and negative terminal are found to be different in practice. Therefore, even with the same voltage applied at both the inputs, the output is not found to be zero. Then the output can be expressed as

$$V_o = A_1 V_{o1} + A_2 V_{o2}$$

where  $A_1$  and  $A_2$  are the voltage amplification factors for the inputs  $V_{i1}$  and  $V_{i2}$  respectively, when the other input is grounded.

Using Eq. (3.65) and the fact that  $V_{id} = (V_{i1} - V_{i2})$ , we get

$$V_{i1} = V_{cm} + \frac{1}{2} V_{id} \text{ and} \quad (3.66)$$

$$V_{i2} = V_{cm} - \frac{1}{2} V_{id} \quad (3.67)$$

Substituting the values of  $V_{i1}$  and  $V_{i2}$  from Eqs. (3.66) and (3.67) in Eq. (3.65), we get

$$V_o = A_{dm} V_{id} + A_{cm} V_{cm} \quad (3.68)$$

where the difference mode gain  $A_{dm} = \frac{1}{2} (A_1 - A_2)$  and the common mode gain  $A_{cm} = A_1 + A_2$ .

**Common-Mode Rejection Ratio (CMRR)** The common-mode rejection ratio is defined as the ratio of the differential gain  $A_{dm}$  to the common-mode gain  $A_{cm}$ .

i.e.

$$CMRR = \frac{A_{dm}}{A_{cm}} \quad (3.69)$$

This represents the *figure of merit* for the differential amplifier and it is usually represented in *decibels* (dB).

For example, the IC  $\mu$ A 741 has a minimum CMRR of 70 dB and a precision op-amp such as  $\mu$ A725A has 120dB for its CMRR. Higher the value of CMRR, better is the op-amp.

### Example 3.31

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For a given op-amp,  $CMRR=10^5$  and differential gain  $A_{dm} = 10^5$ . Determine the common-mode gain  $A_{cm}$  of the op-amp.

#### Solution

$$CMRR = \frac{A_{dm}}{A_{cm}} = 10^5$$

Therefore, the common-mode gain  $A_{cm} = \frac{A_{dm}}{CMRR} = \frac{10^5}{10^5} = 1$ .

### Example 3.32

---

The two input terminals of an op-amp are connected to voltage signals of strengths  $745 \mu V$  and  $740 \mu V$  respectively. The gain of the op-amp in differential mode is  $5 \times 10^5$  and CMRR is 80 dB. Calculate the output voltage and % error due to common mode.

**Solution** Given  $CMRR = 80 \text{ dB}$ ,  $V_1 = 745 \mu V$ ,  $V_2 = 740 \mu V$ ,  $A_d = 5 \times 10^5$

$$\text{CMRR in dB} = 20 \log \frac{A_{dm}}{A_{cm}}$$

Therefore,  $80 = 20 \log \frac{5 \times 10^5}{A_{cm}}$

$$\text{i.e. } 10000 = \frac{5 \times 10^5}{A_{cm}}$$

Hence, common mode gain  $A_{cm} = 50$

$$\begin{aligned} V_o &= A_{dm}V_{dm} + A_{cm}V_{cm}, \text{ where } V_{cm} = \frac{V_1 + V_2}{2}, V_{dm} = V_1 - V_2 \\ &= 5 \times 10^5 [745 - 740] \times 10^{-6} + 50 \times \left[ \frac{745 + 740}{2} \right] \times 10^{-6} = 2.5371 \text{ V} \end{aligned}$$

Ideal output  $A_{dm}V_{dm} = 2.5 \text{ V}$

$$\text{Hence, } \% \text{ error} = \frac{2.5371 - 2.5}{2.5} \times 100 = 1.484\%$$

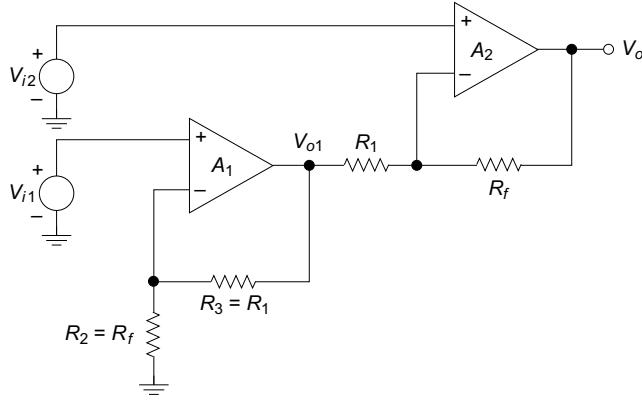
**Limitations of the basic differential amplifier** The two major limitations of the basic differential amplifier are (i) it has low input resistance, and (ii) modifying the gain is cumbersome, since the resistor ratios must be closely matched.

The first disadvantage can be eliminated by *isolating* or *buffering* the two inputs using voltage followers. This is realised by using two op-amps connected as voltage followers as discussed in the next subsection.

The second limitation of the basic differential amplifier is the lack of adjustable gain feature. This can be eliminated by the use of three more resistors. This will be discussed as part of instrumentation amplifier circuit of Section 4.15. The amplifier gain in such a circuit will be changed by only a single resistor.

### 3.12.2 Differential Amplifier with Two Op-amps

The gain of the differential amplifier shown in Fig. 3.59 is the same as that of inverting amplifier shown in Fig. 3.39. The gain can be increased further by the use of two op-amps. The input resistance of such a circuit also increases.



**Fig. 3.59** Differential amplifier with two op-amps

Figure 3.59 shows the circuit configuration of the differential amplifier with two op-amps. It is composed of a non-inverting amplifier formed by op-amp  $A_1$  followed by a differential amplifier, both with unequal gains. By calculating the individual gains of these stages, the overall gain of the circuit can be calculated.

The output  $V_{o1}$  of the first stage is given by

$$V_{o1} = \left(1 + \frac{R_3}{R_2}\right) V_{i1} \quad (3.70)$$

The input  $V_{i2}$  acts as the non-inverting input with the gain of  $\left(1 + \frac{R_f}{R_l}\right) V_{i2}$  and the output  $V_{o1}$  of the first stage acts as the inverting input with a gain of  $-\frac{R_f}{R_l} V_{o1}$  for the differential amplifier formed by the op-amp  $A_2$ . Therefore, by applying superposition theorem to the second stage, we get the output voltage  $V_o$  represented by

$$V_o = -\frac{R_f}{R_l} V_{o1} + \left(1 + \frac{R_f}{R_l}\right) V_{i2} \quad (3.71)$$

Substituting for the value of  $V_{o1}$  from Eq. (3.70) in (3.71), we get

$$V_o = -\frac{R_f}{R_l} \left(1 + \frac{R_3}{R_2}\right) V_{i1} + \left(1 + \frac{R_f}{R_l}\right) V_{i2} \quad (3.72)$$

Assuming  $R_f = R_3$  and  $R_1 = R_2$ , we have

$$V_o = \left(1 + \frac{R_f}{R_1}\right)(V_{i2} - V_{i1}) \quad (3.73)$$

Therefore, the gain of the two op-amp differential amplifier is given by

$$A_D = \frac{V_o}{V_{id}} = \left(1 + \frac{R_f}{R_1}\right) \quad (3.74)$$

where

$$V_{id} = V_{i2} - V_{i1}$$

**Input resistance** The input resistance  $R_i$  of the differential amplifier is the resistance found looking into either of the two non-inverting input terminals with the other input grounded as shown in Fig. 3.59. The first stage is a non-inverting amplifier and its input resistance is

$$R_{i1} = R_i(1 + A\beta_1) \quad (3.75)$$

where  $R_i$  is the open-loop resistance of the op-amp and  $\beta_1 = \frac{R_2}{R_2 + R_3}$ .

Similarly, shorting the input  $V_{o1}$  to ground, the second stage  $A_2$  also becomes a non-inverting amplifier and its input resistance can be expressed as

$$R_{i2} = R_i(1 + A\beta_2) \quad (3.76)$$

where  $R_i$  is the open-loop resistance of the op-amp and  $\beta_2 = \frac{R_1}{R_1 + R_f}$ .

Assuming  $R_1 = R_3$  and  $R_f = R_2$ , we find  $R_{i1} \neq R_{i2}$ . Since  $R_{i1} \neq R_{i2}$ , the loading of the input sources  $V_{i1}$  and  $V_{i2}$  may happen. In other words, the output signal may be amplified less than what is expected. This is the limitation of the differential amplifier formed using two op-amps. The advantage of this circuit is the high input impedance achieved for the two input signals.

**Output resistance and bandwidth** The output resistance of the differential amplifier is the same as that of the non-inverting or inverting amplifier configurations with the exception that  $\beta = 1/A_D$ . It can be expressed as

$$R_{of} = \frac{R_o}{1 + A/A_D}$$

where  $A_D$  is the closed-loop gain of the differential amplifier, which is different for each of the differential amplifier configurations and  $R_o$  is the output resistance of the op-amp.

The bandwidth of the differential amplifier also depends on the closed-loop gain of the amplifier and it is given by

$$BW_{CL} = \frac{\text{Unity gain bandwidth}}{\text{Closed loop gain}}$$

or

$$BW_{CL} = \frac{A_0 \times f_1}{A_D}$$

where  $f_1$  is the open-loop break frequency of the op-amp.

### Example 3.33

Assume that  $R_i = R_3 = 560 \Omega$ ,  $R_f = R_2 = 5.6 \text{ k}\Omega$ ,  $v_{o1} = -2 \text{ V (peak-to-peak)}$ ,  $v_{o1} = -1 \text{ V (peak-to-peak)}$

for the circuit shown in Fig. 3.59 and IC 741 is used with  $R_i = 2\text{M}\Omega$  and open-loop gain  $A = 2 \times 10^5$ . Determine the (i) voltage gain, (ii) input resistance and (iii) output voltage of the differential amplifier.

### Solution

- (i) Using Eq. (3.74), the voltage gain

$$A_D = 1 + \frac{R_f}{R_i} = 1 + \frac{5.6 \times 10^3}{560} = 11$$

- (ii) The input resistances can be found using Eqs. (3.75) and (3.76) as follows.

$$R_{i1} = R_i \left[ 1 + \frac{AR_2}{R_2 + R_3} \right] = 2 \times 10^6 \left[ 1 + \frac{2 \times 10^5 \times 5.6 \times 10^3}{5.6 \times 10^3 + 560} \right] = 363.7 \text{ G}\Omega$$

$$R_{i2} = R_i \left[ 1 + \frac{AR_1}{R_1 + R_f} \right] = 2 \times 10^6 \left[ 1 + \frac{2 \times 10^5 \times 560}{560 + 5.6 \times 10^3} \right] = 36.37 \text{ G}\Omega$$

- (iii) The output voltage can be calculated using the equation

$$v_o = A_D v_{id} = \left( 1 + \frac{R_f}{R_i} \right) (v_{o2} - v_{o1}) = 11 \times (-1 + 2) = 11 \text{ V (peak-to-peak)} \text{ at the input frequency of } 1 \text{ kHz.}$$

## 3.13 GENERAL DESCRIPTION, MANUFACTURER'S SPECIFICATIONS AND ELECTRICAL CHARACTERISTICS OF THE OP-AMP 741

Each integrated circuit manufacturer employs a specific code and allots a specific type number to the ICs, which they produce. For instance, the IC 741, which is an internally compensated and widely used op-amp originally manufactured by Fairchild as  $\mu\text{A}741$  has the symbols  $\mu\text{A}$  representing the identifying initials used by Fairchild. The codes used by some of the well known manufacturers of linear ICs are:

(i) Fairchild	$\mu\text{A}, \mu\text{AF}$
(ii) National Semiconductor	LM, CH, LF, TBA
(iii) Motorola	MC, MFC
(iv) RCA	CA, CD
(v) Texas Instruments	SN
(vi) Signetics	N/S, NE/SE
(vii) Burr-Brown	BB

A number of other manufacturers also produce the most popular ICs such as these known manufacturers. For easy identification and use, they usually preserve the original type number of the IC along with their identifying initials distinctive for their company. Fairchild's original  $\mu\text{A}741$  is manufactured by other manufacturers and designated as follows by the vendors:

(i) National Semiconductor	LM741
(ii) Motorola	MC1741
(iii) RCA	CA3741
(iv) Texas Instruments	SN52741
(v) Signetics	N5741

It can be noticed that the last three digits in each manufacturer's designation is 741. All these op-amps have the same specifications. Since a number of manufacturers produce the same IC with the same numeral identification, one can refer to such ICs by their type number itself. For example,  $\mu A741$  or MC1741 can be simply referred to as 741.

Some linear ICs are available in various classes such as *A*, *C*, *E*, *S* and *SC*. For instance, the ICs identified by 741, 741A, 741C, 741E, 741S and 741SC are different versions of the same op-amp. The main difference among these op-amps are

741	Military grade op-amp (Operating temperature range 55° to 125°C)
741C	Commercial grade op-amp (Operating temperature range 0° to 70°/75°C)
741A	Improved version of 741
741E	Improved version of 741C
741S	Military grade op-amp with higher slew-rate
741SC	Commercial grade op-amp with higher slew-rate

The schematic diagram and electrical parameters for all these models of IC 741 are the same, except that the values of some of the parameters differ from one model to the other. The general description and electrical characteristics of the Fairchild  $\mu A741$  op-amp are given below:

### 3.13.1 General Description

- (i)  $\mu A741$  is an internally frequency-compensated op-amp
- (ii) It is a monolithic IC, fabricated using planar epitaxial process
- (iii) It has internal short-circuit protection
- (iv) It has externally connected offset null capability
- (v) It has large common-mode and differential voltage ranges
- (vi) It is useful in many applications such as integrator, differentiator, adder, subtractor, voltage follower or buffer and other feedback applications
- (vii) It consumes low power
- (viii) No latch-up occurs
- (ix) It is available in all the three types of packages, namely, 8-pin metal Can, 10-pin Flatpack and 8 or 14-pin dual-in-line package or DIP
- (x) For 741C, two sets of electrical specifications are provided, where the first set is meant for operating characteristics at room temperature (25°C) and the other set applies to the commercial temperature range (0° to +70°C)

### 3.13.2 Absolute Maximum Ratings

Supply voltage	
$\mu A741A$ , $\mu A741$ , $\mu A741E$	±22V
$\mu A741C$	±18V
Internal Power Dissipation	
Metal Can	500mW
Moulded and Hermetic DIP	670mW
Mini DIP	310mW
Flatpack	570mW
Differential Input Voltage	±30V

Input Voltage	$\pm 15$ V
Operating temperature range	
Military ( $\mu A741A, \mu A741$ )	-55°C to 125°C
Commercial ( $\mu A741E, \mu A741C$ )	0°C to 70°C

### 3.13.3 Electrical Characteristics

The different electrical characteristics are given in Table 3.1.

**Table 3.1** Electrical characteristics at  $V_s = 15V$ ,  $T_A = 25^\circ C$

Characteristics	Conditions	Min	TYP	MAX
Input Offset Voltage	$R_s \leq 10$ k $\Omega$		20 mV	60 mV
Input Offset Current			20 nA	200 nA
Input Bias Current			80 nA	500 nA
Input Resistance		0.3 M $\Omega$	2 M $\Omega$	
Input Capacitance			1.4 pF	
Offset Voltage Adjustment Range		$\pm 15$ mV		
Input Voltage Range		$\pm 12$ V	$\pm 13$ V	
Common Mode Rejection Ratio	$R_s \leq 10$ k $\Omega$	70 dB	90 dB	
Supply Voltage Rejection Ratio	$R_s \leq 10$ k $\Omega$		30 $\mu$ V/V	150 $\mu$ V/V
Large Signal Voltage Gain	$R_L \geq 2$ k $\Omega$	20,000	200,000	
	$V_{out} = \pm 10$ V			
Output Voltage Swing	$R_L \geq 10$ k $\Omega$	$\pm 12$ V	$\pm 14$ V	
	$R_L \geq 2$ kW	$\pm 10$ V	$\pm 13$ V	
Output Resistance			75 $\Omega$	
Output Short Circuit Current			25 mA	
Supply Current			1.7 mA	2.8 mA
Power Consumption			50 mW	85 mW
Transient Response Rise Time	$V_i = 20$ mV, $R_L = 2$ k $\Omega$			0.3 $\mu$ s
(Unity Gain) Overshoot	$C_L = 100$ pF			6%
Slew Rate	$R_s \geq 2$ k $\Omega$			0.5 V/ms

### 3.13.4 Description of Electrical Parameters

The various electrical parameters given in Table 3.1 are described below:

**Input offset voltage** It is the voltage that must be supplied between the two input terminals of an op-amp for making the output zero. For 741C, the maximum value of input offset voltage is  $\pm 60$  mV

**Input offset current** The algebraic difference between the two currents entering the inverting (-) input and non-inverting (+) input is referred to as the input offset current. For IC 741C, the maximum value of offset current is 200 nA.

**Input bias current** The average of the currents entering the inverting (–) input and non-inverting (+) input terminals of an op-amp is called the input bias current. Its maximum value is 500nA for 741C.

**Input resistance** This is the differential input resistance as observed at either of the input terminals, with the other terminal connected to ground terminal. For 741 C, the typical input resistance is 2 M $\Omega$ .

**Input capacitance** It is the equivalent capacitance that is measured at either of the two input terminals with the other terminal connected to ground terminal. The typical value of input capacitance  $C_i$  is 1.4 pF.

**Offset voltage adjustment range** The special feature of the 741 family op-amp is the external terminals provided for offset voltage nulling. For IC 741C, the offset voltage adjustment range is of the order of  $\pm 15$  mV.

**Input voltage range** This is the common-mode voltage that can be applied to both input terminals without hindering the performance of the op-amp. The maximum range of the input common-mode voltage for the IC 741 is  $\pm 15$  V. The common-mode configuration is used mainly for testing the degree of matching achieved between the inverting and non-inverting input terminals.

**Supply voltage rejection ratio** The change in input offset voltage of the op-amp due to variations in supply voltage is called the supply voltage rejection ratio (SVRR). Some manufacturers use terms such as power supply rejection ratio (PSRR) or power supply sensitivity (PSS). These terms are expressed in microvolts per volt or in decibels. For the IC 741C, SVRR = 150  $\mu$ V/V. It is understood that op-amps with lower value of SVRR are preferable for achieving better performance.

**Large signal voltage gain** An op-amp amplifies the voltage difference between the two input terminals and, therefore, its voltage gain is defined as

$$\text{Voltage gain} = \frac{\text{Output voltage}}{\text{Differential input voltage}}$$

Since the amplitude of the output signal is much larger than that of the input signal, the voltage gain is commonly referred to as large signal voltage gain. For 741C, the typical value is 200,000 or  $2 \times 10^5$  under test conditions with  $R_L \geq 2$  k $\Omega$  and  $V_o = \pm 10$  V.

**Output voltage swing** The output voltage swing denotes the value of positive and negative saturation voltages of the op-amp, and it can never exceed the supply voltage  $V^+$  and  $V^-$ . For 741C, the output voltage swing is guaranteed to be between the range of +13 V and –13 V for  $R_L \geq 2$  k $\Omega$ .

**Output resistance:** Output resistance  $R_o$  is the resistance measured between the output terminal of the op-amp and the ground terminal. It is 75  $\Omega$  for the 741C op-amp.

**Output short circuit current** This is the current that may flow when the op-amp gets accidentally short-circuited and it is generally high. Hence, the op-amp must be provided with short circuit protection. The short circuit current  $I_{SC}$  for 741C is 25 mA. This represents that the built-in short circuit protection is guaranteed to withstand a maximum current of 25 mA.

**Supply current** Supply current  $I_S$  is the current drawn by the op-amp from the power supply. It is normally 2.8 mA for 741C.

**Power consumption** This gives the amount of quiescent power ( $V_i = 0$  V) that is consumed by the op-amp to operate effectively. The value is 85 mW for 741C.

**Transient response** The rise time and overshoot are the two important characteristics representing the transient response of any circuit. These parameters are of concern while selecting an op-amp for ac applications. For 741C, the rise time is  $0.3\mu$ s and the overshoot can be 5%.

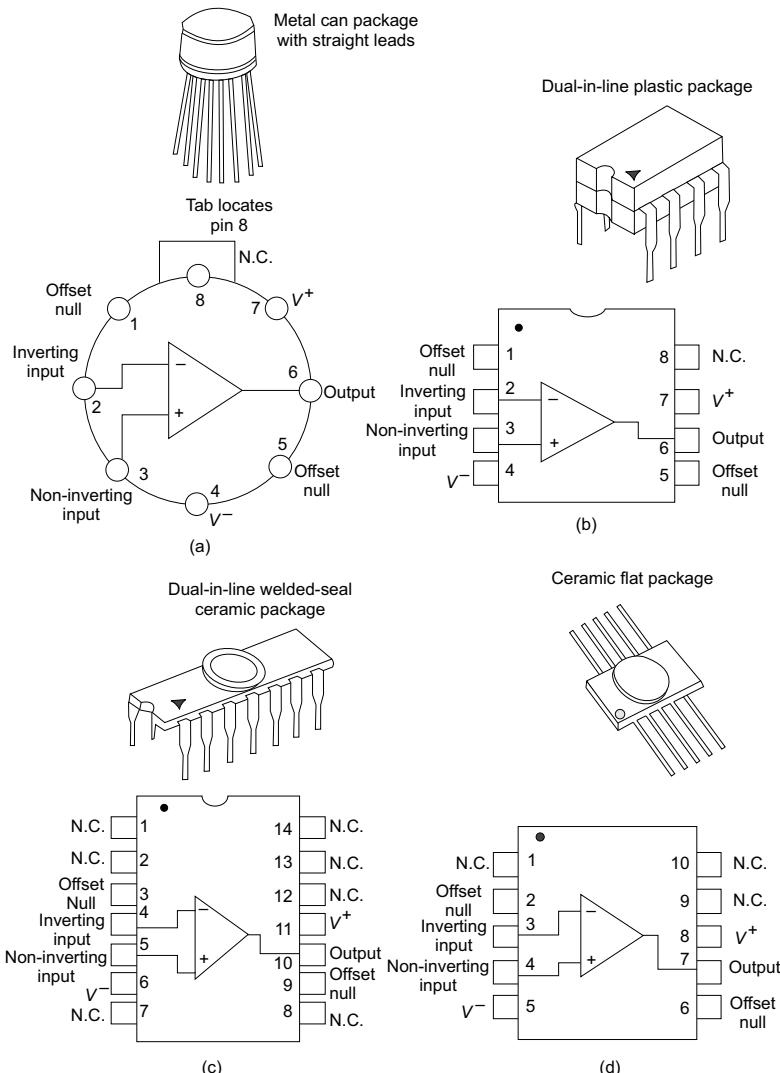
**Slew rate** This is another parameter of importance while selecting an op-amp for high frequency applications. Op-amp 741C has a low slew rate (0.5 V/ $\mu$ s) and this value limits its use for high frequency applications.

### 3.13.5 Packages

The normal packages available for the op-amps are

- the metal Can (TO) package
- the dual in line (DIP) package
- the flat package

The op-amp packages are available with single, dual or quad (four) op-amps contained in a single package. The typical packages have 8, 10 or 14 terminals for a single op-amp IC. The widely popular IC  $\mu$ A741 is a single op-amp available as an 8-pin DIP and TO package, a 10-pin Can or a 14-pin DIP. The  $\mu$ A747 is a chip containing two op-amps which comes as a 10-pin Can or a 14-pin DIP. The packages and the pin connections of IC 741 are shown in Fig. 3.60(a) through Fig. 3.60(d).



**Fig. 3.60** Packages of IC  $\mu$ A741 with pin diagrams: (a) 8-pin metal Can (b) 8-pin mini DIP (c) 14-pin DIP (d) 10-pin Flatpack

### 3.13.6 Op-amp Terminals

The general purpose op-amp normally has five basic terminals, namely, two input terminals, one output terminal and two power supply terminals for positive and negative voltages.

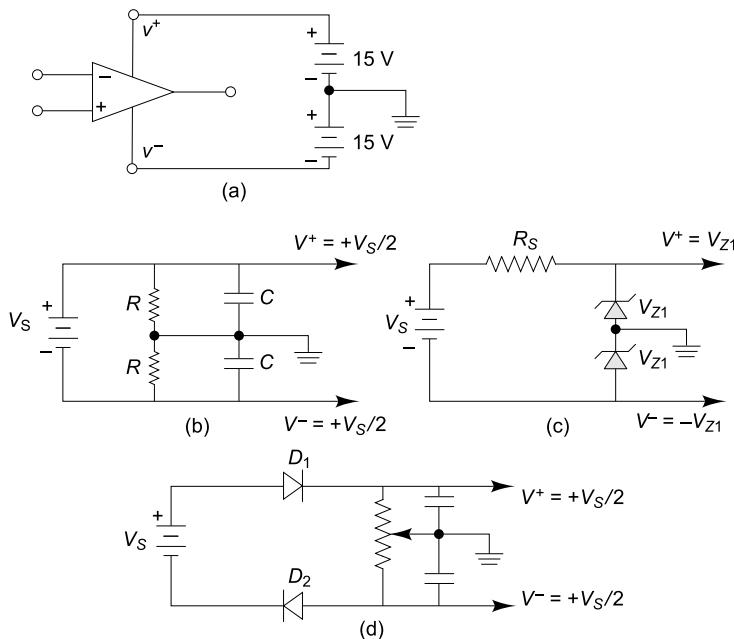
Referring to the top view of a metal Can package of IC  $\mu$ A741 with 8 pins shown in Fig. 3.60(a), the pin number 8 is identified with a tab. The numbering for the IC is done counter clockwise starting from pin number 1 at the left towards 8 at the right. The pin number 2 forms the inverting terminal and pin 3 forms the non-inverting input terminal.

The output is available at pin 6 and the terminal 1 and 5, called the null terminals are provided for dc offset null adjustment. The pins 7 and 4 form the positive and negative power supply terminals respectively, shown as  $V^+$  and  $V^-$  in Fig. 3.4. The pin 8 is a *no connection* terminal.

For the mini DIP and 14-pin DIP packages shown in Fig. 3.60(b) and Fig. 3.60(c) respectively, the top pin on the left hand side is identified as pin 1. For the flat pack type shown in Fig. 3.60(d), pin 1 is identified with a dot near pin 1. The remaining pins are counted counterclockwise from pin 1.

### 3.14 POWER SUPPLY CONNECTIONS

The power supply terminals of the IC are connected to two voltage sources of value  $\pm 5$  V to  $\pm 22$  V. The typical values of the power supply are normally  $\pm 15$  V. The common terminal of the positive and negative voltage sources is connected to a common reference point or the ground terminal. The equivalent representation for the power supply connection with the op-amp is shown in Fig. 3.61(a). A single power supply can also be employed as shown in Fig. 3.61(b) through Fig. 3.61(d). It is further discussed in Chapter 4. The resistors  $R$  shown in Fig. 3.61(b) are chosen to be larger than  $10\text{ k}\Omega$ , so that, no appreciable current flows through them. The capacitors can be of any value in the range of  $0.01\text{ }\mu\text{F}$  to  $10\text{ }\mu\text{F}$ . They provide decoupling of the power supply noise.



**Fig. 3.61** Power supply connections

The power supply circuit shown in Fig. 3.61(c) uses Zener diodes to provide symmetrical supply voltages. The value of  $R_s$  is selected so that, it provides enough current for the Zener diode to operate in its avalanche region of operation. A potentiometer is used in Fig. 3.61(d) to achieve the  $V^+$  and  $V^-$  voltages. The diodes  $D_1$  and  $D_2$  provide protection against any accidental reversal of power supply voltages.

## SUMMARY

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- The operational amplifier is commonly called op-amp and was conceived as an integrated circuit in the year 1966. They find applications in audio and radio communication, medical electronics, instrumentation, mathematical computations, integration and differentiation and in many signal processing applications.
- The op-amp is symbolised in the form of a triangle with two input terminals called the *inverting input* terminal (-) and the *non-inverting input* terminal (+) and one output terminal.
- The characteristics of an ideal op-amp are
  - Infinite input resistance,  $R_i = \infty$
  - Zero output resistance,  $R_o = 0$
  - Infinite voltage gain,  $A_v = \infty$
  - Infinite bandwidth,  $BW = \infty$
  - Infinite common-mode rejection ratio,  $CMRR = \infty$
  - Infinite slew rate,  $SR = \infty$
  - Zero offset, i.e when  $v_1 = v_2$ ,  $v_o = 0$
  - Characteristics do not drift with temperature
- A practical op-amp is not ideal. It has an open-loop gain  $A \neq \infty$ , the input resistance  $R_i \neq \infty$ , the output resistance  $R_o \neq 0$  and the output is a voltage controlled voltage source  $A v_{id}$  of equivalent Thevenin's voltage source.
- The op-amp is a three stage circuit consisting of an input stage, a gain stage and an output stage.
- The input stage is a differential amplifier, the gain stage provides additional voltage gain with necessary dc level shifting and the output stage provides current gain and low output impedance
  - FET input stage is normally preferred for achieving very small input bias currents of the order of picoamperes.
  - MOSFETs input stage can be used with additional devices for preventing any damage for the gate oxide due to electrostatic discharges.
  - The gain stage uses Darlington transistor pair.
  - Internal Miller compensation is achieved by a dominant low-frequency pole using the feedback capacitor  $C_1$  connected between the output and input terminals of the gain stage.
  - The final stage of the op-amp is a class AB complementary push-pull output stage.
- The overall voltage gain is the product of individual gains or  $A_v = A_d A_{v2} A_{v3}$ .
- Non-ideal dc characteristics of the op-amp are
  - Input bias current
  - Input offset current
  - Input offset voltage and
  - Thermal drift
- The input of the op-amp is a differential amplifier comprising either BJT or FET with a small value of dc current entering the input called bias currents.
- The input bias current  $I_B$  is given by the average  $I_B = \frac{I_{B1} + I_{B2}}{2}$  and the input offset current  $I_{OS}$  is given by  $I_{OS} = |I_{B1}| - |I_{B2}|$ .

- ❑ Compensating resistor  $R_{comp}$  that is equal to the parallel combination of input resistors  $R_1$  and feedback resistor  $R_f$  as given by  $R_{comp} = R_1 \parallel R_f$ .
- ❑ The manufacturers specify  $I_{OS}$  with output  $V_o$  zero at a temperature of 25°C.
- ❑  $I_{OS}$  is normally less than 25% of  $I_B$  and it is around 200 nA for BJT op-amp and 10pA for FET op-amp.
- ❑ The effect of  $I_{OS}$  on  $V_o$  is given by  $V_o = R_f I_{OS}$ .
- ❑ Since  $I_{OS} \ll I_B$ , the output offset induced by  $I_{OS}$  is smaller than that caused by  $I_B$ .
- ❑ Input offset voltage  $V_{OS}$  is the differential input voltage existing between the inverting and non-inverting input terminals and the process imbalances introduce  $V_{OS}$ .
- ❑ The output offset voltage of the closed-loop inverting and non-inverting configuration of op-amp is  $V_o = \left(1 + \frac{R_f}{R_1}\right) V_{OS}$ . The total output offset voltage  $V_{OT}$  is due to either the input bias current or the input offset voltage, and it can be either positive or negative. It is given by  $V_{OT} = \left(1 + \frac{R_f}{R_1}\right) V_{OS} + R_f I_B$ .
- ❑ The total output offset voltage  $V_{OT}$  when  $R_{comp}$  is connected is given by  $V_{OT} = \left(1 + \frac{R_f}{R_1}\right) V_{OS} + R_f I_{OS}$
- ❑ Offset voltage compensation can be made by
  - Providing offset null terminals
  - Connecting an external offset compensation network
- ❑ Offset null is achieved by connecting a 10 kΩ trimming potentiometer between offset null pins 1 and 5 and the variable terminal is connected to the negative supply pin 4.
- ❑ Nulling procedure involves
  - Connect  $R_{comp}$  and offset null circuit
  - Make all source of signals zero
  - Connect the load to the output, and a dc voltmeter or an oscilloscope across the load and turn the circuit ON
  - Adjust the offset voltage adjustment trimming potentiometer for  $V_o$  to become zero
- ❑ Change in temperature, change in supply voltage and long use pose a great challenge to the values of  $V_{OS}$ ,  $I_B$  and  $I_{OS}$  in the form of drift. The thermal drift is the average rate of change of
  - Input offset voltage per unit change in temperature  $\frac{\Delta V_{OS}}{\Delta T}$  ( $\mu$  V/°C)
  - Input offset current per unit change in temperature  $\frac{\Delta I_{OS}}{\Delta T}$  (pA/°C)
  - Input bias current per unit change in temperature  $\frac{\Delta I_B}{\Delta T}$  (pA/°C)
- ❑ The ac response characteristics are
  - Frequency response
  - Bandwidth
  - Slew rate
- ❑ The gain of the op-amp is not constant and it is a complex number and function of frequency.
- ❑ Two major sources responsible for the capacitive component are
  - The physical characteristics of semiconductor devices, such as BJTs and FETs containing junction capacitors
  - The construction of the op-amp on a substrate introduces parasitic or stray capacitances
- ❑ The voltage transfer function for op-amp with one corner frequency is  $A = \frac{A_0}{1 + j(f/f_1)}$ .

- The transfer function of an op-amp with three break frequencies is given by

$$A = \frac{A_0}{\left(1 + j\frac{f}{f_1}\right)\left(1 + j\frac{f}{f_2}\right)\left(1 + j\frac{f}{f_3}\right)} \quad \text{where } 0 < f_1 < f_2 < f_3.$$

- As frequency of operation increases, the cascading effect of RC pairs introduces roll-off rate at  $-20\text{dB/decade}$  successively at each of the corner frequencies.
- The frequency response plot of the data sheet of an op-amp shows the magnitude of gain Vs frequency. They normally give
  - The plot of open-loop gain  $A$  Vs frequency, with the point  $f_{unity}$  indicating the point where  $A = 1$
- The transient response time (unity gain) is typically  $0.25\text{ }\mu\text{s}$  and  $0.8\text{ ms}$  at maximum for a 741 op-amp.
- The bandwidth  $BW$  can be determined using the relation,  $BW = \frac{0.35}{\text{Rise time}}$ .
- The product of the open-loop gain  $A$  and the frequency of operation  $f$  gives the bandwidth  $BW = A \times f$ .
- The product of closed-loop gain  $A_v$  and closed-loop bandwidth  $BW_{CL}$  is same as the product of open-loop gain and open-loop bandwidth or  $A_v \times BW_{CL} = A \times BW_{OL}$ .
- Two types of compensation techniques used in practice are
  - External frequency compensation methods, which are classified as
    - Dominant-Pole compensation
    - Pole-Zero (lag) compensation
    - Miller effect compensation
  - Internal frequency compensation
- The compensated transfer function  $A'$  after dominant-pole compensation is given by

$$A' = \frac{A_0}{\left(1 + j\frac{f}{f_d}\right)\left(1 + j\frac{f}{f_1}\right)\left(1 + j\frac{f}{f_2}\right)\left(1 + j\frac{f}{f_3}\right)} \quad \text{with } f_d < f_1 < f_2 < f_3$$

- The main disadvantage of dominant-pole compensation technique is the reduced bandwidth.
- The advantage of dominant-pole compensation technique is the improved noise immunity of the system.
- The transfer function of the pole-zero compensation network is given by

$$A' = \frac{A_0}{\left(1 + j\frac{f}{f_0}\right)\left(1 + j\frac{f}{f_2}\right)\left(1 + j\frac{f}{f_3}\right)} \quad \text{with } f_0 < f_2 < f_3$$

- The advantage of the pole-zero compensation method is the improved bandwidth at the cost of additional external components.
- Internally compensated op-amps are called compensated op-amps and they are stable without any external compensation methods.
- LM741, LM107 and LM112 from National Semi-Conductor, MC1558 from Motorola and  $\mu\text{A} 741$  from Fairchild are internally compensated op-amps.
- Slew rate limits the bandwidth for large signals and it is defined as the maximum rate of change of output voltage specified in units of  $\text{V}/\mu\text{s}$ .
- 741 has a maximum slew rate of  $0.5\text{ V}/\mu\text{s}$ .
- Any unwanted signal is called noise and it is random in nature.
- Noise can be Internal or self-induced, and External or man-made.

- ❑ The common types of noise associated with op-amps are thermal noise, short noise,  $1/f$  noise or flicker noise, and burst noise or popcorn noise. The *rms* noise voltage at the op-amp output is  $v_{no} = k_n v_{ni}$  where  $k_n$  is the noise gain value of op-amp. The noise voltage gain of non-inverting amplifier is given by

$$k_n = 1 + \frac{R_f}{R_i}.$$

- ❑ The three open-loop configurations of op-amp are differential amplifier, inverting amplifier and non-inverting amplifier
  - The output voltage of a differential amplifier is  $V_o = A(V_{i1} - V_{i2})$
  - The input of an inverting amplifier is amplified by the open-loop gain  $A$  and it is phase-shifted by  $180^\circ$  at the output or  $V_o = -AV_i$
  - The input of a non-inverting amplifier is amplified by the open-loop gain  $A$  and the output is in-phase with the input, or  $V_o = AV_i$
- ❑ The four types of feedback configurations are voltage-series, voltage shunt, current series and current shunt.
- ❑ The most commonly employed configurations are the voltage-series, or the non-inverting amplifier circuits, and voltage-shunt feedback, or the inverting amplifier types.
- ❑ The op-amp can be effectively utilised in linear applications by the use of a feedback from the output to the input. If the signal feedback is out-of-phase by  $180^\circ$  to the input, then it is referred as negative or degenerative feedback. If the feedback signal is in-phase, then it is called as positive or regenerative feedback.
- ❑ A virtual ground is the ground which acts like a ground without having any physical connection to ground.
- ❑ The closed-loop gain of a non-inverting amplifier is always greater than unity and it depends on the ratio of the feedback resistors. If precision resistors are used in the feedback network, a precise value of closed-loop gain are achieved. The closed-loop gain does not drift with temperature changes or op-amp replacements.
- ❑ Peaking amplifiers amplify signals of a particular frequency. However, the frequency under consideration has to be less the UGB of the op-amp.
- ❑ Capacitor-coupled operational amplifier circuits are designed for ac applications. The capacitors are allowed to interrupt the bias current paths to the op-amp input terminals with the use of additional bias resistors. These coupling capacitors must be selected based on the desired lower cutoff frequency ( $f_l$ ). The chapter explains some ac amplifier configurations using op-amp.
- ❑ The differential amplifier can be constructed using a single op-amp with constant or variable gain in closed-loop configuration. Though it is symmetric, the mismatch between the circuit components makes the output non-zero with the same voltage applied at both the inputs.
- ❑ The gain of the differential amplifier using two op-amps is high. The input resistance of such a circuit also increases.
- ❑ The advantage of this circuit is the high input impedances for the two input signals. The limitation is the input loading which results in reduced amplification.
- ❑ Higher the value of CMRR for the differential amplifier, better is the op-amp.
- ❑ Some 741 op-amps are LM741 from National Semiconductor, MC1741 from Motorola, SN52741 from TI, N5741 from Signetics and CA3741 from RCA.
- ❑ IC 741 is a widely used all-bipolar general purpose op-amp, typical voltage gain is in the range of 200,000, unity gain-bandwidth value is 1 MHz, has an input bias current of 80 nA, has an open-loop gain of 200,000 and a bandwidth of about 5 Hz and the product of its open-loop gain and bandwidth is  $A \times BW_{OL} = 200,000 \times 5 = 1 \text{ MHz}$ .
- ❑ The sample data from the datasheet of IC  $\mu\text{A}741$  is presented.

## REVIEW QUESTIONS

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1. What is an op-amp?
2. What are the characteristics of an ideal op-amp?
3. An ideal op-amp has infinite input resistance and zero gain (True / False).
4. Mention the characteristics of a practical op-amp.
5. What are the non-ideal dc characteristics of an op-amp?
6. Compare the ideal and practical characteristics of an op-amp.
7. Draw the basic block diagram of a general op-amp and explain the operation of each block.
8. Draw the circuit diagram of a general op-amp, identify the stages in it and explain their function in detail.
9. Draw the internal circuit diagram of the IC 741 operational amplifier and explain the function of each stage.
10. Perform the DC analysis of op-amp 741.
11. Perform the AC analysis of op-amp 741.
12. Calculate the reference current  $I_{REF}$  for Fig. 3.7, assuming  $V_{BE11} = V_{BE12} = 0.65$  V and  $I_{REF} = 0.7$  mA.
13. Calculate the bias current for the output stage of the op-amp shown in Fig. 3.10. Assume  $I_{REF} = 0.7$  mA,  $V_{BE} = 0.65$  V and saturation current for  $Q_{18}$  and  $Q_{19}$  is  $10^{-14}$  A and  $I_{S14}$  and  $I_{S20} = 1.5 \times 10^{-14}$  A. Assume that the base currents are negligibly small.
14. How is Miller compensation achieved in op-amp 741?
15. Elaborate on the short circuit protection facility in IC 741.
16. Comment on the frequency response of IC 741.
17. How do you determine the overall gain of an op-amp?
18. What is zero offset suppression in an op-amp?
19. List the dc and ac characteristics of an op-amp.
20. Lower bias current means higher input impedance: (True / False).
21. Discuss the input offset current and input offset voltage of an operational amplifier.
22. Define offset voltage.
23. Assume for Fig. 3.15(c),  $I_{OS} = 300$  nA and  $R_1 = 1.5$  k $\Omega$  and  $R_f = 150$  k $\Omega$ . Calculate the maximum output offset voltage.
24. Define thermal drift. What are the parameters that cause the thermal drift?
25. An op-amp has the drift specifications as given below:

$$\frac{\Delta I_{OS}}{\Delta T} = 0.4 \text{ nA/}^{\circ}\text{C}$$

$$\frac{\Delta V_{OS}}{\Delta T} = 20 \mu\text{V/}^{\circ}\text{C}$$

and temperature span of variation =  $25^{\circ}\text{C}$  to  $60^{\circ}\text{C}$ .

$$R_f = 2 \text{ M}\Omega$$

$$R_1 = 200 \text{ k}\Omega$$

Assuming that after nulling at  $25^{\circ}\text{C}$ , the output voltage  $V_o = 0$ . At a temperature of  $60^{\circ}\text{C}$ , calculate what would be the maximum change in output voltage due to (a) drift in  $V_{OS}$  and (b) drift in  $I_{OS}$ .

26. The frequency response plot of IC 741C is shown in Fig. 3.21(b). Find the gain that can be used to have a maximally flat response at 100 kHz.
27. Explain the performance of the open-loop gain of an op-amp as a function of frequency.
28. Define (a) bandwidth with feedback and (b) unity gain-bandwidth.
29. Define slew rate and what causes it?
30. How is the slew rate measured?
31. What is meant by the *roll-off* rate?
32. A non-inverting amplifier has a gain of 200 and it is nulled at  $25^{\circ}\text{C}$ . What is the change in output voltage that can be expected at an increased temperature of  $60^{\circ}\text{C}$  for an offset voltage drift of  $0.2$  mV/ $^{\circ}\text{C}$ ?
33. Assume that an op-amp 741 connected as a unity gain inverting amplifier has an input change of 8 V. What is the time taken for the output to change by 8 V?



75. For a non-inverting amplifier using an op-amp, assume  $R_1 = 120 \Omega$  and  $R_f = 5.6 \text{ k}\Omega$ . Calculate the closed-loop voltage gain of the amplifier.
76. Draw the circuit of an inverting amplifier using op-amp and give its important characteristics.
77. Derive the voltage gain and input resistance of an inverting operational amplifier configuration. Assume a non-ideal operational amplifier.
78. Derive for the gain, input resistance and output resistance of an inverting op-amp.
79. Derive for the gain, input resistance and output resistance of a non-inverting op-amp circuit.
80. Explain the differential amplifier circuit using one op-amp with a neat circuit, and explain the parameters.
81. What are the limitations of basic differential amplifier? How can you eliminate them? Briefly outline.
82. Explain the difference amplifier using two op-amps using a neat circuit and derive for the input resistance, output resistance and bandwidth.
83. An IC op-amp 741 is used as an inverting amplifier with a gain of 100. The voltage gain Vs frequency characteristic is flat up to 12 kHz. Find the maximum peak-to-peak input signal that can be fed without causing any distortion to the output.
84. For the practical inverting amplifier circuit shown in Fig. 3.35(a), assume  $R_1 = 470 \Omega$ ,  $R_f = 4.7 \text{ k}\Omega$ ,  $V_i = 2 \text{ V}$ . A load of  $20 \text{ k}\Omega$  is connected to the output terminal. Calculate the input current, output voltage and the load current.
85. For a non-inverting amplifier shown in Fig. 3.39, calculate (a)  $A_v$ , (b)  $V_o$ , (c)  $I_L$  and (d)  $I_o$  assuming  $V_i = 0.5 \text{ V}$ ,  $R_f = 20 \text{ k}\Omega$ ,  $R_1 = 10 \text{ k}\Omega$  and  $R_L = 1 \text{ k}\Omega$ .
86. Draw the circuit of a capacitor-coupled voltage follower circuit using op-amp and explain its operation.
87. Show how to calculate the capacitance values of a capacitor-coupled voltage follower.
88. Explain the circuit of a high input impedance capacitor-coupled voltage follower circuit and explain its operation. Derive for the input impedance.
89. Draw the circuit of a capacitor-coupled non-inverting amplifier, and explain the operation. How do you define its input impedance?
90. Draw the circuit of a capacitor-coupled inverting amplifier, and explain the operation. How do you define its input impedance?
91. Discuss the upper cutoff frequency of an op-amp circuit and explain how the cutoff frequency can be set for inverting, non-inverting and difference amplifier circuits.
92. Draw the circuit of a capacitor-coupled difference amplifier. Explain its operation. How will you calculate the capacitance values?
93. Show how a capacitor-coupled voltage follower circuit be designed to operate with a single polarity power supply.
94. Draw the operation of a capacitor-coupled non-inverting amplifier using an op-amp driven by a single polarity power supply.
95. Draw the operation of a capacitor-coupled inverting amplifier using an op-amp driven by a single polarity power supply.
96. For a given op-amp,  $\text{CMRR} = 10^4$  and differential gain  $A_{dm} = 10^4$ . Determine the common-mode gain  $A_{cm}$  of the op-amp.
97. An op-amp circuit shown in Fig. 3.54(a) has differential gain  $A_d = 5 \times 10^5$ . Determine  $V_o$ . Assume  $R_1 = R_2 = R_3 = 1 \text{ k}\Omega$  and  $R_f = R_L = 10 \text{ k}\Omega$
98. Determine the output voltage of a differential amplifier with gain = 2000 and  $\text{CMRR} = 100$ .
99. For the non-inverting op-amp shown in Fig. 3.37(a) with input resistance  $R_1 = 100 \text{ k}\Omega$  and feedback resistance of  $R_f = 900 \text{ k}\Omega$ , determine the effect on output voltage due to common mode voltage when the input voltage changes by 1V. Assume CMRR is 70 dB.
100. In response to a square wave input, the output of an op-amp changes from  $-3 \text{ V}$  to  $+3 \text{ V}$  over a time interval of  $0.25 \mu\text{s}$ . Determine the slew rate of the op-amp.
101. Refer to Fig. 3.41(a). Given a BJT op-amp, design a capacitor-coupled voltage follower, for a lower cutoff frequency of 100 Hz and a load resistance of  $R_L = 4.7 \text{ k}\Omega$ .
102. Refer to Fig. 3.47. Using the IC LF353 BIFET op-amp, design a high input impedance capacitor-coupled noninverting amplifier for a lower cutoff frequency of 50 Hz. The input and output voltages are to be 20 mV and 2 V respectively, and the minimum load resistance is  $10 \text{ k}\Omega$ .

# Applications of Operational Amplifiers

# 4

## 4.1 INTRODUCTION

The operational amplifier, or op-amp, was originally developed in response to the requirements of analog computer designers. An op-amp is a high gain, direct coupled amplifier. The voltage gain can be controlled by the externally connected feedback components. The op-amp can be used in amplifier and signal processing applications involving dc to several MHz of frequency ranges. The operational amplifier circuits can be designed with various types of active devices. However, IC technology is remarkably successful in offering low-cost, high-performance and versatile op-amps in a monolithic form, and the op-amp became a widely accepted building block of modern signal processing and conditioning circuits.

Since the IC op-amps are inexpensive, versatile and easy to use, they are used for negative feedback amplifier applications, and they also find applications in waveshaping, filtering and solving mathematical operations. Some common applications are discussed in this chapter.

## 4.2 SIGN CHANGER (PHASE INVERTER)

Figure 4.1 shows the basic inverting amplifier configuration using an op-amp with input impedance  $Z_1$  and feedback

impedance  $Z_f$ . Here, the closed-loop voltage gain is  $-\frac{Z_f}{Z_1}$ . If

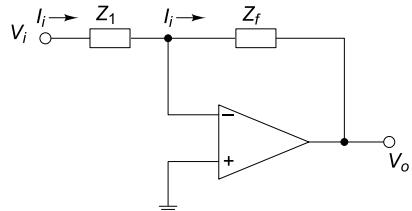
the impedances  $Z_1$  and  $Z_f$  are equal in magnitude and phase, then the closed-loop voltage gain is  $-1$ , and the input signal will undergo a  $180^\circ$  phase shift at the output. Hence, such a circuit is also called *phase inverter*. If two such amplifiers are connected in cascade, then the output from the second stage is the same as the input signal without any change of sign. Hence, the outputs from the two stages are equal in magnitude but opposite in phase and such a system is an excellent paraphase amplifier.

## 4.3 SCALE CHANGER

Referring to Fig. 4.1, if the ratio  $Z_f/Z_1 = k$ , a real constant, then the closed-loop gain is  $-k$ , and the input voltage is multiplied by a factor  $-k$  and the scaled output is available at the output. Usually, in such applications,  $Z_f$  and  $Z_1$  are selected as precision resistors for obtaining precise and scaled value of input voltage.

## 4.4 PHASE SHIFT CIRCUITS

The phase shift circuits produce phase shifts that depend on the frequency and maintain a constant gain. These circuits are also called *constant-delay filters* or *all-pass filters*. The constant delay refers to the



**Fig. 4.1** Inverting op-amp with voltage shunt feedback

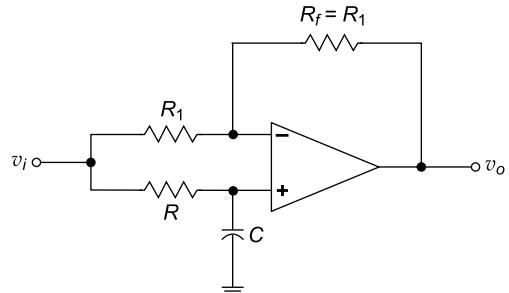
fact that the time difference between input and output remains constant when frequency is changed over a range of operating frequencies. This is called all-pass because normally a constant gain is maintained for all the frequencies within the operating range. The two types of circuits, for lagging phase angles and leading phase angles are discussed below.

Referring to Fig. 4.1, if  $Z_1$  and  $Z_f$  are equal in magnitude and differ in angle, then the op-amp shifts the phase of the sinusoidal input voltage. Any phase shift between  $-180^\circ$  and  $+180^\circ$  can be obtained by varying  $Z_1$  and  $Z_f$ .

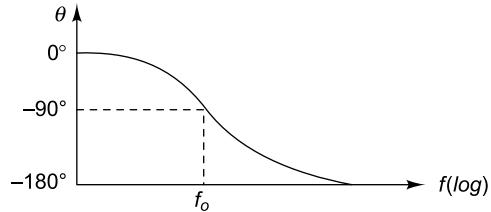
#### 4.4.1 Phase-Lag Circuit

Figure 4.2(a) shows the phase-lag circuit constructed using an op-amp, connected in both inverting and non-inverting modes. To analyse the circuit operation, it is assumed that the input voltage  $v_i$  drives a simple inverting amplifier with input applied at  $(-)$  and  $(+)$  terminals of op-amp. It is also assumed that inverting gain is  $-1$  and non-inverting gain after the low-pass

circuit is  $1 + \frac{R_f}{R_1} = 1 + 1 = 2$ , since  $R_f = R_1$



**Fig. 4.2 (a)** Phase-lag circuit



**Fig. 4.2 (b)** Bode plot for the phase-lag circuit

For the circuit shown in Fig. 4.2(a), it can be written as

$$V_o(j\omega) = -V_i(j\omega) + 2 \frac{1}{1 + j\omega RC} V_i(j\omega) \quad (4.1)$$

Therefore,

$$V_o(j\omega) = V_i(j\omega) \left( -1 + 2 \frac{1}{1 + j\omega RC} \right) = V_i(j\omega) \left( \frac{1 - j\omega RC}{1 + j\omega RC} \right)$$

The relationship between output and input can be expressed by

$$\frac{V_o(j\omega)}{V_i(j\omega)} = \left( \frac{1 - j\omega RC}{1 + j\omega RC} \right) \quad (4.2)$$

The relationship is complex as defined by Eq. (4.2), and it shows that it has both magnitude and phase. Since the numerator and denominator are complex conjugates, their magnitudes are identical and the overall phase angle is equal to the angle of numerator minus the angle of the denominator. The phase angle is then given by

$$\theta = -\tan^{-1}(\omega RC) - \tan^{-1}(\omega RC) = -2 \tan^{-1}(\omega RC) \quad (4.3)$$

Here, when  $\omega = 0$ , the phase angle approaches zero. When  $\omega = \infty$ , the phase angle approaches  $-180^\circ$ . Then Eq. (4.3) can be written as

$$\theta = -2\tan^{-1}(f/f_o) \quad (4.4)$$

where the frequency  $f_o$  is given by

$$f_o = \frac{1}{2\pi RC} \quad (4.5)$$

Here, when  $f = f_o$  in Eq. (4.4), the phase angle  $\theta = -90^\circ$ . The Bode plot for the phase-lag circuit is shown in Fig. 4.2(b).

### Example 4.1

Determine the phase angle and the time delay for the circuit shown in Fig. 4.2(a) for a frequency of 2 kHz, assuming  $R_1 = 20 \text{ k}\Omega$ ,  $R = 39 \text{ k}\Omega$ ,  $R_f = R_1$  and  $C = 1 \text{nF}$

**Solution** The circuit is a phase-lag network.

$$\text{Therefore, } f_o = \frac{1}{2\pi RC} = \frac{1}{2 \times \pi \times 39 \times 10^3 \times 1 \times 10^{-9}} = 4081 \text{ Hz.}$$

The phase angle for frequency of 2 kHz is given by

$$\theta = -2\tan^{-1}\left(\frac{2 \times 10^3}{4081}\right) = -52.2^\circ$$

The phase angle is directly proportional to delay, and  $360^\circ$  of delay corresponds to one period.

$$\text{Therefore, } \frac{\theta}{360^\circ} = \frac{t_d}{T} \text{ which gives}$$

$$t_d = \frac{1}{f} \frac{\theta}{360^\circ} = \frac{1}{2 \times 10^3} \frac{-52.2}{360^\circ} = 72.5 \mu\text{s.}$$

### 4.4.2 Phase-Lead Circuit

The phase-lead circuit is shown in Fig. 4.3(a) in which the  $RC$  circuit forms a high-pass network. The output voltage is derived and expressed by

$$V_o(j\omega) = -V_i(j\omega) + 2\left(\frac{j\omega RC}{1 + j\omega RC}\right)V_i(j\omega)$$

$$\text{Therefore, } \frac{V_o(j\omega)}{V_i(j\omega)} = \frac{-1 + j\omega RC}{1 + j\omega RC} \quad (4.6)$$

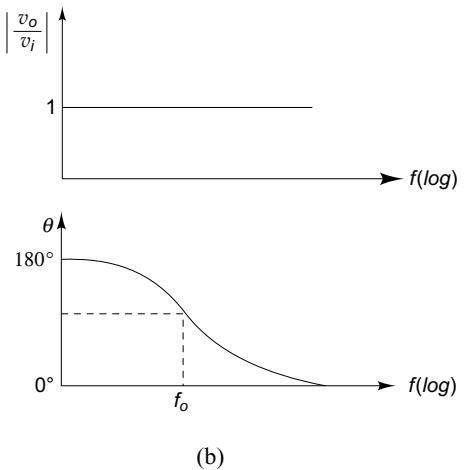
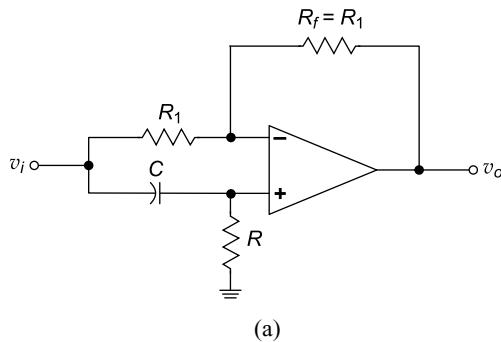
Equation (4.6) signifies that the ratio of magnitude is constant and the phase is obtained as shown in Eq. (4.3). It is to be noted that the numerator has a negative real part and overall phase is given by

$$\theta = 180^\circ - \tan^{-1}(\omega RC) - \tan^{-1}(\omega RC) = 180^\circ - 2\tan^{-1}(\omega RC) \quad (4.7)$$

When the frequency approaches zero, the phase angle approaches  $180^\circ$ . As the frequency is increased, the leading phase decreases and it finally approaches zero at high frequencies. Hence, Eq. (4.7) can be written as

$$\theta = 180^\circ - 2\tan^{-1}(f/f_o) \quad (4.8)$$

where  $f_o = \frac{1}{2\pi RC}$ . Figure 4.3(b) shows the Bode plot for the phase-lead circuit of Fig. 4.3(a).



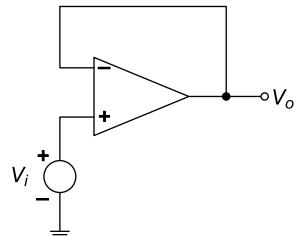
**Fig. 4.3** (a) Phase-lead circuit (b) Bode plot for the phase-lead circuit

## 4.5 VOLTAGE FOLLOWER

If  $R_1 = \infty$  and  $R_f = 0$  in the non-inverting amplifier configuration discussed in Chap. 3, then the amplifier acts as a unity-gain amplifier or voltage follower as shown in Fig. 4.4. That is,

$$A_v = 1 + \frac{R_f}{R_1} \text{ or } \frac{R_f}{R_1} = A_v - 1$$

Since  $\frac{R_f}{R_1} = 0$ , we have  $A_v = 1$ .



**Fig. 4.4** Voltage follower

The circuit consists of an op-amp and a wire connecting the output voltage to the input, i.e. the output voltage is equal to the input voltage, both in magnitude and phase. In other words,  $V_o = V_i$ .

Since the output voltage of this circuit follows the input voltage, the circuit is called *voltage follower*. It is also referred to as a source follower, buffer amplifier, isolation amplifier or unity gain amplifier in practice. It offers very high input impedance of the order of  $M\Omega$  and very low output impedance. Therefore, this circuit draws negligible current from the source. Thus, the voltage follower can be used as a buffer between a high impedance source and a low impedance load for *impedance matching* applications.

### Example 4.2

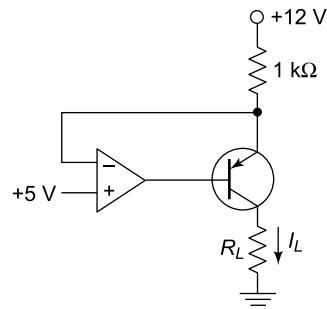
Determine the output current  $I_L$  for the circuit shown in Fig. 4.5.

**Solution** The op-amp acts as a voltage follower with  $+5V$  at the emitter of the transistor with  $V_{EE} = +12V$ .

When the transistor is ON, the current through  $1\ k\Omega$  resistor

$$\text{is } \frac{7V}{1 \times 10^3} = 7 \text{ mA.}$$

Neglecting the base current, the current through  $R_L$  is  $I_L = 7 \text{ mA}$ .



**Fig. 4.5**

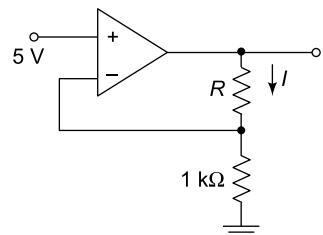
**Example 4.3**

Determine the current  $I$  in the circuit shown in Fig. 4.6.

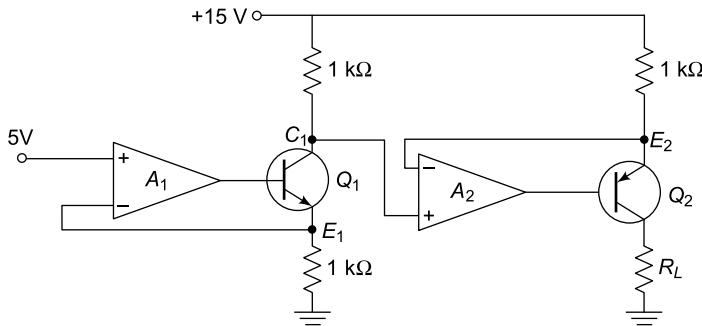
**Solution** The op-amp with 5V at the non-inverting input drops

$$5 \text{ V across the } 1 \text{ k}\Omega \text{ resistance with a resulting current of } \frac{5\text{V}}{1\text{k}\Omega} = 5 \text{ mA.}$$

Hence, the current  $I$  through  $R$  is 5 mA, since no current enters the inverting input terminal of op-amp.

**Fig. 4.6****Example 4.4**

Determine the current through  $R_L$  in the circuit shown in Fig. 4.7.

**Fig. 4.7**

**Solution** With 5 V at non-inverting terminal of op-amp  $A_1$ , the voltage at  $E_1$  across  $1 \text{ k}\Omega$  resistor is 5 V. Assuming negligible  $V_{CE}$  drop across  $Q_1$ , the voltage available at  $C_1$  is 5 V, which makes the voltage at  $E_2$  node also to be 5 V. Here, op-amps  $A_1$  and  $A_2$  act as voltage followers.

Hence, the current through  $1 \text{ k}\Omega$  resistor connected at  $E_2$  is

$$\frac{V_{CC} - V_{E2}}{R_{E2}} = \frac{15 - 5}{1 \times 10^3} = 10 \text{ mA}$$

Assuming that the base current is negligible, the current through  $R_L$  is 10 mA.

## 4.6 VOLTAGE-CONTROLLED VOLTAGE SOURCE

An ideal voltage-controlled voltage source is the one, whose (i) output voltage  $V_o$  equals a fixed constant  $k$  times the value of input voltage, i.e.  $V_o = k V_i$  and (ii) output voltage  $V_o$  is independent of the current drawn from it.

The inverting and non-inverting amplifiers of op-amp discussed in Chap.3 fall under the category of voltage-controlled voltage source (VCVS).

## 4.7 CURRENT SOURCES

Sometimes it is required to source a fixed current through a load. Figure 4.8(a) shows one way to do it. Since the error voltage is negligibly small, essentially all of  $V_i$  appears across  $R$  producing a current of

$$I_i = \frac{V_i}{R}$$

All this current must flow through the load, because negligible current enters into the op-amp inverting input. Depending on the application, the load may be a resistor, capacitor, inductor, or a combination of them.

Figure 4.8(b) shows an inverting amplifier used to source current through a load. Because of the virtual ground at the inverting terminal, the input current  $I_i$  can flow only through the load resistor, which is given by

$$I_o = \frac{V_i}{R}$$

This allows to set up a precise value of  $I_o$ . Again, the load may be a resistor, capacitor, inductor, or a combination of them.

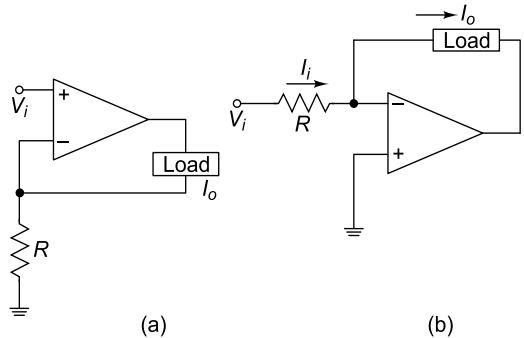
## 4.8 INVERTING CURRENT AMPLIFIER

The basic circuit configuration of an inverting current amplifier is shown in Fig. 4.9. The input impedance of the circuit is zero due to the parallel negative feedback connection at the inverting input terminal of the op-amp. Therefore, the input node  $a$  is at virtual ground. This makes the current flowing into the op-amp negligible and therefore all the input current flows through the input resistance  $R_1$  to the node  $b$ . Hence the resistors  $R_1$  and  $R_f$  are in parallel since they share the node  $b$  and the ground, and this makes the voltages  $V_{R_1}$  and  $V_{R_f}$  to be equal. This effectively means that a current flows through  $R_f$  from ground to node  $b$ . These two currents combine to form the load current through the load resistor  $R_L$ . In this manner, the current gain is achieved. When the current  $I_{R_f}$  is made larger relative to input current  $I_i$ , the current gain increases. The current gain can be expressed by

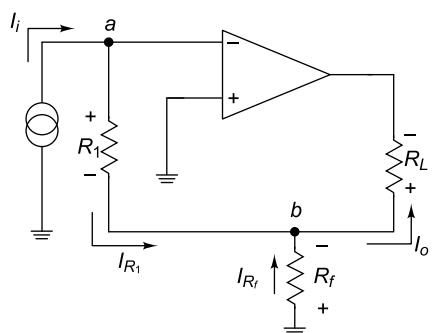
$$A_i = \frac{I_o}{I_i} = \frac{I_{R_f} + I_{R_1}}{I_i} \quad (4.9)$$

and

$$I_{R_1} = I_i, \quad I_{R_f} = \frac{V_{R_f}}{R_f} \quad (4.10)$$



**Fig. 4.8** Op-amp current sources  
(a) non-inverting and  
(b) Inverting



**Fig. 4.9** Inverting current amplifier

Since  $V_{R_f}$  and  $V_{R_1}$  are equal,

$$I_{R_f} = \frac{V_{R_f}}{R_f} = \frac{I_i R_1}{R_f} \quad (4.11)$$

Substituting Eq. (4.11) for  $I_{R_f}$  in Eq. (4.9) and using Eq. (4.10), we get

$$I_o = I_i + \frac{I_i R_1}{R_f} = I_i \left( 1 + \frac{R_1}{R_f} \right)$$

$$\text{Therefore, the current gain } A_i = \frac{I_o}{I_i} = 1 + \frac{R_1}{R_f} \quad (4.12)$$

Equation (4.12) identifies that the current gain is a function of the two feedback resistors and it is very similar to the voltage gain equation of the non-inverting voltage amplifier.

### Example 4.5

Assume that  $R_1 = 22 \text{ k}\Omega$ ,  $R_f = 1 \text{ k}\Omega$ ,  $R_L = 10 \text{ k}\Omega$  and  $I_i = 10 \mu\text{A}$  for the circuit shown in Fig. 4.9. Determine the load gain.

#### Solution

$$A_i = 1 + \frac{R_1}{R_f} = 1 + \frac{22 \times 10^3}{1 \times 10^3} = 23$$

Therefore,  $I_o = A_i I_i = 23 \times 10 \mu\text{A} = 230 \mu\text{A}$ .

The maximum voltage at the output of op-amp is

$$\begin{aligned} V_{\max} &= I_o \times R_L + I_i \times R_1 = 230 \times 10^{-6} \times 10 \times 10^3 + 10 \times 10^{-6} \times 22 \times 10^3 \\ &= 2.3 + 0.22 = 2.52 \text{ V} \end{aligned}$$

Hence, it is verified that the output clipping does not occur.

## 4.9 CURRENT-CONTROLLED CURRENT SOURCE (CCCS)

An ideal current-controlled current source is the one which supplies (i) a current  $I_L$  that equals a fixed constant  $k$  times the value of an independent controlling or input current. In other words,  $I_L = kI_i$  and (ii) a current  $I_L$  that is independent of the load to which the current is supplied. The constant  $k$  is dimensionless.

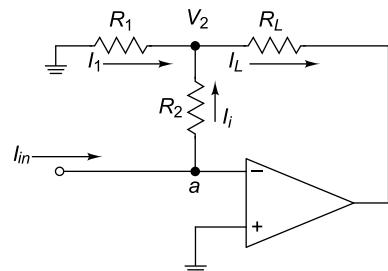
Figure 4.10 shows the current-controlled current source circuit with floating load since no current can flow into the inverting input terminal of op-amp,  $I_{in} = I_i$

The inverting input terminal node  $a$  is a virtual ground and hence voltage  $V_2$  is given by

$$V_2 = -I_i R_2$$

The current  $I_1$  in  $R_1$  is,

$$I_1 = \frac{0 - V_2}{R_1} = \frac{I_i \times R_2}{R_1}$$



**Fig. 4.10** Current-controlled current source with floating load

Using Kirchhoff's Current Law at node  $V_2$ ,

$$\begin{aligned} I_L &= I_1 + I_i = \frac{I_i \times R_2}{R_1} + I_i \\ &= \left( \frac{R_2}{R_1} + 1 \right) I_i \end{aligned} \quad (4.13)$$

Equation (4.13) shows that the load current  $I_L$  is independent of  $R_L$ . This circuit is preferred where floating load such as the one shown in Fig. 4.10 is to be driven.

## 4.10 VOLTAGE TO CURRENT CONVERTER (TRANSCONDUCTANCE AMPLIFIER)

An ideal voltage-controlled current source (VCCS) is the one that supplies (i) a current  $I_o$  that equals a fixed constant  $k$  times the value of an independent, controlling voltage  $V_i$ , or in other words,  $I_o = kV_i$  and (ii) a current which is independent of the load that it drives.

For converting a voltage signal to a proportional output current, there are two converting circuits, namely (i) voltage to current with floating load, and (ii) voltage to current with grounded load. The voltage to current converter accepts an input voltage  $V_i$  and gives an output current  $I_L$ .

The voltage to current converter with floating load is shown in Fig. 4.11(a). The voltage at node  $a$  is  $V_a$ . Therefore, as  $I_B = 0$ ,  $V_i = I_L R_1$ , i.e.  $I_L = V_i / R_1$ , and the input voltage is converted into an output current  $I_L$ . Since the same current flows through the signal source and load, the signal source provides this load current.

The voltage to current converter with grounded load is shown in Fig. 4.11(b). Here, the voltage at node  $a$  is  $V_a$ . Applying KCL at node  $a$ , and assuming  $R = R_1 = R_f$ , we get

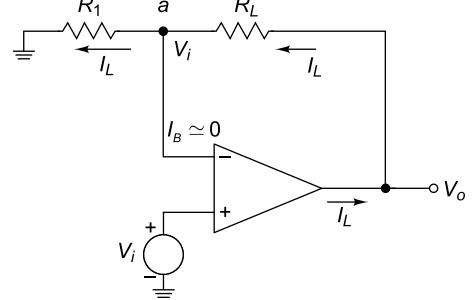
$$\begin{aligned} I_1 + I_2 &= I_L \\ (V_i - V_a)/R + (V_o - V_a)/R &= I_L \\ V_i + V_o - 2V_a &= I_L R \\ V_a &= (V_i + V_o - I_L R)/2 \end{aligned}$$

The gain of this non-inverting op-amp circuit is  $1 + R/R_f = 2$ . Therefore,

$$\begin{aligned} V_o &= 2V_a = V_i + V_o - I_L R \\ V_i &= I_L R \\ I_L &= V_i/R \end{aligned} \quad (4.14)$$

Hence, the load current is determined by the ratio of  $V_i$  and  $R$ . This circuit can also be called *voltage to current transducer*, since

$$\text{Transconductance } (g_m) = \frac{I_L}{V_i} = \frac{1}{R}$$



**Fig. 4.11 (a)** Voltage to current converter with floating load

Therefore, the transconductance of the circuit is determined by the feedback resistor  $R_f = R$ . The circuits shown in Fig. 4.11(a) and (b) are also called voltage-controlled current source (VCCS), since the load current is given by

$$I_L = \frac{V_i}{R} = V_i g_m \quad (4.15)$$

where  $g_m$  is the transconductance in *Siemens*. The load resistance  $R_L$  does not appear in Eq. (4.15), and hence the load current  $I_L$  is independent of the load resistance  $R_L$ . The direction of the current through the load is controlled by the polarity of  $V_i$ . Figure 4.11(a) shows the floating load, that is so called, because neither side of  $R_L$  is grounded. This circuit is preferred in applications, where the load cannot have the same ground reference as the input controlling voltage  $V_i$ .

As the input impedance of this circuit is very high, it draws negligible current from the source. This converter is used in low voltage voltmeter, LED and Zener testers.

Caution is to be exercised in the selection of  $R_f$  and  $R_L$  due to the following reasons:

- (i) When  $R_f$  and  $R_L$  are very small, the op-amp output current may be too high and the op-amp may be pushed into saturation.
- (ii) When  $R_f$  and  $R_L$  are made very large, the output voltage may exceed the power supply voltage since the product of the value of two resistors and  $I_L$  make the output voltage.

### Example 4.6

Assume that  $R_f = 10 \text{ k}\Omega$ ,  $R_L = 2 \text{ k}\Omega$  and  $V_i = 0.5 \text{ V}$  for the circuit shown in Fig. 4.11(a). Determine the load current.

**Solution** The load current is  $I_L = \frac{V_i}{R_f} = \frac{0.5}{10 \times 10^3} = 50 \mu\text{A}$

The op-amp will not be overloaded with the output current of  $50 \mu\text{A}$ , since any commonly available op-amp such as 741 can produce an output current of  $20 \text{ mA}$ .

To verify if the output voltage clipping would occur,

$V_{\max} = (R_f + R_L) I_L = (10 \times 10^3 + 2 \times 10^3) \times 50 \times 10^{-6} = 0.6 \text{ V}$ , which is well below the clipping or saturation level of the op-amp.

### Example 4.7

Given a voltage-to-current converter as shown in Fig. 4.12, find the transconductance,  $g_m$ , of the circuit, and calculate the maximum load current  $I_L$  that could be drawn. Check whether overload can happen and calculate the output voltage  $V_o$ .

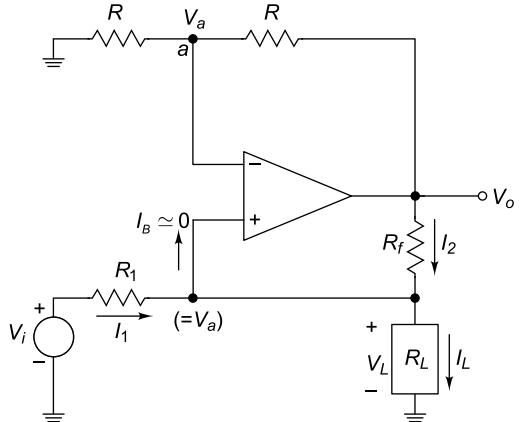


Fig. 4.11 (b) Voltage to current converter with grounded load

From Fig. 4.12,

$$I_L = I_{R_1}$$

However,

$$I_{R_1} = \frac{V_i}{R_1}$$

Therefore,

$$I_L = \frac{V_i}{R_1}$$

i.e.,

$$\frac{I_L}{V_i} = \frac{1}{R_1}$$

Transconductance is given by

$$g_m = \frac{I_L}{V_i} = \frac{1}{R_1}$$

Therefore,

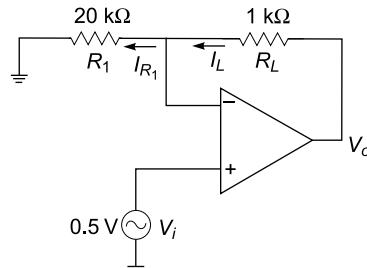
$$g_m = \frac{1}{20 \times 10^3} = 50 \mu \text{S}$$

$$\text{Load current } I_L = g_m \times V_i = 50 \times 0.5 = 25 \mu \text{A}$$

Since the op-amp can operate with a current (max) of 25 mA, it will not be overloaded.

$$\text{Then the output voltage, } V_o = (R_L + R_1) I_L = (20 + 10) \times 10^3 \times 25 \times 10^{-6} = 0.75 \text{ V.}$$

This shows that the output voltage also is well below the saturation level of the op-amp.

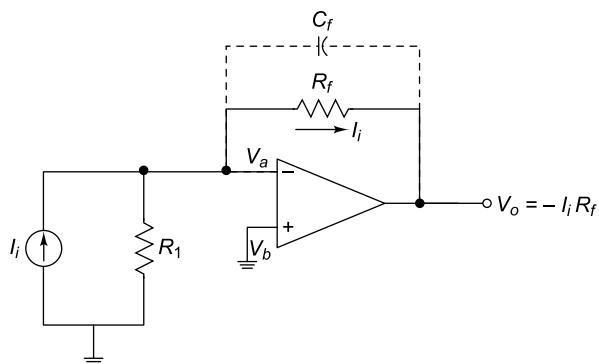


**Fig. 4.12**

## 4.11 CURRENT TO VOLTAGE CONVERTER (CURRENT-CONTROLLED VOLTAGE SOURCES)

A current to voltage converter or an ideal current-controlled voltage source, also called *transresistance amplifier* is the one, whose (i) output voltage is equal to a constant  $k$  times the magnitude of an independent input current  $I_i$  or in other words,  $V_o = kI_i$  and (ii) output voltage is independent of the load connected to it. The constant  $k$  has the unit of ohms.

These CCVS or current to voltage converters are required, since it is generally easier to measure voltages. For example, an output current proportional to an incident light energy is obtained from photo devices such as a photocell and photo diode. This output current from the photo-devices can be converted to voltage by using this current to voltage converter shown in Fig. 4.13. Due to the virtual ground,  $V_b = V_a = 0$ , the current through  $R_1$  is zero and  $I_i$  flows through the feedback resistor  $R_f$ . Thus  $V_a = -I_i R_f$ . In order to reduce the high frequency and possible oscillations, a capacitor  $C_f$  is connected across  $R_f$ .

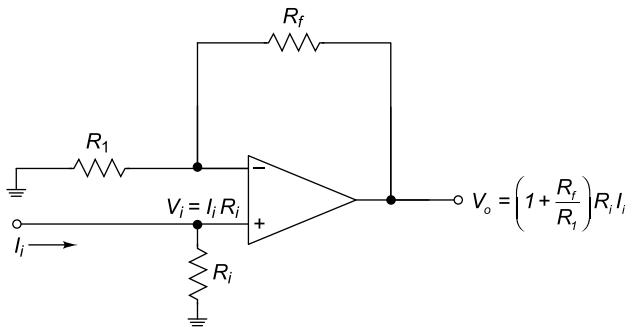


**Fig. 4.13** Inverting current to voltage converter

Figure 4.14 shows a non-inverting current to voltage converter circuit. The input current  $I_i$  has a return path to ground. The voltage at the non-inverting input is given by  $V_i = I_i R_i$ .

Then the voltage  $V_o$  at the output is given by

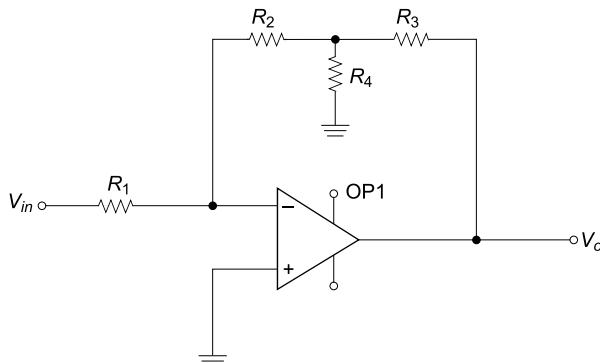
$$V_o = \left(1 + \frac{R_f}{R_1}\right) V_i = \left(1 + \frac{R_f}{R_1}\right) I_i R_i \quad (4.16)$$



**Fig. 4.14** Non-inverting current to voltage converter

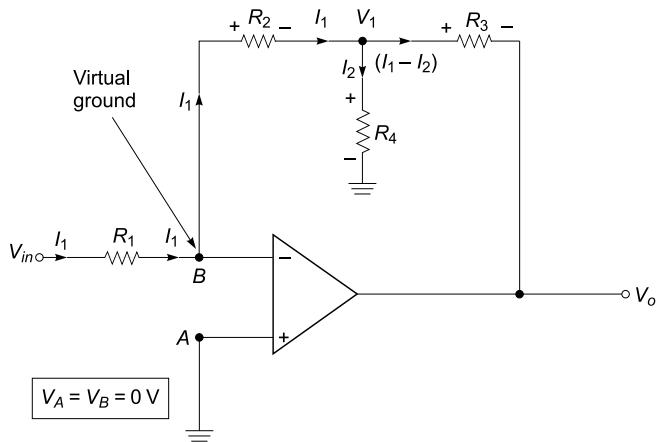
### Example 4.8

For the circuit shown in Fig. 4.15(a), find output voltage,  $V_o$ .



**Fig. 4.15(a)**

**Solution** Assuming that the op-amp is ideal, input current of op-amp is zero while point B is at virtual ground as shown in Fig. 4.15(b).



**Fig. 4.15(b)**

$$\text{Therefore, } I_1 = \frac{V_{in} - V_B}{R_1} = \frac{V_{in}}{R_1}, I_1 = \frac{V_B - V_1}{R_2} = \frac{-V_1}{R_2}$$

Equating the above equations, we get

$$\frac{V_{in}}{R_1} = -\frac{V_1}{R_2} \quad \text{i.e.} \quad V_1 = \frac{-R_2}{R_1} V_{in} \quad (1)$$

From Fig. 4.15(b), we find that

$$V_1 = I_2 R_4 \quad \text{and} \quad I_1 - I_2 = \frac{V_1 - V_o}{R_3} \quad (2)$$

$$\text{Then, } I_2 = \frac{V_1}{R_4} \quad (3)$$

Using Eqn (2) above, we get

$$\frac{V_{in}}{R_1} - \frac{V_1}{R_4} = \frac{V_1}{R_3} - \frac{V_o}{R_3}$$

$$\frac{V_{in}}{R_1} - V_1 \left[ \frac{1}{R_3} + \frac{1}{R_4} \right] = -\frac{V_o}{R_3}$$

Using Eq. (1), we get

$$\frac{V_{in}}{R_1} + \frac{R_2}{R_1} V_{in} \left[ \frac{R_3 + R_4}{R_3 R_4} \right] = -\frac{V_o}{R_3}$$

$$\frac{V_{in}}{R_1} \left[ 1 + \frac{R_2(R_3 + R_4)}{R_3 R_4} \right] = -\frac{V_o}{R_3}$$

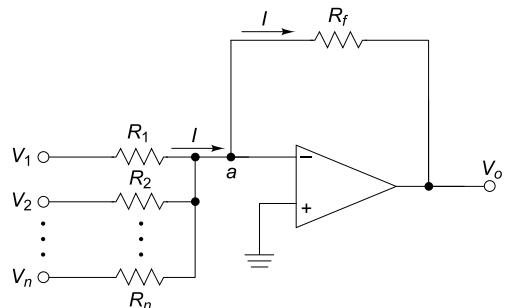
$$\frac{V_{in}}{R_1 R_3 R_4} [R_3 R_4 + R_2(R_3 + R_4)] = -\frac{V_o}{R_3}$$

$$\text{Therefore, } V_o = -\frac{1}{R_1 R_4} [R_3 R_4 + R_2 R_3 + R_2 R_4] V_{in}$$

## 4.12 ADDER OR SUMMING AMPLIFIER

The adder, also called summing amplifier, is shown in Fig. 4.16. The output of this arrangement is the linear addition of a number of input signals. Since a virtual ground exists at the inverting input of op-amp at the node  $a$ ,

$$I = \frac{V_1}{R_1} + \frac{V_2}{R_2} + \dots + \frac{V_n}{R_n}$$



**Fig. 4.16** Summing amplifier

and

$$V_o = -R_f I = - \left[ V_1 \frac{R_f}{R_1} + V_2 \frac{R_f}{R_2} + \dots + V_n \frac{R_f}{R_n} \right] \quad (4.17)$$

If

$$R_1 = R_2 = \dots = R_n = R, \text{ then}$$

$$V_o = -\frac{R_f}{R} (V_1 + V_2 + \dots + V_n) \quad (4.18)$$

Therefore, the output is proportional to the sum of the individual inputs. From Eq. (4.17), it is clear that the output signal is the sum of all the inputs multiplied by their associated gains. It can then be expressed as

$$V_o = V_1 A_{V1} + V_2 A_{V2} + V_3 A_{V3} + \dots + V_n A_{Vn}$$

where  $A_{V1}, A_{V2} \dots A_{Vn}$  are the individual gains of the inputs. The summing amplifier may have equal gain for each of the inputs, and then it is referred to as an *equal-weighted configuration*.

The advantage of this method of summation of signals is that a very large number of inputs can be added together, thus requiring only one additional resistor for each additional input with individual gain controls.

Since the input to the op-amp is at virtual ground, the inverting input summing node is an ideal current summing node. Each input signal is made to drive its own input resistance. Hence, there is very little mutual effect among the neighbouring inputs.

A typical application of the summing amplifier circuit is in the broadcast and recording applications. A typical music recording will require a multitude of microphones, with individual volume controls needed for proper balancing of all sound signals while combining them together. The ideal summing amplifier will thus present the individual input signals with an isolated load and not influenced by any other channel signals. It can be noted that a master volume control can also be produced by connecting a potentiometer as the feedback resistor,  $R_f$ .

The summing amplifier can also be used as a level shifter for any ac signal. When used as a two-input summing amplifier, with one input connected to the ac input signal and the second input connected to the desired offset dc signal, the output is the ac signal offset by the dc signal magnitude. These are the typical applications which are limited only by the ingenuity of the circuit designer.

Theoretically, individual gain controls may be produced by making the input resistors variable, or by making the feedback resistor  $R_f$  variable with the use of potentiometer. However, for ac signals, the summation is not so straight forward, since ac signals of different frequency and phase relationships do not add correctly. Then, an RMS calculation can be made for finding the effective value.

A *level-shifter* circuit can also be realised by use of a two-input summing circuit, in which, one input can be the ac signal, and the second input can be the dc value by whose value the ac signal is to be shifted. The dc value acts as the *offset* for the ac signal.

### Example 4.9

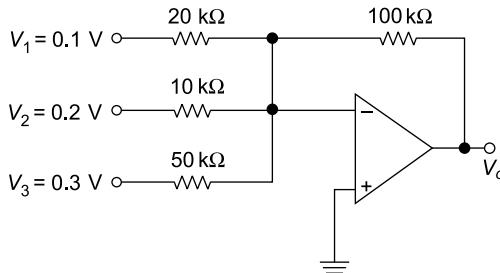
The summing amplifier shown in Fig. 4.16 has the following inputs,  $V_1 = +2 \text{ V}$ ,  $V_2 = +3 \text{ V}$ ,  $V_3 = +4 \text{ V}$  and  $R_f = R_1 = R_2 = R_3 = R = 1 \text{ k}\Omega$ , and the supply voltages are  $\pm 15 \text{ V}$ . Determine the output voltage. Assume that the op-amp is initially nulled.

**Solution** The output voltage is given by

$$V_o = -\frac{R_f}{R} (V_1 + V_2 + \dots + V_n) = -\frac{1 \times 10^3}{1 \times 10^3} (2 + 3 + 4) = -9 \text{ V}$$

**Example 4.10**

Determine the  $V_0$  for the circuit shown in Fig. 4.17.

**Fig. 4.17****Solution**

$$\begin{aligned} V_0 &= - \left[ \frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3 \right] \\ &= - \left[ \frac{100 \times 10^3}{20 \times 10^3} \times 0.1 + \frac{100 \times 10^3}{10 \times 10^3} \times 0.2 + \frac{100 \times 10^3}{50 \times 10^3} \times 0.3 \right] \\ &= - [0.5 + 2 + 0.6] = - 3.1 \text{ V} \end{aligned}$$

**Example 4.11**

Calculate the output voltage of an op-amp summing amplifier for the following sets of input voltages  $V_1$ ,  $V_2$  and  $V_3$  and input resistors  $R_1$ ,  $R_2$  and  $R_3$ . Use  $R_f = 1 \text{ M}\Omega$  in all cases.

$$(a) V_1 = +1 \text{ V}, V_2 = +2 \text{ V}, V_3 = +3 \text{ V}, R_1 = 500 \text{ k}\Omega, R_2 = 1 \text{ M}\Omega, R_3 = 1 \text{ M}\Omega$$

$$(b) V_1 = -2 \text{ V}, V_2 = +3 \text{ V}, V_3 = +1 \text{ V}, R_1 = 200 \text{ k}\Omega, R_2 = 500 \text{ k}\Omega, R_3 = 1 \text{ M}\Omega$$

**Solution** We know that the output of an op-amp summing amplifier is

$$V_o = - \left[ \frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3 \right]$$

$$(a) V_o = - \left[ \frac{1 \times 10^6}{500 \times 10^3} \times 1 + \frac{1 \times 10^6}{1 \times 10^6} \times 2 + \frac{1 \times 10^6}{1 \times 10^6} \times 3 \right] = -7 \text{ V}$$

$$(b) V_o = - \left[ \frac{1 \times 10^6}{200 \times 10^3} \times (-2) + \frac{1 \times 10^6}{500 \times 10^3} \times 3 + \frac{1 \times 10^6}{1 \times 10^6} \times 1 \right] = 3 \text{ V}$$

## 4.13 SUBTRACTOR

The basic op-amp can be used as a *subtractor* as shown in Fig. 4.18. To analyse the operation of the circuit, assume that all resistors are of equal value  $R$ , i.e.  $R_1 = R_2 = R_3 = R_f = R$ . The output voltage can be determined by using the superposition principle. If  $V_1 = 0$ , i.e.  $V_1$  is grounded, then the output voltage  $V_{o2}$  will be due to the input voltage  $V_2$  alone. Hence the circuit shown in Fig. 4.18 becomes a non-inverting amplifier of unity gain with input voltage  $V_2/2$  at the non-inverting input terminal and the output voltage is given by

$$V_{o2} = [V_2/2](1 + R/R) = V_2$$

Similarly, if  $V_2 = 0$ , then the output voltage  $V_{o1}$  will be due to  $V_1$  alone. Hence, the circuit becomes an inverting amplifier of unity gain and the output voltage is given by

$$V_{o1} = -V_1$$

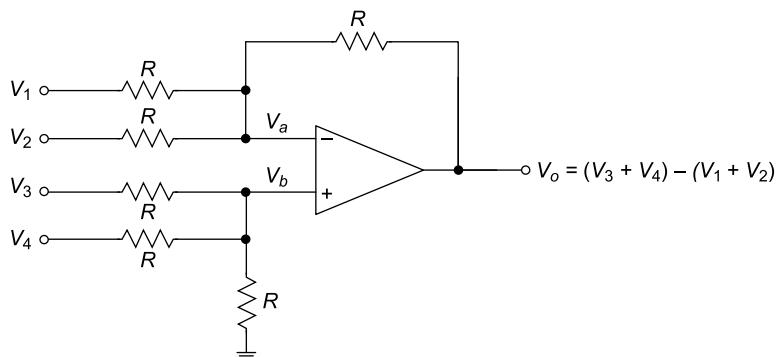
Now, considering that both the inputs are applied, the output voltage  $V_o$  is

$$V_o = V_{o2} + V_{o1} = V_2 - V_1 \quad (4.19)$$

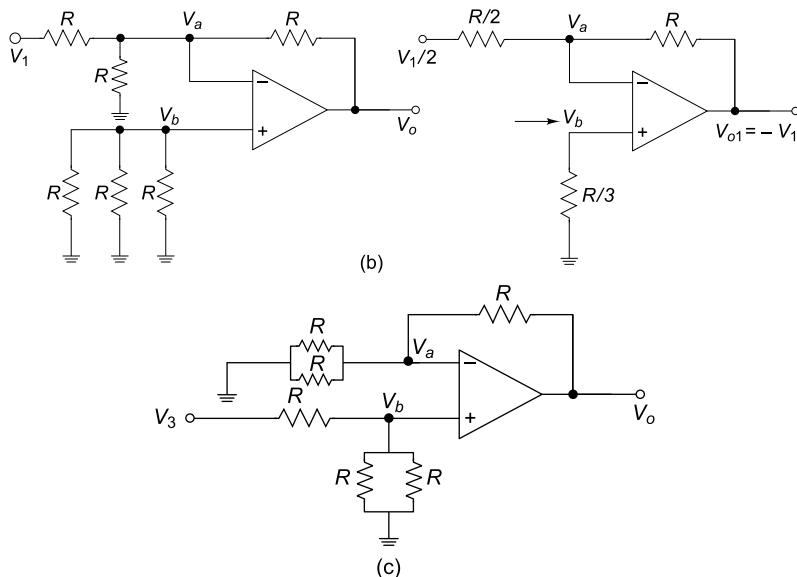
Thus, the output voltage is proportional to the difference between the two input voltages. Hence, it acts as a *difference amplifier* with unity gain.

## 4.14 ADDER–SUBTRACTOR

The circuit shown in Fig. 4.19(a) can perform both addition and subtraction simultaneously on the input signals.



**Fig. 4.19 (a) Adder–Subtractor**



**Fig. 4.19** (b) Equivalent circuit for  $V_2 = V_3 = V_4 = 0$  and (c) Equivalent circuit for  $V_1 = V_2 = V_4 = 0$

The output voltage  $V_o$  can be determined with the help of superposition theorem. The output voltage  $V_{o1}$  due to the input voltage  $V_1$  alone can be found by making all other input voltages equal to zero. The equivalent circuit is shown in Fig. 4.19(b).

Thus the circuit becomes an inverting amplifier for the input  $V_1$  alone and its output voltage is

$$V_{o1} = -\frac{R}{R/2} \frac{V_1}{2} = -V_1$$

Similarly, the output voltage  $V_{o2}$  due to  $V_2$  alone is

$$V_{o2} = -V_2$$

The output voltage  $V_{o3}$  due to the input voltage  $V_3$  alone can be determined by making other input voltages  $V_1$ ,  $V_2$  and  $V_4$  equal to zero. The equivalent circuit is shown in Fig. 4.19(c). Here the circuit becomes a non-inverting amplifier and the voltage at the non-inverting terminal or node  $b$  is

$$V_b = \frac{R/2}{R + R/2} V_3 = \frac{V_3}{3}.$$

Therefore, the output voltage  $V_{o3}$  due to input  $V_3$  alone is given by

$$V_{o3} = \left(1 + \frac{R}{R/2}\right) V_b = 3 \left(\frac{V_3}{3}\right) = V_3$$

Similarly, for the input voltage  $V_4$ , the output voltage  $V_{o4}$  is

$$V_{o4} = V_4$$

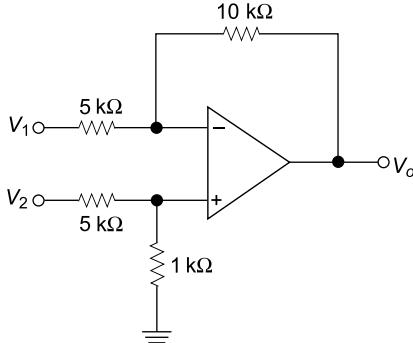
Therefore, the output voltage for all four input voltages applied at the inputs simultaneously is

$$\begin{aligned} V_o &= V_{o1} + V_{o2} + V_{o3} + V_{o4} \\ &= -V_1 - V_2 + V_3 + V_4 \\ V_o &= (V_3 + V_4) - (V_1 + V_2) \end{aligned} \tag{4.20}$$

Hence, the circuit using op-amp shown in Fig. 4.16(a) is an adder-subtractor.

### Example 4.12

Find the output voltage of the following op-amp circuit shown in Fig. 4.20(a).

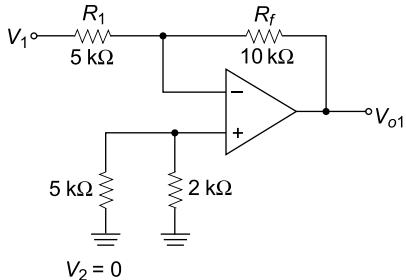


**Fig. 4.20(a)**

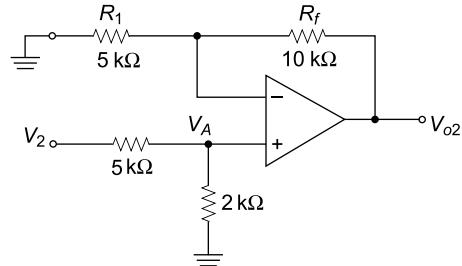
**Solution** Let us use the principle of superposition

**To find output due to  $V_1$ :** Let  $V_2 = 0$  and only  $V_1$  being applied as shown in Fig. 4.20(b). This is the inverting amplifier.

$$\text{Therefore, } V_{o1} = -\frac{R_f}{R_i} \times V_1 = -\frac{10}{5} \times V_1 = -2V_1$$



**Fig. 4.20(b)**



**Fig. 4.20(c)**

**To find output due to  $V_2$ :** Let  $V_1 = 0$  and only  $V_2$  being applied as shown in Fig. 4.20(c). This is the non-inverting amplifier.

$$\begin{aligned} \text{Therefore, } V_{o2} &= \left(1 + \frac{R_f}{R_i}\right) V_A = \left(1 + \frac{R_f}{R_i}\right) \times \frac{2 \times 10^3}{5 \times 10^3 + 2 \times 10^3} \times V_2 \\ &= \left(1 + \frac{10 \times 10^3}{5 \times 10^3}\right) \times \frac{2}{7} \times V_2 = \frac{6}{7} V_2 \end{aligned}$$

**To find  $V_o$**

$$V_o = V_{o1} + V_{o2} = -2V_1 + \frac{6}{7} V_2$$

### Example 4.13

Find out  $V_o$  in the circuit shown in Fig. 4.21.

**Solution** The given circuit is a non-inverting adder.

$$\begin{aligned} V_o &= A_{vf} \times V_i = \left[ 1 + \frac{R_f}{R_1} \right] \times \frac{V_a + V_b}{2} \\ &= \left[ 1 + \frac{3 \times 10^3}{1 \times 10^3} \right] \times \frac{(2 + 3)}{2} = 4 \times 2.5 = 10 \text{ V} \end{aligned}$$

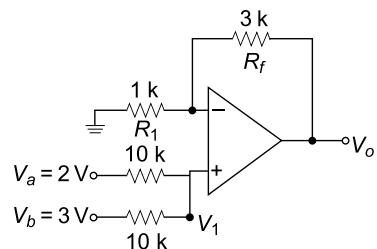


Fig. 4.21

## 4.15 INSTRUMENTATION AMPLIFIER

Instrumentation amplifiers are used in monitoring and controlling of the physical quantities in the industrial processes for measurement and control of temperature, humidity, and light intensity. Normally, a transducer which can convert one form of energy into another is used to sense and deliver the required information in the form of an electrical quantity such as voltage, current or resistance. The signal is sent to the preamplifier stage for initial amplification and, after further amplification and processing, may be passed to the output stages such as meters, oscilloscopes, charts, memories and magnetic recorders.

The major function of an instrumentation amplifier is precise amplification of low level output signal of the transducer, and the instrumentation amplifier is widely used in applications where low noise, low thermal and time drifts, high input impedance and accurate closed-loop gains are required. There are many commercially available instrumentation amplifier ICs, such as AD521, AD524 and AD624 manufactured by Analog Devices, and μA725, TCL7605 and LH0036.

The requirements for instrumentation amplifiers are more rigid than that of general purpose amplifiers. The important features required for an instrumentation amplifier are

- (i) high gain accuracy
- (ii) high CMRR
- (iii) high gain stability with low temperature coefficient
- (iv) low dc offset
- (v) low output impedance

Consider a basic difference amplifier shown in Fig. 4.22. The output voltage  $V_o$  is given by

$$V_o = -\frac{R_2}{R_1} V_2 + \frac{1}{1 + \left( \frac{R_3}{R_4} \right)} \left( 1 + \frac{R_2}{R_1} \right) V_1$$

$$\text{Therefore, } V_o = -\frac{R_2}{R_1} \left[ V_2 - \frac{1}{1 + \left( \frac{R_3}{R_4} \right)} \left( 1 + \frac{R_1}{R_2} \right) V_1 \right]$$

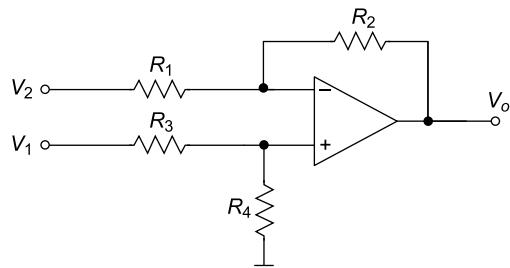


Fig. 4.22 Differential amplifier using single op-amp

If  $\frac{R_1}{R_2} = \frac{R_3}{R_4}$ , then  $V_o = \frac{R_2}{R_1}(V_1 - V_2)$ , i.e. the output voltage  $V_o$  is the difference of the two input voltages with the gain of  $R_2/R_1$ .

The differential amplifier discussed above has its input impedance value limited by the value of resistor  $R_1$ . The gain of the differential amplifier is decided by the factor  $R_2/R_1$ , which restricts the high gain values. This limitation is overcome by the use of a voltage follower between each signal input terminal and the difference amplifier. This has the disadvantage that the gain of the amplifier cannot easily be changed. Hence, a circuit with the possibility of gain adjustment by the use of a single resistor is preferable for instrumentation applications involving very low voltages of the order of microvolts and common-mode signals existing between the two input terminals. The instrumentation amplifier shown in Fig. 4.23 has this feasibility of offering high input impedance and a high gain.

The op-amps  $A_1$  and  $A_2$  as shown in Fig. 4.23 are voltage follower or buffer circuits acting as the input stage for each of the inputs  $V_1$  and  $V_2$ . They have zero differential input voltage, i.e.  $V_{id} = 0$ . Under such conditions with common mode signal = 0, and  $V_1 = V_2$ , the voltage across the resistor  $R$  is zero. The voltages at the inverting terminals of the buffers are equal to the input voltages. Since no current flows through the resistors  $R$  and  $R'$ , the output voltages are  $V'_2 = V_2$  and  $V'_1 = V_1$  respectively. However, if  $V_1 > V_2$ , then a current flows through the resistors  $R$  and  $R'$ , and  $(V'_2 - V'_1) > (V_2 - V_1)$ . Therefore, this circuit will have more differential gain and CMRR compared to the single op-amp circuit shown in Fig. 4.22.

The current flowing in the resistor  $R$  is  $I = \frac{(V_1 - V_2)}{R}$  and the same current  $I$  will flow through the resistors  $R'$  in the direction shown. The voltage at the non-inverting terminal of op-amp  $A_3$  is  $\frac{R_2 V'_1}{R_1 + R_2}$ . By using superposition theorem, we get

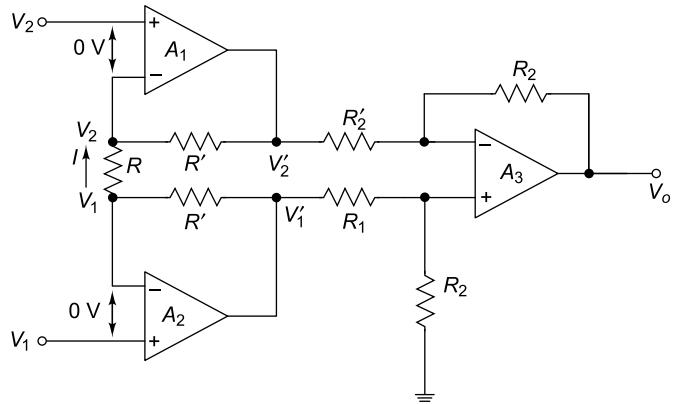
$$V_o = -\frac{R_2}{R_1} V'_2 + \left(1 + \frac{R_2}{R_1}\right) \left(\frac{R_2 V'_1}{R_1 + R_2}\right)$$

Simplifying, we get

$$V_o = \frac{R_2}{R_1} (V'_1 - V'_2) \quad (4.21)$$

Since there is no current entering the op-amp, the current  $I = \frac{(V_1 - V_2)}{R}$ , which flows through the resistor  $R'$ .

$$V'_1 = R'I + V_1 = \frac{R'}{R} (V_1 - V_2) + V_1$$



**Fig. 4.23** Instrumentation amplifier

and

$$V'_2 = -R'I + V_2 = -\frac{R'}{R}(V_1 - V_2) + V_2$$

Substituting the values of  $V'_1$  and  $V'_2$  in Eq. (4.21),  $V_o$  is given by

$$V_o = \frac{R_2}{R_l} \left[ \frac{2R'}{R} (V_1 - V_2) + (V_1 - V_2) \right]$$

That is,

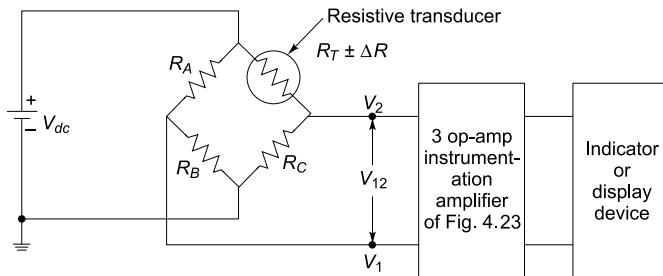
$$V_o = \frac{R_2}{R_l} \left[ 1 + \frac{2R'}{R} \right] (V_1 - V_2)$$

By using a variable resistor  $R$ , the gain of this instrumentation amplifier can be varied.

When  $V_1 = V_2 = V_{cm}$ ,  $V'_1 = V'_2 = V_{cm}$ , where  $V_{cm}$  is the common mode signal. The input stage thus passes the common mode signals with unity gain. On the other hand, when the input stage uses individually connected voltage follower circuits, they would allow both the common mode and the differential mode signals with the same gain. Therefore, the advantage of the coupled differential input stage is that it amplifies only the differential input signals with some voltage gain. The circuit, thus theoretically possesses an infinite CMRR, with the possibility of gain setting by the resistor  $R$  and the circuit is not affected by resistor tolerance value of  $R$ . However, in practice, CMRR is not infinite due to the fact that the two op-amps incur differences in internal common-mode errors.

Use of dual op-amps in those cases is an ideal way to alleviate such errors.

Figure 4.24 shows a differential instrumentation amplifier using transducer bridge. In a resistive transducer, the resistance of the transducer changes as a function of the physical quantity under measurement, which is connected as one arm of the bridge, with a small circle shown around it in Fig. 4.24. Due to a change in temperature, the effective resistance of the transducer changes and it is indicated by  $(R_T \pm \Delta R)$ , where  $R_T$  is the resistance of the transducer and  $\Delta R$  is the change in resistance  $R_T$ .



**Fig. 4.24** Instrumentation amplifier using transducer bridge

The operation of the instrumentation amplifier using the transducer is explained as follows. The bridge is initially balanced with the use of a dc supply voltage  $V_{dc}$ , so that  $V_1 = V_2$ .

That is,

$$\frac{R_B(V_{dc})}{R_B + R_A} = \frac{R_C(V_{dc})}{R_C + R_T}$$

Therefore,

$$\frac{R_A}{R_B} = \frac{R_T}{R_C}$$

or

$$R_T = \left( \frac{R_A}{R_B} \right) R_C$$

If the ratio of  $R_A$  to  $R_B$ , which is called the *ratio arms* of the bridge is assumed as constant  $k$ , then the value of the transducer resistance  $R_T = kR_C$ . As the physical quantity changes, the resistance value  $R_T$  of the transducer changes, and this causes an imbalance in the bridge. That is, the output of the bridge  $V_1 \neq V_2$ . The three op-amp instrumentation amplifier shown in Fig. 4.23 amplifies this differential voltage.

Let  $\Delta R$  be the change in resistance of the transducer. As the resistor  $R_B$  and  $R_C$  are fixed resistors, the voltage  $V_1$  is constant. However, the voltage  $V_2$  varies as a function of the change in transducer resistance.

Therefore,

$$V_2 = \frac{R_C(V_{dc})}{R_C + (R_T + \Delta R)}$$

$$V_1 = \frac{R_B(V_{dc})}{R_A + R_B}$$

Consequently, the voltage  $V_{12}$  across the output terminal of the bridge is  $V_{12} = V_2 - V_1$ .

Therefore,

$$V_{12} = \frac{R_C(V_{dc})}{R_C + R_T + \Delta R} - \frac{R_B(V_{dc})}{R_C + R_B}$$

If  $R_A = R_B = R_C = R_T = R$ , then the above equation becomes

$$V_{12} = -\frac{\Delta R(V_{dc})}{2(2R + \Delta R)}$$

The gain of the basic differential amplifier is  $-R_2/R_1$ . Therefore, the output voltage  $V_o$  is

$$V_o = V_{12} \left( \frac{R_2}{R_1} \right) = \frac{\Delta R(V_{dc})}{2(2R + \Delta R)} \frac{R_2}{R_1}$$

Since the change in resistance of a transducer is normally very small,  $(2R + \Delta R) \approx 2R$ . Hence the output voltage  $V_o$  becomes

$$V_o = \left( \frac{R_2}{R_1} \right) \frac{\Delta R(V_{dc})}{4R}$$

Therefore, the output voltage is a function of the change in resistance of the transducer element, multiplied by the gain value of the op-amp  $A_3$  and it is also determined by the resistor  $R$ .

### Example 4.14

For the circuit shown in Fig. 4.25, show that the input resistance  $R_i = \frac{V_i}{I_i} = \frac{R_1 R_3}{R_3 - R_1}$ .

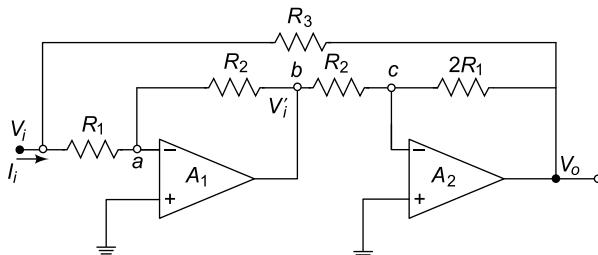


Fig. 4.25

**Solution** For op-amp  $A_1$ , voltage at node  $a$  is zero. The current entering at node  $a$  is given by

$$\frac{V_i - 0}{R_1} = \frac{V'_i - 0}{R_2}$$

For op-amp  $A_2$ , with input  $V'_i$  at node  $b$ , the current entering at node  $c$  is given by

$$\frac{V_o - 0}{2R_1} = \frac{V'_i - 0}{R_2}$$

Using the above two equations,  $\frac{V'_i}{R_2} = \frac{V_o}{2R_1}$

$$\text{Therefore, } \frac{V'_i}{R_1} = \frac{V_o}{2R_1} \text{ or } V_o = 2V_i$$

The current  $I_i$  from source  $V_i$  is given by the sum of current through  $R_3$  and  $R_1$ .

$$\text{Therefore, } I_i = \frac{V_i - V_o}{R_3} + \frac{V_i - 0}{R_1}$$

Substituting  $V_o = 2V_i$  in the above equation, we get

$$I_i = \frac{V_i - 2V_i}{R_3} + \frac{V_i}{R_1} = \frac{-V_i R_1 + V_i R_3}{R_1 R_3} = \frac{V_i (R_3 - R_1)}{R_1 R_3}$$

$$\text{Hence, the input impedance of the circuit, } R_i = \frac{V_i}{I_i} = \frac{R_1 R_3}{R_3 - R_1}$$

## 4.16 AC AMPLIFIER

The op-amps are fundamentally high-gain dc amplifiers. However, they can often be used for ac amplification also. This section highlights the inverting and non-inverting ac amplifier applications of the op-amp. This was already discussed in Sub-section 3.11.5.

The inverting and non-inverting amplifiers using op-amps can respond to both dc and ac signals. If a dc voltage is superimposed on an ac input signal, then it is necessary to block the dc component to obtain the ac frequency response of an op-amp. This can be achieved by using an ac amplifier with a coupling capacitor. These ac amplifiers can be realised in two configurations, namely, (i) inverting ac amplifier and (ii) non-inverting ac amplifier.

### 4.16.1 Inverting ac Amplifier

The inverting ac amplifier is shown in Fig. 4.26(a). The capacitor  $C$  connected in series with the resistor  $R_1$  blocks the dc component of the input. It sets the lower 3dB frequency of the amplifier.

To analyse the circuit in frequency domain:

The node  $a$  is at virtual ground, and thus, the output voltage  $v_o$  is given by

$$v_o = -iR_f = -\frac{v_i}{R_1 + 1/sC} R_f$$

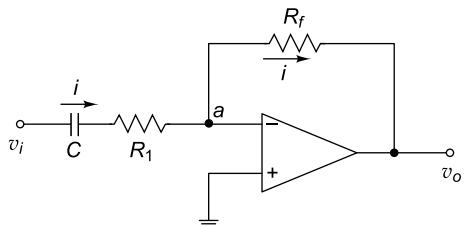


Fig. 4.26 (a) Inverting ac amplifier

Therefore,

$$A_{CL} = \frac{v_o}{v_i} = -\frac{R_f}{R_l} \frac{s}{s + 1/R_l C} \quad (4.22)$$

From the above equation, we get the lower 3dB frequency as

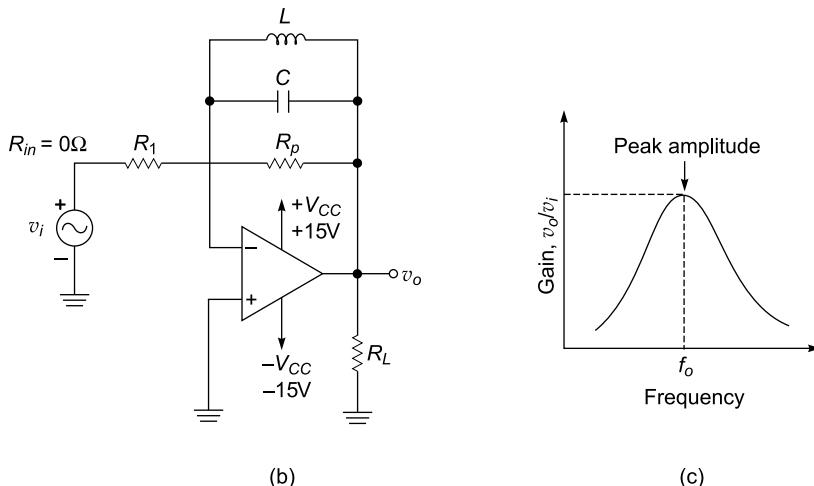
$$f_L = \frac{1}{2\pi R_l C} \quad (4.23)$$

At higher frequencies, the capacitor  $C$  behaves like a short circuit and hence Eq. (4.22) becomes

$$A_{CL} = -\frac{R_f}{R_l}$$

**Peaking amplifier** The unit gain bandwidth (UGB) of the op-amp represents the operational bandwidth of the op-amp when the voltage gain is 1. It is also called *closed-loop bandwidth* and *small-signal bandwidth*. While the op-amp 741 has approximately 1 MHz of UGB, the newer op-amps such as LF351 and MC34001 have a gain-bandwidth product of 4 MHz.

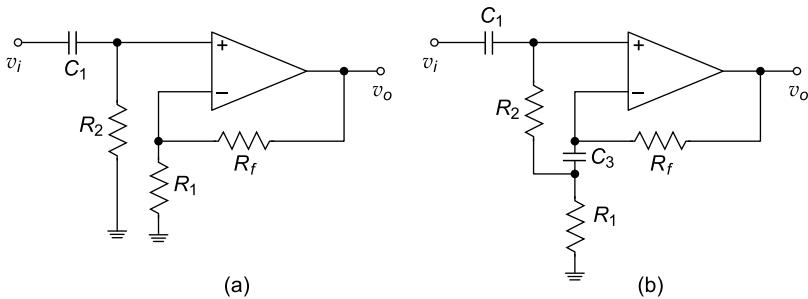
When an application requires amplification of signals of a particular frequency, the peak amplifier circuit shown in Fig. 4.26(b) with its frequency response shown in Fig. 4.26 (c) can be employed. Here, the frequency under consideration must be less than the UGB.



**Fig. 4.26** (b) Peaking amplifier, and (c) its frequency response

#### 4.16.2 Non-inverting ac Amplifier

The non-inverting ac amplifier is shown in Fig. 4.27(a). Here, a resistor  $R_2$  is included to provide a dc return to ground, which reduces the overall input impedance of the amplifier that is approximately equal to  $R_2$ . A high input impedance for the non-inverting ac amplifier may be obtained by using the circuit shown in Fig. 4.27(b).



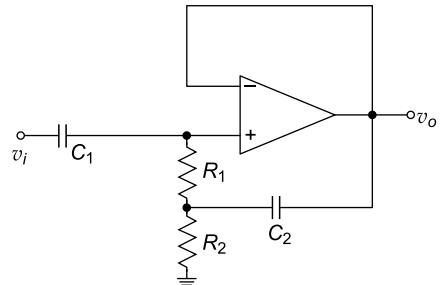
**Fig. 4.27** Non-inverting ac amplifier: (a) With low input impedance  
(b) With high input impedance

### 4.16.3 The ac Voltage Follower

The circuit of an ac voltage follower is shown in Fig. 4.28, which is used as a buffer to connect a high impedance input signal to a low impedance load. The capacitors  $C_1$  and  $C_2$  of larger values are selected so that they behave like a short circuit at any frequency. The resistors  $R_1$  and  $R_2$  provide a path for the flow of dc input current to the non-inverting terminal. The capacitor  $C_2$  acts as a bootstrapping capacitor which is connected to resistor  $R_1$  for ac operation. From Miller's theorem, the input resistance is given by

$$R_i = \frac{R_1}{1 - A_{CL}}$$

Here, since the gain  $A_{CL}$  of the voltage follower is close to unity, the input impedance is very high.



**Fig. 4.28** AC voltage follower

### 4.17 INTEGRATOR

A circuit in which the output voltage waveform is the time integral of the input voltage waveform is called *integrator* or *integrating amplifier*. Integrator produces a summing action over a required time interval and the circuit is based on the general parallel-inverting voltage feedback model.

#### 4.17.1 Ideal Integrator

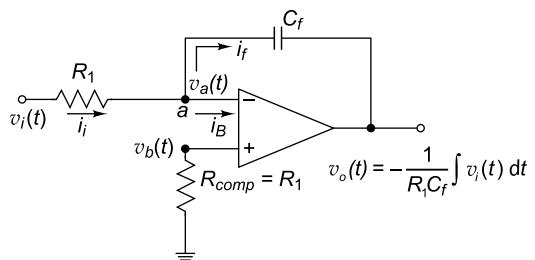
In order to achieve integration, the basic inverting amplifier configuration shown in Fig. 4.1 can be used with the feedback element  $Z_f$  replaced by a capacitor  $C_f$  as shown in Fig. 4.29.

The expression for the output voltage  $v_o(t)$  can be obtained by writing Kirchhoff's current equation at node  $a$  as given by

$$i_i = i_B + i_f$$

Since  $i_B$  is negligibly small,

$$i_i = i_f$$



**Fig. 4.29** Integrator circuit

The current through the capacitor,  $i_C(t) = C \frac{dv_c(t)}{dt}$

$$\text{Therefore, } \frac{v_i(t) - v_a(t)}{R_l} = C_f \frac{d}{dt}(v_a(t) - v_o(t))$$

However,  $v_b(t) = v_a(t) = 0$  because the gain of the op-amp  $A_v$  is very large. Therefore,

$$\frac{v_i(t)}{R_l} = C_f \frac{d}{dt}(-v_o(t))$$

Integrating both sides with respect to time, we get the output voltage as defined by

$$\int_0^t \frac{v_i(t)}{R_l} dt = \int_0^t C_f \frac{d}{dt}(-v_o(t)) dt = -C_f v_o(t) + v_o(0)$$

Therefore,

$$v_o(t) = -\frac{1}{R_l C_f} \int_0^t v_i(t) dt + v_o(0) \quad (4.24)$$

where  $v_o(0)$  is the integration constant and is proportional to the value of the output voltage  $v_o(t)$  at  $t = 0$ . Equation (4.24) indicates that the output voltage is directly proportional to the negative integral of the input voltage and inversely proportional to the time constant  $R_l C_f$ .

In frequency domain, the above equation becomes

$$V_o(s) = -\frac{1}{s R_l C_f} V_i(s) \quad (4.25)$$

Letting  $s = j\omega$  in steady-state, we get

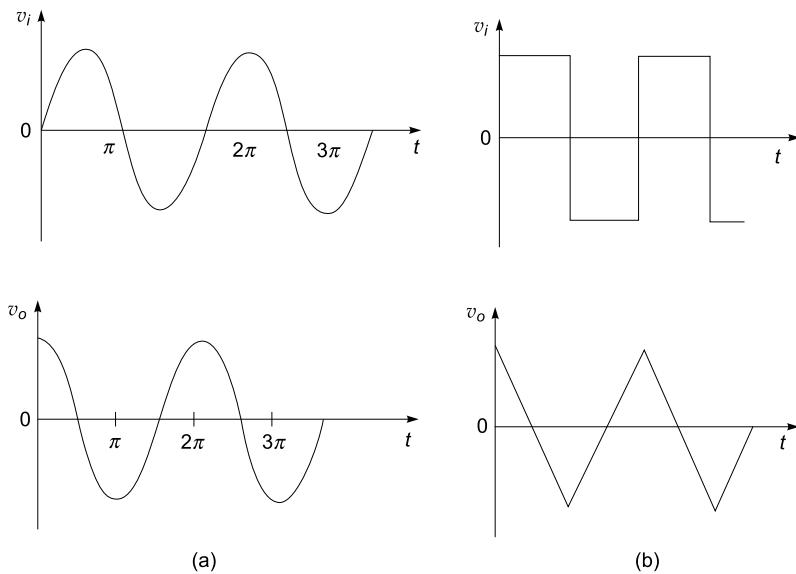
$$V_o(j\omega) = -\frac{1}{j\omega R_l C_f} V_i(j\omega) \quad (4.26)$$

Hence, the magnitude of the transfer function of the integrator is

$$|A| = \left| \frac{V_o(j\omega)}{V_i(j\omega)} \right| = \left| \frac{j}{\omega (R_l C_f)} \right| = \frac{1}{\omega R_l C_f} \quad (4.27)$$

At  $\omega = 0$ , the gain of the integrator is infinite. Also the capacitor acts as an open circuit and hence there is no negative feedback. Thus, the op-amp operates in open loop and hence the gain becomes infinite (or the op-amp saturates). In practice, the output will never become infinite. As the frequency increases, the gain of the integrator decreases.

The input sinusoidal and square waveforms and the corresponding output waveforms of integrator circuit using op-amp are shown in Fig. 4.30(a) and (b).



**Fig. 4.30** (a) Sine-wave input and its integrated cosine output and  
(b) Square-wave input and its triangular output

### 4.17.2 Limitations of an Ideal Integrator

Even in the absence of input signal, the two components, namely, the offset voltage and the bias current contribute for an error voltage at the output. Thus, it is not possible to get a true integration of the input signal at the output. The output waveform is distorted due to this error voltage. Further, the bandwidth of an ideal integrator is very small. Hence, an ideal integrator can be used for very small ranges of input frequency only.

In the ideal integrator circuit, a small dc offset at the input can force the output into saturation. To avoid this, a resistor is placed in parallel with the integrator capacitor to limit the low frequency gain. However, this has an undesirable side effect of limiting the useful integration range at higher frequencies.

Due to the above limitations, an ideal integrator is not used in practice. A few additional components are used along with the ideal integrator circuit to minimise the effect of the error voltage. Such an integrator is called *practical integrator*.

**Integrator errors** The integrator errors are the deviations from the ideal behaviour found in a practical integrator circuit. The major sources of error are the offset and drift of the op-amp. The op-amp's input offset voltage and bias current cause continuous charging of feedback capacitor even in the absence of an input signal. As a result, the op-amp output can drift into the positive or negative saturation.

The error component at the output due to the op-amp bias current can be compensated by connecting a resistor of the same value as the integrating resistor between the non-inverting input and ground. The drift error can be minimised by the use of a large value capacitor. This makes the bias current contribution to the drift negligibly small. However a large value of  $C$  needs a smaller value of  $R$ . To avoid drift by the dielectric absorption of the capacitor, polypropylene or polystyrene dielectric capacitors can be used.

The use of low current FET input op-amps make low drift integrators with long-term stability realisable. They also allow the bias current contribution to drift negligibly small. This can eliminate the need of excessively large capacitors also.

### 4.17.3 Summing Integrator

The circuit diagram of a summing integrator is shown in Fig. 4.31, which is derived from the simple integrator shown in Fig. 4.29(a). Using Eq. (4.24), the output voltage for the summing integrator can be written as

$$v_o(t) = -\frac{1}{C_f} \int_0^t \left( \frac{v_1(t)}{R_1} + \frac{v_2(t)}{R_2} + \frac{v_3(t)}{R_3} \right) dt + v_o(0)$$

Taking Laplace transform, we get

$$V_o(s) = -\frac{1}{sC_f} \left( \frac{V_1(s)}{R_1} + \frac{V_2(s)}{R_2} + \frac{V_3(s)}{R_3} \right)$$

### 4.17.4 Double Integrator

The circuit that integrates the input signal twice is called double integrator. The design of double integrator requires two reactive portions for obtaining double integration. In the circuit of double integrator shown in Fig. 4.32, a pair of  $RC$  Tee networks is used. The output equation is

$$v_o(t) = -\frac{4}{(RC)^2} \iint v_i(t) dt$$

### 4.17.5 Practical Integrator Circuit (ac Integrator Circuit)

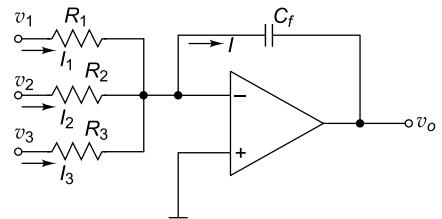
The practical integrator circuit (*lossy integrator*) is shown in Fig. 4.33(a). Here, the feedback capacitor is shunted by a resistor  $R_f$  so that the gain of the integrator at low frequency is limited to avoid any saturation problem. Since the parallel combination of resistor  $R_f$  and capacitor  $C_f$  dissipates power, this circuit is called a lossy integrator. The resistor  $R_f$  provides the dc stabilisation, by limiting the low frequency gain to  $-R_f/R_1$ . The resistor  $R_{comp}$  is given by  $R_{comp} = R_1 \parallel R_f$  and when  $R_f \gg R_1$ ,  $R_{comp} = R_1$ .

At the inverting input terminal of the op-amp, the nodal equation may be written as

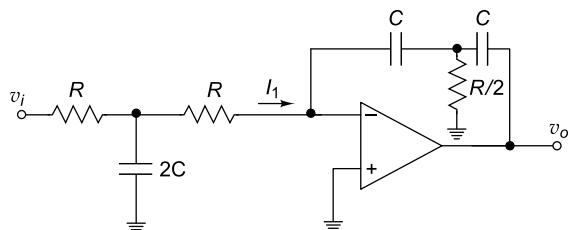
$$\frac{V_i(s)}{R_1} + sC_f V_o(s) + \frac{V_o(s)}{R_f} = 0$$

Rearranging the above equation, we get

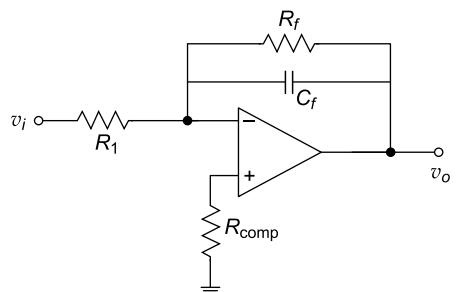
$$V_o(s) = -\frac{1}{sR_1 C_f + R_1 / R_f} V_i(s)$$



**Fig. 4.31** Summing integrator



**Fig. 4.32** Double integrator



**Fig. 4.33 (a)** Practical integrator circuit

Substituting  $s = j\omega$ , we get the transfer function as expressed by

$$|A| = \left| \frac{V_o}{V_i} \right| = \frac{1}{\sqrt{\omega^2 R_l^2 C_f^2 + R_l^2 / R_f^2}} = \frac{R_f / R_l}{\sqrt{1 + (\omega R_f C_f)^2}}.$$

When  $R_f$  is very large, the lossy integrator will approximately become an ideal integrator. At low frequencies, assuming the low level frequency to be  $f_a$ , the gain is approximately equal to  $R_f/R_l$ . At 3 dB level the gain is  $0.707(R_f/R_l)$ .

Therefore,

$$\sqrt{1 + (\omega R_f C_f)^2} = \sqrt{2}$$

Solving for  $f = f_a$ , we get

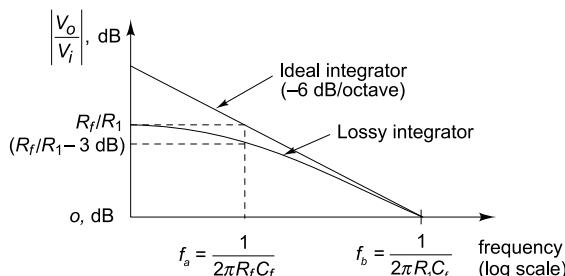
$$2\pi f_a R_f C_f = 1$$

$$\text{Hence, } f_a = \frac{1}{2\pi R_f C_f}$$

The frequency responses of the ideal integrator and the lossy integrator are shown in Fig. 4.33(b). The ideal integrator of Fig. 4.29 exhibits a  $-6$  dB/octave ( $-20$  dB/decade) slope through the useful integration range. The frequency  $f_b$  is the frequency at which the transfer function or gain of the integrator is 1 or

$0$  dB i.e.  $1 = \frac{1}{2\pi f_b R_l C_f}$ . Hence,  $f_b = \frac{1}{2\pi R_l C_f}$ . When the input frequency is less than  $f_a$ , the circuit will

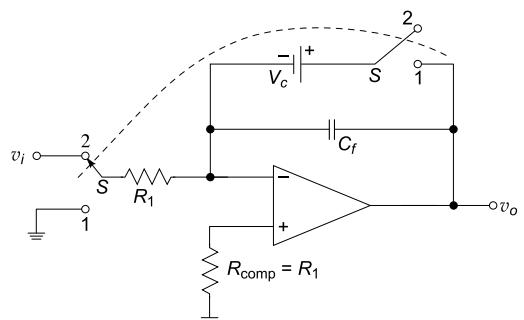
not act as an integrator and it will only act as a simple inverting amplifier. When the input frequency is equal to  $f_a$ , there will be 50 percent accuracy. As a thumb rule, if the input frequency is 10 times  $f_a$ , then it results in 99% of accuracy.



**Fig. 4.33 (b)** Frequency responses of the ideal and lossy integrators

#### 4.17.6 Initial Condition

The circuit shown in Fig. 4.34 sets the initial condition for the integrator circuit as required for some applications. When the ganged switch  $S$  is turned ON initially before powering the op-amp, the capacitor  $C_f$  immediately charges to the voltage  $V_c$  of the battery. When the switch  $S$  is moved to position 2, the op-amp circuit with the feedback capacitor  $C_F$  and input resistor  $R_1$  acts as an integrator with the initial conditions as set by the battery  $V_c$ .

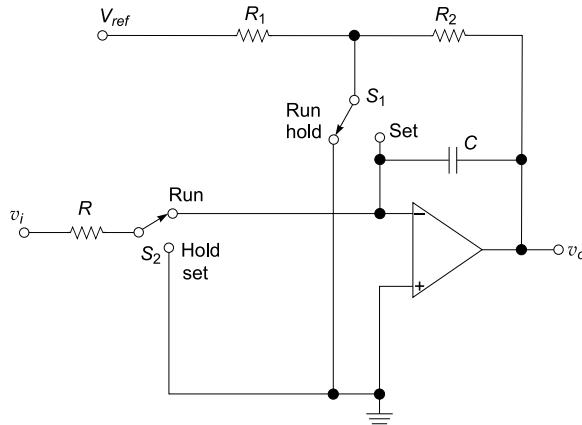


**Fig. 4.34** Integrator circuit with initial condition

The capacitor is normally chosen to have very low leakage, and Teflon, Polystyrene or Mylar dielectric capacitors are preferred.

#### 4.17.7 Integrator Run, Set and Hold Modes

A practical integrator circuit may need to possess the abilities, namely (i) provision to set a desired initial value of the integrator output voltage before the start of integration, (ii) facility to stop the integration process at a specified time, and (iii) provision to maintain the integrated output value constant. Figure 4.35 shows the operation of integrator with the run, set and hold modes.



**Fig. 4.35** Integrator run, set and hold modes of operation

The switches  $S_1$  and  $S_2$  facilitate the operating modes. Switch  $S_1$  when switched to 'set' position allows the initial value of the integrator output  $v_o$  to be initialised to the desired value, as given by

$$v_{o(t=0)} = -\frac{R_2}{R_1} V_{ref}$$

Assuming  $v'_o$  to be the voltage at output at the time instant of switching, the output  $v'_o$  follows the relationship

$$v_o = v_{o(t=0)} + \left( v'_o - v_{o(t=0)} \right) e^{-t/R_2 C}$$

With  $v'_o$  zero at the start of integration

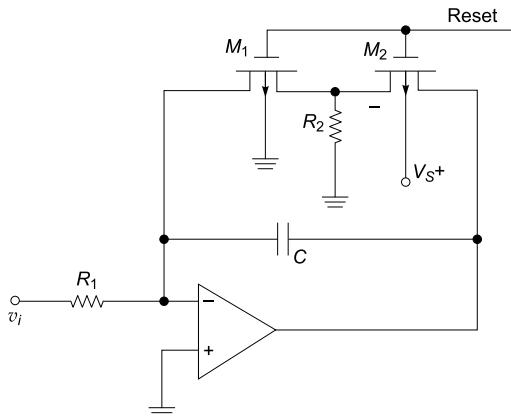
$$\begin{aligned} v_o &= v_{o(t=0)} \left( 1 - e^{-t/R_2 C} \right) \\ &= -\frac{R_2}{R_1} V_{ref} \left( 1 - e^{-t/R_2 C} \right) \end{aligned}$$

When the switches are pushed to *run* mode, the integrator circuit integrates the input voltage  $v_i$  and

$$v_o = v_{o(t=0)} - \frac{1}{RC} \int_0^t v_i dt$$

Then, the circuit acts as the inverting integrator. When the integrator is set to the *hold* mode, the integration process stops, and the output of the integrator remains ideally constant. However, during the *run* and *hold* modes, drift and offset of op-amps introduce integrator errors.

**Integrator reset** The output of an integrator does not fall to zero when the input voltage is made zero or when removed. Hence, the reset switches are needed to null the integrator output. Figure 4.36 shows a low leakage integrator reset circuit using two p-channel MOSFET switches. A negative going reset pulse turns the  $M_1$  and  $M_2$  transistors ON. This shorts the integrating capacitor  $C$  and sets the output voltage to near zero. This is realised by making resistance  $R_2$  much larger than the ON resistance  $R_{on}$  of the MOS transistor. The substrate of  $M_2$  is connected to a substrate voltage  $V_{s+}$  to avoid source-substrate junction from becoming forward biased.



**Fig. 4.36** Low leakage integrator reset circuit

#### 4.17.8 Applications of Integrators

Integrators may be used in combination with summers and amplifiers to form analog computers which are used to model a variety of physical systems in real time. The integrator circuits are used as waveshaping circuits and used to convert square-waves into triangular waves. Further they are used for solving differential equations in analog to digital converters, and ramp generators.

#### Example 4.15

Assuming  $R_1 = 10 \text{ k}\Omega$ ,  $R_f = 100 \text{ k}\Omega$  and  $C_f = 10 \text{ nF}$  in a practical integrator circuit of Fig. 4.33(a), determine the lower frequency limit of integration and the output response for the inputs (a) sine-wave (b) square-wave and (c) step input.

**Solution** Given  $R_1 = 10 \text{ k}\Omega$ ,  $R_f = 100 \text{ k}\Omega$  and  $C_f = 10 \text{ nF}$ . The lower frequency limit of integration is

$$\begin{aligned} f_a &= \frac{1}{2\pi R_f C_f} \\ &= \frac{1}{2\pi \times 100 \times 10^3 \times 10 \times 10^{-9}} = 159 \text{ Hz} \end{aligned}$$

For accurate integration, the input frequency must be at least one decade above  $f_a$ , i.e. 1590 Hz.

##### (a) For the sine-wave input

For an input of 1V peak sine-wave at 2.5 kHz, the output  $v_o$  is

$$\begin{aligned} v_o(t) &= -\frac{1}{R_1 C_f} \int v_i(t) dt \\ &= -\frac{1}{10 \times 10^3 \times 10 \times 10^{-9}} \int 1 \sin(2\pi \times 2500t) dt \\ &= -10^4 \int \sin(2\pi \times 2500t) dt \\ &= -\frac{10^4}{2\pi \times 2500} [-\cos(2\pi \times 2500t)] \\ &= 0.637 \cos(2\pi \times 2500t) \end{aligned}$$

The output is a cosine wave with peak amplitude of 0.637 V only as shown in Fig. 4.37(a).

### (b) For the square-wave input

The output waveform for an input of 2.5 kHz, 1V peak square-wave is shown in Fig. 4.37(b).

It can be seen that input is of constant amplitude of 1V from 0 to 0.2 ms and -1V from 0.2 ms to 0.4 ms. The output for each of these half periods will be ramps as seen above for step inputs. Thus, the expected output waveform will be a triangular wave. The peak value of the output for first half cycle is

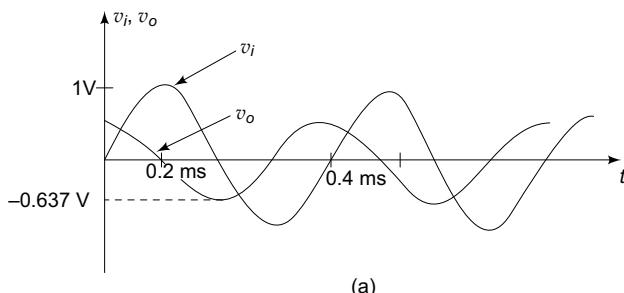
$$v_o = -\frac{1}{R_i C_f} \int_0^{0.2 \text{ ms}} 1 dt = -10^4 \times 0.2 \times 10^{-3} = -2 \text{ V}$$

This represents the total change in the output voltage over the first half cycle from 0 to 0.2 ms. Similarly, integration over the next half-cycle produces a positive change to reach 1V.

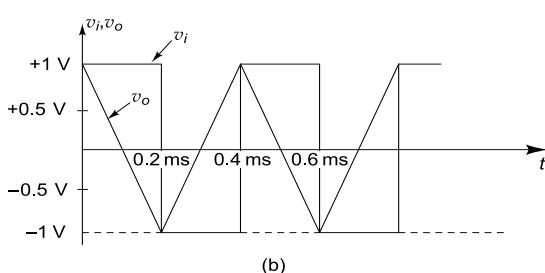
### (c) For the step input

If input is a step voltage  $V_1 = 1\text{V}$  for  $0 \leq t \leq 0.6 \text{ ms}$ , then the output voltage as shown in Fig. 4.37(c) is given by

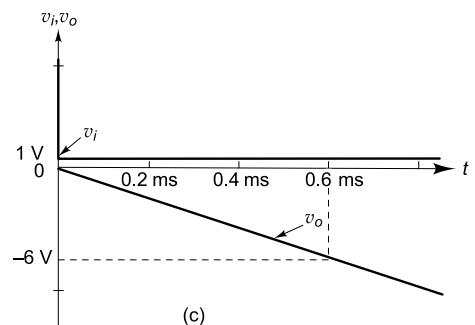
$$\begin{aligned} v_o &= -\frac{1}{R_i C_f} \int_0^{0.6 \text{ ms}} 1 dt \\ &= -\frac{1}{10 \times 10^3 \times 10 \times 10^{-9}} \times t \Big|_{t=0}^{t=0.6 \text{ ms}} = -10^4 \times 0.6 \times 10^{-3} = -6 \text{ V} \end{aligned}$$



(a)



(b)



(c)

**Fig. 4.37** Input and output waveforms for the integrator: (a) Sine-wave input, (b) Square-wave input (c) Step input

## 4.18 DIFFERENTIATOR

The differentiator can perform the mathematical operation of differentiation, i.e. the output voltage is the differentiation of the input voltage. This operation is very useful to find the rate at which a signal varies with time.

### 4.18.1 Ideal Differentiator

The ideal differentiator is obtained by interchanging the position of the resistor and capacitor in the ideal integrator circuit, or it may be constructed from a basic inverting amplifier shown in Fig. 4.1, if the input resistor  $R_1$  is replaced by a capacitor  $C_1$ . The ideal differentiator circuit is shown in Fig. 4.38.

**Analysis** The expression for the output voltage can be obtained from Kirchhoff's Current Law written at node  $a$  as follows:

$$i_c = I_B + i_f$$

Since  $I_B \approx 0$ ,

$$i_c = i_f$$

$$C_1 \frac{d}{dt} (v_i - v_a) = \frac{v_a - v_o}{R_f}$$

But  $v_a = v_b \approx 0$  V, since  $A$  is very large.

Therefore,

$$C_1 \frac{d v_i}{d t} = - \frac{v_o}{R_f}$$

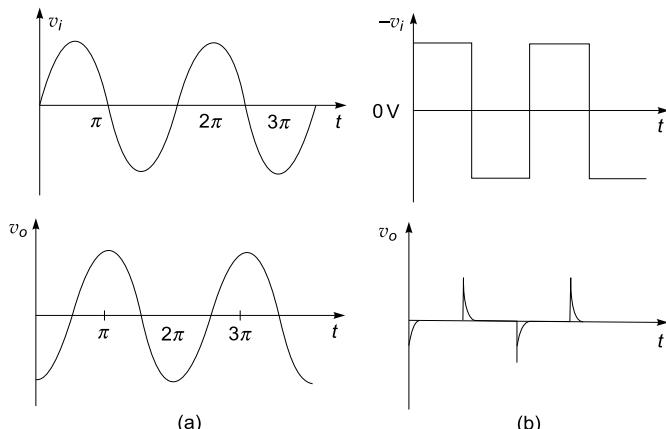
or

$$v_o = - R_f C_1 \frac{d v_i}{d t} \quad (4.28)$$

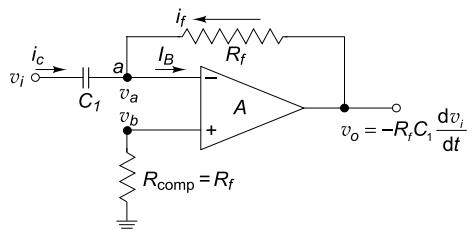
Thus, the output  $v_o$  is equal to the  $R_f C_1$  times the negative instantaneous rate of change of the input voltage  $v_i$  with time. A differentiator performs the reverse of the integrator's function. The upper cut-off frequency is given by

$$f_a = \frac{1}{2\pi R_f C_1}$$

The input sinusoidal and square waveforms and the corresponding output waveforms of differentiator circuit using op-amp are shown in Figs. 4.39(a) and (b).



**Fig. 4.39** (a) Sine-wave input and its differentiated cosine output, (b) Square-wave and its differentiated spike output



**Fig. 4.38** Differentiator

### 4.18.2 Summing Differentiator

The circuit diagram of a summing differentiator is shown in Fig. 4.40, which is derived from the simple differentiator shown in Fig. 4.38. Using Eq. (4.28), the output voltage for the summing differentiator can be written as

$$v_o(t) = -R_f \left[ C_1 \frac{dv_1(t)}{dt} + C_2 \frac{dv_2(t)}{dt} \right]$$

For  $C_1 = C_2$ , we get

$$v_o(t) = -R_f C_1 \left[ \frac{dv_1(t)}{dt} + \frac{dv_2(t)}{dt} \right]$$

### Example 4.16

Design a differentiator to differentiate an input signal that varies in frequency from 10 Hz to about 1 kHz.

**Solution** The upper cut-off frequency  $f_a = 1 \text{ kHz} = \frac{1}{2\pi R_f C_1}$

Letting  $C_1 = 1 \mu\text{F}$ , we have

$$R_f = \frac{1}{(2\pi)(10^3)(10^{-6})} = 1.59 \text{ k}\Omega$$

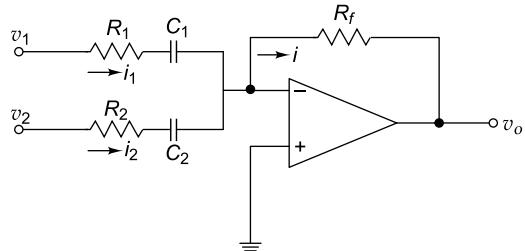
### 4.18.3 Limitations of Differentiators

When compared to integrator circuits, the differentiator circuits are more susceptible to noise. The input noise fluctuations of small amplitudes will have large derivatives. When differentiated, these noise fluctuations will generate large noise signals at the output, which will introduce a poor signal-to-noise-ratio. This problem may be minimised by placing a resistor in series with the input capacitor. This modified circuit differentiates only low frequency signals with a constant high frequency gain.

In a differentiator circuit, the limitations due to noise, stability and input impedance can pose problems. In order to minimise noise and aid in stability, a small capacitor may be placed in parallel with  $R_f$ , which will reduce the high frequency gain. In order to place a lower limit on the input impedance, a resistor may be connected in series with the differentiating capacitor. The addition of either component will limit the upper range of differentiation.

As the frequency increases, the gain of the differentiator increases due to the reduction of input impedance  $X_{C1} = \frac{1}{2\pi f C_1}$ . Therefore, at high frequencies, the differentiator will become unstable due to very high gain and it may enter into saturation. This makes the circuit very sensitive to noise and the stability is affected. The noise component may override the signal also.

These limitations are overcome using a practical differentiator circuit with additional components connected as discussed in the next section.



**Fig. 4.40** Summing differentiator

#### 4.18.4 Practical Differentiator

A practical differentiator circuit is shown in Fig. 4.41(a). This eliminates the limitations of noise and stability. The effective current at the node  $a$  is zero. The input current  $i_C = \frac{v_i - v_a}{Z_1} = \frac{v_i}{Z_1}$  where  $Z_1 = R_1$  in series with  $C_1$ .

Therefore, the input impedance

$$Z_1 = R_1 + \frac{1}{sC_1} = \frac{1 + sR_1 C_1}{sC_1}$$

$$I_C = \frac{sC_1 V_i(s)}{(1 + sR_1 C_1)}$$

The current  $i_{f1}$  flowing through  $R_f$  is given by

$$i_{f1} = \frac{v_a - v_o}{R_f} = -\frac{v_o}{R_f}$$

Taking Laplace transform, we get

$$I_{f1} = \frac{V_o(s)}{R_f}$$

Similarly, the current  $I_{f2}$  flowing through  $C_f$  is given by

$$i_{f2} = C_f \frac{d(v_a - v_o)}{dt} = -C_f \frac{dv_o}{dt}$$

Taking Laplace transform, we get

$$i_{f2} = -sC_f V_o(s)$$

Applying Kirchhoff's Current Law at node  $a$ , we have,  $I_C = i_{f1} + i_{f2}$

$$\text{Therefore, } \frac{sC_1 V_i(s)}{(1 + sR_1 C_1)} = -\frac{V_o(s)}{R_f} - sC_f V_o(s)$$

Simplifying

$$V_o(s) = -\frac{sR_f C_1 V_i(s)}{(1 + sR_f C_f)(1 + sR_1 C_1)} \quad (4.29)$$

The transfer function for the circuit is given by

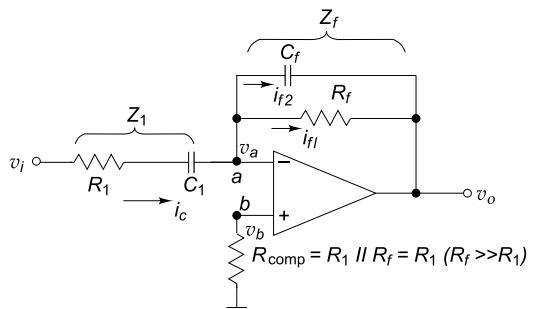
$$\frac{V_o(s)}{V_i(s)} = \frac{Z_f}{Z_i} = -\frac{sR_f C_1}{(1 + sR_f C_f)(1 + sR_1 C_1)} \quad (4.30)$$

Letting  $R_f C_f = R_1 C_1$ , we get

$$\frac{V_o(s)}{V_i(s)} = -\frac{sR_f C_1}{(1 + sR_1 C_1)^2} = -\frac{sR_f C_1}{\left(1 + j \frac{f}{f_b}\right)^2} \quad (4.31)$$

$$\text{where } f_b = \frac{1}{2\pi R_1 C_1}.$$

Equation (4.31) shows that the gain increases at +20 dB/decade for frequency ranges of  $f < f_b$  and decreases at the rate of -20 dB/decade for  $f > f_b$ . It is shown as the gain characteristics in Fig. 4.41(b)

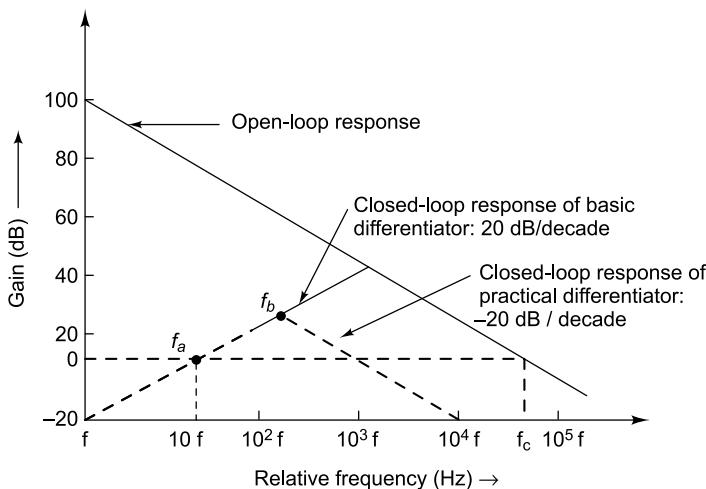


**Fig. 4.41 (a) Practical differentiator**

in dotted lines. This 40 dB/decade variation in gain is due to the  $R_1C_1$  and  $R_fC_f$  factors. For the ideal differentiator of Fig. 4.38, the frequency response would have steadily increased at 20dB / decade even beyond  $f_b$ , which could cause stability problems at high frequencies. The gain for the practical differentiator circuit is reduced significantly and this avoids the high frequency noise, and results in better stability.

The value  $f_b$  is normally selected such that  $f_a < f_b < f_c$  where  $f_c$  denotes the unity gain-bandwidth of the op-amp in open loop configuration mode. For effective differentiation, the time period  $T$  of the input signal is given by  $T \geq R_f C_1$  as indicated in Eq. (4.30).

When  $R_1C_1$  and  $R_fC_f$  are much less than  $R_fC_1$ , then Eq. (4.29) becomes,  $v_o = -R_f C_1 \frac{dv_i}{dt}$ . A compensation resistor  $R_{\text{comp}}$  is normally connected at the non-inverting terminal of the op-amp to provide compensation for input bias current.



**Fig. 4.41 (b)** Frequency response of practical differentiator

#### 4.18.5 Applications of Differentiators

The differentiators can be used as waveshaping circuits. They can be used to convert triangular waves into square-waves. In fact, since differentiators tend to seek rapid changes in the input signal, they are quite useful as edge detectors in the FM demodulators. The integrators and differentiators may be used in combination with adders and amplifiers to form analog computers.

#### Example 4.17

(a) Design a differentiator using op-amp to differentiate an input signal with  $f_{\text{max}} = 200 \text{ Hz}$  (b) Also draw the output waveforms for a sine-wave and a square-wave input of 1 V peak at 200 Hz.

#### Solution

(a) Given  $f_{\text{max}} = f_a = 200 \text{ Hz}$

$$f_a = \frac{1}{2\pi R_f C_1}$$

Assuming  $C_1 = 0.1\mu\text{F}$ , we get

$$R_f = \frac{1}{2\pi(200)(10^{-7})} = 7.95\text{k}\Omega$$

Let us select  $f_b = 10f_a = 2000\text{Hz}$

$$\text{We know that } f_b = \frac{1}{2\pi R_i C_1}$$

$$\text{Therefore } R_i = \frac{1}{2\pi(2000)(10^{-7})} = 0.795\text{k}\Omega$$

Since  $R_f C_f = R_i C_1$ , we get

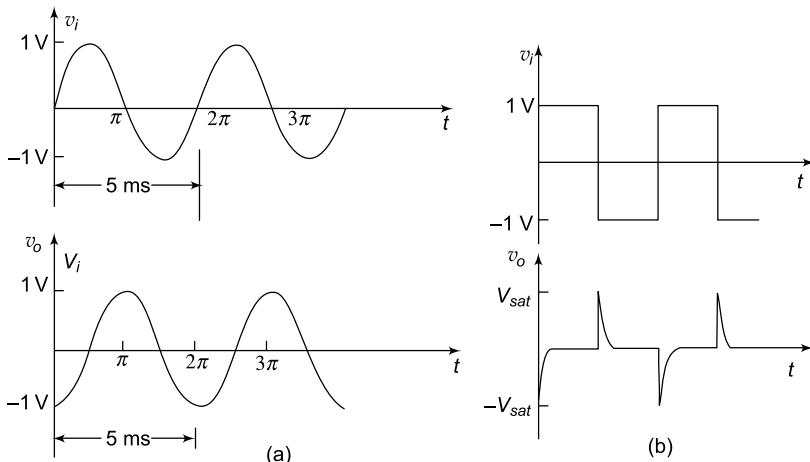
$$C_f = \frac{0.795 \times 10^3 \times 10^{-7}}{7.95 \times 10^3} = 0.01\mu\text{F}$$

- (b) (i) For the sine-wave input  $v_i = 1 \sin 2\pi(200)t$

$$\begin{aligned} \text{We know that } v_o &= -R_f C_1 \frac{dv_i}{dt} \\ &= (7.95\text{k}\Omega)(0.1\mu\text{F}) \frac{d}{dt} [(1\text{V}) \sin(2\pi)(200)t] \\ &= (7.95\text{k}\Omega)(0.1\mu\text{F})(2\pi)(200) \cos(2\pi \times 200t) \\ &= -1 \cos(2\pi \times 200t) \end{aligned}$$

The input and output waveforms are shown in Fig. 4.42(a).

- (ii) For the square-wave input with 1 V peak at 200 Hz, the output waveform will have positive and negative spikes of magnitude  $V_{sat}$  which is approximately  $\pm 13\text{V}$  for  $\pm 15\text{V}$  op-amp power supply. When the input is constant at  $\pm 1\text{V}$ , the differentiated output will be zero. When the input transits between  $\pm 1\text{V}$  level, the differentiated output will be infinite and gets clipped to about  $\pm 13\text{V}$  for a  $\pm 15\text{V}$  op-amp power supply as shown in Fig. 4.42(b).



**Fig. 4.42** (a) Sine-wave input and its differentiated cosine output and (b) Square wave input and its differentiated spike output

#### 4.18.6 Comparison between an Integrator and a Differentiator

Since the process of integration involves the accumulation of signal over time, sudden changes in the signal are suppressed. Therefore, an effective smoothing of the signal is achieved and integration can be viewed as *low-pass filtering*.

Since the process of differentiation involves the identification of sudden changes in the input signal, constant and slowly changing signals are suppressed. Therefore, the differentiator can be viewed as a form of *high-pass filtering*.

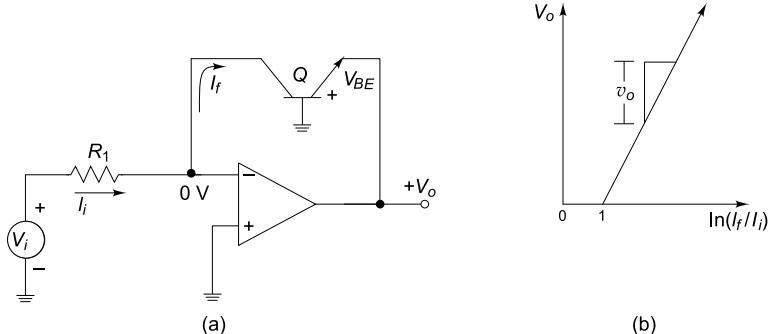
#### 4.19 LOGARITHMIC AMPLIFIER

The response of the op-amp circuit is determined by the choice of elements used in the feedback network of op-amp. When resistors are used, which have a linear relation between the voltage and current, the resulting circuit shows a linear response for the input. On the other hand, when a logarithmic *PN* junction obtained from a transistor is used, the circuit results in a log or antilog response.

The log and antilog responses can be derived from the popular log/antilog ICs such as 755 and 759 from Analog Devices and IC 4127 from Burr-Brown, which are monolithic devices. These logarithmic amplifiers can also be used in applications where significant rise in the dynamic range of certain signal processing systems are desired. There will be no loss in accuracy and resolution, even when the input signal is very small in comparison with the full dynamic range. A typical situation is when the instrument can display a pulse voltage of 10 mV and 10 V with visible precision on the same scale for both the extremes of voltages.

**Basic log circuit** The logarithmic amplifier, called a log-amp or a logger, is basically a current to voltage converter with the transfer characteristics of

$$V_o = V_i \ln \left( I_f / I_i \right)$$



**Fig. 4.43** Logarithmic Amplifier (a) Fundamental circuit and (b) Its logarithmic characteristics

The transistor  $Q$  with its base grounded and its collector at virtual ground is connected in a transdiode configuration.

Its voltage-current relationship is thus defined by

$$I_E = I_S \left[ e^{qV_{BE}/kT} - 1 \right]$$

For the transdiode or grounded base transistor configuration,  $I_E = I_C$  and hence

$$I_C = I_S \left[ e^{qV_{BE}/kT} - 1 \right] \quad (4.32)$$

where  $I_s$  is the emitter saturation current and  $kT/q$  is the volt-temperature equivalent. From Eq. (4.32),

$$e^{qV_{BE}/kT} = \frac{I_C}{I_S} + 1 \approx \frac{I_C}{I_S}, \text{ since } I_C \gg I_S$$

Applying natural log on both sides and rearranging,

$$V_{BE} = \frac{kT}{q} \ln\left(\frac{I_C}{I_S}\right)$$

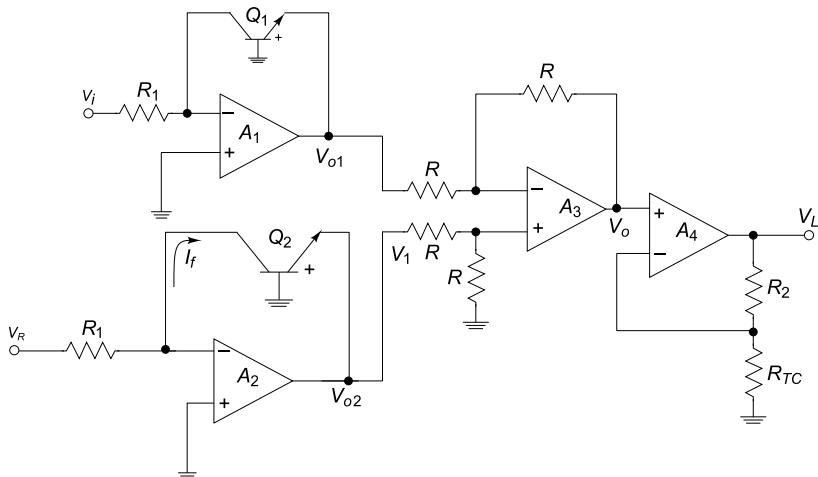
From the figure,  $I_1 = \frac{V_i}{R_i}$  and  $V_{BE} = -V_o$

$$\text{Therefore, } V_o = -\frac{kT}{q} \ln\left(\frac{V_i}{R_i I_S}\right) = -\frac{kT}{q} \ln\left(\frac{V_i}{V_R}\right) \quad (4.33)$$

where  $V_R = R_1 I_S$

Hence, the output voltage is found to be the logarithmic equivalent of input voltage. The emitter saturation current  $I_s$  of the transistor widely varies from one transistor to the other. This problem could be eliminated by employing two transistors  $Q_1$  and  $Q_2$  shown in Fig. 4.44, manufactured under the same process conditions on a single silicon wafer. The input conversion is applied to one log amp and an external reference voltage  $V_R$  is applied to another. By this arrangement, close matching of  $V_R$  and good thermal tracking are achieved. That is,

$$I_{S1} = I_{S2} = I_S$$



**Fig. 4.44** Logarithmic amplifier with compensation of emitter saturation current

From Fig. 4.44, the output  $V_{o1}$  is found as

$$V_{o1} = -\frac{kT}{q} \ln\left(\frac{V_i}{R_1 I_S}\right)$$

and the output  $V_{o2}$  is

$$V_{o2} = -\frac{kT}{q} \ln\left(\frac{V_R}{R_1 I_S}\right)$$

The op-amp  $A_3$  configured as a subtractor will subtract the two inputs, thus providing at the output,

$$\begin{aligned} V_o &= -\frac{kT}{q} \ln\left(\frac{V_R}{R_I I_S}\right) - \left(-\frac{kT}{q} \ln\left(\frac{V_i}{R_I I_S}\right)\right) \\ &= \frac{kT}{q} \ln\left(\frac{V_i}{V_R}\right) \end{aligned} \quad (4.34)$$

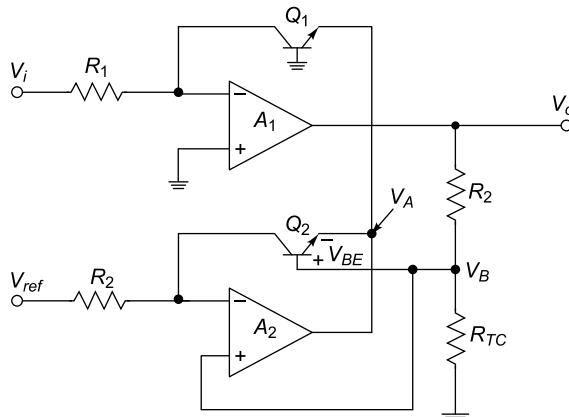
The  $V_R$  is thus set with a single external voltage source. Therefore, the dependence of the circuit on the device and temperature has been removed.

The op-amp  $A_4$  configured as the fourth stage compensates for the effects of temperature with the inclusion of the temperature sensitive resistor  $R_{TC}$  with positive temperature coefficient.

The overall output voltage  $V_L$  is thus

$$V_L = \left(1 + \frac{R_2}{R_{TC}}\right) \frac{kT}{q} \ln\left(\frac{V_i}{V_R}\right) \quad (4.35)$$

Negligible variation in  $V_L$  is achieved with matched coefficients and resistor values. Figure 4.45 shows a logarithmic amplifier using only two op-amps. The output as obtained for the circuit of Fig. 4.44 can be derived for this circuit also.

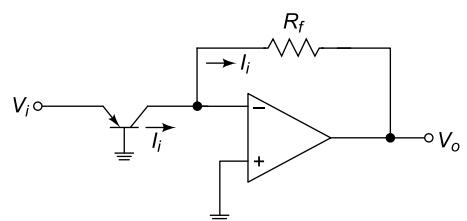


**Fig. 4.45** Logarithmic amplifier using two op-amps

## 4.20 ANTILOGARITHMIC AMPLIFIER

**Basic antilog circuit** Antilog amplifier is a *decoding* circuitry to convert the logarithmically *encoded* signal back to the real world signal levels. A decade change in the input of the logarithmic amplifier causes a one volt change in its output, and conversely, the antilog amplifier creates a decade change in output with respect to a unit change in the input signal.

A basic antilog amplifier circuit is shown in Fig. 4.46. The transistor is connected at the inverting input terminal with its base grounded. It is used to convert the



**Fig. 4.46** Basic antilog amplifier circuit

input voltage into an input current, with a log function. Due to the virtual ground at the inverting input terminal, the log function of input voltage passes through the feedback resistor  $R_f$ . The drop across  $R_f$  produces the output voltage.

The output voltage is derived as  $V_o = -R_f I_i$

Using Eq. (4.32),

$$I_i = I_C = I_S \left( e^{qV_{BE}/kT} \right)$$

Therefore,

$$V_o = -R_f I_S \left( e^{qV_{BE}/kT} \right)$$

The schematic arrangement for the antilog amplifier is shown in Fig. 4.47.

The input for the antilog is fed through the potential divider  $R_2$  and  $R_{TC}$ , to the base of transistor  $Q_2$ . The output of op-amp  $A_2$  is fed back to  $R_1$  at the inverting input of op-amp  $A_1$ . The non-inverting inputs are connected to ground.

$$\text{From the figure, } V_{1BE} = \frac{kT}{q} \ln \left( \frac{V_L}{R_L I_S} \right) \quad (4.36)$$

$$\text{and} \quad V_{2\text{-}BE} = \frac{kT}{q} \ln \left( \frac{V_R}{R_l I_S} \right) \quad (4.37)$$

Since the base of  $Q_1$  is connected to ground,

$$V_A = -V_{1BE} = -\frac{kT}{q} \ln \left( \frac{V_L}{R_L I_S} \right) \quad (4.38)$$

The base voltage of  $Q_2$  is the drop across  $R_{TC}$ , and therefore,

$$V_B = \frac{R_{TC}}{R_2 + R_{TC}} V_i \quad (4.39)$$

The emitter voltage of  $Q_2$  is

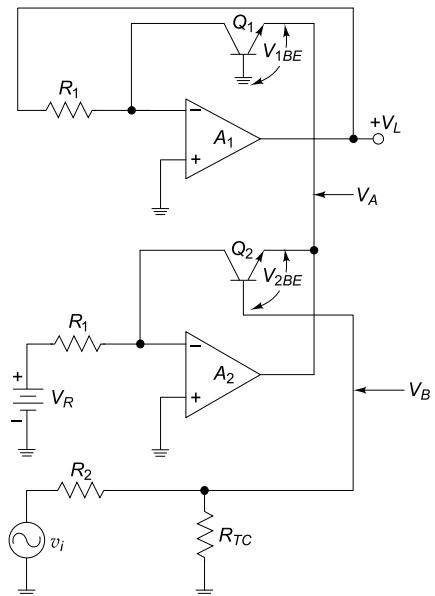
$$V_{Q2E} = V_B + V_{2BE} \quad (4.40)$$

Substituting Eqs. (4.38) and (4.39) in Eq. (4.40), we get

$$V_{Q2E} = \frac{R_{TC}}{R_2 + R_{TC}} V_i - \frac{kT}{q} \ln \left( \frac{V_R}{R_1 I_S} \right)$$

From Fig. 4.44 and Eq. (4.38), we see that  $V_{O2E} = V_A$

$$\text{Therefore, } -\frac{kT}{q} \ln \left( \frac{V_L}{R_l I_S} \right) = \frac{R_{TC}}{R_2 + R_{TC}} V_i - \frac{kT}{q} \ln \left( \frac{V_R}{R_l I_S} \right)$$



**Fig. 4.47** Antilogarithmic amplifier

Rearranging, we get

$$\begin{aligned}\frac{R_{TC}}{R_2 + R_{TC}} V_i &= -\frac{kT}{q} \ln\left(\frac{V_L}{R_l I_S}\right) + \frac{kT}{q} \ln\left(\frac{V_R}{R_l I_S}\right) \\ &= -\frac{kT}{q} \ln\left(\frac{V_L}{V_R}\right)\end{aligned}$$

We know that  $\log_{10} x = 0.4343 \ln x$ .

Therefore,  $-0.4343\left(\frac{q}{kT}\right)\left(\frac{R_{TC}}{R_2 + R_{TC}}\right)V_i = 0.4343 \ln\left(\frac{V_L}{V_R}\right)$

That is,  $-0.4343\left(\frac{q}{kT}\right)\left(\frac{R_{TC}}{R_2 + R_{TC}}\right)V_i = \log_{10}\left(\frac{V_L}{V_R}\right)$

or,  $-KV_i = \log\left(\frac{V_L}{V_R}\right)$

where  $K = 0.4343\left(\frac{q}{kT}\right)\left(\frac{R_{TC}}{R_2 + R_{TC}}\right)$

Hence,  $V_L = V_R 10^{-KV_i}$

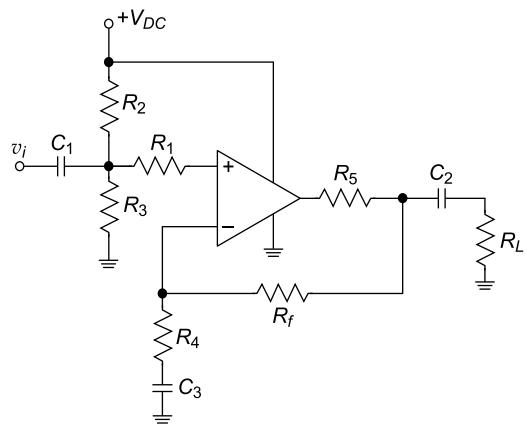
The IC manufacturers provide log/antilog circuits in IC form. A typical device is IC4127 from Burr-Brown which is a hybrid IC using matched transistors to improve the circuit accuracy.

## 4.21 SINGLE POWER SUPPLY OPERATION

All the circuits discussed so far operated using a bipolar power supply, normally  $\pm 15$  V. Sometimes, a situation may arise, where a small amount of analog circuit is used along with a predominantly digital circuit, which operates with a unipolar supply voltage. In such cases, the op-amp can be configured to operate with a  $+30$  V unipolar supply, producing a similar performance.

The basic idea of such a circuit is biasing the input at one-half of the total supply voltage, which can be done with a simple voltage divider. Figure 4.48 shows a non-inverting voltage amplifier circuit using single-supply bias.

A coupling capacitor  $C_1$  is used to isolate the dc biasing potential from the driving stage. The dc gain is set to unity without affecting the ac gain using capacitor  $C_3$ , placed in series with resistor  $R_4$ . Resistors  $R_2$  and  $R_3$  decide the 50% bias point and their parallel combination sets the input impedance also. Resistors  $R_4$  and  $R_5$  are used for preventing unwanted discharge of coupling capacitors  $C_1$  and  $C_2$  into op-amp.



**Fig. 4.48** Non-inverting amplifier with single-supply bias

The voltage gain of the circuit is given by

$$A_{CL} = \left( 1 + \frac{R_f}{R_1} \right)$$

the same as that of dual supply circuit for the frequency range in which capacitive reactances can be neglected.

Figure 4.49 shows the single-supply inverting voltage amplifier. The input resistance is set by  $R_1$ . The closed-loop gain  $A_{CL}$  is given by

$$A_{CL} = \frac{v_o}{v_i} = \frac{-R_f}{R_1}$$

To achieve a relatively flat response over the desired frequency range, the reactances offered by the two capacitors  $C_1$  and  $C_2$  must be less than the respective series resistances  $R_1$  and  $R_L$  at the lowest signal frequency.

As the frequency reduces below a certain range, the series reactance of  $C_1$  increases and the effective gain reduces. At the same time, the series reactance of output capacitance  $C_3$  increases causing a further loss in gain. Hence, both the capacitors decide the low frequency roll-off of the gain. The lowest frequency

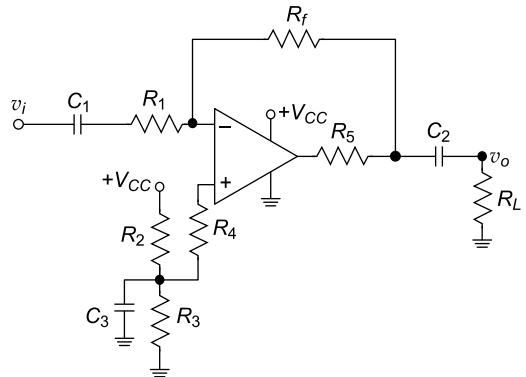
$f_L$  is set by  $f_L \leq \frac{1}{2\pi R_1 C_1}$  and  $f_L \geq \frac{1}{2\pi R_L C_2}$ .

## 4.22 ANALOG COMPUTATION

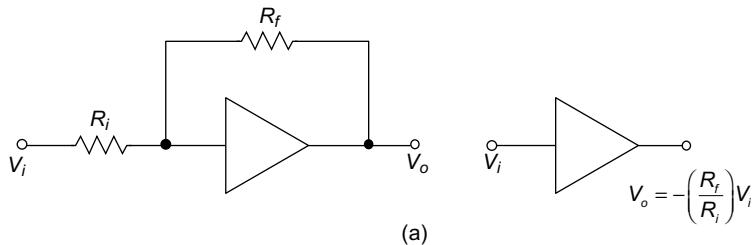
There are two types of computers, namely, digital computers and analog computers. The widely used digital computers employ numerical methods to solve differential equations. The analog computers use a physical model equivalent to the physical system, and the model is subjected to inputs analogous to the inputs of the given physical system. The output obtained is a continuously varying voltage, which is a function of time. Such an analog computer could be designed using electronic circuits and an electronic differential analyser could be used to solve a differential equation depicting any system.

Some of the important mathematical operations to be performed are the linear operations of multiplication by a constant, addition, subtraction and integration. Since these operations are sufficient for the solution of linear differential equations, it is possible to connect various modules of an analog computer for obtaining the solution of differential equations.

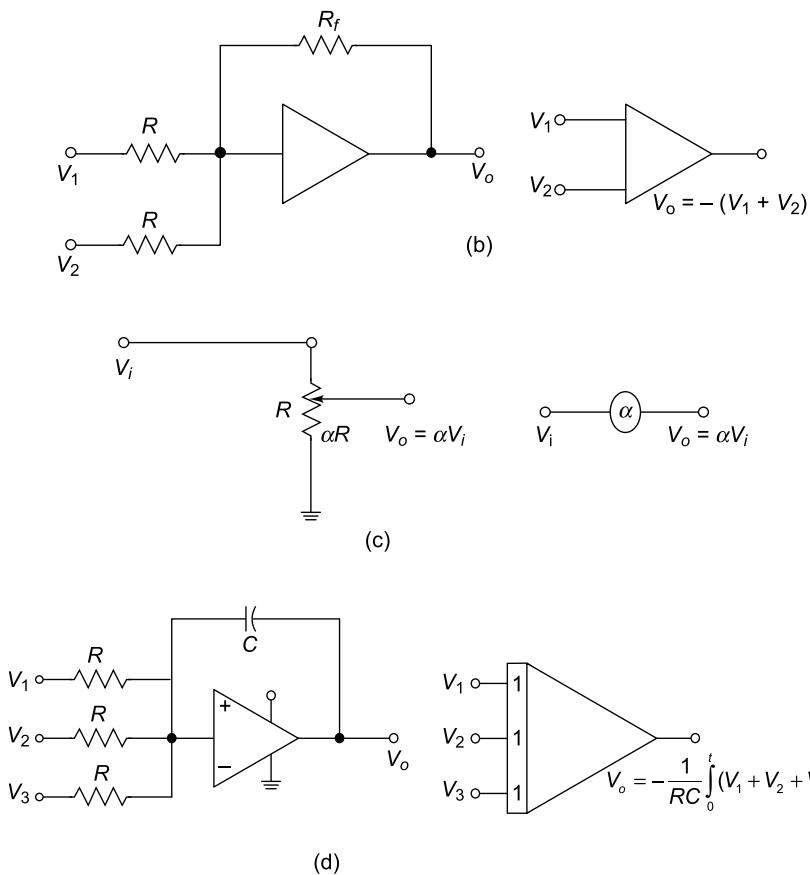
The symbolic representation of a scale changer, summer, potentiometer and summing integrator are provided in Fig. 4.50(a) to (d).



**Fig. 4.49** Inverting amplifier with single-supply bias



(Contd.)



**Fig. 4.50** Symbolic representation used in analog computation methods:  
 (a) Scale changer circuit and its symbol  
 (b) Summer circuit and its symbol  
 (c) Potentiometer and its symbol  
 (d) Summing integrator circuit and its symbol

#### 4.22.1 Linear Ordinary Differential Equation with Constant Coefficients

The modules shown above can be interconnected to solve any linear differential equation. This method is called bootstrap method.

Assume the differential equation to be solved is

$$\frac{d^2y}{dt^2} + ady/dt + by = c(t)$$

with the initial conditions  $y(0) = 0$  and  $dy/dt = 0$ .

Rewriting the equation to keep the highest order derivative on the left hand side and taking all the other terms to the right, we get

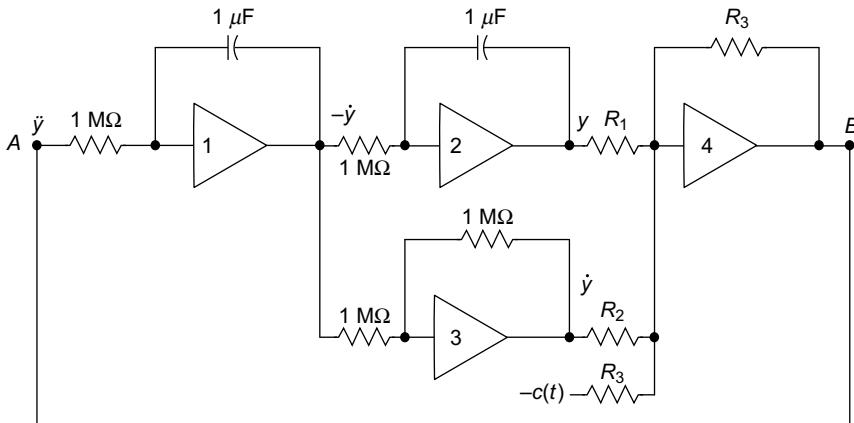
$$\frac{d^2y}{dt^2} = -ady/dt - by + c(t)$$

or,

$$\ddot{y} = -a\dot{y} - by + c(t)$$

Assuming  $d^2y/dt^2$  as available, it can be successively integrated to obtain  $dy/dt$  and  $y$  as shown in Fig. 4.51. At the output of op-amp 4, we have

$$-(R_3/R_1)y - (R_3/R_2)dy/dt + c(t)$$



**Fig. 4.51** Solution of linear ordinary differential equation

Choosing  $R_3/R_1 = b$  and  $R_3/R_2 = a$ , we obtain at the output point  $B$ ,

$$-by - ady/dt + c(t)$$

This is precisely equal to  $d^2y/dt^2$  with which we started. Therefore, the points  $A$  and  $B$  can be connected together. Such a setup solves the differential equation, with the output  $y$  available at the output of amplifier 2.

### Example 4.18

Draw a computer simulation setup for solving the differential equation

$$\ddot{y} + 5.4\dot{y} + 0.58y = c(t).$$

#### Solution

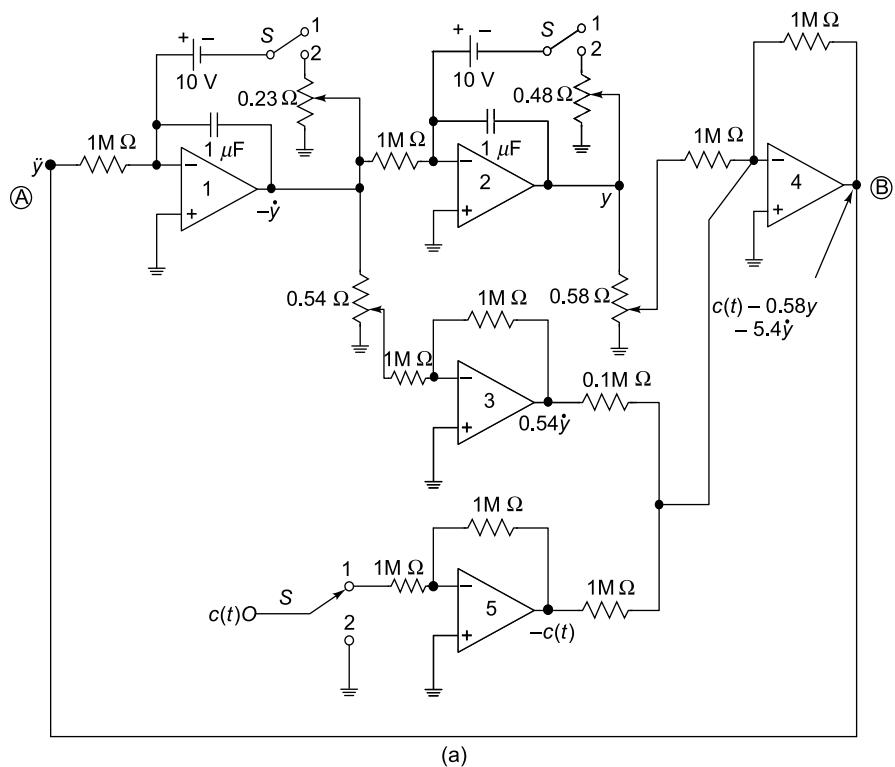
As discussed above, keeping the highest order derivative in the left side and taking over all the other terms to the right side, we get

$$\ddot{y} = -5.4\dot{y} - 0.58y + c(t)$$

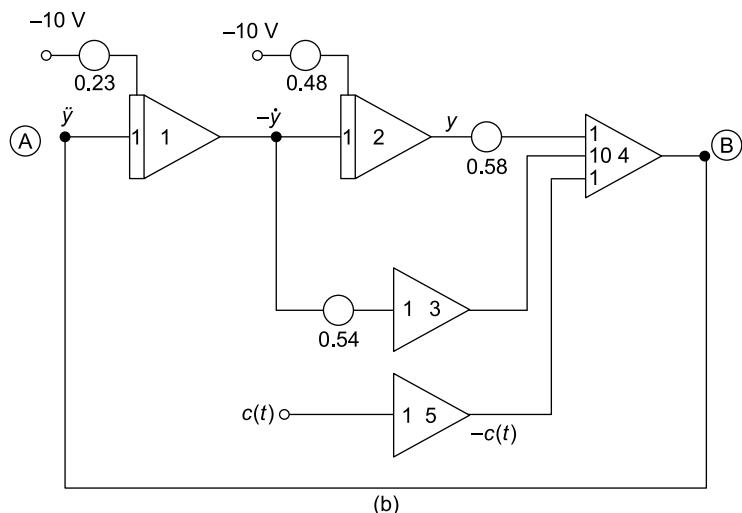
Successively integrating to obtain  $\dot{y}$  and  $y$  as shown in Fig. 4.52, we get the sum at the output of amplifier 4 as

$$-5.4\dot{y} - 0.58y = c(t)$$

Interconnection of the points  $B$  and  $A$  provides the setup for the differential equations. The initial conditions  $y(0) = -4.8$  and  $\dot{y}(0)$  are placed in the computer setup with the reference voltage and potentiometer. Note the polarity of the reference voltage is kept negative to accommodate polarity inversion through the integrator.



(a)



(b)

**Fig. 4.52** (a) Simulation of second order differential equation  
(b) Symbolic diagram

### 4.22.2 Simulation of Simultaneous Equations

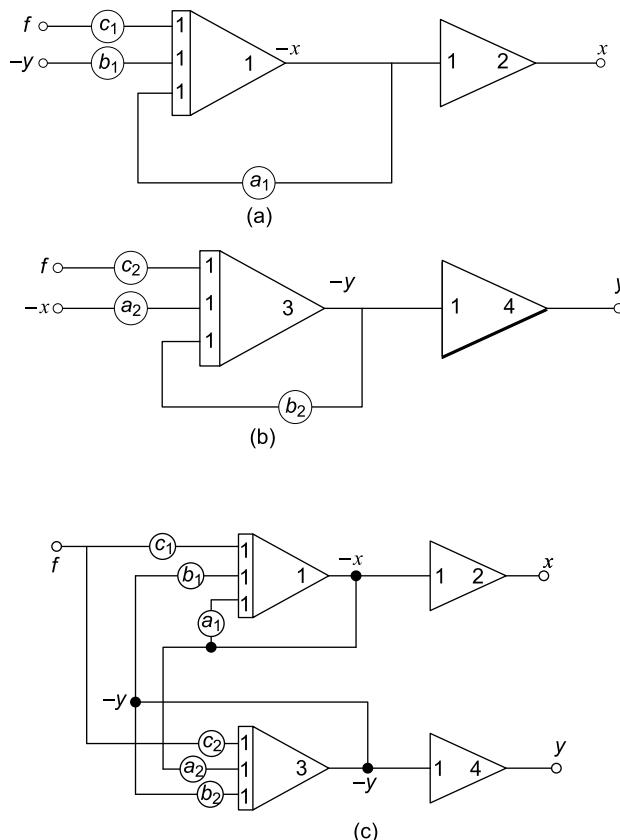
A set of simultaneous equations with two unknown variables can be solved using analog simulation setup. Assuming two first order differential equations given by

$$\frac{dx}{dt} = -a_1x - b_1y + c_1f \quad (4.41)$$

and

$$\frac{dy}{dt} = -a_2x - b_2y + c_2f \quad (4.42)$$

where  $x$  and  $y$  are the two unknown variables,  $f$  is the input and all coefficients are known coefficients. Equations (4.41) and (4.42) can be simulated individually as shown in Fig. 4.53(a) and (b). Then the two individual systems can be interconnected to get the unknown variables  $x$  and  $y$  as represented in Fig. 4.43(c). This simulation procedure can be extended to any number of simultaneous equations with many variables.



**Fig. 4.53** (a) Simulation of simultaneous Eq. (4.41)  
(b) Simulation of simultaneous Eq. (4.42) (c) Final circuit

### 4.22.3 Simulation of Transfer Functions

An important application of analog computers is in the simulation of control systems, which are normally represented as block diagrams, with each block performing a given transfer function. Two popular methods for simulating such circuits are

- (i) using regular computing modules, namely integrators, summers and potentiometers
- (ii) using three terminal  $RC$  networks in the input and feedback paths of high-gain op-amps

The second method is not applicable to many computers since they do not have the flexibility for such designs. As an example, for simulation of transfer function in the first method, consider the transfer function

$$\frac{Y(s)}{X(s)} = \frac{as + d}{s^2 + bs + c} \quad (4.43)$$

where  $Y(s)$  represents the output and  $X(s)$  represents the input.

To obtain the equation for simulation diagram, Eq. (4.43) can be written as

$$(s^2 + bs + c)Y(s) = (as + d)X(s) \quad (4.44)$$

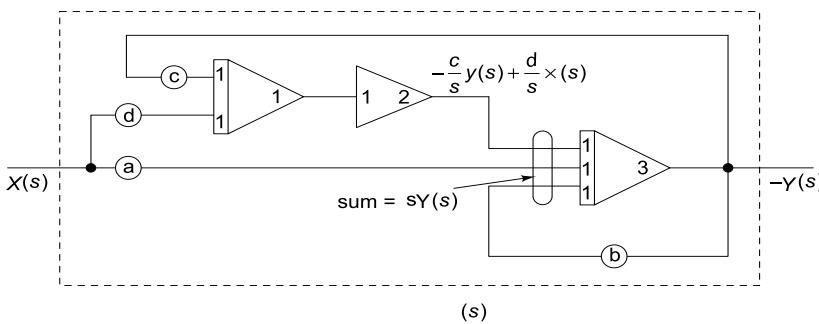
Dividing Eq. (4.44) throughout by  $s$ , we get,

$$sY(s) + bY(s) + \frac{c}{s}Y(s) = aX(s) + \frac{d}{s}X(s) \quad (4.45)$$

Rearranging Eq. (4.45),

$$\begin{aligned} sY(s) &= -bY(s) - \frac{c}{s}Y(s) + aX(s) + \frac{d}{s}X(s) \\ &= -bY(s) + aX(s) + \frac{1}{s}\{-cY(s) + dX(s)\} \end{aligned} \quad (4.46)$$

Using Bootstrapping procedure for the implementation of Eq. (4.46), and assuming the input  $X(s)$  is given at the input and  $-Y(s)$  is available, the computer setup for the simulation of transfer function represented by Eq. (4.43) is shown in Fig. 4.54.



**Fig. 4.54** Simulation of the transfer function of Eq. (4.43)

#### Example 4.19

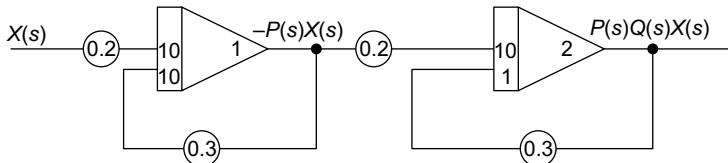
Implement the transfer function  $H(s) = \frac{Y(s)}{X(s)} = \frac{4}{s^2 + 3.3s + 0.9}$ .

**Solution** The above transfer function can be represented after factoring as given by

$$H(s) = \frac{Y(s)}{X(s)} = P(s) \times Q(s) = \frac{2}{(s+3)} \frac{2}{(s+0.3)} \quad (4.47)$$

This transfer function can be realised using the simulation setup shown in Fig. 4.55.

In the example shown above, the initial conditions were assumed zero. It is possible to introduce the initial conditions with the output in the steady-state of the integrator made equal to the initial condition input with its sign inverted.



**Fig. 4.55** Simulation of transfer function of Eq. (4.47)

## SUMMARY

- An op-amp is a high gain and direct coupled amplifier, and the voltage gain can be controlled by the externally connected feedback components.
  - The op-amp can be used in amplifier and signal processing applications involving dc to several MHz of frequency ranges.
  - Sign changer circuit is called phase inverter.
  - Phase shift circuits are constant-delay filters or all-pass filters.
  - Voltage follower circuits offer very high input impedance of the order of  $M\Omega$  and very low output impedance finding use in impedance matching applications.
  - The current gain of an inverting current amplifier is  $A_i = \frac{I_o}{I_i} = 1 + \frac{R_f}{R_i}$ .
  - An ideal current-controlled current source supplies a current  $I_L$  that is a fixed constant  $k$  times the value of an input current as given by  $I_L = kI_i = \left( \frac{R_2}{R_1} + 1 \right) I_i$ .
  - An ideal voltage-controlled current source (VCCS) supplies a current  $I_o$  that is  $k$  times the value of an independent controlling voltage  $V_i$  or  $I_o = \frac{V_i}{R_i} = V_i g_m$ .
  - A current to voltage converter is called transresistance amplifier and its output voltage is  $k$  times the magnitude of an independent  $I_i$  or  $V_o = kI_i = \left( 1 + \frac{R_f}{R_i} \right) V_i = \left( 1 + \frac{R_f}{R_i} \right) I_i R_i$ .
  - The output of a summing amplifier is the sum of all the inputs multiplied by their associated gains as given by
- $$V_o = V_1 A_{V1} + V_2 A_{V2} + V_3 A_{V3} + \dots + V_n A_{Vn}$$
- The output voltage of a subtractor or difference amplifier is proportional to the difference between the two input voltages as given by  $V_o = V_2 - V_1$ .

- The instrumentation amplifier is used for precise amplification of low level output signals where low noise, low thermal and time drifts, high input impedance and accurate closed-loop gains are required. They achieve high CMRR, high gain stability with low temperature coefficient, low dc offset and low output impedance. AD521, AD524 and AD624 manufactured by Analog Devices, and  $\mu$ A 725, ICL 7605, and LH0036 are some of the commercial instrumentation amplifiers.
- AC amplifiers can be realised in two configurations, namely, (i) inverting ac amplifier, and (ii) non-inverting ac amplifier.
- Integrator or integrating amplifier is a circuit in which the output voltage waveform is the time integral of the input voltage waveform as given by  $v_o(t) = -\frac{1}{R_i C_f} \int_0^t v_i(t) dt + v_o(0)$ .
- As the frequency increases, the gain of the integrator decreases.
- The circuit that integrates the input signal twice is called double integrator and output

$$v_o(t) = -\frac{4}{(RC)^2} \int \int v_i(t) dt.$$

- Integrators in combination with summers and amplifiers form analog computers which model a variety of physical systems in real time.
- The integrator circuits are used as wave shaping circuits and used to convert square-waves into triangular waves and ramp generators.
- The differentiator performs the mathematical operation of differentiation, i.e. the output voltage is the differentiation of input voltage as given by  $v_o = -R_f C_1 \frac{dv_i}{dt}$ .
- The differentiator circuits are more susceptible to noise and at high frequencies, the differentiator may become unstable due to very high gain and enter into saturation.
- The differentiators can be used as waveshaping circuits and edge detectors in FM demodulators.
- The process of integration involves the accumulation of signal over time, and hence sudden changes in the signal are suppressed. The process of differentiation involves the identification of sudden changes in the input signal, and hence it can be viewed as high-pass filtering.
- When a logarithmic PN junction is used in the feedback network of op-amp, the circuit exhibits log response.
- The logarithmic amplifier is a current to voltage converter with the transfer characteristics of  $V_o = V_i \ln(I_f/I_i)$ .
- Antilog amplifier is a decoding circuit which converts the logarithmically encoded signal back to the original signal levels as given by  $V_L = V_R 10^{-KV_i}$ .
- Op-amp can operate with a +30V unipolar supply.
- Two types of computers are digital computers and analog computers. The analog computers use a physical model equivalent to the physical system, and the model is subjected to inputs analogous to the inputs of the given physical system.
- The major blocks of an analog computer are scale changer, summer, potentiometer and summing integrator.

## REVIEW QUESTIONS

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1. Explain how a basic inverting amplifier configuration of an op-amp is used as the following circuits:
  - (a) Sign changer
  - (b) Scale changer
  - (c) Phase shift circuit
2. Explain how an op-amp can be used as a sign changer and a scale changer.

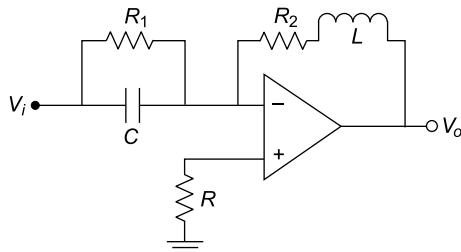
3. For a non-inverting amplifier using op-amp, determine the voltage gain and output voltage. Assume  $R_1 = 2 \text{ k}\Omega$ ,  $R_f = 10 \text{ k}\Omega$  and  $V_i = 5 \text{ mV}$ .
4. Explain the principles of phase-lag and phase-lead circuits.
5. Find the phase angle and the time delay for the circuit shown in Fig. 4.2 (a) for a frequency of 2 kHz, assuming  $R_1 = 10 \text{ k}\Omega$ ,  $R = 22 \text{ k}\Omega$ ,  $R_f = R_1$  and  $C = 1 \text{ nF}$ .
6. What is a dc voltage follower? How will you simulate such a device using op-amp?
7. Why is the voltage follower called the buffer amplifier and an isolation amplifier?
8. An input of 3V is fed to the noninverting terminal of an operational amplifier. The amplifier has  $R_1$  of 10 k $\Omega$  and  $R_f$  of 10 k $\Omega$ . Find the output voltage.
9. Define
 

(a) VCVS	(b) VCSC
(c) CCVS	(d) CCCS
10. Explain how a Voltage Controlled Voltage Source (VCVS) can be connected for non-inverting and inverting configurations using op-amp.
11. What is a current amplifier? Explain the operation of the inverting mode of current amplification using op-amp.
12. What is the effect of saturation during amplification process using op-amp?
13. Explain the operation of Current Controlled Current Source (CCCS) with a neat diagram.
14. What do you mean by floating load? How does the CCCS source current into a floating load?
15. Define transconductance amplifier.
16. Explain a Voltage Controlled Current Amplifier operation for (i) floating load, and (ii) grounded load.
17. Explain the operation of a CCVS with a neat diagram.
18. What is a transresistance amplifier?
19. Differentiate the output gains which are achievable for an inverting CCVS and non-inverting CCVS.
20. Draw the circuit of a voltage to current converter if the load is (i) floating, and (ii) grounded. Is there any limitation on the size of the load when grounded?
21. Explain with a circuit the working of V to I converter with floating load. Where can we use it?
22. What is a voltage to current converter? How can an op-amp be used as a voltage to current converter for grounded load?
23. With a circuit diagram explain the working of a current to voltage converter.
24. Design a non-inverting adder circuit to be used for dc applications with a gain of 10.
25. Draw an op-amp summing amplifier circuit and obtain an expression for the output voltage.
26. The summing amplifier shown in Fig. 4.14 has the inputs,  $V_1 = +1 \text{ V}$ ,  $V_2 = +2 \text{ V}$ ,  $V_3 = +3 \text{ V}$ ,  $R_f = R_1 = R_2 = R_3 = R = 2 \text{ k}\Omega$ , and the supply voltages are  $\pm 15 \text{ V}$ . Determine the output voltage.
27. Draw an op-amp circuit whose output is  $V_1 - V_2 + V_3 - V_4$ .
28. Determine the output voltage  $V_o$  for Fig. 4.11 with three inputs  $V_1 = 5 \text{ mV}$ ,  $V_2 = 2 \text{ mV}$ ,  $V_3 = 3 \text{ mV}$ . Assume  $R_1 = R_2 = R_3 = 2 \text{ k}\Omega$  and  $R_f = 10 \text{ k}\Omega$ .
29. Explain how addition and subtraction may be accomplished using op-amp.
30. Draw the adder-subtractor circuit using op-amp and discuss the operation.
31. What is an instrumentation amplifier? Draw a system whose gain is controlled by a variable resistance?
32. What are the desirable characteristics of an instrumentation amplifier?
33. What is the advantage of having a coupled differential input stage in the instrumentation amplifier?
34. What is the ideal CMRR value of the instrumentation amplifier? Justify your answer.
35. Explain the difference between the dc and ac amplifiers.
36. Explain the operation of inverting and non-inverting amplifiers.
37. How can the input impedance of a non-inverting ac amplifier be varied? What are the salient features of the circuit?

38. What is a peaking amplifier? Explain using a circuit schematic and identify the frequency response characteristics of the circuit.
39. Draw and explain the operations of an ac voltage follower having very high input resistance.
40. What is the basic function of an integrator?
41. Draw the circuit of an Ideal integrator and explain its operation.
42. Explain the summing integrator and double integrator. Derive for their output voltages.
43. Explain and draw the output waveforms of the ideal integrator circuit when the input is (i) sine wave, (ii) square-wave, and (iii) step input.
44. What are the limitations of an ideal integrator?
45. Explain the various errors in an ideal integrator circuit. How are these errors minimised?
46. What practical modifications are needed to be done to the basic integrator and why?
47. How are the initial conditions introduced in an integrator?
48. Explain the practical integrator circuit. Explain its advantages.
49. Derive the frequency response of a practical integrator.
50. Show the response of an integrator for the following inputs: (a) Sine wave input, and (b) square wave input.
51. What are the integrator errors? What are the major sources of such errors? How can they be compensated in practice?
52. What are advantages of the FET input op-amps as related to the integrator errors?
53. Define the integrator *Run*, *Set* and *Hold* modes of a practical integrator circuit using a neat circuit diagram showing the state switches.
54. Draw a typical low leakage integrator reset circuit and explain its operation.
55. For performing differentiation, integrator is preferred to differentiator. Explain.
56. What is the basic function of a differentiator?
57. What are the limitations of an ideal differentiator?
58. Design a differentiator to differentiate an input signal that varies in frequency from 10 Hz to about 10 kHz.
59. What is the function of the capacitor in the basic integrator and differentiator?
60. What is the principle of a differentiator using op-amp? What are its drawbacks?
61. What are the practical modifications needed to be done to the basic differentiator and why?
62. Explain the design procedure of a practical differentiator.
63. Draw the circuit diagram of an op-amp differentiator and derive an expression for the output in terms of the input.
64. Show the response of a differentiator for the following inputs: (a) Sine wave input, and (b) square wave input.
65. Derive the output voltage equation for the following:
  - (i) Integrator,      (ii) Differentiator and      (iii) Summing amplifier
66. Show how an op-amp can be used in the following applications:

(i) Differentiator	(ii) Integrator
--------------------	-----------------
67. Design a differentiator using op-amp to differentiate an input signal with  $f_a = 1 \text{ kHz}$ .
68. Explain the difference between integrator and differentiator. List one application of each.
69. A signal  $V_i$  is applied to the inverting terminal of an op-amp through  $Z_1$  and to the non-inverting terminal through  $Z_2$ . From inverting terminal to ground is an impedance  $Z_3$  and between non-inverting terminal and the output is  $Z_4$ . Derive the expression for the gain.
70. Assuming  $R_1 = 1 \text{ k}\Omega$ ,  $R_f = 10 \text{ k}\Omega$ ,  $C_f = 0.1 \text{ MF}$  in a practical integrator circuit of Fig. 4.33, determine the lower frequency limit of integration and the output response for a sine-wave input of 0.5 V peak at 5 kHz.
71. Using a differential amplifier, explain how to multiply two analog voltages.
72. What are the uses of log and antilog amplifiers?
73. Explain the principle of a basic logarithmic amplifier circuit.
74. How is the current characteristic of a *PN* junction employed in a log amplifier?
75. Draw the circuit diagram of a logarithmic amplifier using op-amps and explain its operation.
76. Explain a basic antilogarithmic amplifier using op-amp.
77. Draw the circuit diagram of an antilogarithmic amplifier using op-amps and explain its operation.
78. Explain the single power supply operation of op-amp.
79. Compare analog computation and digital computation methods.

80. Write detailed notes on any five applications of op-amp.
81. Explain the functions of multipliers, integrators and summers in an analog computer.
82. How are the initial conditions of the variables introduced in analog computer set-up while solving differential equations?
83. Explain how multiplication and integration are realised in analog computer. Also explain why differentiator is not preferred for use in analog computers.
84. Write a short note on the application of analog computers.
85. What are the advantages and disadvantages of the analog computer over the digital computer?
86. Write a short note on the application of analog computers in system design.
87. Draw the circuit diagram to realise the following differential equation  $\frac{d^2x}{dt^2} + \frac{dy}{dt} + z = 30$
88. Draw the simulation set-up for the solution of simultaneous equations given below.
- $$\frac{dx}{dt} = 3x - 4y + 2f$$
- $$\frac{dx}{dt} = -5x - 6y + 3f$$
89. How can the transfer functions be simulated using analog computer structure?
90. Implement the transfer function  $H(s) = \frac{Y(s)}{X(s)} = \frac{4}{s^2 + 2.2s + 0.4}$ .
91. For the phase-lag circuit shown in Fig. 4.2(a), find the phase angle for frequencies (a) 1 kHz, (b) 5 kHz, (c) 10 kHz and (d) 20 kHz. Find the time delay for all these frequencies.
92. Assuming  $R_1 = R_2 = 100 \text{ k}\Omega$  and  $R' = 330 \text{ k}\Omega$  for Fig. 4.18, calculate the value of  $R$  for achieving a gain of 1000.
93. Design a differentiator to produce an output of 6V when the input changes by 2 V in 100  $\mu\text{s}$ .
94. Write the differential equation for the circuit shown in Fig. Q4.94.



**Fig. Q4.94**

# Operational Amplifier— Non-linear Circuits

5

## 5.1 INTRODUCTION

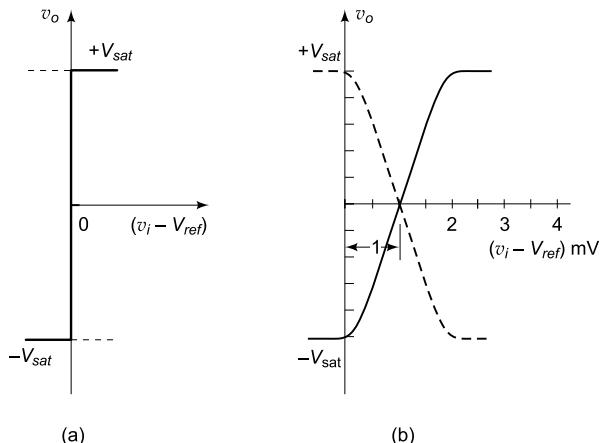
An operational amplifier, in open loop configuration, operates in a non-linear manner. It finds use in many applications in which the output needs to be switched between positive and negative saturation levels. Positive feedback can also be employed in these circuits to obtain hysteresis characteristics, i.e., to provide the upper and lower input voltage levels that trigger the output voltage to change from one saturation level to the other. The non-linear circuits using op-amp, namely comparators, such as zero-crossing detector, amplitude-distribution analyser, pulse-time modulator, window detector, timing marker signal generator, phase detector and Schmitt trigger, and precision half-wave and full-wave rectifiers, analog switches, peak detectors, sample-and-hold circuits, clippers and clampers are discussed in this chapter.

## 5.2 OP-AMP COMPARATORS

An op-amp comparator compares an input voltage signal with a known voltage, called the *reference voltage*. In its simplest form, the comparator consists of an op-amp operated in open-loop, and when fed with two analog inputs, it produces one of the two saturation voltages  $\pm V_{sat}$  ( $\approx \pm V_{CC}$  or  $-V_{EE}$ ) at the output of the op-amp.

The input-output transfer characteristics of an ideal comparator and a practical comparator using op-amp are shown in Fig. 5.1(a) and 5.1(b) respectively. It can be seen from Fig. 5.1(b) that the output state of a practical comparator can change with an input increment of only 2 mV. This width of 2 mV is the region of uncertainty of a practical comparator. Two types of comparators, viz. (i) Non-inverting comparator, and (ii) Inverting comparator can be constructed using op-amps.

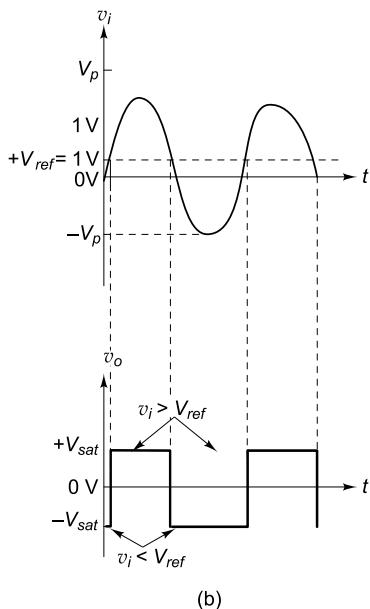
Figure 5.2(a) shows an op-amp configured for use as a non-inverting comparator. A fixed reference voltage  $V_{ref}$  is applied to (-) input and a time-varying signal  $v_i$  is applied to (+) input. When the non-inverting input  $v_i$  is less than the reference voltage  $V_{ref}$ , i.e.  $v_i < V_{ref}$ , the output voltage  $v_o$  is at  $-V_{sat} \equiv -V_{EE}$ . On the other hand, when  $v_i$  is greater than  $V_{ref}$ , i.e.  $v_i > V_{ref}$ , the output voltage  $v_o$  is at  $+V_{sat} \equiv +V_{CC}$ . Thus, the output  $v_o$  changes from one saturation level to another depending on the voltage difference



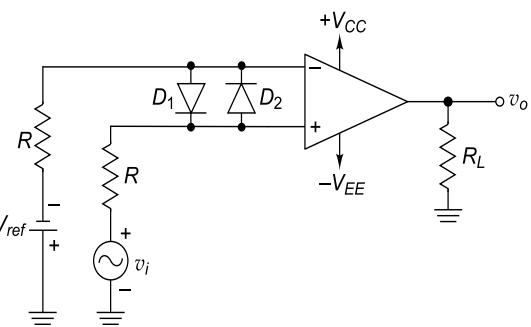
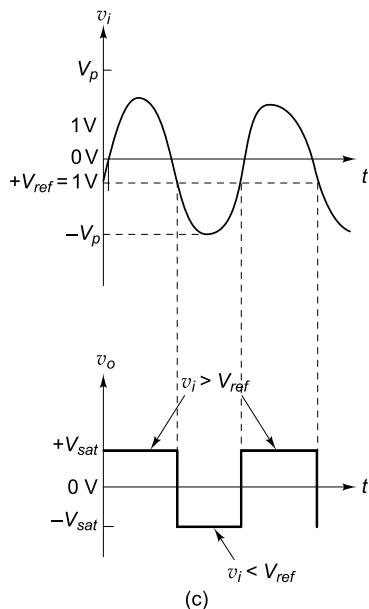
**Fig. 5.1** Transfer characteristics of (a) ideal comparator, and (b) practical comparator

between  $v_i$  and  $V_{ref}$ . Figures 5.2(b) and (c) show the input and output waveforms of the comparator when  $V_{ref}$  is positive and negative respectively.

The diodes  $D_1$  and  $D_2$  are connected to protect the op-amp from excessive input voltages of  $V_{ref}$  as shown in Fig. 5.2(a). In practical circuits,  $V_{ref}$  can be obtained by the use of a  $10\text{ k}\Omega$  potentiometer forming a voltage divider with the use of supply voltages  $+V_{CC}$  and  $-V_{EE}$ , and the wiper connected to ( $-$ ) input terminal of op-amp as shown in Fig. 5.2(d).

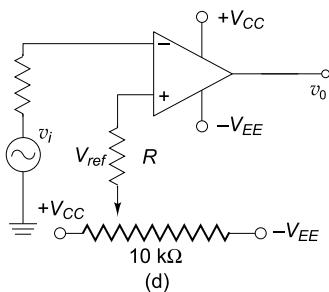


(b)

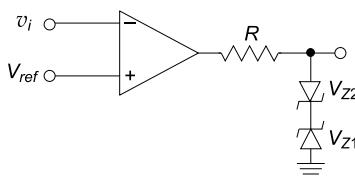
**Fig. 5.2 (a) Non-inverting comparator**

(c)

**Fig. 5.2 (b) Input and output waveforms when  $V_{ref}$  is +ve  
(c) Input and output waveforms when  $V_{ref}$  is -ve**



(d)

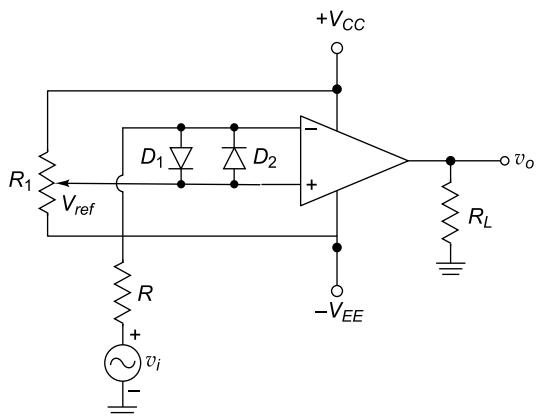


(e)

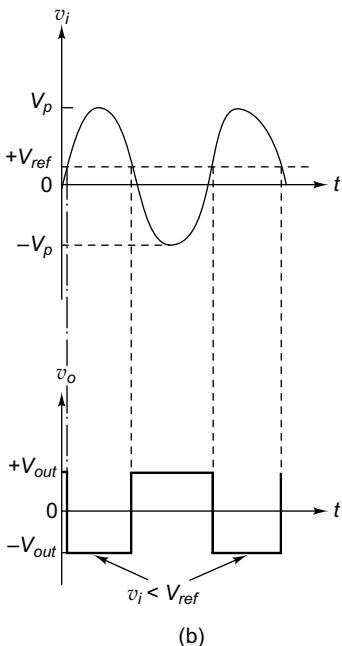
**Fig. 5.2 (d) Comparator with variable  $V_{ref}$  and  
(e) Comparator with Zener diode at the output**

Output voltage level other than  $\pm V_{sat}$  at the output can be obtained by using a resistor  $R$  and back-to-back Zener diodes connected at the output of op-amp as shown in Fig. 5.2(e). Then, the limiting values of voltage  $v_o$  becomes  $(V_{Z1} + V_D)$  and  $-(V_{Z2} + V_D)$ , where  $V_D \approx 0.7\text{V}$ , and  $V_{Z1}$  and  $V_{Z2}$  are the Zener voltages.

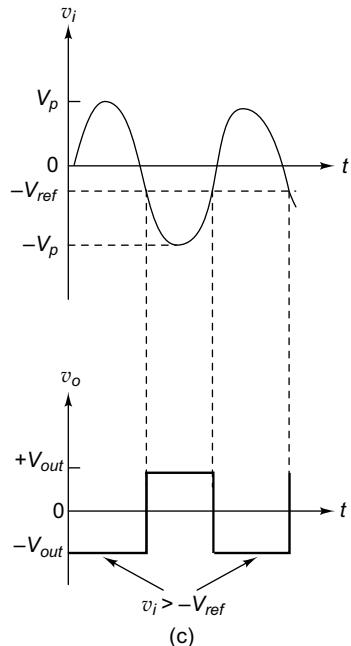
Figure 5.3(a) shows a practical inverting comparator with the reference voltage  $V_{ref}$  applied to (+) input and the voltage signal  $v_i$  applied to the (-) input. For a sinusoidal input signal  $v_i$  and for positive and negative  $V_{ref}$ , the input and output waveforms are as shown in Fig. 5.3(b) and (c) respectively.



**Fig. 5.3 (a) Inverting comparator**



(b)



(c)

**Fig. 5.3 (b) Input and output Waveforms when  $V_{ref}$  is +ve  
(c) Input and output Waveforms when  $V_{ref}$  is -ve**

### Example 5.1

Draw the transfer characteristics of the comparator circuit shown in Fig. 5.4(a), when (a) op-amp is ideal and (b) open-loop gain of op-amp is 100000. Assume  $V_{Z1} = V_{Z2} = 5.5\text{V}$ .

#### Solution

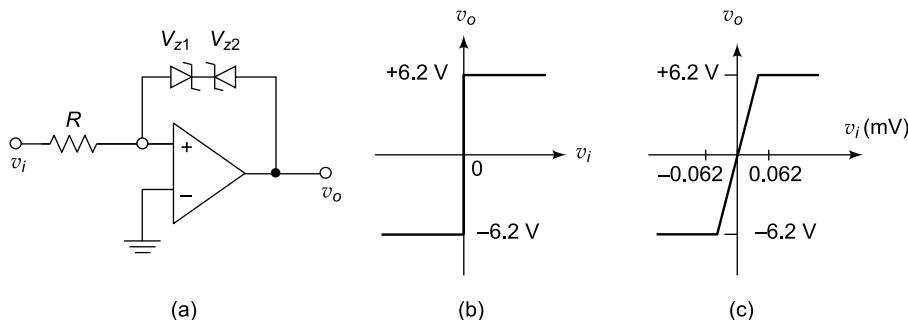
- (a) Since the op-amp is ideal, the open-loop gain  $A_{OL} = \infty$ . Therefore, a very small positive or negative voltage at the input results in  $\pm V_{sat}$  at the output. This causes  $V_{Z1}$  or  $V_{Z2}$  to breakdown,

driving the output  $v_o$  to  $\pm(V_Z + V_D) = \pm(5.5 \text{ V} + 0.7 \text{ V}) = \pm 6.2 \text{ V}$ . The curve shown in Fig. 5.4(b) shows the transfer characteristics of the ideal op-amp.

- (b) Given,  $A_{OL} = 100000$

$$\text{Therefore, } \Delta v_i = \frac{v_o}{A_{OL}} = \frac{6.2}{100000} = 0.062 \text{ mV}$$

That is, the Zener diodes break down at  $\pm 0.062 \text{ mV}$ . The transfer characteristic of such an arrangement is shown in Fig. 5.4(c).



**Fig. 5.4** (a) Circuit of comparator (b) Transfer characteristics for ideal op-amp, (c) Transfer characteristics for op-amp with open loop gain = 100000

**Applications of comparator** The important applications of comparator are:

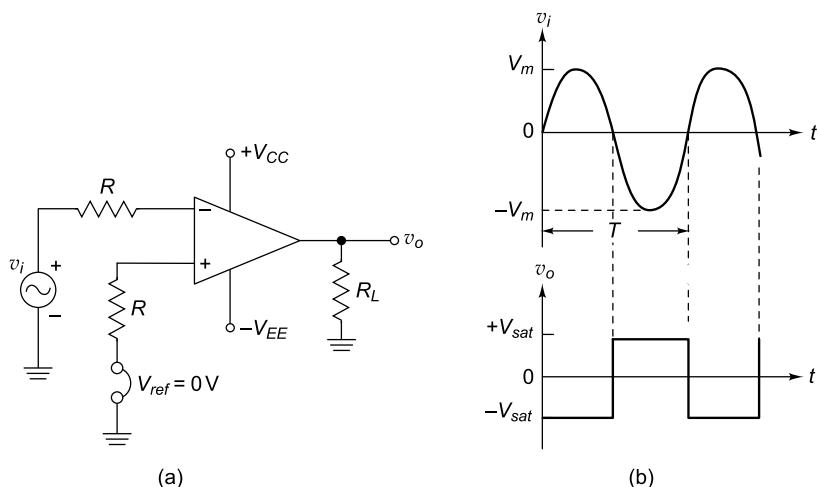
- (i) Zero crossing detector (sine wave to square wave converter)
- (ii) Amplitude distribution analyser
- (iii) Pulse-time modulator
- (iv) Window detector
- (v) Timing marker signal generator
- (vi) Phase detector

The circuit arrangement and operation of these systems are discussed briefly in the following sections.

### 5.2.1 Zero Crossing Detector (Sine Wave to Square Wave Converter)

The comparator connected as a zero crossing detector is shown in Fig. 5.5(a). The reference voltage input  $V_{ref}$  is set to zero and the sinusoidal input  $v_i$  is applied to (-) input. The output waveform  $v_o$  switches between positive and negative saturation levels as shown in Fig. 5.5(b), when the input signal  $v_i$  passes through zero in the negative and the positive directions respectively.

In some applications, the input  $v_i$  may be a slowly varying signal, consuming more time to cross 0 V. Thus switching of  $v_o$  between saturation voltages may take longer time. Conversely, due to noise at the input terminals of op-amp, output  $v_o$  may unnecessarily switch between the saturation voltages  $+V_{sat}$  and  $-V_{sat}$ . Both these problems are overcome with the use of *regenerative* or *positive feedback* in the circuit of Schmitt trigger discussed in Section 5.3.



**Fig. 5.5** (a) Zero crossing detector (b) Input and output waveforms

## 5.2.2 Amplitude Distribution Analyser

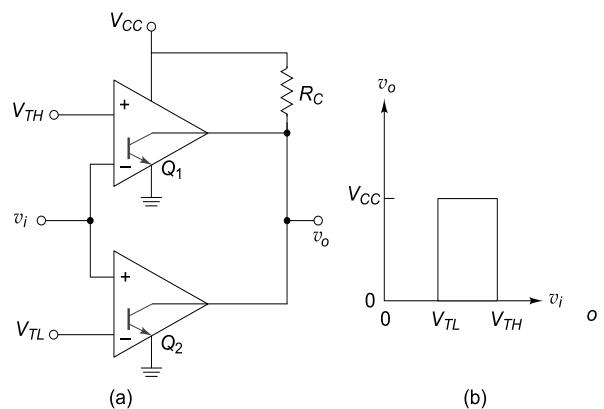
The comparator can be used to analyse the amplitude distribution of the noise that is developed in an active device. Figure 5.5(a) can be employed for amplitude distribution analysis with the positive and negative saturation output voltage levels set for +12 V and 0 V. The voltage spectrum of the noise pulses can be produced by connecting the reference voltage  $V_{ref}$  with a set value and the noise signal is connected as input  $v_i$  to the inverting input of the comparator. When  $v_i > V_{ref}$ , the output reaches the negative saturation of 0 V and when  $v_i < V_{ref}$ , the output reaches the positive saturation of +12 V. A dc meter can be used to measure the average value of the output square voltage. For any other reference voltage  $V_{ref}$ , the dc meter reading indicates the probability that the amplitude of the noise is greater than  $V_{ref}$ . In this manner, the cumulative amplitude probability distribution of the noise can be obtained by recording the meter readings against the  $V_{ref}$  voltage levels.

## 5.2.3 Pulse-time Modulator

A pulse-time modulator for a communication system can be constructed by connecting the modulating pulse signal as  $V_{ref}$  and a periodic sweep waveform applied to the other input as  $v_i$  in Fig. 5.5(a). The relative spacing between the successive output pulses indicates the input information.

## 5.2.4 Window Detector

The *window detector*, also called a *window comparator* identifies an unknown input voltage falling within two threshold voltage levels. The span of threshold voltage difference is called the *window*. Figure 5.6(a) shows a set of voltage comparators connected



**Fig. 5.6** (a) Window detector (b) Its voltage transfer characteristics

to form a window detector. The threshold voltage levels are  $V_{TH}$  and  $V_{TL}$  for the upper limit and lower limit of the window respectively. Referring to Fig. 5.6(a), when  $V_{TL} < v_i < V_{TH}$ , both the transistors  $Q_1$  and  $Q_2$  are OFF, and the pull-up resistor  $R_C$  pulls the output high, thus producing a high output voltage. When the voltage  $v_i$  falls outside the range, that is when  $v_i > V_{TH}$ ,  $Q_1$  is ON and if  $v_i < V_{TL}$ ,  $Q_2$  is ON. Either of these conditions makes the output zero. If the resistor  $R_C$  is replaced by an LED in series with current limiting resistors, the LED will glow when the input voltage  $v_i$  falls outside the windows. Figure 5.6(b) shows the voltage transfer characteristics of the window detector circuit.

A three level detector/comparator with LED indicators is shown in Fig. 5.7. The three LEDs are connected to the output of comparators in series with appropriate current limiting resistors. The LEDs will glow when the input  $v_i$  falls within the respective windows. Alternately, placing an inverter between the comparator and LED-resistor combination makes the LEDs glow when  $v_i$  falls outside the corresponding windows. Table 5.1 shows the status of LEDs for different input voltage ranges with 6 V connected as  $+V_{CC}$ .

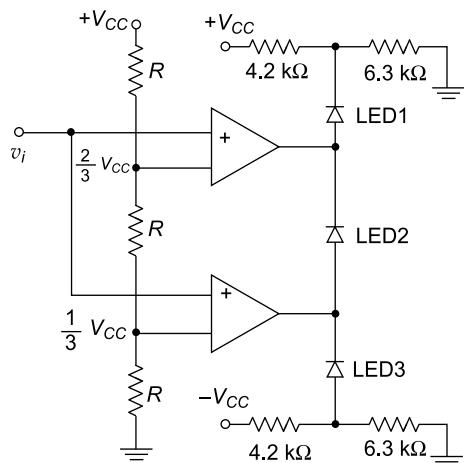
**Table 5.1** Three level comparator

Input (Volts)	LED3	LED2	LED1
Less than 2 V	ON	OFF	OFF
Less than 4 V and more than 2 V	OFF	ON	OFF
More than 4 V	OFF	OFF	ON

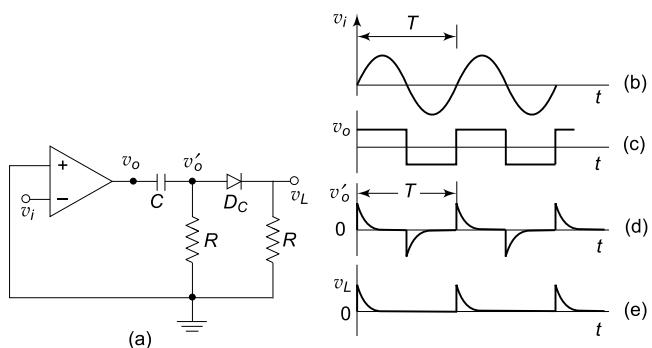
The window detectors find applications in production line testing for sorting-out circuits, raising industrial alarms and level detectors. They are available as individual IC modules, such as 4115/04 of Burr-Brown and LTC1040 of Linear technology.

### 5.2.5 Timing Marker Signal Generator

A timing marker signal generator using a sine wave is shown in Fig. 5.8(a). The input signal  $v_i$  and the output signal of the zero crossing detector are shown in Fig. 5.8(b) and (c). The output  $v_o$  of the zero crossing detector circuit is applied to the differentiator formed by an RC circuit. The differentiated signal  $v'_o$  is shown in Fig. 5.8(d). The value of  $RC$  is made much less than the time period  $T$  of the input signal  $v_i$ . This helps in generating steep pulse spikes which can act as time markers. The diode  $D_C$  clips



**Fig. 5.7** Three level comparator



**Fig. 5.8** (a) Time marker signal generator circuit  
(b) Input waveform, (c) Output  $v_o$  of op-amp  
(d) Differentiated output  $v'_o$   
(e) Pulses across  $R$ ,  $v_L$

off the negative portion of the waveform. The time marking signal output  $v_L$  is shown in Fig. 5.8(e). The frequency of the sinusoidal signal  $v_i$  determines the pulse spacing interval  $T$  and the frequency of time marking.

The time marker signal is used as trigger signals for monoshot multivibrator, SCR circuit and sweep voltage generator of CRT.

### 5.2.6 Phase Detector

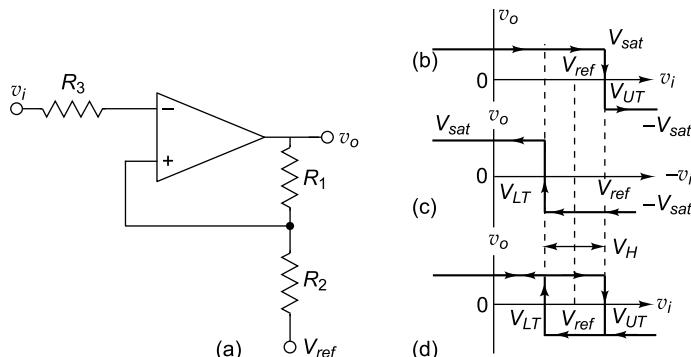
The phase angle between two time varying voltages can be measured using the circuit of Fig. 5.8(a). The two voltages are converted into spikes using the time marker circuit shown in Fig. 5.8(e). The time interval between the pulse spikes is then measured, and it is an indication of the phase difference between the two signals. The phase angle difference from  $0^\circ$  to  $360^\circ$  can be detected using such a circuit.

## 5.3 SCHMITT TRIGGER

The basic comparator is used in open-loop mode. Since the open loop gain of the op-amp is very large, false triggering at the output can occur even due to a few tenths of millivolts peak of the input or less. When the input changes slowly as compared to the output, noise is coupled from the output of the comparator back to the input. The comparator circuit designed with a positive feedback to avoid such an unwanted triggering is called the *Schmitt Trigger* or the *Regenerative Comparator*.

The positive feedback makes the gain very large and the transfer curve of the comparator becomes closer to the ideal curve as shown in Fig. 5.4(b). Theoretically, if the loop gain  $\beta A_{OL}$  is adjusted to be unity, the gain with feedback  $A_{vf}$  becomes infinite. This results in an abrupt transition (zero rise and fall timings) between the two saturation voltages. But, in practical circuits, the loop gain may not be maintained exactly equal to unity for a long time. This may be due to supply voltage or temperature variations. Hence, a value greater than one is chosen normally. This gives an output waveform exhibiting the characteristics of *hysteresis* or *backlash*.

Figure 5.9(a) shows the regenerative comparator or the inverting Schmitt Trigger. It consists of an inverting comparator provided with positive feedback. The input voltage to be wave-shaped is applied to the (−) input terminal and the feedback voltage is applied to the (+) input terminal. The input voltage  $v_i$  triggers the output  $v_o$  every time it crosses certain voltage levels. These voltage levels are called Upper Threshold Voltage  $V_{UT}$  and Lower Threshold Voltage  $V_{LT}$ .



**Fig. 5.9** (a) Inverting Schmitt Trigger circuit (b), (c) and (d) Transfer Characteristics of Schmitt Trigger

The difference between the two threshold voltages  $V_{UT}$  and  $V_{LT}$  is called the *hysteresis voltage*,  $V_H = V_{UT} - V_{LT}$ . The voltage span of hysteresis is set to be greater than the peak-to-peak noise voltage. Therefore, there will not be any incorrect output variations due to noise signals.

The threshold voltage values can be obtained as follows. Suppose the output is at positive saturation with  $v_o = +V_{sat}$ , then the voltage at (+) input terminal is given by

$$V_{ref} + \frac{R_2}{R_1 + R_2} (V_{sat} - V_{ref}) = V_{UT} \quad (5.1)$$

where  $V_{UT}$  is the upper threshold voltage. The output voltage  $v_o$  remains constant at  $+V_{sat}$  as long as  $v_i$  is less than  $V_{UT}$ . When  $v_i$  is just slightly more positive than  $V_{UT}$ , the output  $v_o$  switches from  $+V_{sat}$  to  $-V_{sat}$  and remains at the same level, as long as  $v_i$  is greater than  $V_{UT}$  as shown in Fig. 5.9(b). When  $V_o = -V_{sat}$ , the voltage at the (+) input terminal is given by

$$V_{ref} - \frac{R_2}{R_1 + R_2} (V_{sat} + V_{ref}) = V_{LT} \quad (5.2)$$

This voltage is identified as Lower Threshold Voltage  $V_{LT}$ . The input voltage  $v_i$  must be slightly more negative than  $V_{LT}$  to switch  $v_o$  from  $-V_{sat}$  to  $+V_{sat}$  as shown in Fig. 5.9(c). The complete transfer characteristics of the regenerative action are shown in Fig. 5.9(d). The *hysteresis width*  $V_H$  is the difference between the two threshold voltages. That is,

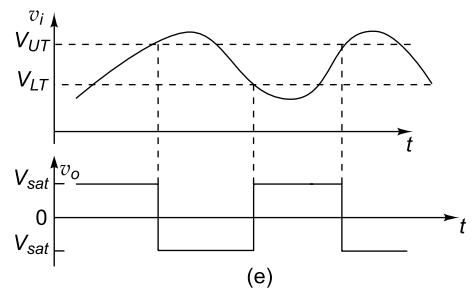
$$V_H = V_{UT} - V_{LT} = \frac{2R_2 V_{sat}}{R_1 + R_2} \quad (5.3)$$

It can be observed from the above equation that  $V_H$  is independent of  $V_{ref}$ . Resistor  $R_3$  of Fig. 5.9(a) is selected such that  $R_3 = R_1 \parallel R_2$ . This compensates for the variations in input bias current of the op-amp.

A *non-inverting Schmitt trigger* is constructed in the same manner with a modification. The signal  $v_i$  and  $V_{ref}$  are interchanged between (-) and (+) input terminals of op-amp. If  $V_{ref}$  in Fig. 5.9(a) is made equal to 0 V, the upper and lower threshold voltage levels are

$$V_{UT} = -V_{LT} = \frac{R_2}{R_1 + R_2} V_{sat} \quad (5.4)$$

When an input sinusoidal signal of frequency  $f$  is applied to such a comparator, a symmetrical square wave is produced at the output as shown in Fig 5.9(e). Hence, the most important application of the Schmitt trigger circuit is to convert a slowly varying input voltage into a square wave output. Hence, the circuit is also called a *squarer*.



**Fig. 5.9 (e)** Schmitt Trigger output when used as a squarer

### Example 5.2

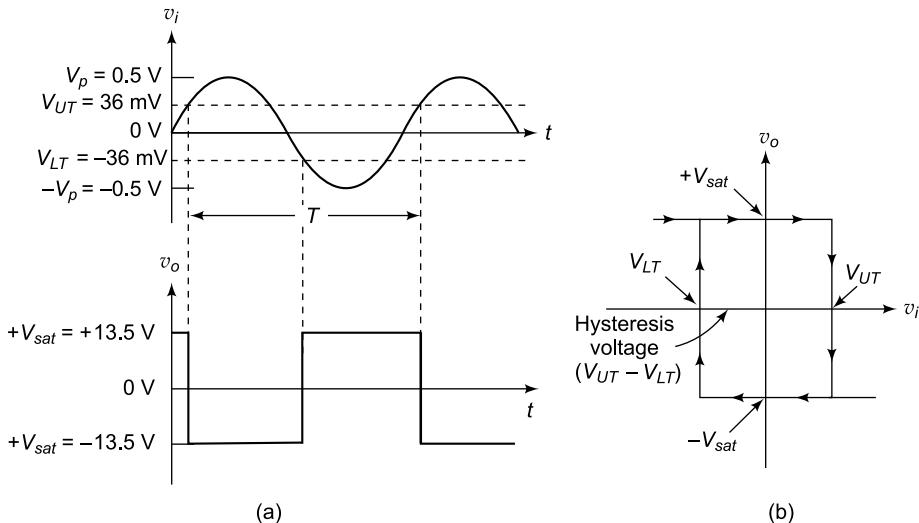
Refer to the circuit of Fig. 5.9(a),  $R_1 = 56 \text{ k}\Omega$ ,  $R_2 = 150 \Omega$ ,  $v_i = 1 \text{ V}_{pp}$  sine wave of frequency 50 Hz,  $V_{ref} = 0 \text{ V}$  and op-amp 741 is used with supply voltages of  $\pm 15 \text{ V}$  and the saturation voltages are  $\pm 13.5 \text{ V}$ . Determine the threshold voltages  $V_{UT}$  and  $V_{LT}$  and draw the input and output waveforms of Schmitt trigger. Also, plot the hysteresis voltage curve.

**Solution** We know,  $V_{UT} = -V_{LT} = \frac{R_2}{R_1 + R_2} V_{sat}$

$$\text{Therefore, } V_{UT} = \frac{150}{56150} \times (+13.5) \approx 36 \text{ mV}$$

$$V_{LT} = -V_{UT} = -36 \text{ mV}$$

Figures 5.10(a) and (b) show the input and output waveforms of the Schmitt trigger and the hysteresis voltage curve respectively.



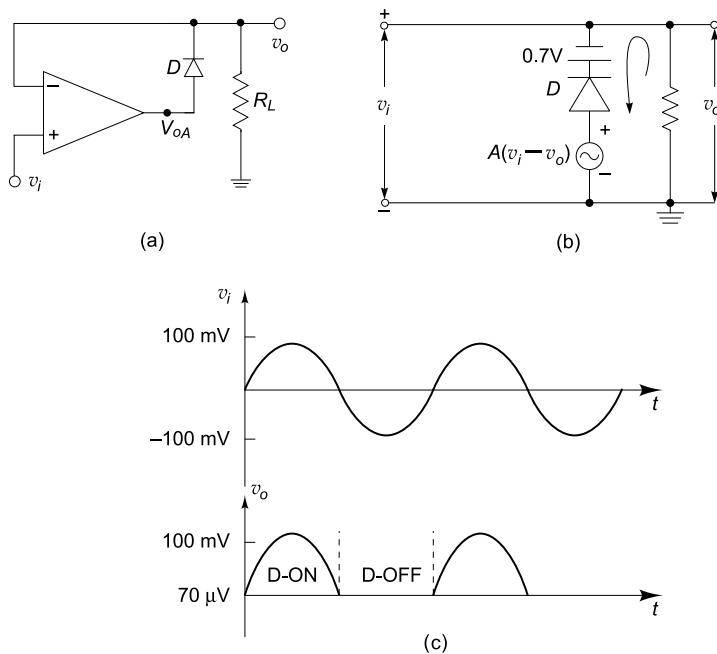
**Fig. 5.10** (a) Input and Output waveforms of Schmitt Trigger  
(b) Output  $v_o$  versus  $v_i$  plot of the hysteresis voltage

## 5.4 PRECISION RECTIFIER

The signal processing applications with very low voltage, current and power levels require rectifier circuits. The ordinary diodes cannot rectify voltages below the *cut-in* voltage of the diode. A circuit which can act as an *ideal diode* or *precision signal-processing rectifier circuit* for rectifying voltages which are below the level of *cut-in voltage* of the diode can be designed by placing the diode in the feedback loop of an op-amp.

### 5.4.1 Precision Diodes

Figure 5.11(a) shows the arrangement of a precision diode. It is a single diode arrangement and functions as a non-inverting precision half-wave rectifier circuit. It is called super diode, since it provides a nearly perfect rectifier. If  $v_i$  in the circuit of Fig. 5.11(a) is positive, the op-amp output  $V_{O4}$  also becomes positive. Then the closed loop condition is achieved for the op-amp and the output voltage  $v_o = v_i$ . When  $v_i < 0$ , the voltage  $V_{O4}$  becomes negative and the diode is reverse biased. The loop is then broken and the output  $v_o = 0$ .



**Fig. 5.11** (a) Precision diode (b) Equivalent circuit (c) Input and output waveforms

Consider the open loop gain \$A\_{OL}\$ of the op-amp is approximately \$10^4\$ and the cut-in voltage \$V\_\gamma\$ for silicon diode is \$\approx 0.7\text{ V}\$. When the input voltage \$v\_i > \frac{V\_\gamma}{A\_{OL}}\$, the output of the op-amp \$V\_{OA}\$ exceeds \$V\_\gamma\$ and the diode \$D\$ conducts. Then the circuit acts like a voltage follower for input voltage level \$v\_i > \frac{V\_\gamma}{A\_{OL}}\$ (i.e. when \$v\_i > \frac{0.7}{10^4} = 70\mu\text{V}\$) and the output voltage \$v\_o\$ follows the input voltage during the positive half cycle for input voltages higher than \$70\mu\text{V}\$ as shown in Fig. 5.11(c). When \$v\_i\$ is negative or less than \$\frac{V\_\gamma}{A\_{OL}}\$, the output of op-amp \$V\_{OA}\$ becomes negative and the diode becomes reverse biased. The loop is then broken and the op-amp swings down to negative saturation. However, the output terminal is now isolated from both the input signal and the output of the op-amp and thus \$v\_o = 0\$. No current is then delivered to the load \$R\_L\$ except for the small bias current of the op-amp and the reverse saturation current of the diode.

From the equivalent circuit shown in Fig. 5.11(b), we have

$$v_o + 0.7 - A(v_i - v_o) = 0$$

$$v_o + Av_o = Av_i - 0.7$$

$$\text{Therefore, } v_o = \frac{A}{1+A}v_i - \frac{0.7}{1+A}$$

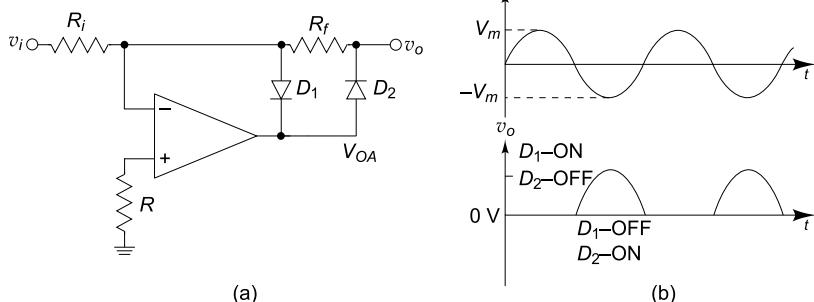
As \$A\$ is large, \$v\_o \approx v\_i\$.

This circuit is an example of a non-linear circuit, in which linear operation is achieved over the region ( $v_i > 0$ ) and non-linear operation is achieved over the remaining region ( $v_i < 0$ ). Since the output swings to negative saturation level when  $v_i < 0$ , the circuit is basically of saturating form. Thus the frequency response is also limited. The precision diodes are used in Half-wave rectifier, Full-wave rectifier, Peak value detector, Clipper and Clamper circuits.

It can be observed that the precision diode shown in Fig. 5.11(a) operates in the first quadrant with  $v_i > 0$  and  $v_o > 0$ . The operation in third quadrant can be achieved by connecting the diode in reverse direction.

### 5.4.2 Half-wave Rectifier

A non-saturating half-wave precision rectifier circuit is shown in Fig. 5.12(a). When  $v_i > 0$ , the voltage at the inverting input becomes positive, forcing the output  $V_{OA}$  to go negative. This results in forward biasing the diode  $D_1$  and the op-amp output drops only by  $\approx 0.7$  V below the inverting input voltage. Diode  $D_2$  becomes reverse-biased. The output voltage  $v_o$  is zero since no current flows in the feedback circuit through  $R_f$ . Hence, the output  $v_o$  is zero when the input is positive. When  $v_i < 0$ , the op-amp output  $V_{OA}$  becomes positive, forward biasing the diode  $D_2$  and reverse biasing the diode  $D_1$ . The circuit then acts like an inverting amplifier circuit with a non-linear diode in the forward path. The gain of the circuit is unity when  $R_f = R_i$ .



**Fig. 5.12** (a) Non-saturating half-wave precision rectifier circuit  
(b) Input and output waveforms

The circuit operation can mathematically be expressed as

$$v_o = 0 \text{ when } v_i > 0$$

and 
$$v_o = -\frac{R_f}{R_i} v_i \text{ for } v_i < 0$$

The voltage  $V_{OA}$  at the op-amp output is

$$V_{OA} \approx -0.7 \text{ V for } v_i > 0$$

and 
$$V_{OA} \approx \frac{R_f}{R_i} v_i + 0.7 \text{ V for } v_i < 0.$$

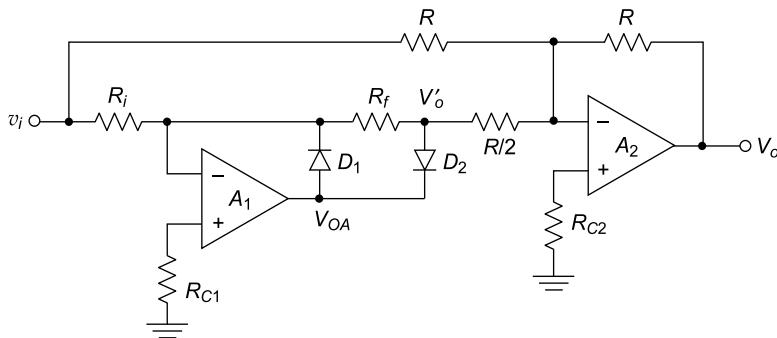
The input and output waveforms are shown in Fig. 5.12(b). The op-amp shown in the circuit must be a high-speed op-amp. This accommodates the abrupt changes in the value of  $V_{OA}$  when  $v_i$  changes sign and improves the frequency response characteristics of the circuit.

The advantages of half-wave rectifier are (i) it is a precision half-wave rectifier, and (ii) it is a non-saturating one.

The inverting characteristics of the output  $v_o$  can be circumvented by the use of an additional inversion for achieving a positive output.

### 5.4.3 Full-wave Rectifier

The full-wave rectifier circuit commonly called an *absolute value circuit* is shown in Fig. 5.13(a). The first part of the total circuit is a half-wave rectifier circuit considered earlier in Fig. 5.12(a). The second part of the circuit is an inverting summing circuit.



**Fig. 5.13 (a)** Active non-saturation full-wave rectifier circuit

For positive input voltage  $v_i > 0$  V and assuming that  $R_f = R_i = R$ , the output voltage  $V'_o = -v_i$ . The voltage  $V'_o$  appears as (−) input to the summing op-amp circuit formed by  $A_2$ . The gain for the input  $V'_o$ , i.e.  $\frac{-R}{(R/2)}$  is shown in Fig. 5.13(a). The input  $v_i$  also appears as an input to the summing amplifier. Then, the net output is

$$\begin{aligned} V_o &= -v_i - 2V'_o \\ &= -v_i - 2(-v_i) = v_i \end{aligned}$$

Since  $v_i > 0$  V,  $V_o$  will be positive, with its input-output characteristics in first quadrant. For negative input  $v_i < 0$  V, the output  $V'_o$  of the first part of rectifier circuit is zero. Thus, one input to the summing circuit has a value of zero. However,  $v_i$  is also applied as an input to the summer circuit formed by the op-amp  $A_2$ . The gain for this input is  $\left(-\frac{R}{R}\right) = -1$ , and hence the output is  $V_o = -v_i$ . Since  $v_i$  is negative,

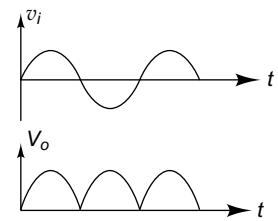
$V_o$  will be inverted and will thus be positive. This corresponds to the second quadrant operation of the circuit.

To summarise the operation of the circuit,

$$V_o = v_i \text{ when } v_i < 0 \text{ V and}$$

$$V_o = v_i \text{ for } v_i > 0 \text{ V, and hence } V_o = |v_i|$$

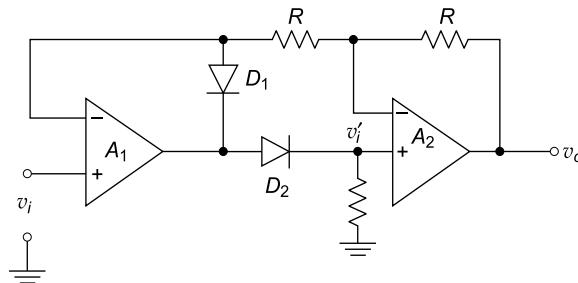
It can be observed that this circuit is of non-saturating form. The input and output waveforms are shown in Fig. 5.13(b).



**Fig. 5.13 (b)** Input and output waveforms

#### 5.4.4 Absolute Value Circuit

Figure 5.13(c) shows a high-input impedance absolute value circuit. It employs as voltage follower realised by  $A_1$  and unity gain amplifier achieved by the op-amp  $A_2$ .



**Fig. 5.13 (c)** High-input impedance absolute value circuit

When,  $v_i > 0$ ,  $D_2$  conducts and  $D_1$  remains off. The voltage  $v'_i$  at the non-inverting input of  $A_2$ , appearing as  $v_o = v_i$ . When  $v_i < 0$ ,  $D_1$  conducts and  $D_2$  gets off. Then, the op-amp  $A_1$  acts as a unity gain follower, and this passes the signal to the inverting unity gain circuit formed by  $A_2$ . Hence, the signal  $v_o = v_i$  is realised during both the positive and negative half-cycles.

### 5.5 ANALOG SWITCHES

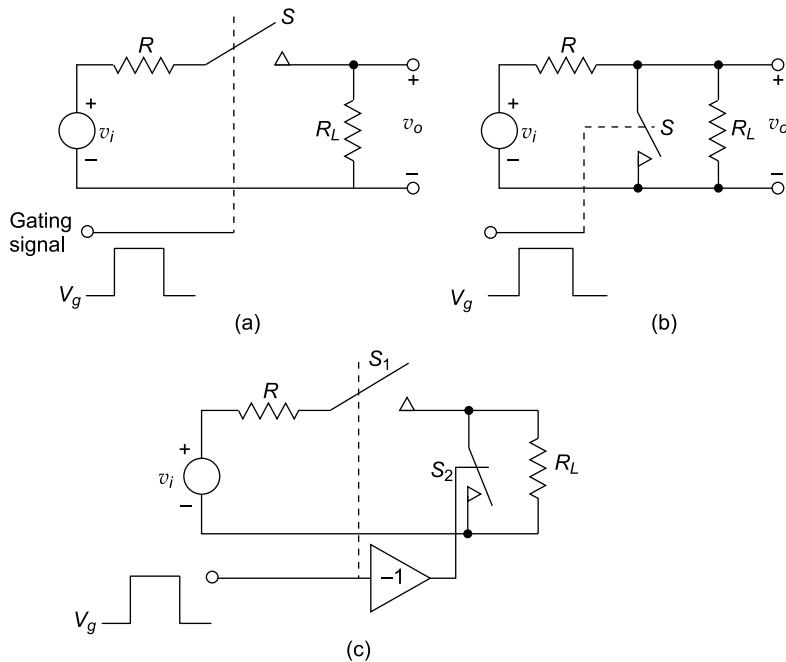
Analog switches are electronic components through which, an *open* or *closed* condition between two points can be achieved. These components are employed extensively in circuits and systems operating on analog signals. They are operated by digital control signals for the *opening* and *closing* applications. The circuits configured using such analog switches are called analog gates, transmission gates, linear gates or time-selection circuits.

The practical analog switches exhibit a small forward resistance in the ON state and a minimum amount of leakage in the OFF state. Most of the practical analog switches employ Field Effect Transistor devices namely, JFET or MOSFET devices and CMOS structures.

#### 5.5.1 Basic Principle of Operation

Figures 5.14(a), (b) and (c) show the different switch configurations. These switches control the transmission of an analog signal  $v_i$  to the load resistance  $R_L$ . A gating signal  $V_g$ , normally a digital signal controls the switch  $S$ . Figure 5.14(a) shows a series switch  $S$  transmitting  $v_i$  to the load  $R_L$  when the switch  $S$  is closed. On the other hand, the switch shown in Fig. 5.14(b) illustrates that the signal  $v_i$  is transmitted to the load when the shunt switch  $S$  is open.

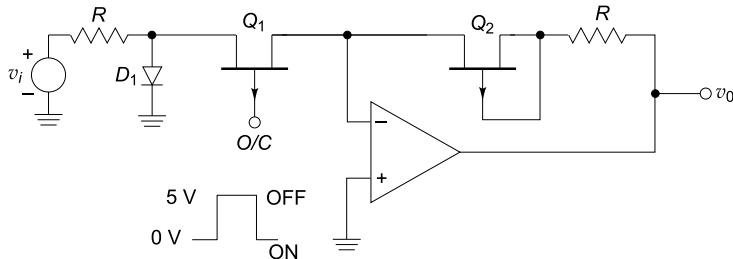
However, these practical switches are not ideal in many aspects. When the switch is closed, they do not exhibit ideal zero resistance. The series switch  $S$  shown in Fig. 5.14(a) introduces a small amount of attenuation and signal distortion may occur due to this reason. Similarly, the switch shown in Fig. 5.14(b) generates some capacitance, shunting the switch.



**Fig. 5.14** Switch configurations: (a) Series switch (b) Shunt switch  
(c) Combination of series and shunt switches

This results in some partial transmission of high frequency signals through the switch even when it is open and it results in waveform distortion. Thirdly, capacitive coupling may exist between the analog signal path and gate control input signal in both the types of switches. These imperfections of series and shunt switches lead to the series-shunt combination switch connected with an inverting buffer as shown in Fig. 5.14(c).

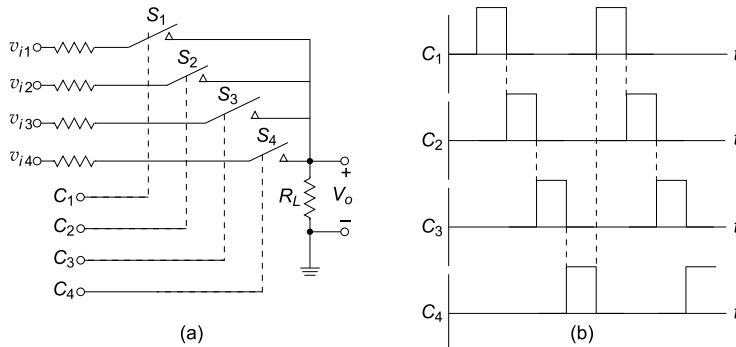
Figure 5.15 shows a P-channel JFET analog switch with OFF and ON models. This form is compatible with TTL voltage levels. When a logic 1 is applied to the gate of FET, it turns OFF or *opens* the switch. When a logic 0 is applied to the gate, it turns the FET ON or *closes* the switch. The ON resistance of JFET analog switch is typically less than  $100\ \Omega$ . The OFF resistance of the switch is near ideal, assuming negligible leakage currents through the FET.



**Fig. 5.15** Analog switch using P-channel JFETs and op-amp

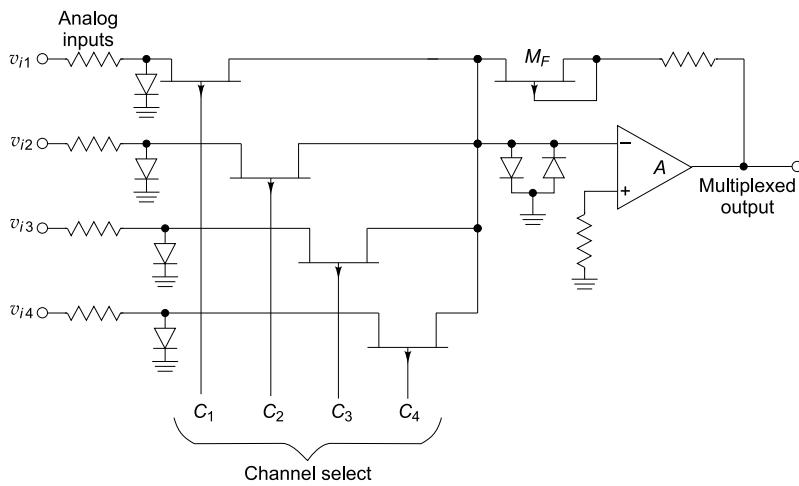
### 5.5.2 4-Channel Multiplexer

Figure 5.16(a) shows a basic switch arrangement for a 4-channel multiplexer. This allows passing four analog signals, one at a time, to a common load. The four analog signals are  $v_{i1}$ ,  $v_{i2}$ ,  $v_{i3}$  and  $v_{i4}$ , which are controlled by the channel-select control signals  $C_1$ ,  $C_2$ ,  $C_3$  and  $C_4$ . The waveforms of the channel-select signals are shown in Fig. 5.16(b).



**Fig. 5.16** (a) Switch arrangement showing multiplexing of four signals  
(b) The channel-select signals

A circuit utilising the 4-channel JFET P-channel multiplexer is shown in Fig. 5.17. This is based on the switch arrangement of Fig. 5.16. The signals  $v_{i1}$  to  $v_{i4}$  are successively sampled and are fed to the output op-amp A. The FET ( $M_F$ ) connected in the feedback path of op-amp A adds a resistance, approximately equal to that of the individual FETs in the input circuit. This results in more accurate gain realisation.



**Fig. 5.17** A circuit using the 4-channel JFET P-channel multiplexer

## 5.6 PEAK DETECTORS

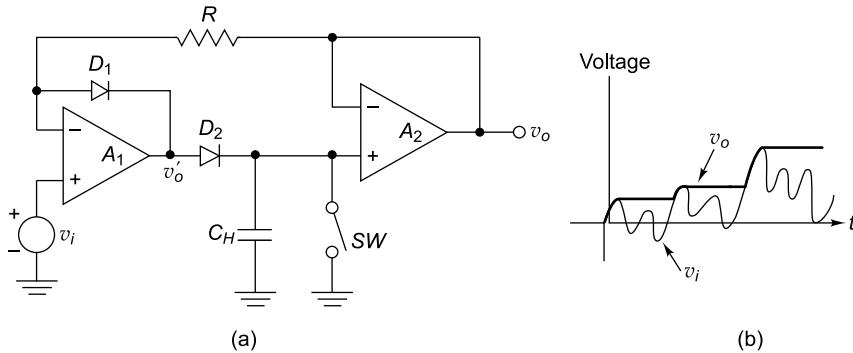
A peak detector is a circuit that produces an output voltage equal to the positive or negative peak value of the input voltage. A positive peak detector detects the positive peak magnitude of the input and a negative peak detector identifies the negative peak magnitude of the input.

The basic blocks required for the peak detector circuit are:

- (i) an analog memory such as a capacitor to store the charge proportional to the peak value
- (ii) a unidirectional switch such as a diode to charge the capacitor when a new peak arrives at the input
- (iii) a device such as a voltage follower circuit for making the capacitor charge to the input voltage and
- (iv) a switch to periodically reinitialise the output to zero.

Figure 5.18(a) shows the circuit of a positive peak detector. The capacitor  $C_H$ , diode  $D_2$ , op-amp  $A_1$  and switch  $SW$  perform the four functions listed above in order. The op-amp  $A_2$  acts as a buffer. This prevents discharging of the capacitor  $C_H$ . The diode  $D_2$  is preferred to be of very low leakage current. The diode  $D_1$  and resistance  $R$  avoids saturation of op-amp when a peak is detected. When the input signal  $v_i > 0$ , the output  $v'_o$  of op-amp  $A_1$  is positive. The diode  $D_2$  is hence forward-biased and diode  $D_1$  is reverse-biased. The capacitance  $C_H$  then gets charged. The feedback path provided by diode  $D_2$ , op-amp  $A_2$  and resistor  $R$  maintain the virtual short between the input terminals of  $A_1$ . In other words, the voltages at the inverting and non-inverting terminals of  $A_1$  are equal. Then, the voltage  $v_i$  during this phase is  $v_i = v_o + V_{D2(ON)}$ .

The output  $v_o$  tracks  $v_i$  and this phase is called the *track mode*. The op-amp  $A_1$  sources current to charge  $C_H$  through diode  $D_2$ . When  $v_i$  begins to decrease,  $D_2$  becomes reverse-biased and  $D_1$  becomes forward-biased and conducts. The output  $v'_o$  of  $A_1$  is now  $v'_o = v_i - V_{D1(ON)}$ . The feedback path from  $v_o$  to  $v_i$  through diode  $D_2$  and  $R$  is now *open*. During this phase, the capacitor voltage remains constant. Hence it is called the *hold mode* and the output of op-amp  $A_2$  retains the peak voltage.

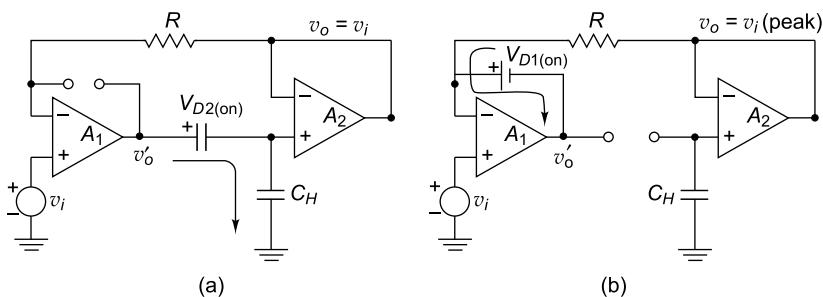


**Fig. 5.18** (a) Peak detector circuits (b) Input and output waveforms

Figure 5.18(b) shows the voltage waveforms for the positive peak detector for a certain input signal  $v_i$ . The circuit can be reset at any time by closing the switch  $SW$ . The switch  $SW$  can be a low leakage MOSFET. Negative peak detectors can be obtained by reversing the diode connections.

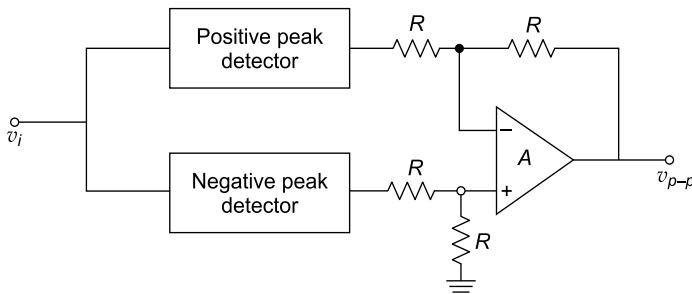
Figure 5.19(a) and (b) show the equivalent circuits of the peak detector when the circuit operates in the *track mode* and *hold mode*. It can be observed that, placing the diode  $D_2$  and op-amp  $A_2$  within the feedback path of  $A_1$  eliminates the possible errors due to the diode drop across  $D_2$  and the input offset voltage of  $A_2$ .

The requirements for op-amp  $A_1$  are low dc input error and high output current capability to charge  $C_H$  during fast occurring peaks. The op-amp  $A_2$  with low input bias current is preferred to minimise the capacitance discharge between peaks.



**Fig. 5.19** Peak detector equivalent circuits: (a) Track mode (b) Hold mode

The negative peak detector circuit can be realised by simply reversing the diode directions of Fig. 5.18(a). Figure 5.20 shows a peak-to-peak detector circuit.



**Fig. 5.20** Peak-to-peak detector circuit

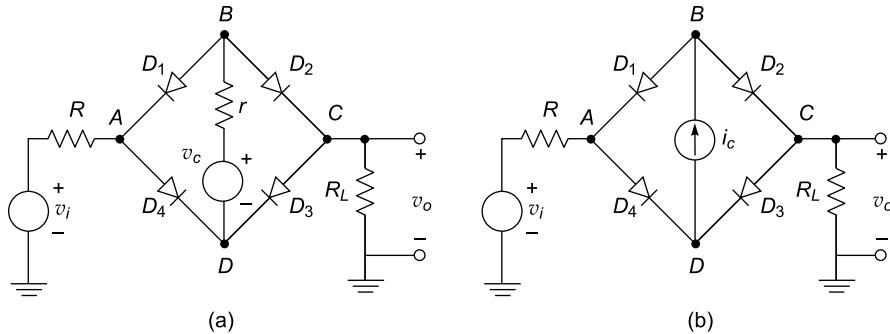
The op-amp  $A$  is a subtractor connected the op-amp circuit, which enables the signal  $v_{p-p}$  to identify the peak-to-peak value of the input signal  $v_i$ .

## 5.7 HIGH-SPEED SAMPLE/HOLD CIRCUIT USING DIODE SWITCHES

The diode switches are proved to be faster than transistor switches. This is due to the fact that the storage times and capacitances associated with diodes are much smaller than that of transistors. On the other hand, the diodes lack the *control terminal* which the three-terminal devices have. Hence, diode-gates are devised for applications where high speed of operation is required. One-diode gate, two-diode transmission gate, four-diode gates and six-diode gates are used for analog switching applications. The RCA type CA3019 integrated circuit diode array consists of six diodes, which are capable of operating with analog signals up to  $0.5V\text{ rms}$  and at frequencies of the order of 170 MHz. Gating signal of 1 V to 3 V  $\text{rms}$  is required and it can switch at a maximum rate of 500 kHz.

The four-diode gate arrangement, in combination with an op-amp circuitry can be employed for high-speed sample-and-hold circuit applications. Figures 5.21(a) and(b) show two different configurations of four-diode gates operated by a control voltage  $v_c$  and a control current source  $i_c$  respectively. The four diodes form a bridge, with the voltage  $v_i$  applied at node A and output voltage  $v_o$  observed across  $R_L$  at node C. As shown in Fig. 5.21(a), the control voltage  $v_c$  is maintained positive during transmission of analog signal  $v_i$  to output. It is switched negative for non-transmission so that the diodes are kept OFF.

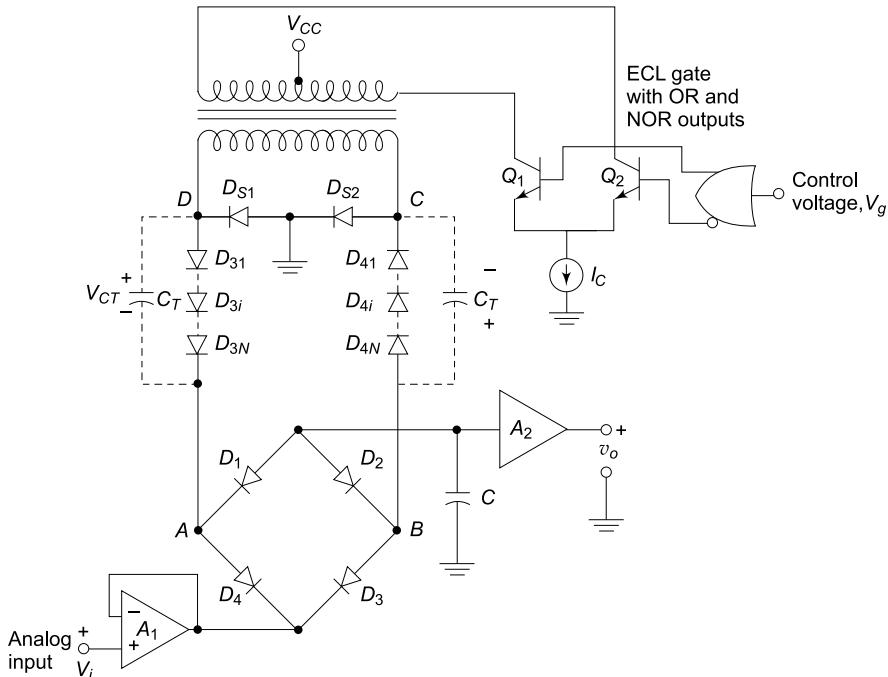
Alternatively, the current source  $i_c$  may be made ON for transmission and OFF for non-transmission as shown in Fig. 5.21(b).



**Fig. 5.21** A four-diode gate circuit: (a) Voltage controlled gating  
(b) Current controlled gating

## 5.8 HIGH-SPEED SAMPLE-AND-HOLD CIRCUIT USING FOUR-DIODE GATE

Figure 5.22 shows the circuit of a sample-and-hold circuit using such a high-speed four-diode gate. The capacitor  $C$  is made to charge to the current value of analog signal while sampling. This constitutes the



**Fig. 5.22** High-speed four-diode gate based Sample-and-Hold circuit

load. The Schottky barrier type diodes are used to enable higher speed of operation. The op-amps  $A_1$  and  $A_2$  act as buffers. The circuit employs a current source  $I_c$ . The transistors  $Q_1$  and  $Q_2$  alternately allow the current  $I_c$  to flow in either direction through the primary coil of the transformer. During transmission, a nominal value of constant current flows through the diodes  $D_{3i}$  and  $D_{4i}$ . This current flows in the forward direction through diodes  $D_1$  and  $D_4$ , and the capacitor  $C$  charges to the present value of input analog voltage. During this interval of time, the diodes,  $D_{S1}$  and  $D_{S2}$  connected across the secondary of the transformer are reverse-biased.

During *non-transmission* or the *hold* time, the load capacitor  $C$  is isolated from the input analog voltage  $v_i$ , by reversing the transformer current. This is achieved by applying the necessary gate control voltage  $V_g$  to transistors  $Q_1$  and  $Q_2$ , which reverses the direction of current through the transformer primary.

The diodes  $D_{S1}$  and  $D_{S2}$  now become forward-biased. The diodes  $D_{31}$  to  $D_{3N}$  and  $D_{41}$  to  $D_{4N}$  are diode capacitors connected in each leg of diode gate. They offer a stray capacitance of  $C_T$  and the voltage  $V_{CT}$  across  $C_T$  cannot change momentarily, when the current direction through secondary of transformer is altered. Then the voltage at point  $B$  of diode bridge increases to  $(V_{CT} + V_{DS2})$  and the voltage at point  $A$  falls to  $-(V_{CT} + V_{DS1})$ . Assuming  $N$  diodes are connected, the voltage between points  $A$  and  $B$  is  $V_{BA} = (2N + 2) 0.7\text{V}$  and hence the diode bridge becomes reverse biased instantaneously, thus enabling *non-transmission* or *hold* mode of the *S/H* circuit.

When the charge across stray capacitance  $C_T$  decreases to zero through the diodes  $D_{3i}$  and  $D_{4i}$ ,  $V_{CT}$  becomes zero, and the voltage between terminals  $A$  and  $B$  is  $V_{AB} = 1.4\text{V}$ . This keeps the bridge at *cut-off*. This state continues until the transformer current is again reversed, thus enabling the next sampling.

It can be observed that the diode bridge is maintained at *cut-off* during *non-transmission* by the voltage drop across  $D_{S1}$  and  $D_{S2}$ . This circuit can operate with a charging time of the order of 15 ns. Therefore, this arrangement makes the circuit, a very high-speed sample-and-hold circuit.

## 5.9 CLIPPERS

The wave-shaping circuits such as those used on digital computers and communication applications mainly perform voltage limiting, voltage clipping and voltage clamping functions.

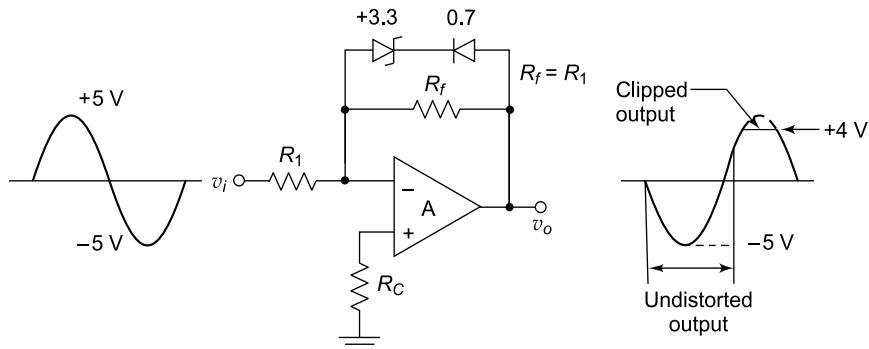
Note that the precision rectifier circuits of Section 5.4 enabled either the removal of negative half cycle of the waveform, producing half-wave rectification or reversal of the negative half cycle adding to the existing positive half cycle, thus producing continuous positive half cycles or the so-called *full-wave rectification*. The diodes in such applications acted as ideal switches. When ON they completed the feedback loop and when OFF (or reverse biased), they acted as open circuit.

On the other hand, the clipper circuits employ Zener diodes for fixing up the clipping voltage level. The direction of the Zener diode connection determines the positive and negative voltage clipping operation.

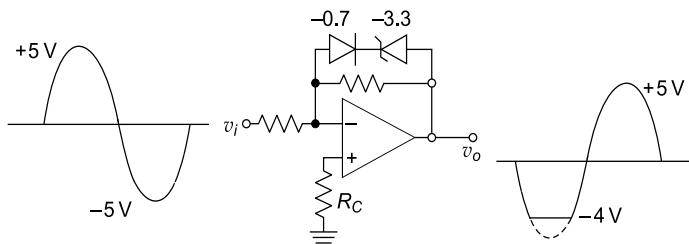
A clipper, also called an *amplitude limiter*, consists of an inverting amplifier circuit with a *back-to-back* Zener diode and a signal diode connected in the feedback loop. Figure 5.23(a) shows a single polarity voltage clipper circuit constructed using op-amp  $A$ . The gain of the circuit is determined by the ratio of resistors  $R_f/R_1$ . The signal to be clipped is applied to the inverting input of the op-amp. The output  $v_o$  follows the input  $v_i$  with  $180^\circ$  phase difference, if the Zener diode and signal diode do not exist in the feedback path.

Let us assume that a  $\pm 5\text{V}$  peak sine wave input signal  $v_i$  is applied, the breakdown voltage of Zener diode is  $3.3\text{V}$  and the *cut-in* voltage of diode is  $0.7\text{V}$ . Then, for an output voltage of  $V_Z + V_D$  ( $3.3\text{V} + 0.7\text{V} = 4\text{V}$ ), the Zener diode *avalanches*. The output signal is *clipped* or *limited* to this voltage, until the transition at the input signal makes the output to fall below  $4\text{V}$ . When the input voltage is less than

4V, the circuit acts just like an inverting amplifier with a gain of  $R_f/R_1$  during the remaining duration of the cycle. Then the diodes do not affect the inverting amplifier operation. This is due to the fact that, when the output voltage becomes negative, the semiconductor diode gets reverse biased and makes the Zener diode path open and inactive.

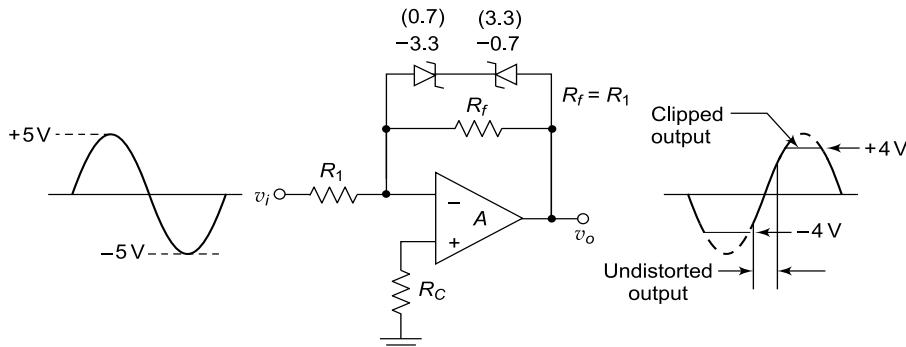


**Fig. 5.23 (a)** A single polarity positive voltage clipper circuit and its output waveform



**Fig. 5.23 (b)** A single polarity negative clipper circuit and its output waveform

A clipper that clips or limits the amplitude in both directions can be achieved by connecting two Zener diodes *back-to-back* as shown in Fig. 5.23(c). The clipping voltage level of this circuit is the sum of the forward-bias voltage of one Zener diode and the avalanche voltage of the second Zener diode. The circuit acts as an inverting amplifier between the two clipping levels.



**Fig. 5.23 (c)** Dual polarity voltage clipper circuit and its output waveform

### Example 5.3

Design a clipper circuit for a clipping level of  $+0.35V$  given an input sine wave signal of  $0.5V$  peak. Assume the gain of the amplifier is 10 and it has an input resistance of  $1\text{ k}\Omega$  connected.

#### Solution

When unclipped, output voltage =  $0.5 \times 10 = 5\text{ V}$

When clipped, output voltage =  $0.35 \times 10 = 3.5\text{ V}$

Then the circuit requires a Zener diode with breakdown voltage of  $(3.5\text{ V} - 0.7\text{ V}) = 2.8\text{ V}$ . Therefore, a  $2.8\text{ V}$  Zener diode can be chosen and connected in series with the  $0.7\text{ V}$  Zener diode as shown in Fig. 5.23(a).

## 5.10 CLAMPERS

A clamp circuit is used to add a fixed voltage level to the minimum or maximum value of an input signal. The output is clamped to a desired level by either *shifting up* or *shifting down* an input signal, depending on whether a positive or negative clamping action is required. A typical example of a clamp circuit is the *dc restorer* used in television circuit to restore the dc level for the video signal. This circuit is also called a *dc inserter*.

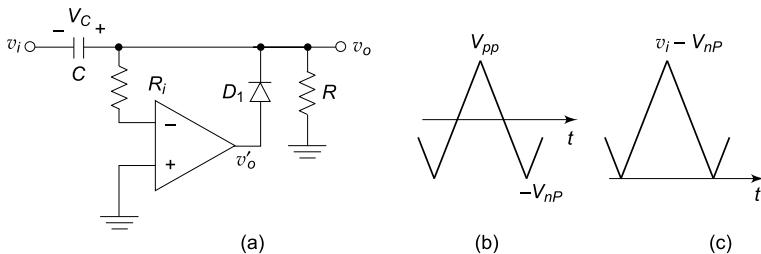
Figure 5.24(a) shows the positive clamping circuit. The input signal  $v_i$  is applied at the negative input terminal through a capacitor  $C$ . During the negative half-cycle transition of the input voltage, the output of op-amp becomes positive. The diode  $D_1$  connected at the output of op-amp is forward-biased and this causes the capacitor to get charged. The charging continues until the inverting input terminal of the op-amp attains virtual ground condition. At that instant, the peak voltage  $V_C$  across the capacitor becomes equal to the negative peak of input signal  $V_{np}$ . That is,

$$V_C = V_{np}$$

where  $V_{np}$  is the negative peak amplitude of input signal. When the input voltage goes positive, diode  $D_1$  becomes reverse-biased. The capacitor retains the previous voltage  $V_C$ . The output voltage  $v_o$  is then given by

$$v_o = v_i + V_C = v_i + V_{np}$$

The voltage  $v_i$  is hence shifted by the voltage across capacitor. The input and output waveforms are shown in Fig. 5.24(b) and (c).

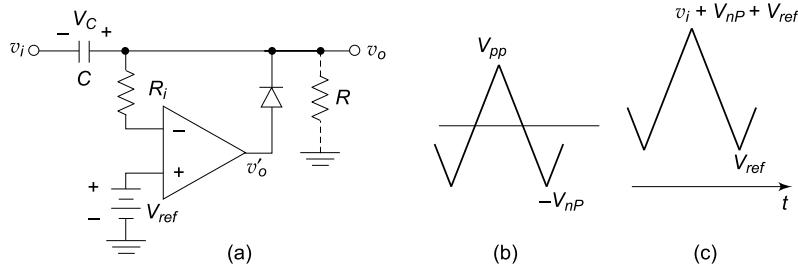


**Fig. 5.24** (a) Positive clamping circuit: (b) Input waveform  
(c) Output waveform

If a reference voltage  $V_{ref}$  is connected to the non-inverting input terminal of op-amp as shown in Fig. 5.25(a), then the capacitor charges to a value  $V_C$  such that,  $V_C = V_{np} + V_{ref}$  to maintain virtual ground at the inverting terminal of op-amp. The total output voltage is then given by

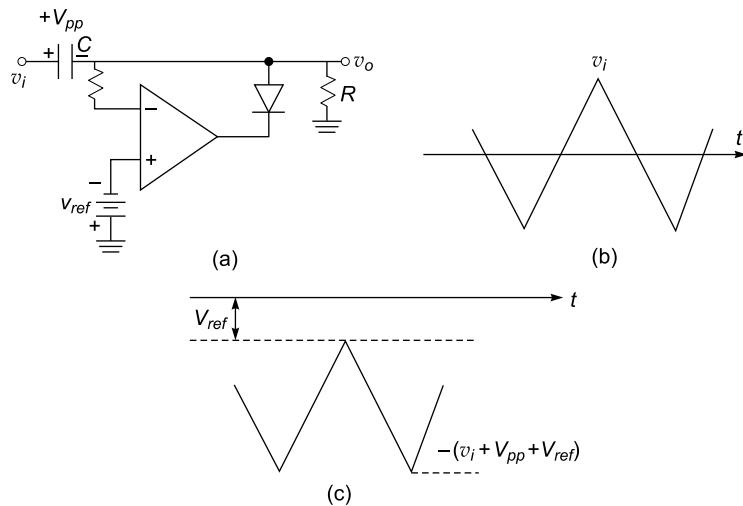
$$v_o = v_i + V_{np} + V_{ref}$$

The input and output waveforms are shown in Figs. 5.25(b) and (c). When the capacitor is recharging, the output voltage is  $v_o \approx V_{ref}$ . The negative peak clamping is achieved by reversing the diode connection and with the use of a negative reference voltage  $-V_{ref}$ :



**Fig. 5.25** (a) Positive clamping circuit using  $V_{ref}$ : (b) Input, and (c) output waveforms

Figures 5.26(a), (b) and (c) show the negative voltage clamping circuit. The reference voltage ( $-V_{ref}$ ) is connected to the non-inverting input. The input  $v_i$  when applied, changes the capacitance to  $-(V_{pp} + V_{ref})$  as the loop closes during positive transit of input signal, which makes the diode to conduct. Then, the total output voltage is given by  $v_o = -(v_i + V_{pp} + V_{ref})$ . The input and output waveforms so obtained are shown in Fig. 5.26(b) and (c).



**Fig. 5.26** (a) Negative clamping circuit using  $-V_{ref}$ : (b) Input, and (c) output waveforms

### Example 5.4

For the negative clamping circuit shown in Fig. 5.25(a), assume  $V_{ref} = 1.5$  V and input voltage varies from 2.5 V to 5 V. Determine

- the voltage  $V_C$  across the capacitor
- the peak value of the clamped output voltage
- output of op-amp during charging interval
- maximum value of differential input voltage for the op-amp.

### Solution

(a) The peak voltage  $V_{pp} = 5\text{V}$  and  $V_{np} = 2.5\text{ V}$  (i.e.  $-V_{np} = -2.5\text{ V}$ )

$$\text{The capacitor voltage } V_C = V_{np} + V_{ref} = 2.5 + 1.5 = 4\text{ V}$$

(b) The input signal is shifted up by 4 V.

Minimum level is  $V_{ref} = 1.5\text{ V}$

The peak value of the clamped output voltage is

$$V_{o(peak)} = V_{np} + V_{ref} + V_{pp} = 2.5 + 1.5 + 5 = 9\text{ V}$$

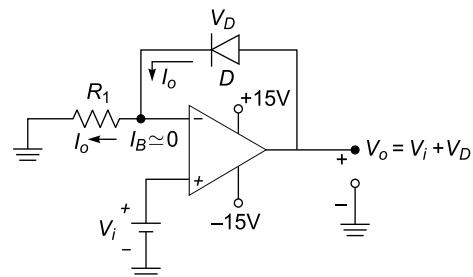
(c) Op-amp output voltage during the time of charging is  $v'_o = v_{ref} + 0.7\text{ V} = 2.2\text{ V}$

(d) Maximum differential input voltage of the op-amp occurs when  $V_{o(peak)}$  reaches its maximum, and it is given by  $v_d = 1.5\text{ V} - 9.0\text{ V} = -7.5\text{ V}$ . Note that the maximum differential input voltage is the value of peak-to-peak input signal.

## 5.11 DIODE TESTER (DIODE MATCH FINDER)

Some applications require matched diodes from a production batch with equal forward voltage drop values at a specific value of diode current. A typical application is a ring modulator. In such situations, the diode match finder shown in Fig. 5.27 is employed. The circuit is obtained by replacing the floating load  $R_f$  of Fig. 4.11(a) with the diode under test. The current through the loop is set by the input voltage  $V_i$  and resistor  $R_1$ . The input terminals of the op-amp draw negligible current. Therefore, the current through the diode  $D$  is  $I_o = \frac{V_i}{R_1}$ . As long as the voltage  $V_i$  and resistor  $R_1$

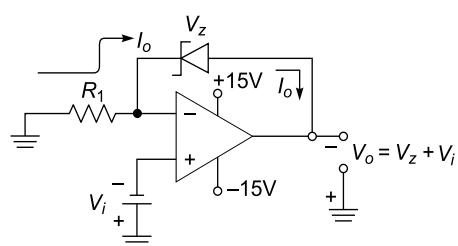
are maintained constant, the current  $I_o$  will remain constant. The output voltage  $V_o$  is thus equal to  $(V_i + V_D)$  where  $V_D$  is the diode voltage drop. Any possible errors in the output voltage can be *nulled* initially. Matching diodes can be selected by connecting the diodes one by one in the feedback path and by measuring the voltage across them. The test current  $I_o$  can be set by the combination of  $V_i$  and  $R_1$ .



**Fig. 5.27** Diode match-finder circuit

## 5.12 ZENER DIODE TESTER

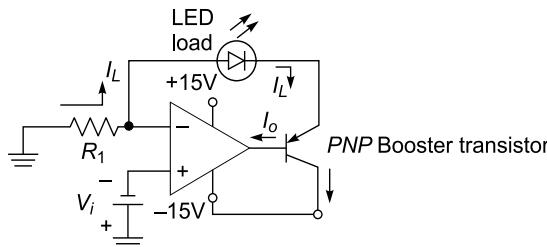
The Zener diode tester circuit is shown in Fig. 5.28. The circuit can be used to identify the breakdown voltage of Zener diodes. The input voltage  $V_i$  and  $R_1$  set the value of  $I_o$ , the load or Zener current at a constant value  $I_o = V_i/R_1$ .  $V_i$  pushes  $V_o$  to go negative until the Zener diode breaks down and maintains the Zener voltage at  $V_z$ . Since  $V_i$  and  $R_1$  are constant, the Zener current will be constant regardless of the Zener diode voltage. Thus, the Zener breakdown voltage can be found out by  $V_z = V_o - V_i$ . Identification of matched Zener diodes can be useful in designing dual ( $\pm$ ) supply voltages from a single supply.



**Fig. 5.28** Zener diode tester circuit

## 5.13 LIGHT EMITTING DIODE (LED) TESTER

Figure 5.29 can be used as an LED tester. The op-amp 741 can supply around 5 to 10 mA at its output. Thus, in order to realise higher load currents, a *PNP* transistor with required  $\beta$  can be used as shown. If the op-amp can produce a current of  $I_o$ , the maximum load current can be  $\beta I_o$ . The diode current  $I_L$  is set by  $I_L = V_i/R_1$ . Thus, the brightness of LEDs can be measured easily for matching or testing purposes, since the current through the diode is exactly maintained constant by  $V_i$  and  $R_1$ . Here, two LEDs at a time can also be connected as the load, since both would carry the same current  $V_i/R_1$ . Hence, matched LEDs with equal brightness can be identified.



**Fig. 5.29** LED tester circuit

## SUMMARY

- An operational amplifier operates in a non-linear manner when operated in open-loop configuration. Under such conditions, it finds use in applications such as Schmitt trigger, voltage level detectors or comparators, discriminators, window detectors, limiters and data converters.
- The comparator consists of an op-amp operated in open-loop. The output waveform  $v_o$  of a comparator switches between positive and negative saturation levels, when the input signal  $v_i$  passes through zero in the negative and the positive directions.
- The important applications of comparator are their use as
  - Zero crossing detector or sine-wave to square-wave converter
  - Amplitude distribution analyser
  - Pulse time modulator
  - Window detector
  - Timing marker signal generator
  - Phase detector
- The window detector, also called a window comparator identifies an unknown input voltage falling within two threshold voltage levels. 4115/04 of Burr-Brown and LTC1040 of Linear technology are the window detectors available as individual IC modules.
- The comparator circuit designed with a positive feedback to avoid unwanted triggering is called the Schmitt Trigger or the Regenerative Comparator.
- The input voltage  $v_i$  of a Schmitt Trigger, triggers the output  $v_o$  every time it crosses certain voltage levels. These voltage levels are called Upper Threshold Voltage  $V_{UT}$  and Lower Threshold Voltage  $V_{LT}$ . The difference between them is called the hysteresis voltage  $V_H = V_{UT} - V_{LT}$
- An ideal diode or precision rectifier rectifies voltages which are below the level of cut-in voltage of the diode.

- The full-wave rectifier circuit constructed using op-amp and diode is called *absolute value circuits*.
- Analog switches used in analog gates, transmission gates, linear gates or time-selection circuits are electronic components which open or close the connection between two points.
- The practical analog switches exhibit a small forward resistance in the ON state and a minimum amount of leakage in the OFF state.
- A peak detector produces an output voltage equal to the positive or negative peak value of the input voltage. A positive peak detector detects the positive peak magnitude of the input and a negative peak detector identifies the negative peak magnitude of the input.
- The RCA type CA3019 integrated circuit switch array consists of six diodes, which are capable of operating with analog signals up to 0.5V *rms* and at frequencies of the order of 170 MHz.
- The Schottky barrier type diodes are used to enable higher speed of operation in high speed sample-and-hold circuits.
- A clipper is also called an amplitude limiter.
- A clamer circuit adds a fixed voltage level to the minimum or maximum value of an input signal by either shifting up or shifting down an input signal.

## REVIEW QUESTIONS

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1. What are the characteristics of an ideal and a practical comparator?
2. List different types of comparator circuits.
3. Draw an op-amp based comparator circuit.
4. List the applications of comparator circuits.
5. An op-amp comparator circuit connected with two Zener diodes of rating  $V_{Z1} = V_{Z2} = 6.3$  V is operated by  $\pm 15$  V power supply. Determine the output voltage levels in saturation conditions assuming (i) an ideal op-amp and (ii) open-loop gain of op-amp is 50000.
6. What is a zero crossing detector?
7. What is a window detector? Explain its operation.
8. Explain phase difference measurement using comparator circuits.
9. For the circuit of Fig. 5.4(a), assume  $v_i = 120$  mV peak sine-wave of 200 Hz frequency,  $R = 1\text{ k}\Omega$  and  $V_{Z1} = V_{Z2} = 6.2$  V. Assume supply voltages of  $\pm 15$  V. Draw the transfer characteristics of the circuit for (a) an ideal op-amp and (b) an op-amp with an open-loop gain of 60000.
10. Define the term *hysteresis*. Name the parameters determining the hysteresis.
11. Explain the operation of a Schmitt trigger circuit using comparator.
12. Define the terms Upper and Lower Tripping Points of a Schmitt trigger. What is the significance of the two parameters?
13. In the circuit of Fig. 5.9(a),  $R_1 = 33\text{ k}\Omega$ ,  $R_2 = 56\text{ }\Omega$ ,  $v_i = 1V_{PP}$  sine-wave of frequency 50 Hz,  $V_{ref} = 0\text{ V}$  and op-amp 741 is used with supply voltages  $= \pm 15\text{ V}$ . Assume the saturation voltages are  $\pm 13.5\text{ V}$ . Determine the threshold voltages  $V_{UT}$  and  $V_{LT}$ .
14. Calculate the ON duration of a 1 kHz pulse generator with 20% duty cycle.
15. What is a *precision diode*?
16. Draw a precision half-wave rectifier circuit and explain its operation.
17. Draw a half-wave rectifier circuit to rectify an ac voltage of 0.2 V. Explain the circuit diagram.
18. Draw the circuit of a full-wave rectifier circuit and explain its operation.
19. What is an absolute value circuit? How does it attain high-input impedance? Explain using a neat circuit diagram.
20. What is an analog switch? Explain its principle of operation.
21. Design a 4-channel multiplexer using analog switches.
22. Explain the operation of a peak detector circuit.
23. How do you design for detecting negative peak and positive peaks?

24. Sketch a precision rectifier peak-to-peak detector circuit. Draw the input and output waveforms and explain the circuit operation.
25. How will you realise a peak detector using a precision rectifier?
26. Realise a negative peak detector circuit using op-amp. Draw the input and output transient waveforms.
27. Construct a peak-to-peak detector circuit using op-amp. Elaborate the operation.
28. Explain the operation of a practical sample-and-hold circuit. What are its applications?
29. Explain why the buffers used in sample-and-hold circuits should have high input impedance values.
30. Draw the circuit of a high speed sample-and-hold circuit and explain its operation, sketching the input signal, control and output voltage waveforms.
31. Draw the circuits for negative, positive and dual polarity clipping circuits and explain their operations.
32. Design a clipper circuit for a clipping level of  $+0.54$  V, given an input sine-wave signal of 1V peak. Assume the gain of the amplifier is 10 and it has an input resistance of  $1\text{ k}\Omega$  connected.
33. Draw the circuits of (a) Clippers and (b) Clampers. Explain their operations.
34. For the clamping circuit shown in Fig. 5.24 (a), assume  $V_{ref} = 2\text{ V}$  and input voltage varies from 3V to 5V. Determine
  - (a) the voltage  $V_c$  across the capacitor
  - (b) the peak value of the clamped output voltage
  - (c) output of op-amp during charging interval and
  - (d) maximum value of differential input voltage for the op-amp.
35. Explain the operation of a negative clamper circuit using a reference voltage  $V_{ref}$ . Assume a sinusoidal input voltage at the input. Draw the clamped output waveform.
36. Design a nonsaturating precision half-wave rectifier of Fig. 5.12(a) to produce 4V peak output using sinewave input of peak amplitude 0.5 V. The frequency of sine wave signal is 2 MHz.
37. An application requires diodes with accurately same forward voltage drops a specific value of output current. Devise a circuit for the same using op-amp and explain.
38. Construct a zener diode tester using op-amp and explain its operation.
39. Construct an LED tester using op-amp and explain its operation. What is the use of the BJT booster transistor at the output?

# Active Filters

## 6.1 INTRODUCTION

A filter is a frequency selective circuit that allows only a certain band of the desired frequency components of an input signal to pass through and attenuates the signals of undesired frequency components.

The filters are of two types namely (i) analog filters and (ii) digital filters. The analog filters are further classified as passive filters and active filters. The passive filters utilise only resistors, inductors and capacitors. An active network is a circuit obtained by interconnecting passive elements (resistors and capacitors) and active elements (transistors, tunnel diodes and operational amplifiers). An active filter uses an op-amp in order to minimise the effect of loading on the frequency characteristics of the filter.

The filters are widely used in communication, signal processing and sophisticated electronic instruments. The applications of filters also include the suppression of power-line hum, reduction of very low or high-frequency interference and noise, bandwidth limiting and specialised spectral shaping.

## 6.2 COMPARISON BETWEEN PASSIVE AND ACTIVE NETWORKS

The limitations of passive *RLC* networks and active *RC* networks, advantages of active filters, and properties of passive and active networks are presented in this section.

### 6.2.1 Limitations of Passive *RLC* Networks over Active *RC* Networks

- (i) In *RLC* networks, the practical inductors tend to deviate from the inductance realised.
- (ii) There is a power loss because of the dissipation in resistive and inductive elements of the passive network.
- (iii) The *Q* factor is defined by  $Q = \frac{\omega L}{r_L}$ . Since  $r_L = 0$  for an ideal inductor,  $Q = \infty$ . But in practical networks, *Q* will not be infinity because  $r_L$  cannot be zero.
- (iv) For most practical inductors, the total dissipative losses tend to increase with frequency, since *Q* does not increase linearly with frequency.
- (v) The magnetic coupling creates additional problem in the form of unwanted and stray field which is harmful for applications such as satellite instrumentation.
- (vi) At low frequency (less than 1 kHz) applications such as control systems and analog computers, practical inductors of reasonable *Q* tend to become bulky and expensive.
- (vii) The dissipative losses start increasing when an inductor is miniaturised. The *Q* of a low-frequency inductor is roughly proportional to the square of the scaling factor. The demand for space-saving systems requires network miniaturisation. This becomes a formidable problem when inductors are present in the circuit. Use of quartz crystals helps the designer to alleviate some of the above problems at higher frequency ranges.

- (viii) In addition to the unavoidable use of inductors, passive networks have some fundamental limitations also. For example, it is well known that the driving point function  $Z(s)$  of an *RLC* network must satisfy the following conditions.
- $Z(s)$  is real for real values of  $s$
  - $R_e Z(s) \geq 0$  for  $R_e s \geq 0$

For a transformerless *RLC* network, the transfer voltage (or current) ratio  $H(s)$  is again restricted by the following condition

$$H(s) < 1 \text{ for real values of } s.$$

### 6.2.2 Advantages of Active Filters over Passive Filters

- The maximum value of the transfer function or gain may be greater than unity.
- The loading effect is minimal, which means that the output response of the filter is essentially independent of the load driven by the filter.
- The active filters do not exhibit insertion loss. Hence, the passband gain is equal to 0dB.
- Complex filters can be realised without the use of inductors.
- The passive filters using  $R$ ,  $L$  and  $C$  components are realisable only for radio frequencies. Because, the inductors become very large, bulky and expensive at audio frequencies. Due to low  $Q$  at low frequency applications, high power dissipation is incurred. The active filters overcome these problems.
- Rapid, stable and economical design of filters for variety of applications is possible.
- The active filters are easily tunable due to flexibility in gain and frequency adjustments.
- The op-amp has high input impedance and low output impedance. Hence, the active filters using op-amp do not cause loading effect on the source and load. Therefore, cascading of networks does not need buffer amplifier.
- Active filters for fixed frequency and variable frequency can be designed easily. The adjustable frequency response is obtained by varying an external voltage signal.
- There is no restriction in realising rational function using active networks.
- Use of active elements eliminates the two fundamental restrictions of passivity and reciprocity of *RLC* networks. Thus, active networks can realise network functions using *RLC* networks and driving point or transfer characteristic which are unachievable with passive networks.

### 6.2.3 Limitations of Active Filters over Passive Filters

- The high frequency response is limited by the gain-bandwidth product and slew rate of the practical op-amps, leading to comparatively lower bandwidth than the designed bandwidth.
- The design of active filters becomes costly for high frequencies.
- Active filters require dual polarity dc power supply whereas passive filters do not.
- The active element is prone to the process parameter variations and they are sensitive to ambient conditions like temperature. Hence, the performance of the active filter deviates from the ideal response.

### 6.2.4 General Properties of Passive and Active Networks

The general properties of passive and active networks are summarised in Table 6.1.

**Table 6.1** General properties of passive and active networks

S. No.	Feature	Passive RLC Network	Active RC network
1	Realisability	Can realise only a class of real rational functions which are analytic in the right half of rational s-plane	No restrictions. Can realize any real function
2	Requirement of inductors	Inductors are required in almost all cases	Inductors are not required
3	Applicability	Used for applications frequency response	Can be used both for fixed and variable frequency response type applications.
4	Frequency range	Above 200 Hz	Below 100 kHz
5	Signal source	Suitable only for resistive source impedances. The low impedance source must be capable of supplying enough signal power.	High input impedance can be achieved with the use of op-amps. Hence, filter is independent of source impedance. Operates with lower signal power.
6	Load impedance	Suitable only for resistive load impedances. Filter operation depends mainly on load impedance.	Very low output impedance can be achieved. Hence, filter operation is independent of load impedance.
7	Buffer amplifiers	Buffer amplifier is required, resulting in increased number of stages.	Additional buffers are not required due to good impedance matching characteristics.
8	Insertion loss	Insertion loss is significantly high. Hence, additional amplification is required.	Insertion gain control can be made. Hence, additional amplifiers are not required.
9	Micro-miniaturisation	Since inductors play a role, miniaturisation and integration are not possible.	Resistors and capacitors being replaced by MOS devices result in miniaturisation to the order of 65 nm feature sized devices.
10	Stability	Absolutely stable	Instability may arise due to varying process conditions in fabrication. Stability margin can be improved by more accurate process conditions.
11	Sensitivity	The ladder type filter is less sensitive.	More sensitive.
12	Power supplies	Does not require any power supplies	Dual power supplies are required to bias the active elements.

## 6.3 ACTIVE NETWORK DESIGN

A filter is a circuit that processes the signals based on the frequency dependency characteristics. The manner in which the behaviour of the filter varies with frequency is called its *frequency response* and it is expressed in terms of the *transfer function*  $H(j\omega)$ , where  $\omega = 2\pi f$  is the *angular frequency* in radians per second (rad/s) and  $j$  is the imaginary unit. A filter is a linear two-port network with a transfer function  $H(s) = V_o(s)/V_i(s)$ . This response is also expressed as  $H(j\omega) = |H(j\omega)| e^{j\phi(\omega)}$  where  $|H(j\omega)|$  is the *magnitude response* and  $\phi(\omega)$  is the *phase response*.

A filter can be realised in any one of the following four basic response types:

- (i) Low-pass filter (LPF)
- (ii) High-pass filter (HPF)
- (iii) Bandpass filter (BPF)
- (iv) Band-reject filter (BRF), Bandstop or Band elimination filter (BEF)

### 6.3.1 Low-pass Filter (LPF)

A low-pass filter allows only low frequency signals up to a certain break-point  $f_H$  to pass through, while suppressing high frequency components as shown in Fig. 6.1(a). The range of frequencies from 0 to higher cut-off frequency  $f_H$  is called *passband* and the range of frequencies beyond  $f_H$  is called *stopband*.

### 6.3.2 High-pass Filter (HPF)

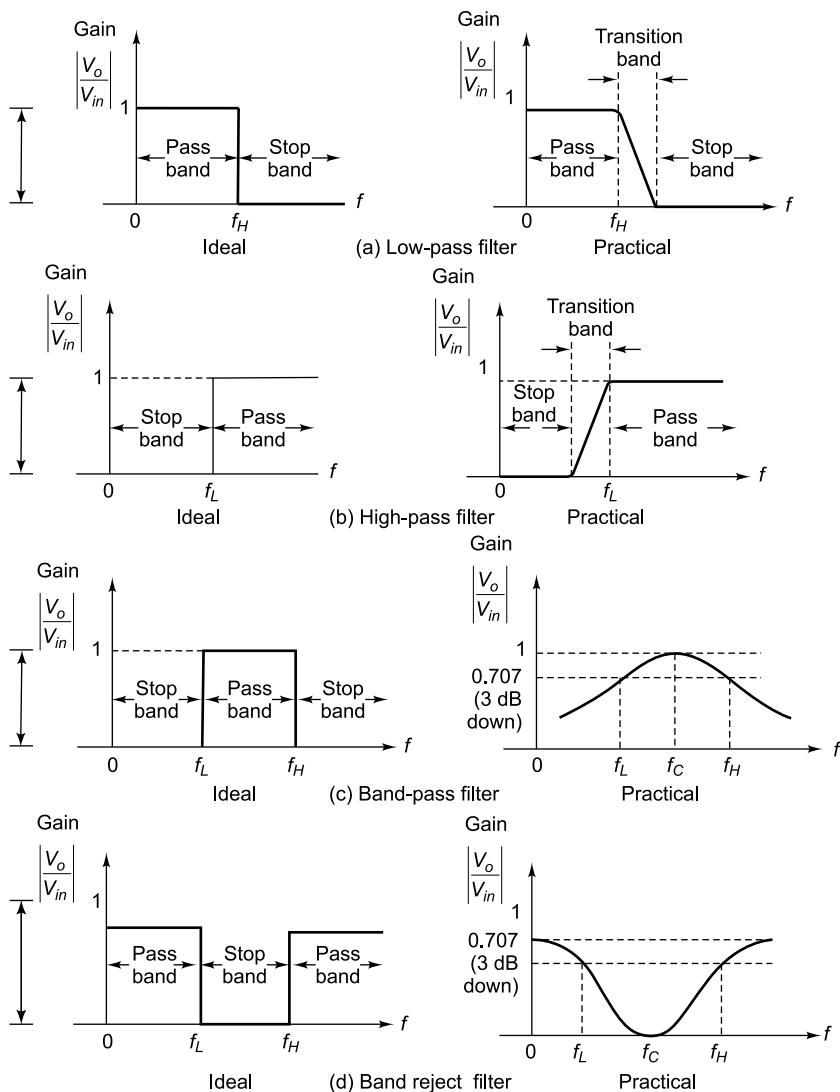
A high-pass filter allows only frequencies above a certain break-point  $f_H$  to pass through and attenuates the low frequency components as shown in Fig. 6.1(b). The range of frequencies beyond its lower cut-off frequency  $f_L$  is called *passband* and the range of frequencies from 0 to  $f_L$  is called *stopband*.

### 6.3.3 Bandpass Filter (BPF)

The bandpass filter is the combination of high and low-pass filters, and this allows a specified range of frequencies to pass through. The ideal and practical characteristics of the bandpass filter are shown in Fig. 6.1(c). It has two stopbands in the range of frequencies between 0 and  $f_L$  and beyond  $f_H$ . The band between  $f_L$  and  $f_H$  is called *passband*. Hence its bandwidth is  $(f_H - f_L)$ .

### 6.3.4 Band-Reject Filter (BRF) or Band-Elimination Filter (BEF)

The band-reject filter is the logical inverse of bandpass filter, which does not allow a specified range of frequencies to pass through. The ideal and practical characteristics of the band-reject filter are shown in Fig. 6.1(d). It has two passbands in the range of frequencies between 0 and  $f_L$  and beyond  $f_H$ . The band between  $f_L$  and  $f_H$  is called *stopband*.



**Fig. 6.1** The ideal and practical characteristics of (a) Low-Pass Filter, (b) High-pass Filter, (c) Bandpass Filter and (d) Band Reject Filter

## 6.4 DESIGN OF LOW-PASS FILTERS

In order to improve the response of the filter, a higher order filter can be used. A second order low-pass filter consists of two  $RC$  pairs and has a roll-off rate of  $-40\text{dB/decade}$ .

### 6.4.1 First Order Low-pass Filter with Unity Gain

The first order (one-pole) active low-pass filter with unity gain, i.e. with voltage follower is shown in Fig. 6.2(a).

The voltage transfer function for the circuit is

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{\frac{1}{sC}}{\frac{1}{sC} + R} = \frac{1}{1 + sRC}$$

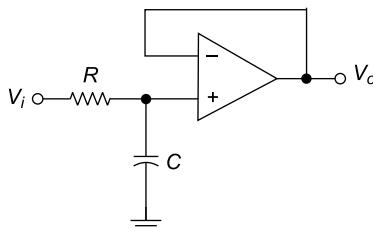
$$H(j\omega) = \frac{1}{1 + j \frac{\omega}{\omega_H}}$$

where

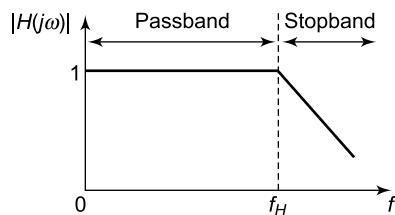
$$\omega_H = \frac{1}{RC}$$

Therefore,

$$|H(j\omega)| = \frac{1}{\sqrt{1 + \left(\frac{\omega}{\omega_H}\right)^2}} \text{ or } |H(jf)| = \frac{1}{\sqrt{1 + \left(\frac{f}{f_H}\right)^2}}$$



(a)



(b)

**Fig. 6.2** (a) First order low-pass filter with voltage follower (unity gain) and (b) Bode plot of low-pass filter with voltage follower (unity gain)

The Bode plot of the voltage gain magnitude curve is shown in Fig. 6.2(b). The slope of the voltage gain magnitude curve outside the passband is 6 dB/octave or 20 dB/decade. This characteristic is called the roll-off. The roll-off becomes sharper or steeper with higher-order filters.

### Example 6.1

A first order low-pass Butterworth active filter has a cut-off frequency of 10 kHz and unity gain at low frequency. Find the voltage transfer function magnitude, in dB, at 12 kHz for the filter.

**Solution** The voltage transfer function magnitude of the first order low-pass Butterworth filter is given by

$$\begin{aligned} |H(jf)| &= \frac{1}{\sqrt{1 + \left(\frac{f}{f_H}\right)^2}} = \frac{1}{\sqrt{1 + \left(\frac{12 \times 10^3}{10 \times 10^3}\right)^2}} \\ &= 0.64, \text{ i.e. } 20 \log 0.64 = -3.87 \text{ dB} \end{aligned}$$

### 6.4.2 First Order Low-pass Filter with Variable Gain

Figure 6.3(a) is an active low-pass filter with single  $RC$  network connected to the non-inverting terminal of op-amp. The input resistor  $R_i$  and feedback resistor  $R_f$  are used to determine the gain of the filter in the passband. At low frequencies, the capacitor appears open. And the circuit acts like a non-inverting amplifier with a voltage gain

of  $\left(1 + \frac{R_f}{R_i}\right)$ . As the frequency increases,

the capacitive reactance decreases, causing the voltage gain to drop off.

Referring to Fig. 6.3(a), the voltage  $V_1$  across the capacitor is

$$V_1 = \frac{V_i}{1 + j2\pi f RC}$$

The output voltage  $V_o$  for noninverting amplifier is

$$V_o = \left(1 + \frac{R_f}{R_i}\right) V_1$$

By substituting  $V_1$  in the above equation, the output voltage  $V_1$  becomes

$$V_o = \left(1 + \frac{R_f}{R_i}\right) \frac{V_i}{1 + j2\pi f RC}$$

or 
$$\frac{V_o}{V_i} = \frac{A}{1 + j\left(\frac{f}{f_H}\right)}$$

where  $\frac{V_o}{V_i}$  is the gain of the low-pass filter which is a function of frequency,

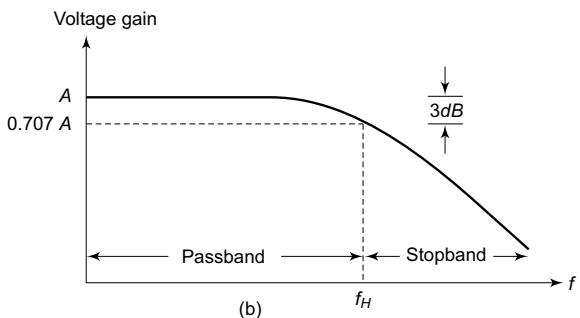
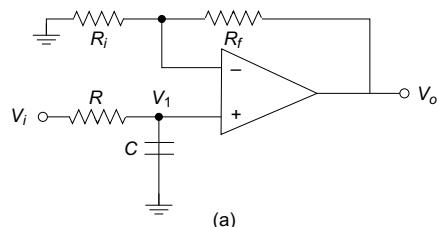
$$A = 1 + \left(\frac{R_f}{R_i}\right)$$
 is the passband gain of the filter,

$f$  is the frequency of the input signal, and

$$f_H = \frac{1}{2\pi RC}$$
 is the high cut-off frequency of the filter.

The frequency response of the filter can be determined by using the magnitude of the gain of the low-pass filter, which is expressed as

$$\left| \frac{V_o}{V_i} \right| = \frac{A}{\sqrt{1 + \left(\frac{f}{f_H}\right)^2}} \quad (6.1)$$



**Fig. 6.3** (a) First order low-pass filter with variable gain and (b) Its frequency response

At very low frequencies, i.e.  $f < f_H$ , the gain is  $\equiv A$ . When the frequency reaches the cut-off frequency, i.e.  $f = f_H$ , the gain falls to 0.707 times the maximum gain  $A$ . The frequency from 0 to  $f_H$  is called the passband. At high frequencies, i.e.  $f > f_H$ , the gain decreases at a constant rate of  $-20$  dB/decade. The frequency range beyond  $f_H$  is called stopband. The frequency response of the active low-pass filter (non-ideal) is shown in Fig. 6.3(b).

**Low-pass filter design** The following steps are used for the design of an active low-pass filter.

1. Choose the value of high cut-off frequency  $f_H$ .
2. Select the value of capacitor  $C$  such that its value is  $\leq 1 \mu\text{F}$ .
3. When the values  $f_H$  and  $C$  are known, the value of  $R$  can be calculated by using  $f_H = \frac{1}{2\pi RC}$ .
4. Finally, select the values of  $R_i$  and  $R_f$  depending on the desired passband gain by using

$$A = 1 + \left( \frac{R_f}{R_i} \right).$$

### Example 6.2

Design a first order low-pass filter at a cut-off frequency of  $2 \text{ kHz}$  with a passband gain of  $2$ .

**Solution** Refer to Fig. 6.3(a)

Given

$$f_H = 2 \text{ kHz} \text{ and } A = 2$$

Let

$$C = 0.01 \mu\text{F}$$

We know that

$$f = \frac{1}{2\pi RC}$$

Therefore,

$$R = \frac{1}{2\pi f C} = \frac{1}{2\pi (2 \times 10^3) \times 10^{-8}} = 7.95 \text{ k}\Omega$$

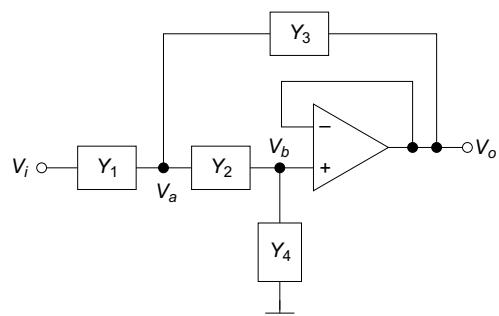
$$A = 1 + \frac{R_f}{R_i} = 2$$

Therefore,

$$R_f = R_i = 10 \text{ k}\Omega \text{ (say)}$$

## 6.5 GENERAL SECOND-ORDER ACTIVE FILTER WITH UNITY GAIN

Figure 6.4 shows a general second order (two-pole) active filter, also called *Sallen-Key filter*, with admittances  $Y_1$  through  $Y_4$  and an ideal voltage follower. The loading effect will be eliminated by using a voltage follower which has high input impedance and low output impedance. Further, a non-inverting amplifier configuration can be incorporated to increase the gain and to eliminate the loading effects. The transfer function for the general network is derived and then the specific admittance is applied to obtain the characteristics of the particular filter.



**Fig. 6.4** General second order active filter with unity gain

Applying Kirchhoff's current law equation at node  $V_a$ , we get

$$(V_i - V_a)Y_1 = (V_a - V_b)Y_2 + (V_a - V_o)Y_3 \quad (6.2)$$

Applying Kirchhoff's current law equation at node  $V_b$ , we get

$$(V_a - V_b)Y_2 = V_b Y_4 \quad (6.3)$$

According to voltage follower characteristics,  $V_b = V_o$ . Therefore, Eq. (6.3) becomes

$$V_a = V_b \left( \frac{Y_2 + Y_4}{Y_2} \right) = V_o \left( \frac{Y_2 + Y_4}{Y_2} \right) \quad (6.4)$$

Substituting Eq. (6.4) into Eq. (6.2) and using the relation  $V_b = V_o$ , we get

$$\begin{aligned} V_i Y_1 + V_o (Y_2 + Y_3) &= V_a (Y_1 + Y_2 + Y_3) \\ &= V_o \left( \frac{Y_2 + Y_4}{Y_2} \right) (Y_1 + Y_2 + Y_3) \end{aligned} \quad (6.5)$$

Multiplying Eq. (6.5) by  $Y_2$  and rearranging the terms, the transfer function becomes

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{Y_1 Y_2}{Y_1 Y_2 + Y_4 (Y_1 + Y_2 + Y_3)} \quad (6.6)$$

For obtaining a low-pass filter, both  $Y_1$  and  $Y_2$  should be conductances, i.e.  $Y_1 = 1/R_1$  and  $Y_2 = 1/R_2$  which will permit the signal to pass into the voltage follower at lower frequencies. If  $Y_4$  is a capacitor, then the output will roll-off at high frequencies.

For producing a two-pole function,  $Y_3$  should also be a capacitor. If both  $Y_1$  and  $Y_2$  are capacitors, then the signal will be blocked at low frequencies but will be passed into the voltage follower at high frequencies, which results in a high-pass filter. Hence, both the admittances  $Y_3$  and  $Y_4$  should be conductances to produce a second order high-pass transfer function.

### 6.5.1 General Second-Order Active Filter with Variable Gain

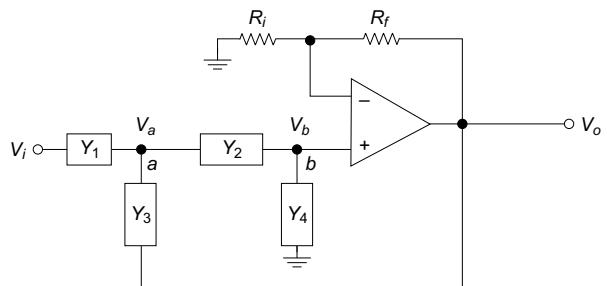
A general second-order active filter with variable gain is shown in Fig. 6.5. Here the op-amp is connected in non-inverting amplifier configuration. The results thus obtained can be used for the analysis of low-pass and high-pass filters. Therefore,

$$V_o = \left( 1 + \frac{R_f}{R_i} \right) V_b = A V_b \quad (6.7)$$

$$\text{where } A = \left[ 1 + \frac{R_f}{R_i} \right] \quad (6.8)$$

Applying Kirchhoff's current law at node  $V_a$ , we get

$$V_i Y_1 = V_a (Y_1 + Y_2 + Y_3) - V_o Y_3 - V_b Y_2$$



**Fig. 6.5** General second-order active filter (Sallen-key filter)

$$= V_a (Y_1 + Y_2 + Y_3) - V_o Y_3 - \frac{V_o Y_2}{A} \quad (6.9)$$

Applying Kirchhoff's current law at node  $V_b$ , we get

$$\begin{aligned} V_a Y_2 &= V_b (Y_2 + Y_4) = \frac{V_o (Y_2 + Y_4)}{A} \\ V_a &= \frac{V_o (Y_2 + Y_4)}{A Y_2} \end{aligned} \quad (6.10)$$

Substituting Eq. (6.10) into Eq. (6.9) and simplifying, we get

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{AY_1 Y_2}{Y_1 Y_2 + Y_4 (Y_1 + Y_2 + Y_3) + Y_2 Y_3 (1 - A)} \quad (6.11)$$

### 6.5.2 Second-Order Low-pass Filter with Unity Gain

The transfer function of a general second order low-pass filter given in Eq. (6.6) can be used to analyse the second order low-pass and high-pass filters. A Butterworth filter is a maximally flat magnitude filter. The transfer function of the filter is designed in such a way that its magnitude is as flat as possible in the passband.

Let  $Y_1 = Y_2 = 1/R$ ,  $Y_3 = sC_3$  and  $Y_4 = sC_4$ . Then the transfer function is

$$H(s) = \frac{\frac{1}{R^2}}{\frac{1}{R^2} + sC_4 \left( \frac{2}{R} + sC_3 \right)} = \frac{1}{1 + sRC_4 (2 + sRC_3)}$$

Let the time constant  $\tau_1 = RC_3$  and  $\tau_2 = RC_4$ . Substituting  $s = j\omega$ , we get

$$H(j\omega) = \frac{1}{1 + j\omega\tau_2 (2 + j\omega\tau_1)} = \frac{1}{(1 - \omega^2\tau_1\tau_2) + j(2\omega\tau_2)}$$

Therefore, its magnitude is

$$|H(j\omega)| = \left[ (1 - \omega^2\tau_1\tau_2)^2 + (2\omega\tau_2)^2 \right]^{-1/2}$$

A maximally flat Butterworth filter will have a minimum rate of change. Therefore,

$$\frac{d|H|}{d\omega} \Big|_{\omega=0} = 0$$

Differentiating  $|H(j\omega)|$ , we obtain

$$\frac{d|H|}{d\omega} = -\frac{1}{2} \left[ (1 - \omega^2\tau_1\tau_2)^2 + (2\omega\tau_2)^2 \right]^{-3/2} \left[ -4\omega\tau_1\tau_2(1 - \omega^2\tau_1\tau_2) + 8\omega\tau_2^2 \right]$$

Letting the derivative to zero at  $\omega = 0$ , we get

$$\begin{aligned}\frac{d|H|}{d\omega} \Big|_{\omega=0} &= \left[ -4\omega\tau_1\tau_2(1 - \omega^2\tau_1\tau_2) + 8\omega\tau_2^2 \right] \\ &= 4\omega\tau_2 \left[ -\tau_1(1 - \omega^2\tau_1\tau_2) + 2\tau_2 \right]\end{aligned}$$

The above equation is satisfied when  $2\tau_2 = \tau_1$ . That is,  $C_3 = 2C_4$ . Therefore the magnitude of the transfer function becomes

$$|H| = \frac{1}{\left[1 + 4(\omega\tau_2)^4\right]^{1/2}}$$

The cut-off frequency occurs when  $|H| = \frac{1}{\sqrt{2}}$ , or  $4(\omega_{3dB}\tau_2)^4 = 1$ . Therefore,

$$\omega_{3dB} = 2\pi f_{3dB} = \frac{1}{\tau_2\sqrt{2}} = \frac{1}{\sqrt{2}RC_4}$$

We know that the cut-off frequency is  $\omega_H = \omega_{3dB} = \frac{1}{RC}$ . Comparing the above equations, we get

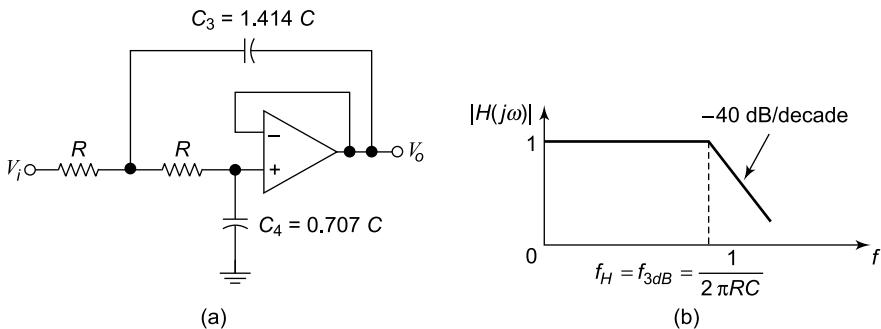
$$C_4 = 0.707C$$

$$C_3 = 1.414C$$

The magnitude of the voltage transfer function for the second order low-pass Butterworth filter is

$$|H(jf)| = \frac{1}{\sqrt{1 + \left(\frac{f}{f_H}\right)^4}}$$

The second order low-pass Butterworth filter is shown in Fig. 6.6(a). The Bode plot of the transfer function magnitude is shown in Fig. 6.6(b).



**Fig. 6.6** (a) Second order low-pass Butterworth filter with unity gain  
(b) Its Bode plot of the transfer function magnitude

### Example 6.3

Design a second-order low-pass Butterworth filter with a cut-off frequency of 10 kHz and unity gain at low frequency. Also determine the voltage transfer function magnitude in dB at 12 kHz for the filter.

**Solution** Refer to Fig. 6.6(a).

We know that

$$f_H = \frac{1}{2\pi RC}$$

Therefore,

$$RC = \frac{1}{2\pi f_H} = \frac{1}{2\pi \times 10 \times 10^3} = 15.92 \times 10^{-6}$$

Letting

$$R = 200 \text{ k}\Omega, \text{ then } C = 79.6 \text{ pF}$$

Therefore,

$$C_3 = 1.414C = 113 \text{ pF} \text{ and}$$

$$C_4 = 0.707C = 56.3 \text{ pF}$$

The voltage transfer function is

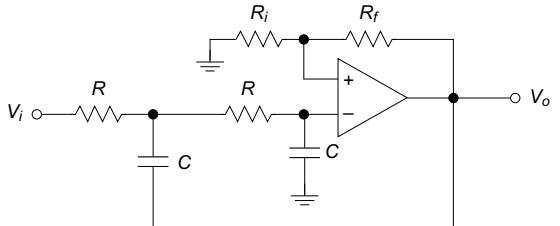
$$\begin{aligned} |H(jf)| &= \frac{1}{\sqrt{1 + \left(\frac{f}{f_H}\right)^4}} = \frac{1}{\sqrt{1 + \left(\frac{12 \times 10^3}{10 \times 10^3}\right)^4}} \\ &= 0.5704 \quad \text{i.e.} \quad 20 \log 0.5704 = -4.88 \text{ dB} \end{aligned}$$

#### 6.5.3 Second-Order Low-pass Filter with Variable Gain

To form a low-pass filter, we choose  $Y_1 = Y_2 = 1/R$  and  $Y_3 = Y_4 = sC$  as shown in Fig. 6.7(a). Here, equal value of components is used for simplicity. Therefore, the transfer function  $H(s)$  of a second order low-pass filter becomes

$$\begin{aligned} H(s) &= \frac{V_o(s)}{V_i(s)} = \frac{A \cdot \frac{1}{R^2}}{\frac{1}{R^2} + sC \left( \frac{1}{R} + \frac{1}{R} + sC \right) + \frac{sC}{R} (1-A)} \\ &= \frac{A}{1 + sCR^2 \left( \frac{2}{R} + sC \right) + sCR(1-A)} \\ &= \frac{A}{1 + s^2 C^2 R^2 + 3sCR - AsCR} \\ H(s) &= \frac{A}{s^2 C^2 R^2 + sCR(3-A) + 1} \end{aligned} \tag{6.12}$$

When  $s = 0$ ,  $H(0) = A$ ; when  $s = \infty$ ,  $H(\infty) = 0$ , which indicates that this configuration is for low-pass active filters.



**Fig. 6.7** (a) A second-order low-pass filter with variable gain

For second order physical systems such as electrical, mechanical, chemical and hydraulic, the transfer function can be expressed as

$$H(s) = \frac{A\omega_H^2}{s^2 + \alpha\omega_H s + \omega_H^2} \quad (6.13)$$

where  $A$  is the gain of the system,  $\omega_H$  is the higher cut-off frequency in rad/sec and  $\alpha$  is the damping coefficient.

Comparing Eq. (6.12) and Eq. (6.13), we obtain

$$\omega_H = \frac{1}{RC} \quad (6.14)$$

$$\alpha = (3 - A) \quad (6.15)$$

Substituting  $s = j\omega$  in Eq. (6.13), we get

$$H(j\omega) = \frac{A}{(j\omega/\omega_H)^2 + j\alpha(\omega/\omega_H) + 1} \quad (6.16)$$

The normalised expression for low-pass filter is given by

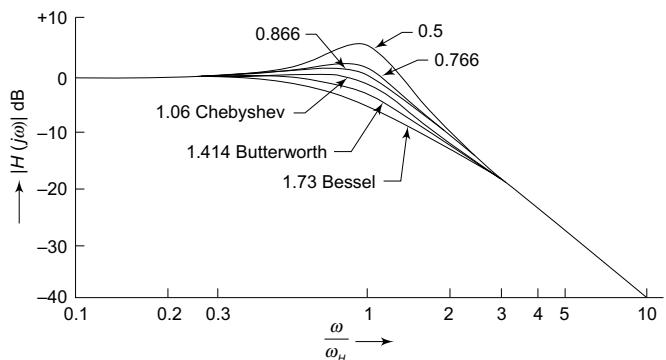
$$H(j\omega) = \frac{A}{s^2 + \alpha s + 1} \quad (6.17)$$

where normalised frequency  $s = j\left(\frac{\omega}{\omega_H}\right)$

The expression of magnitude in dB of the transfer function is

$$\begin{aligned} 20 \log |H(j\omega)| &= 20 \log \left| \frac{A}{1 + j\alpha(\omega/\omega_H) + (j\omega/\omega_H)^2} \right| \\ &= 20 \log \left[ \frac{A}{\sqrt{\left(1 - \frac{\omega^2}{\omega_H^2}\right)^2 + \left(\alpha \frac{\omega}{\omega_H}\right)^2}} \right] \end{aligned} \quad (6.18)$$

Figure 6.7(b) shows the frequency response for different values of damping coefficient  $\alpha$ . For a heavily damped filter, the response is stable. But the roll-off to the passband starts very early. For lower values of  $\alpha$ , the response overshoots and ripple appears at the early stages of passband. If  $\alpha$  is very low, then the filter becomes oscillatory. The flattest passband occurs when  $\alpha = \sqrt{2} = 1.414$ , which is called Butterworth filter response.



**Fig. 6.7 (b)** Frequency response of second order low-pass filter for different damping with unity gain ( $A = 1$ )

Therefore,

$$20 \log |H(j\omega)| = 20 \log \frac{A}{\sqrt{\left(1 + \left(\frac{\omega}{\omega_H}\right)^4\right)}} \quad (6.19)$$

Therefore, for the generalised  $N^{\text{th}}$  order low-pass Butterworth filter, the normalised transfer function is

$$\left| \frac{H(j\omega)}{A} \right| = \frac{1}{\sqrt{\left(1 + \left(\frac{\omega}{\omega_H}\right)^{2N}\right)}} \quad (6.20)$$

For the unity gain system, the above equation becomes

$$|H(j\omega)| = \frac{1}{\sqrt{\left(1 + \left(\frac{\omega}{\omega_H}\right)^{2N}\right)}} \quad (6.21)$$

### Example 6.4

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Design a second order Butterworth low-pass filter having upper cut-off frequency of 2 kHz.

**Solution** Refer to Fig. 6.6(a).

Given  $N = 2$  and  $f_H = 2 \text{ kHz} = 1/2 \pi RC$ .

Letting  $C = 0.1 \mu\text{F}$ , we get

$$R = 0.8 \text{ k}\Omega$$

The order of the filter  $N = 2$ . From the Table 6.2, we get  $\alpha = 1.414$ .

The passband gain  $A = 3 - \alpha = 3 - 1.414 = 1.586$

Hence the transfer function of second order low-pass Butterworth filter is

$$H(s) = \frac{A}{s^2 + 1.414s + 1} = \frac{1.586}{s^2 + 1.414s + 1}$$

Here,  $A = 1 + R_f/R_i = 1.586$

Therefore,  $\frac{R_f}{R_i} = 0.586$

Let  $R_f = 5.86 \text{ k}\Omega$ . Hence,  $R_i = 10 \text{ k}\Omega$

#### 6.5.4 Higher Order Low-pass Filter

It is evident that the filter order identifies the number of poles. An  $N$ -pole active low-pass filter has a high frequency roll-off rate of  $N \times 20 \text{ dB/decade}$  or  $N \times 6 \text{ dB/octave}$ , for which the 3 dB frequency is given by

$$f_{3\text{dB}} = f_H = \frac{1}{2\pi RC} \quad (6.22)$$

The magnitude of the voltage transfer function for a Butterworth  $N^{\text{th}}$  order low-pass filter is

$$|H(jf)| = \frac{1}{\sqrt{1 + \left(\frac{f}{f_H}\right)^{2N}}} \quad (6.23)$$

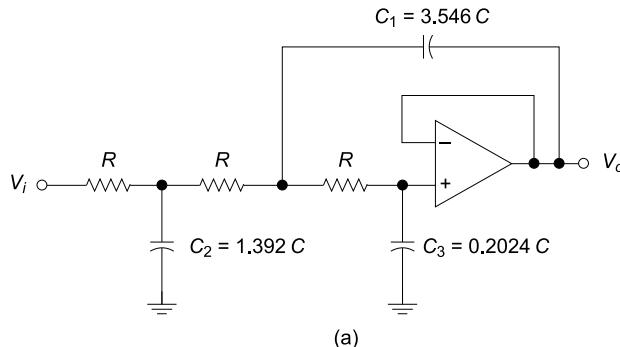
Higher order filters can be designed by adding additional  $RC$  networks, that is, by cascading a required number of first and second order filters. The transfer function of higher order filters will be of the type, as given by

$$H(s) = \frac{A_1}{s^2 + \alpha_1 s + 1} \cdot \frac{A_2}{s^2 + \alpha_2 s + 1} \cdots \frac{A}{s + 1}$$

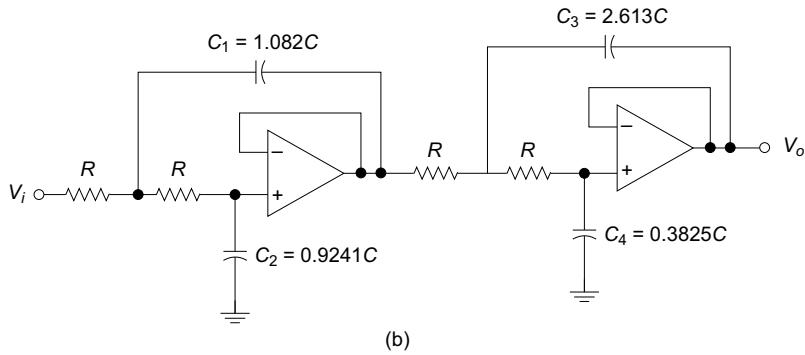
Second	Second	First
order	order	order

(6.24)

Figures 6.8(a) and (b) show the third order low-pass Butterworth filter and fourth order low-pass Butterworth filter respectively.



(a)



(b)

**Fig. 6.8** (a) Third order low-pass Butterworth filter with unity gain  
(b) Fourth order low-pass Butterworth filter with unity gain

### Example 6.5

A third order and a fourth order low-pass Butterworth filters have a cut-off frequency of 10 kHz and unity gain at low frequency. Determine the magnitude of the voltage transfer function in dB at 12 kHz for each filter.

**Solution** The voltage transfer function magnitude of the third order low-pass Butterworth filter is given by

$$|H(jf)| = \frac{1}{\sqrt{1 + \left(\frac{f}{f_H}\right)^6}} = \frac{1}{\sqrt{1 + \left(\frac{12 \times 10^3}{10 \times 10^3}\right)^6}}$$

$$= 0.5009, \text{ i.e. } 20 \log 0.5009 = -6.0053 \text{ dB}$$

The voltage transfer function magnitude of the fourth order low-pass Butterworth filter is given by

$$|H(jf)| = \frac{1}{\sqrt{1 + \left(\frac{f}{f_H}\right)^8}} = \frac{1}{\sqrt{1 + \left(\frac{12 \times 10^3}{10 \times 10^3}\right)^8}}$$

$$= 0.4343, \text{ i.e. } 20 \log 0.4343 = -7.24 \text{ dB}$$

### Example 6.6

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Design a fourth order Butterworth low-pass filter having an upper cut-off frequency of 2 kHz.

**Solution**

Given  $N = 4$  and  $f_H = 2 \text{ kHz} = 1/2 \pi RC$ .

Letting  $C = 0.1 \mu\text{F}$ , we get

$$R = 0.8 \text{ k}\Omega$$

The order of the filter is  $N = 4$ . From the Table 6.5, we get two damping factors namely  $\alpha_1 = 0.765$  and  $\alpha_2 = 1.848$ . Then the passband gain of two quadratic factors are

$$A_1 = 3 - \alpha_1 = -0.765 = 2.235$$

$$A_2 = 3 - \alpha_2 = 3 - 1.848 = 1.152$$

Hence, the transfer function of fourth order low-pass Butterworth filter is

$$\begin{aligned} H(s) &= \frac{A_1}{s^2 + 0.765s + 1} \cdot \frac{A_2}{s^2 + 1.848s + 1} \\ &= \frac{2.235}{s^2 + 0.765s + 1} \cdot \frac{1.152}{s^2 + 1.848s + 1} \end{aligned}$$

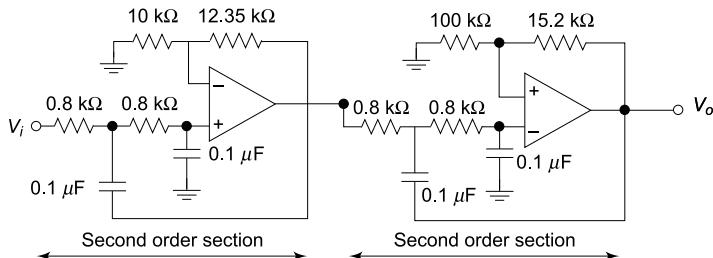
Here  $A_1 = 1 + \frac{R_{f1}}{R_{i1}} = 2.235$ . Hence  $\frac{R_{f1}}{R_{i1}} = 1.235$ .

Letting  $R_{f1} = 12.35 \text{ k}\Omega$ , we get  $R_{i1} = 10 \text{ k}\Omega$

Similarly  $A_2 = 1 + \frac{R_{f2}}{R_{i2}} = 1.152$ . Hence  $\frac{R_{f2}}{R_{i2}} = 0.152$

Letting  $R_{f2} = 15.2 \text{ k}\Omega$ , we get  $R_{i2} = 100 \text{ k}\Omega$

The realisation of fourth order Butterworth low-pass filter is shown in Fig. 6.9.



**Fig. 6.9** Realisation of fourth order Butterworth low-pass filter

## 6.6 DESIGN OF HIGH-PASS FILTERS

The high-pass filter is the complement of the low-pass filter. Hence the high-pass filter can be obtained by simply interchanging  $R$  and  $C$  in the circuit of low-pass configuration.

### 6.6.1 First-Order High-pass Filter with Unity Gain

The first order active high-pass filter with unity gain, i.e. with voltage follower is shown in Fig. 6.10(a). The voltage transfer function for this circuit is

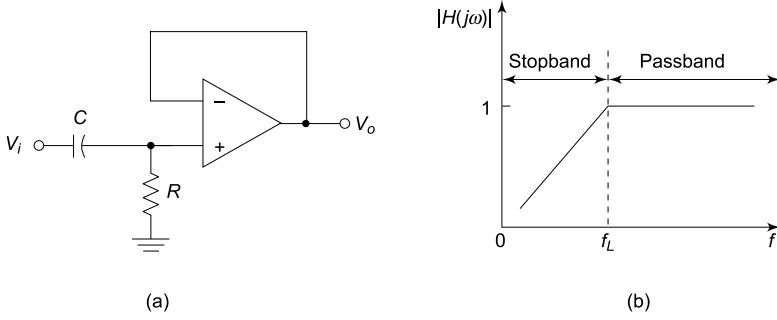
$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{R}{R + \frac{1}{sC}} = \frac{1}{1 + \frac{1}{sRC}}$$

$$H(j\omega) = \frac{1}{1 + j\left(\frac{\omega_L}{\omega}\right)} \text{ where } \omega_L = \frac{1}{RC}$$

Therefore,

$$|H(j\omega)| = \frac{1}{\sqrt{1 + \left(\frac{\omega_L}{\omega}\right)^2}} \text{ or } |H(jf)| = \frac{1}{\sqrt{1 + \left(\frac{f_L}{f}\right)^2}}$$

The Bode plot of the voltage gain magnitude curve is shown in Fig. 6.10(b). The slope of the voltage gain magnitude curve outside the passband is 6 dB/octave or 20 dB/decade. This characteristic is called the roll-off. The roll-off becomes sharper or steeper with higher-order filters.

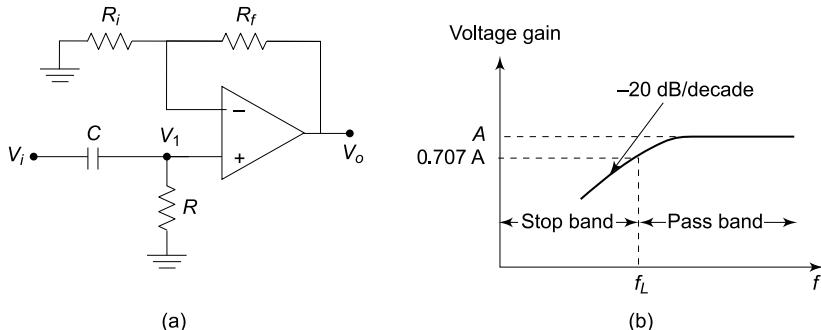


**Fig. 6.10** (a) First-order high-pass filter with voltage follower (unity gain)  
(b) Bode plot of high-pass filter with voltage follower (unity gain)

### 6.6.2 First-Order High-pass Filter with Variable Gain

The active high-pass filter with a single  $RC$  network connected to non-inverting terminal of the op-amp is shown in Fig. 6.11(a). The input resistor  $R_i$  and feedback resistor  $R_f$  are used to determine the gain of the filter in the passband. At low frequencies, the capacitor appears open, and the voltage gain approaches zero. At high frequencies, the capacitor appears shorted, and the circuit becomes a non-inverting amplifier

with a voltage gain of  $\left(1 + \frac{R_f}{R_i}\right)$ .



**Fig. 6.11** (a) First-order active high-pass filter with variable gain (b) Frequency response of an active high-pass filter

The output voltage  $V_o$  of the first order active high-pass filter is

$$V_o = \left(1 + \frac{R_f}{R_i}\right) \frac{j2\pi fRC}{1 + j2\pi fRC} V_i$$

Therefore, the gain of the filter becomes

$$\frac{V_o}{V_i} = A \left( \frac{j \left( \frac{f}{f_L} \right)}{1 + j \left( \frac{f}{f_L} \right)} \right) \quad (6.25)$$

where passband gain of the filter is  $A = 1 + \left(\frac{R_f}{R_i}\right)$ ,  $f$  is the frequency of the input signal and the lower

cut-off frequency of the filter is  $f_L = \frac{1}{2\pi RC}$ .

The frequency response of the filter is obtained from the magnitude of the filter,

$$\text{That is, } |H(jf)| = \left| \frac{V_o}{V_i} \right| = \frac{A \left( \frac{f}{f_L} \right)}{\sqrt{1 + \left( \frac{f}{f_L} \right)^2}} = \frac{A}{\sqrt{1 + \left( \frac{f_L}{f} \right)^2}} \quad (6.26)$$

At very low frequencies, i.e.  $f > f_L$ , the gain is approximately  $A$ . At frequency  $f = f_L$ , the gain falls to 0.707 times the maximum gain  $A$ . The range of frequency above  $f_L$  is called the *passband*. For frequency

$f < f_L$ , the gain decreases at a constant rate of  $-20$  dB/decade. The frequency range below the cut-off frequency is called *stop band*. The frequency response of the first order active high-pass filter is shown in Fig. 6.10(b).

It is to be noted that the high-pass second order filter is obtained from the low-pass second order filter by applying the transformation.

$$\left. \frac{s}{\omega_0} \right|_{low-pass} = \left. \frac{\omega_0}{s} \right|_{high-pass}$$

Hence, the resistors  $R$  and capacitors  $C$  are interchanged in a low-pass active filter to get a high-pass active filter.

### Example 6.7

Design a first order high-pass filter at a cut-off frequency of  $2$  kHz with a passband gain of  $2$ . Also, plot its frequency response.

**Solution** Refer to Fig. 6.14(a).

Given  $f_L = 2$  kHz

Let  $C = 0.01 \mu F$

We know that  $f_L = \frac{1}{2\pi RC}$

$$\text{Therefore, } R = \frac{1}{2\pi f_L C} = \frac{1}{2\pi(2 \times 10^3) \times 10^{-8}} = 7.95 \text{ k}\Omega$$

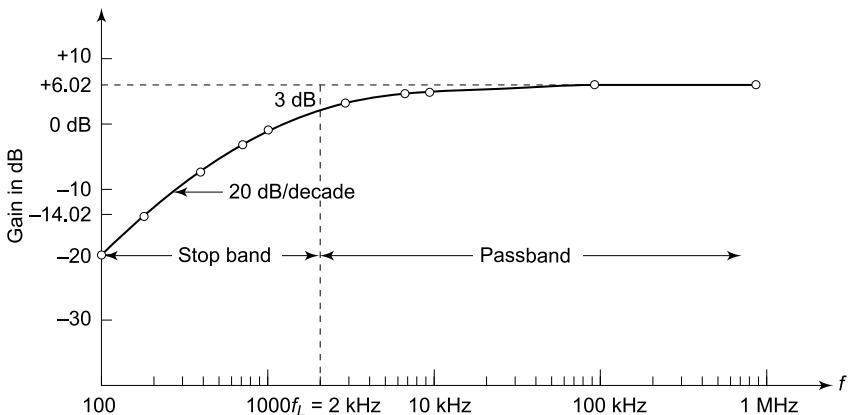
$$A = 1 + \frac{R_f}{R_i} = 2$$

Therefore,  $R_f = R_i = 10 \text{ k}\Omega$  (say)

The frequency response data for the first order high-pass filter of this example are given in Table 6.2. The plot of the resulting frequency response is shown in Fig. 6.12.

**Table 6.2** Frequency response data for the first order high-pass filter of Example 6.7

Frequency, $f$ (Hz)	Gain, $ V_o/V_i $	Gain in dB, $20 \log  V_o/V_i $
100	0.10	-20.01
200	0.20	-14.02
400	0.39	-8.13
700	0.66	-3.60
1000	0.89	-0.97
3000	1.66	4.42
7000	1.92	5.68
10000	1.96	5.85
13000	1.98	5.92
100000	2.00	6.02



**Fig. 6.12** Frequency response of first-order high-pass filter

### 6.6.3 Second-Order High-Pass Filter with Unity Gain

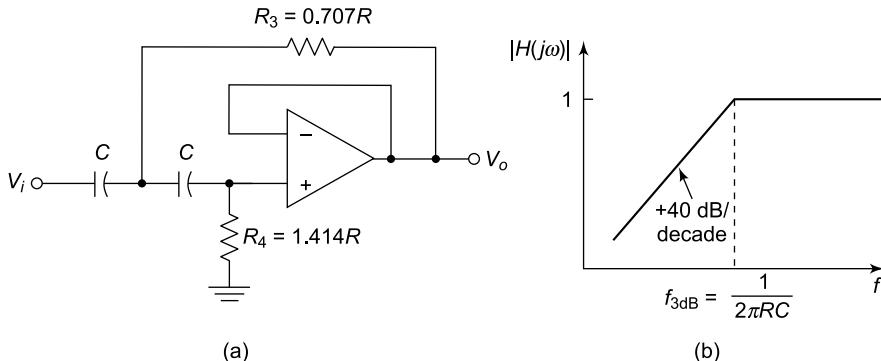
A second order high-pass Butterworth filter is shown in Fig. 6.13(a). The analysis can be done exactly the same way as for the low-pass filters except that the derivative is set equal to zero at  $s = j\omega = \infty$ . Also, the two capacitors are assumed equal. The 3dB cut-off frequency is

$$f_L = \frac{1}{2\pi RC}$$

Here, we find that  $R_3 = 0.707R$  and  $R_4 = 1.414R$ . The magnitude of the transfer function for the second order high-pass Butterworth filter is

$$|H(jf)| = \frac{1}{\sqrt{\left(1 + \left(\frac{f_L}{f}\right)^4\right)}}$$

The Bode plot of the transfer function magnitude for the second order high-pass Butterworth filter is shown in Fig. 6.13(b).



**Fig. 6.13** (a) Second order high-pass Butterworth filter with unity gain  
(b) Its Bode plot of the transfer function magnitude

### 6.6.4 Second-Order High-Pass Filter with Variable Gain

To form a high-pass filter, using Eq. (6.11) we choose  $Y_1 = Y_2 = sC$  and  $Y_3 = Y_4 = 1/R$  as shown in Fig. 6.14. Here, equal value of components is used for simplicity. Therefore, the transfer function  $H(s)$  of a second order high-pass filter becomes

$$\begin{aligned}
 H(s) &= \frac{As^2 C^2}{s^2 C^2 + \frac{1}{R} \left( 2sC + \frac{1}{R} \right) + \frac{sC}{R} (1-A)} \\
 &= \frac{As^2}{s^2 + \frac{2s}{RC} + \frac{1}{R^2 C^2} + \frac{s}{RC} (1-A)} \\
 &= \frac{As^2}{s^2 + \frac{1}{RC} (3-A)s + \frac{1}{R^2 C^2}} \\
 H(s) &= \frac{As^2}{s^2 + (3-A)\omega_L s + \omega_L^2} \tag{6.27}
 \end{aligned}$$

where  $\omega_L = \frac{1}{RC}$ .

$$H(s) = \frac{A}{1 + \frac{\omega_L}{s} (3-A) + \left( \frac{\omega_L}{s} \right)^2} \tag{6.28}$$

When  $s = 0$ ,  $H(0)=0$ , and when  $s = \infty$ ,  $H(\infty) = A$ . It is obvious that this configuration is for high-pass active filters. Therefore, the lower cut-off frequency is

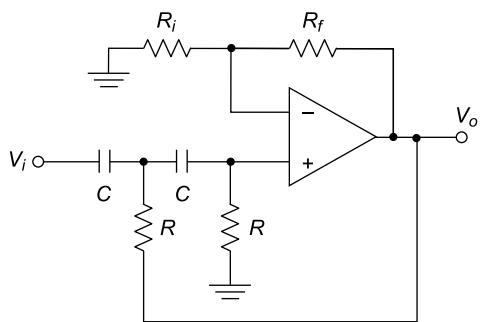
$$f_L = f_{3\text{dB}} = \frac{1}{2\pi RC} \tag{6.29}$$

Letting  $s = j\omega$  in Eq. (6.28) and  $(3 - A) = \alpha = \sqrt{2} = 1.414$ , the transfer function of second order Butterworth high-pass filter becomes

$$|H(j\omega)| = \frac{A}{\sqrt{1 + \left( \frac{\omega_L}{\omega} \right)^4}} \tag{6.30}$$

or,

$$|H(jf)| = \frac{A}{\sqrt{1 + \left( \frac{f_L}{f} \right)^4}} \tag{6.31}$$



**Fig. 6.14** Second-order high-pass filter with variable gain

Therefore, for the generalised  $N^{th}$  order high-pass Butterworth filter, the normalised transfer function is

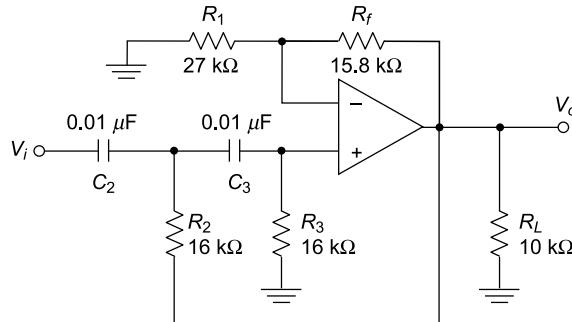
$$\left| \frac{H(j\omega)}{A} \right| = \frac{1}{\sqrt{\left( 1 + \left( \frac{\omega_L}{\omega} \right)^{2N} \right)}} \quad (6.32)$$

For the unity gain system, the above equation becomes

$$\left| H(j\omega) \right| = \frac{1}{\sqrt{\left( 1 + \left( \frac{\omega_L}{\omega} \right)^2 \right)}} \quad (6.33)$$

### Example 6.8

- (a) Find the lower cut-off frequency  $f_L$  for the second order high-pass Butterworth filter shown in Fig. 6.15. (b) Also, find the passband gain of the filter, and (c) plot the frequency response of the filter.



**Fig. 6.15** Second order high-pass Butterworth filter with variable gain

### Solution

- (a) Given  $R_2 = R_3 = 16 \text{ k}\Omega$  and  $C_2 = C_3 = 0.01 \mu\text{F}$

Therefore, the lower cut-off frequency is

$$\begin{aligned} f_L &= \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}} \\ &= \frac{1}{2\pi\sqrt{(16 \times 10^3)^2 (0.01 \times 10^{-6})^2}} \approx 1 \text{ kHz} \end{aligned}$$

- (b) The passband gain of the filter is

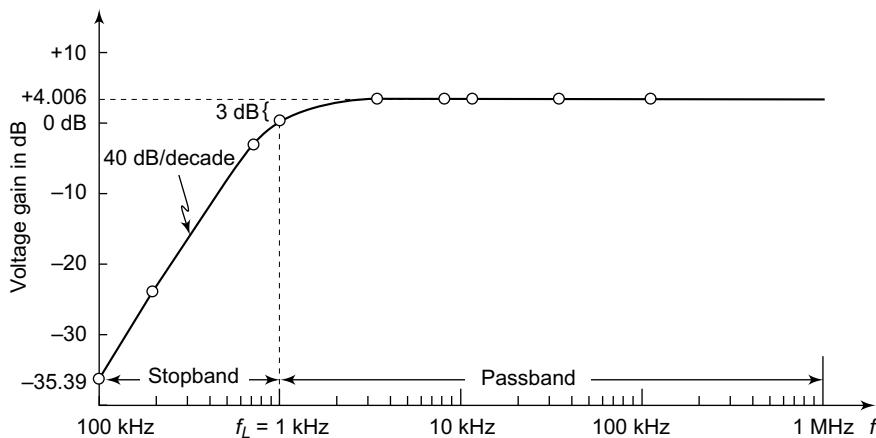
$$A = 1 + \frac{R_f}{R_i} = 1 + \frac{15.8 \times 10^3}{27 \times 10^3} = 1.586$$

The voltage gain magnitude is  $|H(jf)| = \left| \frac{V_o}{V_i} \right| = \frac{A}{\sqrt{1 + (f_L/f)^4}}$

- (c) The frequency response data for the second order high-pass filter of this example are given in Table 6.3. The plot of the resulting frequency response is shown in Fig. 6.16.

**Table 6.3** Frequency response data for the second order high-pass filter of Example 6.8

Frequency, $f$ (Hz)	Gain, $ V_o/V_i $	Gain in dB, $20 \log  V_o/V_i $
100	0.02	-35.99
200	0.06	-23.96
700	0.70	-3.12
1000	1.12	1.00
3000	1.58	3.95
7000	1.59	4.00
10000	1.59	4.01
30000	1.59	4.01
100000	1.59	4.01



**Fig. 6.16** Frequency response of second order high-pass filter

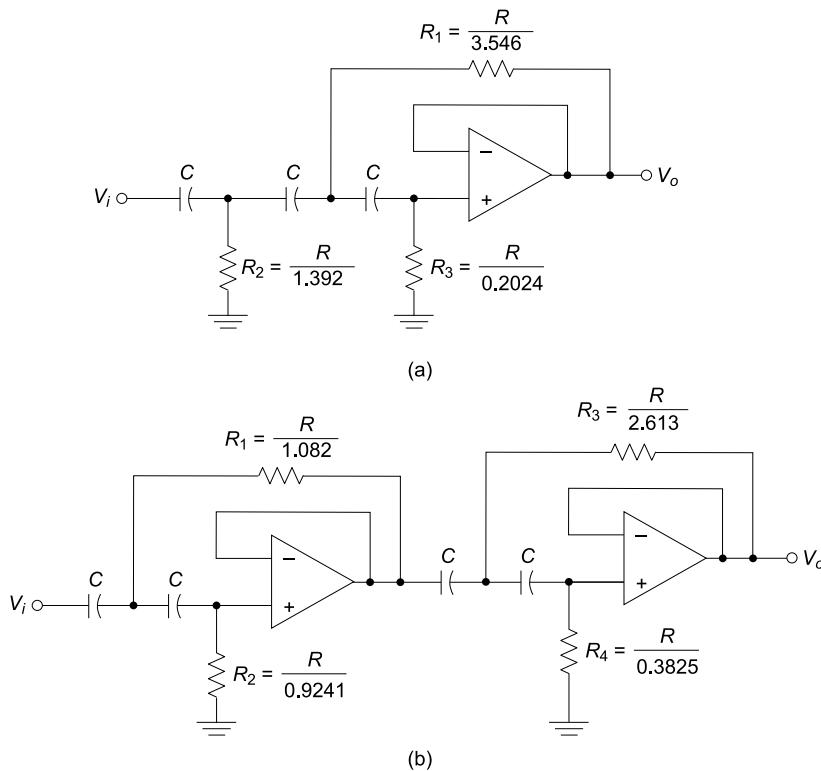
### 6.6.5 Higher Order High-pass Filter

It is known that the filter order identifies the number of poles. The response of an  $N$ -pole active high-pass filter increases at a rate of  $N \times 20$  dB/decade up to the cut-off frequency, for which the 3 dB frequency is given by

$$f_{3\text{dB}} = f_L = \frac{1}{2\pi RC} \quad (6.34)$$

The magnitude of the voltage transfer function for an  $N^{th}$  order Butterworth high-pass filter is

$$|H(jf)| = \frac{1}{\sqrt{\left(1 + \left(\frac{f_L}{f}\right)^{2N}\right)}} \quad (6.35)$$



**Fig. 6.17** (a) Third order high-pass Butterworth filter with unity gain  
(b) Fourth order high-pass Butterworth filter with unity gain

Higher order filters can be designed by adding additional \$RC\$ networks, that is, by cascading a required number of first and second order filters.

Figures 6.17(a) and (b) show the third order high-pass Butterworth filter and fourth order high-pass Butterworth filter respectively.

### Example 6.9

Design a fourth order high-pass Butterworth filter with unity gain having a cut-off frequency of 50 kHz. Determine the frequency at which the voltage transfer function magnitude is 2% of its maximum value.

#### Solution

Refer to Fig. 6.17(b).

We know that

$$f_L = \frac{1}{2\pi RC}$$

Therefore,

$$RC = \frac{1}{2\pi f_L} = \frac{1}{2\pi \times 50 \times 10^3} = 3.184 \times 10^{-6}$$

Assume \$C = 0.001\mu F\$, then \$R = 3.184\text{ k}\Omega\$

$$\text{Then, } R_1 = \frac{R}{1.082} = \frac{3.184 \times 10^3}{1.082} = 2.943 \text{ k}\Omega$$

$$R_2 = \frac{R}{0.9241} = \frac{3.184 \times 10^3}{0.9241} = 3.446 \text{ k}\Omega$$

$$R_3 = \frac{R}{2.613} = \frac{3.184 \times 10^3}{2.613} = 1.219 \text{ k}\Omega$$

$$R_4 = \frac{R}{0.3825} = \frac{3.184 \times 10^3}{0.3825} = 8.324 \text{ k}\Omega$$

When the voltage transfer function magnitude of the fourth order high-pass Butterworth filter is 2% of its maximum value, then

$$|H(jf)| = \frac{1}{\sqrt{1 + \left(\frac{f_L}{f}\right)^8}}$$

That is,

$$0.02 = \frac{1}{\sqrt{1 + \left(\frac{50 \times 10^3}{f}\right)^8}}$$

Upon solving, we get

$$f = 11.18 \text{ kHz}$$

## 6.7 BANDPASS FILTERS

A bandpass filter passes a particular band of frequencies and attenuates any input frequency outside this passband. The bandpass filter has a passband between higher cut-off frequency  $f_H$  and lower cut-off frequency  $f_L$  such that  $f_H > f_L$ . This filter has a maximum gain at the resonant frequency ( $f_r$ ), which is defined as

$$f_r = \sqrt{f_H f_L}$$

The *figure of merit* or *quality factor*  $Q$ , is given by

$$Q = \frac{f_r}{f_H - f_L} = \frac{f_r}{B}$$

where  $B$  is the bandwidth. A filter with high  $Q$  selects a smaller band of frequencies (more selective).

If the resonant frequency ( $f_r$ ) and Bandwidth ( $B$ ) are known, then the cut-off frequencies can be determined from

$$f_L = \sqrt{\frac{B^2}{4} + f_r^2} - \frac{B}{2}$$

and

$$f_H = f_L + B$$

The bandpass filters can be classified as (i) wideband bandpass filter and (ii) narrowband bandpass filter.

### Example 6.10

If a bandpass filter has a lower cut-off frequency  $f_L = 250 \text{ Hz}$  and a higher cut-off frequency  $f_H = 2500 \text{ Hz}$ , then find its bandwidth and the resonant frequency.

**Solution** The bandwidth of the bandpass filter is

$$B = f_H - f_L = 2500 - 250 = 2250 \text{ Hz}$$

The resonant frequency of the bandpass filter is

$$f_r = \sqrt{f_H f_L} = \sqrt{2500 \times 250} = 790.56 \text{ Hz}$$

Here, the centre frequency is  $(250 + 2500)/2 = 1375 \text{ Hz}$ . Hence it proves that the resonant frequency is always less than the centre frequency.

### Example 6.11

Given a bandpass filter with resonant frequency  $f_r$  of 1000 Hz and a bandwidth ( $B$ ) of 3000 Hz, find its (a) quality factor; (b) lower cut-off frequency and (c) higher cut-off frequency.

**Solution**

(a) We know that the figure of merit or quality factor  $Q$  is given by

$$Q = \frac{f_r}{f_H - f_L} = \frac{f_r}{B} = \frac{1000}{3000} = 0.33$$

Since  $Q < 0.5$ , this filter is a wideband filter.

(b) We know that the lower cut-off frequency of the bandpass filter is

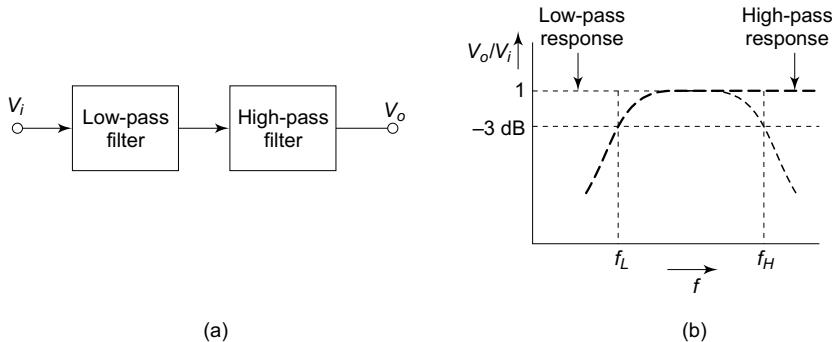
$$f_L = \sqrt{\frac{B^2}{4} + f_r^2} - \frac{B}{2} = \sqrt{\frac{(3000)^2}{4} + (1000)^2} - \frac{3000}{2} = 302.77 \text{ Hz}$$

(c) The upper cut-off frequency is

$$f_H = f_L + B = 302.77 + 3000 = 3302.77 \text{ Hz}$$

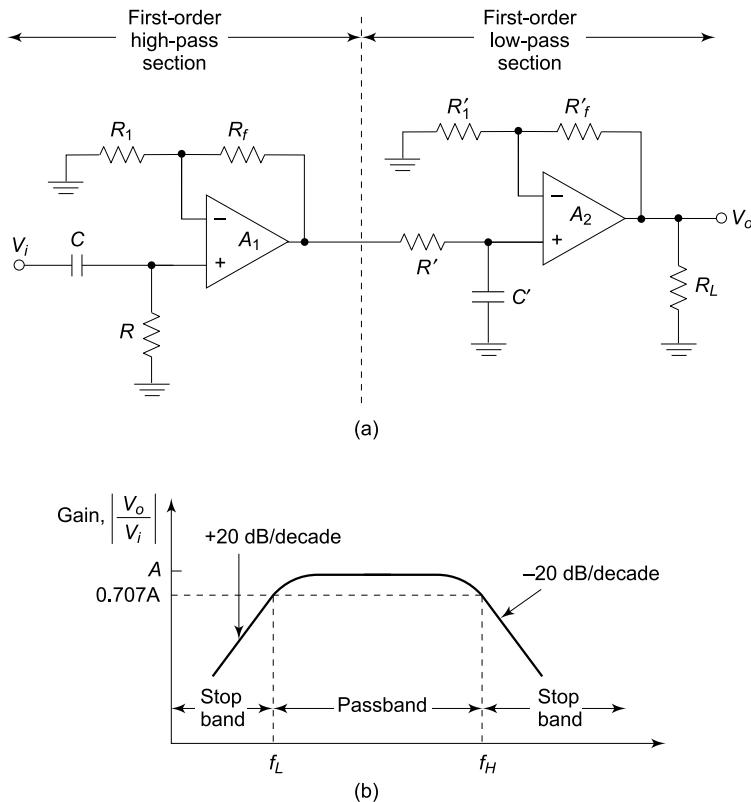
#### 6.7.1 Wideband Bandpass Filter

A bandpass filter can be constructed simply by connecting low-pass and high-pass filters in cascade as shown in Fig. 6.18(a). Here the low-pass circuit will pass all frequencies up to its cut-off frequency  $f_H$ , while the high-pass circuit will block all frequencies below its cut-off frequency  $f_L$ , provided  $f_H > f_L$ , i.e.  $f_H$  must be at least 10 times  $f_L$ . The cut-off frequencies of the low and high-pass sections must have the equal passband gain. Hence, the combination gives a filter with passband from  $f_L$  to  $f_H$  as shown in Fig. 6.18(b).



**Fig. 6.18** (a) Cascaded low-pass and high-pass filters acting as bandpass filter  
(b) Frequency response of the bandpass filter

For realising a  $\pm 20$  dB/decade bandpass filter, first-order high-pass and first-order low-pass sections are cascaded as shown in Fig. 6.19(a), in which  $A_1$  and  $A_2$  are dual op-amps 1458/353. Its frequency response is shown in Fig. 6.19(b). For realising a  $\pm 40$  dB/decade bandpass filter, second-order high-pass and second-order low-pass sections can be cascaded and so on.



**Fig. 6.19** (a)  $\pm 20$  dB/decade-wide bandpass filter (b) Its frequency response

### 6.7.2 Narrowband Bandpass Filter

The narrowband bandpass filter using one inverting mode op-amp with two feedback paths is shown in Fig. 6.20(a) and its frequency response is shown in Fig. 6.20(b). The resonant frequency can be changed by adjusting  $R_r$  without changing the bandwidth or gain. The bandwidth  $B$  is determined by resistor  $R$  and the two matched capacitors  $C$  as given by

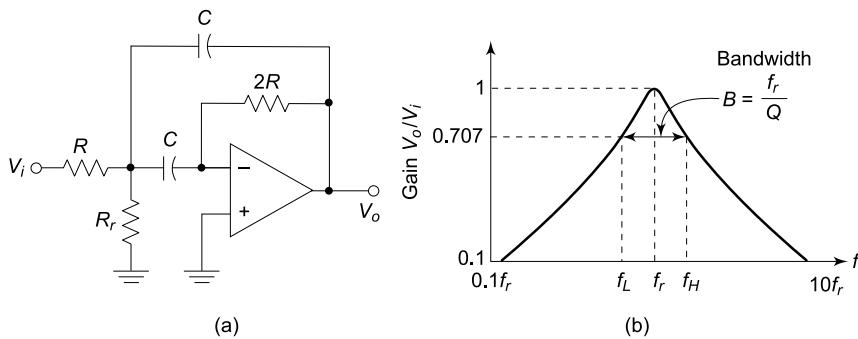
$$B = \frac{0.1591}{RC}$$

where  $B = f_r/Q$ . The adjustable resistor  $R_r$  is determined by

$$R_r = \frac{R}{2Q^2 - 1}$$

Its resonant frequency  $f_r$  is determined from

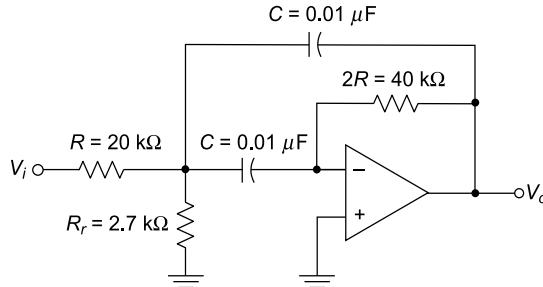
$$f_r = \frac{0.1125}{RC} \sqrt{1 + \frac{R}{R_r}}$$



**Fig. 6.20** (a) Narrowband bandpass filter circuit (b) Its frequency response

### Example 6.12

Given a bandpass filter with the component values shown in Fig. 6.21, find its (a) resonant frequency and (b) bandwidth.



**Fig. 6.21** Narrowband bandpass filter

#### Solution

(a) The resonant frequency of the bandpass filter is

$$\begin{aligned} f_r &= \frac{0.1125}{RC} \sqrt{1 + \frac{R}{R_r}} \\ &= \frac{0.1125}{(20 \times 10^3)(0.01 \times 10^{-6})} \sqrt{1 + \frac{20 \times 10^3}{2.7 \times 10^3}} \approx 1631 \text{ Hz} \end{aligned}$$

(b) The bandwidth of the bandpass filter is

$$B = \frac{0.1591}{RC} = \frac{0.1591}{(20 \times 10^3)(0.01 \times 10^{-6})} = 795.5 \text{ Hz}$$

### Example 6.13

Design a narrowband bandpass filter with a resonant frequency of 200 Hz and a bandwidth of 20 Hz.

#### Solution

Here

$$Q = \frac{f_r}{B} = \frac{200}{20} = 10$$

Let

$$C = 0.33 \mu\text{F}$$

We know that  $R = \frac{0.1591}{BC} = \frac{0.1591}{20(0.33 \times 10^{-6})} = 24.1 \text{ k}\Omega$

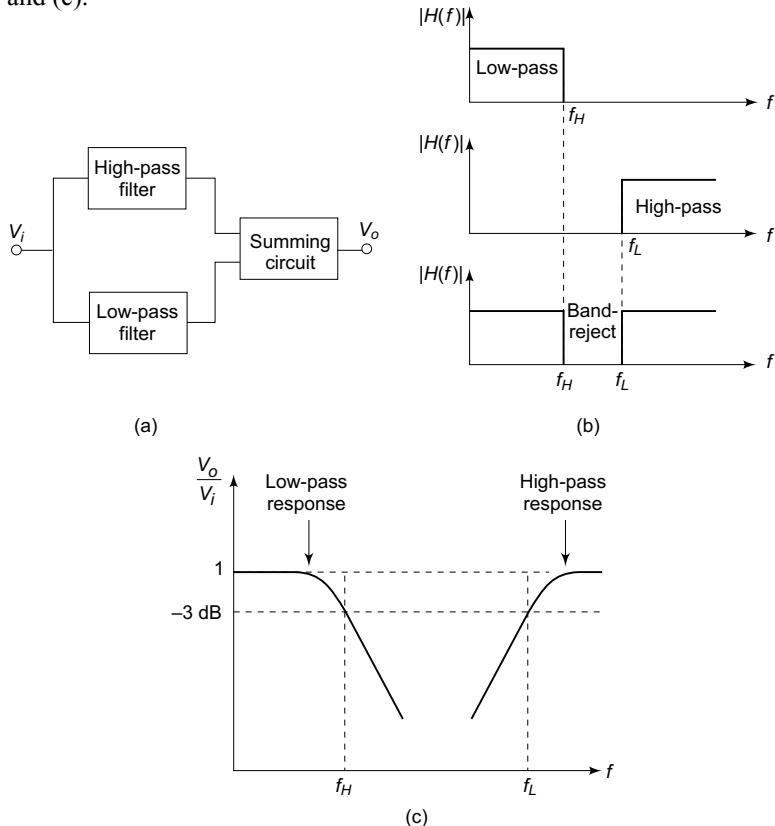
$$R_r = \frac{R}{2Q^2 - 1} = \frac{24.1 \times 10^3}{2 \times 10^2 - 1} = 121.1 \Omega$$

## 6.8 BAND-REJECT FILTERS

The band-reject filter, often called the *band-elimination* or *band-stop* filter, attenuates the frequencies in the stopband and passes them outside this band. The band-reject filter can be classified as (i) wideband band-reject filter, and (ii) narrowband band-reject filter.

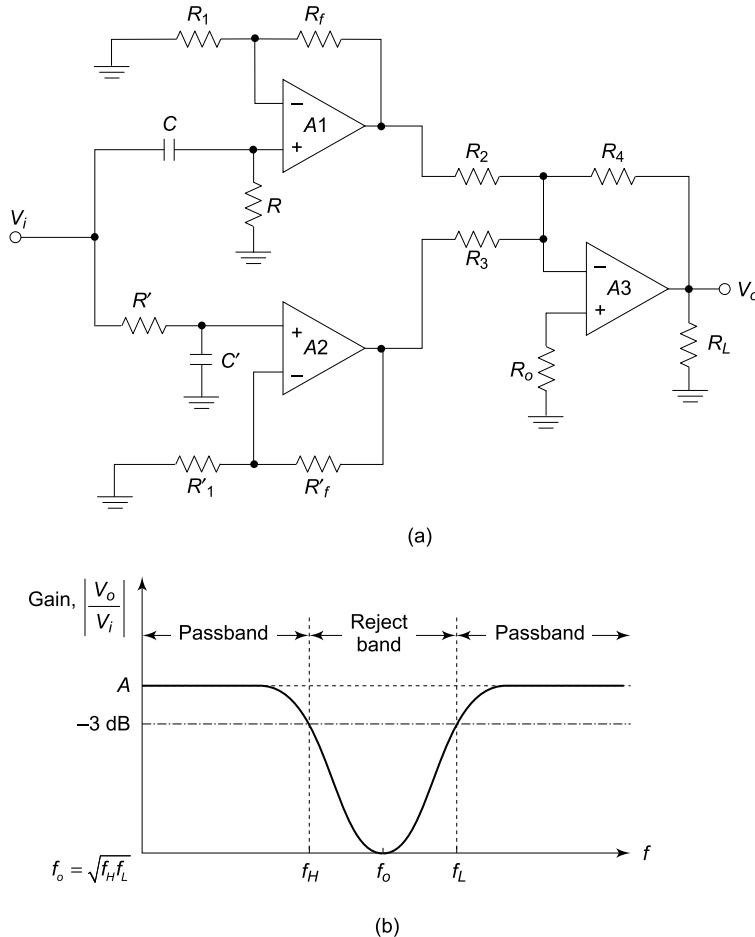
### 6.8.1 Wideband Band-reject Filter

A band-reject filter or bandstop filter can be constructed by parallel connecting a low-pass filter and a high-pass filter as shown in Fig. 6.22(a). The inputs are connected in parallel, and the outputs should be applied to a summing circuit in order to avoid one input overloading the other. Here, the low-pass circuit will block all frequencies above its cut-off frequency  $f_H$ , while the high-pass circuit will block frequencies below its cut-off frequency  $f_L$ , provided  $f_L > f_H$ . The result is a stopband of  $f_L$  to  $f_H$  as shown in Fig. 6.22(b) and (c).



**Fig. 6.22** (a) Parallel combination of low-pass and high-pass filters results in a band-reject filter,  
 (b) Ideal band-reject filter frequency response  
 (c) Practical frequency response of the band-reject filter

Figure 6.23(a) shows a wideband band-reject filter that is obtained by paralleling a high-pass filter with a cut-off frequency of  $f_L$  with a low-pass filter with cut-off frequency of  $f_H$ , provided  $f_L > f_H$  and a summing amplifier connected in series to add the filtered individual passband components. The passband gains of both the high-pass and low-pass sections must be equal. The frequency response characteristic of the wideband band-reject filter is shown in Fig. 6.23(b).



**Fig. 6.23** (a) Circuit of a wideband band-reject filter (b) Its frequency response

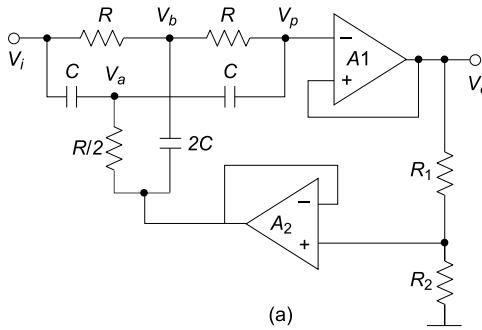
The amplifiers  $A_1$ ,  $A_2$  and  $A_3$  can be obtained by using the quad op-amp  $\mu\text{AF774}$  or  $\text{MC34004}$ . The design of the filter is based on the design of individual sections of the circuit. The passband gain can also be suitably selected. If the gain is set at 1, then  $R_2 = R_3 = R_4$ . The value of  $R_o$  is parallel combination of  $R_2$ ,  $R_3$  and  $R_4$ .

### 6.8.2 Narrowband Band-reject Filter (Notch filter)

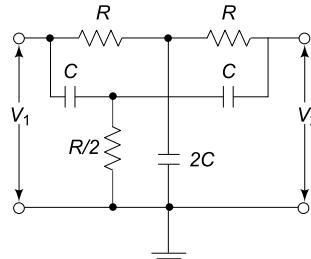
The narrowband band-reject filter, often called the *notch filter*, is the *twin-T* network cascaded with the voltage follower as shown in Fig. 6.24(a). By using the Star-Delta conversion formulae, the *Twin-T* network shown in Fig. 6.24(b) can be modified as equivalent delta network shown in Fig. 6.24(c).

$$Z_1 = Z_3 = \frac{sCR + 1}{2sC}$$

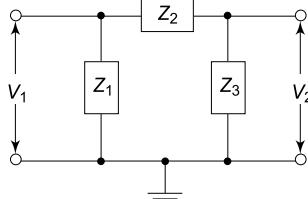
$$Z_2 = \frac{2R(sCR + 1)}{(s^2 R^2 C^2 + 1)}$$



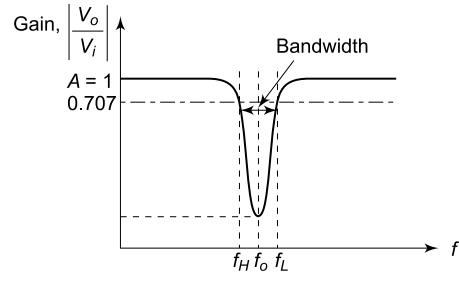
(a)



(b)



(c)



(d)

**Fig. 6.24** (a) Circuit of a narrowband band-reject (notch) filter (b) Twin-T network, (c) Equivalent Delta network (d) Its frequency response

From Fig. 6.24(c), we can get the relation expressed by

$$\frac{V_2}{V_1} = \frac{s^2 C^2 R^2 + 1}{s^2 C^2 R^2 + 4sCR + 1}$$

By substituting  $s = j\omega$ , the above equation becomes

$$\frac{V_2}{V_1} = \frac{1 - \omega^2 C^2 R^2}{1 - \omega^2 C^2 R^2 + j4\omega RC}$$

By setting the real part to be zero, we get the notch-out frequency  $f_o$ , at which the maximum attenuation occurs as given by

$$f_o = \frac{1}{2\pi RC}$$

Applying Kirchhoff's current law at node  $V_a$ , we get

$$(V_i - V_a)sC + (V_o - V_a)sC + (KV_o - V_a)2G = 0$$

$$\text{or } sCV_i + (sC + 2KG)V_o = 2(sC + G)V_a$$

where

$$K = \frac{R_2}{(R_1 + R_2)} \text{ and } G = \frac{1}{R}$$

Applying Kirchhoff's current law at node  $V_b$ , we get

$$(V_i - V_b)G + (V_o - V_b)G + 2(KV_o - V_b)sC = 0$$

or

$$GV_i + (G + 2KsC)V_o = 2(G + sC)V_b$$

At node  $V_p$ ,

$$(V_a - V_o)sC + (V_b - V_o)G = 0$$

or

$$sCV_a + GV_b = (G + sC)V_o$$

From the above three node voltage equations, the transfer function can be written as,

$$\begin{aligned} H(s) &= \frac{V_o(s)}{V_i(s)} = \frac{G^2 + s^2 C^2}{G^2 + s^2 C^2 + 4(1-K)sCG} \\ &= \frac{s^2 + \left(\frac{G}{C}\right)^2}{s^2 + \left(\frac{G}{C}\right)^2 + 4(1-K)s\left(\frac{G}{C}\right)} \end{aligned}$$

In the steady-state, that is  $s = j\omega$ ,

$$H(j\omega) = \frac{\omega^2 - \omega_o^2}{\omega^2 - \omega_o^2 - j4(1-K)\omega\omega_o}$$

$$\text{where } \omega_o = \frac{G}{C} = \frac{1}{RC} \text{ or } f_o = \frac{1}{2\pi RC}$$

From the above equation  $H(j\omega)$  becomes zero for  $\omega = \omega_o$  and approaches unity as  $\omega \ll \omega_o$  and for  $\omega \gg \omega_o$ . In practice, the high frequency response will be limited by the high frequency response characteristics of the op-amp. At 3dB cut-off frequency,  $|H| = \frac{1}{\sqrt{2}}$

$$\text{Therefore, } \omega^2 - \omega_o^2 = \pm 4(1-K)\omega\omega_o$$

$$\text{or } \left(\frac{\omega}{\omega_o}\right)^2 \pm 4(1-K)\left(\frac{\omega}{\omega_o}\right) - 1 = 0$$

Upon solving the above quadratic equation, we obtain the upper and lower half power frequencies as,

$$f_H = f_o \left[ \sqrt{1 + 4(1-K)^2} + 2(1-K) \right]$$

and

$$f_L = f_o \left[ \sqrt{1 + 4(1-K)^2} - 2(1-K) \right]$$

The 3 dB bandwidth is

$$B = f_H - f_L = 4(1-K)f_o$$

$$Q = \frac{f_o}{B} = \frac{1}{4(1-K)}$$

As  $K$  approaches unity,  $Q$  factor becomes very large and  $B$  approaches zero. In fact, mismatches between resistors and capacitors limit the  $Q$  factor and bandwidth ( $B$ ) to a practically realisable value.

The frequency response of the active notch filter is shown in Fig. 6.24(d). These notch filters are used in communications and bio-medical instrumentation applications to eliminate the undesired frequencies. They are also useful for the rejection of a single frequency, such as 50 or 60 Hz power line frequency hum.

## 6.9 FREQUENCY TRANSFORMATION

There are basically four types of frequency selective filters, viz. low-pass, high-pass, bandpass and bandstop. In the design techniques discussed so far, we have considered only low-pass filters. This low-pass filter can be considered as a prototype filter and its system function can be obtained. Then, if a high-pass or bandpass or bandstop filter is to be designed, it can be easily obtained by using frequency transformation. Frequency transformation can be accomplished in two ways. In the analog frequency transformation, the analog system function  $H_p(s)$  of the prototype filter is converted into another analog system function  $H(s)$  of the desired filter.

**Analog frequency transformation** The frequency transformation formulae used to convert a prototype low-pass filter into a low-pass (with a different cut-off frequency), high-pass, bandpass or bandstop are given below.

- (i) Low-pass with cut-off frequency  $\omega_c$  to low-pass with a new cut-off frequency  $\omega_c^*$

$$s \rightarrow \frac{\omega_c}{\omega_c^*} s$$

Thus, if the system response of the prototype filter is  $H_p(s)$ , the system response of the new low-pass filter will be

$$H(s) = H_p \left( \frac{\omega_c}{\omega_c^*} s \right)$$

- (ii) Low-pass with cut-off frequency  $\omega_c$  to high-pass cut-off frequency  $\omega_c^*$

$$s \rightarrow \frac{\omega_c \omega_c^*}{s}$$

The system function of the high-pass filter is then,

$$H(s) = H_p \left( \frac{\omega_c \omega_c^*}{s} \right)$$

- (iii) Low-pass with cut-off frequency  $\omega_c$  to bandpass with lower cut-off frequency  $\omega_1$  and higher cut-off frequency  $\omega_2$

$$s \rightarrow \omega_c \frac{s^2 + \omega_1 \omega_2}{s(\omega_2 - \omega_1)}$$

The system function of the high-pass filter is then

$$H(s) = H_p \left( \omega_c \frac{s^2 + \omega_1 \omega_2}{s(\omega_2 - \omega_1)} \right)$$

- (iv) Low-pass with cut-off frequency  $\omega_c$  to bandstop with lower cut-off frequency  $\omega_1$  and higher cut-off frequency  $\omega_2$

$$s \rightarrow \omega_c \frac{s(\omega_2 - \omega_1)}{s^2 + \omega_1 \omega_2}$$

The system function of the bandstop filter is then

$$H(s) = H_p \left( \omega_c \frac{s(\omega_2 - \omega_1)}{s^2 + \omega_1 \omega_2} \right)$$

Table 6.4 gives the analog frequency transformations formulae.

**Table 6.4** Analog frequency transformation

Type	Transformation
Low-pass	$s \rightarrow \frac{\omega_c}{\omega_c^*} s$
High-pass	$s \rightarrow \frac{\omega_c \omega_c^*}{s}$
Bandpass	$s \rightarrow \omega_c \frac{s^2 + \omega_1 \omega_2}{s(\omega_2 - \omega_1)}$
Band stop	$s \rightarrow \omega_c \frac{s(\omega_2 - \omega_1)}{s^2 + \omega_1 \omega_2}$

## 6.10 FILTER APPROXIMATIONS

The rate at which the response of a filter falls in the transition band is determined by the order of the filter. When the order of the filter is higher, the *roll-off* rate becomes faster. The order of the filter is derived from the transfer function of the filter. Besides the order, the type of filter determines the shape of the transition band. This is reflected by its *damping factor*.

The popular alignment types are Chebyshev, Butterworth, Elliptic and Bessel approximations. The Chebyshev approximation provides a low-pass response that is equiripple in the passband with the transmission decreasing monotonically in the stopband. All the transmission zeros are at  $s = \infty$ .

The Butterworth approximation provides a low-pass response that is maximally flat at  $\omega = 0$  and it is characterised by its moderate amplitude and phase response. The transmission decreases monotonically as  $\omega$  increases, reaching 0 (infinite attenuation) at  $\omega = \infty$ , where all  $N$  transmission zeros lie. It exhibits the fastest roll-off of any monotonic or smooth filter. This is the only filter whose 3dB frequency equals its critical frequency ( $f_{3dB} = f_c$ ). Hence, the Butterworth approximation is widely used in the design of active filters.

### 6.10.1 Butterworth Filters

The Butterworth low-pass filter has a magnitude response given by

$$|H(j\omega)| = \frac{A}{\sqrt{1 + \left(\frac{\omega}{\omega_c}\right)^{2N}}} \quad (6.36)$$

where  $A$  is the filter gain and  $\omega_c$  is the 3dB cut-off frequency and  $N$  is the order of the filter. The magnitude response of the Butterworth filter is shown in Fig. 6.25. The magnitude response has a maximally flat passband and stopband. It can be seen that by increasing the filter order  $N$ , the Butterworth filter response approximates the ideal response. However, the phase response of the Butterworth filter becomes increasingly non-linear with higher values of  $N$ .

The design parameters of the Butterworth filter are obtained by considering the low-pass filter with the desired specifications as given below.

$$\delta_1 \leq |H(e^{j\omega})| \leq 1, \quad 0 \leq \omega \leq \omega_1$$

$$|H(e^{j\omega})| \leq \delta_2, \quad \omega_2 \leq \omega \leq \pi$$

The corresponding analog magnitude response is to be obtained in the design process. Using the above equations and if  $A = 1$ , we get

$$\delta_1^2 \leq \frac{1}{1 + (\omega_1/\omega_c)^{2N}} \leq 1$$

$$\frac{1}{1 + (\omega_2/\omega_c)^{2N}} \leq \delta_2^2$$

This equation can be written in the form

$$(\omega_1/\omega_c)^{2N} \leq \frac{1}{\delta_1^2} - 1 \quad (6.37a)$$

$$(\omega_2/\omega_c)^{2N} \leq \frac{1}{\delta_2^2} - 1 \quad (6.37b)$$

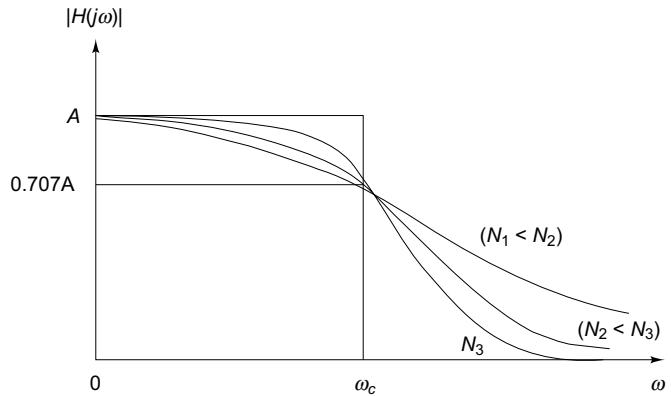
Equality is assumed in Eqs. (6.37a and b) in order to obtain the filter order  $N$  and the 3dB cut-off frequency  $\omega_c$ . Dividing Eq. (6.37b) by Eq. (6.37a), we get

$$(\omega_2/\omega_1)^{2N} = (1/\delta_2^2 - 1)/(1/\delta_1^2 - 1)$$

From the above equation, the order of the filter  $N$  is given by

$$N = \frac{1}{2} \frac{\log \left[ \left( (1/\delta_2^2 - 1)/(1/\delta_1^2 - 1) \right) \right]}{\log (\omega_2/\omega_1)} \quad (6.38)$$

The value of  $N$  is chosen to be the next nearest integer to the value of  $N$  as given by Eq. (6.38).



**Fig. 6.25** Magnitude response of a Butterworth low-pass filter

Using Eq. (6.37a), we get

$$\omega_C = \frac{\omega_l}{\left[\left(1/\delta_l^2\right) - 1\right]^{1/2N}} \quad (6.39)$$

The transfer function of the Butterworth filter is usually written in the factored form as given below.

$$H(s) = \prod_{k=1}^{N/2} \frac{B_k \omega_c^2}{s^2 + b_k \omega_c s + c_k \omega_c^2} \quad N = 2, 4, 6, \dots$$

$$\text{or} \quad H(s) = \frac{B_0 \omega_c}{s + c_0 \omega_c} \prod_{k=1}^{(N-1)/2} \frac{B_k \omega_c^2}{s^2 + b_k \omega_c s + c_k \omega_c^2} \quad N = 3, 5, 7, \dots \quad (6.40)$$

The coefficients  $b_k$  and  $c_k$  are given by

$$b_k = 2 \sin[(2k-1)\pi/2N] \text{ and } c_k = 1$$

The parameter  $B_k$  can be obtained from

$$A = \prod_{k=1}^{N/2} B_k, \text{ for even } N$$

$$\text{and} \quad A = \prod_{k=1}^{(N-1)/2} B_k, \text{ for odd } N$$

**Note:** If the passband attenuation  $\alpha_p$  and the stopband attenuation  $\alpha_s$  are specified in dBs, then they can be related with  $\delta_l$  and  $\delta_2$  respectively as follows:

$$\alpha_p = 20 \log \frac{1}{\delta_l}, \text{ i.e. } \frac{1}{\delta_l^2} = 10^{0.1\alpha_p} \quad (6.41)$$

$$\alpha_s = 20 \log \frac{1}{\delta_2}, \text{ i.e. } \frac{1}{\delta_2^2} = 10^{0.1\alpha_s} \quad (6.42)$$

**Poles of a normalised Butterworth filter** The Butterworth low-pass filter has a magnitude squared response given by

$$|H(j\omega)|^2 = \frac{1}{1 + (\omega/\omega_c)^{2N}}$$

For a normalised filter,  $\omega_c = 1$ . Thus,

$$|H(j\omega)|^2 = \frac{1}{1 + \omega^{2N}}$$

The normalised poles in the  $s$ -domain can be obtained by substituting  $\omega = s/j$  and equating the denominator polynomial to zero, i.e.

$$1 + \left(\frac{s}{j}\right)^{2N} = 0, \text{ or } 1 + (-s^2)^N = 0$$

The solution to the above expression gives us the poles of the filter. The above expression can be written as

$$(-1)^N s^{2N} = -1$$

Expressing  $-1$  in the polar form,

$$(-1)^N s^{2N} = e^{j(2n-1)\pi} *, n = 1, 2, \dots, N$$

The poles in the left-half of the  $s$ -plane are given by,

$$s_n = \sigma_n + j\omega_n = e^{j(2n+N-1)\pi/2N} = je^{j(2n-1)\pi/2N}$$

Using the polar to rectangular conversion,  $e^{j\theta} = \cos \theta + j \sin \theta$ , the normalised poles are obtained as

$$s_n = -\sin\left(\frac{2n-1}{2N}\right)\pi + j\cos\left(\frac{2n-1}{2N}\right)\pi$$

where  $n = \begin{cases} 1, 2, \dots, (N+1)/2, & \text{for } N \text{ odd} \\ 1, 2, \dots, N/2, & \text{for } N \text{ even} \end{cases}$

The un-normalised poles  $s'_n$ , can also be obtained from the normalised poles as shown below,

$$s'_n = s_n (\omega_c)^{-1/N}$$

The normalised poles lie on the unit circle spaced  $\pi/N$  apart.

**Butterworth polynomials** The Butterworth polynomials are given in Table 6.5.

**Table 6.5 Butterworth polynomials**

<i>N</i>	<i>Factors</i>	<i>Polynomial</i>
1	$s + 1$	$s + 1$
2	$s^2 + \sqrt{2}s + 1$	$s^2 + \sqrt{2}s + 1$
3	$(s + 1), (s^2 + s + 1)$	$s^3 + 2s^2 + 2s + 1$
4	$(s^2 + 0.765s + 1), (s^2 + 1.848s + 1)$	$s^4 + 2.613s^3 + 3.414s^2 + 2.613s + 1$
5	$(s + 1), (s^2 + 0.618s + 1), (s^2 + 1.618s + 1)$	$s^5 + 3.236s^4 + 5.236s^3 + 5.236s^2 + 3.236s + 1$
6	$(s^2 + 0.518s + 1), (s^2 + \sqrt{2}s + 1), (s^2 + 1.932s + 1)$	$s^6 + 3.864s^5 + 7.464s^4 + 9.142s^3 + 7.464s^2 + 3.864s + 1$
7	$(s + 1), (s^2 + 0.44s + 1),$ $(s^2 + 1.247s + 1), (s^2 + 1.802s + 1)$	$s^7 + 4.494s^6 + 10.098s^5 + 14.592s^4 +$ $14.592s^3 + 10.098s^2 + 4.494s + 1$
8	$(s^2 + 0.3s + 1), (s^2 + 1.111s + 1),$ $(s^2 + 1.166s + 1), (s^2 + 1.962s + 1)$	$s^8 + 5.126s^7 + 13.137s^6 + 21.846s^5 +$ $25.688s^4 + 21.846s^3 + 13.137s^2 + 5.126s + 1$
9	$(s + 1), (s^2 + 0.347s + 1), (s^2 + s + 1),$ $(s^2 + 1.532s + 1), (s^2 + 1.879s + 1)$	$s^9 + 5.759s^8 + 16.582s^7 + 31.163s^6 + 41.986s^5 +$ $41.986s^4 + 31.163s^3 + 16.582s^2 + 5.757s + 1$
10	$(s^2 + 0.313s + 1), (s^2 + 0.908s + 1),$ $(s^2 + \sqrt{2}s + 1), (s^2 + 1.792s + 1),$ $(s^2 + 1.975s + 1)$	$s^{10} + 6.393s^9 + 20.432s^8 + 42.802s^7 +$ $64.882s^6 + 74.233s^5 + 64.882s^4 + 42.802s^3 +$ $20.432s^2 + 6.393s + 1$

## 6.10.2 Chebyshev Filters

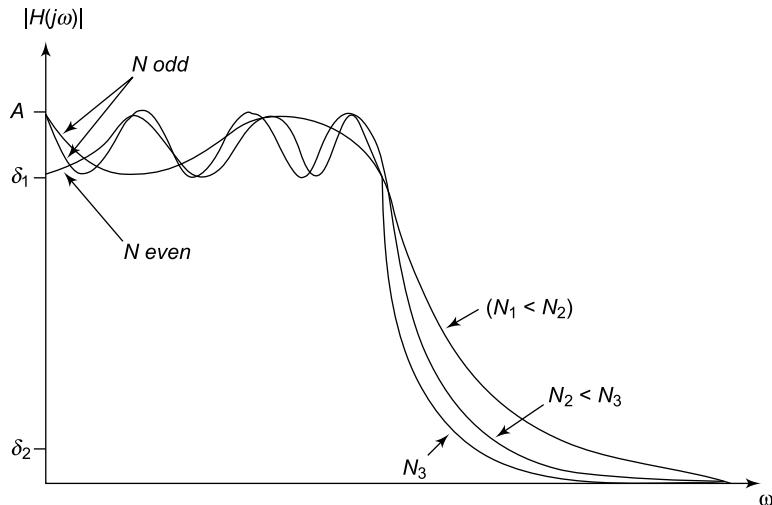
The Chebyshev low-pass filter has a magnitude response given by

$$|H(j\omega)| = \frac{A}{\sqrt{1 + \varepsilon^2 C_N^2(\omega/\omega_c)}} \quad (6.43)$$

where  $A$  is the filter gain,  $\varepsilon$  is a constant and  $\omega_c$  is the 3dB cut-off frequency. The Chebyshev polynomial of the first kind of  $N^{\text{th}}$  order,  $C_N(x)$  is given by

$$C_N(x) = \begin{cases} \cos(N \cos^{-1} x), & \text{for } |x| \leq 1 \\ \cosh(N \cosh^{-1} x), & \text{for } |x| \geq 1 \end{cases} \quad (6.44)$$

The magnitude response of the Chebyshev filter is shown in Fig. 6.26. The magnitude response has equiripple passband and maximally flat stopband. It can be seen that by increasing the filter order  $N$ , the Chebyshev response approximates the ideal response. The phase response of the Chebyshev filter is more non-linear than the Butterworth filter for a given filter length  $N$ .



**Fig. 6.26** Magnitude response of a low-pass Chebyshev filter

The design parameters of the Chebyshev filter are obtained by considering the low-pass filter with the desired specifications as given by

$$\delta_1 \leq |H(e^{j\omega})| \leq 1 \quad 0 \leq \omega \leq \omega_l \quad (6.45a)$$

$$|H(e^{j\omega})| \leq \delta_2 \quad \omega_2 \leq \omega \leq \pi \quad (6.45b)$$

The corresponding analog magnitude response is to be obtained in the design process. Using Eq. (6.43) in Eq. (6.45) and if  $A = 1$ , we get

$$\delta_1^2 \leq \frac{1}{1 + \varepsilon^2 C_N^2(\omega_l/\omega_c)} \leq 1$$

$$= \frac{1}{1 + \varepsilon^2 C_N^2(\omega_c/\omega_c)} \leq \delta_2^2$$

Assuming  $\omega_c = \omega_l$ , we will have  $C_N(\omega_c/\omega_c) = C_N(1) = 1$ . Therefore, the above equation can be written as

$$\delta_1^2 \leq \frac{1}{1 + \varepsilon^2} \quad (6.46)$$

Assuming equality in the above equation, the expression for  $\omega_c = \omega_l$  is

$$\varepsilon = \left[ \frac{1}{\delta_1^2} - 1 \right]^{0.5}$$

The order of the analog filter,  $N$  can be determined from the above equations. Assuming  $\omega_c = \omega_l$ , we have

$$C_N(\omega_2/\omega_l) \geq \frac{1}{\varepsilon} \left[ \frac{1}{\delta_2^2} - 1 \right]^{0.5}$$

Since  $\omega_2 > \omega_l$ ,

$$\cos h \left[ N \cos h^{-1}(\omega_2/\omega_l) \right] \geq \frac{1}{\varepsilon} \left[ \frac{1}{\delta_2^2} - 1 \right]^{0.5}$$

or

$$N \geq \frac{\cos h^{-1} \left\{ \frac{1}{\varepsilon} \left[ \frac{1}{\delta_2^2} - 1 \right]^{0.5} \right\}}{\cos h[(\omega_2/\omega_l)]} \quad (6.47)$$

Choose  $N$  to be the next nearest integer to the value given by the above equation.

**Chebyshev polynomials** The Chebyshev polynomials are given in Table 6.6.

**Table 6.6** Chebyshev polynomials

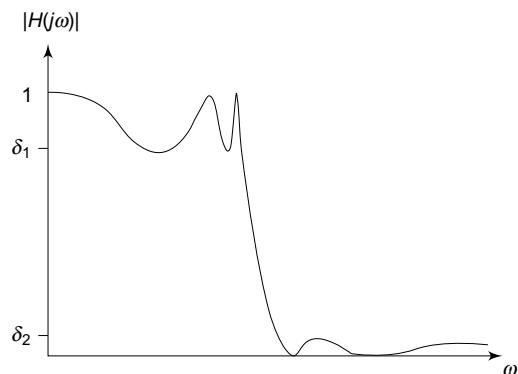
$N$	$C_N(\omega)$
0	1
1	$\omega$
2	$2\omega^2 - 1$
3	$4\omega^3 - 3\omega$
4	$8\omega^4 - 8\omega^2 + 1$
5	$16\omega^5 - 20\omega^3 + 5\omega$
6	$32\omega^6 - 48\omega^4 + 18\omega^2 - 1$
7	$64\omega^7 - 112\omega^5 + 56\omega^3 - 7\omega$
8	$128\omega^8 - 256\omega^6 + 160\omega^4 - 32\omega^2 + 1$
9	$256\omega^9 - 576\omega^7 + 432\omega^5 - 120\omega^3 + 9\omega$
10	$512\omega^{10} - 1280\omega^8 + 1120\omega^6 - 400\omega^4 + 50\omega^2 - 1$

### 6.10.3 Elliptic Filters

The elliptic filter is sometimes called the Cauer filter. This filter has equiripple passband and stopband. Among the filter types discussed so far, for a given filter order, passband and stopband deviations, elliptic filters have the minimum transition bandwidth. The magnitude response of an odd ordered elliptic filter is shown in Fig. 6.27. The magnitude squared response is given by

$$|H(j\omega)|^2 = \frac{1}{1 + \varepsilon^2 U_N(\omega/\omega_c)} \quad (6.48)$$

where  $U_N(\omega/\omega_c)$  is the Jacobian elliptic function of order  $N$  and  $\varepsilon$  is a constant related to the passband ripple.



**Fig. 6.27** Magnitude response of a low-pass elliptic filter

## 6.11 ALL-PASS FILTERS

An all-pass filter allows all the frequency components of the input signal to pass without attenuation, while providing the required phase shift at a given frequency of the input signal. The phase shift circuits, namely, phase lag and phase lead circuits discussed in Sec. 4.4 fall into the category of all-pass filters, wherein  $R_f = R_i$ . They pass all frequencies but delay the signal by a predictable time. The all-pass filters are also called *delay equalisers*, *phase correctors*, or *constant delay filters*.

All-pass filters provide a delay without varying the amplitude response. Some analog computational functions provide a delay, i.e. inverting amplifiers give a constant  $180^\circ$  phase shift, differentiators give a  $90^\circ$  phase lead and integrators give a  $90^\circ$  phase lag. All-pass filter provides an adjustable phase shift.

The phase of the signals may change when transmitted over telephone wires. Hence all-pass filters are required to correct these phase changes. Also the all-pass filters are used to prevent *aliasing*, to reject high-frequency interference such as that from the power line frequency and harmonics, and ripples from isolation amplifiers, and to limit bandwidth.

## 6.12 STATE-VARIABLE FILTER

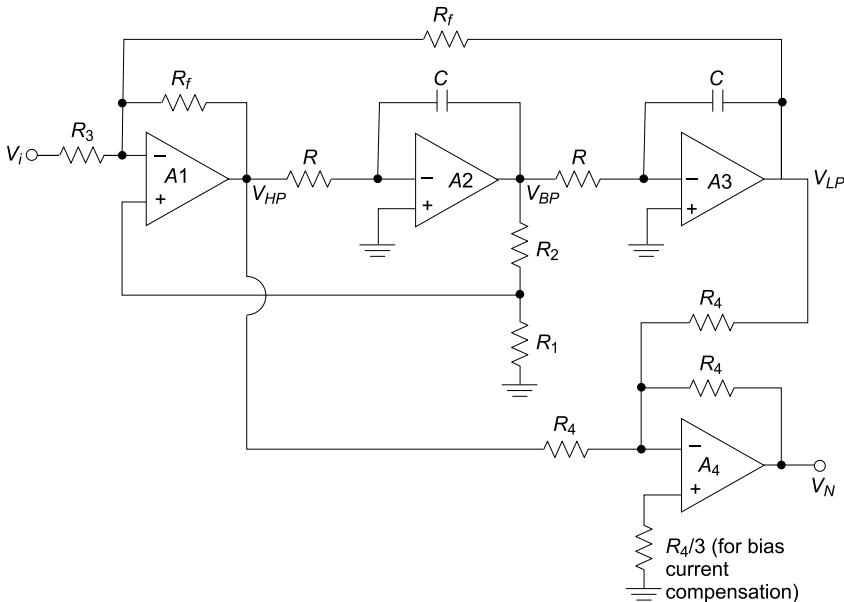
The state-variable filter is a versatile type of active filter, which can function as a second order low-pass, high-pass and bandpass filters. It is also called *RHN filter* after its inventor. As a bandpass circuit, it can have a very high *quality factor Q*, and a very normal *bandwidth B*. Further, it can be used as a band-reject filter with the addition of a summing circuit. Hence, the state-variable configuration uses an integrator consisting of two op-amps and an adder consisting of one op-amp for implementing any type of filter.

The state-variable filter has the following advantages.

- (i) It is easy to tune the filter over a broad frequency range electronically
- (ii) Independent adjustment of  $Q$  and tuning frequency are possible for various responses
- (iii) More complex filter configurations can be created with the use of multiple response output responses obtainable from the circuit.

The state-variable filter circuit is shown in Fig. 6.28. It uses the op-amps  $A_1$  and  $A_4$  acting as the summer circuits, and the op-amps  $A_2$  and  $A_3$  and their associated components acting as integrators. The outputs at various output nodes of the four op-amps are the high-pass response  $V_{HP}$ , bandpass response  $V_{BP}$ , low-pass response  $V_{LP}$  and notch response  $V_N$ . The negative feedback around the first three stages

is provided by the resistor  $R_f$  and the resistors  $R_1$  and  $R_2$  form a positive feedback path around the first two stages of the circuit. The resistor  $R$  and the capacitor  $C$  act as the timing elements. The resistors of value  $R_4$  and  $R_4/3$  constitute the final summer circuit for obtaining the notch response using the op-amp  $A_4$ . As shown in Fig. 6.28, the op-amp  $A_4$  combines the low-pass response  $V_{LP}$  with the high pass response  $V_{HP}$ , to produce the notch response  $V_N$ .



**Fig. 6.28** State-variable filter with high-pass, bandpass, low-pass and notch responses

The analysis of the circuit using Laplace transforms can be made as follows. The output  $V_{BP}$  of op-amp  $A_2$  working as an integrator can be represented by

$$V_{BP} = -\frac{1}{sRC} \times V_{HP} \quad (6.49)$$

where  $V_{HP}$  is the output of the adder stage formed by  $A_1$ . Considering  $R = 1 \text{ M}\Omega$  and  $C = 1 \mu\text{F}$ , the time constant becomes  $RC = 1$ . Therefore, the response at the output  $V_{BP}$  is given by

$$V_{BP} = -\frac{1}{s} V_{HP} \quad (6.50)$$

For the integrator circuit using op-amp  $A_3$ , similar treatment results in

$$V_{LP} = -\left(-\frac{1}{s} V_{HP}\right) = \frac{1}{s} V_{HP} \quad (6.51)$$

The op-amp  $A_1$  is a three input adder for the input signals given by (i)  $V_{HP}$  with a gain as defined by the resistors of value  $R_3$ , (ii) the feedback input due to  $V_{BP}$  through a potential divider, and (iii)  $V_{LP}$  with a gain factor defined by the resistors of value  $R_3$ .

That is,

$$V_{HP} = -\left(\frac{R_f}{R_3}\right)V_i - \left(\frac{R_f}{R_3}\right)V_{LP} + \left(1 + \frac{R_f}{R_f \parallel R_3}\right)\left(\frac{R_1}{R_1 + R_2}\right)V_{BP}$$

Assuming  $R_f = R_3$ , we get

$$V_{HP} = -V_i - V_{LP} + 3 \left( \frac{R_1}{R_1 + R_2} \right) V_{BP}$$

Substituting the parameter  $\alpha$  for  $3 \left( \frac{R_1}{R_1 + R_2} \right)$ , we get

$$V_{HP} = -V_i - V_{LP} + \alpha V_{BP} \quad (6.52)$$

Substituting Eqs. (6.50) and (6.51) in Eq. (6.52), we get

$$\begin{aligned} V_{HP} &= -V_i - \frac{V_{HP}}{s^2} - \frac{\alpha}{s} V_{HP} \\ -V_i &= V_{HP} \left( 1 + \frac{\alpha}{s} + \frac{1}{s^2} \right) \end{aligned}$$

Therefore, the high-pass transfer function  $H_{HP}$  is given by

$$H_{HP} = \frac{V_{HP}}{V_i} = \frac{-s^2}{s^2 + \alpha s + 1} \quad (6.53)$$

where  $\alpha$  is the damping factor and it can be set using the resistors  $R_1$  and  $R_2$  forming the potential divider network as shown in Fig. 6.28 for various filter responses such as Bessel, Butterworth or Chebyshev responses.

Equation (6.53) shows that it is the standard second-order high-pass response with a negative sign. Therefore, comparing this response with the standard response as given by

$$\frac{As^2}{s^2 + \alpha \omega_L s + \omega_L^2}$$

we get,  $A = -1$  and  $\omega_L = 1$  for the high-pass filter operation of the state-variable filter.

The low-pass transfer function is derived from Eq. (6.52) and Eq. (6.51) by eliminating the  $V_{HP}$  and  $V_{BP}$  responses.

$$s^2 V_{LP} \left( 1 + \frac{\alpha}{s} + \frac{1}{s^2} \right) = -V_i$$

Therefore, the transfer function for low-pass filtering is given by

$$H_{LP} = \frac{V_{LP}}{V_i} = \frac{-1}{s^2 + \alpha s + 1} \quad (6.54)$$

We have  $A = -1$  and  $\omega_H = 1$ .

Similarly, the bandpass response is derived from Eq. (6.52) by substituting for  $V_{HP}$  and  $V_{LP}$  in terms of  $V_{BP}$  as given by

$$H_{BP} = \frac{V_{BP}}{V_i} = \frac{s}{s^2 + \alpha s + 1} \quad (6.55)$$

The standard bandpass transfer function is given by

$$\frac{A \alpha \omega_o s}{s^2 + \alpha \omega_o s + \omega_o^2} \quad (6.56)$$

Comparing the response of bandpass filter as given by Eq. (6.55) with the standard response of Eq. (6.56), we get

$$A\alpha\omega_o = 1$$

Assuming  $RC = 1$ , we get

$$\omega_o = \frac{1}{RC} = 1$$

We can infer that the bandpass response can be obtained by integrating the high-pass response, and the low-pass response can be generated by integrating the bandpass response.

The notch filter output  $V_N$  is given by

$$V_N = -\left(\frac{R_4}{R_4}\right)V_{HP} - \left(\frac{R_4}{R_4}\right)V_{LP} = -V_{HP} - V_{LP}$$

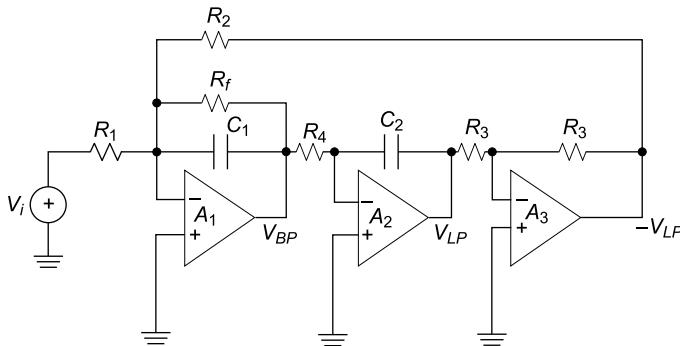
since the gain for the two inputs are made unity. The transfer function  $H_N$  of the notch filter is given by

$$H_N = \frac{V_N}{V_i} = \frac{s^2 + 1}{s^2 + \alpha s + 1} \quad (6.57)$$

The state-variable filters are also known as *universal filters* since it is possible to obtain LP, BP, HP and notch filter outputs. The Quad op-amps such as LF347, TL074 and TLC274, and op-amps with FET input devices are ideally suited for filter circuits. Universal filters are available as a single IC chip from Datel with series FLT-U2 and AF100 from National Semiconductor.

## 6.13 BIQUAD FILTER (TOW–THOMAS)

The biquad filter is called Tow–Thomas filter, after its inventors. It is also referred to as a *resonator filter*. Figure 6.29 shows the biquad filter circuit. It consists of two integrators formed by  $A_1$  and  $A_2$ . Here, the integrator formed using  $A_1$  is a lossy type. The op-amp  $A_3$  is a unity gain inverting amplifier and its only use is to provide the polarity reversal for the output.



**Fig. 6.29** Biquad filter

The circuit can be analysed by considering the op-amp  $A_1$  and summing the currents at its inverting input node,

i.e.

$$\frac{V_i}{R_1} - \frac{V_{LP}}{R_2} + \frac{V_{BP}}{R_f} + \frac{V_{BP}}{1/sC_1} = 0$$

From the circuit,

$$V_{LP} = -\frac{1}{R_4 C_2 s} V_{BP}$$

Substituting this to eliminate  $V_{LP}$  in the previous equation, we have

$$\frac{V_{BP}}{V_i} = T_{OBP} T_{BP}$$

and

$$\frac{V_{LP}}{V_i} = -\frac{1}{R_4 C_2 s} \frac{V_{BP}}{V_i} = T_{OLP} T_{LP}$$

where

$$T_{OBP} = -\frac{R_f}{R_l}$$

$$T_{OLP} = \frac{R_2}{R_l}$$

$$\omega_o = \frac{1}{\sqrt{R_4 R_2 C_1 C_2}}$$

and

$$Q = \frac{R_f \sqrt{C_1}}{R_4 R_2 C_2}$$

Thus, it is observed that the biquad yields only two significant responses.

The advantages of biquad filter are as given below:

1. It permits adjustment of all the three parameters, namely,  $\omega_o$ ,  $Q$  and gain. This is unlike the state-variable filters.
2. The above adjustments can be done in three individual steps, without the need of many iterations.
3. The common-mode limitations are avoided, since all the op-amps are operated in inverting mode. It enables the realisation of higher-gain bandwidth product (GBP).

However, unlike the state-variable filter circuit, the biquad filter offers only two of the three filter responses.

The circuit normally uses  $R_2 = R_4$  and  $C_2 = C_1 = C$

$$\text{Then, } J_{OBP} = -\frac{R_f}{R_l}, \quad T_{OLP} = \frac{R}{R_l}, \quad \omega_o = \frac{1}{RC} \quad \text{and} \quad Q = \frac{R_f}{R}$$

The tuning process normally proceeds as follows:

- (a) Adjust  $R_2$  or  $R_4$  to tune  $\omega_o$ .
- (b) Adjust  $R_f$  to tune  $Q$ .
- (c) Adjust  $R_l$  for realising desired  $T_{OBP}$  or  $T_{OLP}$ .

The notch response can be configured as was done for the state variable filter using a fourth op-amp.

## 6.14 IMPEDANCE CONVERTER

Impedance transformation or impedance conversion is used to change the impedance amplitude and sign. The transconductance circuits and current amplifier circuits discussed in Chap. 4 are impedance transformers. The impedance transformers to be discussed in this section are those operating on capacitor

as the specific impedance element. The impedance converter changes a positive impedance into a negative impedance and vice-versa. The capacitive reactance is converted into an inductive reactance and vice-versa. These conversions are aimed at neutralising the resistance or reactance, and thereby to broaden the signal bandwidth and for noise reduction in some applications.

### 6.14.1 Negative Impedance Conversion

Negative impedance conversion is the process of obtaining a normally grounded impedance, which is proportional to a given negative impedance, that may be a grounded or floating one. Figure 6.30 shows the circuit of a negative impedance converter (NIC) using an op-amp.

Considering an ideal op-amp, the node voltage at the inverting input node  $a$  is equal to that at the non-inverting input node  $b$ . Using the gain equation of a non-inverting amplifier, the output voltage  $v_o$  is then given by

$$v_o = v_i \left( 1 + \frac{Z_1}{Z} \right) \quad (6.58)$$

The voltage at the non-inverting input is given by

$$v_i - v_o = i_i Z_2 \quad (6.59)$$

Using Eqs. (6.58) and (6.59), and with impedance defined as

$$Z_i = \frac{v_i}{i_i},$$

we get

$$Z_i = -Z \frac{Z_2}{Z_1} \quad (6.60)$$

In Eq. (6.60) the impedance to be converted can be any one of  $Z$ ,  $Z_1$  or  $Z_2$ . The condition to be satisfied is that

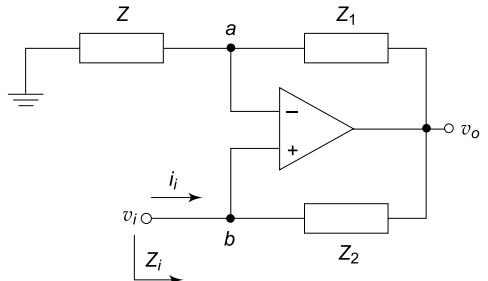
$$\frac{Z}{Z_1} > \frac{Z_s}{Z_2}$$

where the impedance  $Z_s$  denotes the source impedance of the circuit. The next condition is that the impedance conversion is possible only for the frequencies for which, the op-amp open-loop gain is considered infinite.

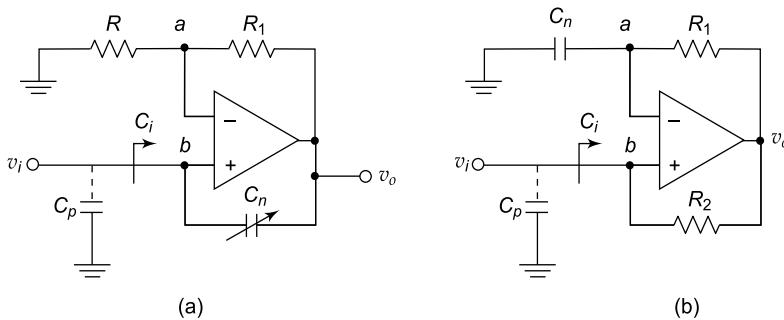
**Neutralising the amplifier input capacitance** Figure 6.31(a) shows a circuit arrangement for neutralising the amplifier input capacitance. The high-resistance signals such as those obtained from microelectrodes recording cell biopotentials and very small input parasitic capacitances can result in a low frequency response inadvertently. This can generate a corner frequency, which may be so low as to hinder the recording of fast changes in voltage. Assuming the op-amp and layout stray capacitances at

the non-inverting terminal as  $C_p$ , then  $C_i$  would preferably be  $-C_p$ . Using Eq. (6.60),  $C_i = -C_n \times \frac{R_1}{R}$ , and by tuning  $C_n$ , we can achieve input capacitance of very small value. The non-inverting input is applied from a signal source  $v_i$  and the output voltage  $v_o$  is given by

$$v_o = v_i \left( 1 + \frac{R_1}{R} \right).$$



**Fig. 6.30** Negative Impedance Converter (NIC) using op-amp



**Fig. 6.31** Negative capacitance neutralising circuits for (a) Input capacitance, and (b) Constant capacitance

### Neutralising the amplifier constant capacitance

Figure 6.31(b) shows a neutralising circuit for a constant capacitance  $C_o$ . Using Eq. (6.63), the capacitance  $C_i$  is given by  $C_i = -C \frac{R_1}{R_2}$ . The capacitance  $C$  is selected so that  $C_i + C_p = C_o$ . Choosing  $R_2 > R_1$  ensures frequency stability and values from  $10 \text{ k}\Omega$  to  $20 \text{ k}\Omega$  are preferred for preventing loading of op-amp.

**Simulation of negative resistance** The negative impedance converters of Fig. 6.31 can be used for simulating negative resistances, when they are connected to a low impedance source  $Z_s$  (to ensure stability). Figure 6.32 shows a circuit arrangement for simulating negative resistances for high impedance sources using a voltage feedback amplifier (VFA).

The current  $i_i$  at the inverting node is given by

$$i_i = \frac{v_i - v_o}{R_1} \quad (6.61)$$

Using the potential divider consisting of  $R_2$  and  $R_3$ , the voltage  $v_o$  is then given by

$$v_o = v_i \left( 1 + \frac{R_2}{R_3} \right) \quad (6.62)$$

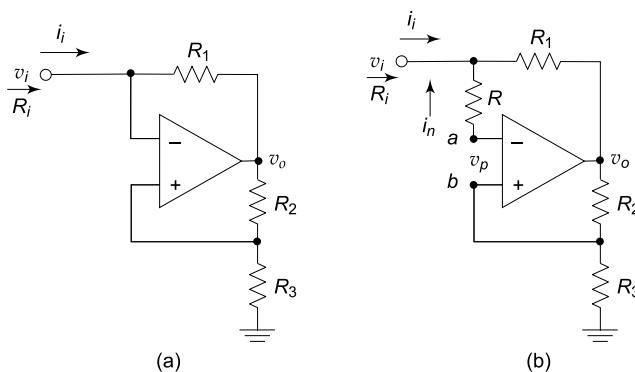
Substituting Eq. (6.62) into Eq. (6.61) and defining  $R_i = \frac{v_i}{i_i}$ , we get

$$R_i = -\frac{R_1 R_3}{R_2} \quad (6.63)$$

Frequency stability necessitates the ratio  $\frac{Z_s}{R_1} > \frac{R_3}{R_2}$ . When  $Z_s$  is very small at low frequencies, a capacitor connected in series with  $R_2$  enhances the frequency stability. Making one of the resistors adjustable makes the negative resistance an adjustable one too.

A resistor  $R$  in series with the input can be added for achieving negative and positive values of adjustable resistance, thus getting a total effective capacitance of  $R_e = R + R_i$ .

Figure 6.32(b) shows the same technique as that followed for Fig. 6.32(a) using a current feedback amplifier (CFA). This can simulate resistance at high frequencies.



**Fig. 6.32** Negative resistance simulation using (a) Voltage feedback amplifier (VFA), and (b) Current feedback amplifier (CFA)

## 6.15 IMPEDANCE GYRATION

**Principle of gyrators** A gyrator can be considered as a two port device, which can be used to simulate an inductance. Figure 6.33 shows the symbol of a gyrator.

The terminal voltages of the gyrator can be expressed as

$$V_1 = -KI_2$$

and

$$V_2 = KI_1$$

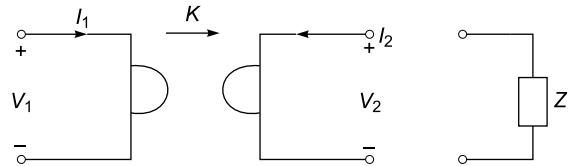
When a load  $I_L$  is connected across the output terminals, the input impedance becomes

$$Z_i = \frac{V_1}{I_1} = \frac{V_1}{V_2/K} = \frac{V_1}{-Z_L I_2/K} = \frac{V_1}{Z_L V_1/K^2} = \frac{K^2}{Z_L}$$

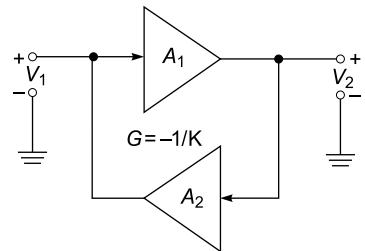
This implies that the ideal gyrator is a *positive impedance inverter*.

Hence, if a capacitive load of impedance value,  $\frac{1}{\omega C}$  is connected as a load, the input impedance becomes  $Z_i = j\omega K^2 C$ . This is actually an inductive impedance equal to  $K^2 C$ . The op-amp can be used to realise such gyrators. Figure 6.34 shows the simple way of Gyrator realisation.

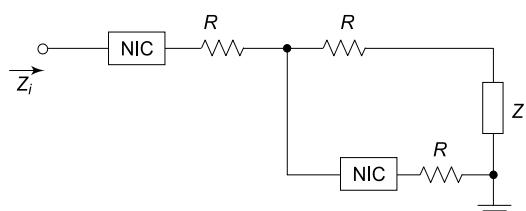
Simulation of inductances using capacitances, and conversely, simulation of capacitances using inductances can be achieved using the negative impedance converters (NIC). Figure 6.35 shows the circuit arrangement for impedance gyration using two NICs. Each NIC turns the impedance between its right side terminal and ground. The impedance  $Z_i$  as seen from the input will be given by



**Fig. 6.33** Gyrator symbol



**Fig. 6.34** Gyrator realisation



**Fig. 6.35** Impedance gyration using negative impedance converters

$$Z_i = - \left[ R + \frac{-R(R+Z)}{-R+(R+Z)} \right] = \frac{R^2}{Z} \quad (6.64)$$

In Eq. (6.64), when the impedance  $Z$  is a capacitor  $C$ , then the impedance  $Z_i = j\omega R^2$ . This simulates an inductor of value  $L = CR^2$ .

When the impedance  $Z$  is an inductor  $L$ , then  $Z_i$  is given by

$$Z_i = \frac{R^2}{j\omega L} \quad (6.65)$$

Therefore, this simulates a capacitor of value  $C = \frac{L}{R^2}$ .

These gyrator circuits find good use in active filter synthesis for the realisation of inductorless filters. The synthesis procedure starts with the design of the usual  $RLC$  prototype filter satisfying the desired specifications. Then the inductors of the circuit are conceived with these impedance converter-simulated inductors (Gyrator). The inductive impedance increases in value with frequency and this is a preferred characteristic for voltage amplifiers.

Figure 6.36(a) and (b) show the circuit arrangement for simulating an inductive impedance using a voltage buffer. Figure 6.36(a) shows the impedance  $Z_3$  maintaining both the terminals of impedance  $Z_1$  at the same potential. This reduces the current flow through  $Z_1$ , thereby providing a high impedance. The input impedance of the circuit is that offered by the path from input terminal to ground, which can be found by using delta-star impedance transformation.

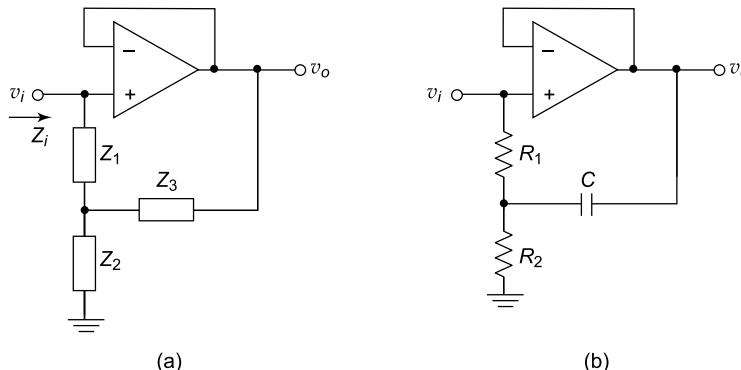
$$Z_i = Z_1 + Z_2 + \frac{Z_1 Z_2}{Z_3}$$

For Fig. 6.36(b), the impedance offered by the input terminal is given by

$$Z_i = R_1 + R_2 + j\omega R_1 R_2 C$$

The input impedance  $Z_i$  is equivalent to an inductor of value  $L_e = R_1 R_2 C$  connected in series with the resistances  $R_1$  and  $R_2$ . When the op-amp operates with unity gain in its passband of frequencies,  $v_o = v_i$ .

The maximum input impedance offered by the circuit is limited by the stray and parasitic capacitances from the inverting terminal to ground, which is normally of the order of 3 pF to 12 pF. This is dependent on the process conditions and op-amp model. The stray capacitances can yield a resonance also, which may increase the input impedance faster than what is expected, followed by a sharp reduction in impedance.



**Fig. 6.36** (a) and (b) Voltage buffer with inductive input impedance

## 6.16 GENERALISED IMPEDANCE CONVERTER

The Generalized Impedance Converter (GIC) shown in Fig. 6.37 is an active  $RC$  circuit. It is designed to simulate inductors and frequency dependent elements. They are available as monolithic ICs.

To identify the equivalent impedance  $Z$  observed looking into node  $A$ , we connect a test voltage  $V$  as shown and calculate the resultant current  $I$ . Then, letting  $Z = V/I$  gives us the equivalent impedance. From the circuit, we have

$$I = \frac{V - V_1}{Z_1}$$

Summation of currents at the node between  $Z_2$  and  $Z_3$  and that between  $Z_4$  and  $Z_5$  respectively, we get

$$\frac{V_1 - V}{Z_2} + \frac{V_2 - V}{Z_3} = 0 \quad \text{and} \quad \frac{V_2 - V}{Z_4} + \frac{0 - V}{Z_5} = 0$$

Solving for elimination of  $V_1$  and  $V_2$ , we get

$$Z = \frac{V}{I} = \frac{Z_1 Z_3 I_5}{Z_2 Z_4}.$$

Based on the components we use in place of  $Z_1$  through  $Z_5$ , we can identify the circuit for various impedance values. The widely followed combinations are as follows:

**Inductance simulator** All  $Z_i$ s are resistors except  $Z_2$  or  $Z_4$ , which is a capacitance element.

$$\text{Putting } Z_2 = \frac{1}{j\omega C_2} \text{ gives } Z = \frac{R_1 R_3 R_5}{\left(\frac{1}{j\omega C_2}\right) R_4} = j\omega \left( \frac{R_1 R_3 R_5 C_2}{R_4} \right) = j\omega L$$

Thus, this circuit simulates a grounded inductance  $L$  of value

$$L = \frac{R_1 R_3 R_5 C_2}{R_4}$$

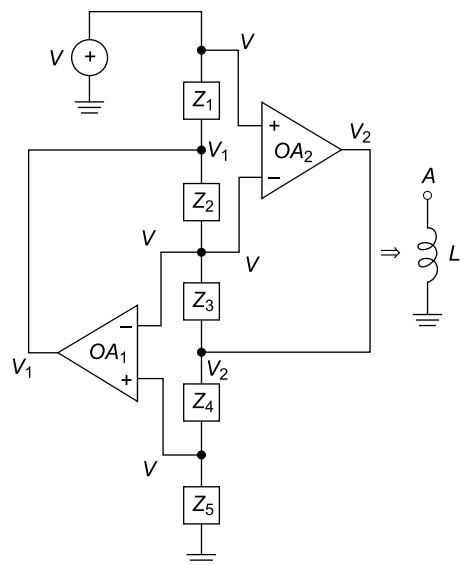
Figure 6.38 shows the grounded inductor simulation using GIC.

**Grounded Frequency Dependent Negative Resistance (Grounded FDNR)** All  $Z_i$ s are resistances, except  $Z_1$  and  $Z_5$ , which are capacitances.

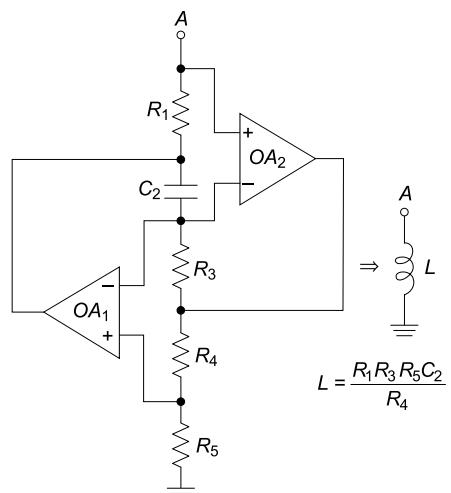
$$\text{Let } Z_1 = \frac{1}{j\omega C_1} \text{ and } Z_5 = \frac{1}{j\omega C_5}$$

$$\text{Then } Z = \frac{\left(\frac{1}{j\omega C_1}\right) R_3 \left(\frac{1}{j\omega C_5}\right)}{R_2 R_4} = -\frac{1}{\omega^2 D}$$

$$\text{where } D = \frac{R_2 R_4 C_1 C_5}{R_3}$$



**Fig. 6.37** Generalised impedance converter (GIC)



**Fig. 6.38** Grounded inductor simulation using GIC

That is, the circuit simulates a grounded frequency dependent resistance. The capacitance produces a voltage that is proportional to the integral of the current. The FDNR, or the so-called  $D$ -element can be viewed as an element integrating the current twice. The  $D$ -element value can be changed by adjusting one of the resistances.

Gyrators and GICs are widely used in realisation of filters without inductors.

## 6.17 KRC (SALLEN–KEY) FILTER

A single  $R-C$  stage provides a first-order low-pass response. A second order or 2-pole stage can be made by cascading two first-order stages. Higher order filters are realised by cascading as many second-order stages as needed. Each second-order stage has a resonance frequency given by

$$H \rightarrow \frac{1}{(j\omega/\omega_1)} \times \frac{1}{(j\omega/\omega_2)} = -\frac{1}{(\omega/\omega_o)^2}$$

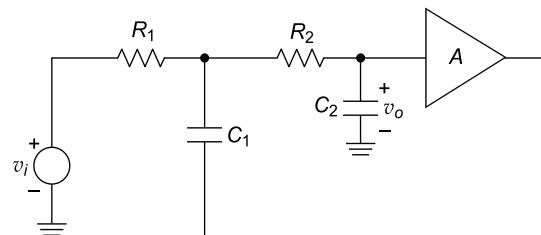
where  $\omega_o = \sqrt{\omega_1\omega_2}$ , with a slope of  $-40\text{dB/dec}$ .

However, the peaking profile around  $\omega/\omega_o = 1$  is not controllable and in practice,  $Q < 0.5$ . Hence, a controlled amount of *positive feedback* can be provided. Figure 6.39 shows the active realisation of a second-order low-pass filter.

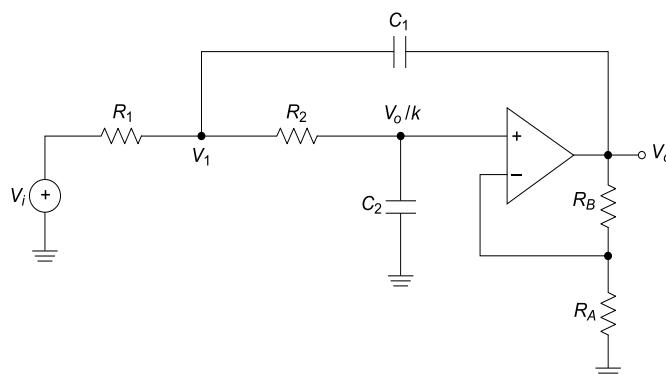
The output of  $R_2 - C_2$  stage is amplified by the factor  $A$  and gets fed back through  $C_1$ . This feedback is made selectively effective in the vicinity of  $\omega = \omega_o$ . For  $\omega/\omega_o \ll 1$ , the impedance offered by  $C_1$  is very large. On the other hand, for  $\omega/\omega_o \gg 1$ , the shunting provided by  $C_1$  makes  $v_o$  very small. However, around  $\omega/\omega_o = 1$ , feedback occurs and desired amount of peaking can be achieved by properly controlling the gain  $A$ .

These filters are called Sallen–Key filters, so named after their inventors, and they are also commonly identified as VCVS (Voltage Controlled Voltage Source) filters. They can implement Butterworth, Chebyshev and Bessel approximations.

Figure 6.40 shows the Sallen–Key second-order low-pass filter. The op-amp  $A$  connected as a non-inverting amplifier has gain of  $A = 1 + \frac{R_B}{R_A}$



**Fig. 6.39** KRC (Sallen–Key) second order low-pass Filter



**Fig. 6.40** Low-pass KRC filter

From the circuit,  $V_o = A \frac{V_1}{R_2 C_2 s + 1}$ .

At node  $V_1$ , using KCL, we can write

$$\frac{V_i - V_1}{R_1} + \frac{\frac{V_o}{k} - V_1}{R_2} + \frac{V_o - V_1}{1/C_1 s} = 0$$

Upon solving the above equation, we get

$$H(s) = \frac{V_o}{V_1} = \frac{A}{R_1 C_1 R_2 C_2 s^2 + [(1-A)R_1 C_1 + R_1 C_2 + R_2 C_2]s + 1}$$

By inspection,  $T_{OLP} = A$ .

Letting  $s = j\omega$  and simplifying, we get

$$\omega_o = \frac{1}{\sqrt{R_1 C_1 R_2 C_2}}$$

Equating  $j\omega[(1-A)R_1 C_1 + R_1 C_2 + R_2 C_2] = (j\omega/\omega_o)/Q$ , we have

$$Q = \frac{1}{(1-A)\sqrt{R_1 C_1 / R_2 C_2} + \sqrt{R_1 C_2 / R_2 C_1} + \sqrt{R_2 C_2 / R_1 C_1}}$$

Using the five parameters of the three equations, the most common designs used are the *equal component* and *unity gain* designs.

**Equal component KRC circuit** Referring to Fig. 6.41, assume that,

$$R_1 = R_2 = R \quad \text{and} \quad C_1 = C_2 = C,$$

$$T_{OLP} = A \quad \omega_o = \frac{1}{RC} \quad \text{and} \quad Q = \frac{1}{3-A}.$$

Therefore,  $RC = \frac{1}{\omega_o}$ ,  $k = 3 - \frac{1}{Q}$  and  $R_B = (A - 1)R_A$

**Unity gain KRC circuit** Letting  $A = 1$ ,  $R_2 = R$ ,  $C_2 = C$ ,  $R_1 = mR$  and  $C_1 = nC$ , we get

$$T_{OLP} = 1, \quad \omega_o = \frac{1}{\sqrt{mnRC}} \quad \text{and} \quad Q = \frac{\sqrt{mn}}{m+1}$$

The advantage of a unity gain KRC circuit is offset by quadratic increase of capacitor by  $n$ . Furthermore,  $\omega_o$  and  $Q$  adjustments mutually interfere.

However, the equal component design becomes too sensitive to  $R_A$  and  $R_B$  tolerances at high  $Q$ s, when their ratio is closer to 2. A slight mismatch results in change in  $Q$  causing the filter to oscillate. Hence, KRC filters are used for  $Q$  values below 10.

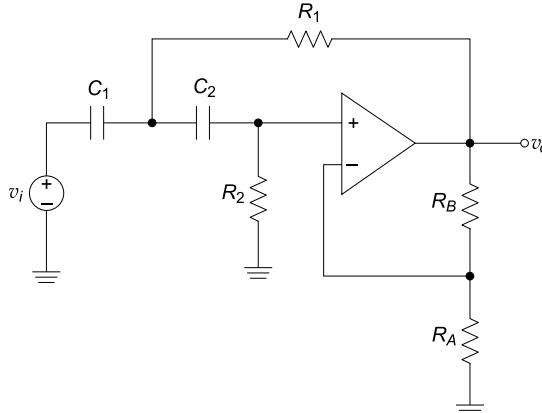
Additionally, for a certain combination of number of poles, the number of stages required and hence the active devices required is more for equal component design than that of unity gain designs.

**High-pass KRC (or) VCVS High-pass filters** In a Sallen–Key unity gain high-pass filter, the resistors and capacitors are interchanged. The value of  $Q$  depends on ratio of resistances rather than on the capacitances.

$$\frac{v_o}{v_i} = T_{OHP} T_{HP}, \quad T_{OHP} = A, \quad \omega_o = \frac{1}{\sqrt{R_1 C_1 R_2 C_2}} \text{ and}$$

$$Q = \frac{1}{(1-A)\sqrt{R_2 C_2 / R_1 C_1} + \sqrt{R_1 C_2 / R_2 C_1} + \sqrt{R_1 C_1 / R_2 C_2}}$$

The design can involve either the unity-gain or equal-component design.



**Fig. 6.41** High-pass KRC Filter

**Multiple feedback filters** As the name implies, these multiple feedback filters employ more than one feedback path. They are also called a *Delyiannis–Friend Filter* or *infinite-gain filters*, since they use the full-open loop gain. It is observed that the KRC filters and the multiple feedback filters are the widely popular forms of second-order responses using op-amps.

**Band-pass filter** Figure 6.42 shows the multiple-feedback filter using two separate feedback paths. The op-amp operates as a differentiator for the voltage  $V_1$ .

Hence,  $V_o = -sR_2 C_2 V_1$

At node  $V_1$ , KCL offers

$$\frac{V_i - V_1}{R_1} + \frac{V_o - V_1}{1/sC_2} + \frac{0 - V_1}{1/sC_1} = 0$$

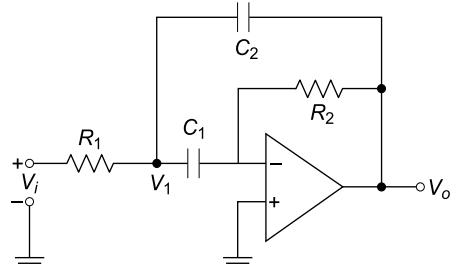
$$H(s) = \frac{V_o}{V_i} = -\frac{sR_2 C_2}{1 + s^2 R_1 R_2 C_1 C_2 + sR_1(C_1 + C_2)}$$

Substituting  $s = j\omega$ , we have

$$H(s) = -\frac{j\omega R_2 C_2}{1 - \omega^2 R_1 R_2 C_1 C_2 + j\omega R_1(C_1 + C_2)}$$

(i) Letting  $\omega^2 R_1 R_2 C_1 C_2 = (\omega/\omega_o)^2$ , we get

$$\omega_o = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$



**Fig. 6.42** Inverting multiple feedback (Delyiannis–Friend) Band-pass filter circuit

(ii) Letting  $j\omega R_1(C_1 + C_2) = (j\omega/\omega_o)/Q$ , we get

$$Q = \frac{\sqrt{R_2/R_1}}{\sqrt{C_1/C_2} + \sqrt{C_2/C_1}}$$

(iii) Letting  $-j\omega R_2 C_2 = H_{OBP} \times (j\omega/\omega_o)/Q$ , we get

$$H_{OBP} = -\frac{R_2/R_1}{1 + C_1/C_2}$$

Assuming  $C_1 = C_2 = C$ ,

$$\omega_o = \frac{1}{\sqrt{R_1 R_2} C}$$

$$Q = \frac{\sqrt{R_2/R_1}}{2}$$

$$H_{OBP} = -\frac{R_2}{2R_1} = -2Q^2$$

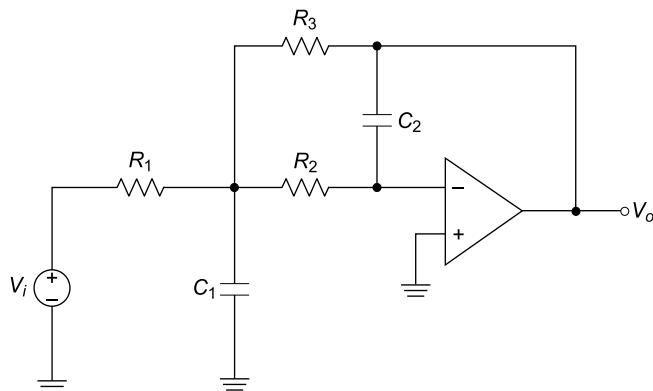
The centre frequency is given by

$$f_o = \frac{1}{2\pi C \sqrt{R_1 R_2}}$$

$$\text{Hence, } R_1 = \frac{1}{2\omega_o Q C} \text{ and } R_2 = \frac{2Q}{\omega_o C}$$

**Multiple feedback low-pass filter** Figure 6.43 shows the multiple feedback low-pass filter constructed using an  $R_1 - C_1$  stage and an integrator circuit using op-amp, and consisting of  $R_2$  and  $C_2$ . The additional resistor  $R_3$  provides the positive feedback for  $Q$  control. The response of the circuit is given by

$$\frac{V_o}{V_i} = H_{OLP} H_{LP}$$



**Fig. 6.43** Multiple feedback low-pass filter circuit

$$\text{where } H_{OLP} = -\frac{R_3}{R_1}, \omega_o = \frac{1}{\sqrt{R_2 R_3 C_1 C_2}} \text{ and } Q = \frac{\sqrt{C_1/C_2}}{\sqrt{R_2 R_3 / R_1^2} + \sqrt{R_3 / R_2} + \sqrt{R_2 / R_3}}$$

Adjustment of  $R_3$  results in variation of  $\omega_o$  and that of  $R_1$  results in fixing  $Q$ .

## 6.18 SWITCHED CAPACITOR FILTERS

The filters studied in earlier sections of this chapter are known as *continuous time filters* with the scaling factor or dc gain  $A$  and *selectivity*  $Q$  controlled by the components employed in the design. The active filters using ICs have the onerous advantage of not using inductors, and this helps in easy implementation of various high performance low-pass, high-pass, bandpass and band elimination filters.

In the early 1970s, continuous time circuits employing resistors, capacitors and op-amps were in practice. The reduced accuracy of the resistors and capacitors of CMOS technologies were not found sufficient enough for most of analog or linear signal processing applications. Hence, the circuits called *switched capacitor circuits* came into vogue which employs analog sample data techniques. The accuracy of the signal processing function depends on the accuracy of the capacitor ratios. The CMOS technology provided relatively good accuracy for the capacitors which resulted in mushrooming growth of switched capacitor circuits. The researchers working with switched capacitors propose architectures that could replace operational amplifiers. These new switched capacitor circuits which may employ comparators can handle voltage differently and they can work with supply voltages of 1V or less. This is an emerging technological area, the outcome of which is a prototype 8-bit 200 MHz analog to digital converter presented recently.

The main advantages of switched capacitor circuits are:

1. The compatibility with CMOS process technology
2. Good accuracy of time constants
3. High linearity with voltage
4. Good temperature characteristics

The important limitations of the circuits are:

1. The clock feed-through which may occur
2. The necessity of generating the non-overlapping clock signals and
3. The limitation of the bandwidth of operation on the clock in frequency.

The discrete resistors and capacitors required for the active filter circuits are very large and difficult to be fabricated on the monolithic IC chip. Resistors of value greater than 10 k $\Omega$  occupy a large chip area with their tolerances also difficult to be controlled. In addition, the maximum value of capacitance obtainable is limited to approximately 100 pF due to very large chip area necessitated and the tolerance expected. Standard resistor and capacitor components may not be available for a filter design aiming at a particular cut-off frequency. In view of these, it is cumbersome to maintain accurate time constants also.

Moreover, the mixed-signal integrated circuits of present-day designs need the digital functions also to coexist on the same chip. The most natural components of VLSI processors are MOS transistors and small MOS capacitors. These provide an attractive alternative for the conventional  $RC$  components of the active filters.

The switched capacitor filters are the all-IC circuits. They were developed through the simulation of resistors by operating MOS capacitors with MOS switches and producing time constants which depend on the capacitance ratios as explained below. The switched capacitor filter uses small capacitance values in combination with MOS switching transistors to simulate large resistance values.

### 6.18.1 Realisation of Resistance using Switched Capacitor

The switched capacitor arrangement using MOSFETs is illustrated in Fig. 6.44(a). The transistors  $M_1$  and  $M_2$  are  $N$ -channel enhancement transistors with the channel resistance, typically less than  $10^3 \Omega$  when gate voltage is high, and a high resistance greater than  $10^{12} \Omega$ , when the gate voltage is low. Hence, the MOSFET can be recognised as a switch for all practical purposes. When the gates of the transistors are driven with *non-overlapping and out-of-phase* clock signals as shown in Fig. 6.44(b), the transistors will conduct during alternate half cycles. This provides a single-pole double-throw (SPDT) switch function with *break-before-make* characteristics.

Figures 6.45(a) and (b) show the simulation of resistance using the switched capacitance arrangement. Assume  $V_1 > V_2$  and also consider that the switch  $S$  is initially in position  $a$ . The capacitor  $C$  is initially charged to voltage  $V_1$ . The switch  $S$  is then thrown to position  $b$  and the capacitor  $C$  discharges to the voltage  $V_2$ . The amount of charge that flows through the capacitor  $C$  is thus,

$$Q = C(V_1 - V_2)$$

If the switch  $S$  is thrown back and forth for every  $T_{ck}$  second, then the current  $i$  that flows through the capacitor  $C$  is,

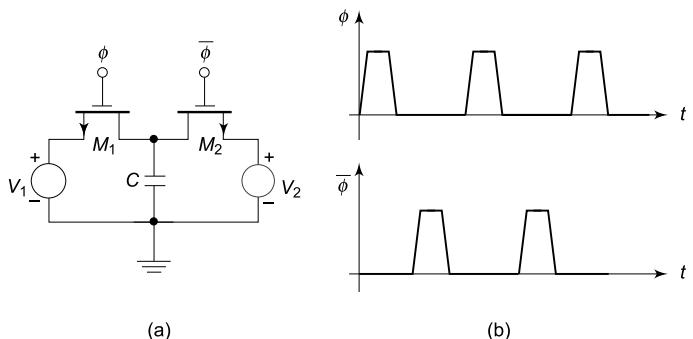
$$i = \frac{Q}{T_{ck}} = \frac{C(V_1 - V_2)}{T_{ck}} = f_{ck} C(V_1 - V_2)$$

where  $T_{ck}$  is the clock period and  $f_{ck} = \frac{1}{T_{ck}}$  is the clock frequency.

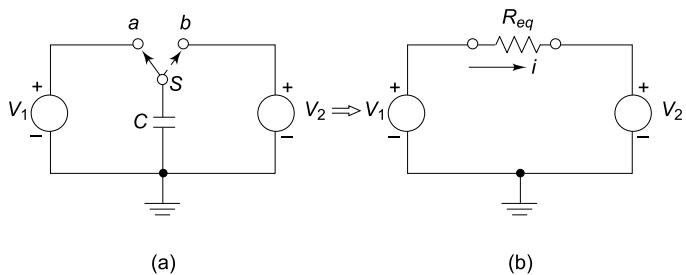
Assuming the clock frequency  $f_{ck}$  to be large compared to the highest signal frequency of  $V_1$  and  $V_2$ , the switch-capacitor combination can be modelled as an equivalent resistance given by

$$R_{eq} = \frac{V_1 - V_2}{i} = \frac{T_{ck}}{C} = \frac{1}{f_{ck} C}$$

The resistance model is shown in Fig. 6.45(b). This is called switched capacitor I (SC-I). Hence, the switched capacitor filters work on the principle that a capacitor  $C$ , when periodically switched between two circuit nodes at a high rate  $f_{ck}$  is equivalent to a resistance  $R_{eq} = \frac{1}{f_{ck} C}$ , connecting the two circuit nodes.



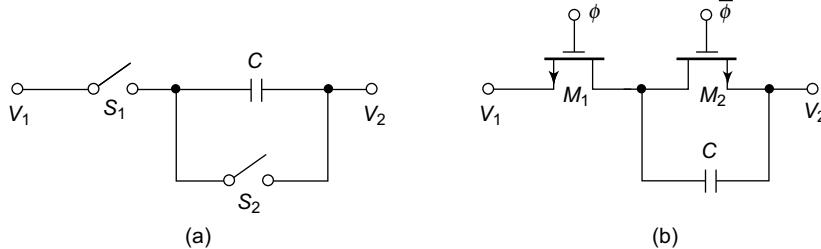
**Fig. 6.44** (a) *Switched capacitor using MOSFETs*  
(b) *Clock signals for the MOSFETs*



**Fig. 6.45** (a) and (b) *Simulation of resistance using a switched capacitor*

The second form of switched capacitor circuit is shown in Fig. 6.46(a). In this arrangement, during the ON period of switch  $S_1$ , the capacitor  $C$  is charged with respect to voltage  $V_1$ . When  $S_1$  is OFF and  $S_2$  is ON, the effective charge  $C(V_1 - V_2)$  is transferred. This delivery of charge occurs for every sampling interval  $T_{ck}$ . Thus, the average current  $i$  flowing through the capacitor  $C$  is given by,

$$i = \frac{C(V_1 - V_2)}{T_{ck}}$$



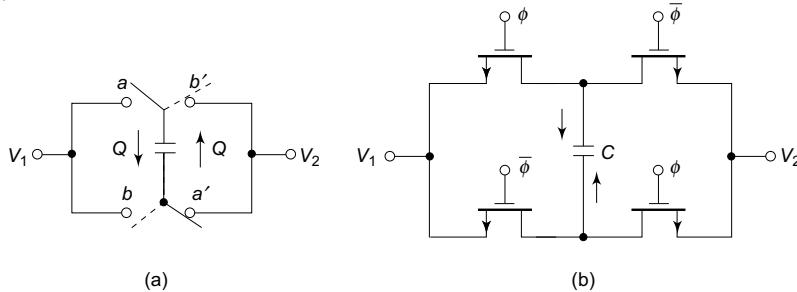
**Fig. 6.46** (a) SC-II Switched capacitor network (b) MOSFET realisation

Therefore, the equivalent value of simulated resistance is given by,

$$R = \frac{V_1 - V_2}{i} = \frac{T_{ck}}{C} = \frac{1}{f_{ck} C}$$

This structure is known as switched capacitor II (SC – II). The MOSFET realisation of the circuit with  $M_1$  acting as switch  $S_1$ , and  $M_2$  acting as switch  $S_2$  is shown in Fig. 6.46(b).

The third form of switched capacitor network SC-III formed by four-transistor arrangement is shown in Fig. 6.47(a).



**Fig. 6.47** (a) SC-III Switched capacitor network (b) MOSFET realisation

As shown in Fig. 6.47(a), when the switches are in positions  $a$  and  $a'$ , the charge acquired across the capacitor is  $C(V_1 - V_2)$ . When the switch is thrown to positions  $b$  and  $b'$ , the charge on the capacitor  $C$  becomes  $C(V_2 - V_1) = -C(V_1 - V_2)$ . It can be observed that the negative sign is due to the change in the direction of current through the capacitor. Assuming the switch is thrown back and forth every  $T_{ck}$  seconds, the total charge transfer occurring during the period  $T_{ck}$  is

$$C(V_1 - V_2) - [-C(V_1 - V_2)] = 2C(V_1 - V_2)$$

The current  $i$  flowing during  $T_{ck}$  is,

$$i = \frac{2C(V_1 - V_2)}{T_{ck}}$$

and the resistance offered is given by

$$R = \frac{V_1 - V_2}{i} = \frac{T_{ck}}{2C} = \frac{1}{2f_{ck}C}$$

The MOSFET realisation of the circuit is shown in Fig. 6.47(b).

The advantage of this SC-III capacitor is the doubling of sampling rate achieved.

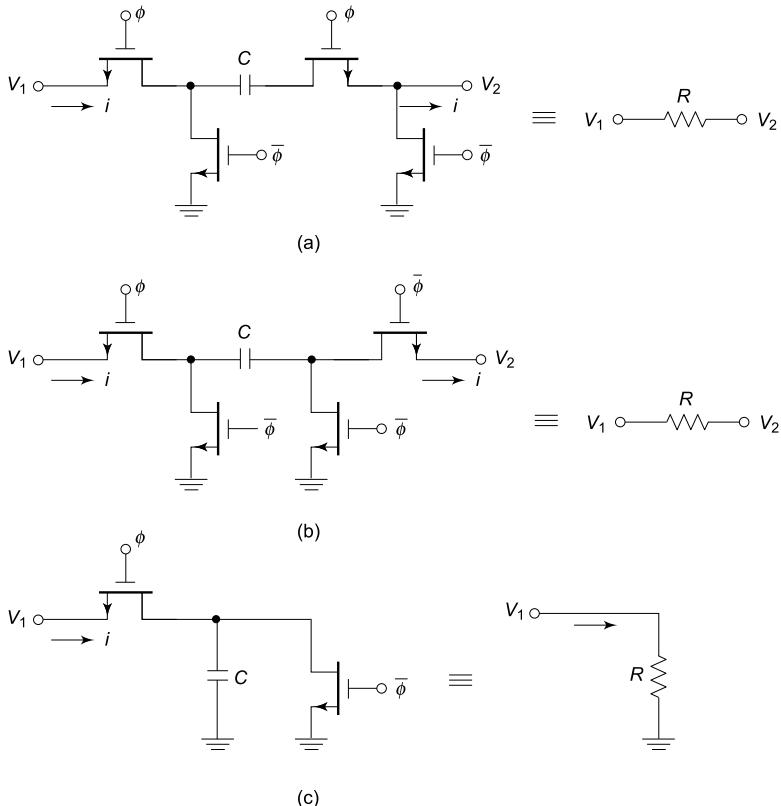
Various other forms of switching capacitors are illustrated in Fig. 6.48(a), (b) and (c). The MOSFET switches are supplied with non-overlapping and complementary clock pulses  $\phi$  and  $\bar{\phi}$ . It is necessary that the switching frequency  $f_{ck}$  is to be much larger than the highest signal frequencies of  $V_1(t)$  and  $V_2(t)$ .

The circuits shown in Fig. 6.48(a) and (b) employ a series switched-capacitor. The circuit of Fig. 6.48(c) uses a shunt switched capacitor. The equivalent resistance obtainable is

$$R = \frac{1}{f_{ck}C}$$

Various types of low-pass, high-pass, bandpass and band-reject active filters can be designed using the capacitor filter circuits.

These switched capacitor filters can also be identified as *sampled-data systems*, since the analog input signal is not transmitted through the circuit as a continuous signal rather it is passed as a series of pulses. The equivalent resistances derived are valid only for clock frequencies which are larger than the analog input signal frequency.



**Fig. 6.48** (a) Noninverting series switched capacitor circuit; (b) Inverting series switched capacitor circuit (c) Shunt switched capacitor circuit

### 6.18.2 Switched Capacitor Integrator

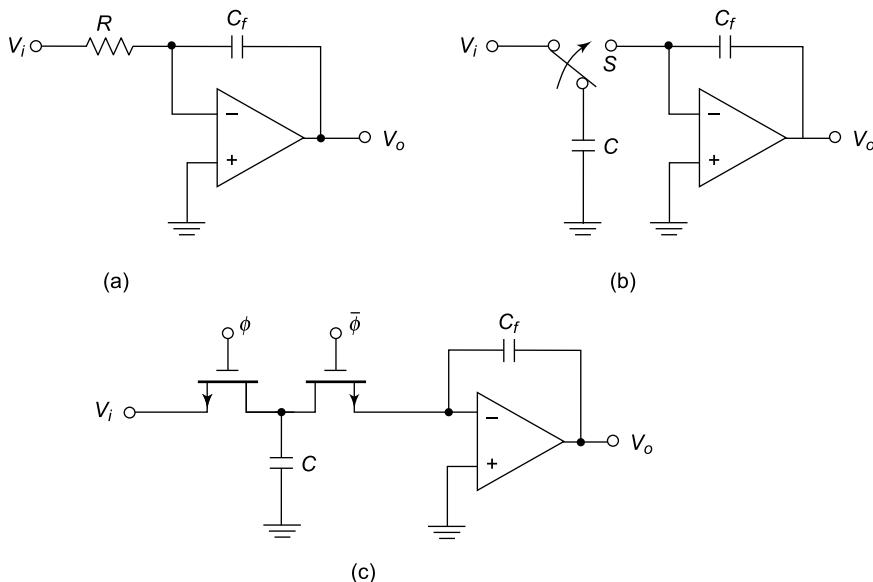
The switched capacitor integrator is an important analog signal processing circuit. All the filter designs can be reduced to non-inverting and inverting integrators. Op-amps can be configured for non-inverting and inverting continuous time integrators as discussed in this section.

An  $RC$ -integrator is shown in Fig. 6.49(a). The transfer function of the integrator is

$$H(S) = \frac{-(1/sC_f)}{R} = -\frac{1}{sRC_f} = -\frac{1}{j\left(\frac{f}{f_o}\right)}$$

where  $f_o = \frac{1}{2\pi RC_f}$  is the unity gain frequency.

The resistor  $R$  can be replaced by a switched-capacitor  $C$  as shown in Fig. 6.49(b).



**Fig. 6.49** (a)  $RC$  integrator (b) Switched capacitor implementation (c) CMOS implementation

The equivalent CMOS circuit is shown in Fig. 6.49(c),

where  $R = \frac{1}{f_{ck} C}$ ,  $f_{ck}$  is the clock frequency and  $f_{ck} \gg f$ .

The unity-gain frequency  $f_o$  is thus,

$$f_o = \frac{1}{2\pi \left( \frac{1}{f_{ck} C} \right) C_f} = \frac{C f_{ck}}{2\pi C_f}$$

The values of  $\left( \frac{C}{C_f} \right)$  and  $f_{ck}$  are chosen in such a way that any desired value of  $f_o$  is achieved.

To summarise the features of *SC* integrator,

- (i) there are no resistors involved as necessitated for IC fabrication.
- (ii) the unity gain frequency  $f_o$  is determined by capacitance ratios, which are easier to control and maintain in present-day IC technology.
- (iii) the unity gain frequency  $f_o$  is proportional to the clock frequency  $f_{ck}$ , thus proving that the *SC* filters are of programmable type.

The practical limitations of *SC* filters are as follows:

- (i) The values of  $f_{ck}$  are not unlimited, which is controlled by the quality of MOS switches, and the speed of op-amp employed. Practical values of  $f_{ck}$  are in MHz range.
- (ii) The lower limit of  $f_{ck}$  is dictated by the leakage currents in MOS switches and the input bias currents of op-amp. Hence, the minimum possible  $f_{ck}$  range is typically 100 Hz.
- (iii) The *SC* filters are discrete-time operated.

### Example 6.14

Determine the clock frequency required to simulate a resistance of value  $1 \text{ M}\Omega$ . Assume a capacitance of  $40 \text{ pF}$ .

#### Solution

$$\text{We know } R = \frac{1}{f_{ck} C}$$

$$\text{Therefore, } f_{ck} = \frac{1}{RC} = \frac{1}{1 \times 10^6 \times 40 \times 10^{-12}} = 25 \text{ kHz}$$

### 6.18.3 Design of First-Order Low-pass Filter

Figure 6.50(a) shows a first order low-pass filter. The transfer function of the circuit is given by

$$H(s) = \frac{V_o(s)}{V_i(s)} = -\frac{R_f}{R_1} \frac{1}{1 + sR_f C_f}$$

The cut-off frequency is given by

$$f_{3 \text{ dB}} = f_L = \frac{1}{2\pi R_f C_f}$$

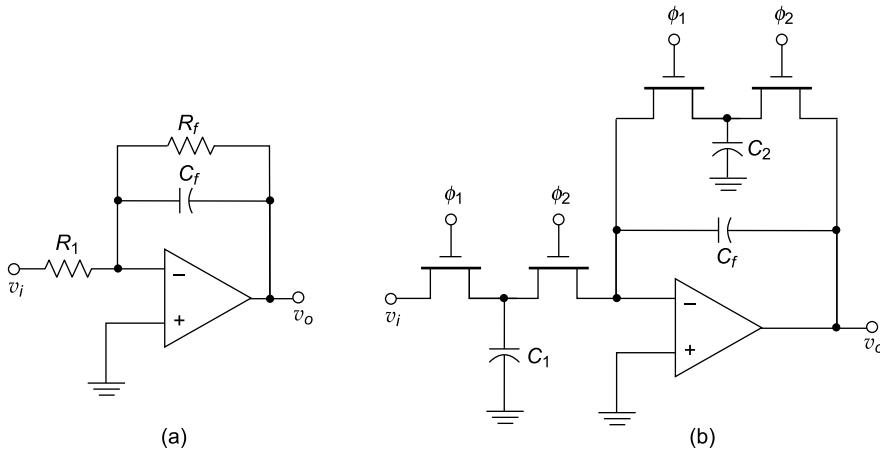
The equivalent switched capacitor circuit implementation is shown in Fig. 6.50(b), with the resistors  $R_1$  and  $R_f$  replaced by the switched capacitor networks formed by the MOSFETs  $M_1, M_2, M_3$  and  $M_4$ . The transfer function is the same as given above with the value of resistances  $R_f$  and  $R_1$  as given by

$$f_{3 \text{ dB}} = \frac{1}{(f_{ck} C_2)} \text{ and } R_1 = \frac{1}{(f_{ck} C_1)}$$

Then the transfer function can be written as

$$H(s) = \frac{V_o(s)}{V_i(s)} = -\frac{1/(f_{ck} C_2)}{1/(f_{ck} C_1)} \frac{1}{1 + \frac{sC_f}{f_{ck} C_2}}$$

$$= -\frac{C_1}{C_2} \frac{1}{\left[1 + j \frac{f}{f_L}\right]}$$



**Fig. 6.50** (a) First order low-pass filter (b) Equivalent switched capacitor circuit implementation

Here the low frequency gain of the circuit is determined by the ratio  $-C_1/C_2$  and the 3dB frequency is given by  $f_{ck}C_2/(2\pi C_f)$ .

#### 6.18.4 Monolithic Switched Capacitor Filter ICs

Monolithic universal switched capacitor filters use the configuration of dual integrator loop biquadratic circuit or biquad, thus achieving basic second order responses. Higher order filters can be constructed using the second order responses. Two of the popular switched capacitor filter ICs are LTC1060 from Linear Technology and MF10 from National Semiconductors. The LTC 1060 is pin compatible with MF10.

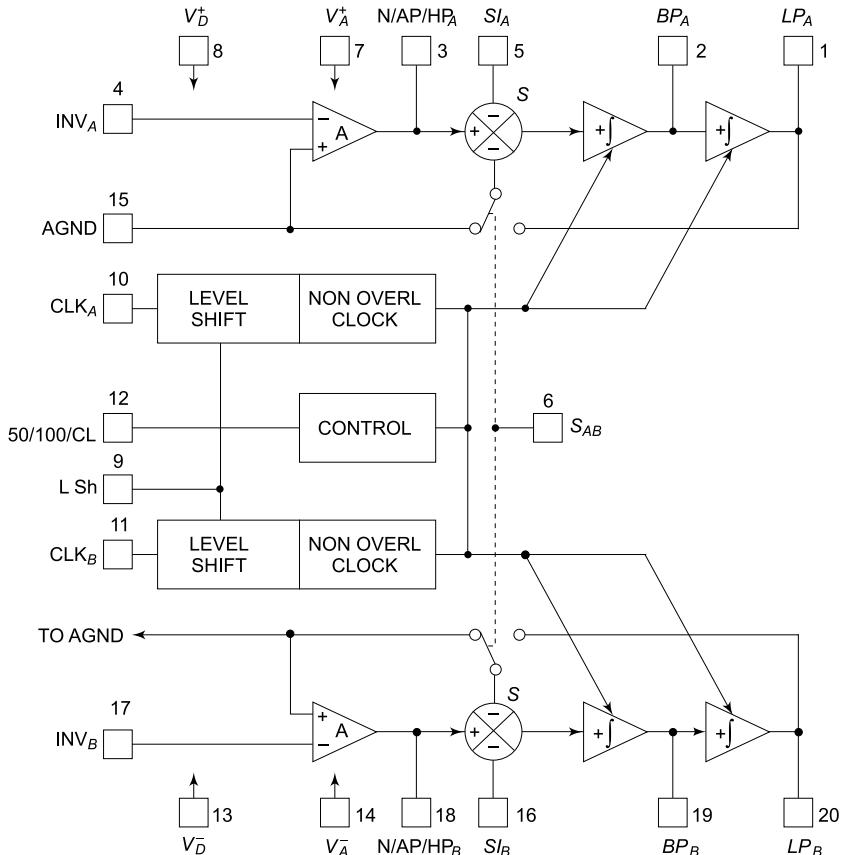
**MF10 universal switched capacitor filter** The block diagram of MF10 switched capacitor filter is shown in Fig. 6.51. It consists of two dual-integrator loop sections.

Each section can be individually configured for any of low-pass, bandpass, high-pass, notch, or all-pass filter responses by means of external resistances connected by the user. The use of external resistors increases the versatility of the IC to the circuit designer. Also the filter parameters are determined by the resistance ratios. Hence, component tracking is easily achieved.

The MF10 is made available as a 20-pin DIP package. Two complete second-order state-variable type active filters can be constructed using the IC. The external resistors determine the filter parameters. The outputs of each section are brought out individually. Hence, fourth order responses can easily be accomplished, by cascading the two sections. Classical filter responses, namely, Butterworth, Chebyshev, Bessel and Cauer can be derived by designing with IC MF10.

As shown in Fig. 6.51, there is a 3-input stage summing amplifier  $S$ . The positive input is connected to the output of the summing op-amp  $A$ . The input  $SI_A$  acts as the signal input to one of the two negative inputs of  $S$ . The second negative input is connected to either  $LP_A$  or  $LP_B$  through an internal switch shown. The direction of this input connection is common to both sections of the IC, and is controlled by the external input  $S_{AB}$  as shown. When  $S_{AB}$  is tied to  $V_D^+$  (at pin 8), the low-pass outputs  $LP_A$  and  $LP_B$

are connected to the respective negative inputs of  $SI_A$  and  $SI_B$ . Tying  $S_{AB}$  to  $V_D^-$  (at pin 13) connects the AGND to the negative inputs of the summing amplifier.



**Fig. 6.51** Block diagram of MF10 Universal switched capacitor filter

The integration outputs, namely,  $BP_A$  and  $LP_A$  are the bandpass and low-pass responses of the top section. The corresponding outputs for the bottom section are  $BP_B$  and  $LP_B$  of the IC.

The integrators provide the bandpass and low-pass responses, and the input summing amplifier provides the notch, all-pass or bandpass responses of the filters depending on the external resistors connected, and the internal switch position.

The SC integrators are of non-inverting type with the transfer function as given by

$$H(jf) = \frac{1}{j\left(\frac{f}{f_1}\right)}$$

where  $f_1$  is the unity gain frequency of integration, and  $f_1 = \frac{f_{ck}}{50}$  or  $\frac{f_{ck}}{100}$ .

The resonant frequency of the filter is controlled by a separate clock. TTL or CMOS clocks can be employed. Referring to pin 12, the voltage level applied at pin 12 (50/100/CL) determines the frequency

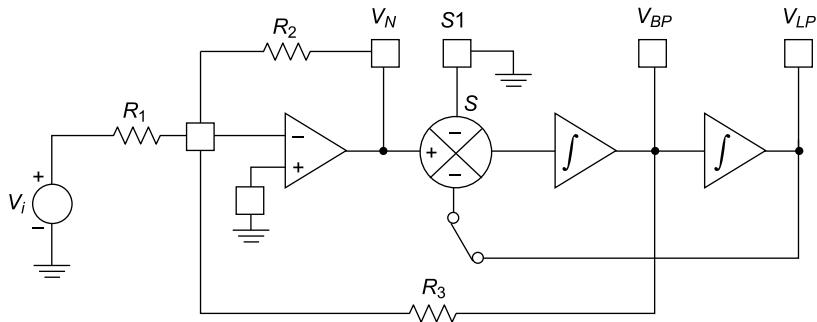
ratio. When tied to ground, ratio 100 is enabled and tying it to  $V_D^+$  enables the 50 ratio. When this pin is connected with  $V_D^-$ , the negative supply, the current limiter circuit shuts down the operation thus saving power. Grounding the pin 9 (*L Sh*) makes the IC operate with a single supply.

The MF10 can be operated with centre frequencies up to 20 kHz, and clocks up to 1 MHz.

### 6.18.5 Modes of Operation for Notch, Bandpass and Low-pass Responses

The circuit arrangement in Fig. 6.52 shows the IC MF10 connected for achieving notch, bandpass and low-pass responses. The summing amplifier is outside the two integrator loop. Hence, this mode is faster and provides a wider range of operating frequencies. As shown in Fig. 6.52, we have

$$V_N = -\frac{R_2}{R_1} V_i - \frac{R_2}{R_3} V_{BP} \quad (6.66)$$



**Fig. 6.52** Basic connection for the notch, bandpass and low-pass responses

where

$$V_{BP} = \frac{V_N - V_{LP}}{jf/f_1} \quad (6.67)$$

and

$$V_{LP} = \frac{V_{BP}}{jf/f_1} \quad (6.68)$$

where  $f_1 = \frac{f_{ck}}{100}$  or  $\frac{f_{ck}}{50}$  is the centre frequency, and

$V_N$ ,  $V_{BP}$  and  $V_{LP}$  are notch, bandpass and low-pass output responses.

Eliminating  $V_{LP}$  and  $V_{BP}$  using Eq. (6.66) through (6.68), we get

$$\frac{V_N}{V_i} = H_{ON} H_N,$$

$$\frac{V_{BP}}{V_i} = H_{OBP} H_{BP} \text{ and}$$

$$\frac{V_{LP}}{V_i} = H_{OLP} H_{LP}$$

where

$$f_z = f_o = \frac{f_{ck}}{100} \text{ or } \frac{f_{ck}}{50}, Q = \frac{R_3}{R_2}$$

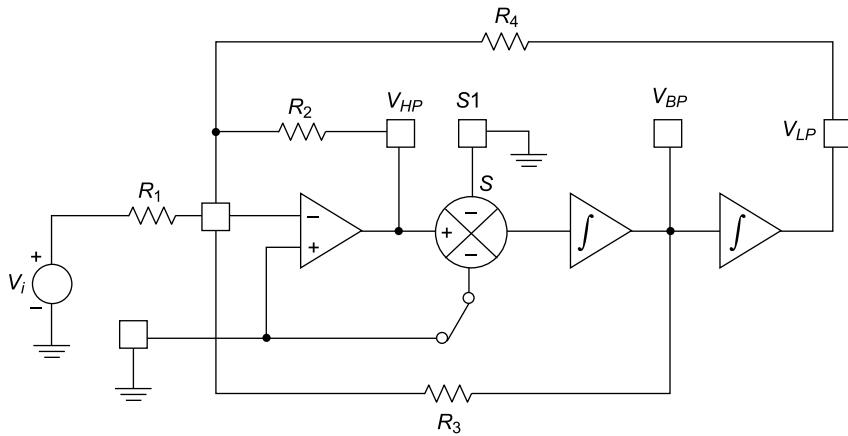
$$H_{ON} = H_{OLP} = -\frac{R_2}{R_1}$$

$$H_{OBP} = -\frac{R_3}{R_1}$$

where  $H_{ON}$ ,  $H_{OLP}$  and  $H_{OBP}$  are the dc gain for notch, low-pass and bandpass responses respectively.

### 6.18.6 State-variable Mode for High-Pass, Bandpass and Low-Pass Responses

Figure 6.53 shows the state-variable mode of operation. It is called state-variable mode, because of the fact that it provides the high-pass, bandpass and low-pass responses by direct and sequential integrations.



**Fig. 6.53** State-variable configuration using the IC MF10

When  $f \ll f_{ck}$ , the circuit offers

$$\frac{V_{BP}}{V_i} = H_{OBP} H_{BP},$$

$$\frac{V_{HP}}{V_i} = H_{OHP} H_{HP} \quad \text{and} \quad H_{OLP} = \frac{V_{LP}}{V_i} = H_{OLP} H_{LP}$$

A special feature of this mode of operation is that  $f_o$  can be tuned independently of  $f_1$ , where  $f_1$  is the integration unity gain frequency as given by

$$f_o = f_1 \sqrt{\frac{R_2}{R_4}}, \text{ i.e. } f_o = \frac{f_{ck}}{50} \sqrt{\frac{R_2}{R_4}} \quad \text{or} \quad f_o = \frac{f_{ck}}{100} \sqrt{\frac{R_2}{R_4}}$$

$$Q = \left( \frac{R_3}{R_2} \right) \sqrt{\frac{R_2}{R_4}}$$

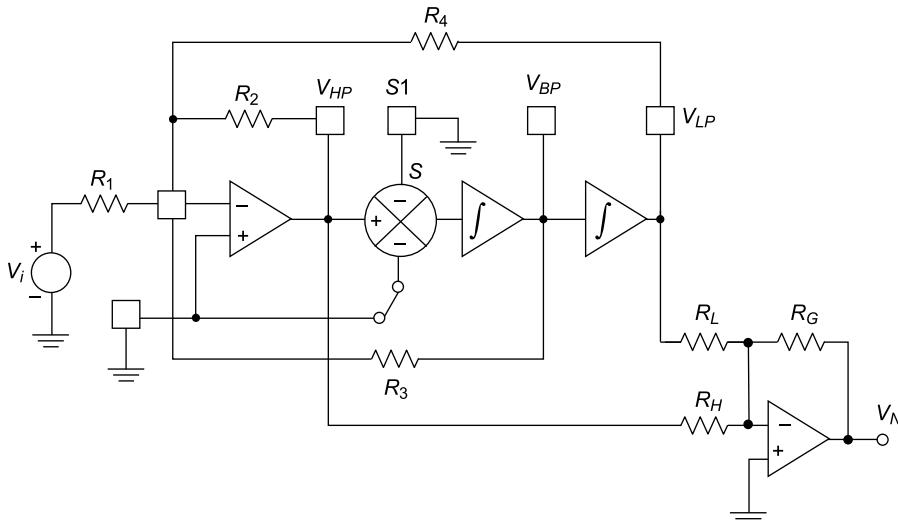
$$H_{OHP} = -\frac{R_2}{R_1}, \quad H_{OBP} = -\frac{R_3}{R_1} \quad \text{and} \quad H_{OLP} = -\frac{R_4}{R_1}$$

From the equation for  $f_o$ , it can be observed that  $f_o$  can be tuned by means of the ratio  $\frac{R_2}{R_4}$ . Hence, it is the most versatile mode of operation.

The summing amplifier is connected inside the integrator loop. Hence, the frequency limitation of its open-loop gain, namely its finite gain-BW product will cause  $Q$  enhancement at high frequencies. This can be compensated by connecting a phase-lead capacitance of the order of 10 pF to 100 pF in parallel with the resistor  $R_4$ .

### 6.18.7 State-variable Mode for Notch Response

Figure 6.54 shows the configuration for obtaining notch response, which is achieved by combining the high-pass obtained from Fig. 6.53 and the low-pass response obtained from Fig. 6.52 with the help of a summing amplifier connected externally. This circuit also provides  $HP$ ,  $BP$  and  $LP$  outputs.



**Fig. 6.54** Notch response using IC MF10 and external op-amp

When  $f \ll f_{ck}$ ,

$$\frac{V_N}{V_i} = H_{ON} \frac{(1 - f/f_z)^2}{1 - (f/f_o)^2 + (jf/f_o)/Q}$$

$$f_o = \frac{f_{ck}}{100} \sqrt{\frac{R_2}{R_4}} \text{ or } f_o = \frac{f_{ck}}{50} \sqrt{\frac{R_2}{R_4}}$$

$$f_z = \frac{f_{ck}}{100} \sqrt{\frac{R_H}{R_L}} \text{ or } f_z = \frac{f_{ck}}{50} \sqrt{\frac{R_H}{R_L}}$$

$$Q = \left[ \frac{R_3}{R_2} \right] \sqrt{\frac{R_2}{R_4}}$$

The gains for low-pass, high-pass, bandpass and notch responses are

$$H_{OLP} = -\frac{R_4}{R_1}, H_{OHP} = -\frac{R_2}{R_1}, H_{OBP} = -\frac{R_3}{R_1} \text{ and } H_{ON} = \frac{R_G R_4}{R_L R_1} \text{ respectively.}$$

The selection of resistances decides whether the notch is of high-pass or low-pass type. The input amplifier of a stage can be used while cascading the high-pass and low-pass outputs of the previous section.

## SUMMARY

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- A filter is a frequency selective circuit that allows a certain band of the input signal frequency components to pass through and attenuates undesired frequency components.
- The filters are classified into
  - Analog filters
    - Passive filters
    - Active filters
  - Digital filters
- The filters find use in communication, signal processing and sophisticated electronic instruments and for applications such as suppression of power-line hum, reduction of very low or high-frequency interference and noise, bandwidth limiting and specialised spectral shaping.
- Advantages of active filters over passive filters are their minimal loading effect, no insertion loss, feasibility for complex circuit design without inductors, rapid, stable and economical design, easy tunability, adjustable frequency response and realisation of network functions using *RLC* components and obtaining driving point or transfer characteristic that are unachievable with passive networks.
- The limitations of active filters are:
  - Their high frequency response is limited by the gain-bandwidth product and slew rate of the practical op-amps leading to comparatively lower bandwidth
  - The design becomes costly for high frequencies
  - They require dual polarity dc power supply
  - Vulnerability of the active element to the process parameter variations which make them sensitive to ambient conditions like temperature
- The basic filter responses are:
  - Low-pass filter (*LPF*) – allows only low frequency signals up to a certain breakpoint  $f_H$  to pass, while suppressing high frequency components.
  - High-pass filter (*HPF*) – allows only frequencies above a certain breakpoint to pass and attenuates the low frequency components.
  - Bandpass filter (*BPF*) – allows a specified range of frequencies to pass and it is the combination of high and low-pass filters.
  - Band-reject filter (*BRF*), Bandstop or Band elimination filter (*BEF*) – does not allow a specified range of frequencies to pass and it is the logical inverse of bandpass filter.
- The rate at which the response of a filter falls in the transition band is determined by the order of the filter. Higher the filter order, faster is the *roll-off* rate.
- The order of the filter is derived from the transfer function of the filter. The type of filter determines the shape of the transition band. This is reflected by its *damping factor*. The popular alignment types are Chebyshev, Butterworth, Elliptic and Bessel approximations.
- Chebyshev approximation provides a low-pass response that is equiripple in the passband with the transmission decreasing monotonically in the stopband.

- ❑ Butterworth approximation provides a low-pass response that is maximally flat at  $\omega = 0$  characterised by its moderate amplitude and phase response. The elliptic filter called as Cauer filter has equiripple passband and stopband. For a given filter order, passband and stopband deviations, the elliptic filters have the minimum transition bandwidth. The magnitude squared response is given by  $|H(j\omega)|^2$

$$= \frac{1}{1 + \varepsilon^2 U_N\left(\frac{\omega}{\omega_c}\right)} \text{ where } U_N\left(\frac{\omega}{\omega_c}\right) \text{ is the Jacobian elliptic function of order } N \text{ and } \varepsilon \text{ is a constant}$$

related to the passband ripple.

- ❑ The frequency transformation formulae for converting

- Low-pass with cut-off frequency  $\omega_c$  to low-pass with a new cut-off frequency  $\omega_c^*$  is given by

$$H(s) = H_p\left(\frac{\omega_c}{\omega_c^*} s\right).$$

- Low-pass with cut-off frequency  $\omega_c$  to high-pass cut-off frequency  $\omega_c^*$  is  $H(s) = H_p\left(\frac{\omega_c \omega_c^*}{s}\right)$ .

- Low-pass with cut-off frequency  $\omega_c$  to bandpass with lower cut-off frequency  $\omega_1$  and higher cut-off frequency  $\omega_2$  is  $H(s) = H_p\left(\omega_c \frac{s^2 + \omega_1 \omega_2}{s(\omega_2 - \omega_1)}\right)$ .

- Low-pass with cut-off frequency  $\omega_c$  to bandstop with lower cut-off frequency  $\omega_1$  and higher cut-off frequency  $\omega_2$  is  $H(s) = H_p\left(\omega_c \frac{s(\omega_2 - \omega_1)}{s^2 + \omega_1 \omega_2}\right)$

- ❑ General second order transfer function is

- $H(s) = \frac{V_o(s)}{V_i(s)} = \frac{Y_1 Y_2}{Y_1 Y_2 + Y_4(Y_1 + Y_2 + Y_3)}$  with unity gain.

- $H(s) = \frac{V_o(s)}{V_i(s)} = \frac{AY_1 Y_2}{Y_1 Y_2 + Y_4(Y_1 + Y_2 + Y_3) + Y_2 Y_3(1 - A)}$  with variable gain.

- ❑ The steps for the design of active low-pass filter are:

- Choose the value of high cut-off frequency  $f_H$
- Select the value of capacitor  $C$  such that its value is  $\leq 1\mu\text{F}$

- For unknown  $f_H$  and  $C$ , value of  $R$  is found by  $f_H = \frac{1}{2\pi RC}$

- Finally, select the values of  $R_i$  and  $R_f$  depending on the desired passband gain using  $A = \left[1 + \frac{R_f}{R_i}\right]$

- ❑ An  $N$ -pole low-pass filter has a high frequency roll-off rate of  $N \times 20$  dB/decade or  $N \times 6$  dB/decade,

and the 3 dB frequency is  $f_{3 \text{ dB}} = f_H = \frac{1}{2\pi RC}$ .

- ❑ Higher order filters are designed by adding additional  $RC$  networks.

- ❑ The bandpass filters are classified as wideband and narrowband bandpass filter.

- ❑ The narrowband band-reject filter called the *notch filter* is the twin- $T$  network cascaded with voltage follower.

- An all-pass filter allows all the frequency components of the input signal while providing the required phase shift at a given frequency of the input signal. They are also called delay equalisers, phase correctors, or constant delay filters.
- The high-pass second order filter is obtained from the low-pass second order filter by applying the transformation  $\frac{s}{\omega_0} \Big|_{\text{low-pass}} = \frac{\omega_0}{s} \Big|_{\text{high-pass}}$ . Hence, the resistors  $R$  and capacitors  $C$  can be interchanged in a low-pass active filter to get a high-pass active filter.
- An all-pass filter allows all the frequency components of the input signal to pass without attenuation, while providing the required phase shift at a given frequency of the input signal. The all-pass filters are also called delay equalisers, phase correctors, or constant delay filters.
- The state-variable filter can function as second order low-pass, high-pass and bandpass filters. It uses an integrator consisting of two op-amps and an adder consisting of one op-amp for implementing any type of filter.
- The state-variable filter has the advantages of easier tuning over a broad frequency range, independent  $Q$  adjustment and more complex filter configurations. Quad op-amps such as LF347, TL074 and TLC274, and op-amps with FET input devices are ideally suited for filter circuits. Universal single chip filters are series FLT-U2 from Datel and AF100 from National Semiconductor.
- The biquad filter called Tow–Thomas filter, after its inventors, is also referred to as a *resonator filter*. Its responses are as follows:

$$\frac{V_{BP}}{V_i} = T_{OBP}T_{BP} \quad \text{and} \quad \frac{V_{LP}}{V_i} = -\frac{1}{R_4C_2s} \frac{V_{BP}}{V_i} = T_{OLP}T_{LP}$$

where  $T_{OBP} = -\frac{R_f}{R_l}$  and  $T_{OLP} = \frac{R_2}{R_l}$

and,  $\omega_o = \frac{1}{\sqrt{R_4R_2C_1C_2}}$  and  $Q = \frac{R_f\sqrt{C_1}}{R_4R_2C_2}$

- The impedance converter changes positive impedance into a negative impedance and vice-versa. The capacitive reactance is converted into an inductive reactance and vice-versa. These conversions are used in neutralising the resistance or reactance thereby broadening the signal bandwidth and for noise reduction.
- Negative impedance conversion is the process of obtaining normally grounded impedance, which is proportional to given negative impedance that may be grounded or floating. Simulation of inductances using capacitances, and conversely, simulation of capacitances using inductances can be achieved using the negative impedance converters (NIC).
- The Generalised Impedance Converter (GIC) is an active  $RC$  circuit used to simulate inductors and frequency dependent elements. They are available as monolithic ICs.
- Sallen–Key filters, so named after their inventors, are commonly identified as VCVS (Voltage Controlled Voltage Source) filters. They can implement Butterworth, Chebyshev and Bessel approximations.
- The low-pass KRC filter response is given by

$$H(s) = \frac{V_o}{V_i} = \frac{A}{R_lC_1R_2C_2s^2 + [(1-A)R_lC_1 + R_lC_2 + R_2C_2]s + 1}$$

- The quadrature oscillator circuit generates two sinusoidal signals that are in quadrature with each other or with  $90^\circ$  phase difference. The frequency of sinusoidal oscillations is given by  $f_o = \frac{1}{2\pi RC}$ .
- The switched capacitor filters are all-IC circuits developed through the simulation of resistors by operating MOS capacitors with MOS switches and producing time constants that depend on the capacitance ratios.

- The switched capacitor filters work on the principle that a capacitor  $C$ , when periodically switched between two circuit nodes at a high rate  $f_{ck}$  is equivalent to a resistance  $R = \frac{1}{f_{ck} C}$  connecting the two circuit nodes.
- The switched capacitor network implementation types are *SC-I*, *SC-II* and *SC-III*.
- Various types of low-pass, high-pass, bandpass and band-reject active filters or sampled-data systems can be designed using the capacitor filter circuits.
- The features of *SC* integrator are:
  - No resistors are involved
  - The unity gain frequency  $f_o$  is determined by capacitance ratios, which are easier to control and maintain in an IC
  - The unity gain frequency  $f_o$  is proportional to the clock frequency  $f_{ck}$  that makes the *SC* filters programmable
- The practical limitations of *SC* filters are:
  - $f_{ck}$  is limited and controlled by the quality of MOS switches and the speed of op-amp, and values in the range of MHz are obtainable
  - The lower limit of  $f_{ck}$  dictated by leakage currents in MOS switches and the op-amp bias currents limit  $f_{ck}$  to a minimum possible value of 100 Hz
  - The *SC* filters are discrete-time operated
- Monolithic universal *SC* filters use dual integrator loop biquadratic circuit or biquad thus achieving second order responses. Higher order filters are constructed using the second order responses. Two of the popular switched capacitor filter ICs are LTC1060 from Linear Technology and MF10 from National Semiconductors, which are pin compatible with each other.
- MF10 switched capacitor filter available in a 20-pin DIP package, consists of two dual-integrator loop sections and each section can individually operate as low-pass, bandpass, high-pass, notch, or all-pass filter responses by the selection of external resistances. The filter parameters are determined by the resistance ratios that makes component tracking easier.
- The MF10 can be operated with centre frequencies up to 20 kHz, and clocks up to 1 MHz.
- State-variable mode provides high-pass, bandpass and low-pass responses by direct and sequential integrations.

## REVIEW QUESTIONS

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1. What is meant by filter?
2. Classify filters.
3. What are the four main types of filters?
4. Discuss the disadvantages of passive filters.
5. What are the advantages of active filters over passive filters?
6. What are the disadvantages of active filters over passive filters?
7. Discuss the advantages of active filters.
8. What do the terms order and poles indicate as related to filters?
9. Name some popular filter alignments.
10. What type of filter has a constant output response for voltage from dc up to the cut-off frequency?
11. What type of filter has a constant output response for voltage over a band of frequencies while attenuating all frequencies outside the band?
12. Explain where each of the following bandpass filters would be appropriate: high-pass/low-pass cascade, multiple-feedback, and state-variable.
13. Define low-pass and high-pass filters.
14. Define passband and stopband of a filter.
15. What is the roll-off rate of first order filter?

16. Why do we use higher order filters?
17. What is meant by Butterworth response?
18. What are the two characteristics of a Butterworth filter?
19. Explain the second order low-pass Butterworth filter.
20. Draw the characteristics of first order Butterworth filter.
21. Compare the frequency response characteristics of first order and second order Butterworth filters.
22. What are the characteristics of Butterworth filter?
23. What is Sallen-Key filter?
24. How do the popular filter alignments differ from one another in terms of phase and magnitude response?
25. Which alignment should be used if linear phase response is of particular importance?
26. Which alignment should be used if faster roll-off rate is of particular importance?
27. First order active LPF can also act as an integrator (True/False).
28. How can you realise a low-pass filter using op-amp? What are the advantages of active filters?
29. State briefly how low-pass to high-pass transformation is achieved.
30. When are the  $3dB$  down and critical frequencies of a filter identical?
31. Outline the process for creating higher order filters and explain why cascades of similar lower order filters do not give the appropriate results.
32. Draw a circuit for a first order active high-pass filter.
33. A first order active LPF has a cut-off frequency of 1 kHz. What is the simplest way to convert it to an HPF for 1 kHz?
34. It is desired to have an amplifier which has such a response that it gives zero amplification (or minimum) at a frequency of 1 kHz and maximum amplification at all other frequencies. Suggest a circuit with op-amp and explain its operation.
35. Explain from first principles how a second order Butterworth low-pass filter can be designed.
36. Draw the characteristics of a first order active notch filter.
37. Explain a band-reject filter.
38. Define an all-pass filter. How can it be justifiably called as *phase shift* circuits?
39. Why is the state-variable filter called the universal filter?
40. Explain the operation of a state-variable filter.
41. Explain the use of state-variable filter for various filter responses.
42. What is an impedance converter? What are its uses?
43. Explain the principle of negative impedance conversion.
44. Draw the circuit for neutralising the amplifier (a) input capacitance and (b) constant capacitance. Explain the operation of the circuit.
45. Why is the Tow–Thomas filter called a resonator filter?
46. Show the design features of biquad filter and analyse the circuit.
47. What are the two advantages of biquad filter?
48. Comment on the two significant responses of the biquad filter.
49. Simulate a negative resistance using NICs.
50. Define gyrator. What are its uses?
51. Explain the concept of impedance gyration with neat figures.
52. Explain the principle of operation of a gyrator using a two-port device model.
53. How do you justify the fact an ideal gyrator is a positive impedance converter?
54. Show the realisation of gyrator using op-amp and realise a grounded inductor using the same.
55. What is a grounded frequency dependent negative resistance?
56. What is  $D$ -element? Explain in brief.
57. Explain the operation of a generalised impedance converter using a circuit schematic using op-amps. How do you analyse for the equivalent impedance?
58. Use the GIC to simulate a grounded inductor.
59. Draw the circuit diagram of a KRC filter and explain its operation.

60. What are Sallen–Key filters? What are the type of approximations that can be implemented using the structure?
61. What are VCVS filters? Why are they so called?
62. Show how the KRC filter can be used as a low-pass filter. Derive for its output response.
63. Show how the KRC filter can be used as a high-pass filter. Derive for its output response.
64. What are multiple feedback filters? What are the other names of this type of filters? Justify the names.
65. Show the operation of a multiple feedback band-pass filter circuit using circuit diagram.
66. Show the operation of a multiple feedback low-pass filter circuit using circuit diagram.
67. Briefly explain the principle of the switched-capacitor filter.
68. What are the advantages and disadvantages of switched-capacitor ICs over the traditional active filters?
69. What are switched capacitor networks? Why do you need switched capacitor filters when you have conventional filters?
70. Switched capacitor networks do not save area in IC fabrication. (True/False)
71. Describe how a capacitor in conjunction with two switching transistors can behave as a resistor.
72. Explain the operation of a switched capacitor integrator with neat figures.
73. Draw the circuits of various switched capacitor arrangements and explain their operations.
74. Explain the operation of a monolithic switched capacitor IC and explain its operation.
75. Explain the use of any one of the switched capacitor ICs for low-pass, high-pass, bandpass and notch responses.
76. A first order low-pass Butterworth active filter has a cut-off frequency of 12 kHz and unity gain at low frequency. Find the voltage transfer function magnitude in dB at 15 kHz for the filter.
77. Design a first order low-pass filter at a cut-off frequency of 2.5 kHz with a passband gain of 1.5.
78. Design a second order Butterworth high-pass active filter with the following specifications with the circuit configuration:
  - (i) Voltage gain = 2.5
  - (ii) Cut-off frequency = 5 kHz
79. Design a second order low-pass Butterworth filter with a cut-off frequency of 12 kHz and unity gain at low frequency. Also determine the voltage transfer function magnitude in dB at 15 Hz for the filter.
80. Design a second order Butterworth low-pass filter having upper cut-off frequency of 2.5 kHz.
81. A third order and a fourth order low-pass Butterworth filters have a cut-off frequency of 12 kHz and unity gain at low frequency. Determine the voltage transfer function magnitude in dB at 15 Hz for each filter.
82. Design a fourth order Butterworth low-pass filter having an upper cut-off frequency of 2.5 kHz.
83. First order active LPF can also act as an Integrator. (True/False)
84. Design a first order high-pass filter at a cut-off frequency of 2.5 kHz with a passband gain of 1.5. Also, plot its frequency response.
85. Design a fourth order high-pass Butterworth filter with unity gain having a cut-off frequency of 60 kHz. Determine the frequency at which the voltage transfer function magnitude is 1% of its maximum value.
86. If a bandpass filter has a lower cut-off frequency  $f_L = 200$  Hz and a higher cut-off frequency  $f_H = 2000$  Hz, find its bandwidth and the resonant frequency.
87. Given a bandpass filter with resonant frequency ( $f_r$ ) of 1 kHz and a bandwidth ( $B$ ) of 4 kHz, find its (a) quality factor, (b) lower cut-off frequency, and (c) higher cut-off frequency.
88. If a bandpass filter has a resonant frequency of 1200 Hz and a bandwidth of 3000 Hz, find the lower and upper cut-off frequencies.
89. Given a bandpass filter with lower and higher cut-off frequencies of 50 Hz and 60 Hz respectively, find its (a) quality factor, (b) resonant frequency, and (c) bandwidth.
90. Design a narrowband bandpass filter using an op-amp. The resonant frequency is 100 Hz and  $Q = 2$ . Assume  $C = 0.1 \mu F$ .
91. Design a narrowband bandpass filter with a resonant frequency of 300 Hz and a bandwidth of 30 Hz.
92. Design a 50 Hz active notch filter.
93. Design a wideband bandpass filter with  $f_L = 200$  Hz and  $f_H = 1$  kHz and calculate the value of  $Q$  for the filter.
94. Design an active bandpass filter for a passband of 500 Hz with  $f_L = 1$  kHz.

# Waveform Generators

## 7.1 INTRODUCTION

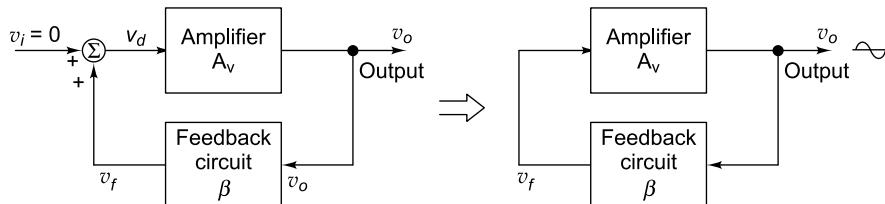
The op-amps are widely used in circuits for generating various waveforms. Most of the analog and digital equipments require one or more periodic waveforms for timing, control and other functions. The commonly used sinusoidal, square and triangular waveform generations are other forms of evolution in the design of operational amplifiers. Their applications have made the design of oscillators possible, which are capable of generating repetitive waveforms of fixed frequency and amplitude without the need of any other signal. The terms oscillator and function generator or waveform generator represent the circuits employed for generating such waveforms. This chapter discusses sinusoidal oscillators, and non-sinusoidal oscillators including multivibrators and applications of timer IC 555. The monolithic ICL8038 function generator and its applications are also dealt with.

## 7.2 SINE-WAVE GENERATORS

The sine-wave is one of the most fundamental waveforms. The generation of sine-wave is a challenging task if ideal waveform characteristics are expected. In the sine-wave oscillators using op-amps, the required phase-shift of  $180^\circ$  in the feedback loop from output to input is obtained by using either  $L$  and  $C$  or  $R$  and  $C$  components.

### 7.2.1 Conditions for Oscillations

An oscillator is basically a feedback amplifier, in which a fraction of the output is fed back to the input with the use of a feedback circuit. The block diagram of an oscillator is shown in Fig. 7.1.



**Fig. 7.1** Block diagram of an oscillator

As illustrated in Fig. 7.1,

$$\begin{aligned} v_d &= v_f + v_i \\ v_o &= A_v v_d = A_v(v_f + v_i) \\ v_f &= \beta v_o = \beta A_v(v_f + v_i) \end{aligned}$$

or  $v_o = A_v(\beta v_o + v_i)$

Therefore,  $\frac{v_o}{v_i} = \frac{A_v}{1 - A_v \beta}$

For an oscillator,  $v_i = 0$ , and for sustained oscillation  $v_o \neq 0$ . Therefore,

$$|A_v \beta| = 1 \quad (7.1)$$

and  $\angle A_v \beta = 0^\circ \text{ or } 360^\circ \quad (7.2)$

Therefore, the two basic requirements for sustained oscillations are:

- (i) the magnitude of the loop gain,  $A_v \beta$ , must be unity and
- (ii) the total phase-shift of the loop gain,  $A_v \beta$ , must be equal to  $0^\circ$  or  $360^\circ$

Many different types of oscillators are available which are characterised by the types of components used in the feedback network, e.g. RC oscillator, LC oscillator and crystal oscillator.

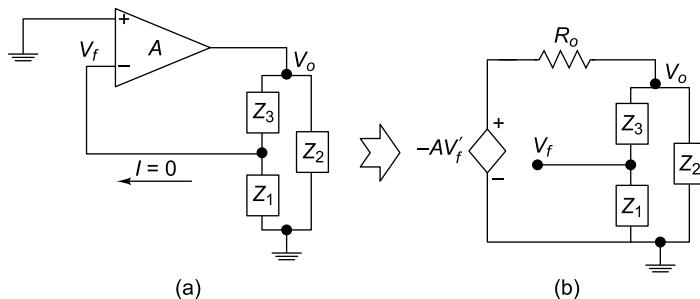
### 7.2.2 LC Oscillators

A general form of LC oscillator is shown in Fig. 7.2(a). Here the amplifier using op-amp is considered ideal and it has a non-zero output resistance  $R_o$ . Referring to its equivalent shown in Fig. 7.2(b), we get

$$\beta = -\frac{V_f}{AV'_f}.$$

Applying the voltage divider equation to Fig. 7.2 (b) gives

$$V_f = \frac{Z_1}{Z_1 + Z_3} V_o$$



**Fig. 7.2** (a) LC Oscillator circuit using an ideal op-amp with output impedance  $R_o$   
 (b) Its equivalent circuit

From Fig. 7.2(b), we get

$$V_o = -\frac{Z}{Z + R_o} AV'_f$$

where  $R_o$  is the output impedance and  $Z = Z_2 \parallel (Z_1 + Z_3)$ .

That is,

$$\frac{1}{AV'_f} = -\frac{1}{V_o} \frac{Z}{Z + R_o} = -\frac{1}{V_o} \frac{Z_2(Z_1 + Z_3)}{Z_2(Z_1 + Z_3) + R_o(Z_1 + Z_2 + Z_3)}$$

Solving for  $\beta$ , we get

$$\beta = -\frac{V_f}{AV'_f} = -\frac{Z_1 Z_2}{R_o(Z_1 + Z_2 + Z_3) + Z_2(Z_1 + Z_3)} \quad (7.3)$$

We know that for the  $LC$  tunable oscillators, the three impedances ( $Z_1 + Z_2 + Z_3$ ) are purely reactive, i.e. the real part is equal to zero as given by

$$Z_i = jX_i, X_i > 0 \quad \text{for } i = 1, 2, 3$$

Then, Eq. (7.3) becomes

$$\beta = \frac{X_1 X_2}{jR_o(X_1 + X_2 + X_3) + X_2(X_1 + X_3)}$$

For  $\beta$  to be real

$$X_1 + X_2 + X_3 = 0, \quad (7.4)$$

and

$$\beta(\omega_o) = -\frac{X_1}{X_1 + X_3}$$

where  $\omega_o$  is the oscillation frequency. Using the two previous equations, we get

$$\beta(\omega_o) = \frac{X_1}{X_2}.$$

Since  $\beta(\omega_o)$  must be positive,  $X_1$  and  $X_2$  must have the same sign. This means that they are of the same kind of reactance, namely, two capacitors or two inductors. From the condition that the imaginary part equals zero, we find that if  $X_1$  and  $X_2$  are capacitors,  $X_3$  must be an inductor and vice versa. Therefore, based on the choice of reactive elements, the  $LC$  oscillators are identified as Colpitts and Hartley oscillators.

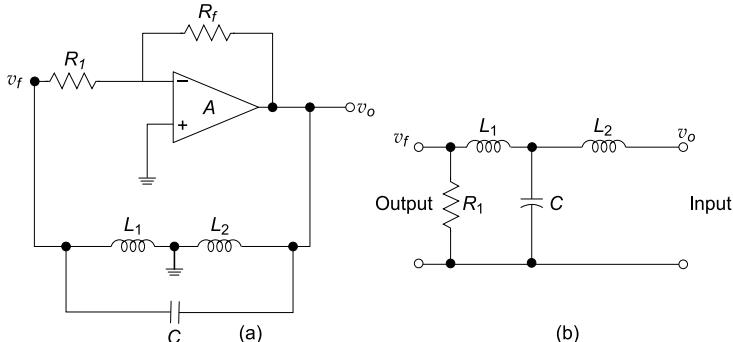
**Hartley oscillator** The circuit diagram of Hartley oscillator is shown in Fig. 7.3. The op-amp is connected to operate in inverting mode. An  $LC$  network consisting of inductive reactances  $X_1$  and  $X_2$  and a capacitive reactance  $X_3$  forms the feedback network and the phase-shift through the feedback network is  $180^\circ$ . The reactances are:

$$X_1 = j\omega L_1$$

$$X_2 = j\omega L_2$$

and

$$X_3 = -\frac{j}{\omega C}$$



**Fig. 7.3** Hartley oscillator (a) Circuit diagram and (b) Feedback network

Using Eq. (7.4), we get the angular frequency of oscillation and the gain as

$$\omega_o = \sqrt{\frac{1}{C(L_1 + L_2)}} \quad \text{and} \quad \beta(\omega_o) = \frac{L_1}{L_2}$$

$$\text{The frequency of oscillation is } f_o = \frac{1}{2\pi\sqrt{CL_T}} \quad (7.5)$$

where  $L_T = L_1 + L_2$  or  $L_T = L_1 + L_2 + 2M$

and  $M$  is the mutual inductance of coils  $L_1$  and  $L_2$ .

**Colpitts oscillator** The circuit diagram of Colpitts oscillator is shown in Fig. 7.4. The feedback signal is connected to (-) input terminal, such that the op-amp is working as an inverting amplifier. The feedback circuit consisting of two capacitive reactances  $X_1$  and  $X_2$ , and the inductive element  $X_3$  provides  $180^\circ$  phase-shift. The oscillation occurs when the feedback  $\beta$  is real. The reactances are:

$$X_1 = \frac{1}{j\omega C_1} = -\frac{j}{\omega C_1}$$

$$X_2 = \frac{1}{j\omega C_2} = -\frac{j}{\omega C_2}$$

and

$$X_3 = j\omega L$$

Using Eq. (7.4), we get the angular frequency of oscillation  $\omega_o$ , and the gain  $\beta(\omega_o)$  as

$$\omega_o = \sqrt{\frac{1}{L\left(\frac{C_1 C_2}{C_1 + C_2}\right)}}$$

and

$$\beta(\omega_o) = \frac{C_2}{C_1}$$

Thus, the frequency of oscillation for the Colpitts oscillator is

$$f_o = \frac{1}{2\pi\sqrt{LC_T}} \quad (7.6)$$

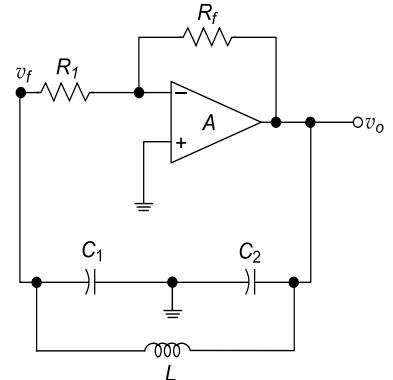
where

$$C_T = \frac{C_1 C_2}{C_1 + C_2}.$$

The feedback factor  $\beta$  at the oscillation frequency is  $-1$ .

### 7.2.3 RC Oscillators

All the oscillators using tuned  $LC$  circuits operate well at high frequencies. At low frequencies, as the inductors and capacitors required for the timing circuit would be very bulky,  $RC$  oscillators are found to be more suitable. Two important  $RC$  oscillators are (i)  $RC$  phase shift oscillator and (ii) Wien Bridge oscillator.

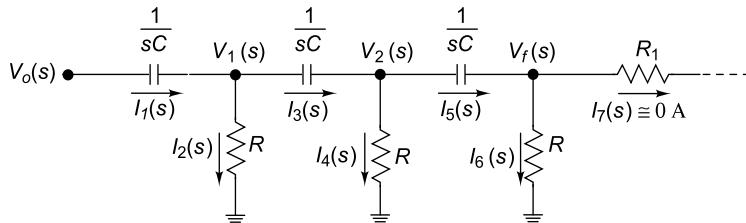


**Fig. 7.4** Colpitts oscillator

**RC phase-shift oscillator** The *RC* phase-shift oscillator consisting of an op-amp serving as the amplifier stage and the cascaded *RC* network acting as the feedback circuit is shown in Fig. 7.5. The op-amp is used in inverting configuration and it produces  $180^\circ$  phase-shift at the output. The cascaded *RC* networks connected in the feedback network path provide an additional phase-shift of  $180^\circ$ . Therefore, the total phase-shift around the loop is  $360^\circ$  (or  $0^\circ$ ). When the gain of the amplifier is sufficiently large and the phase-shift of the cascaded *RC* network is exactly  $180^\circ$ , the circuit will oscillate at the frequency determined by the *RC* feedback network.

**Frequency of oscillation** Consider the *RC* feedback circuit shown in Fig. 7.6. Applying Kirchhoff's current law at node  $V_1(s)$ , we have

$$I_1(s) = I_2(s) + I_3(s)$$



**Fig. 7.6** *RC* network of the phase-shift oscillator in *s*-domain

$$\text{That is, } \frac{V_o(s) - V_1(s)}{(1/sC)} = \frac{V_1(s)}{R} + \frac{V_1(s) - V_2(s)}{(1/sC)}$$

$$\text{Thus, } V_1(s) = \frac{[V_o(s) + V_2(s)]RCs}{2RCs + 1} \quad (7.7)$$

Similarly, at node  $V_2(s)$ ,

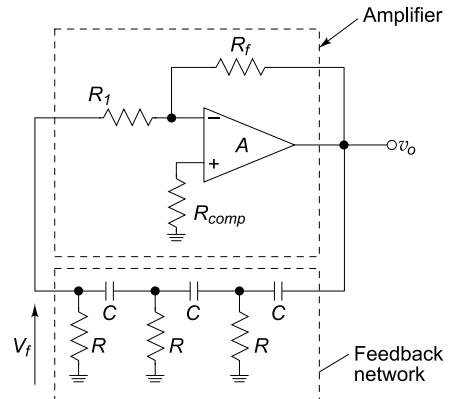
$$I_3(s) = I_4(s) + I_5(s)$$

$$\text{That is, } \frac{V_1(s) - V_2(s)}{(1/sC)} = \frac{V_2(s)}{R} + \frac{V_2(s) - V_f(s)}{(1/sC)}$$

Solving for  $V_1(s)$ , we get

$$V_1(s) = \frac{(2RCs+1)V_2(s)}{RCs} - V_f(s) \quad (7.8)$$

When  $R_1 \gg R$ ,  $I_5 \approx I_6$  and  $V_f(s) = V_2(s) \frac{R}{R + \frac{1}{sC}}$



**Fig. 7.5** *RC* phase-shift oscillator

Therefore,  $V_2(s) = \frac{(RCs + 1)}{RCs} V_f(s)$  (7.9)

Substituting Eq. (7.9) in Eq. (7.8) results in

$$\frac{RCs V_o(s)}{2RCs + 1} + \frac{(RCs + 1)V_f(s)}{2RCs + 1} = \frac{(2RCs + 1)(RCs + 1)V_f(s)}{(RCs)^2} - V_f(s)$$

Simplifying for  $\frac{V_f(s)}{V_o(s)}$ , we get

$$\beta = \frac{V_f(s)}{V_o(s)} = \frac{R^3 C^3 s^3}{R^3 C^3 s^3 + 6R^2 C^2 s^2 + 5RCs + 1} \quad (7.10)$$

The voltage gain of the op-amp  $A_v$  is

$$A_v = \frac{V_o(s)}{V_f(s)} = -\frac{R_f}{R_l} \quad (7.11)$$

We know that for any oscillator, the necessary condition for the oscillation is  $A_v \beta = 1$ . Therefore, using Eqs. (7.10) and (7.11), we obtain

$$A_v \beta = -\frac{R_f}{R_l} \frac{R^3 C^3 s^3}{R^3 C^3 s^3 + 6R^2 C^2 s^2 + 5RCs + 1} = 1$$

Substituting  $s = j\omega$  in the above equation, we obtain

$$\left( -\frac{R_f}{R_l} \right) (-j\omega^3 R^3 C^3) = (-j\omega^3 R^3 C^3) - 6\omega^2 R^2 C^2 + j5\omega RC + 1$$

Equating the real parts, we get

$$0 = -6\omega_o^2 R^2 C^2 + 1$$

$$\omega_o^2 = \frac{1}{6R^2 C^2} \quad (7.12)$$

or  $f_o = \frac{1}{2\pi\sqrt{6RC}}$

Equating the imaginary parts, we get

$$\left( -\frac{R_f}{R_l} \right) (-j\omega_o^3 R^3 C^3) = -j\omega_o^3 R^3 C^3 + 5j\omega_o RC$$

That is,  $\frac{-R_f}{R_l} = 1 - \frac{5}{\omega_o^2 R^2 C^2}$

Substituting for  $\omega_o^2$  from Eq. (7.12),

$$\left| \frac{R_f}{R_l} \right| = |1 - 30| = 29 \text{ or } R_f = 29 R_l \quad (7.13)$$

Therefore, the gain of the amplifier should be at least 29, and the total phase-shift around the loop should be exactly  $360^\circ$ .

For achieving the desired frequency of oscillation  $f_o$ , an available value of capacitor  $C$  is chosen and then the value of  $R$  is calculated using Eq. (7.12). The desired amplitude of oscillations can be obtained by using Zener diodes connected *back-to-back* at the output of op-amp  $A$ .

### Example 7.1

Design the RC phase-shift oscillator of Fig. 7.5 for  $f_o = 300\text{ Hz}$ .

#### Solution

Assume  $C = 0.1 \mu\text{F}$ .

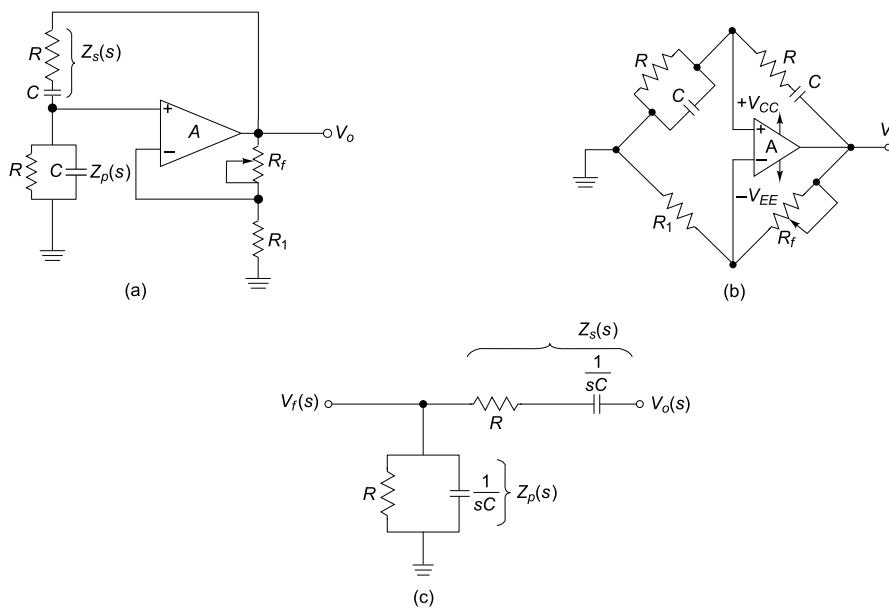
$$\text{We know that, } f_o = \frac{1}{2\pi\sqrt{6}RC}.$$

$$\text{Therefore, } R = \frac{1}{(2\pi\sqrt{6})(0.1 \times 10^{-6})(300)} = 2.17 \text{ k}\Omega$$

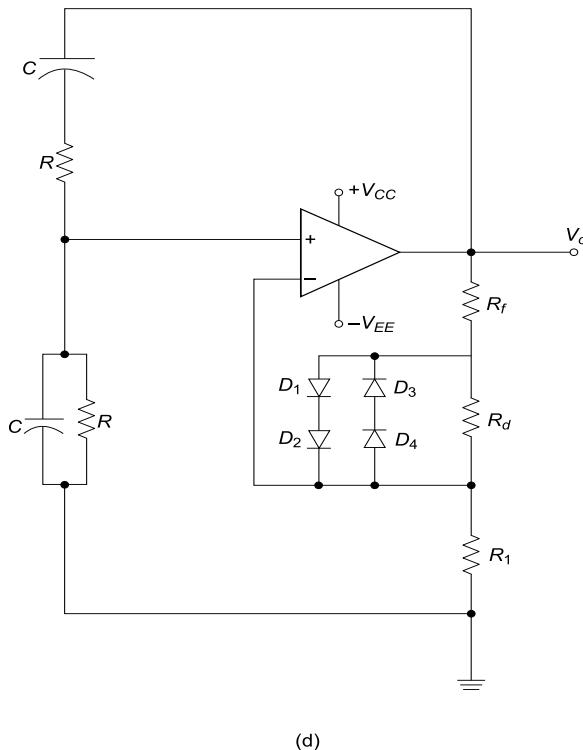
To prevent the  $RC$  network from loading the amplifier, it is selected such that  $R_1 > 10 R$ . Letting  $R = 2.2 \text{ k}\Omega$ , we get  $R_1 = 22 \text{ k}\Omega$ .

We know that,  $R_f = 29 R_1$ . Therefore,  $R_f = 29 \times 22 \times 10^3 = 638 \text{ k}\Omega$

**Wien Bridge oscillator** Wien Bridge oscillator is the most commonly used audio frequency oscillator due to its inherent simplicity and stability. Figure 7.7(a) shows the Wien Bridge oscillator using op-amp. Since the op-amp is connected to operate in non-inverting mode, it produces no phase-shift at the output. The Wien Bridge circuit is connected between the input and output terminals of the amplifier. The bridge consists of a series  $RC$  network (shown as  $Z_s(s)$ ) forming one arm of the bridge circuit, a parallel  $RC$  network (shown as  $Z_p(s)$ ) forming the second arm, input resistance  $R_1$  and feedback resistance  $R_f$  forming the third and fourth arms of the bridge circuit respectively as shown in Fig. 7.7(b). The feedback circuit of the Wien Bridge oscillator is shown in Fig. 7.7(c).



Contd.



(d)

**Fig. 7.7** Wien Bridge oscillator: (a) Circuit diagram (b) Equivalent circuit (c) Feedback circuit of the Wien Bridge oscillator in *s*-domain and (d) Output amplitude stabilisation

It is known that the total phase-shift around the circuit must be  $0^\circ$  or  $360^\circ$  for oscillations to occur. It is achieved when the bridge is balanced, i.e. at resonance. Thus the frequency of oscillation is the resonant frequency of the balanced Wien Bridge.

**Frequency of oscillation** Considering the circuit shown in Fig. 7.7(c) in the *s*-domain,

$$V_f(s) = \frac{Z_p(s)}{Z_p(s) + Z_s(s)} V_o(s)$$

where  $Z_p(s) = R \parallel \frac{1}{sC} = \frac{R}{(RCs + 1)}$  and  $Z_s(s) = R + \frac{1}{sC} = \frac{(RCs + 1)}{sC}$

Therefore,

$$\begin{aligned} \beta &= \frac{V_f(s)}{V_o(s)} = \frac{Z_p(s)}{Z_p(s) + Z_s(s)} = \frac{RCs}{(RCs + 1)^2 + RCs} \\ &= \frac{RCs}{R^2 C^2 s^2 + 3RCs + 1} \end{aligned} \quad (7.14)$$

The voltage gain  $A_v$  of the op-amp is  $A_v = \frac{V_o(s)}{V_f(s)} = 1 + \frac{R_f}{R_l}$  (7.15)

Using Eqs. (7.14) and (7.15) for satisfying the condition of oscillation  $|A_v \beta| = 1$ , we get

$$\left(1 + \frac{R_f}{R_1}\right) \frac{RCs}{R^2C^2s^2 + 3RCs + 1} = 1$$

Substituting  $s = j\omega_o$  in the above equation, we get

$$\left(1 + \frac{R_f}{R_1}\right) j\omega_o RC = (-\omega_o^2 R^2 C^2 + 3j\omega_o RC + 1)$$

Equating the real parts, we have

$$\omega_o^2 R^2 C^2 = 1$$

Therefore,  $f_o = \frac{1}{2\pi RC}$  (7.16)

Equating the imaginary parts, we get

$$\left(1 + \frac{R_f}{R_1}\right) j\omega_o RC = 3j\omega_o RC$$

or  $A_v = 1 + \frac{R_f}{R_1} = 3$  and  $R_f = 2R_1$  (7.17)

The Wien Bridge RC oscillators can be used in the range of 5 Hz to about 1 MHz, e.g. in low frequency applications like audio generators. It is not suitable for high frequency applications above 1 MHz, due to the fact that the phase-shift through the amplifier and the phase-shift of the *lead-lag* circuit jointly cause resonance to occur at different frequencies other than the specified resonant frequency.

To maintain a stable amplitude for the oscillations, the resistor of Fig. 7.7(a) is normally replaced by a non-linear resistor. This adjusts the loop gain based on the existing amplitude of oscillations. When the amplitude increases, it causes a rise in the current through  $R_1$  which in turn rises the value of  $R_1$ . It actually means an increased amount of negative feedback results in a corresponding reduction in loop gain and oscillation amplitude.

It is observed that only the response of the non-linear resistance  $R_1$  determines the stability of oscillations of the circuit shown in Fig. 7.7(d). The stabilisation of output amplitude is realised by controlling the amplifier gain through the diodes  $D_1$  to  $D_4$ .

The series combinations of  $D_1 - D_2$  and  $D_3 - D_4$  are connected in opposite directions across resistor  $R_d$ , introduced between the two resistive arms formed by  $R_f$  and  $R_1$  of Fig. 7.7(a). When the output oscillation amplitude rises large enough to forward bias either the  $D_1 - D_2$  or  $D_3 - D_4$  combination, resistor  $R_d$  is short circuited and the amplifier gain gets controlled. In turn, this will lower the output amplitude. When the output level falls, the diodes would turn-off, thereby increasing the effective  $R_f$  and the resulting gain. Hence, sustained oscillations can be realized.

## Example 7.2

Design a Wien Bridge oscillator of Fig. 7.7 (a) for  $f_o = 2$  kHz

### Solution

We know that  $f_o = \frac{1}{2\pi RC}$ . Assume  $C = 0.05 \mu\text{F}$ .

Therefore,  $R = \frac{1}{2\pi(0.05 \times 10^{-6})(2 \times 10^3)} = 1.592 \text{ k}\Omega$

Assuming

$$R_1 = 1.8 \text{ k}\Omega, \text{ we get } R_f = 2 R_1 = 2 \times 1.8 \times 10^3 = 3.6 \text{ k}\Omega \\ \approx 3.9 \text{ k}\Omega \text{ (Standard value)}$$

### 7.2.4 Quadrature Oscillator

Quadrature signals are those two signals of same frequency but separated by a phase shift of  $90^\circ$  from each other. The quadrature oscillator circuit shown in Fig. 7.8 generates two sinusoidal signals that are in *quadrature* with each other or with  $90^\circ$  phase difference. The quadrature oscillator circuit requires dual op-amp formed by  $A_1$  and  $A_2$  and three  $RC$  combinations. The two amplifiers are connected in cascade to form a feedback loop. The op-amp  $A_1$  operates as a non-inverting integrator. The op-amp  $A_2$  acts as an inverting integrator. The output of  $A_2$  is connected to voltage divider network consisting of  $R_1 - C_1$  combination and the voltage across  $C_1$  is feedback to the non-inverting input of  $A_1$ .

A total phase shift of  $360^\circ$  is needed around the loop. The op-amp  $A_2$  acts as an inverting integrator, contributing for  $270^\circ$  of phase shift i.e.  $180^\circ$  due to inverter arrangement and  $90^\circ$  due to integrator. The remaining  $90^\circ$  phase shift is realised in the voltage divider  $R_1C_1$  and op-amp  $A_1$ .

The feedback loop is represented by the set of differential equations  $RC \frac{dv_s}{dt} = v_c$  and  $RC \frac{dv_c}{dt} = -v_s$ . Then, assuming  $R_1C_1 = RC$ , the frequency of sinusoidal oscillations is given by  $f_o = \frac{1}{2\pi RC}$ . In practice, the resistance  $R_1$  is chosen slightly larger than  $R$ . This ensures sufficient feedback for oscillation. The amplitude of oscillations is stabilised by the use of Zener diodes connected back to back.

## 7.3 MULTIVIBRATORS

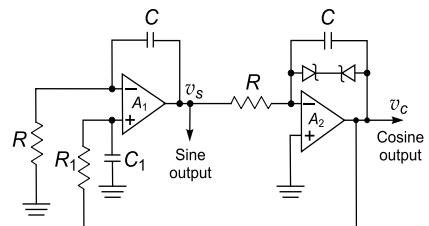
Multivibrators are regenerative circuits, which are mainly used in timing applications. Based on their operational characteristics, they can be classified into three categories, namely,

- (i) Astable multivibrator
- (ii) Monostable multivibrator
- (iii) Bistable multivibrator

The astable multivibrator toggles between one state and the other without the influence of any other external control signal. It is also called a *free-running multivibrator*. The monostable multivibrator or *one-shot* requires an external signal called a *trigger* to force the circuit into a quasi-stable state for a particular time duration or delay. A suitable timing network determines the time delay and it returns to the stable state at the end of the delay time.

### 7.3.1 Astable (Free-running) Multivibrator

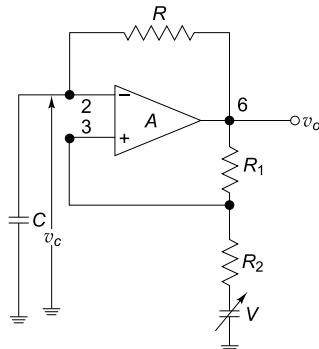
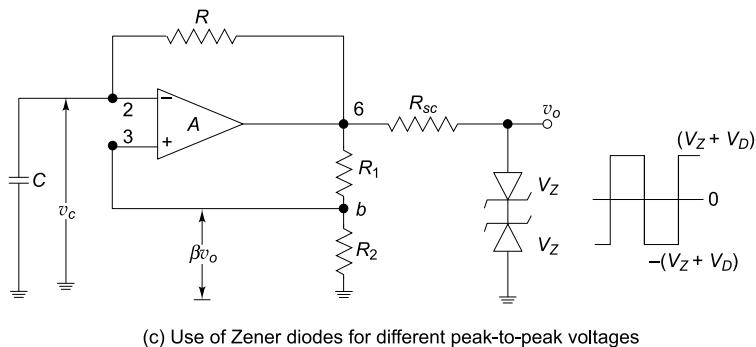
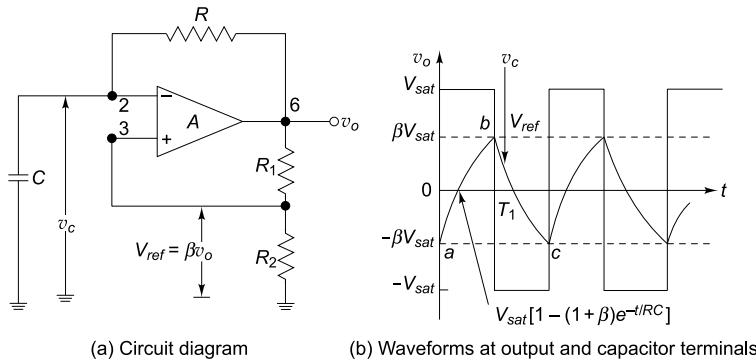
An astable multivibrator is a square-wave generator. Figure 7.9(a) shows the circuit of an astable multivibrator with the output of op-amp feedback to the (+) input terminal. The resistors  $R_1$  and  $R_2$  form



**Fig. 7.8** Quadrature oscillator

a voltage divider network, and a fraction  $\beta = \frac{R_2}{R_1 + R_2}$  of the output is fed back to the input. The output can take values of  $+\beta V_{sat}$  or  $-\beta V_{sat}$ . The voltage  $\pm \beta V_{sat}$  acts as  $V_{ref}$  at the (+) input terminal. The output is also connected to the (-) input terminal through an integrating low-pass RC network. When the voltage  $v_c$  across capacitor  $C$  just exceeds  $V_{ref}$ , switching takes place resulting in a square-wave output.

To understand the operation of the circuit, let us consider that initially the output is at  $+V_{sat}$  as shown in Fig. 7.9(b).



(d) Asymmetric square wave generator

**Fig. 7.9** Square-wave generator using op-amp: (a) Circuit diagram (b) Waveforms at output and capacitor terminals (c) Use of Zener diodes for different peak-to-peak voltages (d) Asymmetric square-wave generator

The capacitor  $C$  with its voltage shown as  $v_c$  starts charging through resistor  $R$  towards  $+V_{sat}$ . The voltage at (+) input terminal is held at  $+\beta V_{sat}$  as indicated by the use of  $R_1 - R_2$  potential divider network. The charging of  $C$  continues until the voltage  $v_c$  at the (-) input terminal is just greater than the voltage at the (+) input terminal,  $+\beta V_{sat}$ . When this happens as shown at point  $b$  of Fig. 7.9(b), the output is switched down to  $-V_{sat}$ . The voltage  $+\beta v_o$  across the capacitor now starts discharging through resistance  $R$  and charging towards  $-V_{sat}$ . The capacitor voltage  $v_c$  now becomes increasingly more and more negative and at point  $c$  just exceeds  $-\beta V_{sat}$ . The output now switches back to  $+V_{sat}$ , and the cycle repeats.

Summarising,

- (i) when  $v_o = +V_{sat}$ ,  $C$  charges from  $-\beta V_{sat}$  to  $+\beta V_{sat}$  and switches  $v_o$  to  $-V_{sat}$  and
- (ii) when  $v_o = -V_{sat}$ ,  $C$  charges from  $+\beta V_{sat}$  to  $-\beta V_{sat}$  and switches  $v_o$  to  $+V_{sat}$ .

**Period and frequency of oscillation** The frequency of the free running multivibrator is determined by the charging and discharging time of the capacitor between the voltage levels  $-\beta V_{sat}$  and  $+\beta V_{sat}$  and vice versa. The voltage across the capacitor as a function of time can be represented as

$$v_c(t) = V_{fin} + (V_{ini} - V_{fin}) e^{\frac{-t}{RC}}$$

where  $V_{fin}$  is the final value of the voltage and  $V_{ini}$  is the initial voltage. Considering the charging of the capacitor from point  $a$  towards  $+V_{sat}$ ,

$$\begin{aligned} v_c(t) &= +V_{sat} + (-\beta V_{sat} - V_{sat}) e^{\frac{-t}{RC}} \\ &= V_{sat} - V_{sat} (1 + \beta) e^{\frac{-t}{RC}} \end{aligned} \quad (7.18)$$

At  $t = T_1$ , the voltage across the capacitor reaches  $+\beta V_{sat}$  and switches at point  $b$ . Therefore, capacitor voltage  $v_c$  at time  $T_1$  is

$$\beta V_{sat} = V_{sat} \left( 1 - (1 + \beta) e^{\frac{-T_1}{RC}} \right)$$

$$\text{That is, } (1 - \beta) = (1 + \beta) e^{\frac{-T_1}{RC}}$$

$$\text{and } T_1 = RC \ln \frac{1 + \beta}{1 - \beta} = RC \ln \frac{R_1 + 2R_2}{R_1}$$

As shown in Fig. 7.9(b), the total time period is given by

$$T = 2T_1 = 2RC \ln \frac{1 + \beta}{1 - \beta} \quad (7.19)$$

$$\text{That is, } T = 2RC \ln \left( \frac{R_1 + 2R_2}{R_1} \right) \quad (7.20)$$

and the output is a symmetrical waveform.

$$\text{Hence, the frequency of oscillation is } f_o = \frac{1}{T} = \frac{1}{2RC \ln \left( \frac{1 + \beta}{1 - \beta} \right)} \quad (7.21)$$

Considering  $R_1 = R_2$ , we have  $\beta = \frac{R}{2R} = 0.5$ ,  $T = 2RC \ln 3$  and

$$f_o = \frac{1}{2RC \ln 3} = \frac{1}{2.2RC} \quad (7.22)$$

Equation (7.19) shows that the period is directly proportional to the time constant,  $RC$ . Thus, varying either  $R$  or  $C$  changes the period correspondingly. Therefore, providing a tunable resistance  $R$  paves the way for a continuously tunable square-wave generator. The output peak amplitudes can be varied by the use of Zener diodes connected back to back as shown in Fig. 7.9(c).

The output voltage is then regulated to  $\pm(V_z + V_D)$  where  $V_z$  is the Zener voltage. Then the peak-to-peak output voltage is given by  $v_o$  (peak-to-peak) =  $2(V_z + V_D)$ . To generate an asymmetric square-wave, a variable voltage source  $V$  can be introduced as shown in Fig. 7.9(d).

### **Example 7.3**

For the circuit shown in Fig. 7.9(a), assuming that  $R_1 = 116 \text{ k}\Omega$ ,  $R_2 = 100 \text{ k}\Omega$ , and  $\pm V_{sat} = \pm 14 \text{ V}$ , find

- (i) the time constant to produce 1 kHz output
- (ii) the resistance  $R$  and
- (iii) the maximum value of differential input voltage.

#### **Solution**

(a) From Eq. (7.20), the time period,  $T = 2RC \ln \frac{R_1 + 2R_2}{R_1}$

$$\begin{aligned} T &= 2RC \ln(116 \times 10^3 + 2 \times 100 \times 10^3 / 116 \times 10^3) \\ &= 2RC \ln(316 \times 10^3 / 116 \times 10^3) \\ &= 2RC \text{ (since, } \ln(316 \times 10^3 / 116 \times 10^3) \approx 1) \end{aligned}$$

$$\text{Given } f = 1 \text{ kHz, } T = \frac{1}{f} = \frac{1}{1 \times 10^3} = 1 \text{ ms}$$

$$\text{That is, } 2RC = 1 \times 10^{-3} \text{ sec}$$

$$\text{Therefore, the time constant } RC = 0.5 \times 10^{-3} \text{ sec}$$

(b) With  $C = 0.01 \mu\text{F}$ ,  $R = \frac{0.5 \times 10^{-3}}{0.01 \times 10^{-6}} = 50 \text{ k}\Omega$

(c) Maximum value of differential input voltage is

$$2V_{sat} \left( \frac{R_2}{R_1 + R_2} \right) = 2 \times 14 \times \frac{100}{100 + 116} = 12.96 \text{ V}$$

Therefore, the peak values for the differential input voltage just exceed  $\pm 2 \times 6.48 \text{ V}$ .

### **Example 7.4**

Design a square wave oscillator for  $f_o = 1 \text{ kHz}$  using 741 op-amp and DC supply voltage of  $\pm 12 \text{ V}$ .

#### **Solution**

Given frequency of oscillation  $f_o = 1 \text{ kHz}$

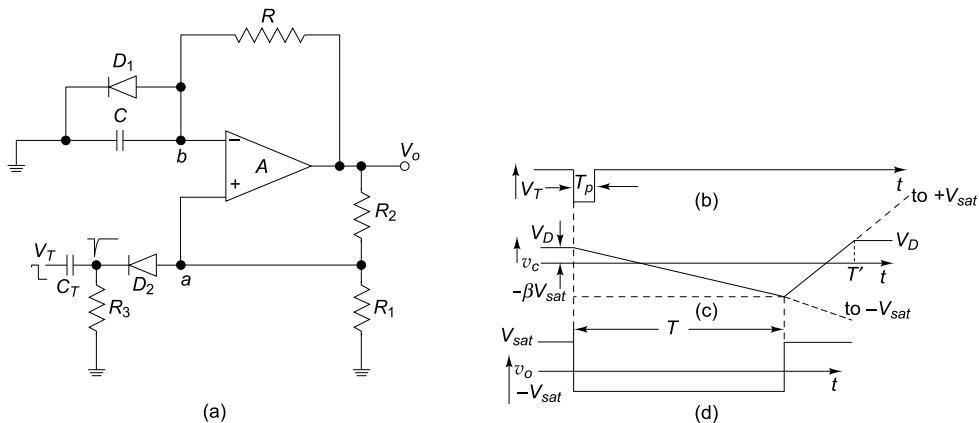
For designing a square wave oscillator, the op-amp based astable multivibrator, shown in Fig. 7.9(a) may be used with the assumption of  $R_1 = R_2 = 10 \text{ k}\Omega$ . Referring to Eq. (7.22), we have

$$f_o = \frac{1}{2.2 RC}$$

Assuming  $C = 0.1 \mu\text{F}$ , we get  $R = \frac{1}{2.2 Cf_o} = \frac{1}{2.2 \times 0.1 \times 10^{-6} \times 1 \times 10^3} = 4.545 \text{ k}\Omega$

### 7.3.2 Monostable Multivibrator

The circuit diagram of a monostable multivibrator, also called a *one-shot* multivibrator is shown in Fig. 7.10(a). This has a stable state and a quasi-stable state. Single output pulse of adjustable time duration in response to a triggering signal can be generated using the monostable multivibrator. The time duration for the output pulse is achieved by connecting the required external components to the op-amp.



**Fig. 7.10** Monostable multivibrator: (a) Circuit diagram (b) Negative polarity triggering signal, (c) Voltage across the capacitor (d) Output voltage waveform

When the output  $V_o$  is at positive saturation, the diode  $D_1$  clamps the capacitor ( $C$ ) voltage to  $V_D$  (0.7 V). This is the stable state of the circuit. In this state, the inverting terminal  $b$  is clamped to ground by diode  $D_1$ . This results in preventing the inverting input terminal going more positive than  $V_D$  (0.7 V). This makes terminal  $a$  also positive by the same voltage  $V_D$ . A negative-going narrow trigger pulse is passed through differentiator  $R_3C_T$  and diode  $D_2$ , and connected to the non-inverting input terminal of op-amp.  $R_3$  is made much larger than  $R_1$ , so that its loading effect may be minimised. The diode  $D_2$  prevents positive spikes arriving from the triggering circuit.

Let us assume that in the stable state, the output  $V_o$  of op-amp is at  $+V_{sat}$ , the voltage at inverting terminal is  $V_D$  and the voltage at (+) terminal through the potential divider  $R_1 - R_2$  is  $+\beta V_{sat}$ , where

$\beta = \frac{R_1}{R_1 + R_2}$ . When a negative trigger signal  $V_T$  is applied to the (+) terminal through the trigger line, the

effective signal is less than 0.7 V. That is, voltage at (+) terminal is  $[\beta V_{sat} + (-V_T)] < 0.7 \text{ V}$ . Then, the op-amp output switches from  $+V_{sat}$  to  $-V_{sat}$ . The diode  $D_1$  is now reverse-biased and the capacitor  $C$  starts charging exponentially to  $-V_{sat}$  through the resistance  $R$  in the closed loop. In this condition, the voltage at positive input terminal is  $-\beta V_{sat}$ .

While charging exponentially, just as the capacitor voltage  $v_c$  becomes slightly more than  $-\beta V_{sat}$ , the voltage at (-) terminal becomes more negative than that at (+) terminal. Then the op-amp output switches back to  $+V_{sat}$ . The capacitor  $C$  now starts charging towards  $+V_{sat}$  through the resistance  $R$ . This continues only until the voltage at (-) terminal becomes  $V_D$  (0.7 V) and then it clamps the capacitor  $C$  to  $V_D$ . The waveforms of the negative polarity triggering signal, voltage across the capacitor and output of op-amp are shown in Fig. 7.10 (b), (c) and (d) respectively.

**To determine the pulse width  $T$**  For a low-pass RC circuit, the general solution is

$$v_o = V_{fin} + (V_{ini} - V_{fin})e^{-t/RC}$$

where  $V_{ini}$  is the initial voltage value and  $V_{fin}$  is the final voltage value. For the circuit explained above,  $V_{fin} = -V_{sat}$  and  $V_{ini} = V_D$  (diode forward voltage)

The output  $v_c$  is then given by,

$$v_c = -V_{sat} + (V_D + V_{sat})e^{-t/RC} \quad (7.23)$$

At the end of time  $t = T$  as shown in Fig. 7.9(c),  $v_c = -\beta V_{sat}$ . Thus,

$$-\beta V_{sat} = -V_{sat} + (V_D + V_{sat})e^{-T/RC}$$

Simplifying for the pulse width, we get

$$T = RC \ln \left( \frac{1 + V_D/V_{sat}}{1 - \beta} \right)$$

where

$$\beta = \frac{R_2}{R_1 + R_2}. \quad (7.24)$$

When  $V_{sat} \gg V_D$  (0.7 V) and  $R_1 = R_2$  with  $\beta = 0.5$ ,

$$T = 0.693 RC \quad (7.25)$$

Understandably, the trigger pulse width should be less than the pulse width  $T$ .

The monostable multivibrator circuit can generate a fast transition after a calculated time  $T$  equal to the pulse width in response to the application of the input trigger pulse. Therefore, it can be used as a time-delay circuit. The rectangular waveform can be used as a gating signal in counters and analog-to-digital converters.

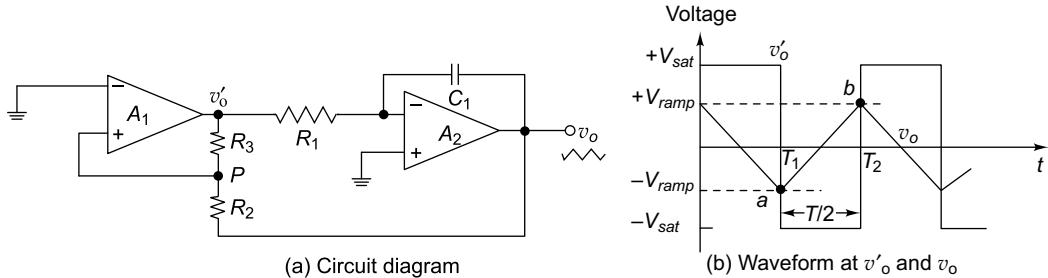
## 7.4 TRIANGULAR WAVE GENERATOR

Figure 7.11(a) shows the circuit of a triangular wave generator. It consists of two op-amps and several passive components. The op-amp  $A_1$  forms a non-inverting comparator with hysteresis, which is a Schmitt Trigger. The op-amp  $A_2$  forms an integrator which integrates the output obtained from the Schmitt trigger. The op-amp  $A_1$  is a two level comparator whose outputs are determined by  $\pm V_{sat}$ . The square-wave output from  $A_1$  is applied to the (-) input terminal of the op-amp  $A_2$ . The output of  $A_2$  is a triangular wave and it is fed back as an input to the comparator  $A_1$  through a voltage divider network formed by  $R_2$  and  $R_3$ .

**Loop analysis** Let us consider that the output  $v'_o$  of comparator  $A_1$  is  $+V_{sat}$  initially. The integrator integrates  $+V_{sat}$  and produces a negative going ramp at its output as shown in Fig. 7.11(b). Hence, the voltages at the two ends of the voltage divider formed by  $R_2 - R_3$  are  $+V_{sat}$  at the output of  $A_1$  and  $-V_{ramp}$  at the output of  $A_2$ . At  $t = T_1$ , when the negative going ramp reaches a value of  $-V_{ramp}$ ,

represented as point *a* in Fig. 7.11(b), the effective value at the point *P* becomes slightly less than 0 V. This switches the op-amp  $A_1$  to its negative saturation level  $-V_{sat}$ .

With the output of  $A_1$  at  $-V_{sat}$ , the op-amp  $A_2$  starts integrating and increases its output in the positive direction. At  $t = T_2$ , shown as point *b* in Fig. 7.11(b), the voltage at *P* becomes just more than 0 V. This switches the output of op-amp  $A_1$  from  $-V_{sat}$  to  $+V_{sat}$ . This cycle repeats itself, and generates a triangular waveform. The frequency of the waveform is determined by the  $RC$  value of the integrator formed by op-amp  $A_2$  and the saturation voltage levels  $\pm V_{sat}$  of comparator op-amp  $A_1$ .



**Fig. 7.11** Triangular waveform generator: (a) Circuit diagram  
(b) Waveforms at  $v'_o$  and  $v_o$

**To determine the amplitude and frequency of the triangular waveform** When the comparator output is at  $+V_{sat}$ , the effective voltage at the point *P* is

$$-V_{ramp} + \frac{R_2}{R_2 + R_3} [ +V_{sat} - (-V_{ramp}) ] = 0$$

Simplifying, we get

$$-V_{ramp} = \frac{-R_2}{R_3} (+V_{sat})$$

Similarly, at  $t = T_2$ , when the output of  $A_1$  switches from  $-V_{sat}$  to  $+V_{sat}$ ,

$$V_{ramp} = \frac{-R_2}{R_3} (-V_{sat}) = \frac{R_2}{R_3} V_{sat} \quad (7.26)$$

Thus the peak-to-peak amplitude of the triangular wave is

$$v_{o(pp)} = +V_{ramp} - (-V_{ramp}) = 2 \frac{R_2}{R_3} V_{sat} \quad (7.27)$$

The time taken for the output of  $A_2$  to switch from  $-V_{ramp}$  to  $+V_{ramp}$  is half of the time period, i.e.  $T/2$ . From the basic integrator output equation,

$$v_o = - \frac{1}{R_1 C_1} \int_0^{T/2} (-V_{sat}) dt = \frac{V_{sat}}{R_1 C_1} \left( \frac{T}{2} \right)$$

Then,

$$T = 2 \frac{R_1 C_1 v_{o(pp)}}{V_{sat}}$$

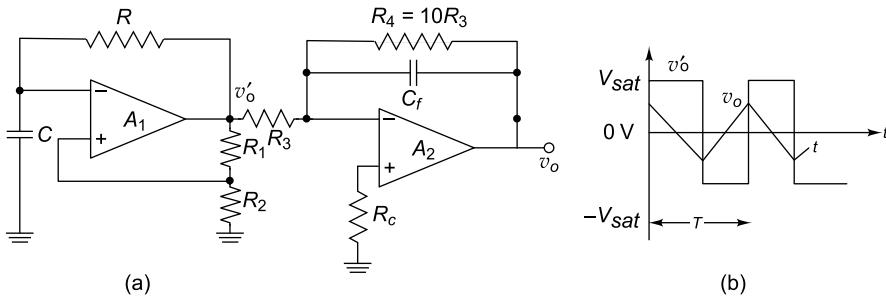
Substituting the value of  $v_{o(pp)}$  from Eq. (7.27) in the above equation, we get

$$T = \frac{4R_1C_1R_2}{R_3} \quad (7.28)$$

Therefore, the frequency of oscillation is

$$f_o = \frac{1}{T} = \frac{R_3}{4R_1C_1R_2} \quad (7.29)$$

A triangular waveform generator can also be constructed by a simple alternate arrangement of a square-wave generator connected to an integrator as shown in Fig. 7.12(a).



**Fig. 7.12** Alternate triangular waveform generator circuit: (a) Circuit diagram  
(b) Waveforms at the output of op-amps

Let us assume that the voltage  $v'_0$  is high at  $+V_{\text{sat}}$ . This forces a current of  $+V_{\text{sat}}/R_3$  through capacitor  $C_f$  of the integrator, producing a negative ramp at the output of the integrator. When  $v'_0$  is low at voltage  $-V_{\text{sat}}$ , the output of integrator ramps up linearly. This cycle repeats itself and hence the frequency of the triangular wave is the same as that of the square-wave. Hence, the value of resistor  $R$  connected in the square-wave generator part of the circuit determines the frequency of the triangular wave. The amplitude of the triangular wave decreases with an increase in frequency value. This is due to the fact that the capacitive reactance decreases at high frequencies and increases at low frequencies. The square waveform and triangular waveform of the circuit are shown in Fig. 7.12(b).

A stable triangular wave can be obtained by maintaining  $5R_3C_2 > T/2$ , where  $T$  is the period of the square-wave input. A resistance  $R_4$  is normally connected across  $C_f$  to avoid saturation problems occurring at low frequencies.

### Example 7.5

Assume that for the circuit shown in Fig. 7.11(a),  $R_1 = 100 \text{ k}\Omega$ ,  $R_2 = 10 \text{ k}\Omega$ ,  $R_3 = 20 \text{ k}\Omega$ ,  $C_1 = 0.01 \mu\text{F}$  and  $\pm V_{\text{sat}} = \pm 14 \text{ V}$  for the op-amps. Determine the (a) period, (b) frequency, (c) peak value of square-wave and (d) peak value of triangular wave.

### Solution

(a) From Eq. (7.28),

$$\text{Time period, } T = \frac{4R_1C_1R_2}{R_3}$$

$$= \frac{4(100 \times 10^3)(0.01 \times 10^{-6})(10 \times 10^3)}{20 \times 10^3} = 2 \text{ ms}$$

(b) Frequency  $f_o = \frac{1}{T} = \frac{1}{2 \times 10^{-3}} = 500 \text{ Hz}$

(c) The peak value of the op-amp is simply the saturation voltage levels, i.e. +14V and -14V.

(d) Peak value of the triangular wave from Eq. (7.26) is

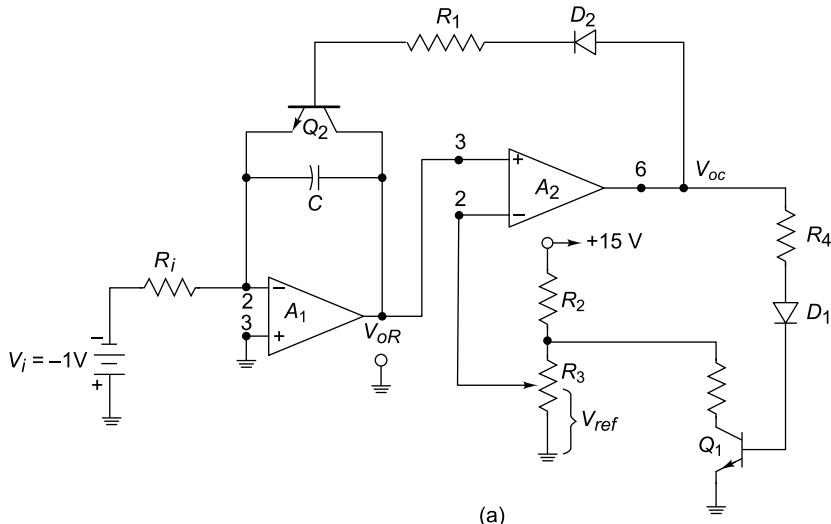
$$V_p = \frac{R_2}{R_3} V_{sat} = \frac{10 \times 10^3}{20 \times 10^3} \times 14 = 7 \text{ V}$$

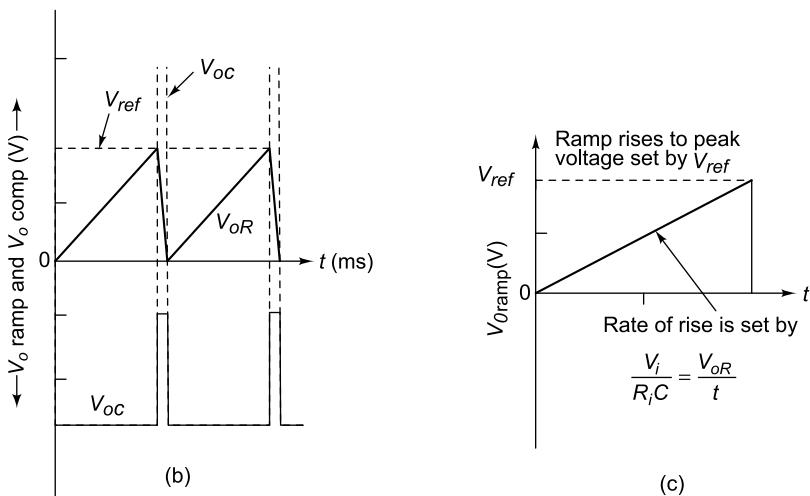
Therefore, the triangular wave oscillates between +7 V and -7 V.

## 7.5 SAWTOOTH WAVE GENERATOR

The sawtooth wave refers to a waveform with its rise time being many times longer than the corresponding fall time or fall time very longer as compared to the rise time. Triangular wave generator can be modified to produce a sawtooth waveform.

The sawtooth wave generator circuit is shown in Fig. 7.13(a). The op-amp  $A_1$  functions as a ramp generator and the op-amp  $A_2$  function as a comparator. The input reference signal  $V_i$  of value less than zero is connected to the inverting input of the op-amp. Since  $V_i$  is negative, the output of op-amp  $A_1$  can only ramp up. The rate of raise is given by  $\frac{V_{oR}}{t} = \frac{V_i}{R_i C}$ . The ramp voltage  $V_{oR}$  is monitored by the comparator  $A_2$ . The output  $V_{oR}$  is connected to the non-inverting terminal of op-amp  $A_2$ , and a reference voltage set by a potentiometer  $V_{ref}$  is connected to the inverting input of comparator. When the capacitor  $C$  charges, and when the voltage  $V_{oR}$  is below  $V_{ref}$ , the output of comparator is negative. Then the transistors  $Q_1$  and  $Q_2$  do not conduct. The diodes  $D_1$  and  $D_2$  protect the transistors from excessive reverse bias voltages.





**Fig. 7.13** Sawtooth wave generator: (a) Circuit Diagram (b) Sawtooth wave and comparator outputs (c) Sawtooth wave design

When  $V_{oR}$  rises and just exceeds  $V_{ref}$ , the output  $V_{oc}$  of comparator goes to positive saturation. This action forward biases the transistor  $Q_2$  into saturation. The saturated transistor then acts as a switch across the capacitor  $C$ , which discharges quickly making the output  $V_{oc}$  come down essentially to 0 V. The positive saturation  $V_{oc}$  of  $A_2$  also makes the transistor  $Q_1$  ON, and the  $V_{ref}$  or negative input of op-amp  $A_2$  drops to 0 V. As the capacitor  $C$  discharges rapidly making  $V_{oR}$  zero volts, it drops below  $V_{ref}$ . This causes the comparator output to become negatively saturated. This action switches the transistor  $Q_2$  OFF and  $C$  begins charging linearly and the cycle repeats.

**Frequency of oscillation** The charging time  $T_c$  is obtained from period  $T = \frac{V_{ref}}{V_i/R_i C}$ . The frequency is the reciprocal of the time period. Therefore,

$$f = \frac{1}{T} = \left( \frac{1}{R_i C} \right) \frac{V_i}{V_{ref}}$$

The sawtooth output waveform is shown in Fig. 7.13(b). Figure 7.13(c) shows the sawtooth wave designing method. The circuit can also be operated as a current-controlled sawtooth wave generator by applying an external control current sink  $I_s$  at the (–) input terminal of op-amp  $A_1$  of Fig. 7.13(a). Then,

$$f = \frac{I_s}{C V_{ref}}.$$

Here, the op-amp  $A_1$  can preferably be a FET input op-amp with low bias current and good slew rate.

### Example 7.6

Design a sawtooth wave generator for 10V peak and frequency of 200 Hz. Assume  $V_i = 2V$  and  $V_{ref} = 10V$ .

#### Solution

The ramp signal rises at a rate of 2 V/ms. Therefore, choose a time constant of  $R_i C$  to produce a time period of 1.0 ms

We know that

$$f = \left( \frac{1}{R_i C} \right) \frac{V_i}{V_{ref}}.$$

Let

$$C = 0.1 \mu\text{F}.$$

Therefore,

$$R_i = \frac{1}{200(0.1 \times 10^{-6})} \left( \frac{2}{10} \right) = 10 \text{ k}\Omega$$

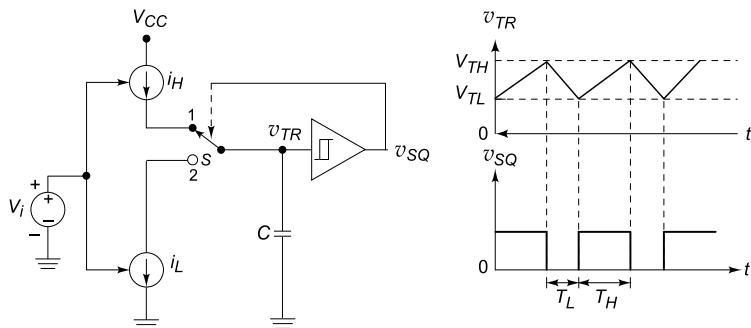
Here,  $V_i$  can be derived from an ideal voltage source.

## 7.6 ICL8038 FUNCTION GENERATOR

The ICL8038 waveform generator is a monolithic integrated circuit which is capable of producing sine, square, triangular, sawtooth and pulse waveforms of high accuracy with a minimum number of external components. It is fabricated through advanced monolithic fabrication technology employing Schottky barrier diodes and thin film resistors. The output voltage is stable over a wide range of temperature and operating supply voltage values.

### 7.6.1 Functional Block Diagram of ICL8038

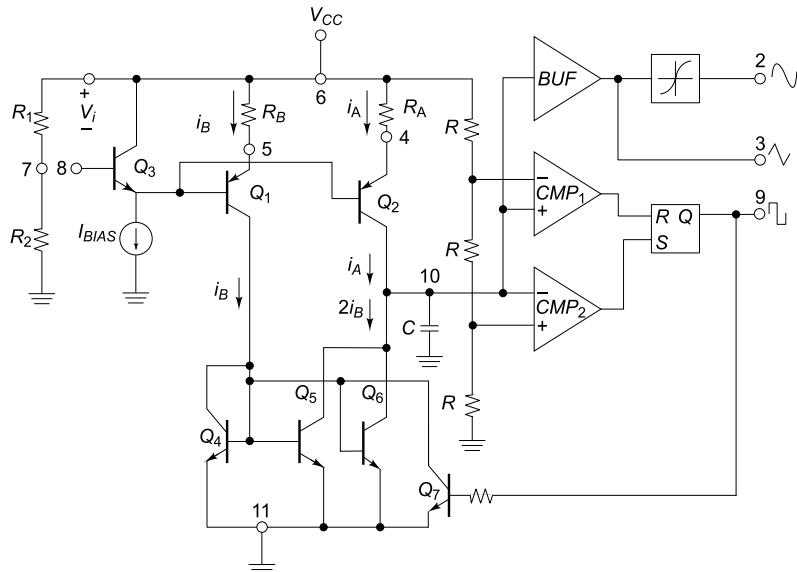
The main part of waveform generator is a VCO, that generates the triangular and square-waves. Sine-wave is generated from triangular wave by passing the later through an on-chip wave shaper. Sawtooth and pulse waveforms are obtained by the use of highly asymmetric duty cycle for the oscillator. The most common VCO circuit configurations are *grounded capacitor* and emitter coupled types. The *grounded capacitor* arrangement is used in the waveform generator ICL8038. The principle of operation of a *grounded capacitor* type VCO is shown in Fig. 7.14(a). When switch  $S$  is in position 1, the capacitor  $C$  charges at a rate fixed by the current source  $i_H$ . When voltage  $v_{TR}$  across capacitor reaches the upper threshold of Schmitt trigger, it changes state and flips the switch  $S$  to position 2. The capacitor  $C$  now discharges through the current sink  $i_L$ . When  $v_{TR}$  reaches the lower threshold level of Schmitt trigger, it triggers flipping the switch  $S$  to position 1. This sequence produces the waveforms shown in Fig. 7.14(b). The current source  $i_H$  and current sink  $i_L$  can be made programmable through the control voltage  $V_i$ .



**Fig. 7.14** Grounded-capacitor type of VCO: (a) Circuit arrangement (b) Waveforms

The circuit diagram of ICL8038 is shown in Fig. 7.15. The transistors  $Q_1$  and  $Q_2$  are two programmable current sources. The magnitudes of current are set by  $R_A$  and  $R_B$ . The emitter follower formed by the transistor  $Q_3$  drives the base of  $Q_1$  and  $Q_2$ . As shown in Fig. 7.15,  $i_A = \frac{V_i}{R_A}$  and  $i_B = \frac{V_i}{R_B}$ . The current  $i_A$  is fed to  $C$  directly and current  $i_B$  is sent to the current mirror formed by the transistors  $Q_4$ ,  $Q_5$ , and  $Q_6$ . Hence the transistors  $Q_5$  and  $Q_6$  produce a total sink current of  $2i_B$  due to their parallel arrangement.

Schmitt trigger circuit is formed by the comparators  $CMP_1$  and  $CMP_2$  in combination with the flip-flop. The threshold voltage levels are  $V_{TL} = \frac{1}{3} V_{CC}$  and  $V_{TH} = \frac{2}{3} V_{CC}$ . This is achieved by the potential divider arrangement consisting of three resistances of equal value  $R$ .



**Fig. 7.15** Functional circuit diagram of ICL8038 waveform generator

Assume that the output  $Q$  of the flip-flop is initially high. This saturates transistor  $Q_7$  and it pulls the bases of  $Q_5$  and  $Q_6$  low, shutting the current sink OFF. Therefore,  $C$  charges up at a rate determined by  $i_H = i_A$ . When the capacitor voltage reaches  $V_{TH}$ , the  $CMP_1$  triggers, resetting the output  $Q$ . This turns  $Q_7$  OFF and this action enables the current mirror. The current through  $C$  is now  $i_c = 2i_B - i_A$ . When  $2i_B > i_A$ , the capacitor continues to discharge and once  $V_{TL}$  is reached,  $CMP_2$  triggers and it sets the flip-flop, thus repeating the cycle.

The frequency  $f_o$  is given by

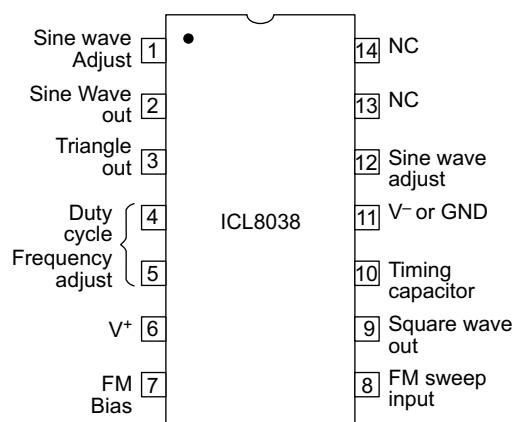
$$f_o = 3 \left( 1 - \frac{R_B}{2R_A} \right) \frac{V_i}{R_A C V_{CC}}$$

$$\text{and duty cycle } D = \left( 1 - \frac{R_B}{2R_A} \right) 100\% .$$

When  $R_A = R_B = R$ ,

$$f_o = KV_i, \quad \text{where } K = \frac{1.5}{RCV_{CC}} \quad (7.30)$$

The sine-wave is obtained by use of a wave shaper which converts the triangular wave to a sine-wave. The buffer isolates the waveform developed across  $C$ . The pin diagram of ICL8038 is shown in Fig. 7.16.



**Fig. 7.16** Pin diagram of ICL8038

### The important specifications of ICL8038 are as follows:

Supply voltage	- $\pm 18V$ or $36V$
Power dissipation	- $750\text{ mW}$
Input voltage	- max of supply voltage level
Input current (at pins 4 and 5)	- $25\text{ mA}$
Output sink current (pins 3 and 9)	- $25\text{ mA}$
Storage temperature range	- $65^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
Low frequency drift with temperature	- $50\text{ ppm}/^{\circ}\text{C}$
Distortion	- 1 % (for sine-wave output)
Linearity	- 0.1 % (for triangular wave output)
Operating frequency range	- 0.001 Hz to 300 kHz.
Duty cycle	- 2% to 98%

### 7.6.2 Basic ICL8038 Application

The basic connection diagram for obtaining 50% duty cycle operation is shown in Fig. 7.17. The control voltage  $V_i$  is derived from the supply voltage  $V_{CC}$  through the internal voltage divider  $R_1$  and  $R_2$  (Refer to Fig. 7.15). Hence from

$$\text{Eq. (7.30), } V_i = \frac{1}{5} V_{CC} \text{ and } f_o = \frac{0.3}{RC}. \text{ Here, the duty cycle } D = 50\%.$$

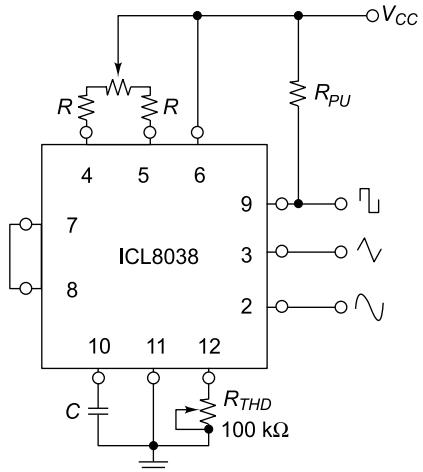
It can be noted that  $f_o$  is independent of supply voltage  $V_{CC}$ . The selection of external components  $R$  and  $C$  enables oscillation of any desired frequency. The frequency range is 0.001 Hz to 1 MHz and the thermal drift of  $f_o$  is typically  $50\text{ ppm}/^{\circ}\text{C}$ . The resistance  $R_{PU}$  acts as the pull-up resistor for the square-wave output. The waveform generator can be operated either from a single power supply (10 to 30V) or a dual power supply ( $\pm 5$  to  $\pm 15V$ ).

With a single power supply, the peak-to-peak amplitudes of square, triangular and sinusoidal waves are  $V_{CC}$ ,  $0.33V_{CC}$  and  $0.22V_{CC}$  respectively. The amplitudes of the waveforms are centered at  $V_{CC}/2$ . Automatic frequency sweep can also be achieved by varying the voltage at pin 8.

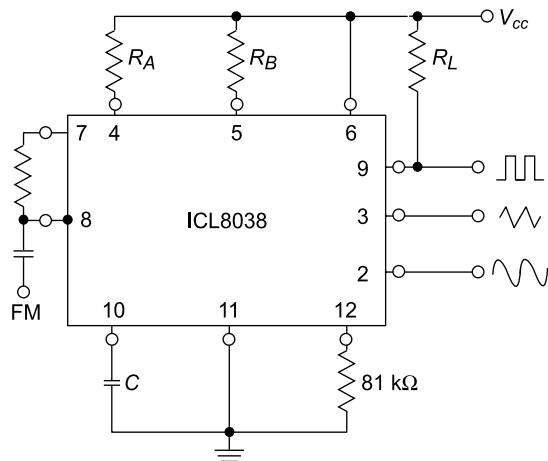
### 7.6.3 Frequency Modulation using ICL8038

The ICL8038 can be used for frequency modulation. The modulating signal voltage is applied at pin 8. The frequency of the waveform generator is then a direct function of the voltage at terminal 8. Frequency modulation is performed by varying the voltage at pin 8. Figures 7.18(a) and (b) show two arrangements of achieving FM modulation using ICL8038.

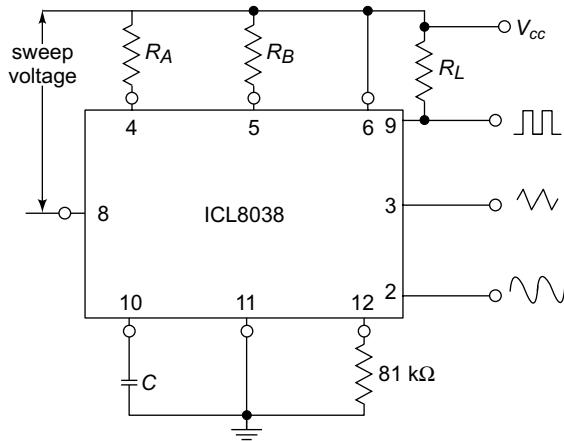
Figure 7.18(a) shows the circuit arrangement for frequency modulating signals of small deviations, e.g.  $\pm 10\%$ . The modulating signal is then directly connected to pin 8 through a dc decoupling capacitor. The resistance  $R$  is used to increase the input impedance by the value of  $R$ .



**Fig. 7.17** Basic ICL8038 connection diagram for 50% duty cycle, fixed frequency operation



**Fig. 7.18 (a)** Frequency modulation for small FM deviations



**Fig. 7.18 (b)** Frequency modulation for larger FM deviations

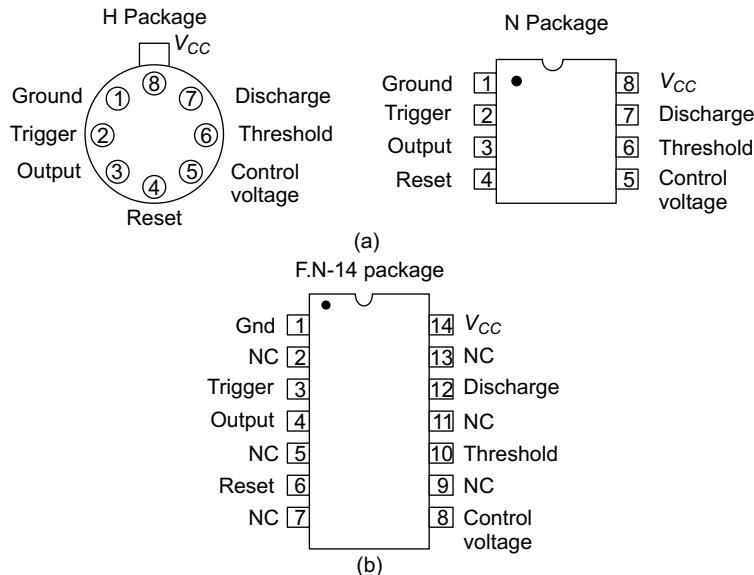
Figure 7.18(b) is used for larger deviations of FM or for frequency sweeping. The sweep voltage or the modulating signal is applied between the positive supply terminal and pin 8. Hence, the effective bias for the current source is created by the modulating signal. A very large sweep (e.g. 1000:1) can be created in this arrangement and value of  $f$  is zero at  $V_{sweep} = 0$ . It is to be noted that the charging current is a function of the modulating sweep signal and the trigger thresholds are functions of the supply voltage. The potential at pin 8 may span from  $+V_{CC}$  down to  $\left(\frac{1}{3}V_{CC} - 2V\right)$ .

$$\text{at pin 8 may span from } +V_{CC} \text{ down to } \left(\frac{1}{3}V_{CC} - 2V\right).$$

## 7.7 TIMER IC 555

The 555 integrated circuit timer was first introduced by Signetics Corporation as Type SE555/NE555. It is available in 8-pin circular style TO-99 Can, 8-pin mini-DIP and 14-pin DIP as shown in Fig. 7.19. The

555 IC is widely popular and various manufacturers provide the IC. The IC 556 contains two 555 timers in a 14-pin DIP package and Exar's XR-2240 contains a 555 timer with a programmable binary counter in a single 16-pin package.



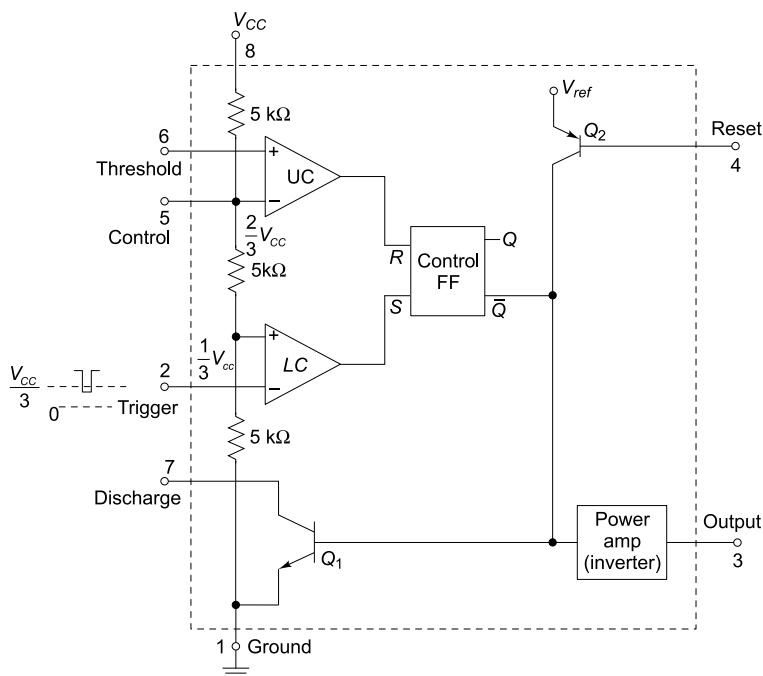
**Fig. 7.19** Pin configurations of IC 555 Timer

The 555 timer can be operated with a dc supply voltage ranging from +5V to +18V. This feature makes the IC compatible to TTL/CMOS logic circuits and op-amp based circuits. The IC 555 timer is very versatile and its applications include oscillator, pulse generator, square and ramp wave generator, *one-shot* multivibrator, safety alarm and timer circuits, traffic light controllers, etc. The 555 timer can provide time delay, ranging from microseconds to hours.

### 7.7.1 General Description of the IC 555

Figure 7.20 shows the functional block diagram of 555 IC timer. The positive dc power supply terminal is connected to pin 8( $V_{CC}$ ) and negative terminal is connected to pin 1(Gnd). The ground pin acts as a common ground for all voltage references while using the IC. The *output* (pin 3) can assume a HIGH level (typically 0.5V less than  $V_{CC}$ ) or a LOW level (approximately 0.1V).

Two comparators, namely, upper comparator (UC) and lower comparator (LC) are used in the circuit. Three  $5\text{ k}\Omega$  internal resistors provide a potential divider arrangement. It provides a voltage of  $(2/3)V_{CC}$  to the (-) terminal of the upper comparator and  $(1/3)V_{CC}$  to the (+) input terminal of the lower comparator. A *control* voltage input terminal (pin 5) accepts a modulation control input voltage applied externally. Pin 5 is connected to ground through a bypassing capacitor of  $0.1\text{ }\mu\text{F}$ . It bypasses the noise or ripple from the supply. The (+) input terminal of the UC is called the *threshold terminal* (pin 6) and the (-) input terminal of the LC is the *trigger terminal* (pin 2). The operation of the IC can be summarised as shown in Table 7.1.

**Fig. 7.20** Functional block diagram of IC 555 Timer**Table 7.1** States of operation of IC 555

<b>Sl. No.</b>	<b>Trigger (pin 2)</b>	<b>Threshold (pin 6)</b>	<b>Output state (pin 3)</b>	<b>Discharge state (pin 7)</b>
1	Below $(1/3)V_{CC}$	Below $(2/3)V_{CC}$	High	Open
2	Below $(1/3)V_{CC}$	Above $(2/3)V_{CC}$	Last state remains	Last state remains
3	Above $(1/3)V_{CC}$	Below $(2/3)V_{CC}$	Last state remains	Last state remains
4	Above $(1/3)V_{CC}$	Above $(2/3)V_{CC}$	Low	Ground

The standby (stable) state makes the output  $\bar{Q}$  of flip-flop (FF) HIGH. This makes the output of inverting power amplifier LOW. When a negative going trigger pulse is applied to pin 2, as the negative edge of the trigger passes through  $\frac{1}{3}(V_{CC})$ , the output of the lower comparator becomes HIGH and it sets the control FF making  $Q = 1$  and  $\bar{Q} = 0$ . When the threshold voltage at pin 6 exceeds  $\frac{2}{3}(V_{CC})$ , the output of upper comparator goes HIGH. This action resets the control FF with  $Q = 0$  and  $\bar{Q} = 1$ .

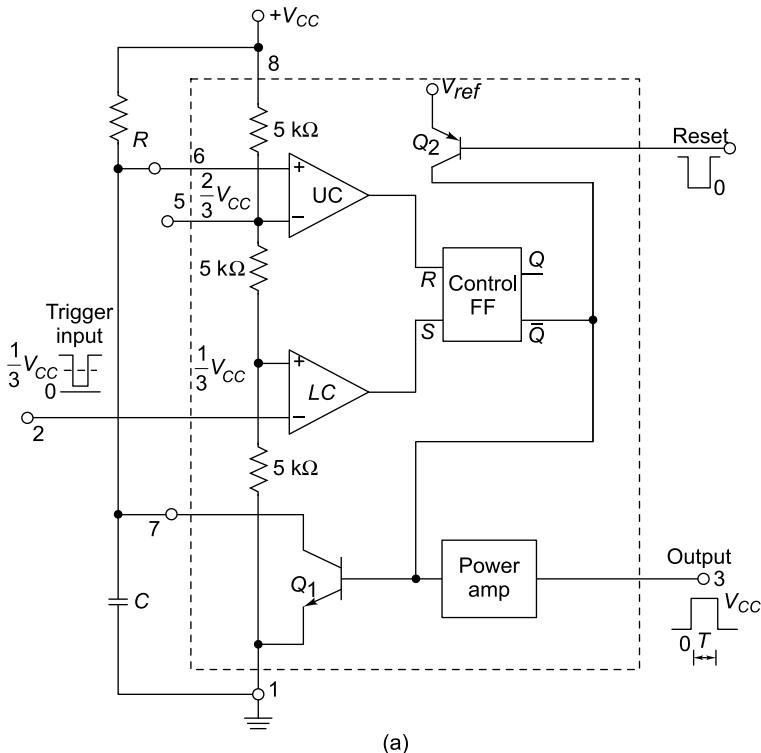
The *reset* terminal (pin 4) allows the resetting of the timer by grounding the pin 4 or reducing its voltage level below 0.4 V. This makes the *output* (pin 3) low overriding the operation of lower comparator. When not used, the *reset* terminal is connected to  $V_{CC}$ . Transistor  $Q_2$  isolates the reset input from the FF and transistor  $Q_1$ . The reference voltage  $V_{ref}$  is made available internally from  $V_{CC}$ . Transistor  $Q_1$  acts as a *discharge* transistor. When *output* (pin 3) is high,  $Q_1$  is OFF making the *discharge* terminal (pin 7) *open*. When the output is low,  $Q_1$  is forward-biased to ON condition. Then, the *Discharge* terminal appears as a short circuit to ground.

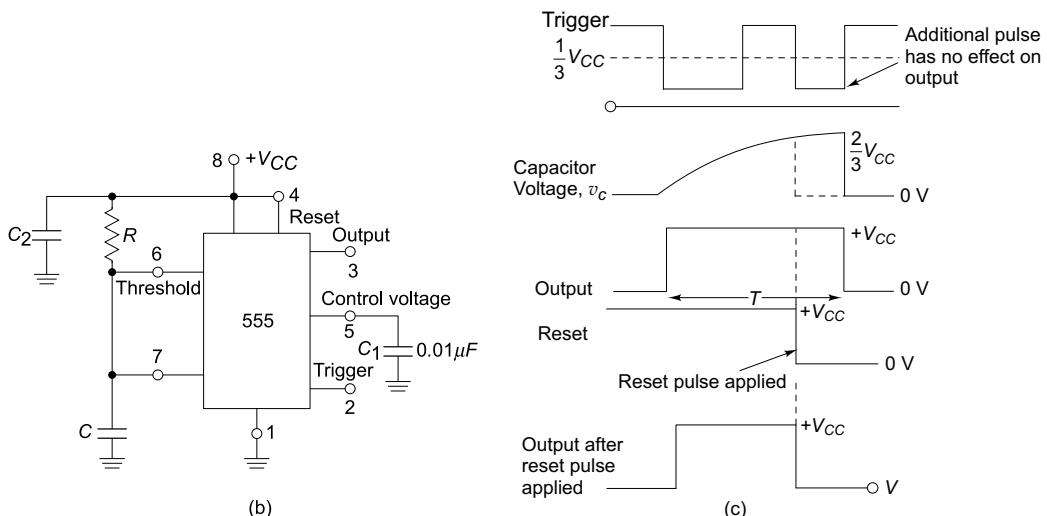
### 7.7.2 Monostable Operation of Timer IC 555

Monostable multivibrator has one stable state and one quasi-stable state. It is also known as *monoshot* or *one-shot* multivibrator or *uni-vibrator*. It remains in its stable state until an input pulse triggers it into its quasi-stable state. It stays in quasi-stable state for a time duration determined by an *RC* timing circuit. The output returns to its original stable state automatically at the end of the time and stays there until the next trigger pulse is applied. Therefore, a monostable multivibrator cannot generate square-waves on its own like an astable multivibrator. Only external trigger pulses will cause it to generate the rectangular pulses.

The functional block diagram and connection diagram of a monostable multivibrator using 555 timer is shown in Fig. 7.21(a) and (b) respectively. In the standby mode, the control flip-flop FF holds  $Q_1$  ON, thus clamping the external timing capacitor  $C$  to ground. The output (pin 3) during this time is at ground potential, or LOW. The three  $5\text{ k}\Omega$  internal resistors act as voltage dividers providing bias voltages of  $(2/3)V_{CC}$  and  $(1/3)V_{CC}$  respectively. Since these two voltages fix the necessary comparator threshold voltages, they aid in determining the timing interval.

The lower comparator (LC) is biased at  $(1/3)V_{CC}$  and it remains in the standby state as long as the trigger (pin 2) input is held above  $(1/3)V_{CC}$ . When triggered by a negative going pulse, the output of the lower comparator goes HIGH setting the flip-flop FF with  $Q = 1$  and  $\bar{Q} = 0$ . This turns the transistor  $Q_1$  OFF, and the output goes HIGH (approximately equal to  $V_{CC}$ ). Since the timing capacitor is now unclamped, the voltage across it now rises exponentially through  $R$  towards  $V_{CC}$  with a time constant  $RC$ . After a period of time, the capacitor voltage will equal  $(2/3)V_{CC}$  and the upper comparator (UC) resets the internal flip-flop. This makes  $\bar{Q} = 1$  and the transistor  $Q_1$  is ON. This in turn discharges the capacitor rapidly to ground potential. As a consequence, the output now returns to the standby state or ground.





**Fig. 7.21** Monostable multivibrator: (a) Functional diagram (b) Connection diagram (c) Timing pulses

The timing sequence of 555 monostable multivibrator is shown in Fig. 7.21(c). The circuit triggers only on a negative going pulse, when the level is less than  $(1/3)V_{CC}$ . Once triggered, the output will remain HIGH until the set time has elapsed, even if it is triggered again during this interval which is indicated in Fig. 7.21(c). Since the external capacitor voltage charges exponentially from 0 to  $(2/3)V_{CC}$ , the voltage across the capacitor  $v_c$  is given by

$$v_c = V_{CC}(1 - e^{-t/RC}) \quad (7.31)$$

At time  $t = T$ ,

$$v_c = (2/3)V_{CC}$$

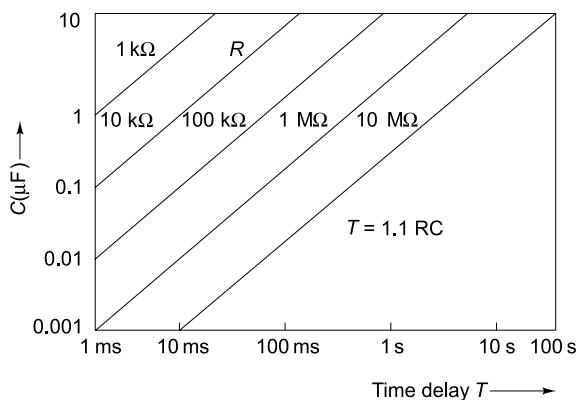
That is,

$$\frac{2}{3}V_{CC} = V_{CC}(1 - e^{-T/RC})$$

Therefore,  $T = -RC \ln\left(\frac{1}{3}\right) = 1.1 RC$  (seconds) (7.32)

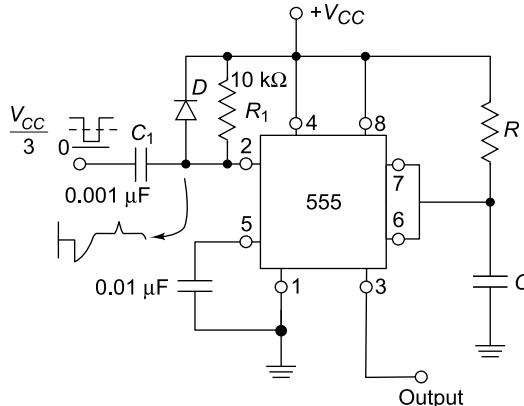
Figure 7.22 shows a graph of various combinations of  $R$  and  $C$  necessary to produce a given time delay. Since the charging rate and comparator thresholds are both directly proportional to the supply voltage, the timing interval given by Eq. (7.32) is independent of the supply voltage.

For proper monostable operation with the 555 timer, the negative-going trigger pulse width should be kept shorter compared to the desired output pulse width. The values of external timing resistor and capacitor can be determined either from Eq. (7.32) or from the graph given in Fig. 7.22.



**Fig. 7.22** Graph of  $RC$  combinations for different time delays

To prevent mistriggering on positive pulse edges, an  $R_1-C_1$  combination with a diode  $D$  can be connected between pin 2 and pin 8 as shown in Fig. 7.23. The value of  $R_1$  and  $C_1$  should be such that  $R_1C_1$  is smaller than the required pulse width. During the positive edge of the trigger pulse, the diode  $D$  gets forward-biased and it limits the amplitude of the positive spike to 0.7 V, which is less than  $(1/3)V_{CC}$  to trigger the lower comparator  $LC$  ON.



**Fig. 7.23** Waveshaping circuit to avoid positive pulse triggering

### Example 7.7

Design a monostable multivibrator using 555 timer for a pulse period of 1 ms.

#### Solution

The period of pulse is  $t = 1.1 RC$

Letting  $C = 0.1 \mu\text{F}$ ,

$$1 \times 10^{-3} = 1.1 \times 10^{-7} R$$

Therefore,  $R = 8.2 \text{ k}\Omega$

### 7.7.3 Applications of Monostable Multivibrator

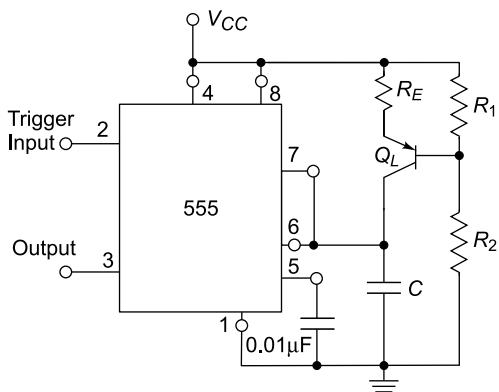
The important applications of monostable multivibrator are: (i) Ramp generation, (ii) Frequency division and (iii) Pulse-width modulation.

**Ramp generation** Linear ramp signal can be generated using the circuit shown in Fig. 7.24(a). The timing capacitor  $C$  is charged by constant current source instead of charging by a resistor. The transistor  $Q_L$  forms a constant current source. Assuming that  $i$  is the current supplied by a constant current source, the capacitor voltage  $v_c$  is given by

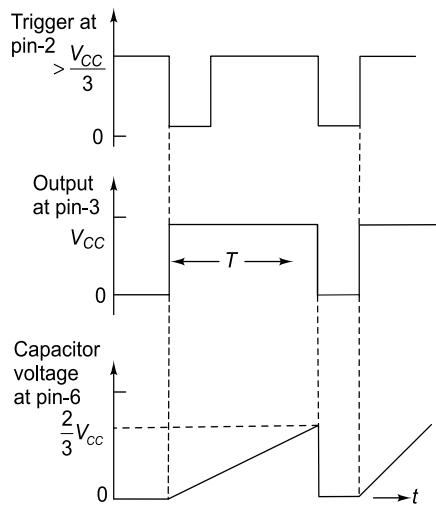
$$v_c = \frac{1}{C} \int_0^t idt \quad (7.33)$$

Referring to Fig. 7.24(a) and employing KVL,

$$\begin{aligned} \frac{R_1}{R_1 + R_2} V_{CC} - V_{BE} &= (\beta + 1) I_B R_E \\ \beta I_B R_E &= I_C R_E = i R_E \end{aligned} \quad (7.34)$$



(a)



(b)

where  $I_B$  and  $I_C$  are the base and collector currents of transistor  $O_L$  and  $\beta$  is the current gain in CE mode.

From Eq. (7.34),

$$i = \frac{R_1 V_{CC} - V_{BE} (R_1 + R_2)}{R_E (R_1 + R_2)} \quad (7.35)$$

Substituting Eq. (7.35) in Eq. (7.33), we get

$$v_c = \frac{1}{C} \int_0^t \frac{R_l V_{CC} - V_{BE} (R_l + R_2)}{R_E (R_l + R_2)} dt$$

Therefore,

$$v_c = \frac{R_l V_{CC} - V_{BE} (R_l + R_2)}{CR_F (R_l + R_2)} \times t \quad (7.36)$$

At the instant of time  $t = T$ ,  $v_c$  becomes  $(2/3)V_{CC}$ . Then,

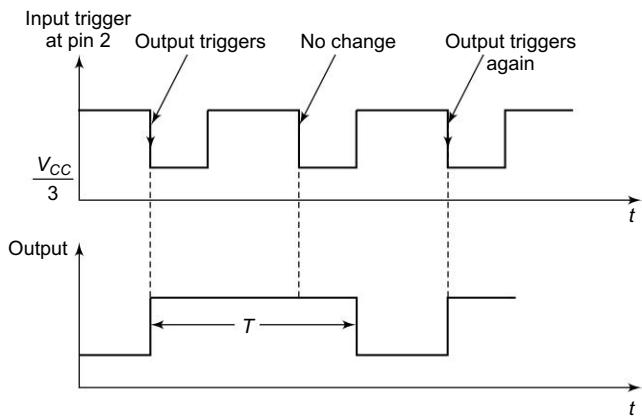
$$(2/3)V_{CC} = \frac{R_1 V_{CC} - V_{BE}(R_1 + R_2)}{CR_E(R_1 + R_2)} \times T$$

That is, the time period  $T$  of linear ramp generator is given by

$$T = \frac{(2/3)V_{CC}CR_E(R_1 + R_2)}{R_1V_{CC} - V_{BE}(R_1 + R_2)} \quad (7.37)$$

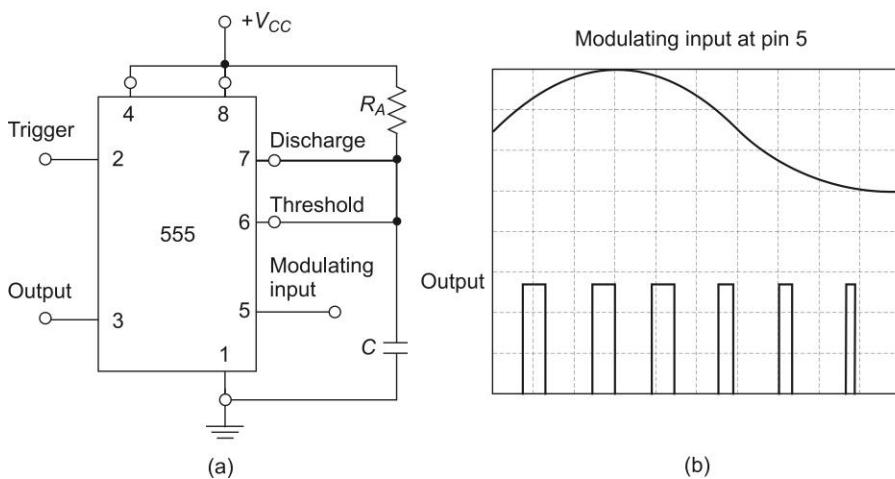
When the capacitor voltage  $v_c$  just goes above  $(2/3)V_{CC}$  the upper comparator triggers, thereby resetting the flip-flop. This discharges the capacitor  $C$ , and the output remains at zero until another trigger pulse is applied. The various waveforms of the circuit are shown in Fig. 7.24(b).

**Frequency divider** The monostable multivibrator, when continuously triggered by a square-wave signal can be used as a frequency divider, if the timing interval  $T$  of the monostable multivibrator is designed to be longer than the period of the triggering square-wave signal. The one-shot is triggered by the first negative edge of the square-wave input. During the second negative edge of the square-wave, the output of monostable multivibrator remains HIGH. However, during the third negative edge of the square-wave signal, the mono-shot once again triggers ON. In this manner, the output pulse can be made any integral fraction of the input triggering square-wave signal. The waveform of the input square-wave and output of monoshot are shown in Fig. 7.25 for a frequency divided-by-two operation.



**Fig. 7.25** The input and output waveforms of frequency divider circuit

**Pulse-width modulation** The monostable multivibrator, when applied with a *modulating control* input signal at pin 5 can act as a pulse width modulator. The circuit of the mono-shot with modulating input signal at pin 5 is shown in Fig. 7.26(a). The series of trigger pulses at pin 2 generates a series of output pulses. The duration of the output pulses are determined by the triggering of the upper comparator, which in turn depends on the modulating signal input at pin 5. This is due to the fact that, the modulating signal is superimposed upon the voltage  $(2/3)V_{CC}$  obtained through voltage divider circuit. The threshold level of the upper comparator thus changes and the output pulse modulation occurs. The modulating control input signal and the output waveforms are shown in Fig. 7.26(b).

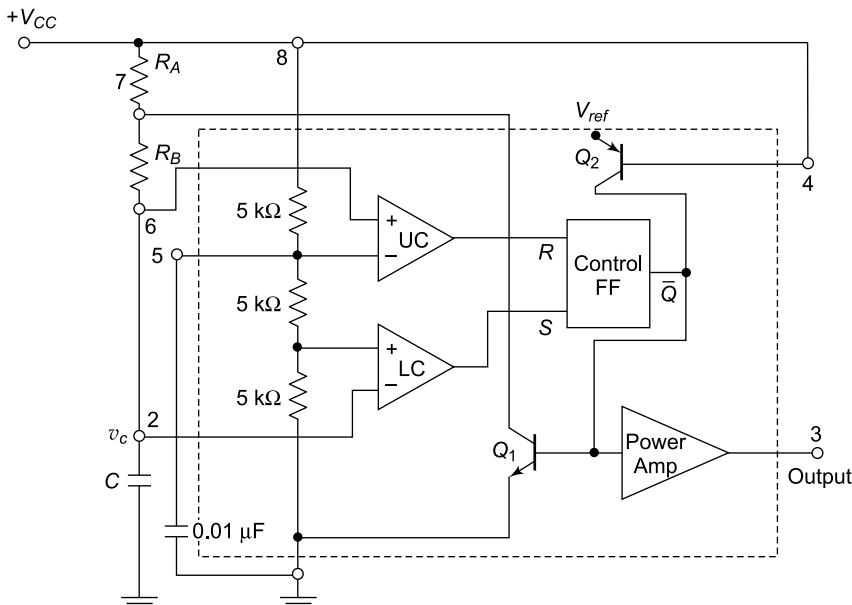


**Fig. 7.26** Pulse width modulator using monostable multivibrator: (a) Circuit diagram  
(b) Input and output waveforms

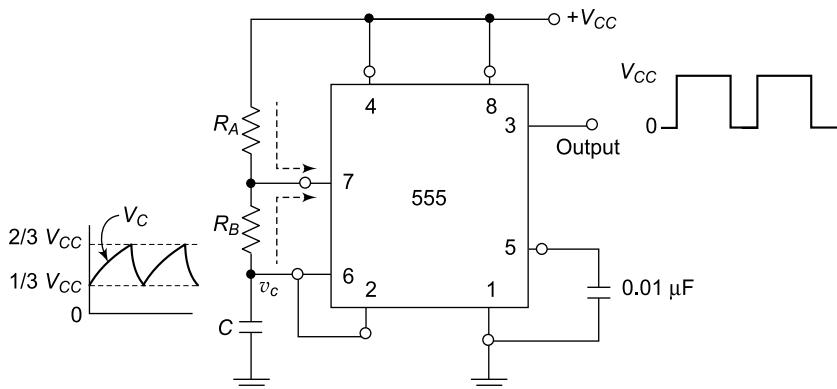
It can be seen that, the frequency of the output remains the same, with the duty cycle of the output varying in response to the modulating input.

### 7.7.4 Astable Operation of the Timer IC 555

The functional diagram of the IC 555 connected for astable operation is shown in Fig. 7.27. The device connection diagram with external components is shown in Fig. 7.28. Resistors  $R_A$  and  $R_B$  form the timing resistors. The *discharge* (pin 7) terminal is connected to the junction of  $R_A$  and  $R_B$ . *Threshold* (pin 6) and *trigger* (pin 2) terminals are connected to the  $v_c$  terminal, and *control* (pin 5) terminal is by-passed to ground through a  $0.01\ \mu\text{F}$  capacitor.



**Fig. 7.27** Functional diagram of astable multivibrator using IC 555 Timer

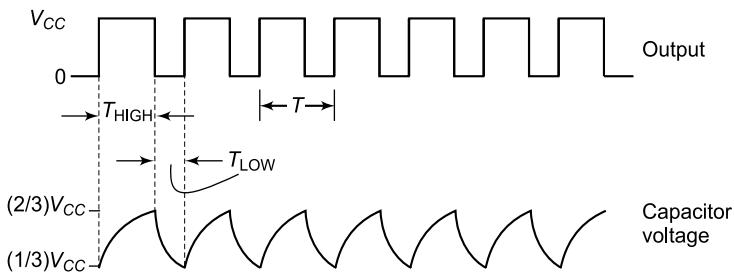


**Fig. 7.28** Connection diagram of astable multivibrator

When the power supply  $V_{CC}$  is connected to the circuit, the capacitor  $C$  charges towards  $V_{CC}$ . The charging rate is determined by the time constant  $(R_A + R_B)C$ . During this period, the *output* (pin 3) is high, since  $R = 0$ ,  $S = 1$  and thus  $Q = 0$ . When the capacitor voltage reaches and rises just above  $(2/3)V_{CC}$ , the upper comparator triggers, and resets the flip-flop (FF). This makes internal *discharge* transistor  $Q_1$  ON, resulting in the capacitor  $C$  discharging towards ground through the resistance  $R_B$  and  $Q_1$ . The time constant for discharging is  $R_B C$ . Since current can also flow through  $R_A$  into  $Q_1$ , the resistance  $R_A$  and  $R_B$  are to be made large enough to limit this current. A maximum current of 0.2A can be allowed to flow through the ON transistor  $Q_1$ .

When the timing capacitor  $C$  discharges, as it reaches and goes just less than  $(1/3)V_{CC}$ , the lower comparator gets triggered. This sets the flip-flop making  $Q = 0$ . This results in unclamping the external timing capacitor by switching  $Q_1$  OFF. This cycle of charging to  $(2/3)V_{CC}$ , and discharging to  $(1/3)V_{CC}$  repeats. Figure 7.29 shows the timing sequence and capacitor voltage waveform during the astable operation. The output (pin 3) is high during the internal charging of the capacitor from  $(1/3)V_{CC}$  to  $(2/3)V_{CC}$ . The capacitor voltage  $v_c$  for a low pass  $RC$  circuit is given by

$$v_c = V_{CC}(1 - e^{t/RC})$$



**Fig. 7.29** The timing waveform of astable multivibrator

Here we assume a step input of  $V_{CC}$  Volts.

If  $t_1$  is the time taken by the capacitor to charge from 0 to  $(2/3)V_{CC}$ , then

$$(2/3)V_{CC} = V_{CC}(1 - e^{-t_1/RC})$$

Therefore,  $t_1 = 1.098 RC$

If  $t_2$  is the time taken by the capacitor to charge from 0 to  $(1/3)V_{CC}$ , then

$$(1/3)V_{CC} = V_{CC}(1 - e^{-t_2/RC})$$

Therefore,  $t_2 = 0.405 RC$

Then the time taken by the capacitor to charge from  $(1/3)V_{CC}$  to  $(2/3)V_{CC}$  is given by

$$\begin{aligned} t_{ON} &= t_1 - t_2 \\ &= 1.098RC - 0.405RC \\ &\approx 0.693RC \end{aligned}$$

Thus,  $t_{ON}$  for the circuit is

$$t_{ON} = 0.693(R_A + R_B)C$$

where  $R_A$  and  $R_B$  form the charging path. The output is in LOW level during the period of discharging from  $(2/3)V_{CC}$  to  $(1/3)V_{CC}$  and the voltage across the capacitor in such a condition is expressed by

$$(1/3)V_{CC} = (2/3)V_{CC}e^{-t/RC}$$

Hence,  $t = 0.693 RC$

Therefore, for the astable circuit,

$$t_{OFF} = 0.693 R_B C$$

where  $R_B$  forms the discharging path for the current.

Thus, total time

$$T = T_{ON} + T_{OFF} \text{ or } T = 0.693(R_A + 2R_B)C$$

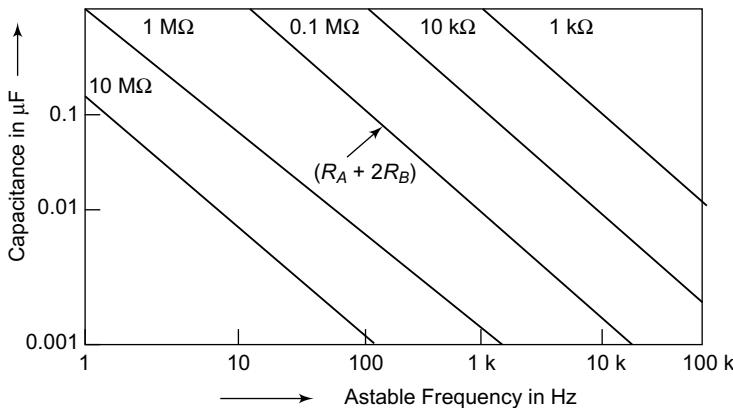
and

$$f = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C}$$

Figure 7.30 shows the various combinations of  $(R_A + 2R_B)$  and  $C$  needed to obtain a stable output frequency. The *duty cycle D* of any pulse generator circuit is

$$D = \frac{\text{high (ON) interval}}{\text{period}} \times 100\% = \frac{T_{ON}}{T} \times 100\%$$

$$D = \frac{R_A + R_B}{R_A + 2R_B} \times 100\%$$



**Fig. 7.30**  $R_A$ ,  $R_B$  and  $R_C$  combinations for different frequencies

Defining the duty cycle in this manner always makes  $D$  greater than 50% since  $T_{ON} > T_{OFF}$ . An alternative way of defining the duty cycle for this circuit is

$$D = \frac{T_{OFF}}{T} \times 100\% = \frac{R_B}{R_A + 2R_B} \times 100\%$$

It can be noted that the later definition takes into account the time when  $Q_1$  is ON as  $T_{ON}$ . The resulting duty cycle value is less than 50%.

### Example 7.8

Determine the frequency of oscillation if the duty cycle  $D = 20\%$  and the ON period  $T_1 = 1 \text{ ms}$ .

**Solution**

The duty cycle is

$$D = \frac{T_{ON}}{T_{ON} + T_{OFF}} \times 100\%$$

Therefore,

$$\frac{20}{100} = \frac{1 \times 10^{-3}}{T_{ON} + T_{OFF}}$$

Here the total period,

$$T = T_{ON} + T_{OFF} = 5 \text{ ms}$$

Therefore, the frequency of oscillation,  $f = \frac{1}{T} = 200 \text{ Hz.}$

**Example 7.9**

*Design an astable multivibrator using 555 timer for a frequency of 1 kHz and a duty cycle of 70%. Assume C = 0.1 μF.*

**Solution**

The ON period  $T_{ON} = 0.693(R_A + R_B)C_1$ .

Similarly, the OFF period  $T_{OFF} = 0.693 R_B C_1$

The total period  $T$  is given by  $T = T_{ON} + T_{OFF} = 0.693(R_A + 2R_B)C_1$

Therefore, the duty cycle  $D$  is given by

$$D = \frac{T_{ON}}{T_{ON} + T_{OFF}} = \frac{T_{ON}}{T} = \frac{0.693(R_A + R_B)C_1}{0.693(R_A + 2R_B)C_1} = \frac{R_A + R_B}{R_A + 2R_B}$$

Given  $D = 0.7$ , we have

$$D = \frac{R_A + R_B}{R_A + 2R_B} = \frac{7}{10}$$

Therefore,

$$R_A = \frac{4}{3}R_B$$

The period of oscillation  $T = 0.693 \times \frac{10}{3} R_B \times 10^{-7}$

Substituting the value of  $T$  and solving, we get

$$R_B = \frac{1 \times 10^4}{0.693 \times \frac{10}{3}} = 4.7 \text{ k}\Omega$$

Therefore,

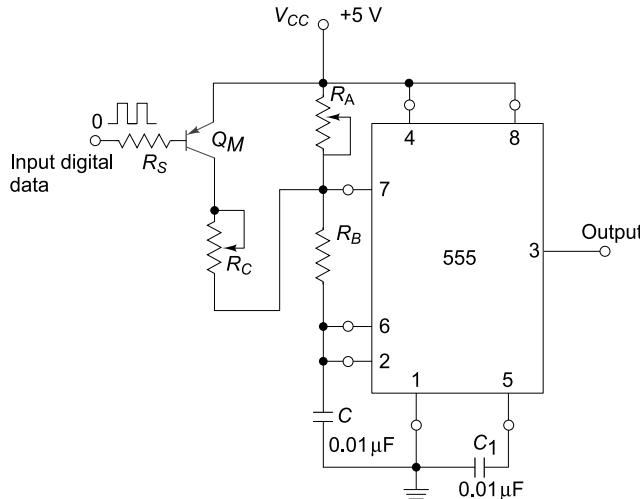
$$R_A = \frac{4}{3} \times 4700 \approx 6.8 \text{ k}\Omega.$$

**7.7.5 Applications of Astable Multivibrator**

The important applications of the astable multivibrator are FSK generator, Pulse position modulator and Schmitt trigger.

**FSK generator** A timer IC 555 connected for FSK (Frequency-Shift-Keying) generation is shown in Fig. 7.31. The FSK method transmits data by identifying the logic 0 and 1 by means of two preset frequencies. The digital data input frequency is normally 150 Hz. Here, when the input is HIGH,  $Q_M$  is OFF. This makes the timer work in normal astable mode with the preset frequency defined by

$$f_1 = \frac{1.45}{(R_A + 2R_B)C}$$



**Fig. 7.31** FSK generator connection diagram

When the input goes LOW,  $Q_M$  is ON and it connects resistance  $R_C$  across  $R_A$ . The effective resistance  $R_A \parallel R_C$  in series with  $R_B$  now forms the charging path. Therefore, the output frequency  $f_2$  is

$$f_2 = \frac{1.45}{(R_A \parallel R_C + 2R_B)C}$$

### Example 7.10

The teletypewriter uses the frequencies 1070 Hz and 1270 Hz for its MODEM. Design the FSK generator circuit shown in Fig. 7.31 for this application.

**Solution** The components  $R_A$ ,  $R_B$  and  $C$  can be selected so that  $f_1 = 1070$  Hz.

That is,

$$f_1 = 1070 = \frac{1.45}{(R_A + 2R_B)C}$$

Assuming

$$R_A = 50 \text{ k}\Omega \text{ and } C = 0.01 \mu\text{F},$$

$$R_B = 42.77 \text{ k}\Omega$$

We know that,

$$f_2 = \frac{1.45}{(R_A \parallel R_C + 2R_B)C}$$

Then, for output frequency

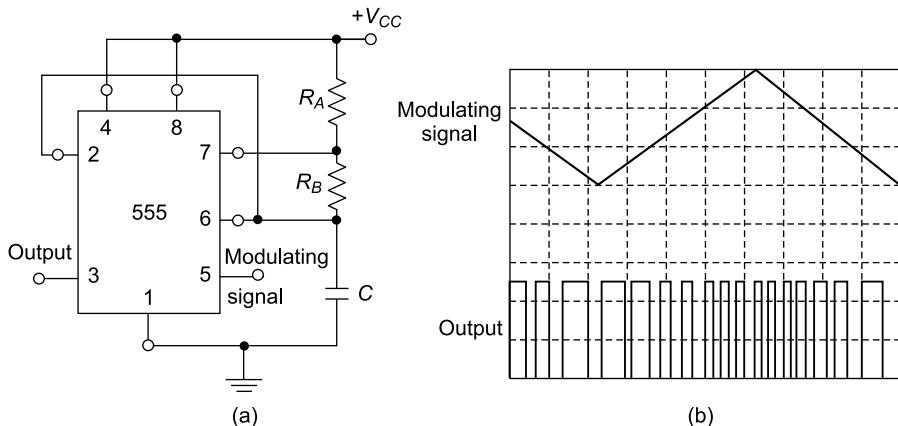
$$f_2 = 1270 \text{ Hz}$$

$$1270 = \frac{1.45}{50 \times 10^3 \parallel R_C + 2(42.77 \times 10^3)}$$

Thus,

$$R_C \approx 76 \Omega \text{ (Standard value).}$$

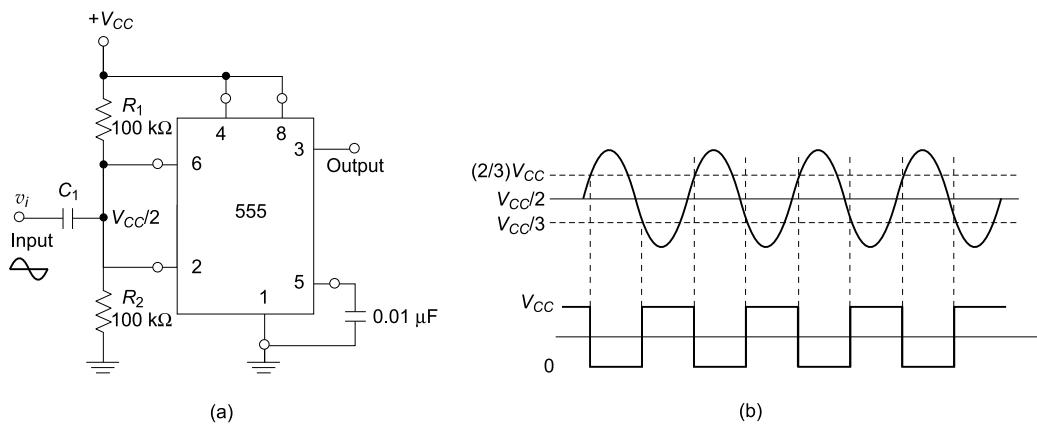
**Pulse-position modulator** The timer IC 555 connected for pulse-position modulation is shown in Fig. 7.32(a). The modulating signal is applied to the modulating control input (pin 5). This changes the threshold voltage condition for the upper comparator. Therefore, the output pulse position varies due to the modulating signal. Figure 7.32(b) shows the output waveform obtained for an input triangular wave modulating signal. It can be seen that the output frequency changes with respect to the modulating signal leading to pulse position modulation.



**Fig. 7.32** Pulse-position modulator using astable operation of IC Timer: (a) The connection diagram (b) Modulating signal and output waveforms

**Schmitt trigger using timer IC 555** The timer IC 555 can be used to function as a Schmitt trigger with variable threshold voltage levels.

The use of timer IC 555 connected as a Schmitt trigger circuit in astable mode of operation is shown in Fig. 7.33(a). The two internal comparator inputs (pins 2 and 6) are connected together and externally biased with a voltage  $V_{CC}/2$  through  $R_1$  and  $R_2$  potential divider network. Since the voltage at pins 6 and 2 will trigger the upper comparator (UC) at  $(2/3)V_{CC}$  and the lower comparator (LC) at  $(1/3)V_{CC}$ , the bias provided by  $R_1$  and  $R_2$  is centered within these two threshold levels. The input and output waveforms are shown in Fig. 7.33(b).



**Fig. 7.33** Schmitt trigger using IC 555 Timer: (a) Connection diagram, (b) Input and output waveforms

When a sine wave input of sufficient amplitude ( $v_i$ ), where  $v_i$  is greater than  $[(2/3)V_{CC} - (1/3)V_{CC}]$  is applied to the circuit, it causes the internal flip-flop to alternatively *Set* and *Reset* generating a square wave output.

Unlike a conventional multivibrator type of square wave generator that divides the input frequency by 2, the main advantage of Schmitt trigger is that it simply converts the sine-wave signal into square-wave signal of the same frequency. Hence, this circuit can be used as a wave shaper.

## SUMMARY

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- ❑ The op-amps are widely used in circuits for generating various waveforms used in timing, control and other functions of analog and digital equipments.
- ❑ The two basic requirements for sustained oscillations are
  - The magnitude of the loop gain  $A_v \beta$  must be unity
  - The total phase-shift of the loop gain  $A_v \beta$  must be equal to  $0^\circ$  or  $360^\circ$
- ❑ In sine-wave oscillators using op-amps, the phase-shift of  $180^\circ$  in the feedback loop is obtained by using either  $L$  and  $C$ , or  $R$  and  $C$  components.
- ❑ Colpitts and Hartley oscillators are LC oscillators.
- ❑ The frequency of oscillation of Hartley oscillator is  $f_o = \frac{1}{2\pi\sqrt{CL_T}}$  where  $L_T = L_1 + L_2$  or  $L_T = L_1 + L_2 + 2M$ .
- ❑ The oscillation frequency of Colpitts oscillator is  $f_o = \frac{1}{2\pi\sqrt{LC_T}}$  where  $C_T = \frac{C_1 C_2}{C_1 + C_2}$ .
- ❑ Oscillators using tuned LC circuits are suitable for high frequencies, since at low frequencies, the inductors and capacitors would become very bulky.
- ❑ RC oscillators are found to be suitable for low frequencies.
- ❑ Two types of RC oscillators are
  - RC phase shift oscillator
  - Wien Bridge oscillator
- ❑ Frequency of oscillation of the phase-shift oscillator is  $f_o = \frac{1}{2\pi\sqrt{6RC}}$  and  $R_f = 29 R_1$ .
- ❑ Zener diodes connected *back-to-back* at the output of an op-amp can limit the amplitude of oscillations.
- ❑ Wien Bridge oscillator possessing simplicity and stability is the most commonly used audio frequency oscillator and it can be used in the range of 5 Hz to about 1 MHz.
- ❑ The frequency of oscillation of Wien Bridge oscillator is  $f_o = \frac{1}{2\pi RC}$ , voltage gain  $A_v = 1 + \frac{R_f}{R_1} = 3$  and  $R_f = 2R_1$ .
- ❑ Multivibrators are regenerative circuits used in timing applications and they are classified as
  - Astable multivibrator or free-running multivibrator
  - Monostable multivibrator or one-shot
  - Bistable multivibrator
- ❑ The frequency of the astable or free running multivibrator is determined by the charging and discharging time of the capacitor between two voltage levels. The output peak amplitudes can be varied by the use of Zener diodes connected back to back at the output.
- ❑ The monostable multivibrator has a stable state of duration  $T$  and a quasi-stable state. Single output pulse of adjustable time duration in response to a triggering signal can be generated using the monostable multivibrator. Different values of  $T$  is achieved by connecting required external components to the op-amp.

- Monostable multivibrator can be used as a time-delay circuit and as gating signal generator in counters and analog-to-digital converters.
- A triangular waveform generator can be designed by using a square-wave generator connected to an integrator.
- The sawtooth wave has its rise time many times longer than the fall time, or fall time much longer compared to the rise time. Triangular wave generator can be modified to produce a sawtooth waveform.
- ICL8038 waveform generator is a monolithic integrated circuit and it can produce sine, square, triangular, sawtooth and pulse waveforms of high accuracy.

The frequency  $f_o$  of ICL8038 is given by  $f_o = 3 \left(1 - \frac{R_B}{2R_A}\right) \frac{V_i}{R_A C V_{CC}}$  and duty cycle  $D = \left(1 - \frac{R_B}{2R_A}\right) 100\%$ .

$$\text{When } R_A = R_B = R, f_o = KV_i \text{ where } K = \frac{1.5}{RCV_{CC}}.$$

- ICL8038 can be used for frequency modulation.
- The Type SE555/NE555 integrated circuit timer was first introduced by Signetics Corporation.
- The 555 timer operates with a dc supply voltage from +5V to +18V. It is compatible to TTL/CMOS logic circuits and op-amp circuits and it is very versatile.
- The applications of 555 timer are oscillator, pulse generator, square and ramp wave generator, one-shot multivibrator, safety alarm and timer circuits, and traffic light controllers. The IC can provide time delay ranging from microseconds to hours.
- The time delay of a monostable multivibrator is given by  $T = -RC \ln(3) = 1.1RC$  sec.
- Some applications of monostable multivibrator are (i) Ramp generation, (ii) Frequency division, and (iii) Pulse-width modulation.
- The astable multivibrator using 555 has the time period

$$T = 0.693(R_A + 2R_B) \text{ and } f = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C}.$$

- The duty cycle is  $D = \frac{\text{high (ON) interval}}{\text{period}} \times 100\% = \frac{T_{ON}}{T} \times 100\%$ .
- Some applications of astable multivibrator are FSK generator, Pulse position modulator and Schmitt trigger.
- Timer IC 555 can be used as a Schmitt trigger with variable threshold voltage levels.

## REVIEW QUESTIONS

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1. What are the two conditions necessary for the generation of oscillations?
2. Distinguish between oscillators and amplifiers.
3. Classify oscillators.
4. Explain the principle of operation of LC oscillators with necessary circuits.
5. Explain the operation of (a) Colpitts oscillator and (b) Hartley oscillator with circuit diagrams.
6. Design a Hartley oscillator to oscillate at 10 kHz. Use 5 mH inductor.
7. Determine the frequency of oscillation of the Colpitts oscillator shown in Fig. 7.4. Assume  $L = 500 \mu\text{H}$ ,  $C = 3.3 \mu\text{F}$  and  $R_1 = R_f = 4.7 \text{ k}\Omega$ .
8. Explain the operation of an RC phase-shift oscillator. Derive for the frequency of oscillation.
9. How do the three sections of RC network bring about a phase-shift of  $180^\circ$  in a phase-shift oscillator?
10. Design an RC phase-shift oscillator which oscillates at 5 kHz. Assume  $C = 0.1 \mu\text{F}$ .
11. Design a phase-shift oscillator using an op-amp for  $f_o = 500 \text{ Hz}$ .
12. Design a phase-shift oscillator using op-amp for an output frequency of 200 Hz.
13. Explain the operation of a Wien Bridge oscillator using op-amp with a circuit diagram.

14. Draw the circuit of a Wien Bridge oscillator and derive an expression for its frequency of oscillation.
15. Design a Wien Bridge oscillator using an op-amp for  $f_o = 1000$  Hz.
16. Design an op-amp based Wien Bridge oscillator for a frequency of 10 kHz and explain its operation.
17. Explain the operation of square-wave generator using op-amp with capacitor and output voltage waveforms. How can you obtain a non-symmetrical square-wave?
18. Draw the circuit of an astable multivibrator using op-amp and derive the expression for its frequency of oscillations. How will you modify this circuit to have independent control of ON and OFF time durations?
19. Design a square-wave oscillator for  $f_o = 1$  kHz using 741 OP-AMP and a dc supply voltage of  $\pm 12$  V.
20. In the Wien Bridge circuit shown in Fig. 7.7 (a), assume  $R_2 = 10$  k $\Omega$ ,  $R_1 = 11.6$  k $\Omega$ ,  $R = 100$  k $\Omega$ ,  $C = 0.01$   $\mu$ F. Calculate the frequency of oscillations.
21. Show how the output amplitude stabilisation could be achieved in the Wien Bridge oscillator.
22. What are quadrature oscillators? Show how two sinusoidal signals are generated with  $90^\circ$  phase difference between them?
23. What is *one-shot*? Explain its operation with a circuit diagram.
24. Design a monostable multivibrator for 0.6s ON time.
25. Explain the operation of a triangular wave generator.
26. Draw the circuit of a triangular wave generator using a comparator and an integrator. Explain its operation with the output waveform.
27. Describe the generation of sinusoidal and triangular wave using two op-amps.
28. Assume that for the circuit shown in Fig. 7.10 (a),  $R_1 = 10$  k $\Omega$ ,  $R_2 = 1$  k $\Omega$ ,  $R_3 = 2.2$  k $\Omega$ ,  $C_1 = 0.01\mu$ F and  $\pm V_{sat} = \pm 14$  V for the op-amps. Determine the (a) period, (b) frequency, (c) peak value of square-wave, and (d) peak value of triangular wave.
29. Draw a circuit using op-amp to generate sawtooth wave. Explain its operation.
30. List the applications of a sawtooth wave generator.
31. Sawtooth generators are used in CROs (True / False).
32. With relevant circuit diagrams, explain how an op-amp is used to produce sinusoidal, triangular and ramp outputs.
33. What is VCO? Explain the operation of a grounded capacitor type of VCO.
34. Explain the operation of ICL8038 with necessary circuit diagrams.
35. How do you use ICL8038 for frequency modulation? Explain.
36. Define a multivibrator.
37. What is timer IC 555? Draw the internal structure of IC555 Timer.
38. Define (a) an astable multivibrator, and (b) a monostable multivibrator.
39. Derive the expression for the period of a pulse generated when 555 Timer is used as a monostable multivibrator.
40. Design a monostable multivibrator using 555 timer for a pulse period of 2 ms.
41. Differentiate an astable multivibrator from a monostable multivibrator.
42. Define the *duty cycle* of an astable multivibrator.
43. Design a square-wave generator using 555 timer for a frequency of 150 Hz and 70% duty cycle. Assume  $C = 0.1\mu$ F.
44. Determine the frequency of oscillation if the duty cycle  $D = 25\%$  and the ON period  $T_1 = 1$  ms.
45. Design a dual frequency generator circuit for the frequencies 1200 Hz and 1000 Hz.
46. Give the advantages of the op-amp based astable multivibrator over the BJT based multivibrator.
47. Write notes on voltage controlled multivibrator using IC 555.
48. List various applications of 555 timer.
49. Explain the operation of a Schmitt trigger using IC 555.
50. Design a circuit to produce a 120  $\mu$ s output pulse using the IC 555.

# Voltage Regulators

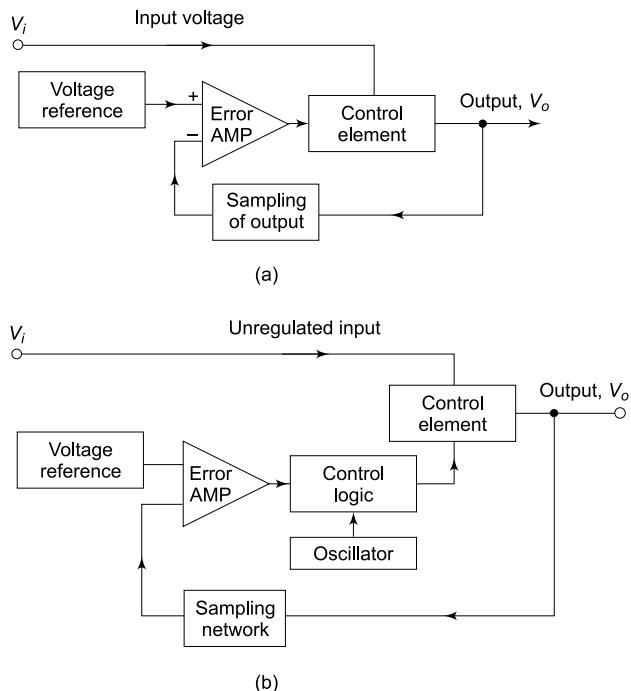
## 8.1 INTRODUCTION

All electronic circuits need dc power supply either from battery or power pack units. It may not be economical and convenient to depend upon battery power supply. Hence, many electronic equipments contain circuits which convert the ac supply voltage into dc voltage at the required level. The dc voltages obtained from such circuits should be stable.

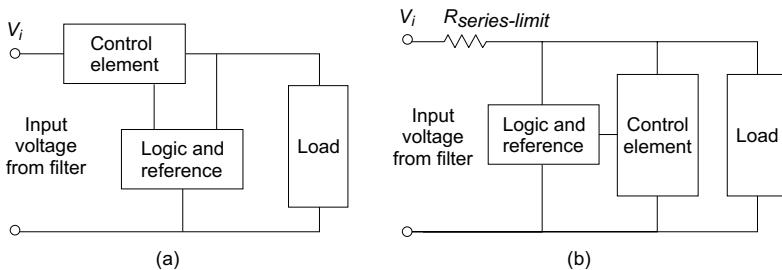
In an unregulated power supply, the output voltage changes whenever the input voltage or load changes. An ideal regulated power supply is an electronic circuit designed to provide a predetermined dc voltage which is independent of the load current and variations in the input voltage. The dc voltage regulated power supplies are employed to provide a stable dc voltage independent of the load current, temperature and ac line voltage variations and to attenuate the ripple.

The commonly used voltage regulators can be classified into (i) Linear voltage regulators and (ii) Switching regulators. The main difference between these two regulators is seen from the block diagrams given in Figs. 8.1(a) and (b).

The linear regulators are classified into two types, namely, (i) Series regulator and (ii) Shunt regulator. Their respective block diagrams are shown in Figs. 8.2(a) and (b). The control element connected in *series* or in *shunt* with the load identifies the circuit as a *series* or a *shunt* voltage regulator. The linear regulators are available for fixed positive or negative output voltages and variable positive or negative output voltages. The schematic, important characteristics, specifications, short-circuit protection, current foldback and current boosting techniques for linear voltage regulators such as 78XX, 79XX, LM317/337 and IC 723 types of linear regulators are discussed in this chapter.



**Fig. 8.1** (a) Block diagram of a linear voltage regulator  
 (b) Block diagram of a switching voltage regulator



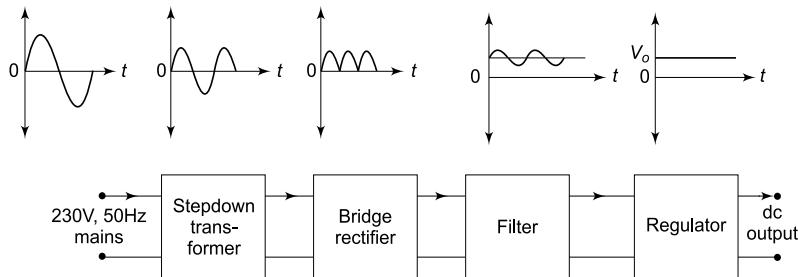
**Fig. 8.2** (a) Block diagram of a series voltage regulator  
(b) Block diagram of a shunt voltage regulator

The switching regulators make use of a power transistor, which acts as a high frequency switch. Therefore, the transistor does not pass current continuously and it results in improved efficiency in regulation. The switching regulators can generate output voltage of opposite polarity, multiple output voltages, or isolated outputs. They can be made to operate directly from the ac power line unlike the linear regulators. The limitations of these regulators are that they need coils, capacitors and complex control circuitry and the operation is noisy. The principle of switching power supply, step-down and step-up switching modes of operation, and switching regulator IC 7840 are also discussed in this chapter.

## 8.2 BASICS OF VOLTAGE REGULATOR

### 8.2.1 Linear Mode Power Supply

The basic building blocks of a linear power supply are shown in Fig. 8.3. A transformer supplies ac voltage at the required level. This bidirectional ac voltage is converted into a unidirectional and pulsating dc using a rectifier. The unwanted ripple contents of this pulsating dc are removed by a filter to get a pure dc voltage. The output of the filter is fed to a voltage regulator which gives a steady dc output, independent of load variations and input supply fluctuations.



**Fig. 8.3** Basic building blocks of linear mode power supply

The performance of a voltage regulator is usually defined in terms of the line regulation, load regulation and ripple rejection.

**Factors determining the stability** The output dc voltage \$V\_o\$ depends on the input unregulated dc voltage \$V\_{in}\$, load current \$I\_L\$ and temperature \$T\$. Hence, the change in output voltage of a power supply can be expressed as follows:

$$\Delta V_o = \frac{\partial V_o}{\partial V_i} \Delta V_i + \frac{\partial V_o}{\partial I_L} \Delta I_L + \frac{\partial V_o}{\partial T} \Delta T$$

or

$$\Delta V_o = S_V \Delta V_i + R_o \Delta I_L + S_T \Delta T$$

where the three coefficients  $S_V, R_o$  and  $S_T$  are defined as

Input regulation factor,  $S_V = \frac{\Delta V_o}{\Delta V_i} \mid \Delta I_L = 0; \Delta T = 0$

Output resistance,  $R_o = \frac{\Delta V_o}{\Delta I_L} \mid \Delta V_i = 0; \Delta T = 0$

Temperature coefficient,  $S_T = \frac{\Delta V_o}{\Delta T} \mid \Delta V_i = 0; \Delta I_L = 0$

Smaller the value of the three coefficients, better the regulation of the power supply.

**Line regulation** Line regulation is defined as the change in output voltage for a change in line-supply voltage keeping the load current and temperature constant. Line regulation is given by

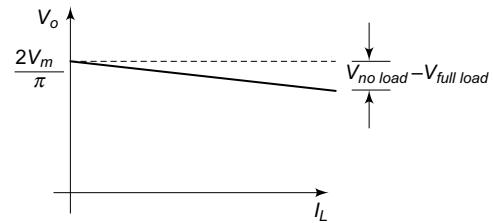
$$\text{Line regulation} = \frac{\text{change in output voltage}}{\text{change in input voltage}} = \frac{\Delta V_o}{\Delta V_i}$$

**Load regulation** Load regulation is expressed as

$$\text{Load regulation} = \frac{(V_{\text{no load}} - V_{\text{full load}})}{V_{\text{no load}}}$$

or  $\text{Load regulation} = \frac{V_{\text{no load}} - V_{\text{full load}}}{V_{\text{full load}}}$

where  $V_{\text{no load}}$  is the output voltage at zero load current and  $V_{\text{full load}}$  is the output voltage at rated full load current. This is usually denoted in percentage. The plot of the output voltage  $V_o$  versus the load current  $I_L$  for a full wave rectifier is shown in the load regulation characteristics of Fig. 8.4. The drop in the characteristic curve is a measure of the internal resistance of the power supply.



**Fig. 8.4** Load regulation characteristics

**Ripple Rejection Ratio (RRR)** The ac performance of linear IC regulators is specified by a parameter called *ripple rejection ratio*. It is defined as the ratio of peak-to-peak input ripple voltage  $\Delta V_{o(\text{unreg})}$  or  $V_r$  to the peak-to-peak output ripple voltage  $\Delta V_{o(\text{reg})}$ . This is typically 60 dB or more for the commonly used voltage regulators.

The Ripple Rejection Ratio (RRR) is expressed in decibels as  $RRR = 20 \log \frac{\Delta V_{o(\text{unreg})}}{\Delta V_{o(\text{reg})}}$ . The RRR specification is used particularly in connection with voltage regulators. This provides an indication of the amount of ripple, normally 100 Hz ripple fed to the output.

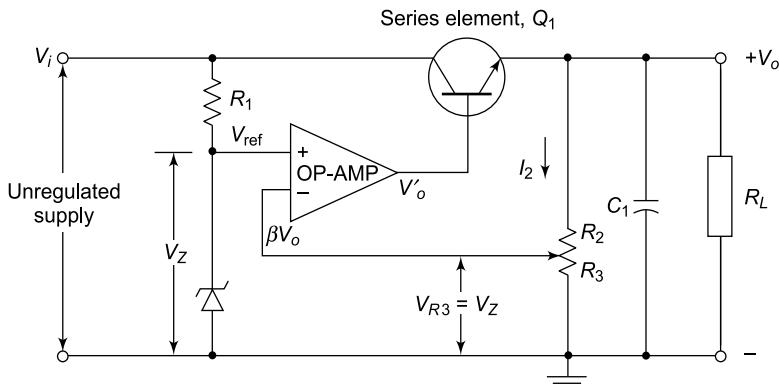
### 8.3 LINEAR VOLTAGE REGULATORS USING OP-AMPS

If the control element of a voltage regulator operates in its linear region, then the regulator is called a linear voltage regulator. Linear voltage regulators are generally of series mode type. The voltage regulator

circuit using Zener diode is vulnerable to the variations in supply voltage since the current through the Zener diode also changes correspondingly. Hence the linear voltage regulator uses an op-amp as an error amplifier, and a pass transistor as a control element. The error output from the op-amp drives the control element, which allows current to the load accordingly and keeps the output voltage constant.

### 8.3.1 Single Polarity Linear Voltage Regulator using Op-amp

The basic circuit of a linear voltage regulator is shown in Fig. 8.5. The regulating circuit consists of a voltage reference  $V_{ref}$ , a differential amplifier called *error amplifier* using op-amp and a series regulating element  $Q_1$  connected as an emitter follower. The output voltage is sampled and fed back to the inverting input of the error amplifier through the potential divider  $R_2 - R_3$ . The error amplifier produces an output voltage that is proportional to the difference between the reference voltage and the sampled output voltage and it may be written as  $V'_o = A[V_{ref} - \beta V_o]$ , where  $A$  is the gain of the amplifier and  $\beta$  is the feedback factor which is equal to  $R_3/(R_2 + R_3)$ . Since the drop across the base-emitter junction of transistor  $Q_1$  is small, the output  $V_o$  can be approximated to  $V'_o$ .



**Fig. 8.5** Basic circuit of a linear voltage regulator

Thus,

$$V'_o = V_o = A[V_{ref} - \beta V_o]$$

That is,

$$V_o = \frac{AV_{ref}}{1 + A\beta} \quad (8.1)$$

Equation (8.1) implies that the output voltage is determined by the reference voltage and the feedback factor. The output voltage thus obtained is kept at a constant level by the control of series element connected with the error amplifier. For instance, an increase in output voltage causes a corresponding decrease in the error amplifier output, which biases the series control transistor with reduced base current. This action causes an increase in collector-to-emitter voltage and thus the increase in the output is reduced.

On the other hand, when the output voltage reduces, the output of the differential amplifier increases. Then, the series transistor is biased heavily at its base and as a consequence, the collector-to-emitter voltage decreases. Thus the reduction in output is compensated and the output voltage is maintained constant.

### Example 8.1

Referring to Fig. 8.5, design a linear voltage regulator to produce an output of 15 V with a maximum load current of 50 mA.

**Solution** Refer to Fig. 8.5. Given  $V_o = 15$  V. We know that

$$V_{i(min)} = V_o + 3\text{V} = 15 + 3 = 18\text{V}$$

Assuming the ripple voltage  $V_r = 2$  V (max), the input voltage is

$$V_i = V_{i(min)} + \frac{V_r}{2} = 18 + 1 = 19\text{V}$$

Therefore, the input voltage,  $V_i = 19$  V with a 2 V (max) ripple superimposed on it.

Then,  $V_Z = \frac{V_i}{2} = \frac{19}{2} = 9.5\text{V}$  (use the Zener diode 1N758 for 10 V)

Therefore,  $V_Z = 10\text{V}$  and  $I_Z \gg 20\text{mA}$

$$R_1 = \frac{V_i - V_Z}{I_Z} = \frac{19 - 10}{20 \times 10^{-3}} = 450\Omega$$

$$I_2 > I_{B(max)}$$

Let  $I_2 = 50\mu\text{A}$

$$R_2 = \frac{V_o - V_Z}{I_2} = \frac{15 - 10}{50 \times 10^{-6}} = 100\text{k}\Omega$$

$$R_3 = \frac{V_Z}{I_2} = \frac{10}{50 \times 10^{-6}} = 200\text{k}\Omega$$

Select  $C_1 = 50\mu\text{F}$

**Specification of transistor  $Q_1$**

$$V_{CE(max)} = V_{i(max)} = V_i + V_r/2 = 19 + 2/2 = 20\text{V}$$

$$I_E = I_L = 50\text{mA}$$

$$P = V_{CE} \times I_L = (V_i - V_o) \times I_L$$

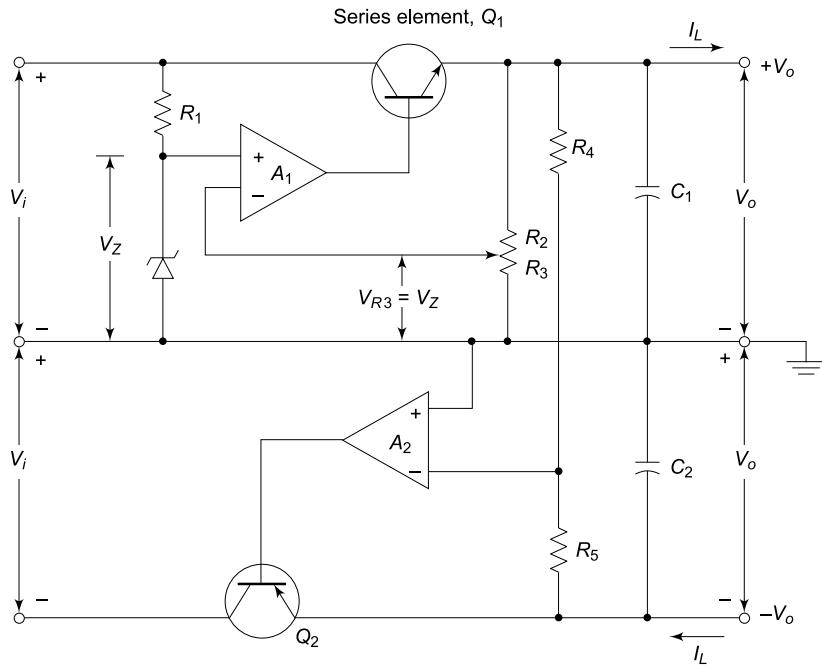
$$= (19 - 15) \times 50 \times 10^{-3} = 200\text{mW}$$

Use the transistor 2N718 for  $Q_1$ .

### 8.3.2 Dual Tracking Voltage Regulator using Op-amps

The circuit diagram of a dual tracking voltage regulator using op-amps is shown in Fig. 8.6. The top half of the circuit is similar to the single polarity positive voltage regulator shown in Fig. 8.5. The bottom half of the circuit consisting of the components op-amp  $A_2$ , PNP transistor  $Q_2$ , resistors  $R_4$  and  $R_5$ , and capacitor  $C_2$  constitutes a negative voltage regulator. The reference voltage for the negative voltage regulator is provided by the output of the positive voltage regulator circuit. The potential divider  $R_4$  and  $R_5$  is connected between the positive and negative output terminals. Any change in the negative voltage output is applied to the op-amp  $A_2$ , which amplifies and inverts to correct the change accordingly. When

the resistors  $R_4$  and  $R_5$  are made equal, the output voltage between the positive and negative terminals is exactly twice the positive voltage. This gives a negative output that is equal to the positive output. This type of negative voltage regulator is called a *tracking regulator*, since the negative voltage output tracks the change in the positive output voltage.



**Fig. 8.6** Dual tracking voltage regulator using op-amps

The arrangement of this type of *plus-minus* power supply is possible only when there is no ground connection in the unregulated power supply.

## 8.4 IC VOLTAGE REGULATORS

Although voltage regulators can be designed using op-amps, it is quicker and easier to use IC voltage regulators. The IC voltage regulators are versatile, relatively inexpensive and are available with features such as programmable output, current/voltage boosting and floating operation for high voltage application. Some important types of linear IC voltage regulators are:

- (i) Fixed positive/negative output voltage regulators
- (ii) Adjustable output voltage regulators

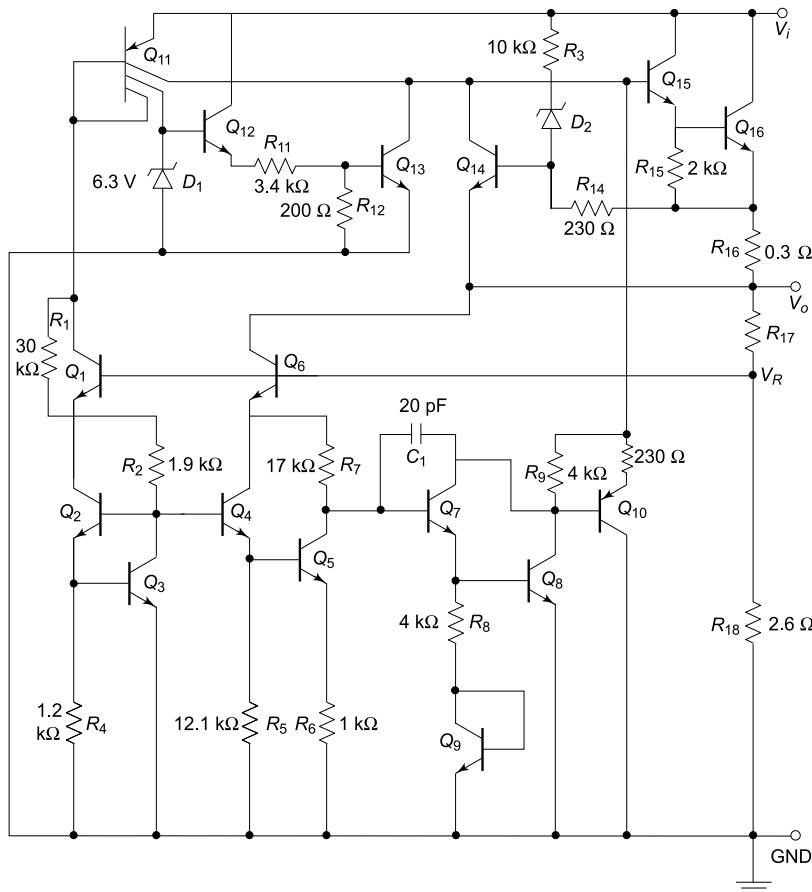
**Fixed voltage regulators** 78XX series are three terminal positive fixed voltage regulators. There are seven voltage regulators with output voltages of 5V, 6V, 8V, 12V, 25V, 18V and 24V. The two digits XX of 78XX are used to identify the fixed output voltage of the regulator.

79XX series are negative fixed voltage regulators which are complements to the 78XX series devices. There are two additional voltage options of -2V and -5.2V available in 79XX series.

### 8.4.1 78XX and 79XX Voltage Regulators

The internal circuit diagram of a three terminal positive voltage regulator integrated circuit 7805 is shown in Fig. 8.7. This circuit provides over-current and thermal overload protections. The functional blocks of the regulator circuit are:

- (i) The band gap voltage reference circuit is formed by the transistors  $Q_1$  through  $Q_8$ . The band gap reference voltage  $V_R$  appears at the base of  $Q_6$  that is across the resistor  $R_{18}$ . This voltage  $V_R$  is applied to the base of  $Q_1$  as input.
- (ii) Transistor  $Q_{10}$  along with resistor  $R_9$  forms an emitter follower which provides the necessary base drive for the series pass output stage consisting of transistors  $Q_{15}$  and  $Q_{16}$ .
- (iii) Transistor  $Q_{11}$  is a lateral PNP transistor with multiple collector terminals providing a multiple current source configuration. One of the collectors of  $Q_{11}$  acts as a current source active load for  $Q_{10}$ .
- (iv) Transistor  $Q_{14}$  with current-limit resistor  $R_{16}$  of  $0.3\ \Omega$  provides foldback current limiting for overload protection. Resistors  $R_3$  and  $R_{14}$  with Zener diode  $D_2$  provide the foldback dependence of the input-output voltage difference.
- (v) Transistors  $Q_{12}$  and  $Q_{13}$  with Zener diode  $D_1$ ,  $R_{11}$  and  $R_{12}$  provide thermal shutdown. Current source biasing for  $D_1$  is provided by one of the collectors of  $Q_{11}$ .



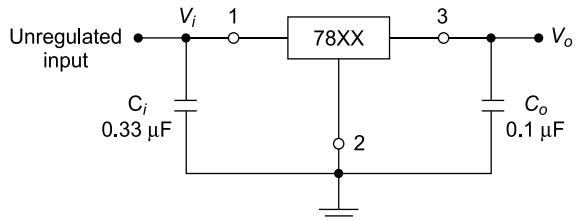
**Fig. 8.7** Internal circuit diagram of IC 7805

The standard circuit connection of the 78XX monolithic voltage regulator is shown in Fig. 8.8. The input capacitor  $C_i$  is used to cancel the inductive effects due to long distribution leads and the output capacitor  $C_o$  improves the transient response and acts as a ripple filter also.

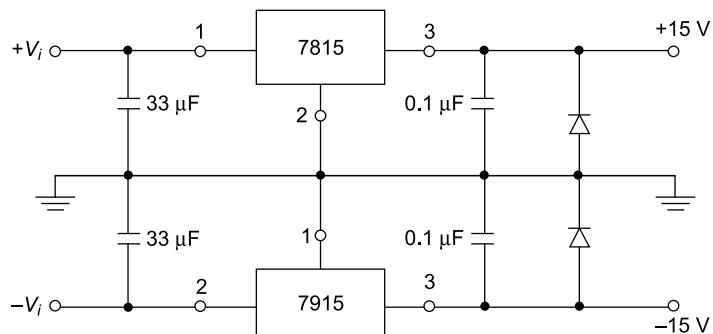
#### 8.4.2 Dual Voltage Regulator

Figure 8.9 shows a dual voltage regulator. The circuit uses fixed positive (IC 7815) and fixed negative (IC 7915) voltage regulators to provide equal +15 V and -15 V respectively. The dual regulated voltage supplies as required for op-amps can be obtained from this circuit.

The advantage of this method is that it can supply a wide range of voltages at much higher currents with the use of heat sinks and external Metal Can package pass transistor.



**Fig. 8.8** IC 78XX monolithic voltage regulator

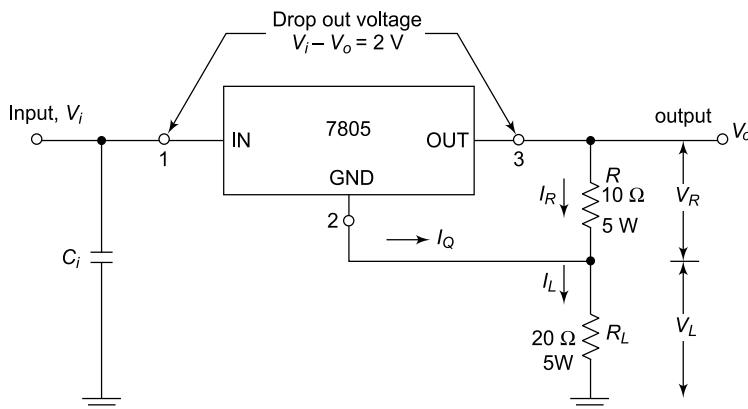


**Fig. 8.9** Dual voltage regulator

#### 8.4.3 Current Source using 7805 Regulation

The three terminal voltage regulator 7805 can be employed as a current source. This is achieved by connecting a current setting resistor  $R$  between the GND and OUT terminals of the regulator IC as shown in Fig. 8.10. Since the voltage at OUT terminal is always constant at 5V, the current through  $R$  is also maintained constant. Thus, by the use of KCL,

$$I_L = I_R + I_Q = \frac{5}{R} + I_Q$$



**Fig. 8.10** IC 7805 used as a current source

Since the quiescent current  $I_Q \approx 4.2 \text{ mA}$  of 7805 is negligible, the load current  $I_R = \frac{V_R}{R}$ . Therefore, for supplying a current of 500 mA to a load of  $20 \Omega$ , 5 W, we need  $R = \frac{5 \text{ V}}{500 \text{ mA}} = 10 \Omega$ .

### Example 8.2

Using 7805 voltage regulator, design a current source to deliver 250 mA current to a  $10 \Omega$ , 3W load.

**Solution** Given  $I_L = 250 \text{ mA}$  and  $V_R = 5 \text{ V}$

Referring to Fig. 8.10, we have

$$R = \frac{V_R}{I_L} = \frac{5 \text{ V}}{250 \times 10^{-3}} = 20 \Omega$$

The output voltage  $V_o = V_R + V_L = 5 + (250 \times 10^{-3} \times 10) = 7.5 \text{ V}$

Therefore, the input voltage  $V_i$  required at the input terminal of 7805 is given by

$$V_i = V_o + \text{Drop out voltage} = 7.5 + 2 = 9.5 \text{ V}$$

#### 8.4.4 Output Current Boosting

The output current of the three terminal regulator can be boosted or amplified by connecting an external pass-transistor  $Q_1$  as shown in Fig. 8.11. The voltage drop across the resistor  $R_1$  for low value of load currents is insufficient to make the transistor  $Q_1$  ON, and therefore the regulator supplies the load current. When the load current  $I_L$  increases beyond a certain limit, the drop across  $R_1$  increases and when it reaches 0.7 V, the transistor  $Q_1$  turns ON, and supplies the additional current to the load. From transistor theory, the additional current is  $\beta$  times the base current.

Then,

$$I_L = I_C + I_o \quad (8.2)$$

and

$$I_C = \beta I_B$$

Thus

$$I_L = \beta I_B + I_o \quad (8.3)$$

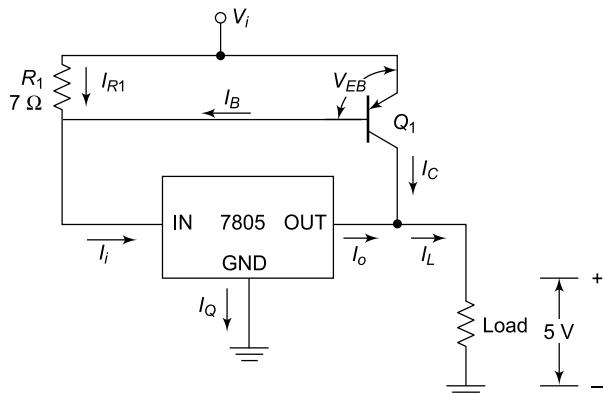
The output current  $I_o$  is given by

$$I_o = I_i - I_Q \approx I_i \text{ since } I_Q \text{ is negligibly small.}$$

Here,

$$I_B = I_i - I_{R1}$$

$$\approx I_o - \frac{V_{EB(ON)}}{R_1} \quad (8.4)$$



**Fig. 8.11** Boosting the output current of IC 7805

Substituting Eq. (8.4) in Eq. (8.3)

$$I_L = I_o (\beta + 1) - \beta \frac{V_{EB(ON)}}{R_1} \quad (8.5)$$

The maximum current that can be obtained by using a 7805 regulator is 1A.

Assuming  $V_{EB(ON)} = 0.7\text{V}$  and  $\beta = 12$  for the transistor,

$$I_L = 1 (12 + 1) - 12 \times \frac{0.7}{7} = 11.8\text{A}$$

### **Example 8.3**

---

Referring to Fig. 8.11, assume  $V_{EB(ON)} = 0.7\text{ V}$  and  $\beta = 50$ . Determine the output current  $I_o$  and  $I_c$  for a load of (a)  $100\Omega$ , (b)  $2\Omega$  in a regulator circuit using IC 7805.

#### **Solution**

$$(a) \text{ Load Current } I_L = \frac{5\text{V}}{100\Omega} = 50 \text{ mA}$$

Voltage across  $R_1 = 50 \text{ mA} \times 7\Omega = 350 \text{ mV}$ .

Since a minimum of  $0.7\text{ V}$  is required to switch a transistor ON,  $Q_1$  is OFF.

Therefore,  $I_L = I_o = I_i = 50 \text{ mA}$

$$(b) \text{ Load Current } I_L = \frac{5\text{V}}{2\Omega} = 2.5 \text{ A}$$

The voltage drop across  $R_1$  is  $2.5\text{A} \times 7\Omega = 17.5\text{V} > 0.7\text{V}$ . Thus,  $Q_1$  is ON.

Using Eq. (8.5), we get

$$\begin{aligned} 2.5 &= I_o \times (50 + 1) - 50 \times \frac{5}{2} \\ I_o &= 0.147 \text{ A} \end{aligned}$$

Therefore,  $I_c = I_L - I_o = 2.5 - 0.147 = 2.353\text{A}$

## **8.5 LM117/LM317 THREE-TERMINAL ADJUSTABLE VOLTAGE REGULATOR**

The fixed voltage regulators are designed and preset for a particular voltage of *positive/negative* polarities. There are applications which require

- (i) regulated voltage sources which are precisely variable, and
- (ii) some supply voltages which are not available from standard fixed voltage regulators.

The most popular variable voltage regulators for such applications are LM117 / LM317 and IC723. The LM117/LM317 and LM137/LM337 families are adjustable three terminal positive and negative voltage regulators respectively. There are several variations of these ICs with different current ratings. The operating specifications are identified by their different suffixes and numbers.

### **8.5.1 LM117/LM317 Adjustable Positive Voltage Regulators**

The LM117/LM317 series regulators are adjustable three terminal positive voltage regulators and they are capable of supplying output current of  $0.1\text{A}$  to  $1.5\text{A}$ , over a range of  $1.2\text{V}$  to  $37\text{V}$  output voltage range. These regulators are available in standard transistor packages as shown in Table 8.1.

**Table 8.1** Different grades of LM117/LM317 regulators

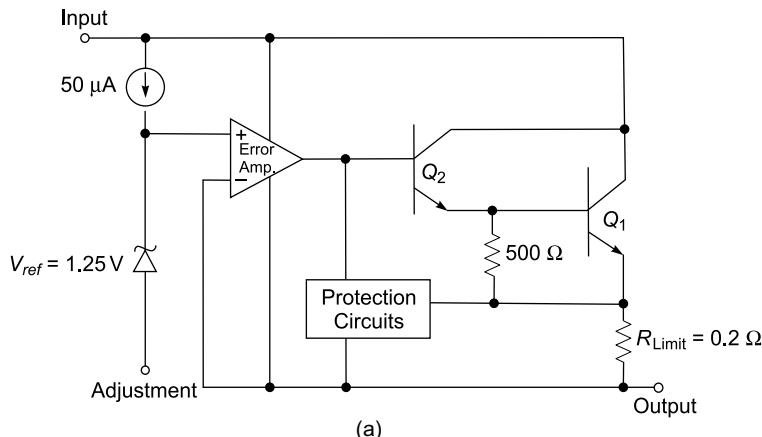
<b>Device</b>	<b>Available <math>V_o</math> (V)</b>	<b>Output Current (A)</b>	<b><math>V_i</math> Max (V)</b>	<b>Ripple Rejection (dB)</b>	<b>Package Type</b>
LM317	1.2 to 37	1.5	40	80	TO-39
LM317H	1.2 to 37	0.5	40	80	TO-39
LM317HV	1.2 to 37	1.5	60	80	TO-3
LM317HVH	1.2 to 37	0.50	40	80	TO-39
LM317L	1.2 to 37	0.10	40	65	TO-92
LM317M	1.2 to 37	0.50	40	80	TO-202

The important specifications of LM117/LM337 are given below:

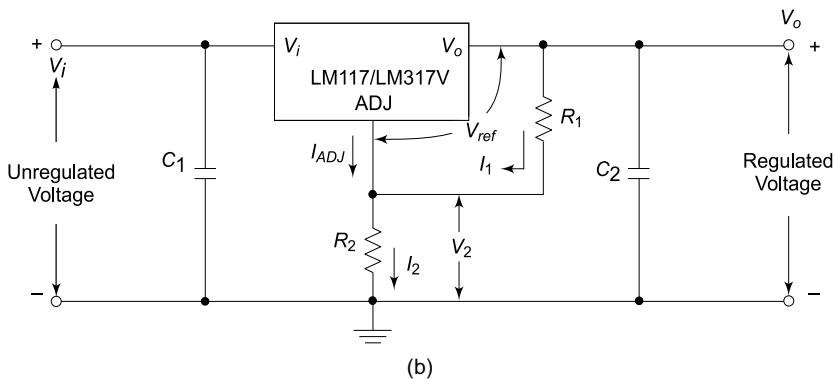
- |  |  |
|--|--|
| Power dissipation (based on the package) | - 0.6W to 20W                              |
| Adjustable output voltage                | - 1.2V to 37V                              |
| Line regulation                          | - 0.01% / V (Typ.)                         |
| Load regulation                          | - 0.1% (Typ.)                              |
| Standard 3-lead Transistor packages      | - TO-3, TO-39, TO-200,<br>TO-202 and TO-92 |
| Ripple rejection                         | - 80dB                                     |

**Circuit connection** The internal functional diagram and the basic circuit connection for the LM317 regulator are shown in Fig. 8.12(a) and (b) respectively. The LM317 needs two resistors  $R_1$  and  $R_2$  for setting the output voltage. Normally capacitors are not required. However, when the LM317 is placed more than 15cm apart from the output filter capacitor  $C_2$  of the power supply circuit, an input bypass capacitor,  $C_1$  of 0.1  $\mu$ F disc or 1  $\mu$ F tantalum is needed to be connected as shown in Fig. 8.12(b). An additional aluminium or tantalum electrolytic capacitor of range 1 to 1000  $\mu$ F may be connected at the output to improve the transient response characteristics. The unregulated voltage is applied at the terminal  $V_i$  of LM317 with respect to ground and it must be higher than the required regulated voltage  $V_o$ , by a value of at least 2V.

When the circuit is connected as shown in Fig. 8.12(b), the IC develops a typical value of *reference voltage*  $V_{ref} = 1.25V$ , between the output and adjustment terminals. This voltage appears across  $R_1$  resulting in a current flow of  $I_1 = \frac{V_{ref}}{R_1}$ .



(Contd.)



**Fig. 8.12** (a) LM317 voltage regulator functional diagram  
 (b) Circuit connection for LM317 regulator

This current also flows through  $R_2$  and an additional current of  $I_{ADJ}$  flows out of the adjustment terminal of the regulator through  $R_2$ . Thus the net current through  $R_2$  is  $I_2 = I_1 + I_{ADJ}$ .

The voltage across  $R_2$  is  $V_2 = I_2 R_2 = (I_1 + I_{ADJ}) R_2$ .

The net output voltage  $V_o$  is then given by

$$V_o = V_{ref} + V_2 = V_{ref} + R_2 (I_1 + I_{ADJ}) \quad (8.6)$$

Substituting  $I_1 = \frac{V_{ref}}{R_1}$  in the above equation,

$$V_o = V_{ref} \left( 1 + \frac{R_2}{R_1} \right) + I_{ADJ} R_2 \quad (8.7)$$

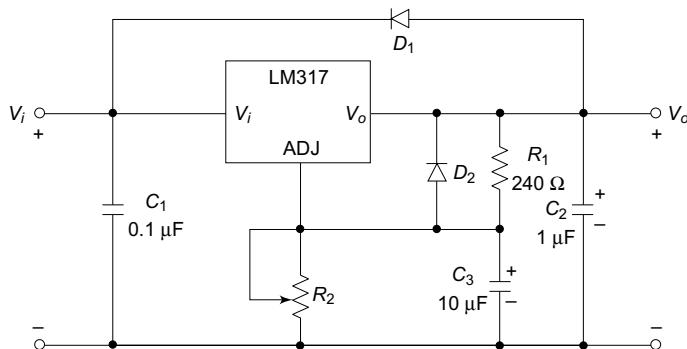
The last term  $I_{ADJ} R_2$  indicates an error term of a typical value of  $50 \mu\text{A}$ , and when  $R_2$  is low, this term can be neglected.

Then,

$$V_o = 1.25 \left( 1 + \frac{R_2}{R_1} \right) \quad (8.8)$$

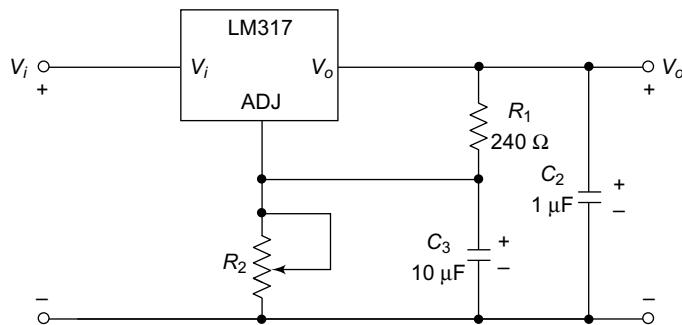
Hence, the output voltage  $V_o$  is a function of  $R_2$  for a specific value of  $R_1$ , which is normally  $240 \Omega$ . The resistor  $R_1$  is to be connected directly to the regulator output.

Protection diodes can be connected to the regulator circuit as shown in Fig. 8.13, when output capacitors of value greater than  $25 \mu\text{F}$  are used. The diode  $D_1$  prevents the capacitors from discharging into the regulator.



**Fig. 8.13** LM317 regulator with capacitors and protective diodes

Figure 8.14 shows the circuit arrangement of an adjustable positive voltage regulator using LM317. The operation of the circuit is explained in Example 8.5.



**Fig 8.14** LM317 adjustable positive voltage regulator

### Example 8.4

An LM317 regulator shown in Fig. 8.14 has  $R_1 = 240 \Omega$  and  $R_2 = 2k \Omega$ . If  $I_{ADJ} = 50 \mu A$  and  $V_{ref} = 1.25 V$ , find the value of  $V_o$ .

#### Solution

$$\begin{aligned} V_o &= V_{ref} \left( 1 + \frac{R_2}{R_1} \right) + I_{ADJ} R_2 \\ &= 1.25 \left( 1 + \frac{2000}{240} \right) + 50 \times 10^{-6} \times 2 \times 10^3 = 11.77 \text{ V} \end{aligned}$$

### Example 8.5

Referring to Fig. 8.14, design an adjustable positive voltage regulator using LM317 for an output voltage  $V_o$  varying from 4 to 12 V and an output current  $I_o$  of 1A.

**Solution** Maximum  $I_{ADJ}$  for LM317 = 100  $\mu A$

Assume a typical value of  $R_1 = 240 \Omega$ . Here,  $V_{ref} = 1.25 \text{ V}$

$$\text{We know that } V_o = V_{ref} \left( 1 + \frac{R_2}{R_1} \right) + I_{ADJ} R_2$$

For the output voltage  $V_o = 4 \text{ V}$ ,

$$4 = 1.25 \left( 1 + \frac{R_2}{240} \right) + 100 \times 10^{-6} \times R_2$$

Therefore,

$$R_2 = 0.52 \text{ k}\Omega$$

Similarly, for  $V_o = 12 \text{ V}$ ,

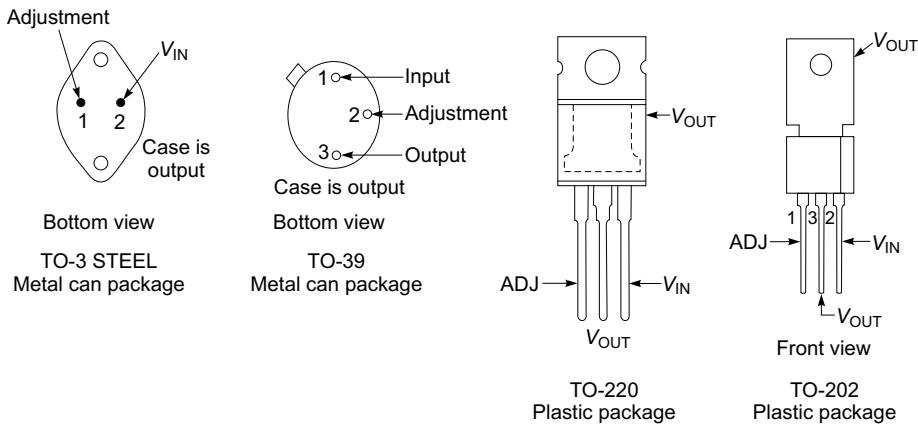
$$12 = 1.25 \left( 1 + \frac{R_2}{240} \right) + 100 \times 10^{-6} \times R_2$$

Therefore,

$$R_2 = \frac{10.75}{5.3 \times 10^{-3}} = 2.01 \text{ k}\Omega$$

Here,  $R_2$  is a variable resistor of range  $0.52 \text{ k}\Omega$  to  $2.01 \text{ k}\Omega$  for obtaining an output voltage of 4 to 12 V. Hence, a  $3 \text{ k}\Omega$  linear potentiometer can be used. For supplying a current of 1A, TO-3 package with 20W power dissipation capability can be employed. Since the output voltage is less than 25V, the protection diode between input and output terminals is not required. If the regulator is placed closer to output filter capacitor of the power supply, capacitor  $C_1$  is also not required. An output capacitor  $C_2$  of  $1 \mu\text{F}$  and an adjustment terminal capacitance  $C_3$  of value  $10 \mu\text{F}$  can be provided to improve rejection of transients and to increase impedance. Note that the input voltage range should obey the condition  $3V \leq (V_i - V_o) \leq 40V$ . Therefore, as a typical example, the input voltage must be  $\geq 15V$  to provide an output voltage of 12V.

Figure 8.15 shows the schematic symbols and package types. The three terminals are input terminal  $V_i$ , output terminal  $V_o$  and adjustment terminal (ADJ).



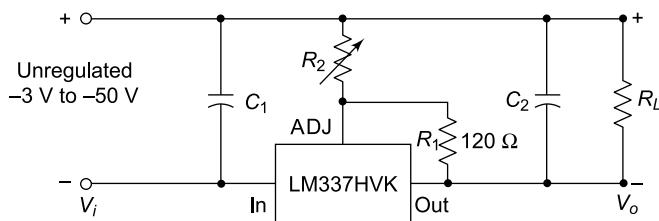
**Fig. 8.15** Schematic symbol and package types of LM117/LM317

### 8.5.2 LM137/LM337 Adjustable Negative Voltage Regulators

The LM137/LM337 series of adjustable three terminal negative voltage regulators are available for the corresponding types of LM117/LM317 positive voltage regulators. The circuit arrangement of LM337 connected for negative variable voltage regulation is shown in Fig. 8.16. Note that  $R_1$  is of value  $120 \Omega$  and maximum input voltage which can be fed to  $V_i$  terminal is 50 V as against 60 V for LM317. The output voltage  $V_o$  is given by

$$V_o = 1.2 \left( 1 + \frac{R_2}{R_1} \right) = 1.2 \left( 1 + \frac{R_2}{120} \right)$$

$$V_o = 1.2 \text{ V} + 10 \text{ mA} \times R_2$$

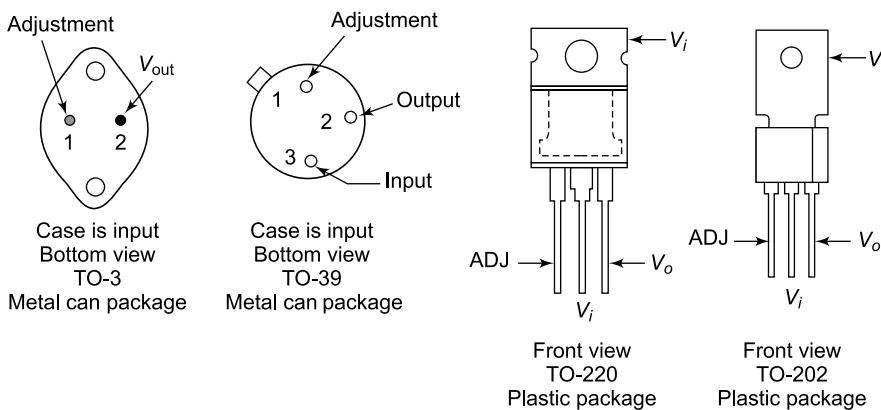


**Fig. 8.16** LM337 adjustable negative voltage regulator

Table 8.2 shows the package types and grades of LM337 regulators. Figure 8.17 shows the schematic symbols and package types of the negative voltage regulators. The three terminals are input terminal  $V_i$ , output terminal  $V_o$  and adjustment terminal (ADJ).

**Table 8.2** Different grades and packages of LM337 regulators

Device	Available $V_o$ (V)	Output Current (A)	$V_i$ Max (V)	Ripple Rejection (dB)	Package Type
LM337	-1.2 to -37	1.5	40	77	TO-39
LM337H	-1.2 to -37	0.5	40	77	TO-39
LM337HV	-1.2 to -37	1.5	50	77	TO-3
LM337HVH	-1.2 to -37	0.5	50	77	TO-39
LM337L	-1.2 to -37	0.1	40	65	TO-92
LM337M	-1.2 to -37	0.5	40	77	TO-202



**Fig. 8.17** Schematic symbol and package types of LM137/LM337

### 8.5.3 Low Drop-Out (LDO) Regulator

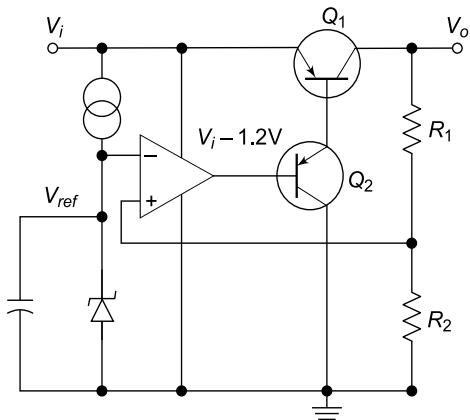
The disadvantage of the typical 78XX series and LM317 type of regulators is that the devices require a minimum voltage  $V_{DO}$ , called the drop-out voltage. This is the minimum voltage difference between input and output terminals needed to regulate the supply voltage within the specifications. To cite an example, the IC  $\mu$ A7805 with  $I_o = 1\text{A}$  needs  $V_{DO} = 2.5\text{V}$  maximum. This indicates that the minimum unregulated input voltage  $V_i$  must never be less than  $V_{i,min} = V_{ref} + V_{DO} = 5\text{V} + 2.5\text{V}$ . Similarly, the LM317 type of regulator needs at least 3 V between the input and output leads to produce power to the internal circuits. Hence, in typical applications, involving batteries whose voltage can easily drop from 12 V to as low as 6 V such as the case of a car battery, the dropout voltage is a detrimental factor.

The LDO regulator shown in Fig. 8.18 is ideal for such applications. This is a simple modification of the LM317 circuit shown in Fig. 8.12(a). It employs a *PNP* BJT as the series element to drive the output. The second *PNP* transistor  $Q_2$  buffers the error amplifier output. The op-amp output is maintained at  $V_i - 1.2\text{V}$ . The voltage at the junction of resistors  $R_1$  and  $R_2$  is fed to the non-inverting input of error amplifier. When this voltage is more than the reference voltage set by the Zener diode, the output of the op-amp goes positive. This reduces the base current of transistor  $Q_2$ , which in turn reduces the base current drive to series element  $Q_1$ . Thus, the circuit realises a minimum voltage of about 0.2 V, being the  $V_{EC(sat)}$  voltage between  $V_i$  and  $V_o$  terminals. It is noted that the transistor base drive from the op-amp is relative to the input voltage  $V_i$ . On the other hand, the base drive of Fig. 8.12(b) was realised in relation to  $V_o$ .

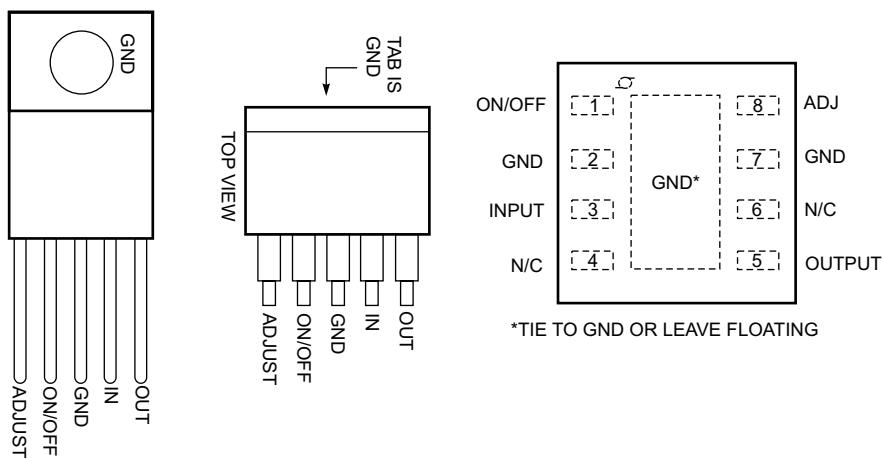
The IC LM2941 is a typical low drop-out positive voltage regulator. It can source an output current of 1 A with a typical dropout voltage of 0.5 V and a maximum of 1 V over the entire temperature range. This IC has a quiescent current reduction circuit which reduces the ground terminal current if the differential voltage across the input and output terminals exceeds approximately 3 V. The quiescent current is only 30 mA while providing with 1 A of output current and an input to output differential voltage of 5 V. Higher quiescent currents exist only when the regulator is in the drop-out mode ( $V_i - V_o \leq 3\text{V}$ ). As pointed out earlier, these types of regulators are mainly used for vehicular applications.

The LM2941 is protected from reverse battery installations or two-battery jumps. During accidental line transients or when the input voltage momentarily exceed the specified maximum operating voltage, the regulator will automatically switch to shut-down mode. This protects both the internal circuits and the load. Furthermore, the short circuit and thermal overload protection features are also provided.

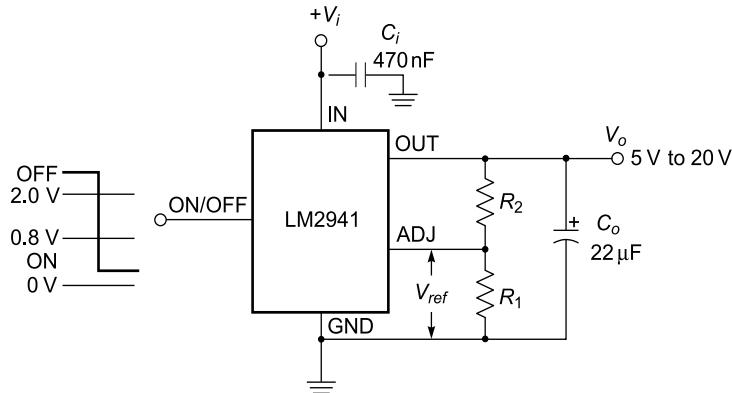
Figure 8.19(a) shows the To-220 plastic, To-263 and 8-lead LLP surface mount packages. Figure 8.19(b) shows a typical regulator circuit using LM2941 to provide a regulated output voltage of 5 V to 20 V.



**Fig. 8.18** Low drop-out positive voltage regulator



**Fig. 8.19(a)** TO-220 Plastic, TO-263 and 8-Lead LLP surface mount packages



$$V_o = V_{ref} \left[ 1 + \frac{R_2}{R_1} \right] \text{ where } V_{ref} = 1.275 \text{ V (Typical)}$$

$$R_2 = R_1 \left( \frac{V_o}{V_{ref}} \right) - 1$$

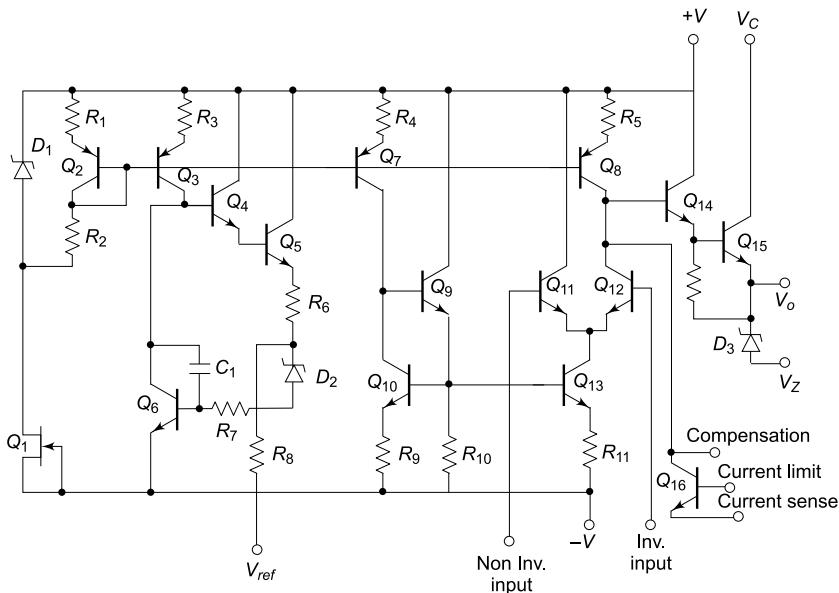
**Fig. 8.19(b)** 5 V to 20 V regulator circuit using LM2941

## 8.6 IC 723 GENERAL PURPOSE REGULATOR

The three-terminal regulators such as 7805, 7815, 7905, 7915, etc. are capable of producing only fixed positive, or negative output voltages. Moreover, such regulators do not have short circuit protection. Therefore, these three terminal regulators evolved into dual polarity variable voltage regulators. They have provision for regulating positive and negative voltage inputs. The evolution further led to the monolithic linear voltage regulators and monolithic switching regulators. The monolithic linear voltage regulator type IC 723 is discussed in this section.

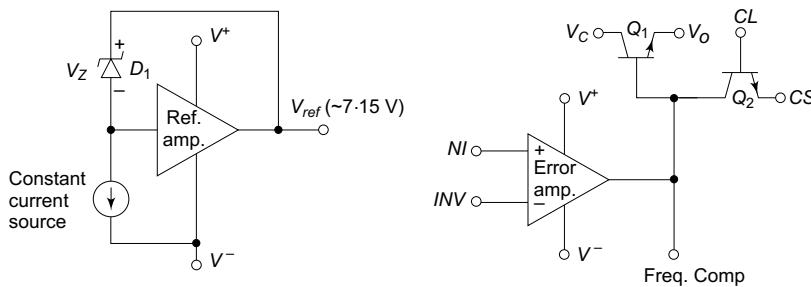
The IC 723 general purpose regulator overcomes the limitations of three terminal fixed voltage regulators. The IC 723 is a low current device, and can be employed for providing a load current up to 10 A or more by the addition of external transistors.

Figure 8.20 shows the detailed internal circuit diagram of IC 723. It consists of a temperature compensated Zener diode  $D_1$ , biased with a constant current source. The reference voltage  $V_{ref}$  is available from a buffer amplifier realised by transistors  $Q_1$  through  $Q_6$  and Zener diodes,  $D_1$  and  $D_2$ . The  $V_{ref}$  has a typical value of 7.15 V. The series-pass element is realised by Darlington-connected transistors  $Q_{14}$  and  $Q_{15}$ . They boost the output current of the regulator to a value of 150 mA. The terminals  $+V$  and  $V_c$  are accessible externally. Current limit protection is provided by the transistor  $Q_{16}$ . The *sense voltage* is the voltage drop obtained across a suitable resistor connected between the terminals *current limit* (CL) and *current sense* (CS) of the IC 723. Transistors  $Q_7$  through  $Q_{13}$  and resistors  $R_{10}$  and  $R_{11}$  form the error amplifier. The transistors  $Q_{11}$  and  $Q_{12}$  with their non-inverting and inverting input terminals produce a differential amplifier. The transistor  $Q_{13}$  acts as the current source for the differential amplifier.

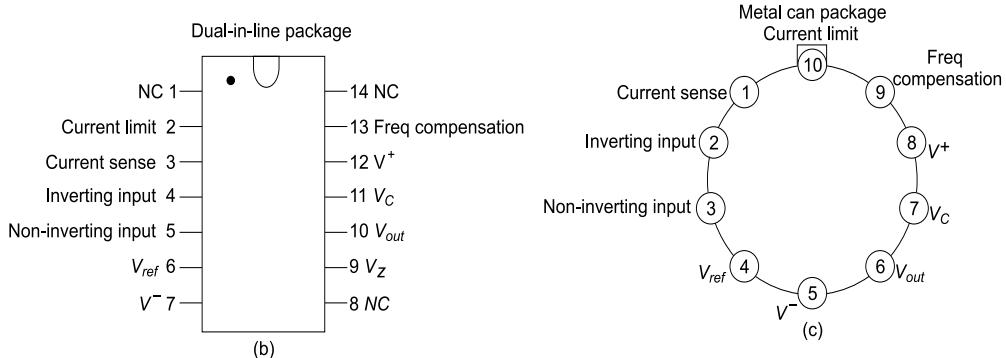


**Fig. 8.20** IC 723 Regulator internal circuit diagram

The functional block diagram of IC 723 is shown in Fig. 8.21 (a). Figures 8.21 (b) and (c) show the pin diagrams for a 14-pin DIP and 10-pin Metal Can packages for the device. The Zener diode, the constant current source and reference amplifier form one section of the IC. The constant current source helps in maintaining a fixed output voltage from Zener diode  $D_2$ . The error amplifier, series pass element  $Q_1$  and current limit transistor  $Q_2$  form the second section. The error amplifier compares the input voltages applied at non-inverting (NI) and inverting (INV) input terminals. The error signal obtainable at the output of error amplifier drives the series pass element  $Q_1$ .



**Fig. 8.21 (a)** Functional block diagram of IC 723

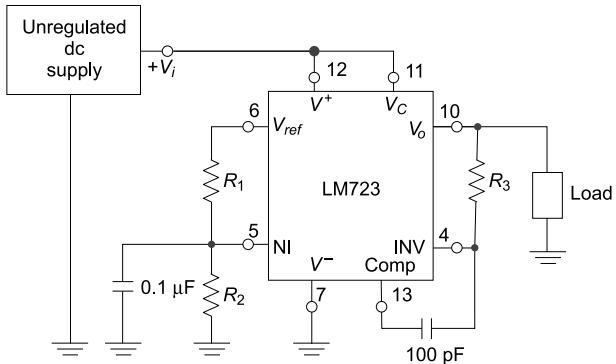


**Fig. 8.21 (b)** Pin diagram of 14-pin DIP **(c)** Pin diagram of 10-pin Metal Can packages

### 8.6.1 Low Voltage Regulator using IC 723

Figure 8.22 shows the functional block diagram for a low voltage regulator using IC 723. This circuit arrangement is used for regulating voltages ranging from 2V to 7V, and hence it is called a low voltage regulator. The output voltage is directly fed back to the INV input terminal. The non-inverting input (NI) is obtained across the potential divider formed by resistor  $R_1$  and  $R_2$ . Hence, voltage at NI terminal is given by

$$V_{NI} = V_{ref} \times \frac{R_2}{R_1 + R_2}$$



**Fig. 8.22** Functional block diagram of a low voltage regulator using IC 723

The error amplifier amplifies the difference and it drives the pass transistor  $Q_1$ . Depending on the error signal, the pass transistor  $Q_1$ , acting as control element, minimises the difference between the NI and INV inputs of error amplifier. Therefore, the output voltage  $V_o$  is given by

$$V_o = V_{ref} \times \frac{R_2}{R_1 + R_2} = 7.15 \times \frac{R_2}{R_1 + R_2}.$$

Now, assuming that the output voltage is low, the INV terminal input goes down, making the output of error amplifier more positive. This drives the NPN pass transistor further into conduction. Hence, higher current is driven into the load, thereby causing the output voltage to increase. This compensates for the drop in output voltage. In a similar manner, any rise in load voltage gets regulated.

### 8.6.2 High Voltage Regulator Circuit using IC 723

The IC 723 can be used for designing a high voltage regulator for output voltages ranging from 7V to 37V. The circuit connection diagram is shown in Fig. 8.23. The non-inverting input (NI) terminal is directly connected to  $V_{ref}$  through  $R_3$ . The inverting input (INV) terminal is connected to the junction of resistors  $R_1$  and  $R_2$  connected with the output  $V_o$ . The resistor  $R_3$  is selected to be equal to  $R_1 \parallel R_2$ . Then the error amplifier acts as a noninverting amplifier with a voltage gain

$$\text{of } A_V = 1 + \frac{R_1}{R_2}.$$

Therefore, the output voltage for the circuit is

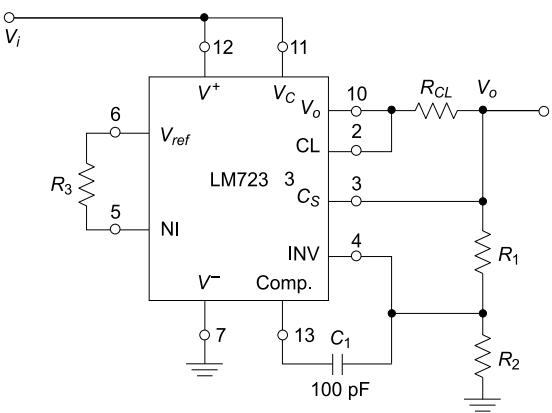
$$V_o = V_{ref} \left( 1 + \frac{R_1}{R_2} \right) = 7.15 \left( 1 + \frac{R_1}{R_2} \right)$$

### 8.6.3 Current Limit Protection

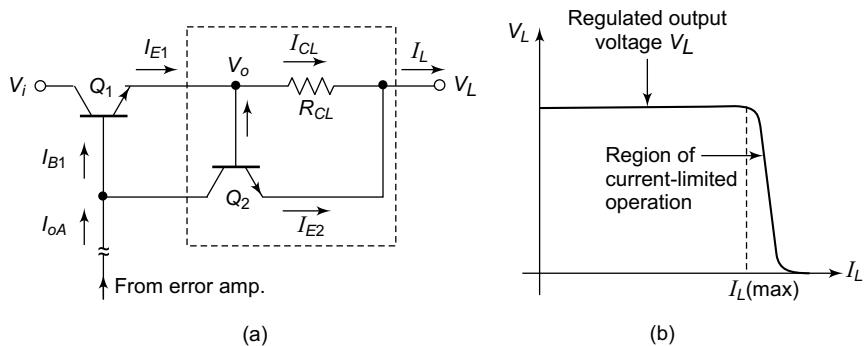
The limitation of the regulator IC 723 is that it has no built-in thermal protection and short circuit protection. Therefore, the current limit protection in regulator ICs is necessary for providing protection against short circuit condition across the load. The low-pass and high-pass regulator circuits discussed in the previous sections have no in-built current limit protection circuit.

An active current limiting circuit for IC 723 is shown in Fig. 8.24(a). This circuit prevents the load current from increasing beyond a safe value. The operation of the circuit can be explained as follows. The series pass element  $Q_1$ , which is part of the regulator circuit, is shown connected in series with a current limiting resistor  $R_{CL}$ . The voltage drop across the resistance  $R_{CL}$  can bias the transistor  $Q_2$  and turn it ON. Assume that the circuit can supply a maximum current of  $I_{L(\max)}$ . The output voltage remains constant for any value of  $I_{CL}$  up to the maximum current  $I_{CL(\max)}$ . In such normal load conditions, the voltage  $V_{CL}$  across the resistor  $R_{CL}$  (i.e.,  $V_{CL} = I_{CL} \times R_{CL}$ ) is insufficient to turn transistor  $Q_2$  ON. Therefore,  $Q_1$  supplies the current demanded by the load conditions at the fixed output voltage  $V_L$ . Now, consider that the load current  $I_L$  increases. This leads to more current through  $R_{CL}$ , and the voltage drop  $V_{CL}$  increases too. This turns the transistor  $Q_2$  ON. Hence, any current, which is in excess of  $I_{L(\max)}$  is diverted away from the base of  $Q_1$ . This effectively reduces the emitter current of  $Q_1$ , and thus the load current reduces. Similarly, when the load current reduces, the drop across  $R_{CL}$  drops, turning  $Q_2$  OFF and allowing  $Q_1$  to pass  $I_L$ .

The curve shown in Fig. 8.24(b) shows the output characteristics of series-pass voltage regulator using such a simple current limiting method. The transistor  $Q_2$  supplies an additional small amount of current to the load when the current limiting takes place.



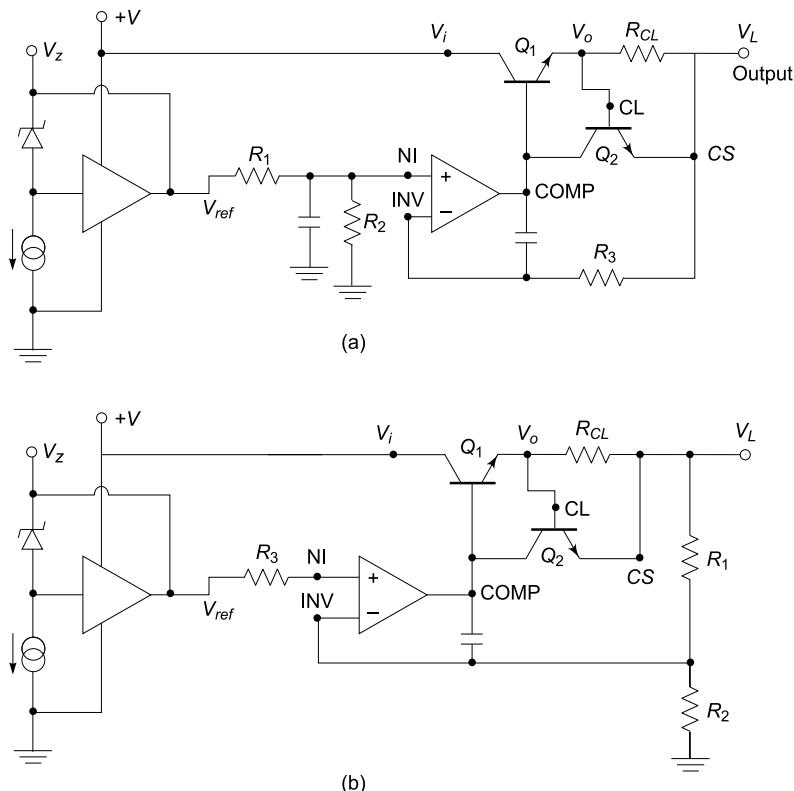
**Fig. 8.23** Functional block diagram of a high voltage regulator using IC 723



**Fig. 8.24** (a) Current limiting circuit (b) Its output characteristics

Figures 8.25 (a) and (b) show the two basic configurations of IC 723 for low voltage and high voltage regulations with current limiting capability. The power dissipation  $P_D$  in the regulator IC mainly occurs in the transistor  $Q_2$  and thus,

$$P_D = V_{CE2} \times I_{C2} = (V_i - V_L) I_L$$



**Fig. 8.25** (a) Current limiting circuit for low voltage regulator ( $V_o < 7.15$  V) (b) Current limiting circuit for high voltage regulator ( $V_o > 7.15$  V)

When the output is accidentally shorted, the worst case power dissipation will occur. Then, the maximum allowable power dissipation,  $P_{D(\max)} = I_{L(\max)} V_{i(\max)}$ .

### **Example 8.6**

---

Referring to Fig. 8.25(b), assume the output voltage,  $V_L = 20\text{ V}$ .

- (i) What value of  $R_{CL}$  is to be used for limiting the maximum current at 0.5 A.
- (ii) With the value of  $R_{CL}$ , find the output voltage from the regulator when  $R_L = 100\text{ }\Omega$ .
- (iii) Comment on the operation of the circuit for  $R_L = 10\text{ }\Omega$ .

**Solution** Given  $I_{L(\max)} = 0.5\text{ A}$

$$(i) \text{ We know that, } I_{L(\max)} = \frac{0.7}{R_{SC}}$$

$$\text{Therefore, } R_{SC} = \frac{0.7}{I_{L(\max)}} = \frac{0.7}{0.5} = 1.4\text{ }\Omega$$

- (ii) Given the load  $R_L = 100\text{ }\Omega$

$$\text{Then, } I_L = \frac{20}{100} = 0.2\text{ A}$$

The maximum current obtainable from the circuit is given as 0.5 A. Since  $I_L < I_{L(\max)}$ , the output voltage will stay at 20 V.

- (iii) If load  $R_L = 10\text{ }\Omega$ , then

$$I_L = \frac{20}{10} = 2\text{ A}$$

Since  $I_L$  of 2 A  $> I_{L(\max)}$  of 0.5 A, current limiting will happen. The output voltage will therefore be,

$$V_o = R_L \times I_{L(\max)} = 10 \times 0.5 = 5\text{ V}$$

### **Example 8.7**

---

Design a +12 V regulator using LM723, with a current limiting value of 50 mA.

**Solution** The basic circuit for obtaining +12V is shown in Fig. 8.20. The appropriate output equation is

$$V_o = V_{ref} \left[ 1 + \frac{R_1}{R_2} \right]$$

Choosing an arbitrary standard value for  $R_2$  of  $10\text{ k}\Omega$ , and solving for  $R_1$ , we get

$$\begin{aligned} R_1 &= \left( \frac{V_o}{V_{ref}} \right) R_2 - R_2 \\ &= \left( \frac{12}{7.15} \right) 10 \times 10^3 - 10 \times 10^3 = 6.78\text{ k}\Omega \end{aligned}$$

#### **8.6.4 Foldback Current Limiting**

In the simple current limiting circuit discussed earlier, the maximum current limit was preset such that the power  $P_D$  will never be more than the value set by  $P_D = V_L I_{L(\max)}$  and the resistance  $R_{CL}$  was accordingly chosen. The net effect is that the regulator is under-utilised. In such conditions, the current foldback method provides full protection to the device, in addition to allowing higher currents to the load.

Figure 8.26(a) shows the foldback current limiting characteristics in comparison with the linear foldback method of Fig 8.24(b). The foldback current limiting method reduces both the output current and voltage when  $I_{L(\max)}$  is reached.

The foldback current limiting circuit is shown in Fig. 8.26(b). This method of over-current protection is employed to reduce both the output load current and voltage, when the load resistance becomes smaller than what would draw a specified maximum current of  $I_{L(\max)}$ . In the current limit protected regulator, as  $I_{L(\max)}$  is exceeded, the output voltage of the regulator decreases. On the other hand, in foldback current limiting, as load resistance decreases beyond a certain minimum value, both load voltage and load current decrease, and when the load becomes a short circuit, they approach zero.

The important advantages of foldback method of current limiting are (a) protecting the load from the over-current operation and (b) protecting the regulator itself. The base of  $Q_3$  is connected to the voltage divider formed by  $R_3$  and  $R_4$ . Applying Kirchhoff's voltage law around the loop, we get

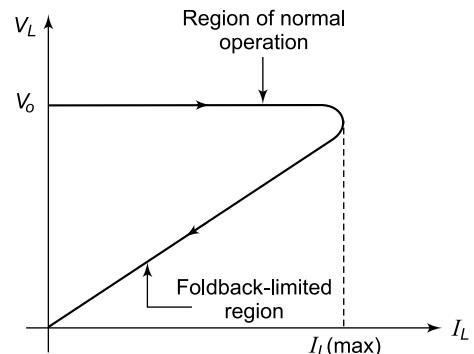
$$V_{BE} = V_{CL} - V_R \approx$$

The current limit transistor  $Q_3$  starts conducting only when its base to emitter voltage  $V_{BE}$  is approximately 0.7 V, that is,  $V_{CL}$  must become sufficiently large to exceed the drop across  $R_3$  by a minimum of 0.7 V.

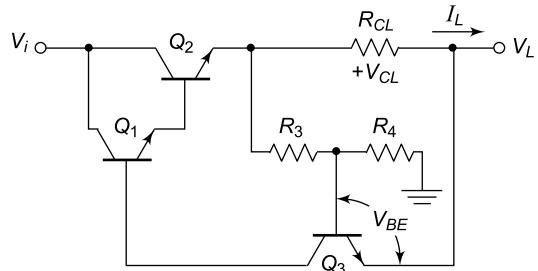
That is,

$$0.7 = V_{BE} = V_{CL} - V_{R3}$$

At this point, current limit starts occurring. As the load resistance decreases, the load voltage drops, and  $V_{R3}$  also reduces. As a consequence, a smaller value of  $V_{CL}$  is then required to maintain  $V_{BE}$  of  $Q_3$  at 0.7 V. Then, as transistor  $Q_3$  starts conducting, transistor  $Q_1$  starts to turn OFF, and the load current decreases. The drop across  $R_3$  further reduces, increasing the conduction of  $Q_3$  and reducing the conduction of  $Q_1$ . The load current  $I_L$  further reduces. This process continues until  $V_o$  becomes 0 V and load current becomes a minimum. If the load resistance is brought to its nominal operating value, the circuit resumes its normal regulation action.



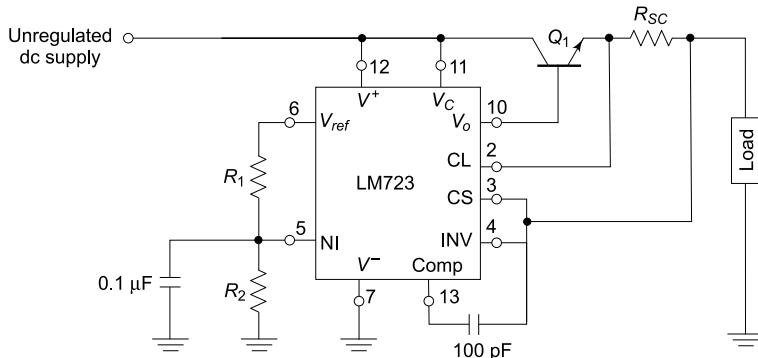
**Fig. 8.26** (a) Foldback current limit characteristics



**Fig. 8.26** (b) Foldback current limiting circuit

### 8.6.5 High Current Low Voltage Regulator

The maximum current obtainable from IC 723 is 140 mA. For applications requiring higher current values, boost pass transistor  $Q_1$  can be added to the regulator as shown in Fig. 8.27. The collector of  $Q_1$  is connected to unregulated dc supply. The output terminal  $V_o$  of regulator drives the base of  $Q_1$ . Therefore,  $I_o = \beta_{\text{Boost transistor}} \times I_{o(723)}$ . A Darlington connected transistor pair can also be used in place of  $Q_1$  as the pass transistor for obtaining much higher values of load currents.



**Fig. 8.27** Low voltage regulator circuit with current boosting

### Example 8.8

Design a continuously adjustable power supply for the range of 2 V to 5 V with a current limit of 1A using IC LM723.

**Solution** The adjustable voltage regulator for high current is shown in Fig. 8.25. The output voltage is given by

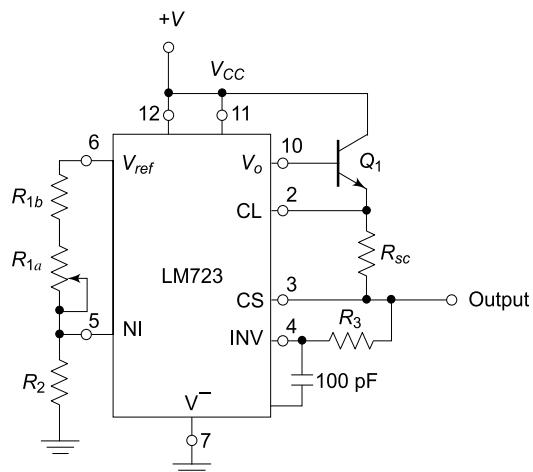
$$V_o = V_{ref} \frac{R_2}{R_1 + R_2}$$

In order to produce a 1A load current, an external pass transistor  $Q_1$  is employed. To obtain the desired voltage adjustment, resistor  $R_1$  is replaced with a series potentiometer/resistor combination ( $R_{1a}, R_{1b}$ ) as shown in Fig. 8.28. Here, the minimum and the maximum values of  $R_1$  will be  $R_{1b}$  and  $(R_{1a} + R_{1b})$  respectively. Then the three resistors are in series and act as a potential divider. Therefore,

$$\frac{R_1 + R_2}{R_2} = \frac{V_{ref}}{V_o}$$

For the maximum voltage of 5V, we have

$$\frac{R_{1b} + R_2}{R_2} = \frac{V_{ref}}{V_o} = \frac{7.15}{5} = 1.43$$



**Fig. 8.28** Adjustable voltage regulator using LM723

Therefore,  $R_{1b} = 0.43 R_2$

For the minimum voltage of 2V, we have

$$= \frac{R_{1a} + R_{1b} + R_2}{R_2} = \frac{V_{ref}}{V_o} = \frac{7.15}{2} = 3.575$$

Substituting  $R_{1b} = 0.43 R_2$  in the above equation, we get

$$R_{1a} = 2.145 R_2$$

Choosing a standard value of  $10\text{ k}\Omega$  for  $R_{1a}$ ,

$$R_2 = \frac{R_{1a}}{2.145} = \frac{10 \times 10^3}{2.145} = 4.66\text{ k}\Omega$$

Similarly,  $R_{1b} = 0.43 R_2 = 0.43 \times 4.66 \times 10^3 = 2\text{ k}\Omega$

For choosing a suitable current sense resistor  $R_{sc}$ ,

$$I_{limit} = \frac{V_{sense}}{R_{sc}}$$

$$R_{sc} = \frac{V_{sense}}{I_{limit}} = 0.65\Omega$$

For minimum temperature drift,  $R_3$  is included as given by

$$R_3 = R_1 \parallel R_2 = 6\text{ k}\Omega \parallel 4.66\text{ k}\Omega = 2.62\text{ k}\Omega$$

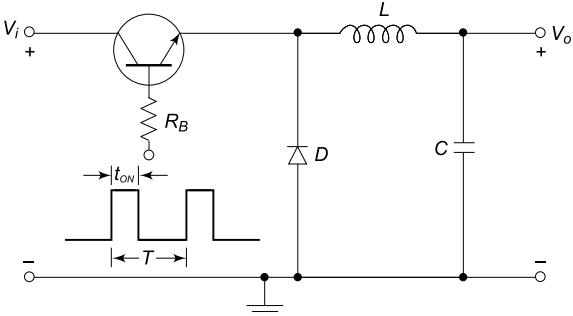
## 8.7 SWITCHED MODE POWER SUPPLIES (SMPS)

The linear voltage regulators have the following limitations:

- (i) The step-down transformer used in the power supply circuit is bulky and it is the most expensive component of the circuit.
- (ii) Large values of filter capacitors are required to eliminate ripples, due to the low line frequency (50 Hz) of operation.
- (iii) The efficiency of series regulator is normally less than 50%.
- (iv) The input voltage must be always more than the required output regulated voltage.
- (v) The difference between the input and output voltage drops across the linear pass transistor and dissipates power.

The switched mode regulators overcome these limitations. They operate on the principle of chopping the unregulated dc supply voltage by the use of a transistor switch and filtering the high frequency components using a high frequency filter. Thus, the output voltage is regulated by varying the duty cycle or the switching period of the transistor.

Figure 8.1(b) of Section 8.1 depicted the operating principle of a practical switching regulator in its simplest form. The elements



**Fig. 8.29** Principle of a switching regulator

added in addition to the components of an unregulated power supply circuit are the control logic and the oscillator circuits. The oscillator allows the control element to be switched ON and OFF. The control element usually consists of a transistor switch, an inductor and a diode as shown in Fig. 8.29. For each switching ON at the base of the transistor, energy is pumped into the magnetic field associated with the inductor which is a transformer winding in practice. This energy is then released to the load at the desired voltage level. By varying the duty cycle or frequency of switching, one can vary the stored energy in each cycle and thus control the output voltage. As a switch can only be ON or OFF, it either allows energy to *pass* or *stop*, but does not itself dissipate energy. Since only the energy required to maintain the output voltage at a particular load current is drawn, there is no dissipation and hence, a higher efficiency is obtained. Energy is pumped in discrete lumps, but the output voltage is kept constant by capacitor storage.

The major feature of SMPS is the elimination of physically massive power transformers and other power line magnetics. The net result is a smaller, lighter package and reduced manufacturing cost, resulting primarily from the elimination of the 50 Hz line frequency components.

However, the switching regulators suffer from the disadvantages as given below:

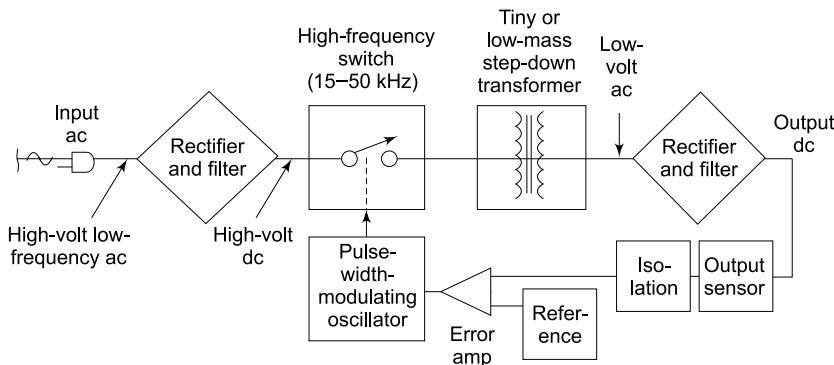
- (i) In a switching regulator, noise is high on both ac input and output lines due to switching at high frequencies. As a result, heavy filtering is required.
- (ii) Since the transient response is limited, switching regulator is normally slower than linear voltage regulator.
- (iii) Switching regulator is more complex compared to a linear regulator.

Due to these limitations, the switching regulators are used for high power levels of around 100 W.

The switched mode regulators can be classified into three categories based on the switching and filtering functions of the circuit, namely, (i) Transformer based type, (ii) Buck switched type, and (iii) Boost switched type.

### 8.7.1 Transformer based Switching Regulator

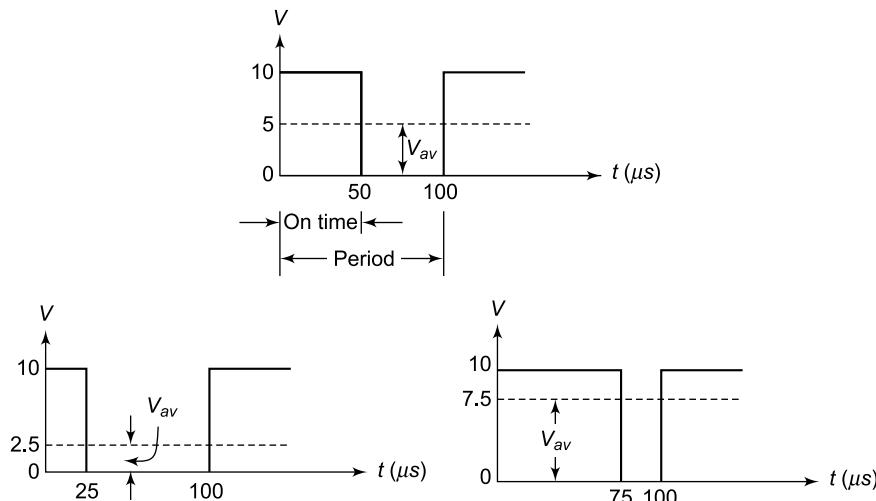
The block diagram of transformer based switching regulator is shown in Fig. 8.30(a). Here, the primary power received from the ac main is rectified and filtered as high voltage dc. It is then switched at a high speed of approximately 15 kHz to 50 kHz and fed to the primary side of a step-down transformer. The step-down transformer is only a fraction of the size of a comparable 50 Hz unit thus relieving the size and weight problems. The output from the secondary side of the transformer is rectified and filtered. Then, it is sent as the output of the power supply. A sample of this output is sent back to the switch to control the output voltage.



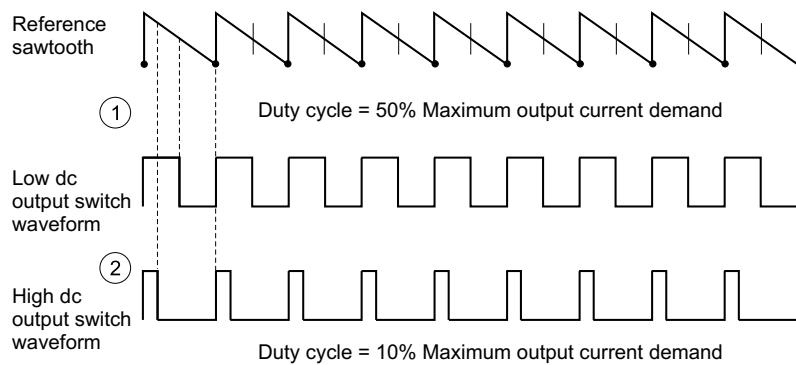
**Fig. 8.30 (a)** Block diagram of switching power supply

SMPS rely on PWM to control the average value of the output voltage. The average value of the respective pulse waveform depends on the area under the waveform. If the duty cycle is varied as illustrated in Fig. 8.30(b), then the average value of the voltage changes proportionally.

As the load increases, the output voltage tends to fall. Most switching power supplies regulate their output using a method called *pulse-width modulation* (PWM). The power switch which feeds the primary side of the step-down transformer is driven by a pulse-width modulated oscillator. When the duty cycle is 50%, the maximum amount of energy will be passed through the step-down transformer. As the duty cycle is decreased, less energy will be passed through the transformer.



**Fig. 8.30 (b) Pulse width modulation and average value**

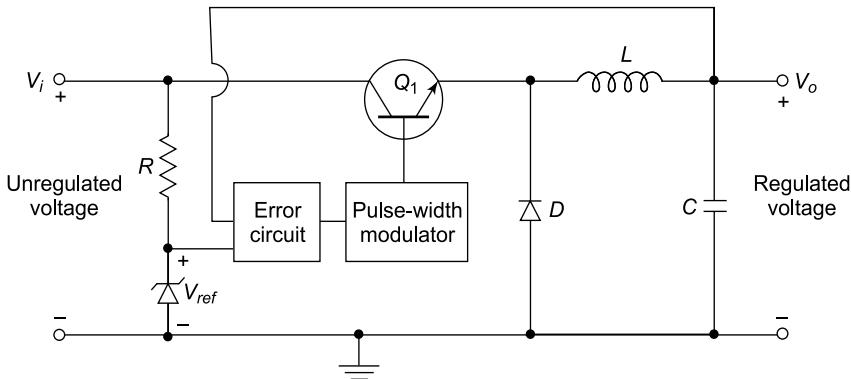


**Fig. 8.30 (c) Switching power supply waveforms**

The width or ON time of the oscillator is controlled by the voltage fed back from the secondary rectifier output forming a closed loop regulator. As shown in Fig. 8.30(c), the pulse width applied to the power switch is inversely proportional to the output voltage. When the output voltage drops, the switch is ON for a longer time, resulting in more energy delivered to the transformer and a higher output voltage. As the output voltage increases, the ON time becomes shorter until the loop stabilises.

### 8.7.2 Bucking (Step-down) Switching Regulator

Figure 8.31 shows the basic diagram of a *step-down* or *bucking* switching regulator circuit. The input voltage  $V_i$  is a dc voltage. A pulse train is applied to the base of the control transistor  $Q_1$ , and the transistor acts as a switch, alternating between its *cut-off* and *saturation* regions. When the transistor is ON, the diode  $D$  gets reverse biased. When the transistor is OFF, it becomes forward biased providing a continuous path for the *inductive* current. The LC filter functions as a smoothing circuit for the input variations that provides a steady dc output voltage.



**Fig. 8.31** Basic diagram of a step-down (Bucking) switching regulator circuit

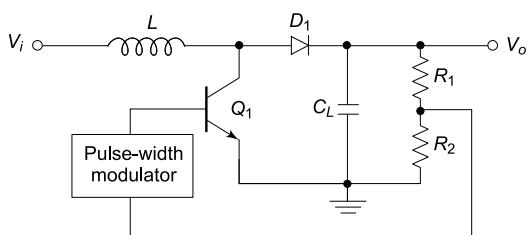
When the transistor  $Q_1$  is turned ON and OFF for equal time durations, i.e. when duty cycle  $D$  of the pulse train is 50%, the dc output voltage  $V_o$  is given by  $V_o = \left( \frac{t_{ON}}{T} \right) V_i = 0.5 V_i$ . Note that the voltage drop across transistor and diodes are neglected. A typical switching frequency for the transistor is several kHz.

The reference voltage  $V_{ref}$  is obtained from the unregulated input voltage with the use of a Zener diode. The error circuit compares the regulated output voltage with the  $V_{ref}$  voltage. The output of the error circuit operates the pulse width modulator. The pulse width modulator generates pulses at a fixed frequency and the width of the pulses is dependent on the control voltage from the error circuit.

When the dc output voltage falls below the reference voltage, the error signal is generated in the error circuit. This causes the width of the pulses to increase, thus increasing the output voltage. If the output voltage is more than the reference voltage, the error signal reduces the pulse width which results in reducing the output voltage. Thus the constant output voltage is maintained.

### 8.7.3 Step-up (Boosting) Switching Regulator

The basic circuit of a boosting or step-up switching regulator is shown in Fig. 8.32. The voltage induced in the inductor is made to add-up to the input voltage. Thus, the resulting output voltage is more than the input voltage. Here, assuming that  $Q_1$  is initially ON, the voltage from the inductor promotes current

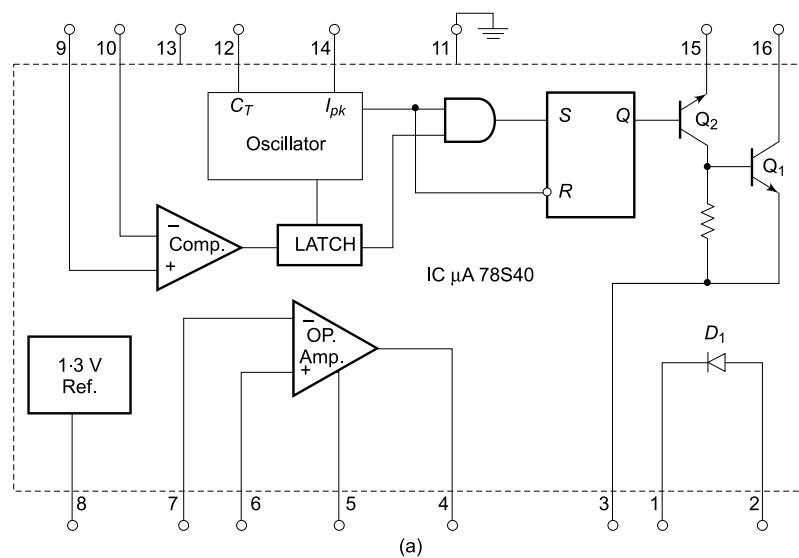


**Fig. 8.32** Basic diagram of a step-up (Boosting) switching regulator circuit

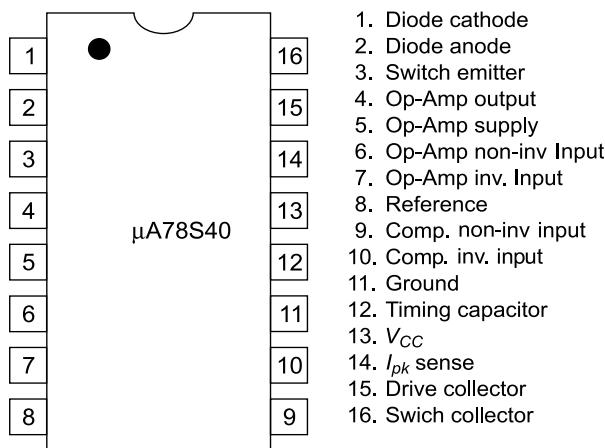
through this element. The diode  $D_1$  is OFF since  $V_D > V_{CE(sat)}$  of  $Q_1$ . When the transistor  $Q_1$  is OFF, the collapsing magnetic field of inductor  $L$  forward biases the diode  $D_1$ . Then, the voltage across inductor  $L$ (i.e.,  $V_L = LdI_L/dt$ ) adds to the voltage  $V_i$  which makes the output greater than  $V_i$ .

## 8.8 MONOLITHIC SWITCHING REGULATOR CIRCUIT

Since the switching regulator circuit is complex, modern IC packages like Motorola MC3420/3520 or Silicon General SG1524 can be used instead of discrete components. The IC  $\mu\text{A}78\text{S}40$  from Fairchild is a universal switching regulator. It is a pulse width modulated type of switching regulator. The internal block diagram and pin configuration of IC  $\mu\text{A}78\text{S}40$  are shown in Fig. 8.33(a) and (b) respectively.



(a)



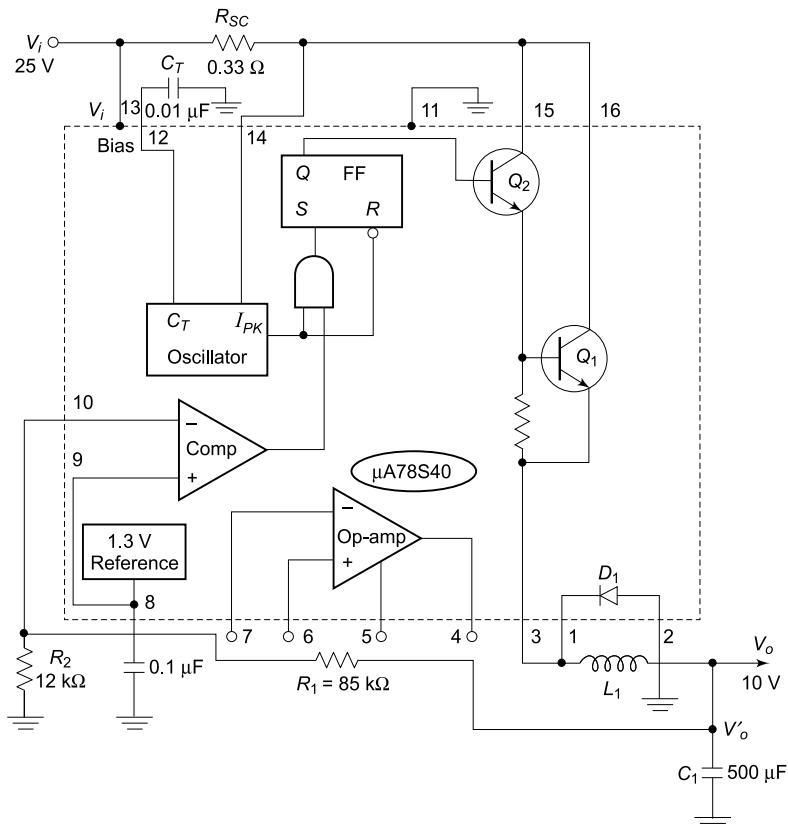
(b)

**Fig. 8.33** (a) Internal block diagram of IC  $\mu\text{A}78\text{S}40$  (b) Pin configuration

It consists of a temperature compensated voltage reference circuit, an oscillator, a high gain comparator, high current and high voltage output switch, a power switching diode  $D_1$  and an op-amp. The reference voltage is available at pin 8. The oscillator is controllable for its duty cycle with the use of an active current-limit circuit. The internal switching frequency of oscillator is set by the timing capacitor  $C_T$ , connected between Pin 12 and ground (pin 11). The initial duty cycle (6 : 1) can be modified by the current limit circuiting which is activated at pin 14 ( $I_{PK}$ ) and comparator outputs controlled by Pins 9 and 10. The typical frequency range of oscillator is between 100 Hz and 100 kHz.

The output transistor can operate at 40 V and supply current up to 1.5 A. The transistor  $Q_2$  operated by the output of SR flip-flop drives the base of  $Q_1$ . The transistors  $Q_1$  and  $Q_2$  can be connected as a Darlington pair. Increased base drive to  $Q_1$  can be applied by connecting an external resistor with  $Q_2$ . The oscillator output is connected to the flip-flop (FF) through an AND gate. The comparator is a high gain amplifier and the unconnected op-amp can be used for voltage polarity changes, when required.

The connection diagram of  $\mu$ A78S40 for step-down switching regulation is shown in Fig. 8.34. The output of comparator determines the OFF time of the switching transistors  $Q_1$  and  $Q_2$ . The voltage reference of 1.3 V is applied to non-inverting input (pin 9) of the comparator. The output voltage  $V'_o$  dropped across the potential divider network consisting of  $R_1 - R_2$  is fed to the inverting input (pin 10) of the comparator.



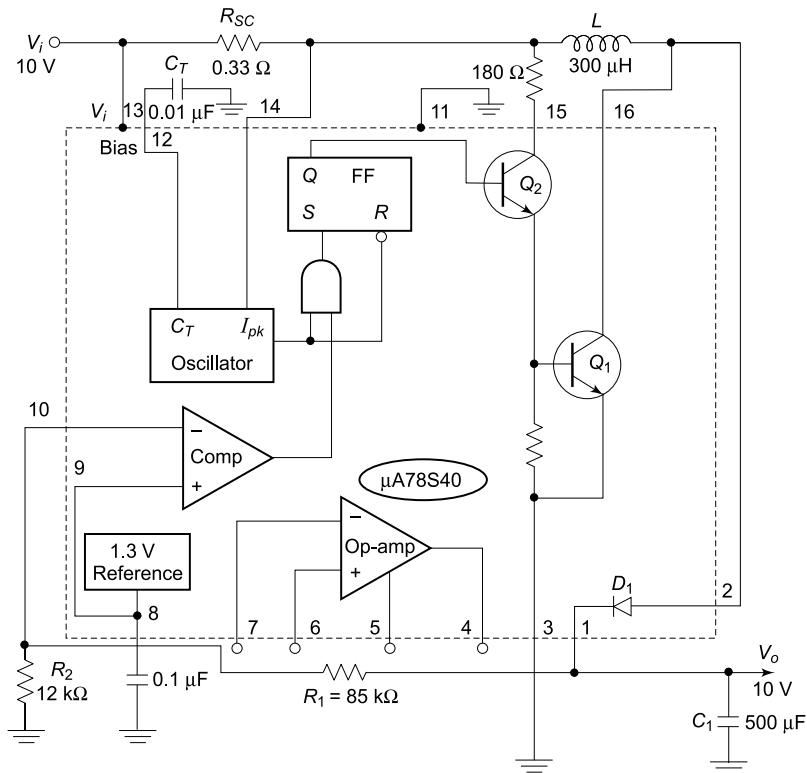
**Fig. 8.34** Step-down regulator using  $\mu$ A78S40

When the output is at the desired voltage level, the comparator output is high and no effect on the circuit operation is observed. Assume that the output voltage is more than the required value. Then, the voltage at the inverting input of comparator is higher than  $V_{ref}$ , and the comparator switches to negative saturation, and this is applied to one input of the AND gate through the latch. This makes output of AND gate low and  $Q_1$  is turned OFF. When the capacitor  $C_T$  times out, the oscillator turns  $Q_1$  ON again until  $I_{PK}$  is reached or output voltage is once again more than the desired value.

When the output voltage drops lower than the required value, the average discharge current of inductor  $L_1$  increases. This increases the time  $t_{ON}$ , since it needs more time to charge the inductor to  $I_{PK}$ . Increase in  $t_{ON}$  rises the voltage  $V_o$  to the desired value. When  $V_o$  increases, the inductor discharges less during  $t_{OFF}$ , and  $I_{PK}$  is reached faster when  $Q_1$  is ON. This causes  $t_{OFF}$  to reduce.

Current limiting is achieved by connecting a sense resistor  $R_{SC}$  between  $I_{PK}$  sense (pin 14) and the  $V_{CC}$  (pin 13). It is activated when a voltage of 330 mV appears across  $R_{SC}$ . This terminates  $t_{ON}$  interval and starts  $t_{OFF}$  interval. The voltage drop  $V_{DI}$  of the power diode  $D_1$  determines the OFF time of inductor  $L_1$  and the efficiency of the switching regulator. This regulator circuit is designed for stepping down from an input voltage of 25 V to an output voltage of 10 V.

The step-up switching regulator using  $\mu$ A78S40 along with the component values is shown in Fig. 8.35. This circuit generates an output voltage of 25 V when an input voltage of 10 V is applied.



**Fig. 8.35** Step-up switching regulator using  $\mu$ A78S40

### **Advantages of Switched Mode Power Supply (SMPS)**

1. Efficiency is high because of less heat dissipation.
2. As the transformer size is very small, it will have a compact unit.
3. Protection against excessive output voltage by quick acting guard circuits.
4. Reduced harmonic feedback into the main supply.
5. Isolation from main supply without the need of large mains transformer.
6. Generation of low and medium voltage supplies is easy.
7. Switching supplies can change an unregulated input of 24V into a regulated dc output voltage of 1000V.
8. Though RF interference can be a problem in SMPS unless properly shielded, SMPS in TV sets is in synchronisation with the line frequency (15.625kHz) and thus switching effects are not visible on the screen.
9. SMPS are also used in personal computers, video projectors and measuring instruments.

**Comparison between the linear mode and switched mode power supplies** Table 8.3 gives the comparison between Switched Mode Power Supply (SMPS) and Linear Mode Power Supply.

**Table 8.3** Comparison between the linear mode and switched mode Power Supplies

<b>Feature</b>	<b>SMPS</b>	<b>Linear power supply</b>
Efficiency	65–75 per cent	25–50 per cent
Temperature rise	20–40°C	50–100°C
Ripple value	Higher 25 to 50 mV	Even 5 mV possible
Overall regulation (percentage drop in volts on load)	0.3 per cent is common, tighter regulation is difficult to get	Even 0.1 percent is possible
RF interference	Can be a problem unless properly shielded	None
Magnetic material	Uses ferrite core	Uses stalloy or CRGO core
Weight	About 60 W/kg	20–30 W/kg
Cost	More parts, special ones, increase the cost	Advantage for smaller units up to 10–15W, but cost is higher if bigger
Reliability	Depends upon availability of suitable transistors	More reliable
Transient response	Slower (in ms)	Faster (in $\mu$ s)
Complexity	More	Less

## **SUMMARY**

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- ❑ An ideal regulated power supply is an electronic circuit designed to provide a predetermined dc voltage that is independent of the load current and variations in the input voltage.
- ❑ The voltage regulators are classified into
  - Linear voltage regulators
    - Series voltage regulator

- Shunt voltage regulator
- Switching regulators
  - Transformer based type
  - Buck switched type
  - Boost switched type
- The basic building blocks of a linear power supply are the transformer supplying ac voltage, rectifier, filter and voltage regulator.
- The output dc voltage  $V_o$  depends on the unregulated dc input voltage  $V_i$ , load current  $I_L$  and temperature  $T$ . The change in output voltage of a power supply is  $\Delta V_o = \frac{\partial V_o}{\partial V_i} \Delta V_i + \frac{\partial V_o}{\partial I_L} \Delta I_L + \frac{\partial V_o}{\partial T} \Delta T = S_v \Delta V_i + R_o \Delta I_L + S_T \Delta T$  where the coefficients  $S_v$ ,  $R_o$  and  $S_T$  are defined as

$$\text{Input regulation factor, } S_v = \frac{\Delta V_o}{\Delta V_i} | \Delta I_L = 0; \Delta T = 0$$

$$\text{Output resistance, } R_o = \frac{\Delta V_o}{\Delta I_L} | \Delta V_i = 0; \Delta T = 0$$

$$\text{Temperature coefficient, } S_T = \frac{\Delta V_o}{\Delta T} | \Delta V_i = 0; \Delta I_L = 0$$

Smaller the value of the three coefficients, better the regulation of the power supply.

- Line regulation is defined as the change in output voltage for a change in line supply voltage when the load current and temperature remain constant. It is given by

$$\text{Line regulation} = \frac{\text{change in output voltage}}{\text{change in input voltage}} = \frac{\Delta V_o}{\Delta V_i}$$

$$\text{□ Load regulation} = \frac{(V_{\text{no load}} - V_{\text{full load}})}{V_{\text{no load}}}$$

- Ripple rejection is defined as the ratio of peak-to-peak input ripple voltage  $\Delta V_{o(\text{unreg})}$  to the peak-to-peak output ripple voltage  $\Delta V_{o(\text{reg})}$ . It is typically 60 dB or more for the commonly used voltage regulators.
- The linear regulator uses an op-amp as an error amplifier, and a pass transistor as a control element.
- Dual tracking voltage regulator or plus-minus power supply can be constructed using op-amps by making the top half of the circuit acting as positive voltage regulator and the bottom half acting as a negative voltage regulator. The arrangement of this type of plus-minus power supply is possible only when there is no ground connection in the unregulated power supply.
- Based on the voltage output, the voltage regulators are classified into fixed positive, fixed negative and adjustable output voltage regulators.
- 78XX series are three terminal positive fixed voltage regulators. The available regulators are for 5V, 6V, 8V, 12V, 25V, 18V and 24V serially identified as 78XX with the digits XX indicating the fixed output voltage of the regulator. Similarly, the 79XX series are negative fixed voltage regulators which are complements to the 78XX series devices with two additional voltage options of -2V and -5.2V available in 79XX series.
- The internal circuit diagram of a three terminal positive voltage regulator IC consists of a band gap voltage reference circuit, emitter follower, a multiple current source, foldback current limiting circuit for overload protection, provides over-current and thermal overload protections and Zener diode circuit for thermal shutdown.
- 7805 regulator can be used as a current source for supplying a current of 500 mA to a load of  $20 \Omega$  for a maximum power of 5W. The maximum current can be increased by the use of a boost circuit that can deliver a current of 1A.
- The variable voltage regulators are used when (i) precisely variable regulated voltage sources and (ii) some specific voltages that are not available from standard fixed voltage regulators are required.

- ❑ LM117/LM317 and LM137/LM337 families are adjustable three terminal positive and negative voltage regulators respectively.
  - ❑ The LM117/LM317 series regulators are capable of supplying output current of 0.1A to 1.5A, over a range of 1.2V to 37V output voltage range available in TO-3, TO-39, TO-200, TO-202 and TO-92 packages with ripple rejection of 80 dB.
  - ❑ The input voltage range of LM117 / LM317 regulators must satisfy the requirement of  $3V \leq (V_i - V_o) \leq 40$  V.
  - ❑ The disadvantage of typical 78XX series and LM317 type of regulators being the drop-out voltage, the Low Drop-Out (LDO) regulators overcome the limitation. The IC LM2941 is a typical low-drop positive voltage regulator. It can source an output current of 1 A with a typical dropout voltage of 0.5 V and a maximum of 1 V over the entire temperature range.
  - ❑ IC 723 is a general purpose regulator that overcomes the limitations of three terminal fixed voltage regulators. It is a low current device that can be employed for load current up to 10A or more by using external transistors.
  - ❑ The terminals current limit (CL) and current sense (CS) of IC 723 provide current limit protection and sense voltage is the voltage drop obtained across a suitable resistor connected between CL and CS terminals.
  - ❑ IC 723 can be connected as low voltage regulator for the voltage range of 2V to 7V and as a high voltage regulator for the voltage range that is greater than 7V.
  - ❑ The limitation of the regulator IC 723 is that there is no built-in thermal protection and short circuit protection. Hence, an active current limiting circuit must be used to prevent the load current from increasing beyond a safe value.
  - ❑ The important advantages of foldback current limiting method are
    - Protecting the load from the over-current operation
    - Protecting the regulator itself
  - ❑ The maximum load current using IC 723 is 140 mA. For applications needing higher current values, a boost pass transistor can be used which can provide  $I_o = \beta_{\text{Boost Transistor}} \times I_{o(723)}$ . Darlington connected transistor pair can also be used as the pass transistor for obtaining much higher values of load currents.
  - ❑ The limitations of linear voltage regulators are:
    - The step-down transformer is bulky and expensive
    - Large values of filter capacitors are needed to eliminate ripples
    - The efficiency of series regulator is normally less than 50%
    - The input voltage must be more than the required output regulated voltage
    - The difference between the input and output voltage drops across the linear pass transistor and dissipates power
  - ❑ The switched mode regulators overcome the above limitations and they operate on the principle of chopping the unregulated dc supply voltage by the use of a transistor switch and filtering the high frequency components using a high frequency filter and the output voltage is regulated by varying the duty cycle or the switching period of the transistor.
  - ❑ The disadvantages of switched mode regulators are:
    - The noise is high on both the ac input and output lines due to switching that needs heavy filtering
    - Switching regulator is normally slower than linear voltage regulator due to the limited transient response
    - Switching regulator is more complex
  - ❑ Due to the above limitations, the switching regulators are used mainly for high power levels around 100 W.
  - ❑ Most of the switching power supplies regulate their output using pulse-width modulation (PWM).
  - ❑ µA78S40 from Fairchild, MC3420/3520 from Motorola and SG1524 from Silicon General are some of the widely used switching regulators.
- Current limiting in µA78S40 is achieved by using the sense resistor  $R_{SC}$ .

## REVIEW QUESTIONS

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1. What is the function of a voltage regulator?
2. Define the terms: Line Regulation, Load regulation and Ripple Rejection.
3. Define RRR. What does it indicate?
4. Write a note on *efficiency* of a voltage regulator and describe the different terms used to represent the same.
5. What are the advantages of IC voltage regulators?
6. What is the voltage reference  $V_{ref}$  in a voltage regulator? Why is it needed?
7. What is a series voltage regulator?
8. Compare series and shunt voltage regulators.
9. Explain the principles of obtaining a regulated power supply.
10. What are the important characteristics of a regulated power supply?
11. Sketch a circuit diagram of a single polarity regulated power supply using op-amp and explain its operation.
12. Design a dual polarity voltage regulator using op-amps. Draw the circuit diagram and explain its operation.
13. Mention the major functional blocks of a switching regulator.
14. Explain the operation of a series op-amp regulator.
15. Explain the operation of a dual-tracking voltage regulator using op-amp.
16. What is a three terminal regulator?
17. Draw a fixed voltage regulator circuit and explain its operation.
18. Differentiate between positive and negative voltage regulators.
19. IC 7805 voltage regulator has a built-in-short circuit protection (True/False).
20. Explain how the IC 7805 can be used as a current source.
21. Explain the method of boosting the current of a three terminal voltage regulator.
22. Give a circuit configuration for a dual power supply ( $\pm 15V$ ) using three terminal voltage regulator ICs.
23. What are the voltage options available in 78XX and 79XX series fixed voltage regulators?
24. What are the limitations of three terminal IC regulators?
25. Using 7805 voltage regulator, design a current source to deliver 400 mA current to a  $50\Omega$ , 5W load.
26. Explain with a circuit diagram, the steps involved in the design of a variable voltage regulated power supply.
27. Assume in Fig. 8.11,  $V_{EB(ON)} = 0.7V$  and  $\beta = 100$ . Calculate the output current  $I_o$  and  $I_C$  for a load of  $50\Omega$  in a regulator circuit using IC 7805.
28. Show the internal circuit arrangement of LM 317 regulator and indicate its output terminals.
29. Sketch a regulator circuit that uses the IC LM317/LM337 regulators. Explain the circuit operation. Write the expressions for the output voltage from the two regulators.
30. Show the circuit of a negative voltage regulator using IC LM137/LM337 and explain.
31. Show how can a dual voltage regulator be designed using ICs LM317 and LM337?
32. LM317 regulator shown in Fig. 8.13 has  $R_1 = 560\ \Omega$  and  $R_2 = 7.2\ k\Omega$ . If  $I_{ADJ} = 50\mu A$  and  $V_{ref} = 1.25\ V$ , find the value of  $V_o$ .
33. Design a practical voltage regulator circuit used in commercial power supplies for a range of 2V to 25V and an output current  $I_o$  of 1A.
34. Sketch and explain the internal circuitry of a programmable negative regulator.
35. What are the disadvantages of voltage regulators such as 78XX and 79XX. How does the low drop-out regulator overcome the limitation? Explain in detail using circuit diagram.
36. Construct a 5V to 20V regulator circuit using IC LM2941.
37. Draw a simplified functional block diagram of the voltage regulator IC 723.
38. State the limitations of linear voltage regulators.
39. Draw the block diagram of a switched mode power supply and mention its advantages over linear type power supply.
40. Draw the internal block diagram of IC 723 voltage regulator and explain the function of each block.
41. Draw the internal architecture of IC 723 voltage regulator.
42. What is the significance of the reference voltage supply in IC 723?

43. How can the IC 723 voltage regulator be used to provide output voltages ranging from 2V to 7V? Draw the circuit diagram and explain its operation. Why is it called *low voltage* regulator?
44. Draw the functional diagram and connection diagram of a low voltage regulator and explain.
45. Explain the circuit operation of a high voltage regulator using IC 723 with a circuit diagram. Write the equation for output voltage and state the ranges of output voltage and current that can be obtained using the circuit.
46. Design a + 15 V regulator using LM723, with a current limiting value of 50 mA.
47. What do you mean by *Low voltage* and *High voltage regulators* while using IC 723?
48. How is current-boosting achieved in IC 723?
49. Discuss the current limit protection in voltage regulators.
50. Draw the short-circuit overload protection circuit and explain its operation.
51. What is foldback current limiting? Explain the idea. Draw a regulator circuit with this implementation.
52. Explain how short circuit protection is provided in IC 723 voltage regulator.
53. Briefly discuss the design methodology for both types of current limit circuit.
54. Explain the implementation of overload protection in an IC voltage regulator.
55. Discuss the limitations of linear voltage regulators.
56. Describe briefly a switched mode power supply using operational amplifier.
57. What are the different configurations of a switching regulator? Explain them with basic block diagram and explain their operation.
58. Describe a step-down type of switching regulator.
59. Explain the operation of a step-up switching regulator with a block diagram.
60. Explain the use of IC 7840 for step-up and step-down voltage regulations.
61. List out the advantages of SMPS.
62. Compare the features and characteristics of linear mode and switching mode regulators.
63. What is the principle of switched mode supplies? Discuss their advantages and disadvantages.
64. Design a regulator using IC 723 for an output voltage  $V_o = 6 \text{ V}$ ,  $I_L = 1 \text{ mA}$ ,  $T_A = 25^\circ\text{C}$ ,  $I_{SC} = 150 \text{ mA}$  and  $V_{sense} = 0.7 \text{ V}$ .
65. For the foldback current limiting circuit shown in Fig. 8.23(b), the related output voltage = 5 V and  $R_4 = 8 \text{ k}\Omega$ . Calculate the value of  $R_{CL}$  to be connected for a maximum current of 1 A.

# Analog Multipliers

## 9.1 INTRODUCTION

The non-linear operations on analog signals are often required in instrumentation, communication and control-system design. These operations include the process of generation, rectification, modulation and demodulation of signals, frequency translation, multiplication and division. This chapter discusses the most commonly used techniques and the integrated circuit components for performing these operations. The Gilbert multiplier cell which forms the basis of a wide variety of circuits is discussed first, followed by the application of the Gilbert multiplier cell as a complete four-quadrant multiplier. The four-quadrant multiplier circuit based on variable transconductance technique is also explained. The analog multiplier IC AD633 is introduced subsequently, followed by important applications of the multiplier ICs.

## 9.2 ANALOG MULTIPLIERS

A multiplier produces an output  $V_o$ , which is proportional to the product of two inputs  $V_x$  and  $V_y$ .

That is,

$$V_o = KV_x V_y \quad (9.1)$$

where  $K$  is the scaling factor that is usually maintained as  $(1/10) V^{-1}$ . There are various methods available for performing analog multiplication. Four of such techniques, namely (i) logarithmic summing technique, (ii) pulse height/width modulation technique, (iii) variable transconductance technique, (iv) multiplication using Gilbert cell, and (v) multiplication using variable transconductance technique are discussed in this chapter.

An actual multiplier has its output voltage  $V_o$  defined by

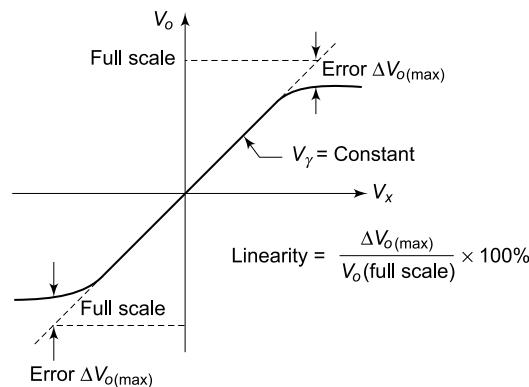
$$V_o = \frac{(V_x + \varphi_x)(V_y + \varphi_y)}{10(1 + \epsilon)} + \varphi_o \quad (9.2)$$

where  $\varphi_x$  and  $\varphi_y$  are the offsets associated with signals  $V_x$  and  $V_y$ ,  $\epsilon$  is the error signal associated with  $K$  and  $\varphi_o$  is the offset voltage of the multiplier output.

### **Commonly used terminologies associated with multiplier characteristics**

**Accuracy** This specifies the deviation of the actual output from the ideal output, for any combination of  $X$  and  $Y$  inputs falling within the permissible operating range of the multiplier.

**Linearity** This defines the accuracy of the multiplier. Figure 9.1 shows the response of the output as a function of one input voltage  $V_x$  when the other voltage  $V_y$  is assumed constant. It represents the maximum percentage deviation from the ideal straight line output. An *error surface* is formed by plotting the output for different combinations of  $X$  and  $Y$  inputs. The *Linearity Error* can be defined as the maximum absolute deviation of the error surface. This linearity error imposes a lower limit on the multiplier accuracy.



**Fig. 9.1** Linearity of the multiplier

**Squaring mode accuracy** The square-law curve is obtained with both the  $X$  and  $Y$  inputs connected together and applied with the same input signal. The maximum deviation of the output voltage from an ideal square-law curve expresses the squaring mode accuracy. This is shown in Fig. 9.2.

**Bandwidth** The bandwidth indicates the operating capability of an analog multiplier at higher frequency values. Small signal 3dB bandwidth defines the frequency  $f_o$  at which the output reduces by 3 dB from its low frequency value for a constant input voltage. This is identified individually for the  $X$  and  $Y$  input channels normally.

The *transconductance bandwidth* represents the frequency at which the transconductance of the multiplier drops by 3 dB of its low frequency value. This characteristic defines the application frequency ranges when used for phase detection or AM detection.

**Quadrant** The quadrant defines the applicability of the circuit for bipolar signals at its inputs. *First-quadrant device* accepts only positive input signals, the *two quadrant device* accepts one bipolar signal and one unipolar signal and the *four-quadrant device* accepts two bipolar signals.

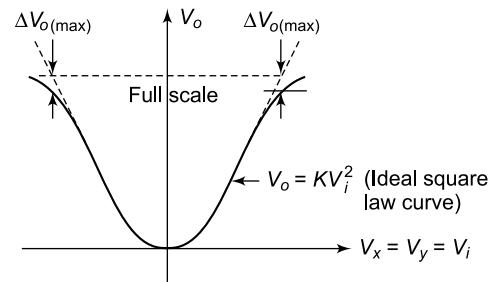
## 9.2.1 Logarithmic Summing Technique

This technique uses the relationship

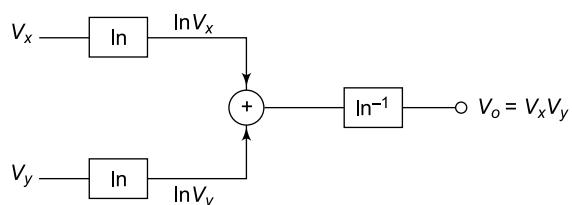
$$\ln V_x + \ln V_y = \ln(V_x V_y)$$

As shown in Fig. 9.3, the input voltages  $V_x$  and  $V_y$  are converted to their logarithmic equivalents, which are then added together by a summer. An antilogarithmic converter produces the output voltage of the summer. The output is given by

$$V_o = \ln^{-1}(\ln(V_x V_y)) = V_x V_y$$



**Fig. 9.2** Squaring mode accuracy of the multiplier



**Fig. 9.3** Multiplication using logarithmic summing technique

The exponential relationship between the collector current and base-to-emitter voltage of bipolar transistor during its active mode of operation could be exploited for the logarithmic and anti-logarithmic conversions. The relationship between  $I_C$  and  $V_{BE}$  of the transistor is given by

$$I_C = I_o e^{(V_{BE}/V_T)} \quad (9.3)$$

It is found that the transistor follows the relationship very accurately in the range of 10 nA to 10 mA. Logarithmic multiplier has low accuracy and high temperature instability. This method is applicable only to positive values of  $V_x$  and  $V_y$ . Therefore, this type of multiplier is restricted to one quadrant operation only.

### 9.2.2 Pulse Height/Width Modulation Technique

In this method, the pulse width of a pulse train is made proportional to one input voltage and the pulse amplitude is made proportional to the second input voltage. Therefore,  $V_x = K_x A$ ,  $V_y = K_y t$  and  $V_o = K_o T$ , where  $K_x$ ,  $K_y$  and  $K_o$  are scaling factors. In Fig. 9.4,  $A$  is the amplitude of the pulse,  $t$  is the pulse width and  $T$  is the area of the pulse. Therefore,

$$V_o = K_o T = K_o At = \frac{V_x V_y}{K_x K_y} \quad (9.4)$$

The modulated pulse train is passed through an integrating circuit. Therefore, the input of the integrator is proportional to the area of pulse, which in turn is proportional to the product of two input voltages.

### 9.2.3 A Simple Multiplier using an Emitter Coupled Transistor Pair

A circuit using an emitter coupled pair is shown in Fig. 9.5. The output currents  $I_{C1}$  and  $I_{C2}$  are related to the differential input voltage  $V_1$  by

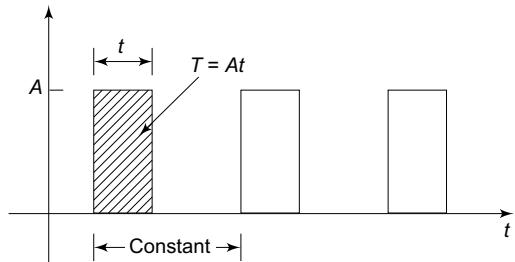
$$I_{C1} = \frac{I_{EE}}{1 + e^{-V_1/V_T}} \quad (9.5)$$

$$\text{and } I_{C2} = \frac{I_{EE}}{1 + e^{V_1/V_T}} \quad (9.6)$$

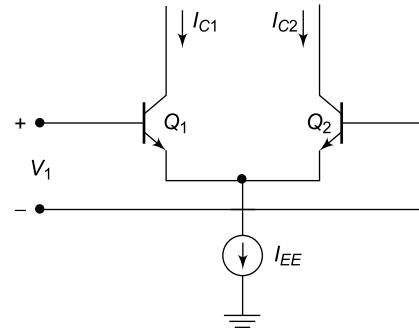
where  $V_T$  is the *thermal voltage* and the base currents have been neglected.

Combining Eqs. (9.5) and (9.6), we have the difference between the two output currents as

$$\begin{aligned} \Delta I_C &= I_{C1} - I_{C2} \\ &= I_{EE} \left( \frac{1}{1 + e^{-V_1/V_T}} - \frac{1}{1 + e^{V_1/V_T}} \right) \\ &= I_{EE} \tanh\left(\frac{V_1}{2V_T}\right) \end{aligned} \quad (9.7)$$



**Fig. 9.4** Multiplication using pulse height/width modulation technique



**Fig. 9.5** Emitter coupled transistor pair

The dc transfer characteristic of the emitter-coupled pair is shown in Fig. 9.6. It shows that the emitter-coupled pair can be used as a simple multiplier using this configuration. When the differential input voltage  $V_1 \ll V_T$ , we can approximate as given by

$$I_{EE} \tanh \frac{V_1}{2V_T} \approx I_{EE} \frac{V_1}{2V_T}.$$

Then, Eq. (9.7) becomes

$$\Delta I_C \approx I_{EE} \left( \frac{V_1}{2V_T} \right) \quad (9.8)$$

The current  $I_{EE}$  is the bias current for the emitter-coupled pair. If the current  $I_{EE}$  is made proportional to a second input signal  $V_2$ , then

$$I_{EE} \approx K_o(V_2 - V_{BE(on)}) \quad (9.9)$$

Substituting Eq. (9.9) into Eq. (9.8), we get

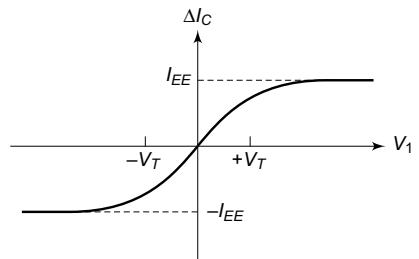
$$\Delta I_C = \frac{K_o V_1 (V_2 - V_{BE(on)})}{2V_T} \quad (9.10)$$

This arrangement is shown in Fig. 9.7. It is a simple modulator circuit constructed using a differential amplifier. It can be used as a multiplier, provided  $V_1$  is small and much less than 50 mV, and  $V_2$  is greater than  $V_{BE(on)}$ . But, the multiplier circuit shown in Fig. 9.7 has several limitations. The first limitation is that  $V_2$  is offset by  $V_{BE(on)}$ . The second is that  $V_2$  must always be *positive* which results in only a two-quadrant multiplier operation. The third limitation is that, the  $\tanh(X)$  is approximated as  $X$ , where  $X = \frac{V_1}{2V_T}$  in

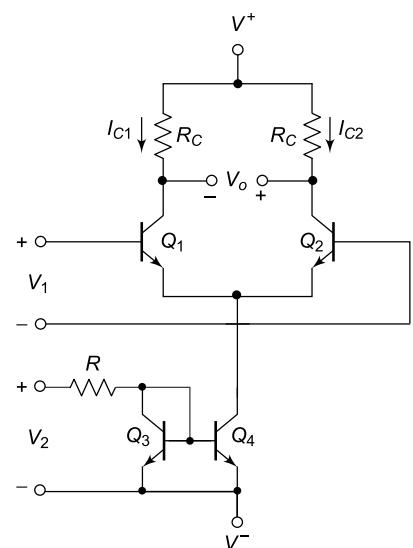
Eq. (9.8). The first two limitations are overcome in the Gilbert cell.

#### 9.2.4 Gilbert Multiplier Cell

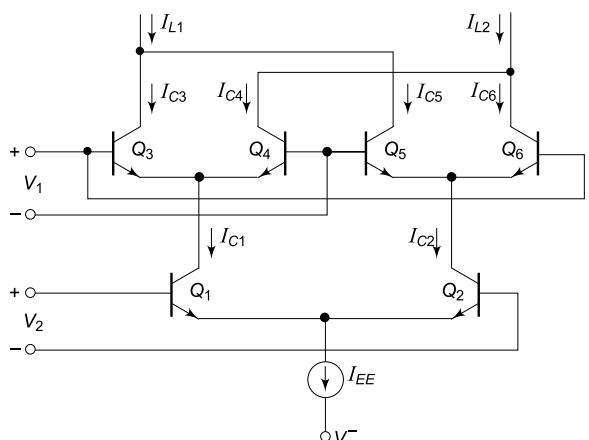
The Gilbert multiplier cell is a modification of the emitter coupled cell and this allows four-quadrant multiplication. Therefore, it forms the basis of most of the integrated circuit balanced multipliers. Two cross-coupled emitter-coupled pairs in series connection with an emitter coupled pair form the structure of the Gilbert multiplier cell. The operation of the Gilbert cell is shown in Fig. 9.8.



**Fig. 9.6** The dc transfer characteristic of emitter-coupled pair



**Fig. 9.7** A simple modulator using a differential amplifier



**Fig. 9.8** Gilbert multiplier cell

The collector currents of  $Q_3$  and  $Q_4$  are given by

$$I_{C3} = \frac{I_{C1}}{1 + e^{-V_1/V_T}} \quad (9.11)$$

and

$$I_{C4} = \frac{I_{C1}}{1 + e^{V_1/V_T}} \quad (9.12)$$

Similarly the collector currents of  $Q_5$  and  $Q_6$  are given by

$$I_{C5} = \frac{I_{C2}}{1 + e^{-V_1/V_T}} \quad (9.13)$$

and

$$I_{C6} = \frac{I_{C2}}{1 + e^{V_1/V_T}} \quad (9.14)$$

The collector currents  $I_{C1}$  and  $I_{C2}$ , of transistors  $Q_1$  and  $Q_2$  can be expressed as

$$I_{C1} = \frac{I_{EE}}{1 + e^{-V_2/V_T}} \quad (9.15)$$

and

$$I_{C2} = \frac{I_{EE}}{1 + e^{V_2/V_T}} \quad (9.16)$$

Substituting Eq. (9.15) in Eqs. (9.11) and (9.12), we get

$$I_{C3} = \frac{I_{EE}}{\left[1 + e^{-V_1/V_T}\right]\left[1 + e^{-V_2/V_T}\right]} \quad (9.17)$$

and

$$I_{C4} = \frac{I_{EE}}{\left[1 + e^{V_1/V_T}\right]\left[1 + e^{-V_2/V_T}\right]} \quad (9.18)$$

Similarly, substituting Eq. (9.16) in Eqs. (9.13) and (9.14), we get

$$I_{C5} = \frac{I_{EE}}{\left[1 + e^{V_1/V_T}\right]\left[1 + e^{V_2/V_T}\right]} \quad (9.19)$$

and

$$I_{C6} = \frac{I_{EE}}{\left[1 + e^{-V_1/V_T}\right]\left[1 + e^{V_2/V_T}\right]} \quad (9.20)$$

The differential output current  $\Delta I$  is given by

$$\Delta I = I_{L1} - I_{L2}$$

That is,

$$\Delta I = (I_{C3} + I_{C5}) - (I_{C4} + I_{C6})$$

or

$$\Delta I = (I_{C3} - I_{C6}) - (I_{C4} - I_{C5}) \quad (9.21)$$

Substituting Eqs. (9.17) to (9.20) in Eq. (9.21) and employing exponential formulae for hyperbolic functions, we get

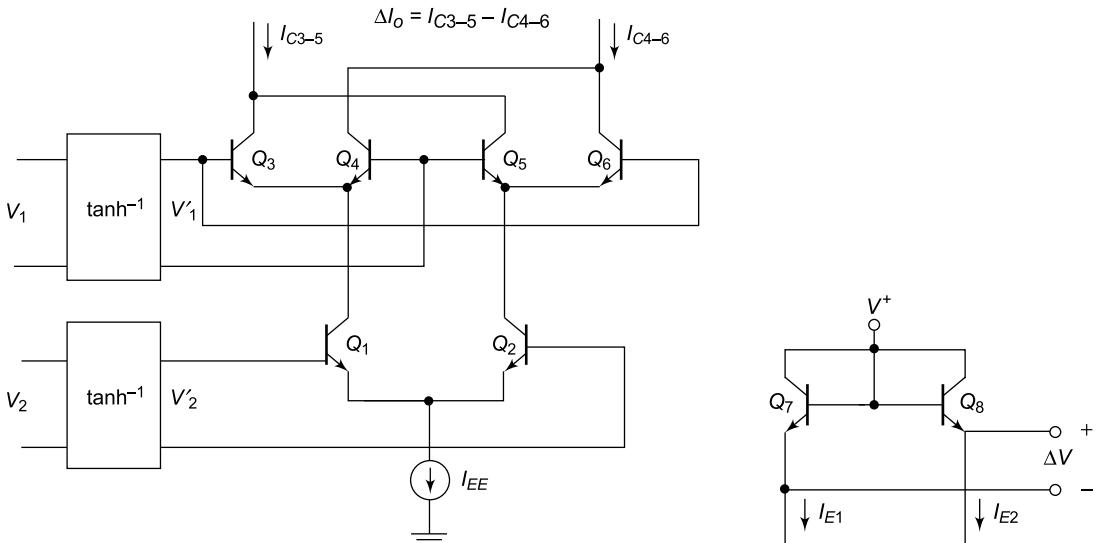
$$\Delta I = I_{EE} \left[ \tanh\left(\frac{V_1}{2V_T}\right) \tanh\left(\frac{V_2}{2V_T}\right) \right] \quad (9.22)$$

The above equation shows that when  $V_1$  and  $V_2$  are small, the Gilbert Cell shown in Fig. 9.8 can be used as a four-quadrant analog multiplier with the use of *current-to-voltage* converters. The dc transfer characteristic of such a multiplier circuit is the product of the hyperbolic tangent of the two input voltages. The output voltage  $V_o$  can be generated from  $\Delta I$ , by using two equal valued resistors connected to  $V_{CC}$  and by sending  $I_{L1}(=I_{C3} + I_{C5})$  through one resistor and  $I_{L2}(=I_{C4} + I_{C6})$  through the second resistor.

A modulator or a mixer is a circuit with two inputs, namely, *carrier input* and *modulating input* and one *modulated output*. A linear response is required only for the modulating input, since the carrier is usually an ac signal with constant amplitude.

The multiplier shown in Fig. 9.8 can also be used as a modulator, if one of the inputs is very large and the second input is very small ( $\tanh(X) \approx X$ ). Then, the transistors operated by the large-signal input act as switches. This effectively multiplies the small input signal by a square wave. Hence, this mode of operation acts as a modulator. These are called *synchronous modulators* and they find applications in signal processing, demodulation and phase detection.

**Gilbert multiplier with predistortion circuits** When the magnitudes of  $V_1$  and  $V_2$  are very small when compared with  $V_T$ , the hyperbolic  $\tan$  function is approximated as linear, and the circuit can be used as a multiplier, for finding the product of  $V_1$  and  $V_2$ . But, when larger  $V_1$  and  $V_2$  are to be multiplied, a nonlinearity function can be used to *predistort* the input signals. This compensates for the hyperbolic tangent transfer characteristic of the basic cell. The required nonlinearity function is an *inverse hyperbolic tangent* characteristic whose arrangement is shown in Fig. 9.9.

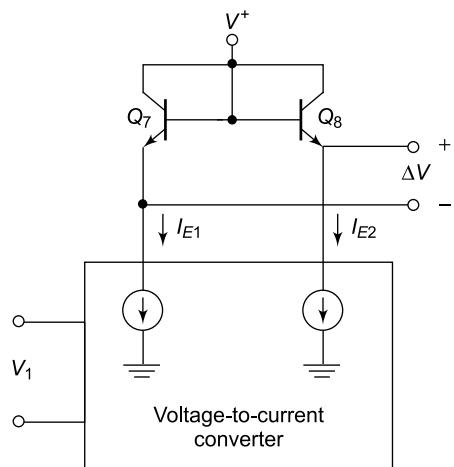


**Fig. 9.9** Gilbert multiplier circuit with predistortion

The generation of the inverse hyperbolic tangent function is shown in Fig. 9.10. Assume that the circuit within the box generates a differential output current, and it linearly depends on the input voltage  $V_1$ .

$$\text{Then, } I_{E1} = I_{o1} + K_1 V_1$$

$$\text{and } I_{E2} = I_{o1} - K_1 V_1$$



**Fig. 9.10** An inverse hyperbolic tangent circuit

where  $I_{o1}$  is the dc current flowing in each output,  $K_1$  is the transconductance of the *voltage-to-current* converter, and it is assumed that  $V_1 = 0$ . The differential voltage  $\Delta V$  across the diode-connected transistors  $Q_7$  and  $Q_8$  is given by

$$\begin{aligned}\Delta V &= V_T \ln\left(\frac{I_{o1} + K_1 V_1}{I_o}\right) - V_T \ln\left(\frac{I_{o1} - K_1 V_1}{I_o}\right) \\ &= V_T \ln\left(\frac{I_{o1} + K_1 V_1}{I_{o1} - K_1 V_1}\right)\end{aligned}$$

This can be transformed into

$$\Delta V = 2V_T \tanh^{-1}\left(\frac{K_1 V_1}{I_{o1}}\right)$$

using the identity  $\tanh^{-1}(X) = \frac{1}{2} \ln\left(\frac{1+X}{1-X}\right)$

When this functional block is used, it compensates for the nonlinearity of the inputs. Then, Eq. (9.22) can be represented by

$$\Delta I = I_{EE} \left( \frac{K_1 V_1}{I_{o1}} \right) \left( \frac{K_2 V_2}{I_{o2}} \right) \quad (9.23)$$

where  $I_{o1}, K_1$  and  $I_{o2}, K_2$  are the parameters of the functional blocks following inputs  $V_1$  and  $V_2$  respectively. Equation (9.23) shows that the differential output current is proportional to the product  $V_1 V_2$ .

**Complete four-quadrant analog multiplier** Figure 9.11 illustrates the circuit diagram of the complete four-quadrant analog multiplier using Gilbert Cell. The three boxes are *voltage-to-current* converters or *current-to-voltage* converters in effect. The pre-distortion for the input signal is achieved by transistors  $Q_7$  and  $Q_8$ . The currents  $I_9$  and  $I_{10}$  passing through the emitters of  $Q_7$  and  $Q_8$  generate a voltage between the two emitter terminals, that is proportional to the inverse hyperbolic tangent of  $V_1$ . This compensates for the hyperbolic tangent expression for Eq. (9.18).

**Analysis of the circuit** A complete four quadrant analog multiplier using Gilbert cell is shown in Fig. 9.11. The current through base-emitter junctions of transistors  $Q_7, Q_3, Q_4$  and  $Q_8$  connected in series can be expressed by

$$I_9 I_3 = I_4 I_{10} \quad (9.24)$$

Similarly, from the series connection of the transistors  $Q_7, Q_6, Q_5$  and  $Q_8$ , we get

$$I_9 I_6 = I_5 I_{10} \quad (9.25)$$

From Fig. 9.11, we see that

$$I_1 = I_3 + I_4 \quad (9.26)$$

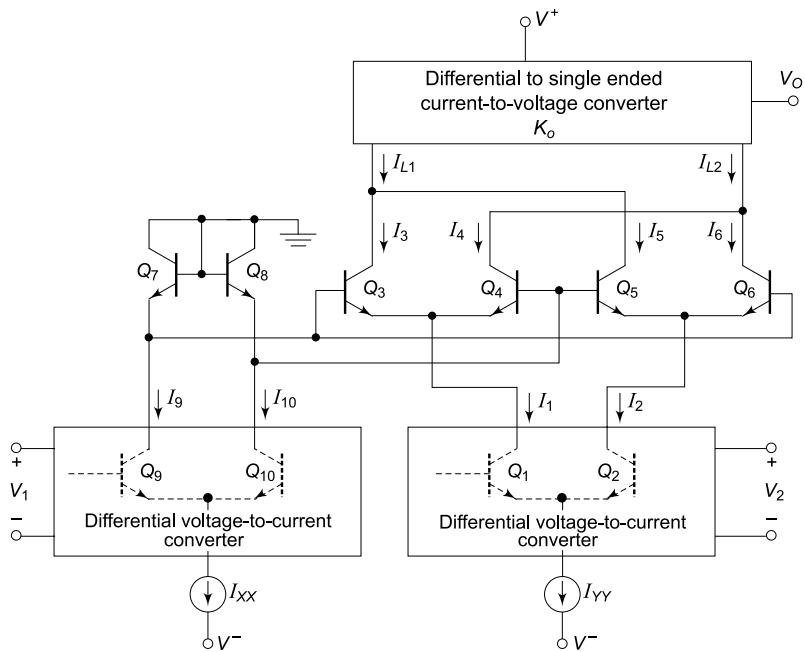
$$I_2 = I_5 + I_6 \quad (9.27)$$

$$I_{L1} = I_3 + I_5 \quad (9.28)$$

$$I_{L2} = I_4 + I_6 \quad (9.29)$$

and

$$I_{XX} = I_9 + I_{10} \quad (9.30)$$



**Fig. 9.11** A complete four quadrant analog multiplier using Gilbert Cell

The transfer characteristics of the differential voltage-to-current converter is given by

$$I_9 - I_{10} = \frac{V_1}{K_1} \quad (9.31)$$

$$I_1 - I_2 = \frac{V_2}{K_2} \quad (9.32)$$

and the transfer characteristics of the differential-to-single ended current-to-voltage converter is given by

$$V_o = K_o(I_{L2} - I_{L1}) \quad (9.33)$$

where  $K_o$ ,  $K_1$ , and  $K_2$  are constants.

Substituting for  $I_{L1}$  and  $I_{L2}$  from Eqs. (9.28) and (9.29), in Eq. (9.33), we get

$$V_o = K_o[(I_4 + I_6) - (I_3 + I_5)]$$

Using Eqs. (9.24) and (9.25),

$$V_o = K_o \left[ \left( I_4 + I_5 \frac{I_{10}}{I_9} \right) - \left( I_4 \frac{I_{10}}{I_9} + I_5 \right) \right] \quad (9.34)$$

Simplifying the above equation, we get

$$V_o = K_o \left( \frac{I_9 - I_{10}}{I_9} \right) (I_4 - I_5) \quad (9.35)$$

From Fig. 9.11, we see that

$$\begin{aligned} I_1 - I_2 &= (I_3 + I_4) - (I_5 + I_6) \\ &= \left( I_4 \frac{I_{10}}{I_9} + I_4 \right) - \left( I_5 + I_5 \frac{I_{10}}{I_9} \right) \end{aligned} \quad (9.36)$$

Solving for  $(I_4 - I_5)$  gives

$$(I_4 - I_5) = \left( \frac{I_9}{I_9 + I_{10}} \right) (I_1 - I_2) \quad (9.37)$$

Substituting Eq. (9.37) in Eq. (9.35) and using Eq. (9.31) and Eq. (9.32), we get

$$\begin{aligned} V_o &= K_o \left( \frac{I_9 - I_{10}}{I_9 + I_{10}} \right) (I_1 - I_2) \\ &= \frac{K_o V_1 V_2}{I_{XX} K_1 K_2} = K_m V_1 V_2 \end{aligned} \quad (9.38)$$

where

$$K_m = \frac{K_o}{I_{XX} K_1 K_2}$$

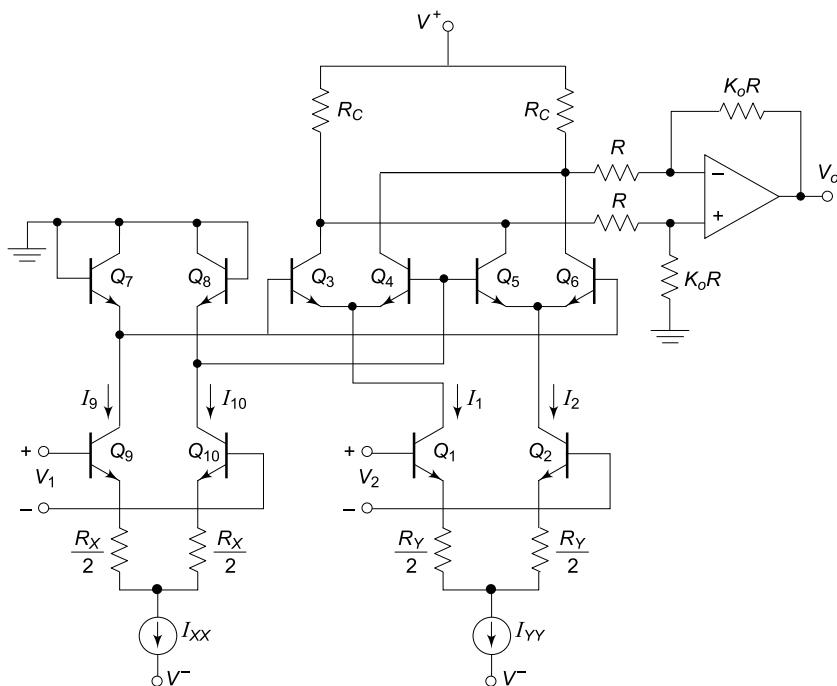
Equation (9.38) employs no approximations. Hence the input signal amplitudes have no constraints.

**Practical implementation of the four-quadrant analog multiplier** A practical four-quadrant analog multiplier circuit is shown in Fig. 9.12. It can be observed that

$$I_1 - I_2 = \frac{2V_2}{R_Y} \quad (9.39)$$

and

$$I_9 - I_{10} = \frac{2V_1}{R_X} \quad (9.40)$$



**Fig. 9.12** Practical four-quadrant analog multiplier circuit

Further it is assumed that the drop across base-emitter of  $Q_9 - Q_{10}$  and  $Q_1 - Q_2$  pairs are small in comparison with the drop across  $R_X$  and  $R_Y$ .

Substituting Eqs. (9.39) and (9.40) in Eq. (9.38), we get

$$\begin{aligned} V_o &= \frac{4K_o R_C V_1 V_2}{I_{XX} R_X R_Y} \\ &= K_m V_1 V_2, \quad \text{where } R \gg R_C \end{aligned}$$

The circuit is capable of performing precise multiplication of a continuously varying analog signal by another signal. One of the problems though, is the need to be able to trim the errors due to offsets and mismatches in the integrated circuit implementation.

### 9.2.5 Variable Transconductance Technique

The variable transconductance technique makes use of the dependence characteristic of the transistor transconductance parameter on the emitter current bias applied. A simple differential circuit arrangement depicting the principle is shown in Fig. 9.13. The relationship between  $V_o$  and  $V_x$  is given by

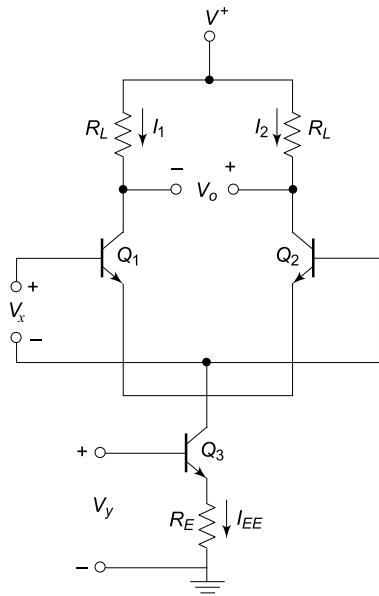
$$V_o = g_m R_L V_x$$

where  $g_m = I_{EE}/V_T$  is the transconductance of the stage. Application of a second input  $V_y$  to the reference current source of the differential amplifier can vary  $g_m$ .

Thus, if  $R_E I_{EE} \gg V_{BE}$ , the bias voltage  $V_y$  is related to  $I_{EE}$  by the relation  $V_y = I_{EE} R_E$ .

Then, the overall voltage transfer expression is given by

$$\begin{aligned} V_o &= g_m R_L V_x = (V_y/V_T R_E) V_x R_L \\ &= V_x V_y \frac{R_L}{V_T R_E} \end{aligned}$$



**Fig. 9.13** Differential stage of the transconductance multiplier

**Generation of logarithmic bias input for differential stage** It is assumed in Sec. 9.2.3 that  $|V_x| \ll V_y$  and there is no emitter degeneration. Referring to Fig. 9.13, the collector currents  $I_1$  and  $I_2$  are related to the applied voltage  $V_x$  by the relation

$$\frac{I_1}{I_2} = e^{(V_x/V_T)} \quad (9.41)$$

Therefore, linearity can be achieved by reducing the exponential current-voltage characteristic to a linear one, as shown in Fig. 9.14. The transistors  $Q_1$  and  $Q_2$  are biased through the diode connected  $Q_A$  and  $Q_B$ , which are driven by controlled current sources  $I_A$  and  $I_B$  respectively. Then the net bias voltage  $V_x$  is represented by

$$V_x = V_T \ln \frac{I_B}{I_A} \quad (9.42)$$

Substituting Eq. (9.42) in Eq. (9.41), we get

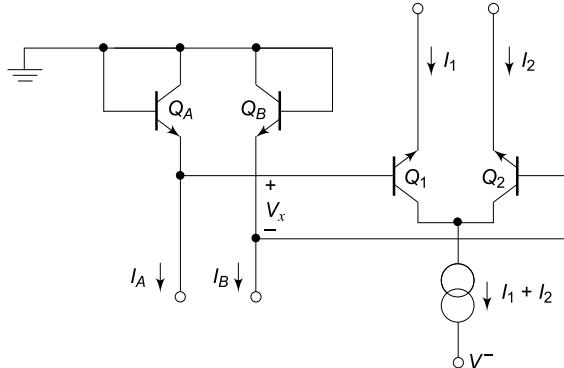
$$\frac{I_1}{I_2} = \frac{I_B}{I_A}$$

Similarly,

$$\frac{I_A}{I_A + I_B} = \frac{I_2}{I_1 + I_2} = \frac{1}{1 + e^{V_x/V_T}} \quad (9.43)$$

and

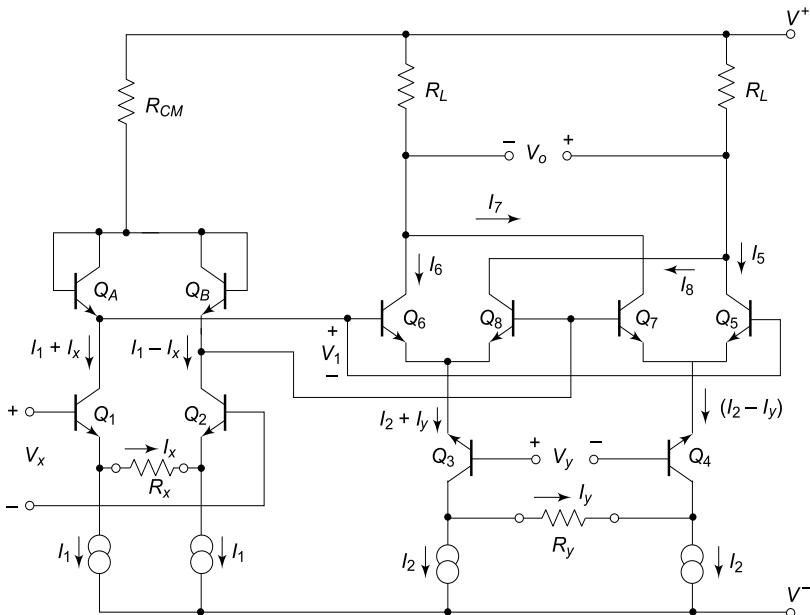
$$\frac{I_B}{I_A + I_B} = \frac{I_1}{I_1 + I_2} = \frac{e^{V_x/V_T}}{1 + e^{V_x/V_T}} \quad (9.44)$$



**Fig. 9.14** Logarithmic biasing for increasing linearity of multiplier

The above equations are valid over a wider range, if the device characteristics are well matched and  $V_{BE}$  obeys the basic diode equation.

**Four-quadrant variable transconductance multiplier** A typical four-quadrant multiplier circuit is shown in Fig. 9.15. The *four-quadrant* operation indicates that the output voltage is directly proportional to the product of the two input voltages regardless of the polarity of the inputs and such multipliers can be operated in all the four quadrants of operation.



**Fig. 9.15** Four-quadrant monolithic multiplier

The first part of the circuit generates an intermediate voltage  $V_1$  across the transistors  $Q_A$  and  $Q_B$  in response to the input signal  $V_x$ . The nonlinear response to the input  $V_x$  in generating  $V_1$  is compensated by the inverse nonlinearity associated with the base-emitter junctions of the quad-transistors  $Q_5-Q_6$  and  $Q_7-Q_8$ . Thus the output voltage  $V_o$  is maintained proportional to the linear product of the two input voltages to differential currents  $I_x$  and  $I_y$ . Thus,  $I_x = V_x/R_x$  and  $I_y = V_y/R_y$ . The value of  $R_x$  and  $R_y$  are chosen such that  $R_x \gg V_T/I_1$  and  $R_y \gg V_T/I_2$  respectively.

The output voltage  $V_o$  can be written as

$$V_o = R_L((I_6 + I_7) - (I_5 + I_8)) \quad (9.45)$$

Applying Eqs. (9.43) and (9.44) to the circuit, we obtain

$$\frac{I_6}{I_2 + I_y} = \frac{I_5}{I_2 - I_y} = \frac{I_1 + I_x}{2I_1} \quad (9.46)$$

and

$$\frac{I_8}{I_2 + I_y} = \frac{I_7}{I_2 - I_y} = \frac{I_1 - I_x}{2I_1} \quad (9.47)$$

Substituting Eqs. (9.46) and (9.47) into Eq. (9.45), we get

$$V_o = \frac{2R_L}{I_1} (I_x I_y) \quad (9.48)$$

Since  $I_x$  and  $I_y$  are linearly related to  $V_x$  and  $V_y$  respectively, we have

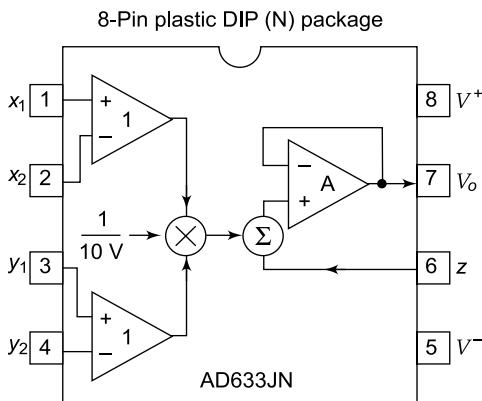
$$V_o = KV_x V_y \quad (9.49)$$

where the scaling factor  $K = \frac{2R_L}{I_1 R_x R_y}$ , which is normally chosen as 0.1.

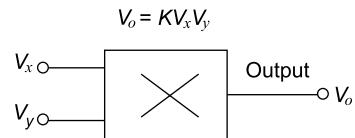
### 9.3 ANALOG MULTIPLIER ICs

Analog multiplier is a circuit whose output voltage at any instant is proportional to the product of instantaneous value of two individual input voltages. The important applications of these multipliers are

multiplication, division, squaring and square-rooting of signals, modulation and demodulation. These analog multipliers are available as integrated circuits consisting of op-amps and other circuit elements. The schematic of a typical analog multiplier, namely, AD633 is shown in Fig. 9.16(a).



**Fig. 9.16 (a)** Schematic symbol of AD633 multiplier IC

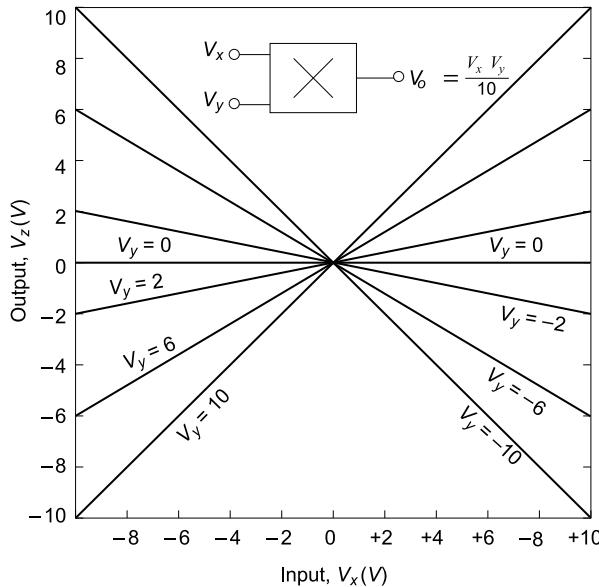


**Fig. 9.16 (b)** Schematic representation with two inputs and one output

The AD633 multiplier is a four-quadrant analog multiplier. It possesses high input impedance, and this characteristic makes the loading effect on the signal source negligible. It can operate with supply voltages ranging from  $\pm 8V$  to  $\pm 18V$ . The IC does not require external components. The calibration by user is not necessary. The typical range of the two input signals is  $\pm 10V$ .

**Schematic representation of a multiplier** The schematic symbol of an analog multiplier is shown in Fig. 9.16(b). The output  $V_o$  is the product of the two inputs  $V_x$  and  $V_y$  divided by a reference voltage  $V_{ref}$ . Normally, the reference voltage  $V_{ref}$  is internally set to 10V. Therefore,  $V_o = \frac{V_x V_y}{10}$ . In other words, the basic input-output relationship can be defined by  $V_o = KV_x V_y$  where  $K = \frac{1}{10}$ , a constant. Therefore, for peak input voltages of 10V, the peak magnitude of output voltage is  $\frac{1}{10} \times 10 \times 10 = 10V$ . Thus, it can be noted that, as long as  $V_x < 10V$  and  $V_y < 10V$ , the multiplier output will not saturate.

**Multiplier quadrants** The transfer characteristic of a typical four-quadrant multiplier is shown in Fig. 9.17. Both the inputs can be positive or negative to obtain the corresponding output as shown in the transfer characteristics.



**Fig. 9.17** Transfer characteristics of four-quadrant multiplier

## 9.4 APPLICATIONS OF MULTIPLIER ICs

The multiplier ICs are used for the following purposes:

- (i) Voltage squarer
- (ii) Frequency doubler
- (iii) Voltage divider
- (iv) Square rooter

- (v) Phase angle detector
- (vi) Rectifier

### 9.4.1 Voltage Squarer

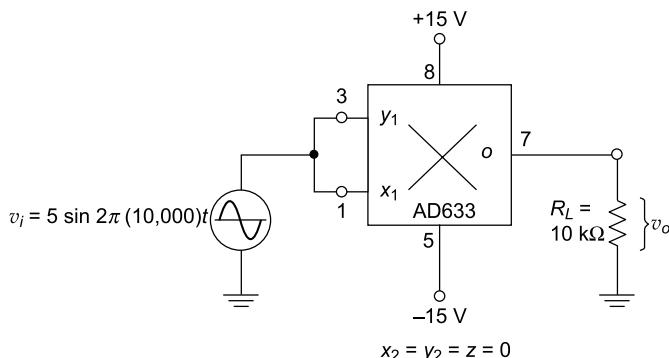
Figure 9.18 shows the multiplier IC connected as a squaring circuit. The inputs can be positive or negative, represented by any corresponding voltage level between 0 and 10 V. The input voltage  $v_i$  to be squared is simply connected to both the input terminals, and hence we have,  $v_x = v_y = v_i$  and the output is  $v_o = Kv_i^2$ .

The circuit thus performs the squaring operation. This application can be extended for frequency doubling applications also as explained in the following section.

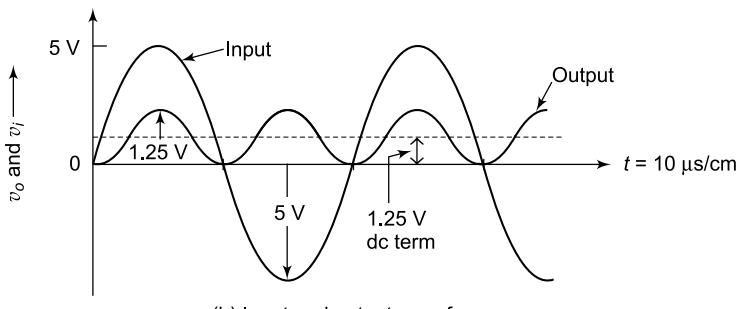
### 9.4.2 Frequency Doubler

Figure 9.19(a) shows the squaring circuit connected for frequency doubling operation. A sine-wave signal  $v_i$  has a peak amplitude of  $A_v$  and frequency of  $f$  Hz. Then, the output voltage of the doubler circuit is given by,

$$\begin{aligned} v_o &= \frac{A_v \sin 2\pi ft \times A_v \sin 2\pi ft}{10} = \frac{A_v^2}{10} \sin^2(2\pi ft) \\ &= \frac{A_v^2}{20} (1 - \cos 4\pi ft) \end{aligned}$$

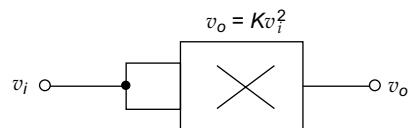


(a) Circuit diagram



(b) Input and output waveforms

**Fig. 9.19** Frequency doubler using multiplier



**Fig. 9.18** Voltage squarer using multiplier

Assuming a peak amplitude  $A_v$  of 5V and frequency  $f$  of 10 kHz,  $v_o = 1.25 - 1.25 \cos 2\pi(20000)t$ . The first term represents the dc term of 1.25V peak amplitude. The input and output waveforms are shown in Fig. 9.19(b). The output waveform ripples with twice the input frequency in the rectified output of the input signal. This forms the principle of application of analog multiplier as rectifier for ac signals.

The dc component of output  $v_o$  can be removed by connecting a  $1\mu F$  coupling capacitor between the output terminal and a load resistor, across which the output can be observed.

### 9.4.3 Voltage Divider

The voltage divider circuit can be constructed using a multiplier and an op-amp as shown in Fig. 9.20. This circuit produces the ratio of two input signals. The division is achieved by connecting the multiplier in the feedback loop of an op-amp. The voltages  $v_{den}$  and  $v_{num}$  represent the two input voltages.  $v_{den}$  forms one input of the multiplier, and output  $v_{OA}$  of op-amp forms the second input. The output  $v_{om}$  of the multiplier is connected back to the inverting input terminal of op-amp in the feedback loop.

Then, the characteristic operation of the multiplier gives

$$v_{om} = K v_{OA} v_{den} \quad (9.50)$$

As shown in Fig. 9.20, no input signal current can flow into the inverting input terminal of op-amp, which is at virtual ground. Therefore, at the junction  $a$ ,  $i_1 + i_2 = 0$ . The current  $i_1 = \frac{v_{num}}{R}$ , where  $R$  is the input resistance and the current  $i_2 = \frac{v_{om}}{R}$ . With virtual ground existing at  $a$ ,

$$i_1 + i_2 = \frac{v_{num}}{R} + \frac{v_{om}}{R} = 0,$$

or

$$v_{om} = -v_{num} \quad (9.51)$$

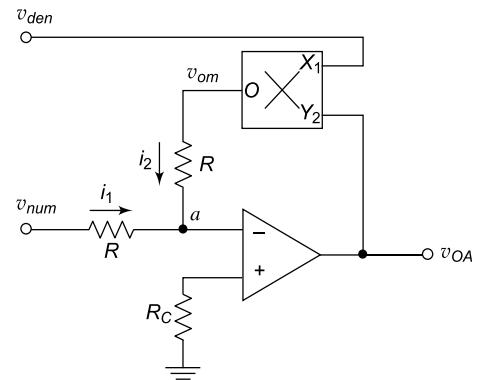
Substituting Eq. (9.50) in Eq. (9.51),

$$K v_{OA} v_{den} = -v_{num}$$

or

$$v_{OA} = \frac{-v_{num}}{K v_{den}}$$

where  $v_{num}$  and  $v_{den}$  are the numerator and denominator voltages respectively. Therefore, the voltage division operation is achieved.  $v_{num}$  can be a positive or negative voltage and  $v_{den}$  can have only positive values to ensure negative feedback. When  $v_{den}$  is changed, the gain  $10/v_{den}$  changes, and this feature is used in *automatic gain control* (AGC) circuits.



**Fig. 9.20** Divider circuit using multiplier and op-amp

### 9.4.4 Square Rooter

The divider circuit of Fig. 9.20 can be used to find the square root of a signal by connecting output of op-amp to both inputs of the multiplier. Then, the output voltage of the multiplier  $v_{om}$  is equal in magnitude but opposite in polarity (with respect to ground) to  $v_i$ . But we know that  $v_{om}$  is one-tenth (*scale factor*) of  $v_o \times v_o$  or

$$-v_i = v_{om} = \frac{v_o^2}{10} \quad (9.52)$$

Solving for  $v_o$  and eliminating  $\sqrt{-1}$  yields

$$v_o = \sqrt{10|v_i|} \quad (9.53)$$

Equation (9.53) states that  $v_o$  equals the square root of 10 times the *absolute magnitude* of  $v_i$ . The input voltage  $v_i$  must be negative, or else, the op-amp saturates. The range of  $v_i$  is between  $-1$  and  $-10$  V. Voltages less than  $-1$  V will cause inaccuracies in the result. The diode prevents negative saturation for positive polarity  $v_i$  signals. For positive values of  $v_i$ , the diode connections are reversed.

### 9.4.5 Phase Angle Detector

The multiplier configured for phase angle detection measurement is shown in Fig. 9.21(a). When two sine-waves of the same frequency are applied to the inputs of the multiplier, the output  $v_o$  has a dc component and an ac component.

The trigonometric identity shows that

$$\sin A \sin B = \frac{1}{2} (\cos(A - B) - \cos(A + B)).$$

When the two frequencies are equal, but with different phase angles, e.g.  $A = 2\pi ft + \theta$  for signal  $v_x$  and  $B = 2\pi ft$  for signal  $v_y$ , then using the identity

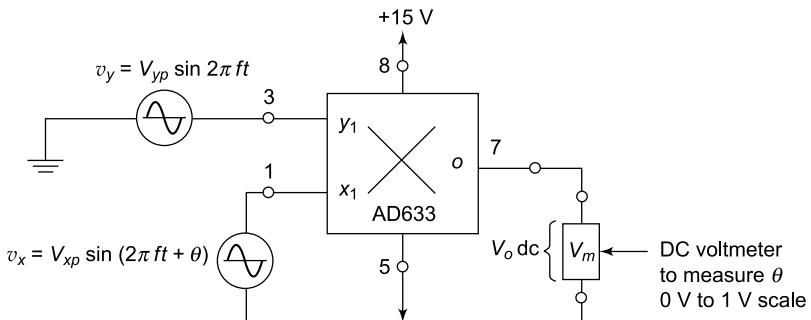
$$\begin{aligned} [\sin(2\pi ft + \theta)][(\sin 2\pi ft)] &= \frac{1}{2} [\cos \theta - \cos(2\pi \times 2ft + \theta)] \\ &= 1/2 (dc - \text{the double frequency term}) \end{aligned}$$

Therefore, when the two input signals  $v_x$  and  $v_y$  are applied to the multiplier,  $v_{o(dc)}$  is given by

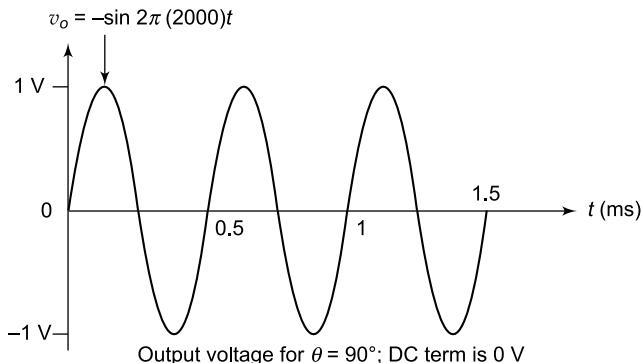
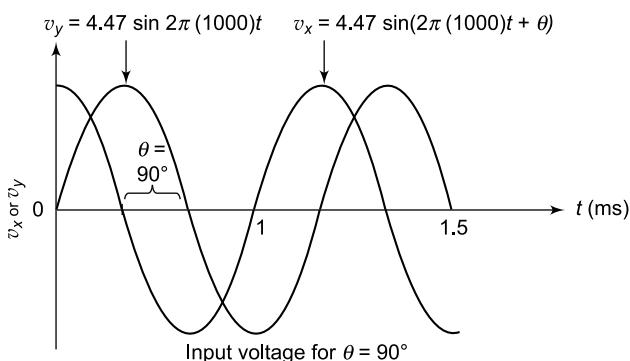
$$v_{o(dc)} = \frac{v_{xp} v_{yp}}{20} \cos \theta \quad (9.54)$$

where  $v_{xp}$  and  $v_{yp}$  are the peak voltage amplitudes of the signals  $v_x$  and  $v_y$ . Thus, the output  $v_{o(dc)}$  depends on the factor  $\cos \theta$ . A dc voltmeter can be calibrated as a *phase angle meter* when the product of  $v_{xp}$  and  $v_{yp}$  is made equal to 20. Then, a  $(0 - 1)$  V range dc voltmeter can directly read  $\cos \theta$ , with the meter calibrated directly in *degrees* from a cosine table. The input and output waveforms are shown in Fig. 9.21(b).

Then the Eq. (9.54) becomes  $v_{o(dc)} = \cos \theta$ , if we make the product  $v_{xp} v_{yp} = 20$  or in other words,  $v_{xp} = v_{yp} = 4.47$  V.



(a) Circuit diagram



(b) Input and output waveforms

**Fig. 9.21** Phase angle measurement using multiplier**Example 9.1**

- (1) For  $v_{o(dc)} = 0$ , calculate phase angle  $\theta$ .
- (2) If  $v_{xp} = 4.47 \sin 2\pi 1000t$  and  $v_{yp} = 4.47 \sin(2\pi(1000)t + \theta)$ , find the dc component for (a)  $\theta = \pm 30^\circ$ , (b)  $\theta = \pm 45^\circ$  and (c)  $\theta = \pm 60^\circ$ .

**Solution**

(1) From Eq. (9.54),

$$v_{o(dc)} = \frac{v_{xp} v_{yp}}{20} \cos \theta$$

When  $v_{o(dc)} = 0$ ,  $\cos \theta = 0$ .

Therefore,  $\theta = \pm 90^\circ$

(2) Substituting the given values of  $v_{xp}$  and  $v_{yp}$ , we get,

$$v_{o(dc)} = \frac{4.47 \times 4.47}{20} \times \cos \theta$$

- (a) For  $\theta = \pm 30^\circ$ ,  $v_{o(dc)} = 0.866$  V
- (b) For  $\theta = \pm 45^\circ$ ,  $v_{o(dc)} = 0.707$  V
- (c) For  $\theta = \pm 60^\circ$ ,  $v_{o(dc)} = 0.5$  V

**SUMMARY**

- An actual multiplier has its output voltage

$$V_o = \frac{(V_x + \varphi_x)(V_y + \varphi_y)}{10(1 + \varepsilon)} + \varphi_o$$

where  $\varphi_x$  and  $\varphi_y$  are the offsets of input signals  $V_x$  and  $V_y$ ,  $\varepsilon$  is the error signal and  $\varphi_o$  is the offset voltage of the multiplier.

- A typical multiplier produces an output  $V_o$ , which is proportional to the product of two inputs  $V_x$  and  $V_y$  or  $V_o = KV_x V_y$ , where  $K$  is the scaling factor that is usually maintained as  $(1/10)$   $V^{-1}$ .
- Multiplication techniques are
  - Logarithmic summing technique
  - Pulse height/width modulation technique
  - Variable transconductance technique
  - Multiplication using Gilbert cell
  - Multiplication using variable transconductance
- The Linearity Error is the maximum absolute deviation of the error surface and this character imposes a lower limit on the multiplier accuracy.
- Squaring Mode Accuracy is the maximum deviation of the output voltage from an ideal square-law curve.
- Small signal 3 dB bandwidth of a multiplier defines the frequency  $f_o$  at which the output reduces by 3 dB from its low frequency value for a constant input voltage and it is indicated individually for the  $X$  and  $Y$  input channels. The transconductance bandwidth is the frequency at which the transconductance of the multiplier drops by 3 dB of its low frequency value.
- Quadrant is used to identify the use of multiplier circuit for bipolar input signals. First-quadrant device can accept positive input signals only, the two quadrant device can accept one bipolar signal and one unipolar signal and the four-quadrant device can accept two bipolar signals.
- Logarithmic summing technique uses the relationship  $\ln V_x + \ln V_y = \ln(V_x V_y)$ .
- Since the relationship between  $I_o$  and  $V_{BE}$  of the transistor is  $I_C = I_o e^{(V_{BE}/V_T)}$ , the logarithmic summing technique operates accurately in the range of 10 nA to 10 mA and suffers from low accuracy and high temperature instability beyond that range. This method is applicable only to positive values of  $V_x$  and  $V_y$  and its operation is restricted to one quadrant operation only.

- In pulse height/width modulation technique, the pulse width of a pulse train is made proportional to one input voltage and the pulse amplitude is made proportional to the second input voltage.

- An emitter coupled pair can be used as a multiplier with the change in collector current

$$\Delta I_C = \frac{K_o V_1 (V_2 - V_{BE(on)})}{2V_T}, \text{ and it is the product of the two input voltages.}$$

- The Gilbert multiplier cell which is a modification of the emitter coupled cell forms the basis of many IC

$$\text{multipliers and this cell allows four-quadrant multiplication. It has } \Delta I = I_{EE} \left[ \tanh\left(\frac{V_1}{2V_T}\right) \tanh\left(\frac{V_2}{2V_T}\right) \right].$$

- A modulator or a mixer is a circuit with two inputs, namely, carrier input and modulating input and one modulated output.

- When the magnitudes of  $V_1$  and  $V_2$  are very small compared to  $V_T$ , the hyperbolic  $\tan$  function is approximately linear, and the circuit is used as a multiplier. On the other hand, when  $V_1$  and  $V_2$  are large, a non-linearity function can be used to predistort the input signals which compensates for the hyperbolic tangent transfer characteristic of the basic cell. The required nonlinearity function is an inverse hyperbolic tangent function. When inverse hyperbolic tangent function block is used, the

$$\text{non-linearity of the inputs is compensated which offers } \Delta I = I_{EE} \left( \frac{K_1 V_1}{I_{o1}} \right) \left( \frac{K_2 V_2}{I_{o2}} \right).$$

- The complete four-quadrant analog multiplier using Gilbert cell using voltage-to-current converters or

$$\text{current-to-voltage converters obtains } V_o = K_o \left( \frac{I_9 - I_{10}}{I_9 + I_{10}} \right) (I_1 - I_2) = \frac{K_o V_1 V_2}{I_{XX} K_1 K_2} = K_m V_1 V_2$$

$$\text{where } K_m = \frac{K_o}{I_{XX} K_1 K_2}.$$

- Variable transconductance multiplier makes use of the dependence characteristic of the transistor transconductance parameter on the emitter current bias applied. The relationship between  $V_o$  and  $V_x$  is given by  $V_o = g_m R_L V_x$  where  $g_m = I_{EE}/V_T$  is the transconductance of the stage. Applying a second input  $V_y$  to the reference current source of the differential amplifier can vary  $g_m$  effectively producing multiplication.

- A typical four-quadrant multiplier circuit finds the product of two input voltages regardless of the polarity of inputs and they can operate in all the four quadrants of operation.

- Analog multiplier ICs are used to find the product of instantaneous value of two individual input voltages. They find use in multiplication, division, squaring and square-rooting of signals, frequency doubling, phase angle detection, rectification, modulation and demodulation.

- AD633 is a four-quadrant analog multiplier possessing high input impedance and it can operate with supply voltages ranging from  $\pm 8$  V to  $\pm 18$  V without the need of any external components and calibration. The typical input signal range is  $\pm 10$  V.

## REVIEW QUESTIONS

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1. Write notes on basic analog multiplication techniques.
2. What are the basic characteristic parameters of an analog multiplier? Comment on the performance of a multiplier.
3. Using Eq. (9.2), show that the circuit can perform the multiplication of two analog input signals.
4. Define the terms Accuracy, Linearity, Squaring mode accuracy, Bandwidth and Quadrant of operation as applied to a multiplier.
5. What are logarithmic multipliers?

6. Explain the operation of a multiplier for multiplying two analog signals using logarithmic and antilogarithmic amplifiers.
7. What is the effect of passing a signal through a log or antilog amplifier?
8. Explain one, two and four quadrant multipliers.
9. What are the typical multiplication techniques used for monolithic realisation of a multiplier? Compare them.
10. Explain an emitter-coupled transistor pair for use as a simple multiplier.
11. Explain the basic Gilbert cell with a neat diagram.
12. What are the limitations of a simple Gilbert cell? How do you overcome the limitations?
13. Perform the dc analysis of Gilbert multiplier cell. Comment on linearity of the output obtained from Gilbert multiplier cell.
14. Why do you need predistortion circuits in Gilbert analog multiplier and how do you configure a Gilbert multiplier with predistortion circuits?
15. Derive a circuit arrangement for implementing an inverse hyperbolic tangent function and explain the operation of the circuit.
16. Explain the principle of variable transconductance technique.
17. Explain the operation of a variable transconductance multiplier circuit. Derive the expression for its output voltage.
18. Explain how to convert a simple emitter coupled pair into a two quadrant multiplier.
19. Show the practical implementation of an analog multiplier circuit and explain.
20. Define modulators. How can the multiplier be used as modulator?
21. What are synchronous modulators? Why are they called so?
22. Realise an analog divider circuit using analog multiplier.
23. Draw the circuit of a four quadrant analog multiplier used for frequency multiplication.
24. Design a circuit to convert a 1 kHz sine-wave into a 2 kHz sine-wave.
25. How many multipliers do you need for phase angle detection? How do you use them?
26. Explain how a four quadrant multiplier be obtained from single quadrant multipliers.
27. Power factor can be measured using multipliers. (True / False)
28. Give a scheme using multipliers to find out the power factor of an incoming signal.
29. Discuss any two applications of an analog multiplier IC.
30. Explain the use of multiplier IC as a
  - (a) Squaring circuit
  - (b) Square rooting circuit
  - (c) Voltage divider
  - (d) Phase detector
  - (e) Frequency doubler
  - (f) Rectifier
31. Given (i)  $x_1 = x_2 = 5 \text{ V}$ ; (ii)  $-x_1 = x_2 = 5 \text{ V}$ ; (iii)  $x_1 = -x_2 = 5 \text{ V}$  and (iv)  $x_1 = x_2 = -5 \text{ V}$ . Find the outputs for the combinations of inputs given above and identify the quadrants.
32. Assume for Fig. 9.18, (i)  $x_1 = x_2 = 10\text{V}$ ; and (ii)  $x_1 = x_2 = -10\text{V}$ . Find the outputs for the combinations of inputs.
33. Assume for Fig. 9.19(a)  $v_i = 2.5 \sin 2\pi(5000)t$ . Calculate the output.

# Phase Locked Loop

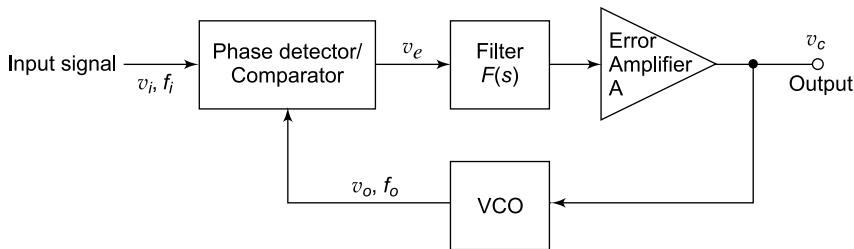
## 10.1 INTRODUCTION

The phase locked loop, commonly called PLL, is a closed loop feedback system, whose output frequency and phase are in lock with the frequency and phase of the input signal. The PLL is an important building block of a linear system, which can detect the phases of two signals and reduce the difference in the presence of a phase difference. The realisation of PLL had been very costly in most industrial and consumer applications. However, the evolution achieved in monolithic IC technology has made the fabrication of IC PLL inexpensive, and the use of PLL is constantly expanding in many applications such as satellite communication systems, FM demodulators, stereo demodulators, tone detectors and frequency synthesisers. This chapter discusses the operation and closed loop analysis of the PLL and the widely used monolithic IC 565. The generation of signals is a basic requirement for a number of commonly used applications. The voltage controlled oscillator (VCO) forms an integral part of the PLL. The commonly used VCO IC 566, and important applications of IC NE/SE565 are also discussed.

## 10.2 OPERATION OF THE BASIC PLL

The basic block diagram of a phase locked loop is shown in Fig. 10.1. The main elements of the PLL are a phase detector/comparator, a low-pass filter, an error amplifier (A) and a voltage controlled oscillator (VCO). The phase detector is fundamentally a multiplier, which generates the sum and difference of the two input signals.

The free running frequency  $f_o$  of the VCO is determined by an externally connected resistor and a timing capacitor. When the loop is locked, the frequency  $f_o$  is directly proportional to an externally applied voltage  $v_c$ , called the *dc control voltage*. When an input periodic signal  $v_i$  of frequency  $f_i$  and VCO output signal  $v_o$  of frequency  $f_o$  are applied to the PLL, the phase detector produces a dc or low frequency signal  $v_e$  which is proportional to the phase difference between the input signal  $v_i$  and the VCO output signal  $v_o$ .



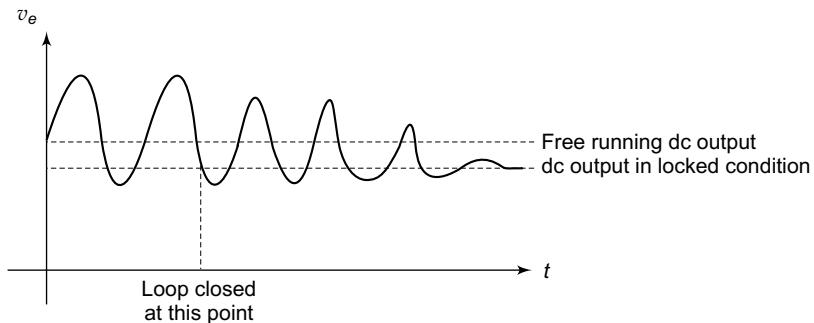
**Fig. 10.1** Basic block diagram of PLL

When the phase sensitive signal from the phase detector is passed through the low-pass filter  $F(s)$ , the high frequency sum component is filtered out. The low frequency difference component passes out of the filter and then amplified by the error amplifier A. This amplified signal is applied to the input of VCO as control voltage  $v_c$ , which changes the VCO frequency  $f_o$  in such a way that the difference between  $f_o$  and  $f_i$  is reduced. If the two frequencies are brought almost identical by this feedback action, then the circuit is said to be *locked*. Once the lock is achieved, the VCO frequency  $f_o$  becomes equal to the input signal frequency  $f_i$  with a finite phase difference  $\phi$ .

**Process of capture** It is an important aspect of PLL, by which the loop achieves the condition of being *in-lock* with a signal from a free-running and unlocked condition. In the unlocked condition of the PLL, the VCO operates at a frequency  $f_c$ , called *centre frequency* or *free running frequency*. This corresponds to an applied voltage of 0V dc at its control input. The capture process is inherently non-linear and starts occurring as described below.

Let us assume that the feedback loop of the PLL is initially open between the loop-filter and VCO control input. An input signal of frequency  $f_i$ , which is assumed to be closer to the VCO centre frequency  $f_c$  applied to the input of the phase detector. The phase detector is usually an analog multiplier that multiplies the two sinusoids together, and it produces the sum and difference of the two signals at its output. Since the high frequency sum component is filtered out by the low-pass filter, the output of the LPF is a sinusoid, whose frequency is equal to the difference between the VCO centre frequency  $f_c$  and incoming signal frequency  $f_i$ .

Considering that the loop is suddenly closed, the difference frequency sinusoid is applied to the VCO input as the control voltage,  $v_c$ . Thus this will make the VCO frequency  $f_o$ , a sinusoidal function of time. Therefore, it alternately moves closer and farther away from  $f_i$ . The output frequency of the phase detector, being the difference between  $f_o$  and  $f_i$ , moves to a higher frequency when  $f_o$  moves away from  $f_i$ , and moves to a lower frequency when  $f_o$  moves closer to  $f_i$ . This fact is reflected in the phase detector output having an asymmetrical wave shape during the capture process as shown in Fig. 10.2. This asymmetry in the waveform produces a dc component in the phase detector output. This dc component shifts the VCO frequency  $f_o$  towards  $f_i$  and the frequency difference gradually diminishes. When the loop is locked, the frequency difference becomes zero, and a dc voltage remains at the loop-filter output.



**Fig. 10.2** Output of phase detector during capture process

The low-pass loop-filter filters out the difference frequency components resulting from interfering signals, which are far away from the centre frequency. It also acts as a memory for the loop, when the

lock is momentarily lost due to a large interfering transient signal. Therefore, the capture-range and pull-in time are dependent on the amount of gain in the loop and the bandwidth of the filter. The signal will be out of capture range when the beat frequency is too high due to the VCO frequency which is far away from the centre frequency. Once lock is achieved, the VCO can track the signal well beyond the capture-range. Reducing the bandwidth of the filter thus improves the *rejectivity* of out-of-band signals, but it reduces the capture range; the pull-in time increases and loop phase margin become less.

The *capture range* of a PLL is defined as the range of input frequencies around the centre frequency within which the loop can get locked from an unlocked condition. The *pull-in time* is the total time required for the loop to get captured with the input signal.

An important feature of PLL is its ability to suppress the noise such as those superimposed on the input signal and the noise generated by the VCO.

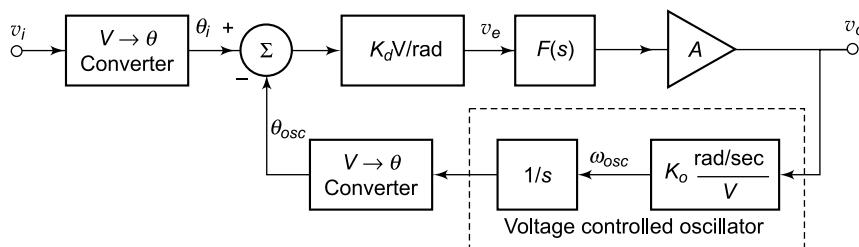
### 10.3 CLOSED LOOP ANALYSIS OF PLL

To study the closed loop analysis of PLL, a more detailed block diagram is used as shown in Fig. 10.3.

Assume that the PLL is initially in locked condition. Also assume that the gain of the phase detector is  $K_d$  Volt/rad of phase difference, the transfer function of the loop-filter is  $F(s)$  and the gain in the forward loop is A.

The input sinusoidal signal  $v_i$  is represented by

$$v_i = V_p \sin(\omega t + \theta_i) \quad (10.1)$$



**Fig. 10.3** Detailed block diagram of PLL

If the phase shift of the signal at the VCO output is  $\theta_{osc}$ , then the average value of the output of the phase detector is

$$v_e = K_d (\theta_i - \theta_{osc}) \quad (10.2)$$

where  $\theta_i$  and  $\theta_{osc}$  are phase shifts with respect to an arbitrarily assumed reference. The phase of the signal at the output of VCO as a function of time is equal to the integral of the VCO output frequency, and it can be expressed as

$$\omega_{osc}(t) = \frac{d\theta_{osc}(t)}{dt}$$

Thus,

$$\theta_{osc}(t) = \int_0^t \omega_{osc}(t) dt + \theta_{osc}|_{t=0}$$

Therefore, the integral component is represented as  $1/s$  inside the VCO block of Fig. 10.3. The oscillator frequency  $\omega_{OSC}$  and the dc control voltage  $v_c$  are actually related by

$$\omega_{OSC} = \omega_c + K_o v_c \quad (10.3)$$

where  $\omega_c$  is the *centre* or *free-running angular frequency* that results when  $v_c = 0$  and  $K_o$  is the VCO gain in rad/s per volt. Then the closed-loop transfer function of the PLL becomes

$$\begin{aligned} \frac{V_c(s)}{\theta_i(s)} &= \frac{K_d F(s) A}{1 + K_d A F(s) \frac{K_o}{s}} \\ &= \frac{s K_d F(s) A}{s + K_d K_o A F(s)} \end{aligned} \quad (10.4)$$

To study the response of the loop to *frequency* variations at the input rather than *phase*, the above equation can be represented as

$$\frac{V_c(s)}{\omega_i(s)} = \frac{V_c(s)}{s \theta_i(s)} = \frac{K_d F(s) A}{s + K_d K_o A F(s)} \quad (10.5)$$

since  $\omega_i = d\theta_i/dt$  and  $\omega_i(s) = s\theta_i(s)$ .

Considering  $F(s) = 1$  with the loop having a first order low-pass frequency response, we have

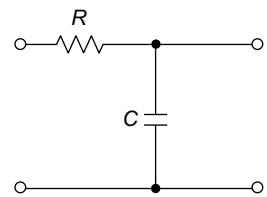
$$\frac{V_c(s)}{\omega_i(s)} = \frac{K_v}{s + K_v} \times \frac{1}{K_o} \quad (10.6)$$

where  $K_v$ , the *loop bandwidth* is given by  $K_v = K_o K_d A$ . Then the loop bandwidth  $K_v$ , is the effective bandwidth, and the loop and capture ranges are very much dependent on  $K_v$ . If  $K_v$  decreases, the capture time rises, and the capture-range reduces. Therefore, the property of interference rejection improves.

**Second order PLL** The first order loop without loop-filter has several limitations such as

- (i) both the sum and difference frequency components are fed to the output from the phase detector and
- (ii) all *out-of-band* interfering signals from the input will appear shifted in frequency at the output.

Therefore, a loop-filter is highly desirable in applications where interfering signals are present. The most common configuration of monolithic PLL is the second-order loop with a loop-filter  $F(s)$  of a simple single-pole, low-pass filter realised with a resistor  $R$  and a capacitor  $C$  as shown in Fig. 10.4.



**Fig. 10.4** Single-pole loop-filter (lag filter)

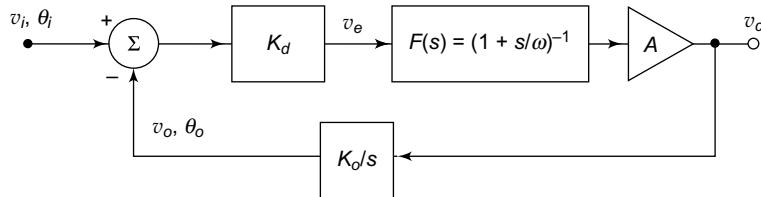
Then,

$$F(s) = \frac{1}{1 + s/\omega} = \frac{1}{1 + s\tau} \quad (10.7)$$

where

$$\omega = \frac{1}{RC} = \frac{1}{\tau}.$$

The resulting block diagram of the second order PLL using single-pole loop-filter is shown in Fig. 10.5. The various dynamic performance requirements of PLL are achieved by the use of different types of filters.



**Fig. 10.5** Block diagram of second-order PLL using single-pole loop filter

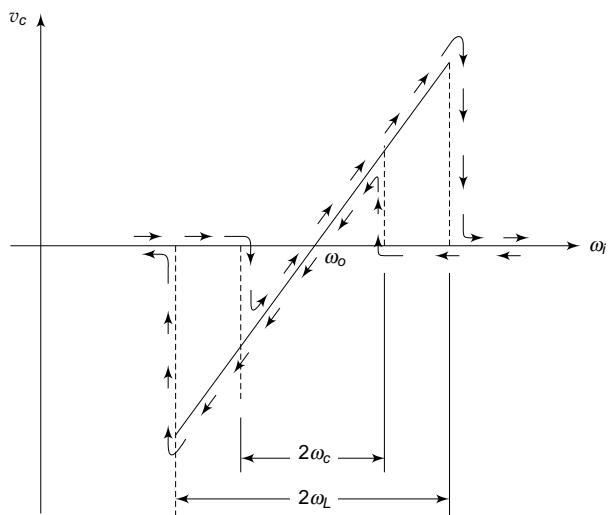
**Loop lock-range and capture-range** The loop *lock-range* is represented as the range of frequencies about  $\omega_o$  for which the PLL maintains the relationship  $\omega_i = \omega_{OSC}$ . If the phase detector can determine the phase difference between  $\theta_i$  and  $\theta_{OSC}$  over a  $\pm\pi/2$  range, then the lock-range is defined as

$$\begin{aligned}\omega_L &= \pm \Delta \omega_{OSC} \\ &= K_d A K_o (\pm \pi/2) \\ &= \pm K_V (\pi/2).\end{aligned}\quad (10.8)$$

The *capture-range* is the range of input frequencies within which an initially unlocked loop will get locked with an input signal. When  $F(s) = 1$ , the capture-range equals the lock-range. If

$$F(s) = \frac{1}{(1 + s/\omega_i)}, \text{ then the capture-range}$$

is smaller than the lock-range. The lock-range and capture-range for such a loop are shown in Fig. 10.6.



**Fig. 10.6** Lock and capture processes of PLL

## 10.4 INTEGRATED CIRCUIT PHASE-LOCKED LOOP

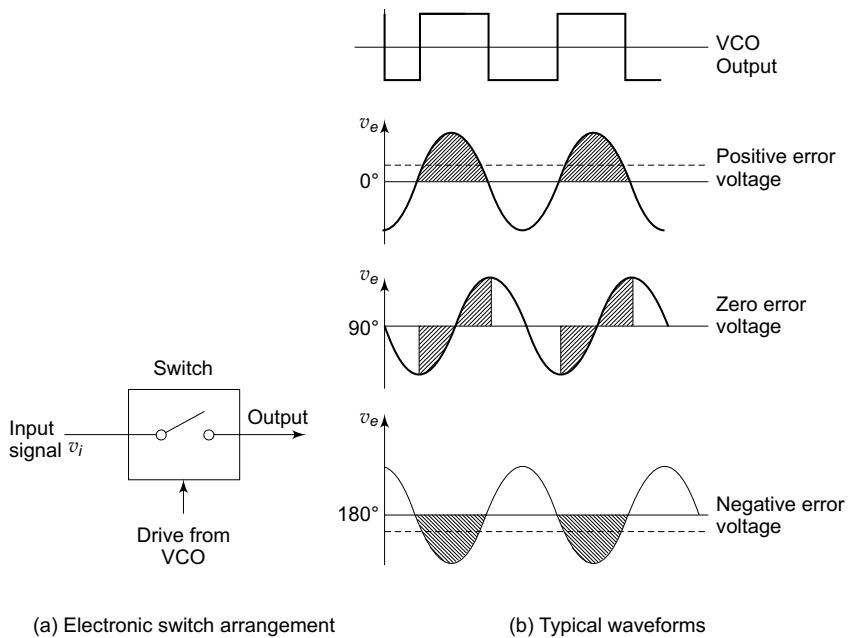
The main reason that the PLL has been widely used as an integrated system component is its feasibility of getting fabricated on a single chip for all the individual PLL components. The component blocks of PLL are discussed in this section.

### 10.4.1 Phase Detector/Phase Comparator

There are two types of phase detectors, namely (i) analog phase detector, and (ii) digital phase detector.

**Analog phase detector** The analog phase detector realised by using an electronic switch is shown in Fig. 10.7(a) and (b). Assuming that the signal from VCO operates the electronic switch, the input sinusoid  $v_i$  is chopped by the VCO frequency. The input sinusoid and the VCO output square wave produce different values of filtered error voltages with respect to various values of phase error  $v_e$ , which

is shown as cross-hatched area in the waveform of Fig. 10.7(b). The output of the phase detector when passed through the filter gives out an average error signal shown as dotted line.



**Fig. 10.7** Analog phase detector using electronic switch

The error voltage is zero when the phase difference between the two inputs equals  $90^\circ$ ; the error voltage is positive for a phase difference of  $0^\circ$  and negative for a phase difference of  $180^\circ$ . In a PLL system configured by this type of phase detector, the PLL achieves a perfect lock when VCO output is in phase quadrature or  $90^\circ$  out of phase with the input.

Considering the input signal  $v_i = V_i \sin \omega_i t$  and VCO output

$$v_o = V_o \sin (\omega_o t + \phi),$$

the phase detector output  $v_e$  becomes

$$v_e = K v_i v_o = K V_i V_o \sin(\omega_i t) \sin(\omega_o t + \phi)$$

where  $K$  is the gain of the phase comparator and  $\phi$  is the phase difference between input signal  $v_i$  and VCO output  $v_o$ . Then,

$$v_e = \frac{K V_i V_o}{2} (\cos(\omega_i t - \omega_o t - \phi) - \cos(\omega_i t + \omega_o t + \phi)).$$

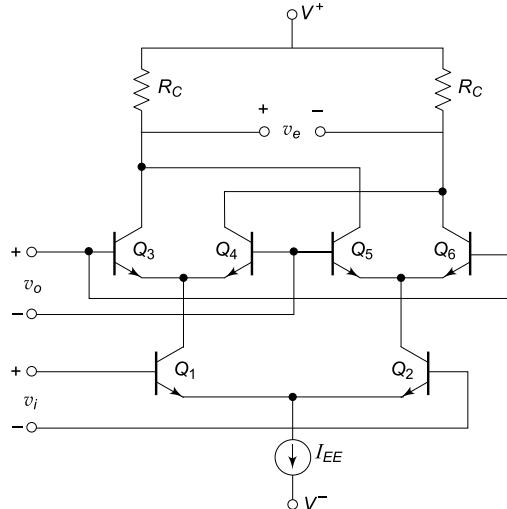
When locked,  $\omega_i = \omega_o$ .

$$\text{Hence, } v_e = \frac{K V_i V_o}{2} (\cos(-\phi) - \cos(2\omega_o t + \phi)) \quad (10.9)$$

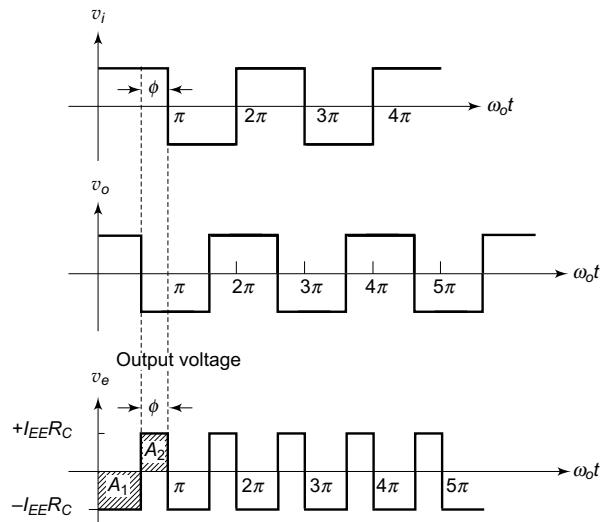
The double frequency term is eliminated by low-pass filter and the dc error voltage is due to the term  $\cos \phi$ . It can be observed that when  $\phi = 90^\circ$ , perfect lock is achieved and hence the error voltage  $v_e = 0$ . From the above equation, it is clear that the output error voltage  $v_e$  is dependent on

- (i) the input signal amplitude  $V_i$ , which makes the phase detector gain and loop gain also dependent on  $V_i$ , and
- (ii)  $\cos \phi$ , that makes the response non-linear.

**Analog phase detector using gilbert multiplier cell** The problem of non-linearity is eliminated in the Gilbert multiplier circuit shown in Fig. 10.8(a). The input signal  $v_i$  is applied to the differential pair  $Q_1 - Q_2$ . The VCO output  $v_o$  is connected to the pairs  $Q_3 - Q_4$  and  $Q_5 - Q_6$  which act as Single-Pole Double-Throw (SPDT) switches. It is assumed that both the phase detector inputs  $v_i$  and  $v_o$  have large amplitudes and that all the transistors behave like switches.



**Fig. 10.8 (a)** Analog phase detector using Gilbert multiplier cell



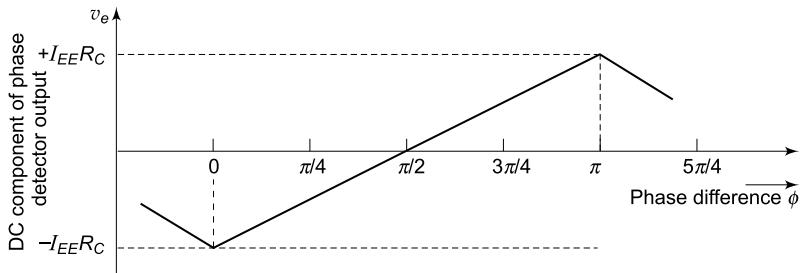
**Fig. 10.8 (b)** Typical input and output waveforms of the analog phase detector

The typical input and output waveforms of the analog phase detector using Gilbert multiplier cell is shown in Fig. 10.8(b). During the interval from 0 to  $(\pi - \phi)$ , both  $v_i$  and  $v_o$  are high. Then, the transistors  $Q_1$  and  $Q_3$  are ON and current  $I_{EE}$  flows through  $Q_3$  and  $Q_1$  providing an output voltage  $v_e = -I_{EE} R_C$ . During the period from  $(\pi - \phi)$  to  $\pi$ , when  $v_i$  is HIGH and  $v_o$  is LOW, transistors  $Q_1$  and  $Q_4$  are ON resulting in an output voltage,  $v_e = I_{EE} R_C$  as shown in the waveform of Fig. 10.8(c).

The average value or the dc component found from the area  $A_1$  and  $A_2$  of the waveform of  $v_e$  is given by

$$\begin{aligned}
 v_e &= -\frac{1}{\pi} [A_1 - A_2] \\
 &= -\left[ \frac{I_{EE} R_C (\pi - \phi)}{\pi} - \frac{I_{EE} R_C \phi}{\pi} \right] \\
 &= I_{EE} R_C \left( \frac{2\phi}{\pi} - 1 \right) \\
 &= \frac{2I_{EE} R_C}{\pi} \left( \phi - \frac{\pi}{2} \right) \\
 &= K_\phi \left( \phi - \frac{\pi}{2} \right)
 \end{aligned} \tag{10.10}$$

where the *phase-angle to voltage* conversion ratio  $K_\phi = \frac{2I_{EE} R_C}{\pi}$ . The linear relationship between  $v_e$  and  $\phi$  is shown in Fig. 10.8(c).



**Fig. 10.8 (c)** Phase detector output  $v_e$  versus the phase difference  $\phi$

**Digital phase detector** The digital phase locked loops employ digital phase detectors. The most commonly used types are:

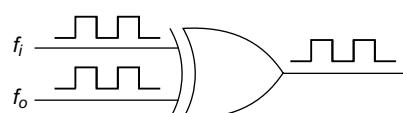
- (i) Phase detector using Exclusive-OR
- (ii) Edge-triggered phase detector using flip-flop, and
- (iii) Monolithic phase detector using charge-pump and quad D-flip flops.

These phase detectors require square-waves for both the input signal and VCO output which forms the second input for the phase detector.

**Exclusive-OR phase detector** The Exclusive-OR phase detector is shown in Fig. 10.9(a). The output of Ex-OR gate circuit is HIGH only when any one of the two input signals, namely  $f_o$  or  $f_i$  is HIGH. The input and output waveforms for  $f_i = f_o$  are shown in Fig. 10.9(b). In a digital phase detector, the phase error  $\phi$  is defined as

$$\phi = \frac{\tau}{T} 2\pi \tag{10.11}$$

where  $T$  is the period of input signals of same frequency and  $\tau$  is the time difference between the leading edges of the two signals. Figure 10.9 (b) shows that  $f_o$  lags  $f_i$  by  $\phi$  degrees and the dc output

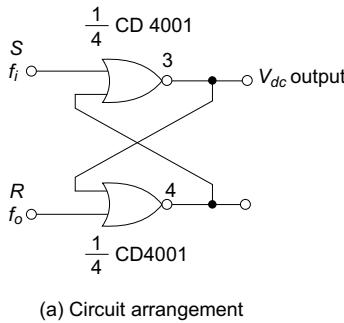


**Fig. 10.9 (a)** Exclusive-OR phase detector

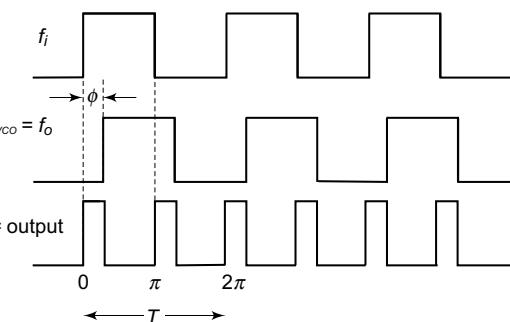
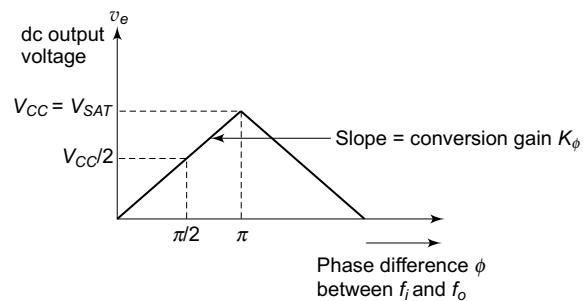
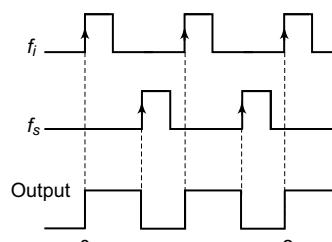
voltage of the Ex-OR gate is a function of the phase error  $\phi$  between the two inputs. Figure 10.9(c) shows the variation of dc output voltage with phase difference  $\phi$ .

Ex-OR phase detector can be realised using ICs such as CD4070. The output dc voltage depends on the duty cycle of the input waveforms. Therefore, this type of phase detector is employed when the waveforms of  $f_i$  and  $f_o$  are of square waveform with 50% duty cycle.

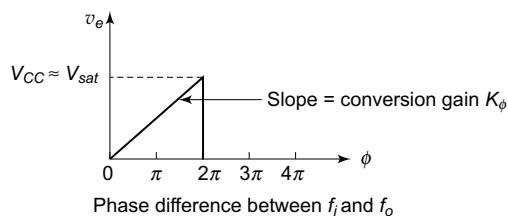
**RS flip-flop phase detector** The RS flip-flop phase detector constructed using NOR gates is shown in Fig. 10.10(a). The input signals,  $f_i$  and  $f_o$ , are connected to the Set and Reset inputs of the RS flip-flop. The output of the RS flip-flop changes its state on the leading edges of  $f_i$  and  $f_o$  as shown in Fig. 10.10(b). The dc value of the output  $Q$  of flip-flop is proportional to the phase difference between the two signals. The change in dc voltage with respect to the phase difference between  $f_i$  and  $f_o$  is shown in Fig. 10.10(c).



(a) Circuit arrangement

**Fig. 10.9 (b)** Input and output waveforms**Fig. 10.9 (c)** The dc output voltage  $v_e$  versus phase difference  $\phi$ 

(b) Input and output waveforms

(c) The dc output voltage  $v_e$  versus phase difference  $\phi$ **Fig. 10.10** RS flip-flop phase detector

The flip-flop phase detector has the following advantages:

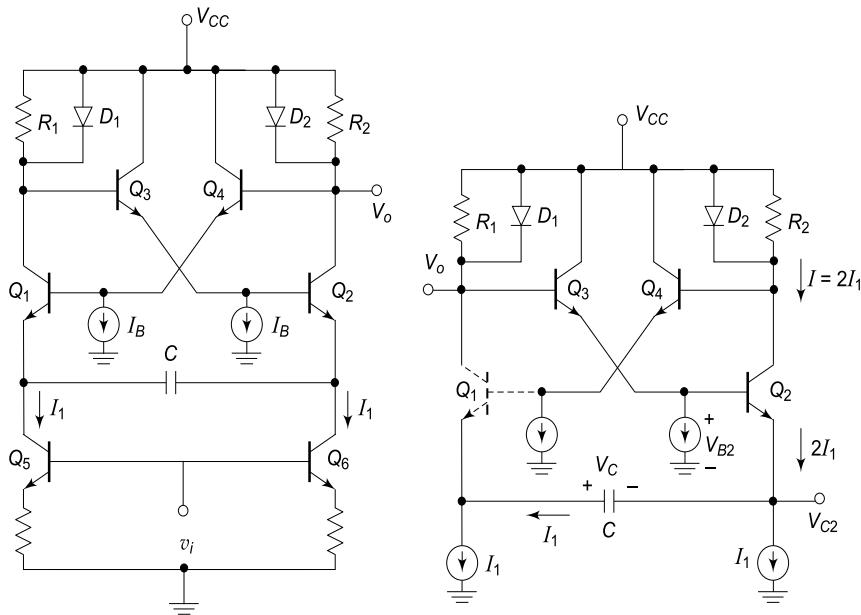
- The dc output voltage is linear over  $2\pi$  radians or  $360^\circ$  and
- It has better capture, tracking and locking characteristics.

## 10.5 VOLTAGE CONTROLLED OSCILLATOR (VCO)

The generation of signals is a basic requirement for a wide variety of applications. Hence, a number of manufacturers fabricate a selection of integrated circuit oscillators and function generators on single chips. Two of the popular ICs are the voltage controlled oscillator and phase locked loop ICs. The voltage controlled oscillator (VCO) is an oscillator whose oscillating frequency varies in response to a control voltage  $v_c$ . It is designed to produce  $f_o = K v_c$ , where  $v_c > 0$  and  $K$  is defined as the *sensitivity* of VCO in rad/volt. The VCO being the most important building block of a monolithic PLL, its desirable properties are:

- Linearity in *voltage-to-frequency* conversion
- Frequency stability against temperature changes and drift characteristics
- High operating frequency and wide tracking range of frequencies and
- High modulation sensitivity  $K_o$  and ease of tuning.

An emitter coupled multivibrator is shown in Fig. 10.11(a). Let us consider that initially  $Q_1$  is OFF and  $Q_2$  is ON as shown in Fig. 10.11(b). The drop across resistor  $R_2$  is assumed large enough to turn the diode  $D_2$  ON. Then the base of  $Q_4$  is one diode drop less than  $V_{CC}$ , and the emitter of  $Q_4$  and the base of  $Q_1$  are two diode drops less than  $V_{CC}$ . Since  $Q_1$  is OFF,  $Q_3$  has its base at  $V_{CC}$  and its emitter at one diode drop below  $V_{CC}$ .



**Fig. 10.11** (a) Voltage-controlled, emitter-coupled multivibrator circuit  
(b) Equivalent circuit during one half-cycle

The current  $I_1$  now charges the capacitor  $C$  with emitter of  $Q_1$  becoming more negative than that of  $Q_2$ . The transistor  $Q_1$  will be ON when its emitter voltage becomes equal to three diode drops below  $V_{CC}$ ,

and the resulting collector current of  $Q_1$  due to voltage drop across resistor  $R_1$  turns  $D_1$  ON. As a result, the base voltage of  $Q_3$  moves in the negative direction by one diode drop. Therefore, the base voltage of  $Q_2$  also moves in the negative direction by one diode drop. The transistor  $Q_2$  will now be turned OFF. Then the current  $I_1$  charges the capacitor voltage in the opposite direction for an amount of two diode drops and hence  $Q_2$  will be switched ON again. Thus, the cycle repeats.

As the circuit is symmetrical, the time required to charge the capacitor is half of the time period. That is,

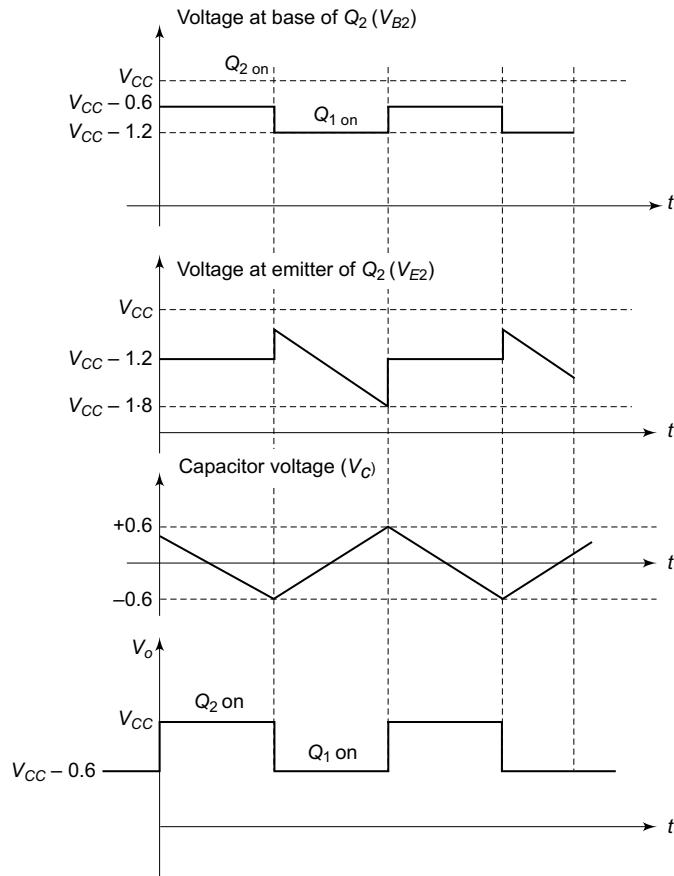
$$\frac{T}{2} = \frac{Q}{I_1} = \frac{C\Delta V}{I_1} = \frac{2CV_{BE(on)}}{I_1}$$

Thus the frequency of oscillation becomes

$$f = \frac{1}{T} = \frac{I_1}{4CV_{BE(on)}} \quad (10.12)$$

The voltage waveforms at various nodes of the circuit are shown in Fig. 10.11(c).

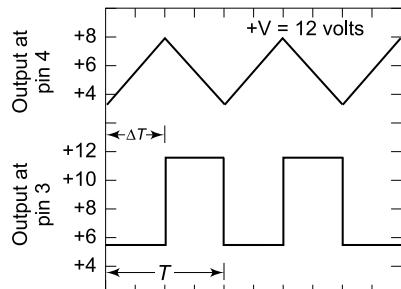
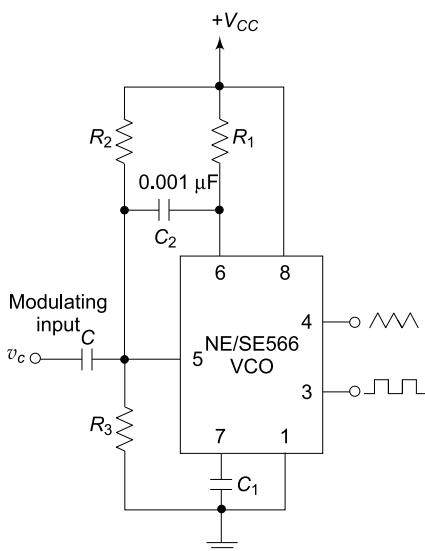
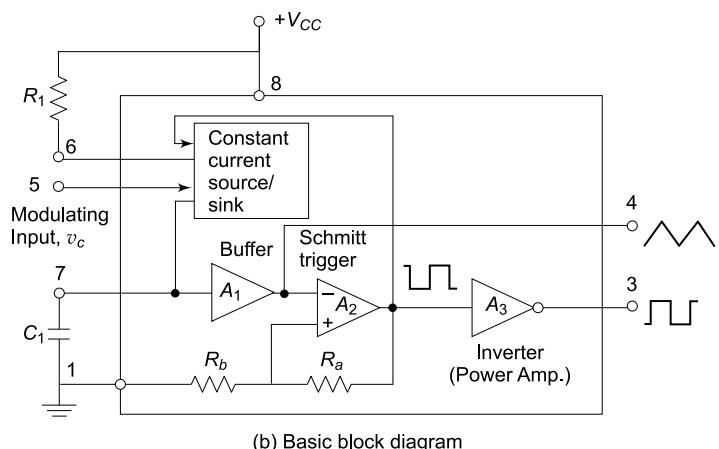
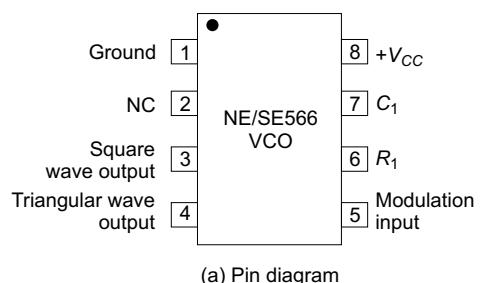
This emitter-coupled VCO is non-saturating and the voltage swings within the circuit are maintained small. Therefore, the circuit operates up to 100 MHz for typical integrated circuit environments. One of the most commonly used VCO is NE/SE566.



**Fig. 10.11 (c)** Voltage waveforms at various nodes

## 10.6 IC VOLTAGE CONTROLLED OSCILLATOR NE/SE566

The pin configuration and the basic block diagram of IC 566 VCO are shown in Fig. 10.12(a) and (b) respectively. The frequency of oscillation is determined by an externally connected resistor  $R_1$  and a capacitor  $C_1$ . The control voltage or the modulating input  $v_c$  is applied at the control terminal (pin 5) as shown in Fig. 10.12(c). The triangular voltage obtained at pin 4 is shown in Fig. 10.12(d). It is generated by alternately charging the capacitor  $C_1$  by one current source, and discharging it linearly through another current source. The amount of charge and discharge voltage swing is determined by the Schmitt trigger. The Schmitt trigger also provides the square-wave output at pin 3 through the power amplifier  $A_3$  and the triangular output is available at pin 4 from the buffer amplifier  $A_1$ .



**Fig. 10.12** Voltage-controlled oscillator

**Operation of VCO** The output voltage swing of the Schmitt trigger is set to the levels  $V_{CC}$  and  $0.5V_{CC}$ . Referring to Fig. 10.12(b), if  $R_a = R_b$  in the positive feedback path, the voltage at the non-inverting terminal of op-amp  $A_2$  swings from  $0.5V_{CC}$  to  $0.25V_{CC}$ . During charging of  $C_1$ , when the voltage across  $C_1$  just exceeds  $0.5V_{CC}$ , the Schmitt trigger switches to LOW ( $0.5V_{CC}$ ) and the capacitor starts discharging. When the voltage across  $C_1$  reduces to  $0.25V_{CC}$ , the Schmitt trigger switches to HIGH ( $V_{CC}$ ) and  $C_1$  starts charging.

By maintaining the source current and sink current of the two current sources equal, a uniform triangular voltage with equal positive and negative slopes is obtained at pin 4. The square-wave output of Schmitt trigger, inverted and buffered is available at pin 3. The waveforms at the output pins 3 and 4 are shown in Fig. 10.12(d).

**Calculation of the free-running frequency  $f_o$  of VCO** The voltage change across the capacitor  $C_1$  is  $\Delta V = 0.25V_{CC}$ . Since constant current sources are used, the rate of change of voltage across the capacitor is given by

$$\frac{\Delta V}{\Delta t} = \frac{i}{C_1}$$

i.e. 
$$\frac{0.25V_{CC}}{\Delta t} = \frac{i}{C_1}$$

or 
$$\Delta t = \frac{0.25V_{CC} C_1}{i} \quad (10.13)$$

The time period  $T$  of the triangular waveform is  $2\Delta t$ . Therefore, the frequency of oscillation  $f_o$  is

$$f_o = \frac{1}{T} = \frac{1}{2\Delta t} = \frac{i}{0.5V_{CC} C_1} \quad (10.14)$$

and 
$$i = \frac{V_{CC} - v_c}{R_l}, \quad \text{where } v_c \text{ is the voltage at pin 5.}$$

Thus, 
$$f_o = \frac{2(V_{CC} - v_c)}{C_1 R_l V_{CC}} \quad (10.15)$$

Therefore, output frequency of VCO can be varied by (i) the external resistor  $R_1$ , (ii) the external capacitor  $C_1$ , or (iii) the control voltage  $v_c$  applied at pin 5. Figure 10.12(c) shows a typical connection diagram for a VCO with modulating input applied at pin 5. The voltage  $v_c$  at pin 5 is set by the voltage divider circuit consisting of  $R_2$  and  $R_3$ . If  $v_c$  is initially set to  $\frac{7}{8}V_{CC}$ , then

$$f_o = \frac{2(V_{CC} - (7/8)V_{CC})}{C_1 R_l V_{CC}} = \frac{1}{4R_l C_1} \quad (10.16)$$

**Voltage-to-frequency conversion factor** The voltage-to-frequency conversion factor is determined by  $K_v = \frac{\Delta f_o}{\Delta v_c}$ , where  $\Delta v_c$  is the change in modulating signal required to produce a corresponding shift  $\Delta f_o$  in frequency. Assuming the centre frequency is  $f_o$  and the new frequency is  $f_1$

$$\begin{aligned} \Delta f &= f_1 - f_o \\ &= \frac{2(V_{CC} - v_c + \Delta v_c)}{C_1 R_l V_{CC}} - \frac{2(V_{CC} - v_c)}{C_1 R_l V_{CC}} \end{aligned}$$

$$= \frac{2\Delta v_c}{C_1 R_l V_{CC}}$$

Therefore,

$$\frac{\Delta f}{\Delta v_c} = K_v = \frac{2}{C_1 R_l V_{CC}}$$

Since,

$$f_o = \frac{1}{4R_l C_1}, \text{ the above equation becomes}$$

$$K_v = \frac{8f_o}{V_{CC}} \quad (10.17)$$

The triangular and square-waveforms are buffered so that their output impedance is  $50 \Omega$ , and the typical amplitude swing of the triangular wave is 2.4 V and that of the square-wave is 5.4 V.

A low value capacitor of  $0.001 \mu F$  is normally connected between pins 5 and 6 to eliminate any possible oscillations produced in the current sources. NE/SE566 is employed for the frequency range of 500 KHz to 1 MHz, and MC4324/4024 and MC1648 are employed for higher frequency ranges beyond 1 MHz.

### Example 10.1

Determine the change in dc control voltage  $v_c$  during lock, if input signal frequency  $f_s = 20 \text{ kHz}$ , the free running frequency is  $21 \text{ kHz}$  and the V/F transfer coefficient of VCO is  $4 \text{ kHz/V}$ .

**Solution** The VCO frequency is given by  $\frac{\Delta f}{\Delta v_c} = K_v = \frac{21 \times 10^3 - 20 \times 10^3}{\Delta v_c}$

or

$$\frac{1000}{\Delta v_c} = 4000 \text{ Hz/V}$$

Therefore, the change in dc control voltage,  $\Delta v_c = \frac{1000}{4000} = 0.25 \text{ V}$ .

### Example 10.2

For the VCO circuit shown in Fig. 10.12(c), assume  $R_2 = 2.2 \text{ k}\Omega$ ,  $R_1 = R_3 = 15 \text{ k}\Omega$  and  $C_1 = 0.001 \mu F$ . Assume  $V_{CC} = 12 \text{ V}$ . Determine (a) the output frequency, and (b) the change in output frequency if modulating input  $v_c$  is varied from 7 V to 8 V.

#### Solution

(a) As shown in Fig. 10.12(c),  $R_2$  and  $R_3$  form a potential divider.

$$\text{Therefore, } v_c = V_{CC} \times \frac{R_3}{R_2 + R_3} = 12 \times \frac{15 \times 10^3}{(2.2 + 15) \times 10^3} = 10.465 \text{ V}$$

Therefore, the output frequency is

$$f_o = \frac{2(V_{CC} - v_c)}{C_1 R_l V_{CC}} = \frac{2(12 - 10.465)}{0.001 \times 10^{-6} \times 15 \times 10^3 \times 12} = 17.06 \text{ kHz}$$

(b) For  $v_c = 7 \text{ V}$ ,

$$f_o = \frac{2(V_{CC} - v_c)}{C_1 R_l V_{CC}} = \frac{2(12 - 7)}{0.001 \times 10^{-6} \times 15 \times 10^3 \times 12} = 55.556 \text{ kHz}$$

For  $v_c = 8 \text{ V}$ ,

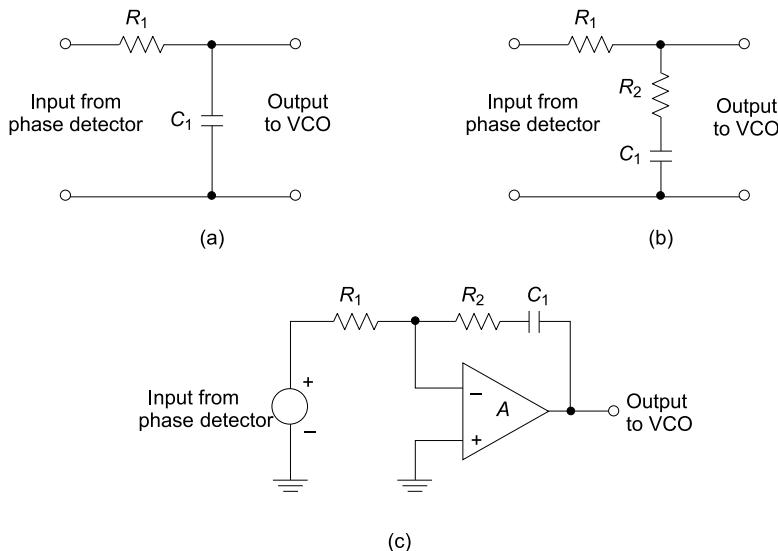
$$f_o = \frac{2(V_{CC} - v_c)}{C_1 R_1 V_{CC}} = \frac{2(12 - 8)}{0.001 \times 10^{-6} \times 15 \times 10^3 \times 12} = 44.444 \text{ kHz}$$

Hence, the change in output frequency =  $(55.556 - 44.444) \text{ kHz} = 11.112 \text{ kHz}$ .

## 10.7 LOW-PASS FILTER

The main function of the low-pass filter in PLL is to remove the high frequency components generated in the output of the phase detector. This filter is also used to eliminate high frequency noise signals and to control the dynamic characteristics such as the capture and lock ranges, bandwidth and transient response of the PLL. If the bandwidth of the filter is reduced, its response time increases at the cost of reduced capture range. The filter also serves another important purpose by acting as a short time *memory* when momentary losses of signal occur, with the dc voltage on the capacitor continuing to shift the frequency of VCO until the signal is picked up again.

The loop-filter employed in PLL may be one of the three types shown in Fig. 10.13 (a), (b) and (c). An amplifier is generally added for the passive filters shown in Fig. 10.13 (a) and (b). The active filter shown in Fig. 10.13 (c) includes gain in its design.



**Fig. 10.13** Low-pass Filters (a) and (b) Passive filters and (c) Active filter

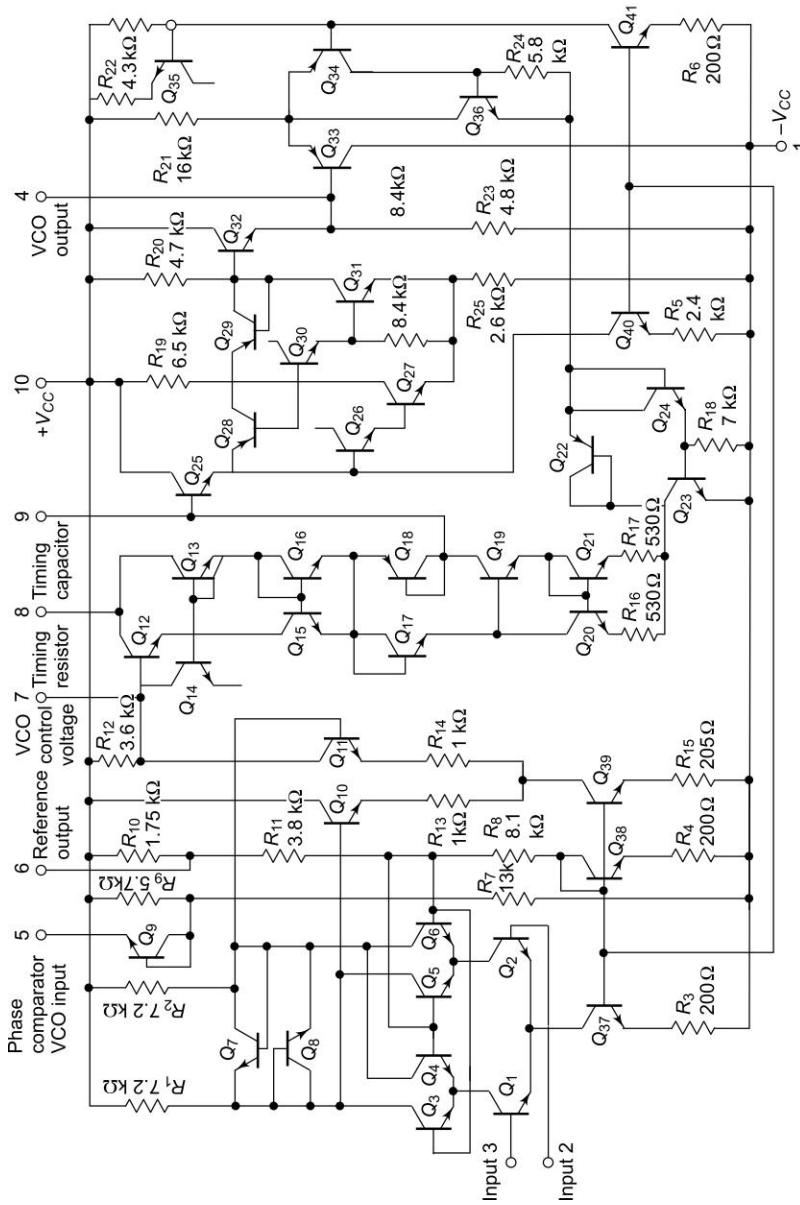
## 10.8 MONOLITHIC PHASE-LOCKED LOOP

The first practical monolithic PLLs developed were 560/561/562 series. Some of the important monolithic PLLs are the SE/NE560 series from Signetics and the LM560 series from National Semiconductor Corp. The SE/NE560, 561, 562, 564, 565 and 567 series differ mainly with respect to their operating frequency range, power supply requirement and bandwidth adjustment ranges. The LM565 being the most commonly used PLL is discussed in this section. These PLL circuits consist of a Gilbert type phase detector, a temperature-compensated VCO and facility for connecting an external RC circuit to perform the loop-filter function.

### 10.8.1 LM565 PLL

Figure 10.14 shows the internal circuit diagram of LM565. The analog phase detector circuit of PLL comprises  $Q_1 - Q_2$ ,  $Q_3 - Q_4$  and  $Q_5 - Q_6$  differential amplifier pairs.  $Q_{37}$  and  $R_3$  serve as current-sink bias source. Resistors  $R_1$  and  $R_2$  serve as loads for the phase detector. The diode-connected transistors  $Q_7$  and  $Q_3$  reduce the voltage swing to  $\pm 0.7$  V, and thus the conversion ratio of the PLL becomes

$$K_d = \frac{0.7 - (-0.7)}{\pi} = \frac{1.4}{\pi} \quad (10.18)$$



**Fig. 10.14** Internal Circuit diagram of IC PLL LM565

The balanced output from the phase detector is supplied to the differential transistor pair  $Q_{10} - Q_{11}$  biased by  $Q_{39}$  which acts as the current sink. This stage works for a gain of 1.4 and a single ended output from this stage is taken across  $R_{12}$ . Resistor  $R_{12}$  in combination with the external capacitor connected between pin 7 and ground form the loop-filter.

The transistors  $Q_{12}$  through  $Q_{23}$  form the voltage controlled current source for the VCO. Equal charging and discharging currents are supplied to the external capacitor  $C_1$  connected at pin 9. Resistor  $R_1$  is connected between pin 8 and  $+V_{CC}$ . The Schmitt trigger formed by  $Q_{25}$  through  $Q_{36}$  with the differential amplifier output circuit consisting of  $Q_{33}$  and  $Q_{34}$  form part of VCO. The charging and discharging cycles through the current source are determined by switching the transistors  $Q_{23}$  and  $Q_{24}$  ON or OFF. The transistors  $Q_{14}$ ,  $Q_{26}$ ,  $Q_{30}$  and  $Q_{35}$  connected as diodes generate the desired level shifting.

The pin diagram and block diagram of IC 565 are shown in Fig. 10.15(a) and (b) respectively. The IC 565 is available in 14-pin DIP package and 10-pin Metal Can package. The output of the phase detector is applied to a differential amplifier as shown in Fig. 10.15(b). A single ended output dropped across  $R$  is connected internally to VCO. It is also available as demodulated output at pin 7 of PLL. The resistor  $R$  is part of the low-pass filter. The capacitor  $C$  between pins 7 and 10 along with the internal resistor,  $R$  of 3.6 k $\Omega$  forms the low-pass-filter. The capacitor  $C$  should be large enough to eliminate variations in the demodulated output voltage at pin 7.

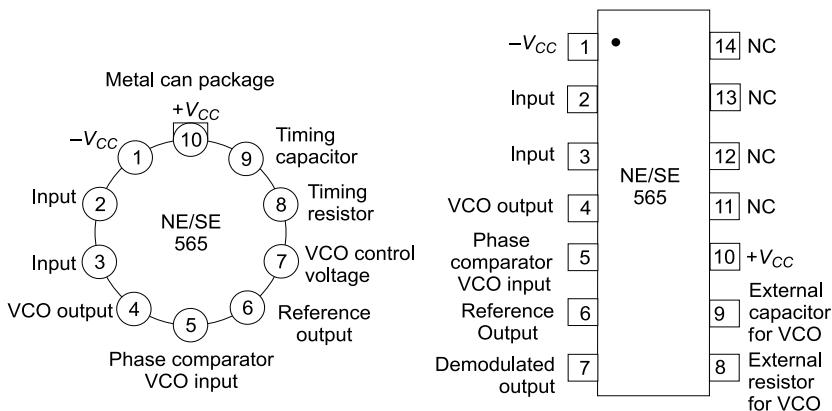
When dual power supplies are used, the power supply requirement for the 565 is any value in the range from  $\pm 6$  V to  $\pm 12$  V. When a single power supply is used, the supply voltage can be between +12 V and +24 V.

The important operating characteristics of LM565 as observed at an operating voltage range of  $\pm 6$  V and  $T_A = +25^\circ\text{C}$  are given below:

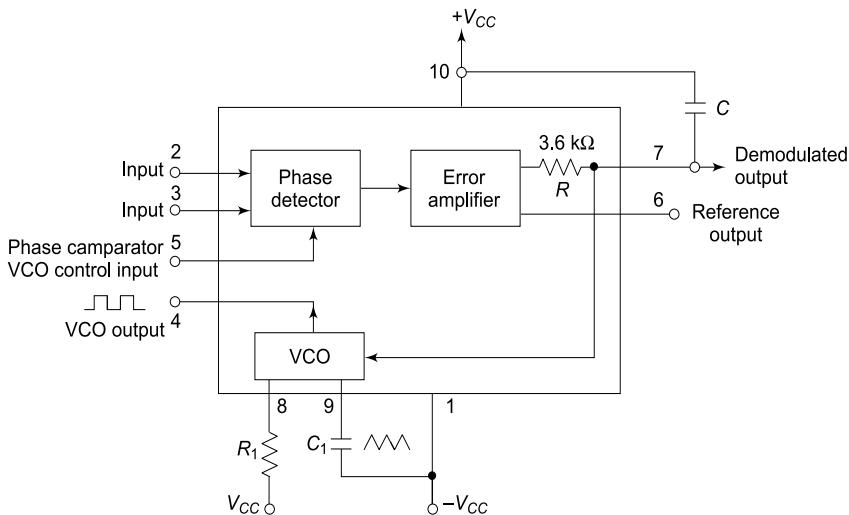
<b>Maximum power dissipation</b>	: 300 mW
<b>Phase Detector</b>	
Input impedance	: 5 k $\Omega$
Input level for limiting	: 10 mV
Output resistance	: 3.6 k $\Omega$
Output common mode voltage	: 4.5 V
Offset voltage between pins 6 and 7	: 100 mV
Sensitivity $K_d$	: 0.68 V/rad
<b>Voltage Controlled Oscillator</b>	
Temperature stability	: 200 ppm/ $^\circ\text{C}$
Square-wave output at pin 4	: 5.2 V (p-p)
Triangular wave output at pin 9	: 2.4 V (p-p)
Maximum operating frequency	: 500 kHz
Sensitivity $K_o$	: 4.1 $f_o$ rad/sec/V
<b>Demodulated Output Characteristics</b>	
Output Voltage level at Pin 7	: 4.5 V
Maximum Voltage Swing	: 2 V (p-p)
Offset Voltage (V6–V7)	: 50 mV
Offset Voltage Vs Temperature (Drift)	: 100 $\mu\text{V}/^\circ\text{C}$
<b>Closed-loop Performance</b>	
Loop gain $K_o K_d$	: $2.79 f_c/\text{sec.}$
A 0.001 $\mu\text{F}$ capacitor is connected between pins 7 and 8 to avoid oscillations due to parasitic effects.	
The free running or centre frequency of VCO is	

$$f_o \equiv \frac{1.2}{4R_1 C_1} \quad (10.19)$$

where  $R_1$  and  $C_1$  are the external resistor connected to pin 8 and the external capacitor connected to pin 9 respectively as shown in Fig. 10.15(b).



**Fig. 10.15** NE/SE565 PLL (a) 10 pin and 14 pin diagrams



**Fig. 10.15** (b) Block diagram of IC LM565

The values of  $R_1$  and  $C_1$  determine the centre frequency of VCO. The value of  $R_1$  is chosen between 2 k $\Omega$  and 20 k $\Omega$ . The device can achieve lock with an input signal over  $\pm 60\%$  of bandwidth with respect to the centre frequency. Pins 2 and 3 form the two input terminals of IC565. The input signal can also be direct-coupled without any dc voltage difference between the pins, and the dc resistances seen from pins 2 and 3 being equal.

**Derivation of lock-in range** Assume  $\phi$  radians is the phase difference between the input signal and the VCO voltage. Then the output voltage  $v_e$  of the analog phase detector is given by

$$v_e = K_d \left( \phi - \frac{\pi}{2} \right) \quad (10.20)$$

where  $K_d$  is the *phase angle-to-voltage transfer coefficient* of the phase detector. Therefore, the control voltage to VCO is

$$v_c = AK_d \left( \phi - \frac{\pi}{2} \right) \quad (10.21)$$

where A is the voltage gain of the amplifier. This control voltage  $v_c$  shifts VCO frequency from its free running frequency  $f_o$  to a frequency  $f$  represented by

$$f = f_o + K_o v_c$$

where  $K_o$  is the *voltage to frequency transfer coefficient* of the VCO.

When PLL achieves *lock* with signal frequency  $f_i$ , we have

$$f = f_i = f_o + K_o v_c \quad (10.22)$$

From Eqs. (10.21) and (10.22) we get

$$v_c = \frac{(f_i - f_o)}{K_o} = AK_d \left( \phi - \frac{\pi}{2} \right) \quad (10.23)$$

Therefore,

$$\phi = \frac{\pi}{2} + \frac{(f_i - f_o)}{K_o K_d A} \quad (10.24)$$

The maximum output voltage magnitude available from the phase detector occurs for  $\phi = \pi$  and 0 radian as shown in Fig. 10.16 and  $v_e(\max) = \pm K_d \frac{\pi}{2}$  from Eq. (10.10). Then, the corresponding value of the maximum control voltage available to drive the VCO is given by

$$v_{c(\max)} = \pm \left( \frac{\pi}{2} \right) K_d A \quad (10.25)$$

The maximum VCO swing in frequency that can be achieved is given by

$$(f - f_o)_{\max} = K_o v_{c(\max)} = K_d K_o A \left( \frac{\pi}{2} \right) \quad (10.26)$$

Therefore, the maximum range of signal frequencies over which the PLL can remain locked will be

$$\begin{aligned} f_i &= f_o \pm (f - f_o)_{\max} \\ &= f_o \pm K_d K_o A \left( \frac{\pi}{2} \right) = f_o \pm \Delta f_L \end{aligned} \quad (10.27)$$

The lock-in frequency range is  $2\Delta f_L$  and from Eq. (10.27) it is given by

$$\text{Lock-in-range} = 2\Delta f_L = K_d K_o A \pi = K_v \pi \quad (10.28)$$

where  $K_d K_o A = K_v$  is the *loop bandwidth*.

Or,

$$\Delta f_L = K_d K_o A \left( \frac{\pi}{2} \right) = K_v \left( \frac{\pi}{2} \right) \quad (10.29)$$

The *lock-in range* is symmetrically located with respect to the free running frequency  $f_o$  of VCO. For IC PLL 565, using Eq. (10.17), we have

$$K_o = \frac{8f_o}{V}$$

where

$$V = +V_{CC} - (-V_{CC})$$

From Eq. (10.18),  $K_d = \frac{1.4}{\pi}$

and  $A = 1.4$

Hence, from Eq. (10.29), the *lock-in range* becomes

$$\Delta f_L = \pm \frac{7.8 f_o}{V} \quad (10.30)$$

**Derivation of capture range** When PLL is not initially locked to the signal, the frequency of the VCO will be its free running frequency  $f_o$ . The phase angle difference between the input signal and the VCO output voltage will be

$$\phi = (\omega_i t + \theta_i) - (\omega_o t + \theta_o) = (\omega_i - \omega_o)t + \Delta\theta \quad (10.31)$$

Thus the phase angle difference does not remain constant. Using Eq. (10.31), it will change with time at a rate given by

$$\frac{d\phi}{dt} = \omega_i - \omega_o \quad (10.32)$$

The phase detector output voltage will therefore not have a dc component but will produce an ac voltage with a triangular waveform of peak amplitude  $K_d \left( \frac{\pi}{2} \right)$  and a fundamental frequency  $(f_i - f_o) = \Delta f$ .

The low pass filter (LPF) is a simple RC network having the transfer function

$$T(f) = \frac{1}{1 + j(f/f_1)} \quad (10.33)$$

The fundamental frequency term supplied to the LPF by the phase detector will be the frequency difference  $\Delta f = f_i - f_o$ . If  $\Delta f > 3 f_1$ , the LPF transfer function will be approximately,

$$T(\Delta f) = \frac{f_1}{\Delta f} = \frac{f_1}{(f_i - f_o)} \quad (10.34)$$

The voltage  $v_c$  to drive the VCO is,

$$v_c = v_e \times T(f) \times A \quad (10.35)$$

or,  $v_{c(\max)} = v_{e(\max)} \times T(f) \times A$

$$\text{From Eq. (10.25), } v_{c(\max)} = \pm K_d (\pi/2) A \left[ \frac{f_1}{\Delta f} \right]$$

Then the corresponding value of the maximum VCO frequency shift is

$$(f_i - f_o)_{\max} = K_o v_{c(\max)} = K_d K_o (\pi/2) A \left[ \frac{f_1}{\Delta f} \right] \quad (10.36)$$

Letting  $f = f_i$  for the acquisition of signal frequency, the maximum signal frequency range that can be acquired by PLL is

$$(f_i - f_o)_{\max} = \pm K_d K_o \left( \frac{\pi}{2} \right) A \left[ \frac{f_1}{\Delta f_C} \right] \quad (10.37)$$

Now  $\Delta f_C = (f_i - f_o)_{\max}$

Therefore, using Eq. (10.37),

$$(\Delta f_C)^2 = K_d K_o \left( \frac{\pi}{2} \right) A f_1$$

Since

$$\Delta f_L = \pm K_d K_o \left( \frac{\pi}{2} \right) A, \text{ we get}$$

$$(\Delta f_C) \approx \pm \sqrt{f_1 \Delta f_L} \quad (10.38)$$

Therefore, the total capture range is

$$2\Delta f_C \approx 2\sqrt{f_1 \Delta f_L}$$

where the lock-in range =  $2\Delta f_L = K_d K_o A \pi = K_v \pi$ . In the case of PLL IC 565,  $R = 3.6 \text{ k}\Omega$ . Hence the capture range is given by

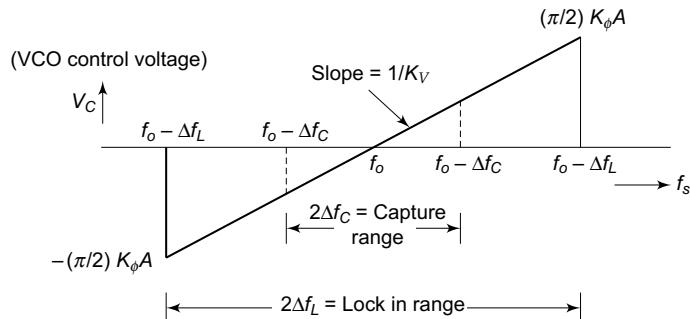
$$\Delta f_C = \pm \left[ \frac{\Delta f_L}{(2\pi)(3.6)(10^3)C} \right]^{\frac{1}{2}} \quad (10.39)$$

where  $C$  is in Farads.

The capture-range is symmetrically located with respect to free running frequency  $f_o$  of VCO as shown in Fig. 10.16. The PLL cannot acquire lock outside the capture-range. Once captured, it will hold-on until the signal frequency goes beyond

the lock-in range. Therefore, in order to increase the lock-in range, larger capture-range is required. However, increasing the capture-range makes the PLL susceptible to noise. Hence, optimisation is to be reached. In practice, the LPF bandwidth is first set for a large value for initial acquisition of signal. When the signal is captured, the bandwidth of LPF is reduced substantially.

This will minimise the interference of undesirable signals and noise.



**Fig. 10.16** Lock-in and capture ranges of PLL

### Example 10.3

For PLL 565, given the free-running frequency as 100 kHz, the demodulation capacitor of  $2 \mu\text{F}$  and supply voltage is  $\pm 6 \text{ V}$ , determine the lock and capture frequencies and identify the component values.

#### Solution

Given  $f_o = 100 \text{ kHz}$ ,  $C = 2 \mu\text{F}$  and  $V_{CC} = \pm 6 \text{ V}$

We know that

$$\Delta f_L = \pm \frac{7.8 f_o}{V} = \pm \frac{7.8 f_o}{+V_{CC} - (-V_{CC})} = \pm \frac{7.8 \times 100 \times 10^3}{+6 - (-6)} = \pm 65 \text{ kHz}$$

Therefore, the lock range =  $2\Delta f_L = 2 \times 65 \text{ kHz} = 130 \text{ kHz}$

$$\begin{aligned} \Delta f_C &= \pm \sqrt{\frac{\Delta f_L}{2\pi \times 3.6 \times 10^3 \times C}} = \pm \sqrt{\frac{65 \times 10^3}{2\pi \times 3.6 \times 10^3 \times 2 \times 10^{-6}}} \\ &= \pm 1.199 \text{ kHz} \end{aligned}$$

The capture range =  $2\Delta f_C = 2 \times 1.199 \text{ kHz} = 2.397 \text{ kHz}$

Referring to Fig. 10.15(b), we know that  $f_o = \frac{1.2}{4R_1C_1}$

Assuming  $R_1 = 12 \text{ k}\Omega$ , a standard value, we have  $100 \times 10^3 = \frac{1.2}{4 \times 12 \times 10^3 \times C_1}$

Therefore,

$$C_1 = \frac{1.2}{4 \times 12 \times 10^3 \times 100 \times 10^3} = 2.5 \times 10^{-10} \text{ F} = 250 \text{ pF.}$$

### Example 10.4

Determine the output frequency  $f_o$ , lock range  $\Delta f_L$  and capture range  $\Delta f_c$  of IC 565. Assume  $R_1 = 15 \text{ k}\Omega$ ,  $C_1 = 0.01 \mu\text{F}$ ,  $C = 1 \mu\text{F}$  and the supply voltage is +12 V.

#### Solution

Given  $R_1 = 15 \text{ k}\Omega$ ,  $C_1 = 0.01 \mu\text{F}$  and  $C = 1 \mu\text{F}$ .

The free running or centre frequency of VCO is

$$f_o \cong \frac{1.2}{4R_1C_1} = \frac{1.2}{4 \times 15 \times 10^3 \times 0.01 \times 10^{-6}} = 2 \text{ kHz}$$

The lock range is given by

$$\Delta f_L = \pm 7.8 f_o / V = \pm 7.8 \times 2000 / 12 = \pm 1.3 \text{ kHz}$$

The capture range is given by

$$\begin{aligned} \Delta f_c &= \pm \left[ \frac{\Delta f_L}{(2\pi)(3.6)(10^3)C} \right]^{\frac{1}{2}} = \pm \left[ \frac{1.3 \times 10^3}{(2\pi)(3.6)(10^3)(1 \times 10^{-6})} \right]^{\frac{1}{2}} \\ &= 239.73 \text{ Hz} \end{aligned}$$

### Example 10.5

Assuming  $C_1 = 470 \text{ pF}$  and  $C = 20 \mu\text{F}$  in the previous problem, calculate the output frequency.

**Solution** The free running or centre frequency of VCO is

$$f_o \cong \frac{1.2}{4R_1C_1} = \frac{1.2}{4 \times 15 \times 10^3 \times 470 \times 10^{-12}} = 42.553 \text{ kHz}$$

The lock range is given by

$$\Delta f_L = \pm \frac{7.8 f_o}{V} = \pm \frac{7.8 \times 42.553 \times 10^3}{12} = \pm 27.66 \text{ kHz}$$

The capture range is given by

$$\begin{aligned} \Delta f_c &= \pm \left[ \frac{\Delta f_L}{(2\pi)(3.6)(10^3)C} \right]^{\frac{1}{2}} = \pm \left[ \frac{27.66 \times 10^3}{(2\pi)(3.6)(10^3)(20 \times 10^{-6})} \right]^{\frac{1}{2}} \\ &= \pm 247.27 \text{ kHz} \end{aligned}$$

## Example 10.6

A PLL has a free running frequency of 300 kHz and the bandwidth of the low pass filter is 50 kHz. Check whether the loop acquires lock for an input signal of 320 kHz.

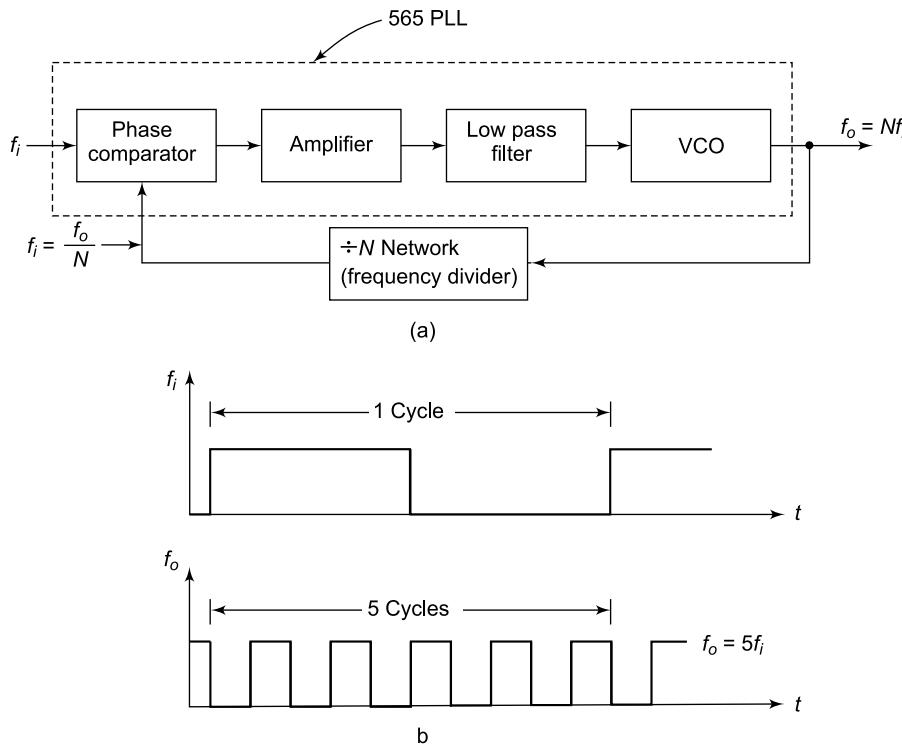
**Solution** The sum frequency of phase detector output =  $(300 + 320)$  kHz = 620 kHz and the difference frequency of phase detector output =  $(320 - 300)$  kHz = 20 kHz. Given the bandwidth of the low pass filter as 50 kHz which is greater than the difference frequency of 20 kHz, the PLL can acquire lock.

## 10.9 APPLICATIONS OF IC 565 PLL

The IC 565 PLL is used for applications such as (i) Frequency Multiplication/Division, (ii) AM Detection, (iii) FM Detection, (iv) FSK modulation/demodulation and (v) Frequency Synthesising.

### 10.9.1 Frequency Multiplication/Division

Figure 10.17(a) shows the block diagram of PLL used for frequency multiplication. A *divide-by-N* network (*frequency divider*) is inserted between the VCO and the phase detector. When the PLL is in locked condition, the output of the frequency divider network is the same as the input frequency  $f_i$ . So, the VCO actually provides the multiple of the input frequency. The desired multiplication factor is achieved by inserting suitable *divide-by-N* network, where  $N$  is an integer. Thus, in locked condition,  $f_o = Nf_i$ . As an example, a *divide-by-5* network can be inserted to achieve the frequency  $5f_i$ .



**Fig. 10.17** Frequency multiplier using IC 565 (a) Block connection diagram, and (b) Input and output waveforms

The frequency multiplication can also be obtained by operating the PLL in harmonic locking mode for input signals, which are rich in harmonics such as a square-wave. Then, the VCO can get directly locked-on to the  $n$ th harmonic of the input signal without the use of a frequency divider network. The value of  $n$  is normally limited to 10 since the amplitude of higher order harmonics decreases as the order increases. Therefore, effective locking may become difficult to achieve.

The circuit shown in Fig. 10.17(a) can also be used for frequency division by locking the  $m$ th harmonic of the square-wave output of VCO with the input signal. Then the output of VCO is given by  $f_d = \frac{f_i}{m}$ . Figure 10.17(b) shows the output waveform of the frequency divider for divide-by-5 circuit.

### Example 10.7

A PLL IC 565 connected as an FM demodulator has  $R_1 = 10 \text{ k}\Omega$ ,  $C_1 = 0.01 \mu\text{F}$  and  $C = 0.04 \mu\text{F}$ . The supply voltage is +12 V. Determine the (a) Free-running frequency, (b) Lock-range and (c) Capture-range.

**Solution** The free running or centre frequency of VCO is

$$f_o \cong \frac{1.2}{4R_1C_1} = \frac{1.2}{4 \times 10 \times 10^3 \times 0.01 \times 10^{-6}} = 300 \text{ kHz}$$

The lock range is given by

$$\Delta f_L = \pm 7.8 f_o / V = 7.8 \times 300 \times 10^3 / 12 = 195 \text{ kHz}$$

The capture range is given by

$$\begin{aligned} \Delta f_C &= \pm \left[ \frac{\Delta f_L}{(2\pi)(3.6)(10^3)C} \right]^{\frac{1}{2}} = \left[ \frac{195 \times 10^3}{(2\pi)(3.6)(10^3)(4 \times 10^{-8})} \right]^{\frac{1}{2}} \\ &= 14.68 \text{ kHz} \end{aligned}$$

### 10.9.2 AM Detection

The PLL can be used as an AM detector for demodulating the amplitude-modulated signals. Assume the AM signal is given by

$$v_m(t) = V_p [1 + m(t)] \sin \omega_c t \quad (10.40)$$

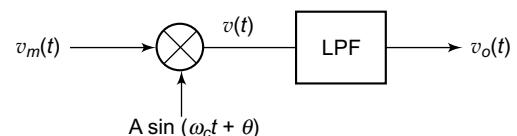
The signal  $v_m(t)$  can be demodulated by multiplying the signal with a local oscillator signal of the same carrier frequency  $f_c$ , as shown in Fig. 10.18.

Then the multiplier output is given by

$$\begin{aligned} v_o(t) &= A V_p [1 + m(t) \sin \omega_c t] \sin(\omega_c t + \theta) \\ &= A V_p [1 + m(t)] \frac{\cos \theta - \cos(2\omega_c t + \theta)}{2} \end{aligned}$$

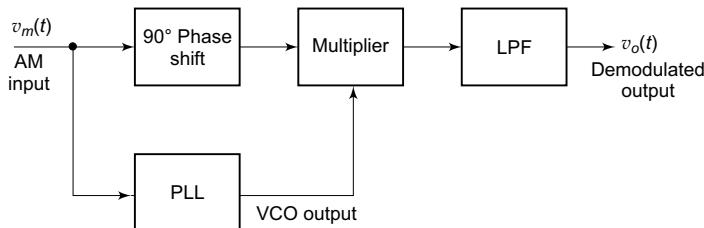
The high-frequency second term can be removed by a low-pass filter, and hence the filter output becomes

$$v_o(t) = V [1 + m(t) \cos \theta] \quad (10.41)$$



**Fig. 10.18** Simple AM detector

where  $V = AV_P$ . This application can be implemented using the PLL as shown in Fig. 10.19. Here the local oscillator signal generated in the PLL is phase-locked with the input signal.



**Fig. 10.19** AM detector using PLL

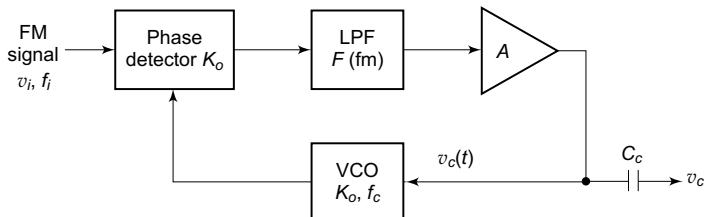
The PLL is locked to the carrier frequency of amplitude-modulated signal. The VCO output of the PLL, which has the same frequency value as the carrier, but unmodulated, is applied as one input to the multiplier. It is to be recalled that under locked condition, the VCO output signal of PLL is  $90^\circ$  out of phase with the input signal. Hence, the AM input signal is phase-shifted by  $90^\circ$  before being applied to the multiplier. The two signals applied to the multiplier, namely, the amplitude-modulated signal and the carrier signal generated in the PLL are now in phase. The output of the multiplier is then passed through the LPF for the removal of the high frequency components. The average value of the output  $V_o(t)$  is thus directly proportional to the amplitude of the input signal.

This AM detector exhibits a high degree of selectivity due to the fact that the PLL responds selectively to the carrier frequencies, which are very close to the VCO output. Due to coherent detection, higher degree of noise immunity is also achieved.

### 10.9.3 FM Detection

Figure 10.20 shows the PLL employed for FM detection. The PLL is set locked with the input FM signal. Then the VCO frequency will be equal to the instantaneous frequency of FM signal  $f_i(t)$  such that

$$f_i(t) = f_c + K_o v_c \quad (10.42)$$



**Fig. 10.20** FM detector using PLL

The VCO control voltage  $v_c$  is the demodulated FM output and  $v_c = \frac{f_i(t) - f_c}{K_o}$ . This error voltage controls the VCO to maintain lock with the input signal. The instantaneous frequency of the FM signal is given by

$$f_i(t) = f_c + \Delta f_c \sin \omega_m t$$

where  $f_c$  is the carrier frequency,  $\Delta f_c$  is the peak frequency deviation and  $\omega_m$  is the angular frequency of the modulating signal.

The ac component of  $v_c(t)$  after the capacitor  $C_c$  is

$$v_c(t) = \frac{f_i(t) - f_c}{K_o} = \frac{f_c + \Delta f_c \sin \omega_m t - f_c}{K_o}$$

Therefore,

$$v_c(t) = \frac{\Delta f_c \sin \omega_m t}{K_o} \quad (10.43)$$

This gives the modulating signal voltage applied to the FM carrier at the transmitter.

The control voltage of VCO is a linear function of the instantaneous frequency deviation. Hence, the FM signal is demodulated, almost without any distortion. Therefore, the PLL can be employed for detection of wideband or narrowband FM signals with a higher degree of linearity, which cannot be achieved by any other detection methods. The centre frequency  $f_o$  should be set as close as possible to the FM carrier frequency  $f_c$  to achieve maximum symmetrical lock-range.

#### 10.9.4 FSK Modulation/Demodulation

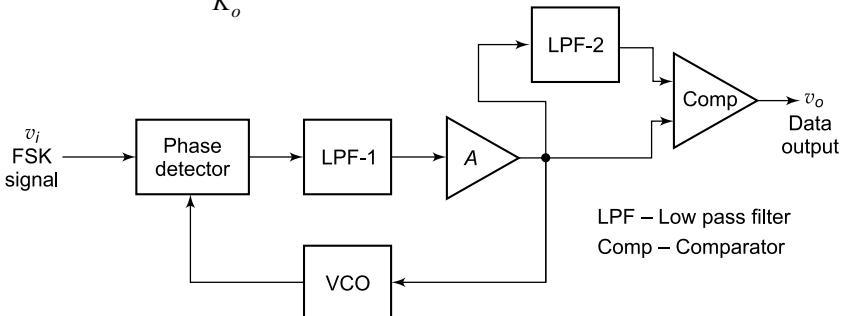
The Frequency Shift Keying (FSK) is a type of frequency modulation, in which the binary data or code is transmitted by means of a carrier frequency that is shifted between two fixed frequency values, namely,  $f_1$  representing logic 0 and  $f_2$  representing logic 1. The frequencies corresponding to logic 1 and logic 0 are called *mark* and *space* respectively.

The block diagram of Fig. 10.21 shows the schematic arrangement for FSK demodulation using PLL. The PLL is designed to remain in-lock with the FSK signal for both the frequencies  $f_1$  and  $f_2$ . Then, the VCO control voltage fed to the comparator is given by

$$V_{f1} = \frac{f_1 - f_o}{K_o} \quad (10.44)$$

and

$$V_{f2} = \frac{f_2 - f_o}{K_o} \quad (10.45)$$



**Fig. 10.21** FSK demodulator using PLL

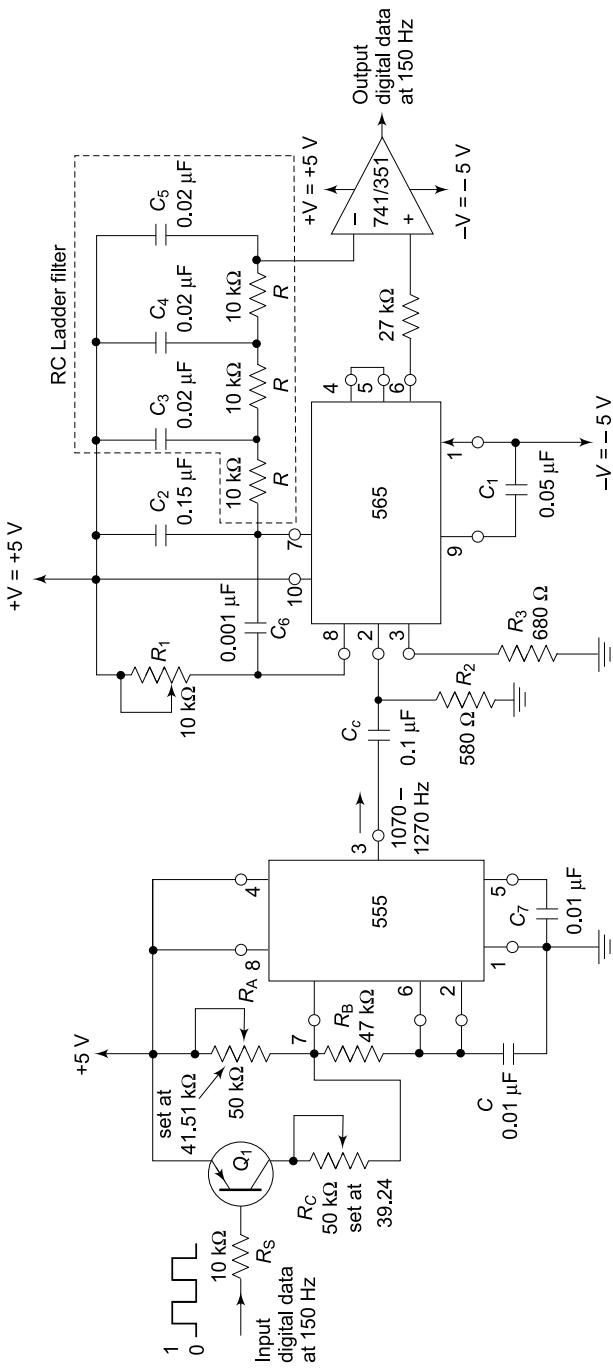
The difference between the two control voltage levels is

$$\Delta V_f = \frac{f_2 - f_1}{K_o} \quad (10.46)$$

Two inputs  $V_{f1}$  and  $V_{f2}$  are applied to the comparator. One of the inputs passes through a second low-pass filter (LPF-2). The filter is designed for a time constant which is longer than the FSK pulse duration to obtain a dc voltage. This dc voltage will have a value midway between  $V_{f1}$  and  $V_{f2}$ .

When the FSK signal  $v_i$  is applied to the input, the loop gets locked to the input frequency and tracks it in between the two frequencies  $f_1$  and  $f_2$ . The corresponding dc shift at the output is made *logic* compatible by adjusting the saturation voltages of the voltage comparator.

A typical and simple circuit diagram for FSK generation and FSK demodulation is shown in Fig. 10.22. The FSK generation is done by an IC 555 timer operated in astable mode, whose frequency at the output is controlled by ON/OFF state of transistor  $Q_1$ . The transistor  $Q_1$  in turn is switched ON by the input digital data applied at its base.



**Fig. 10.22** A practical circuit for FSK generation and FSK demodulation

The frequency values  $f_1$  and  $f_2$ , as determined by the circuit shown in Fig. 10.22 are

$$f_1 = \frac{1.45}{(R_A \parallel R_C + 2R_B)C} = 1270 \text{ Hz}$$

and

$$f_2 = \frac{1.45}{(R_A + 2R_B)C} = 1070 \text{ Hz}$$

The output from the FSK generator is applied to FSK demodulator designed using IC 565. The three stage RC ladder forms the LPF-2 shown in the block diagram of Fig. 10.21 for removing the carrier component.

### 10.9.5 Frequency Synthesising

The Frequency Synthesiser produces a large number of precise frequencies, which are derived from a single reference source of frequency, such as a stable crystal controlled oscillator. The block diagram of Fig. 10.23 shows the principle of frequency synthesising using PLL. A temperature controlled crystal oscillator provides the stable reference frequency  $f_R$ , and the second input signal to phase-detector is provided by the output of VCO. A divide-by- $N$  counter is inserted in the loop as shown in the Fig. 10.23

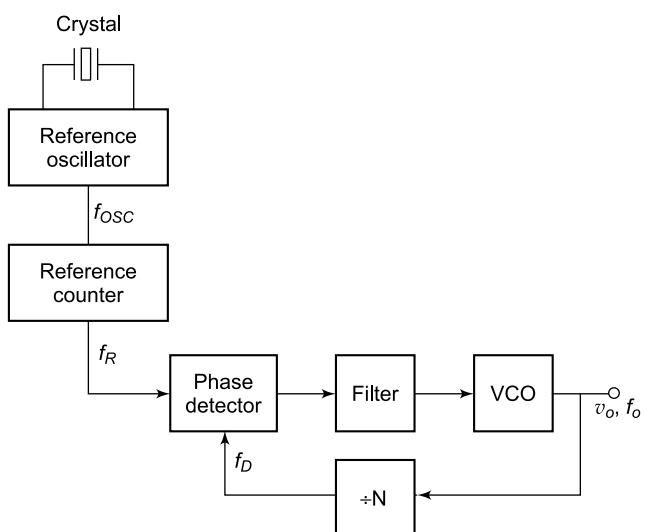
and hence  $f_D = \frac{f_o}{N}$  where  $f_o$  is the output frequency of VCO. In locked condition,  $f_R = f_D$ . Therefore, the output frequency  $f_o$  as observed at the output of VCO is an integral multiple of the reference frequency  $f_R$  or  $f_o = Nf_R$ . The divide-by- $N$  counter is realised with a programmable divider, and therefore, it is possible to achieve multiples of the reference frequency.

The frequency synthesising can also be obtained by *harmonic locking* in which the locking is achieved with the harmonic of the reference signal. Then, the VCO frequency is set to the multiple of the input reference frequency. The VCO then locks-on to the desired harmonic of the input frequency. The drawback of this method of frequency synthesising is that, the lock-range reduces when successively higher and weaker harmonics are used for locking.

The application of IC 565 as frequency synthesiser is shown in Fig. 10.24(a). It employs IC 7490 connected as a *divide-by-6* circuit. The transistor  $Q_1$  is used to drive the counter. When locked, the output of the divider is equal to the input frequency  $f_R$ , and hence  $f_o = 6f_R$ .

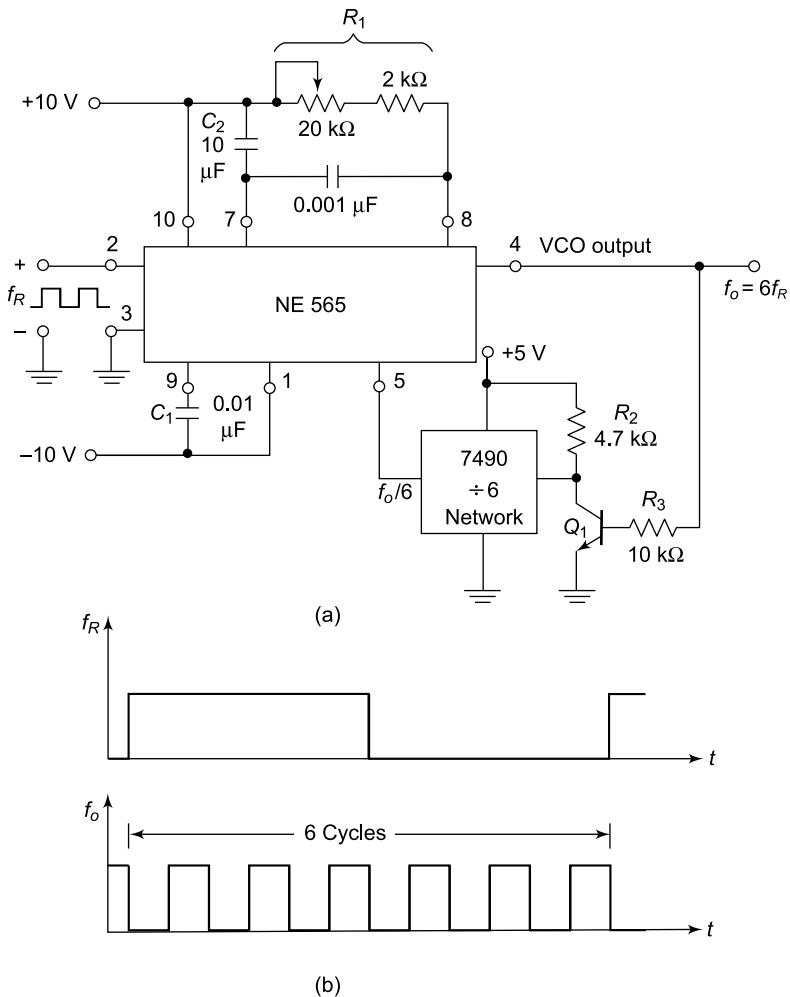
The output frequency  $f_o$  of the VCO is set by the resistor  $R_1$  formed by potentiometer-resistance combination and the capacitor  $C_1$  at pin 9. Adjustment of  $R_1$  provides different frequency values within the predetermined frequency range. For the circuit values shown in Fig. 10.24(a),  $f_o$  can be varied

from 1.5 kHz to 15 kHz using the expression  $f_o \approx \frac{1.2}{4R_1 C_1}$  Hz.



**Fig. 10.23** Block diagram of frequency synthesiser

The input signal  $f_R$  can be a sine or a square-waveform, and the output as obtained at the output VCO is shown in Fig. 10.24(b). The capacitor  $C_3$  eliminates possible oscillations. The frequency stability for VCO can be achieved by using high value for  $C_2$ , viz. around  $10 \mu\text{F}$ .



**Fig 10.24** Frequency multiplier using PLL 565 (a) Circuit arrangement and (b) Input and output waveforms

## SUMMARY

- ❑ The phase locked loop or PLL, an important building block of a linear system is a closed loop feedback system, whose output frequency and phase are in lock with the frequency and phase of the input signal. It can detect the phases of two signals and reduce the difference in the presence of a phase difference.
- ❑ The main blocks of PLL are phase detector/comparator, lowpass filter, error amplifier (A) and voltage controlled oscillator (VCO).

- ❑ In the unlocked condition of the PLL, the VCO operates at a frequency  $f_c$ , called centre frequency or free running frequency which corresponds to an applied voltage of 0 V dc at its control input.
- ❑ The capture range of a PLL is defined as the range of input frequencies around the centre frequency within which, the loop can get locked from an unlocked condition. The pull-in time is the total time required for the loop to get captured with the input signal.
- ❑ The lowpass loop-filter filters out the difference frequency components resulting from interfering signals, which are far away from the centre frequency and it also acts as a memory for the loop, when the lock is momentarily lost due to a large interfering transient signal.
- ❑ Reducing the bandwidth of the filter improves the reactivity of out-of-band signals and it reduces the capture-range, the pull-in time increases and the loop phase margin become less.
- ❑ The closed-loop transfer function of the PLL is given by

$$\frac{V_c(s)}{\theta_i(s)} = \frac{K_d F(s) A}{1 + K_d A F(s) \frac{K_o}{s}} = \frac{s K_d F(s) A}{s + K_d K_o A F(s)}.$$

- ❑ The limitations of first order loop without loop-filter are
  - Both the sum and difference frequency components are fed to the output from the phase detector
  - All out-of-band interfering signals from the input will appear shifted in frequency at the output.
- ❑ The loop lock-range is defined as the range of frequencies about  $\omega_o$  for which the PLL maintains the relationship  $\omega_i = \omega_{OSC}$ . It is defined as

$$\omega_L = \pm \Delta \omega_{OSC} = K_d A K_o (\pm \pi/2) = \pm K_v (\pi/2)$$

- ❑ The capture-range is the range of input frequencies within which an initially unlocked loop will get locked with an input signal. When  $F(s) = 1$ , the capture-range equals the lock-range. If  $F(s) = \frac{1}{(1 + s/\omega_i)}$ , then the capture-range is smaller than the lock-range.
- ❑ The capture-range and pull-in time are dependent on the amount of gain in the loop and the bandwidth of the filter.
- ❑ The two types of phase detectors are analog phase detector and digital phase detector.
- ❑ The analog phase detector output  $v_e = \frac{K V_i V_o}{2} (\cos(-\phi) - \cos(2\omega_o t + \phi))$ . The lowpass filter eliminates the double frequency term and the dc error voltage is due to the term  $\cos \phi$ . The output error voltage  $v_e$  is dependent on the input signal amplitude  $V_i$ .
- ❑ The non-linearity problem of analog phase detector is eliminated in the Gilbert multiplier circuit.
- ❑ The phase-angle to voltage conversion ratio  $K_\phi = \frac{2I_{EE} R_C}{\pi}$ .
- ❑ The commonly used digital phase locked loops are those using Exclusive-OR, edge-triggered phase detector using flip-flop and monolithic phase detector using charge-pump and quad D-flip flops. Ex-OR phase detector can be constructed using ICs such as CD4070.
- ❑ The phase error  $\phi$  of a digital phase detector is  $\frac{\tau}{T} 2\pi$  where  $T$  is the period of same frequency input signals and  $\tau$  is the time difference between their leading edges.
- ❑ The RS flip-flop phase detector are constructed using NOR and their advantages are, the dc output voltage is linear over  $2\pi$  radians or  $360^\circ$  and it possesses better capture, tracking and locking characteristics.
- ❑ The voltage controlled oscillator (VCO) is an oscillator whose oscillating frequency varies in response to a control voltage  $v_c$ . It produces  $f_o = K v_c$ , where  $v_c > 0$  and  $K$  is defined as the *sensitivity* of VCO in rad/volt.

- The desirable properties of VCO are
  - Linearity in *voltage-to-frequency* conversion
  - Frequency stability against temperature changes and drift characteristics
  - High operating frequency and wide tracking range of frequencies
  - High modulation sensitivity  $K_o$  and ease of tuning.
- The frequency of oscillation of VCO is given by  $f = \frac{1}{T} = \frac{I_1}{4CV_{BE(on)}}$ .
- NE/SE566 is a voltage controlled oscillator IC and its oscillation frequency is  $f_o = \frac{2(V_{CC} - v_c)}{C_1 R_1 V_{CC}}$ .
- The output frequency of VCO can be varied by the external resistor  $R_1$ , capacitor  $C_1$ , or the control voltage  $v_c$  applied at pin 5. The voltage  $v_c$  at pin 5 is set by the voltage divider circuit consisting of  $R_2$  and  $R_3$ . If  $v_c$  is initially set to  $\frac{7}{8}V_{CC}$ , then  $f_o = \frac{2(V_{CC} - (7/8)V_{CC})}{C_1 R_1 V_{CC}} = \frac{1}{4R_1 C_1}$ .
- The voltage-to-frequency conversion factor is determined by  $K_v = \frac{\Delta f_o}{\Delta v_c}$ , where  $\Delta v_c$  is the change in modulating signal required to produce a corresponding shift  $\Delta f_o$  in frequency.
- NE/SE566 is employed for the frequency range of 500 kHz to 1 MHz, and MC4324/4024 and MC1648 are employed for higher frequency ranges beyond 1 MHz.
- SE/NE560 series from Signetics and the LM560 series from National Semiconductor Corp., are some of the monolithic PLLs. The SE/NE560, 561, 562, 564, 565 and 567 series differ in operating frequency range, power supply requirement and bandwidth adjustment ranges.
- The conversion ratio of the PLL is  $K_d = \frac{0.7 - (-0.7)}{\pi} = \frac{1.4}{\pi}$ .
- The lock-in range of a PLL is  $\Delta f_L = \pm 7.8f_o/V$ .
- The capture range of a PLL is  $\Delta f_C = \pm \left[ \frac{f_L}{(2\pi)(3.6)(10^3)C} \right]^{\frac{1}{2}}$ .
- The PLL 565 is used in applications such as frequency multiplication, frequency division, AM Detection, FM Detection, FSK modulation and demodulation, and frequency synthesising.
- Frequency Shift Keying (FSK) is a type of frequency modulation, in which the binary data or code is transmitted by means of a carrier frequency, which is shifted between two fixed frequency values  $f_i$  representing logic 0 and  $f_c$  representing logic 1 and the two frequencies are called *mark* and *space* corresponding to logic 1 and logic 0 respectively.
- The frequency synthesiser produces a large number of precise frequencies that are derived from a single reference source of frequency, such as a stable crystal controlled oscillator.
- The frequency synthesising can be made by harmonic locking, in which, locking is achieved with the harmonic of the reference signal.

## REVIEW QUESTIONS

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1. What is PLL?
2. Draw the basic block diagram of a PLL and explain.
3. Define capture-range, lock-range and pull-in time of PLL.
4. Why is capture-range always smaller than the lock-range?
5. Briefly explain the role of LPF in PLL.

6. List the applications of PLL.
7. Explain an analog phase detector with a suitable circuit diagram. Also draw the input and output waveforms.
8. Draw the logic circuit arrangement of a digital phase detector and explain.
9. What are the desirable properties for a VCO?
10. Draw the circuit diagram of a VCO and explain its operation.
11. Draw the block diagram of IC 566 VCO and explain its operation.
12. Derive the expression for free running frequency of VCO.
13. Define voltage-to-frequency conversion factor of VCO.
14. In a VCO, there is a change in frequency for a change in \_\_\_\_\_.  
15. Determine the change in dc control voltage  $v_c$  at lock, if signal frequency  $f_s = 10$  kHz, the free running frequency is 10.5 kHz and the V/F transfer coefficient of VCO is 5 kHz/V.
16. Perform the closed loop analysis of PLL and derive the transfer function of PLL.
17. Derive the expressions for the lock-in and capture ranges of IC 565 PLL.
18. Calculate the output frequency  $f_o$ , lock-range  $f_L$  and capture-range  $f_c$  of IC 565. Assume  $R_1 = 10 \Omega$ ,  $C_1 = 0.01 \mu\text{F}$  and  $C = 20 \mu\text{F}$ .
19. Assuming  $C_1 = 560 \text{ pF}$  in the previous problem, calculate the output frequency.
20. A PLL IC 565 connected for FM detection has  $R_1 = 8.3 \text{ k}\Omega$ ,  $C_1 = 0.001 \mu\text{F}$  and  $C_c = 0.02 \mu\text{F}$ . The supply voltage is +12V. Determine the (a) Free-running frequency, (b) Capture-range and (c) Lock-range
21. A PLL has a free running frequency of 500 kHz and the bandwidth of the low-pass filter is 10 kHz. Will the loop acquire lock for an input signal of 600 kHz? Justify your answer. Assume that the phase detector produces sum and difference frequency components.
22. What are the applications of PLL?
23. Discuss the application of PLL IC for frequency multiplication. Differentiate between frequency multiplication and frequency translation.
24. Using neat sketches, explain how a PLL can be used as frequency translator.
25. Define modulation and demodulation.
26. Draw the circuit diagram of AM detector using PLL and explain its operation.
27. Explain the use of PLL as frequency synthesiser.
28. FM detection can be done using PLL (True/False).
29. Briefly explain the use of PLL for FM detection.
30. Explain the process of FSK demodulation using PLL.
31. What is the use of demodulator in a communication system? What is the advantage of FSK?
32. How is frequency stability obtained in a PLL by the use of VCO?
33. The PLL can be used as a programmable frequency generator (True/False).
34. Find the lock and capture frequencies for PLL 565, with free-running frequency of 120 kHz, demodulation capacitor of 1  $\mu\text{F}$  and supply voltage of  $\pm 5$  V.
35. For the VCO circuit shown in Fig. 10.12(c), assume  $R_2 = 1.5 \text{ k}\Omega$ ,  $R_1 = R_3 = 12 \text{ k}\Omega$ ,  $C_2 = 0.001 \mu\text{F}$  and  $V_{CC} = 10$  V. Calculate the output frequency and the change in output frequency if modulating input  $v_C$  is varied from 7 V to 8 V.

# D/A and A/D Converters

## 11.1 INTRODUCTION

The data converters convert one form of data into another form. Real world processes produce analog signals which carry information pertaining to process variables such as voltage, current, charge, temperature and pressure. The rate of flow of such information may be very slow or very fast. It is difficult to store, manipulate, compare, calculate and retrieve such data with good accuracy using purely analog technology. But, computers can perform these operations quickly and efficiently using digital techniques. Therefore, it is necessary to convert the analog signals from various transducers into its equivalent digital data, which in turn act as the input for digital systems. Thus the requirement for converting analog signal into digital data emerged. The computers also need to communicate with people and physical processes through the use of analog signals, which necessitated the process of digital to analog conversion. This chapter discusses the most common D/A and A/D conversion techniques, D/A converter and A/D converter ICs, delta modulators and demodulators followed by sigma-delta converters and widely used ICs for D/A and A/D conversions.

## 11.2 ANALOG AND DIGITAL DATA CONVERSIONS

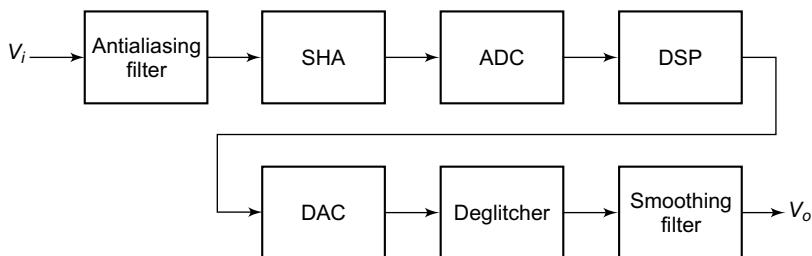
In the application of signal processing, the measurement and analysis of signals are very important to discover their characteristics. If the signal is unknown, the process of analysis begins with the acquisition of the signal. The most common technique of acquiring signals is by *sampling*. Sampling a signal is the process of acquiring its values only at discrete points in time.

The definitions related to the process of sampling and the subsequent analog and digital conversion processes are:

- (i) an *analog signal* is a signal that is defined over a continuous period of time in which the amplitude may assume a continuous range of values.
- (ii) the term *quantisation* refers to the process of representing a variable by a finite set of discrete values.
- (iii) a *quantised variable* is the signal variable that can assume only finite distinct values.
- (iv) a *discrete time signal* is the one that is defined at particular points of time only. Therefore, the independent time variable is quantised. When the amplitude of a discrete-time signal is allowed to assume a continuous range of values, the function is called a *sampled-data* signal. A sampled data signal could result from sampling an analog signal at discrete points of time.
- (v) a *digital signal* is a function, in which the time and amplitude are quantised. A digital signal is always represented by a sequence of *words*, where each word can contain a finite number of *bits* (binary digits).

A D/A Converter (DAC) converts digital data into its equivalent analog data. The analog data is required to drive motors and other analog devices. An A/D converter (ADC) converts analog data into its equivalent digital data, i.e. binary data. The A/D converter and D/A converter are also called *data converters* and they are also available as monolithic integrated circuits.

Figure 11.1 shows a typical application in which A/D and D/A conversions are employed. An analog input signal from a transducer is band-limited by *anti-aliasing filter*. The signal is then sampled at a frequency rate higher than twice the maximum frequency of the band-limited input signal. That is, when the A/D converter is operated at a rate of  $f_s$  samples/second, the highest frequency component of the input signal can be less than  $f_s/2$ . The A/D converters normally require the input to be held constant during the conversion process. Hence, a *Sample-and-Hold Amplifier* (SHA) is introduced in the loop as shown in Fig. 11.1 before A/D converter. The SHA freezes the band-limited signal just before the start of each conversion. The digital signal from A/D converter may be processed, transmitted and recorded in digital form by the digital signal processor (DSP) block. Then, the digital signal is converted into analog signal by D/A converter for use in analog form. The D/A converter is usually operated at the same frequency  $f_s$  as that of A/D converter. The output of D/A converter is commonly a staircase signal, which is passed through a smoothing filter to eliminate the quantisation noise effects. A *deglitcher* may be introduced in the loop before the smoothing process, to remove any output glitches generated during input code variations.



**Fig. 11.1** Sampled data system using A/D and D/A converters

The schematic structure shown in Fig. 11.1 is prevalent either in full or in part in numerous applications such as digital signal processing, direct signal control, digital audio mixing, music and video synthesis, pulse-code modulation (PCM) communication, data acquisition and digital microprocessor based instrumentation.

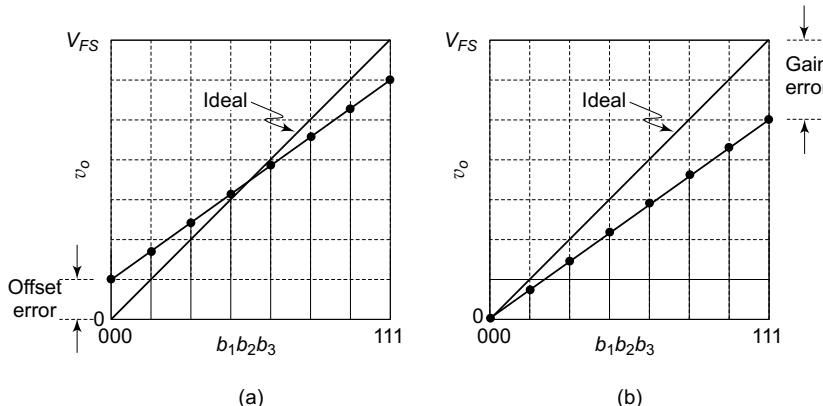
### 11.3 SPECIFICATIONS OF D/A CONVERTER

The important specifications, namely, accuracy, offset voltage, monotonicity, resolution and settling time of D/A converter are discussed below.

**Accuracy** The components in D/A converter circuits are prone to mismatches, drift, ageing, noise and other sources of errors. These factors lead to degradation in conversion performance.

*Absolute accuracy* defines the maximum deviation of the output from the ideal value and it is expressed in fractions of 1 LSB. The D/A converter manufacturers follow different ways of specifying accuracy. The D/A converter errors are classified as *static* and *dynamic errors*.

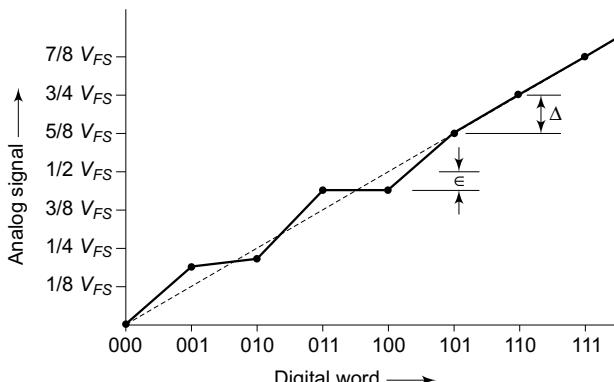
**Offset voltage** The simplest kind of static errors are *offset error* and *gain error*. Ideally, the output of a D/A converter is 0V when all the bits of binary input word are 0s. In practice, however, there is a very small output voltage called *offset voltage* or *offset error* as depicted in Fig. 11.2(a). The offset error is nullified by translating the actual A/D converter characteristics up or down so that it goes through the origin as shown in Fig. 11.2(b). The gain error shown in Fig. 11.2(b) is compensated by adjusting the scale factor  $K$ .



**Fig. 11.2** (a) D/A converter offset and gain errors (b) Nullifying the errors

**Linearity** The most common dynamic errors are *full-scale error* and *linearity error*. *Full-scale error* is the maximum deviation of the output value from its expected or *ideal* value, expressed in percentage of full-scale. *Linearity error* is the maximum deviation in step size from the ideal step size. More expensive D/A converters have full-scale and linearity errors as low as 0.001% of full-scale. General purpose D/A converters have accuracies in the range of 0.01 to 0.1%.

The linearity of a D/A converter is defined as the precision with which the digital input is converted into analog output. An ideal D/A converter produces equal increments in analog output for equal increments in digital input as shown in dotted line curve of the transfer characteristics of Fig. 11.3. However, in an actual D/A converter, the gain and offset errors due to resistors introduce non-linearity as shown by the solid line of the transfer characteristics of Fig. 11.3.



**Fig. 11.3** Linearity error of a 3-bit D/A converter

The *linearity error* measures the deviation of the output from the fitted straight line which passes through the measured output points. It is represented by  $\epsilon/\Delta$  as shown in Fig. 11.3. Commonly, the linearity of D/A converter is specified as less than  $\pm \frac{1}{2}$  LSB meaning that  $|\epsilon| < \frac{1}{2} \Delta$ .

**Differential Nonlinearity (DNL) error** For a D/A converter, the DNL error is the difference between the ideal and the measured output responses for successive D/A converter codes. An ideal D/A converter response would have analog output values exactly one code (1 LSB) apart ( $DNL = 0$ ). A DNL specification of greater than or equal to 1 LSB guarantees monotonicity.

**Integral Nonlinearity (INL) error** For data converters, INL is the deviation of an actual transfer function from a straight line. After nullifying offset and gain errors, the straight line is either a best-fit straight line or a line drawn between the end points of the transfer function. The INL is often called *relative accuracy*.

**Monotonicity** A D/A converter is monotonic if its output value increases as the binary inputs are incremented from one value to the next. That is, the staircase output can have no downward step as the binary input is incremented. Figure 11.3 shows the transfer curve for a non-monotonic D/A converter. The output decreases when the input word changes from 011 to 100.

The monotonic characteristic is important in control applications, without which, oscillations will result. If a D/A converter is identified to be monotonic, the error must be less than  $\pm \frac{1}{2}$  LSB at each output level. Hence, all the D/A converter ICs are designed to have linearity error of less than  $\pm \frac{1}{2}$  LSB.

**Resolution (step size)** Resolution of D/A converter is defined as the smallest change that can occur in the analog output as a result of a change in the digital input. The resolution is always equal to the weight of the LSB and is also known as the step size, since it is the amount of  $V_o$  that will change when the digital input data goes from one step to the next.

Although resolution can be expressed as the amount of voltage or current per step, it is more useful to express it as a percentage of the full-scale output. The percentage resolution is given by

$$\% \text{ Resolution} = \frac{\text{step size}}{\text{full scale}} \times 100 \quad (11.1)$$

Percentage resolution can also be calculated as

$$\% \text{ Resolution} = \frac{1}{\text{total number of steps}} \times 100 \quad (11.2)$$

For an  $n$ -bit digital input, the total number of steps is  $(2^n - 1)$ . Then,

$$\% \text{ Resolution} = \frac{1}{(2^n - 1)} \times 100$$

This means that it is the number of bits which determines the percentage resolution of an A/D converter.

**Settling time** The time required for the output of a D/A converter to settle down to within  $\pm(1/2)$  LSB of the final value for a given digital input is known as *settling time*. It depends on the switching time of the logic circuits, which in turn depends on the inevitable stray capacitances and inductances present in the converter circuit. The settling time normally ranges from 100 ns to 10  $\mu$ s based on the word length and the conversion technique employed.

**Temperature sensitivity** For a fixed digital input, the analog input varies with temperature, normally from  $\pm 50 \text{ ppm}/^\circ\text{C}$  to  $\pm 1.5 \text{ ppm}/^\circ\text{C}$ . This is introduced due to the temperature sensitivity of the reference voltages, the resistors used in the converters, the op-amp and its offset voltage. Therefore, this factor determines the stability of D/A converter.

There are various types of D/A converters, namely, (i) weighted resistor type, (ii) R-2R ladder type, (iii) voltage mode R-2R ladder type and (iv) inverted or current mode R-2R ladder type.

## 11.4 BASIC D/A CONVERSION TECHNIQUES

The D/A converter converts digital or binary data into its equivalent analog value. The input digital data for a D/A converter is an  $n$ -bit binary word  $D$ . The bit  $b_1$  is called the most significant bit (MSB) and bit  $b_n$  the least significant bit (LSB). Then, the quantity  $D$  can be represented by  $D = b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \dots + b_n 2^{-n}$ . The D/A converter accepts the binary input  $D$  and produces an analog output, which is proportional to  $D$  using a reference voltage  $V_R$ . The converted analog value is either in voltage or current form. For a voltage output D/A converter, the conversion characteristic may be expressed as

$$V_o = KV_{FS} \left( b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \dots + b_n 2^{-n} \right) \quad (11.3)$$

where

$V_o$  = output voltage

$V_{FS}$  = full-scale range of voltage

$K$  = scaling factor, usually unity

$b_1 \dots b_n$  =  $n$ -bit binary fractional word with binary point located at the left

$b_1$  = most significant bit (MSB) of weight  $V_{FS}/2$

$b_n$  = least significant bit (LSB) of weight  $V_{FS}/2^n$

The symbolic representation of an  $n$ -bit D/A converter is shown in Fig. 11.4.

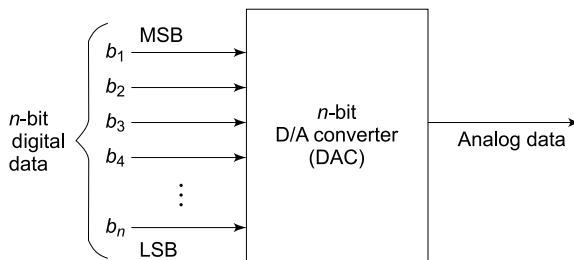


Fig. 11.4  $n$ -bit D/A converter

### 11.4.1 Weighted Resistor Type D/A Converter

In the weighted resistor type D/A converter, each digital level is converted into an equivalent analog voltage or current. In a 4-bit D/A converter which accepts data from 0000 to 1111, there are 15 discrete levels of input above the zero level, and hence it is convenient to divide the output analog signal into 15 levels above zero. The LSB of the digital data causes a change in the analog output that is equal to  $1/15^{\text{th}}$  of the full-scale analog output voltage ( $V_R$ ). Therefore, the weighted resistor network is designed in such a way that a 1 in LSB ( $2^0$ ) position results in  $V_R \times 1/15$  at the output. A 1 in the  $2^1$  bit position must cause a change in the analog output voltage that is equal to  $2/15^{\text{th}}$  of  $V_R$  (i.e. twice the size of the LSB). Similarly, a 1 in  $2^2$  and  $2^3$  bit positions must cause a change of  $V_R \times 4/15V$  and  $V_R \times 8/15V$  respectively

as the analog output. It is important to note that the sum of the weights assigned to various bit positions of a 4-bit D/A converter must be equal to 1, i.e.  $(1/15 + 2/15 + 4/15 + 8/15 = 15/15) V_R = V_{FS}$ . In general, the weight assigned to the LSB is  $1/(2^n - 1)$ , where  $n$  is the number of bits in the digital input.

Thus, the 4-bit weighted resistor network shown in Fig. 11.5 (a) performs the following D/A conversion:

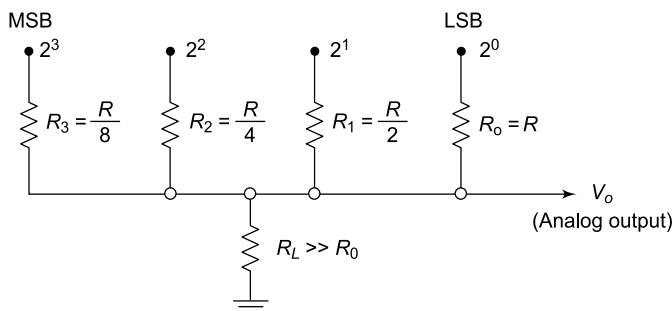
1. The  $2^0$  bit is changed to  $1/15^{\text{th}}$  of  $V_R$ ,  $2^1$  bit to  $2/15^{\text{th}}$  of  $V_R$ ,  $2^2$  bit to  $4/15^{\text{th}}$  of  $V_R$  and  $2^3$  bit to  $8/15^{\text{th}}$  of  $V_R$ .
2. These four voltages are added together to form the analog output voltage using an op-amp summer circuit.

The resistor  $R_0$ ,  $R_1$ ,  $R_2$  and  $R_3$  form the voltage divider network connected with the op-amp and  $R_L$  is the load resistor which should be large enough so as not to load the divider network. The LSB should be connected with the highest input resistance  $R_0$  while the  $2^1$  bit is connected with a resistance of half the value of LSB resistor, i.e.  $R_0/2$ . Therefore, its current contribution at the summing junction of op-amp will be twice that of LSB. The  $2^2$  bit is connected with a  $1/4^{\text{th}}$  of LSB resistance, i.e.  $R_0/4$ . Similarly, the MSB is connected with  $1/8^{\text{th}}$  of the LSB resistance, i.e.  $R_0/8$ . The output is the sum of these four attenuated voltages.

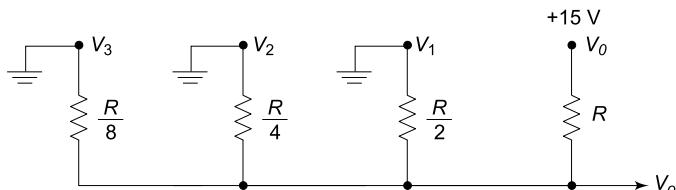
The operating principle of the circuit is explained with the following illustration.

**Illustration** The equivalent circuit of Fig. 11.5(a), when applied with the digital data of 0001, is shown in Fig. 11.5(b). The analog output voltage  $V_o$  can be calculated using Millman's theorem, which states that the voltage at any node in a resistive network is equal to the sum of the currents entering the node divided by the sum of the conductance connected at the node. Then the output voltage is expressed as

$$V_o = \frac{\frac{V_R}{R_0} + \frac{V_R}{R_1} + \frac{V_R}{R_2} + \frac{V_R}{R_3}}{\frac{1}{R_0} + \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}} \quad (11.4)$$



**Fig. 11.5 (a)** Four-bit weighted resistor D/A converter

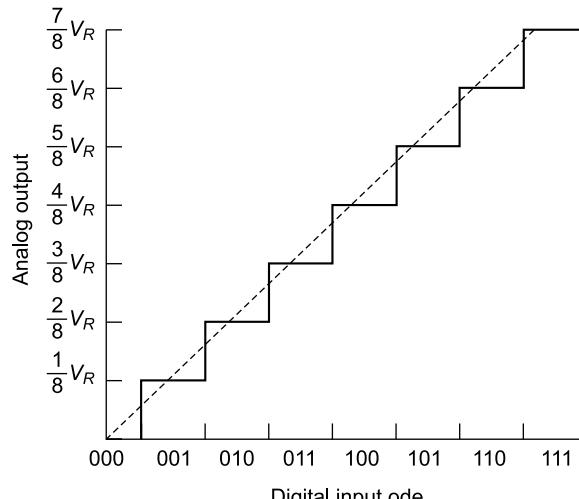
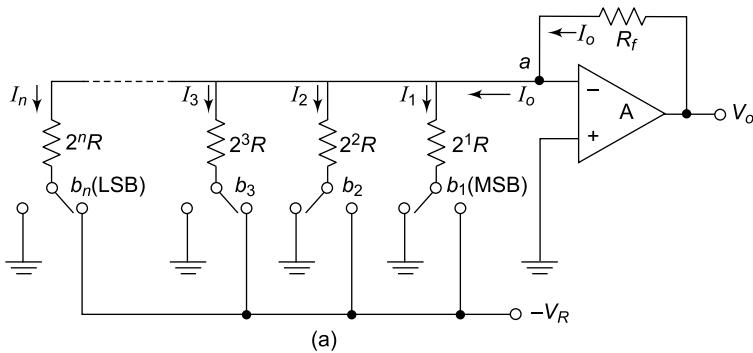


**Fig. 11.5 (b)** Equivalent circuit of a 4-bit weighted resistor D/A converter for input 0001

For the weighted resistor network, assuming  $R_1 = R$ ,  $R_2 = R/2$ ,  $R_3 = R/4$  and  $R_4 = R/8$ , and applying the Millman's theorem to the circuit of Fig. 11.5(b), we get

$$V_o = \frac{\frac{V_R}{R} + \frac{V_R}{R/2} + \frac{V_R}{R/4} + \frac{V_R}{R/8}}{\frac{1}{R} + \frac{1}{R/2} + \frac{1}{R/4} + \frac{1}{R/8}} \quad (11.5)$$

Figure 11.6(a) shows the circuit of an  $n$ -bit D/A converter using op-amp as a summing amplifier. It employs a binary-weighted resistor network to generate the terms  $b_i 2^{-i}$  where  $i = 1, 2, \dots, n$ . The circuit also uses  $n$ -electronic switches controlled by the binary input word  $b_1, b_2, \dots, b_n$  and a reference voltage  $-V_R$ . The switches are of single pole double throw (SPDT) type. If the binary input to a switch is 1, then the switch connects the resistance to the reference voltage  $-V_R$ . When the input bit to the switch is 0, it connects the resistor to ground.



(b)

**Fig. 11.6** An  $n$ -bit weighted resistor D/A converter: (a) Circuit diagram (b) Transfer characteristic

Considering an ideal op-amp A, the output current  $I_o$  is given by

$$\begin{aligned} I_o &= I_1 + I_2 + \cdots + I_n \\ &= \frac{V_R}{2^1 R} b_1 + \frac{V_R}{2^2 R} b_2 + \cdots + \frac{V_R}{2^n R} b_n \\ &= \frac{V_R}{R} [b_1 2^{-1} + b_2 2^{-2} + \cdots + b_n 2^{-n}] \end{aligned}$$

Then the output voltage  $V_o = I_o R_f = \frac{V_R}{R} [b_1 2^{-1} + b_2 2^{-2} + \cdots + b_n 2^{-n}]$  (11.6)

Using Eqs. (11.3) and (11.6), it can be seen that if  $R_f = R$ , then  $K = 1$  and  $V_{FS} = V_R$ .

The  $n$ -bit D/A converter circuit shown in Fig. 11.6(a) uses a negative reference voltage, thus producing a positive staircase voltage. The analog output voltage waveform for 3-bit weighted resistor D/A converter is shown in the transfer characteristics of Fig. 11.6(b) for an input binary word 000, 001, ... 111.

It can be noted that

- (i) The D/A converter output is the result of multiplying the analog signal  $V_R$  by the signal data. Therefore, if  $V_R$  is made variable, then the D/A converter is called a *multiplying D/A converter* [MDAC].
- (ii) Higher the value of  $n$ , finer is the resolution of conversion, and closer is the staircase to a continuous ramp waveform. DACs are available for word lengths ranging from 6 bits to 20 bits or more with 6, 8, 10, 12 and 14 bits being common.
- (iii) The op-amp in Fig. 11.6(a) can be connected in non-inverting mode also.
- (iv) The op-amp is operated as a *current-to-voltage* converter.
- (v) Polarity of  $V_R$  is chosen depending on the switches to be operated.
- (vi) The accuracy and stability of D/A converter are based on the accuracy of resistors and their temperature dependence and the resistors have to handle varying currents based on bit values.
- (vii) The switches are in series with resistors, and therefore the finite ON resistance of the switch must be very low. The bipolar transistor does not perform well as voltage switches due to the voltage offset when it is in saturation. Therefore MOSFET devices are preferred as efficient electronic switches which are discussed in Sec. 11.5.

The main disadvantage of binary weighted D/A converter is the requirement of wide range of resistor values. As the length of the binary word is increased, the range of resistor values needed also increases. For an 8-bit D/A converter, the resistor values to be connected with the bits are  $2^0 R + 2^1 R + \cdots + 2^7 R$ . Therefore, the largest resistor corresponding to bit  $b_8$  is 128 times the value of the smallest resistor corresponding to bit  $b_1$ . The fabrication of such large value of resistors of the order of  $M\Omega$  is not practically possible in monolithic circuit fabrication. In addition, the voltage drop variations across such high value resistors due to the bias currents affect the accuracy. Therefore, the limitations in achieving and maintaining resistor ratios restrict the use of weighted resistor D/A converters to below 8-bits of word length.

The  $R-2R$  ladder type D/A converter is a better choice for practical applications and it overcomes such drawbacks.

### Example 11.1

A system uses a 12-bit word to represent the input signal. If the maximum peak-to-peak voltage at the output is set to 4V, find the resolution of the system and the dynamic range.

**Solution** The 12-bit word can represent  $2^{12}$  or 4096 levels, which are equally spaced across the 4V range. Then, the step size  $= \frac{4\text{ V}}{4096} = 976\mu\text{V}$ . Therefore the system can identify input changes as low as  $976\mu\text{V}$ .

The *dynamic range* gives the ratio of the largest value to the smallest value which can be converted. Therefore, the dynamic range  $\frac{4\text{ V}}{976\mu\text{V}} = 4096$ . The dynamic range in dB is given by  $20 \log_{10} 4096 = 72$  dB.

### Example 11.2

An 8-bit D/A converter has an output of voltage range of 0 to 2.55 V. Find the resolution of the system.

**Solution** An 8-bit D/A converter can identify  $2^8$  or 256 levels. Therefore, the output can have 256 different values starting from 00000000.

$$\text{Then the step size } \frac{2.55\text{ V}}{2^n - 1} = \frac{2.55}{255} = 10\text{ mV.}$$

Therefore, the system can produce output changes as low as 10 mV.

### Example 11.3

A 4-bit R-2R ladder type D/A converter having resistor values of  $R = 10\text{ k}\Omega$  and  $2R = 20\text{ k}\Omega$ , uses  $V_R$  of 10V.

Find (a) the resolution of the D/A converter; and  
 (b)  $I_o$  for a digital input of 1101.

**Solution** Given  $n = 4$ ,  $R = 10\text{ k}\Omega$  and  $V_R = 10\text{ V}$ .

$$\begin{aligned} \text{(a) Resolution of 1 LSB} &= \frac{1}{2^n} \times \frac{V_R}{R} = \frac{1}{2^4} \times \frac{10}{10 \times 10^3} \\ &= \frac{1}{16} \times 1\text{ mA} = 62.5\text{ }\mu\text{A}. \end{aligned}$$

(b) The output  $I_o$  for a digital input of 1101 is

$$I_o = 62.5\text{ }\mu\text{A} \times 13 = 0.8125\text{ mA}$$

(binary 1101 = decimal 13)

### Example 11.4

An 8-bit D/A converter has a resolution of 10 mV/bit. Find the analog output voltage for the inputs

(a) 10001010 and (b) 00010000.

**Solution** The decimal equivalent value  $D = b_82^7 + b_72^6 + b_62^5 + \dots + b_12^0$

(a) For input = 10001010,

$$\begin{aligned} D &= (1)2^7 + 0 + 0 + 0 + (1)2^3 + 0 + (1)2^1 + 0 \\ &= 128 + 8 + 2 = 138 \end{aligned}$$

Therefore,  $V_o = 138 \times 10\text{ mV/bit} = 1.38\text{ V}$

(b) For output = 00010000,

$$D = 0 + 0 + 0 + (1)2^5 + 0 + 0 + 0 + 0 = 32$$

Therefore,  $V_o = 32 \times 10\text{ mV/bit} = 0.32\text{ V}$

### 11.4.2 R-2R Ladder D/A Converter

A wide range of resistor values is required in the design of binary weighted resistor D/A converter. In R-2R ladder D/A converter, resistors of only two values, i.e.  $R$  and  $2R$  are used. Hence, it is suitable for integrated circuit fabrication. The typical values of  $R$  used vary from  $2.5\text{ k}\Omega$  to  $10\text{ k}\Omega$ . The principle of operation of a ladder type network for 4-bit D/A conversion is shown in Fig. 11.7(a), with 4-bit binary input,  $b_1 b_2 b_3 b_4$ , analog output  $V_o$  and one terminating resistor  $2R$ .

In this ladder circuit, the output voltage is a weighted sum of digital inputs. For example, if the 4-bit binary input,  $b_1 b_2 b_3 b_4$  is 1000, i.e. if MSB is 1, while the other three inputs are 0, the circuit shown in Fig. 11.7(a) can be modified as shown in Fig. 11.7(b).

Here, the terminating resistor ( $2R$ ) and the resistor connected to  $b_4$  input ( $2R$ ) are combined at node  $N_1$  to form an equivalent resistor ( $R$ ) as shown in the equivalent circuit of 1<sup>st</sup> stage in Fig. 11.7(c).

Then, at node  $N_2$ , the resistor connected with  $b_3$  input ( $2R$ ) can be combined with the resistor ( $R + R = 2R$ ) to form the 2<sup>nd</sup> stage of equivalent circuit as shown in Fig. 11.7(d).

Similarly, at Node  $N_3$ , the equivalent resistor is  $R$  as shown in the equivalent circuit of stage 3 in Fig. 11.7(e). Then, the analog output voltage  $V_o$  is given by

$$V_o = \frac{V_R \times 2R}{R + R + 2R} = \frac{V_R}{2} \quad (11.7)$$

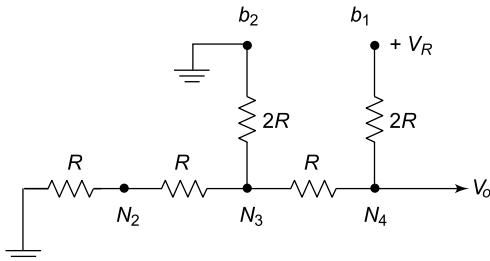


Fig. 11.7 (d) Equivalent circuit of 2<sup>nd</sup> stage

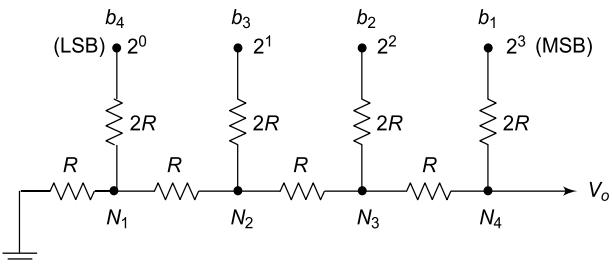


Fig. 11.7 (a) Four-bit R-2R ladder type D/A converter

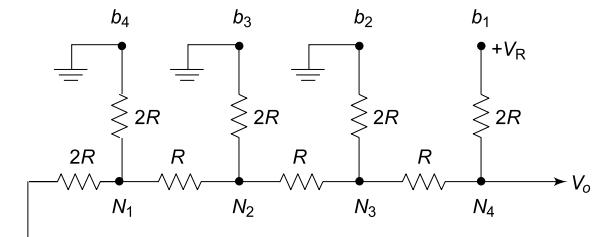


Fig. 11.7 (b) Equivalent circuits for binary input  $b_1 b_2 b_3 b_4 = 1000$

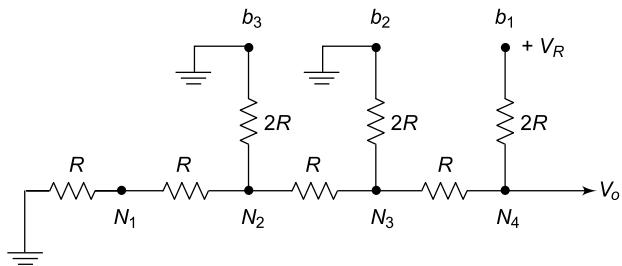


Fig. 11.7 (c) Equivalent circuit of 1<sup>st</sup> stage

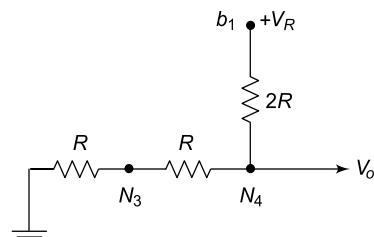


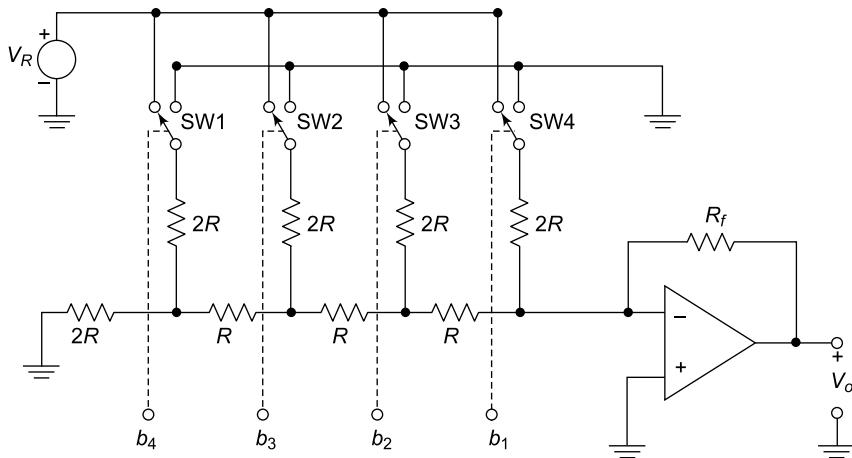
Fig. 11.7 (e) Equivalent circuit of 3<sup>rd</sup> stage

Thus, for digital input  $b_1 b_2 b_3 b_4 = 1000$ , i.e. when MSB = 1, the output is  $V_R/2$ . Similarly, it can be found that for digital input  $b_1 b_2 b_3 b_4 = 0100$ , i.e. when second MSB = 1, the output is  $V_R/4$ ; for  $b_1 b_2 b_3 b_4 = 0010$ , the output is  $V_R/8$  and for  $b_1 b_2 b_3 b_4 = 0001$ , i.e., when LSB = 1, the output becomes  $V_R/16$ .

Since the resistive ladder is a linear network, the principle of superposition can be used to find the total analog output voltage for a particular digital input by adding the output voltages caused by the individual digital inputs. This can be represented for an  $n$ -bit D/A converter as follows:

$$V_o = \frac{V_R}{2^1} + \frac{V_R}{2^2} + \frac{V_R}{2^3} + \cdots + \frac{V_R}{2^n} \quad (11.8)$$

where  $n$  is the total number of bits at the input.



**Fig. 11.8** Four-bit R/2R ladder D/A converter

Figure 11.8 shows a practical circuit arrangement of a 4-bit D/A converter using an op-amp. The inverting input terminal of the op-amp acts as summing junction for the ladder inputs. Using Eq. (11.8) the output voltage  $V_o$  is expressed by

$$\begin{aligned} V_o &= -V_R \frac{R_f}{R} \left( \frac{b_1}{2^1} + \frac{b_2}{2^2} + \frac{b_3}{2^3} + \frac{b_4}{2^4} \right) \\ &= -V_R \frac{R_f}{R \times 2^4} (b_1 2^3 + b_2 2^2 + b_3 2^1 + b_4 2^0) \end{aligned} \quad (11.9)$$

Or, more generally for an  $n$ -bit input signal, assuming  $R_f = R$

$$V_o = -\frac{V_R}{2^n} (b_1 2^{n-1} + b_2 2^{n-2} + \cdots + b_n 2^0)$$

The resolution of the  $R/2R$  ladder type D/A converter with current output is given by

$$\text{Resolution } I = \frac{1}{2^n} \times \frac{V_R}{R} \quad (11.10)$$

The resolution of the  $R/2R$  ladder type D/A converter with voltage output is given by

$$\text{Resolution } V = \frac{1}{2^n} \times \frac{V_R}{R} \times R_f \quad (11.11)$$

where  $R_f$  is the feedback resistance of the op-amp.

### Example 11.5

Consider the  $R - 2R$  4-bit converter of Fig. 11.8 and assume that feedback resistance  $R_f$  of the op-amp is variable, the resistance  $R = 10 \text{ k}\Omega$  and  $V_R = 10\text{V}$ . Determine the value of  $R_f$  that should be connected to achieve the following output conditions.

- (a) The value of 1 LSB at the output is 0.5 V.
- (b) An analog output of 6V for a binary input of 1000.
- (c) The full-scale output voltage of 12 V.
- (d) The actual maximum output voltage of 10 V.

### Solution

- (a) Given  $R = 10 \text{ k}\Omega$ ,  $V_R = 10\text{V}$  and  $n = 4$ . Using Eq. (11.11), for a value of 1 LSB = 0.5 V, we have

$$\frac{R_f \times 10}{10^4 \times 2^4} = 0.5 \quad \text{or} \quad R_f = \frac{10^4 \times 2^4}{10} \times 0.5 = 8 \text{ k}\Omega$$

- (b) For binary value of 1000, using Eq. (11.9) and setting  $b_1 = 1$  and  $b_2 = b_3 = b_4 = 0$ , we get

$$6 = \frac{R_f \times 10 \times 2^{-1}}{10^4} \quad \text{or} \quad R_f = \frac{10^4}{10 \times 2^{-1}} \times 6 = 12 \text{ k}\Omega$$

- (c) For  $V_{FS} = 12 \text{ V}$  we get

$$\frac{R_f \times 10}{10^4} = 12 \quad \text{or} \quad R_f = \frac{10^4}{10} \times 12 = 12 \text{ k}\Omega$$

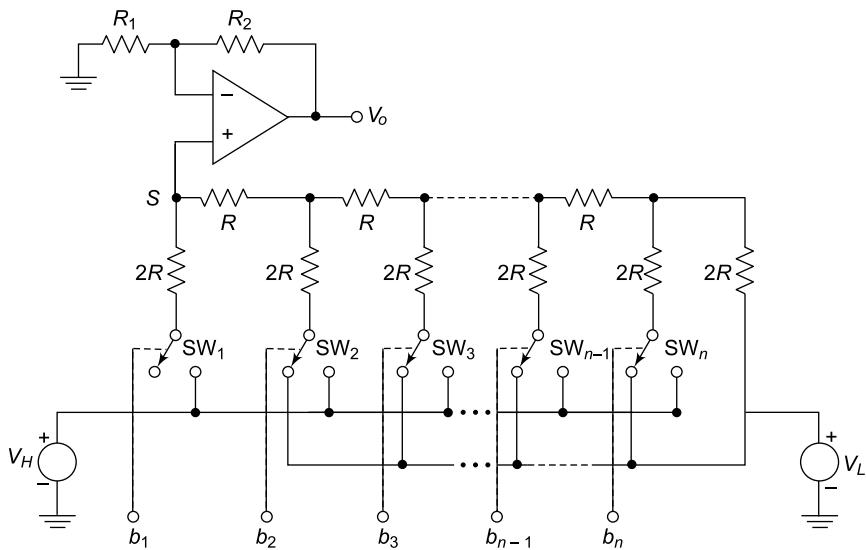
- (d) Let  $b_1 = b_2 = b_3 = b_4 = 1$ . Thus for getting a full scale voltage of 10 V,

$$\frac{R_f \times 10}{10^4} (2^{-1} + 2^{-2} + 2^{-3} + 2^{-4}) = 10$$

That is,  $R_f = \frac{10^4}{10 \times 0.9375} \times 10 = 10.667 \text{ k}\Omega$

### 11.4.3 Voltage Mode $R-2R$ Ladder D/A Converter

Figure 11.9 shows the alternate circuit arrangement of the  $R - 2R$  ladder type called *voltage-mode  $R - 2R$  ladder D/A converter*. The  $2R$  resistors are switched between the two voltage levels  $V_L$  and  $V_H$  as determined by the bit values  $b_1, b_2 \dots b_n$ . The output from ladder is obtained at the left most ladder node  $S$ , and buffered at the output of op-amp. The two voltages  $V_L$  and  $V_H$  can be any two voltage levels. As the input binary word changes from 0...0 (all 0 bits) to 1...1 (all 1 bits), the voltage of node  $S$  changes correspondingly in steps of  $2^{-n}$  ( $V_H - V_L$ ) from the minimum voltage of  $V_o = V_L$  to the maximum of  $V_o = V_H - 2^{-n}(V_H - V_L)$ .



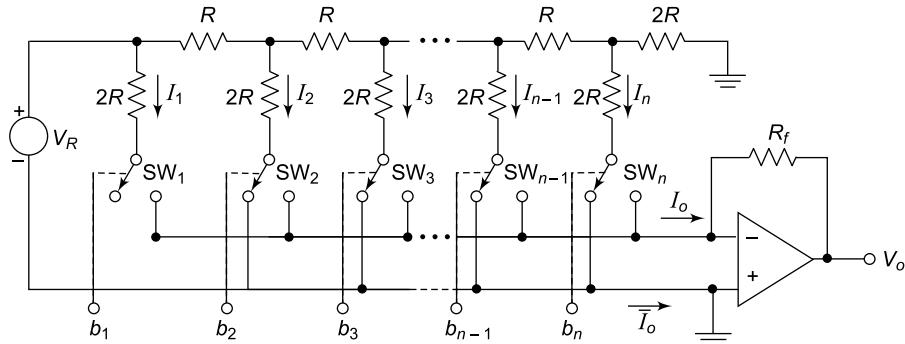
**Fig. 11.9** Voltage-mode R-2R ladder D/A converter

Advantages of  $R-2R$  type D/A converters are

- (i) more accurate selection and design of resistors  $R$  and  $2R$  are possible and
- (ii) the binary word length can be increased by adding required number of  $R-2R$  sections.

#### 11.4.4 Inverted or Current-Mode R-2R Ladder D/A Converter

In weighted resistor and  $R-2R$  ladder types of D/A converters the current flowing through the resistors changes as the input data changes. Power dissipation causes heating, and non-linearity of D/A conversion arises due to varying power dissipation values corresponding to bit patterns. This becomes a serious limitation as the word length increases. This is eliminated in the inverted  $R-2R$  ladder type of D/A converter shown in Fig. 11.10.



**Fig. 11.10** Inverted or current-mode R-2R ladder D/A converter

The bit position of each of the subsequent MSBs and LSBs are interchanged. Each binary input is connected through the switch to either ground or to the inverting input terminal of op-amp, which is at

virtual ground. Since both the positions of switch  $b_i$  are at ground potential, i.e. the actual or virtual ground, the current flow through any resistor is constant and it is independent of the input binary bit value.

These currents can be represented as

$$I_1 = \frac{V_R}{2R} \quad (11.12)$$

$$I_2 = \frac{(V_R/2)}{2R} = \frac{V_R}{4R} = \frac{I_1}{2} \quad (11.13)$$

$$I_3 = \frac{(V_R/4)}{2R} = \frac{V_R}{8R} = \frac{I_1}{4} \quad (11.14)$$

and

$$I_n = \frac{(V_R/2^{n-1})}{2R} = \frac{I_1}{2^{n-1}} \quad (11.15)$$

The output voltage  $V_o$  is given by

$$\begin{aligned} V_o &= -I_o \times R_f \\ &= -R_f(I_1 + I_2 + I_3 + \dots + I_n) \\ &= -\frac{V_R R_f}{R} (b_1 2^{-1} + b_2 2^{-2} + \dots + b_n 2^{-n}) \end{aligned}$$

When  $R_f = R$ ,

$$V_o = V_R (b_1 2^{-1} + b_2 2^{-2} + \dots + b_n 2^{-n}) \quad (11.16)$$

The circuit operates on the principle of summation of the currents. Hence, it is called  $R - 2R$  current mode type of D/A converter. The current divides equally in successive nodes as indicated in Eqs. (11.12) to (11.15) and the current flow in individual arms of the network remains the same irrespective of the binary bit pattern. Therefore, currents are maintained constant in all the branches and the ladder node voltages also remain constant at  $V_R/2^0, V_R/2^1, V_R/2^2 \dots V_R/2^{n-1}$ . The op-amp is used as a current-to-voltage converter and the total current  $I_o$  is determined by the binary word.

The most important advantage of the current mode or inverted ladder type of D/A converter is that the stray capacitances do not affect the speed of response of the circuit due to the constant ladder node voltages. Hence, the speed performance is improved.

The advantage of this type of D/A converter is their capability of using any two voltage levels for the bit switching, neither of which need necessarily be zero.

### Example 11.6

The inverted  $R - 2R$  ladder shown in Fig. 11.10 has  $R = R_f = 10 \text{ k}\Omega$  and  $V_R = 10 \text{ V}$ . Calculate the total current delivered to the op-amp and the output voltage when the binary input is 1110.

**Solution** Using Eqs. (11.12) through (11.15), we get

$$I_1 = \frac{V_R}{2R} = \frac{10}{2 \times 10 \times 10^3} = 0.5 \text{ mA}$$

$$I_2 = \frac{I_1}{2} = 0.25 \text{ mA} \text{ and } I_3 = \frac{I_1}{4} = 0.125 \text{ mA}$$

Therefore, the current  $I_o$  is given by  $I_o = I_1 + I_2 + I_3 = 0.5 + 0.25$

$$+ 0.125 = 0.875 \text{ mA.}$$

The output voltage  $V_o = -0.875 \times 10^{-3} \times 10 \times 10^3 = -8.75 \text{ V}$

## 11.5 SWITCHES FOR D/A CONVERTERS

There is always a need for switches in circuits and systems involving analog signals. The closing and opening of the switches control the signal flow. These switches are normally operated by digital signals. The typical switching circuits using BJTs and MOSFETs are discussed below.

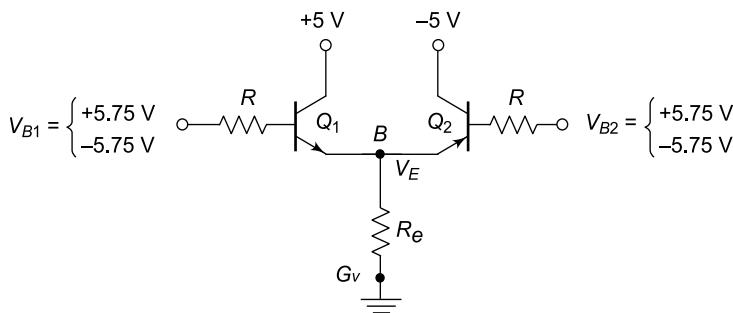
### 11.5.1 Switches using Overdriven Emitter Followers

The diodes and transistors can be used as switches in D/A converters. The characteristics of FETs acting as simple resistors make them ideal switches. The bipolar transistors also have negligible resistance when they are operated in saturation.

The circuit of Fig. 11.11 shows the switching arrangement of a D/A converter using two transistors connected as emitter followers. The bipolar transistors offer negligible resistance when operated in saturation. But it is to be noted that they have an offset voltage of approximately 0.2 V (for silicon transistors) dropped across them. When the transistors are overdriven, the emitter follower circuits can have an offset voltage of 0 V. This is due to the fact that the saturation factor becomes negative. These characteristics can be used for constructing switches in A/D conversion circuits.

The two transistors  $Q_1$  (NPN) and  $Q_2$  (PNP) act as a double-pole switch and  $R$  represents the resistance of the converter.

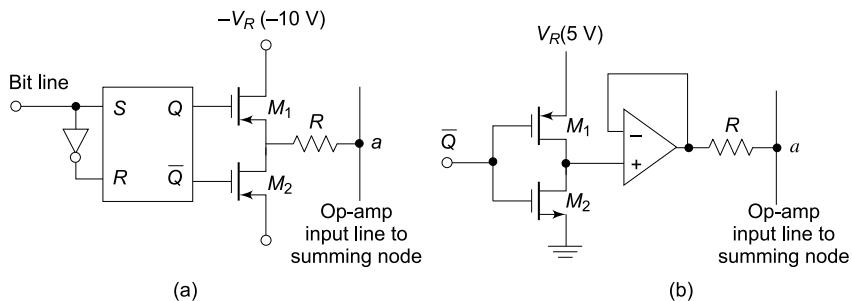
The terminal of the resistor marked  $G_v$  represents the virtual ground connected to the inverting input of op-amp. The bases are driven by voltage levels of  $+5.75 \text{ V}$  and  $-5.75 \text{ V}$ . In (case 1), when  $V_{B1} = V_{B2} = +5.75 \text{ V}$ ,  $Q_1$  is in saturation,  $Q_2$  is OFF and  $V_E \approx 5 \text{ V}$ . The base-emitter voltages of the two transistors are the same as shown in Fig. 11.11 with  $V_{BE1} = V_{BE2} = 0.75 \text{ V}$ . In (case 2), when  $V_{B1} = V_{B2} = -5.75 \text{ V}$ ,  $Q_2$  is ON and  $Q_1$  is OFF. Then, the emitter voltage becomes  $V_E \approx -5 \text{ V}$ . In this manner, the terminal  $B$  of resistor  $R_e$  is connected to either  $-5 \text{ V}$  or  $+5 \text{ V}$  depending on the input bit.



**Fig. 11.11** Switches for D/A converters using overdriven emitter followers

### 11.5.2 Switches using MOS Transistors

**Totem pole MOSFET switch** The totem pole MOSFET switch is shown in Fig. 11.12(a) which is connected in series with the resistors of  $R-2R$  network. Therefore, the ON resistance of the switch must be very low and they should operate with zero offset voltage. The inherent offset voltage of a bipolar transistor, when in saturation, limits its use as a switch. In such cases, the MOSFET is preferred over the bipolar devices.



**Fig. 11.12** Switches for D/A converters using (a) Totem pole MOSFET and (b) CMOS inverter

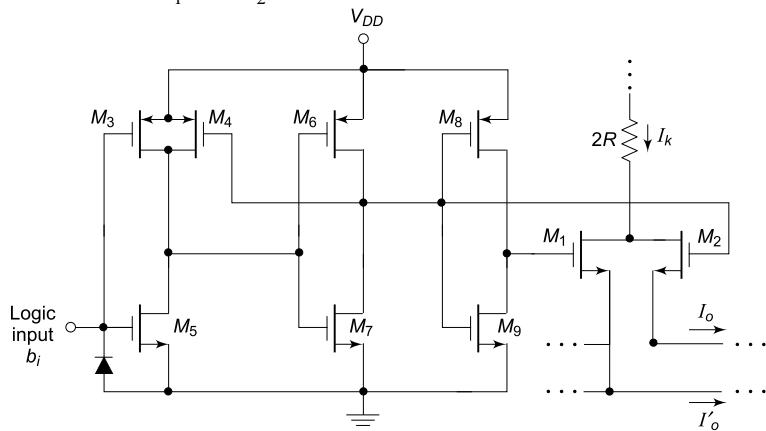
Figure 11.12(a) shows the MOSFET driver connected to the inverting input terminal of the summing op-amps shown in Figs. 11.8, 11.9 and 11.10. The complementary outputs  $Q$  and  $\bar{Q}$  drive the gates of the MOSFETs  $M_1$  and  $M_2$  respectively. The  $S-R$  flip-flop holds one bit of digital information of the binary word under conversion. Assume negative logic for the circuit, where a  $-5\text{ V}$  represents a logic 1 and  $0\text{ V}$  represents a logic 0. When the bit line is 1 with  $S = 1$  and  $R = 0$ , then  $Q = 1$  and  $\bar{Q} = 0$ . This makes the transistor  $M_1$  ON, thereby connecting the resistor  $R$  to the reference voltage  $-V_R$ . The transistor  $M_2$  remains OFF. Similarly, a 0 at the bit line connects the resistor  $R$  to ground through the conducting  $M_2$  transistor.

**Switches using CMOS Inverter** The  $R-2R$  ladder D/A converters are suitable for monolithic fabrication in CMOS technology. The switches for such D/A converters are realised using CMOS transistors and the ladder resistors  $R$  and  $2R$  are fabricated using thin-film deposition over the diffusion regions in the CMOS die.

The arrangement of CMOS inverter used as a switch is shown in Fig. 11.12(b). It consists of a CMOS inverter connected with an op-amp acting as a buffer. The buffer drives the resistor  $R$  with a very low output impedance. Assuming positive logic with  $+5\text{V}$  representing a logic 1 and  $0\text{ V}$  representing logic 0, when the complement of the bit line  $\bar{Q}$  is LOW,  $M_1$  becomes ON connecting  $V_R$  to the non-inverting input of the op-amp. This drives the resistor  $R$  HIGH. When  $\bar{Q}$  is HIGH, transistor  $M_2$  is ON pulling the resistor  $R$  to ground.

### 11.5.3 Switches for Multiplying Type of A/D Converters

Figure 11.13 shows the circuit diagram of a CMOS switch. The heart of the switching element is formed by the transistors  $M_1$  and  $M_2$ .



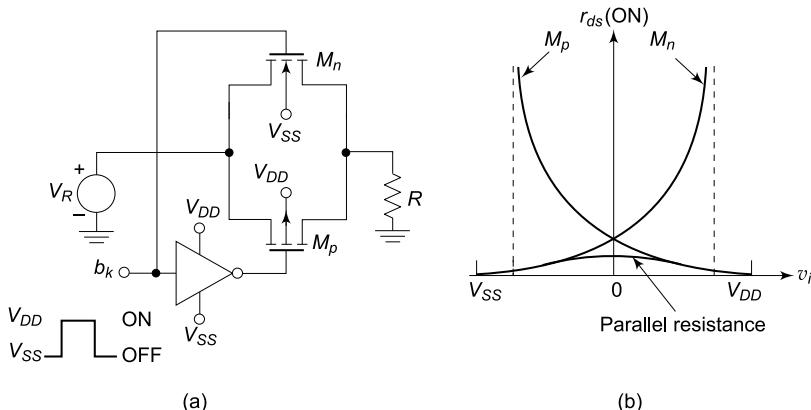
**Fig. 11.13** Switches for D/A converters using CMOS transistors

The remaining transistors accept TTL or CMOS compatible logic inputs, and provide the anti-phase gate drives for the transistors  $M_1$  and  $M_2$ . When the logic input is 1,  $M_1$  is ON and  $M_2$  is OFF. Therefore, the current  $I_k$  is diverted to the  $I_o$  bus. Similarly, when the logic input is 0,  $M_1$  is OFF and  $M_2$  is ON. Therefore, the current  $I_k$  is diverted to the  $I_o$  bus.

#### 11.5.4 Switches using CMOS Transmission Gate

When a single MOS transistor is used as a switch, the NMOS transistor can pass a voltage, which is less than  $V_R$  by one threshold voltage drop and the PMOS transistor can pass a minimum voltage of one threshold voltage. Therefore, switches for D/A converters using transmission gates, formed by parallel connection of the PMOS and NMOS transistors are used as shown in Fig. 11.14(a). This arrangement can pass voltages from  $V_R$  to 0 V acting as an ideal switch. When the bit-line  $b_k$  is HIGH, both the transistors  $M_n$  and  $M_p$  are ON, offering low resistance over the entire range of bit-line voltages. When the bit-line is LOW, both the transistors are OFF and the signal transmission is inhibited. The dynamic resistance characteristics of the transmission gate is shown in Fig. 11.14(b). The nFET ( $M_n$ ) offers low resistance in the lower portion of the signal and pFET ( $M_p$ ) offers lower resistance over the upper portion. As a combination, they offer a low parallel resistance throughout the operating range of voltage.

This form of CMOS switches is available as integrated circuit. The CD4066 and CD4051 from RCA and a wide variety of other MOSFET switches are available.

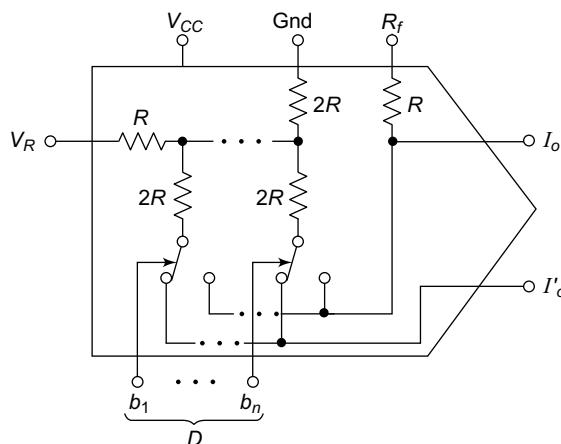


**Fig. 11.14** Switching using CMOS transmission gate (a) Circuit arrangement and (b) Its dynamic resistance

#### 11.6 MULTIPLYING D/A CONVERTERS (MDACs)

An A/D converter which uses a varying analog reference voltage instead of a fixed reference voltage  $V_R$  is called a *multiplier* D/A converter. It is known from Eq. (11.9) that the output is the product of the digital word and the analog reference voltage  $V_R$ . This arrangement can be used as a *programmable attenuator*, when the binary word is made to represent a value less than *unity*. Then the output is a fraction of the input reference voltage  $V_R$ .

The simplified functional diagram of a multiplying D/A converter IC is shown in Fig. 11.15. The input digital word  $D$  is applied to  $b_1 \dots b_n$  terminals. The reference voltage  $V_R$  is applied to circuit, and the switches shown in Fig. 11.14 are employed in this arrangement. The output currents  $I_o$  and  $I'_o$  are functions of the digital word  $D$ . The value of the output is thus programmable from 0V to  $(1-2^{-n}) V_R$ .



**Fig. 11.15** Functional diagram of multiplying D/A converter

The reference voltage of a multiplying D/A converter can be varied over positive and negative values, including zero. This feature makes the multiplying D/A converters most suitable for digitally programmable applications such as programmable filters and oscillators.

## 11.7 A MONOLITHIC D/A CONVERTER DAC 1508/1408

Monolithic D/A converters consisting of  $R-2R$  ladder network with switches and the feedback resistors are available for binary word lengths of 8, 10, 12, 14 and 16. Hybrid D/A converters are available from DATEL Inc. for current and voltage outputs. The MC1508/MC1408 series of 8-bit monolithic D/A converters provide high-speed performance with low cost. They are designed for use when the output current is required to be a linear product of an 8-bit digital word and an analog reference voltage.

The important features of these ICs are their fast settling time of the order of 70ns (typ), a relative accuracy of  $\pm 0.19\%$  (max error), an output voltage swing from +5V to -5V and high multiplying speeds of 4 mA/ $\mu$ s (input slew). The inputs are non-inverting and TTL and CMOS compatible with settling time of 300ns. The ICs operate with standard supply voltages of +5V and -5V to -15 V.

These ICs find applications in tracking A/D converters, Digital Panel Meters (DPM) and Digital Voltmeters (DVM), waveform synthesising circuits, Sample-and-Hold and peak detector circuits, CRT character generation circuits, audio digitising and decoding, programmable power supplies, analog and digital arithmetic operations, speech compression and expansion, stepping motor drive modems and servo motor and pen drivers.

Figures 11.16(a) and (b) shows two different pin configurations of the IC 1408. The internal block diagram of the IC MC1508/MC1408 is shown in Fig. 11.17. It consists of a reference current amplifier, an  $R-2R$  ladder and 8 high-speed current switches. For many applications, only an external reference resistor and the reference voltage need to be added. The switches are non-inverting in operation and hence, a high state on the input turns ON the specified output current component. The switch uses *current steering* for high speed and a termination amplifier consisting of an active load gain stage with unity gain feedback. The termination amplifier holds the parasitic capacitance of the ladder at a constant voltage during switching, and provides a low impedance termination for all legs of the ladder.

The  $R-2R$  ladder network divides the reference amplifier current into binary-weighted components. The maximum output current obtainable for the highest binary input is 255/256 of the reference amplifier current, or 1.992 mA for a 2.0 mA reference amplifier current.

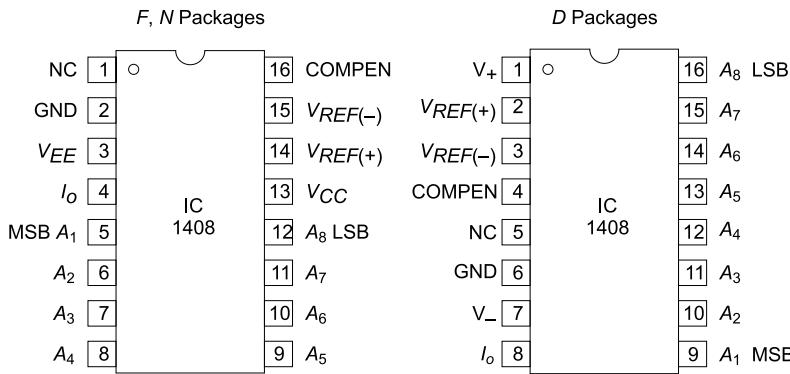
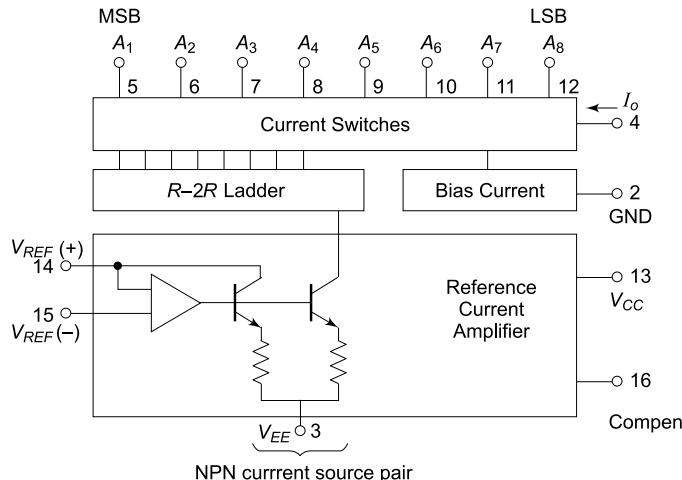
**Fig. 11.16 (a) and (b) Pin configurations of IC 1408****Fig. 11.17 Internal block diagram of IC MC1508/MC1408**

Figure 11.18(a) shows an eight bit D/A converter circuit for unipolar output with 8 input data lines  $b_1$ (MSB) through  $b_8$ (LSB). The reference current of 2 mA for full-scale is provided by two power supplies of values  $V_{CC} = +5V$  and  $V_{EE} = -5V$ . The resistor  $R_{14}$  with the voltage reference  $V_R$  derive a total reference current, as given by

$$I_R = \frac{V_R}{R_{14}} = \frac{5 \text{ V}}{2.5 \text{ k}\Omega} = 2 \text{ mA}$$

The resistors  $R_{14}$  and  $R_{15}$  are selected such that their values match the input impedance of the reference source. The output current is given by

$$I_o = \frac{V_R}{R_{14}} \left( \sum_{i=1}^8 b_i 2^{-i} \right), \quad \text{where } b_1 = 0 \text{ or } 1. \quad (11.17)$$

Then, the output voltage  $V_o$  becomes

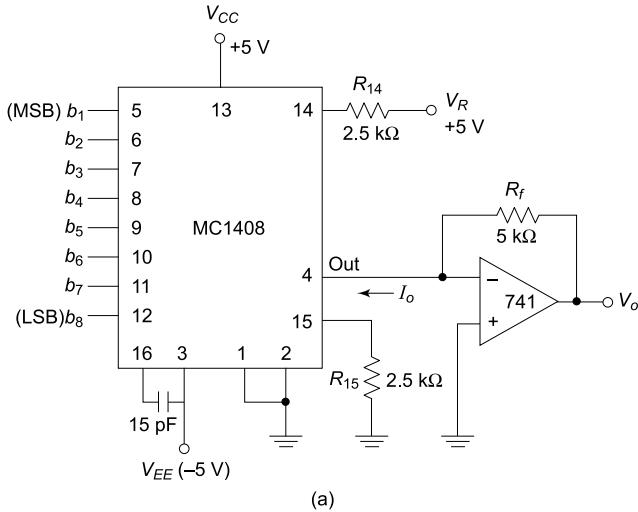
$$V_o = \frac{V_R}{R_{14}} R_f \left[ \frac{b_1}{2} + \frac{b_2}{4} + \frac{b_3}{8} + \dots + \frac{b_8}{256} \right] \quad (11.18)$$

For input  $b_8, \dots b_1 = 11111111$ , the output current  $I_o$  is given by

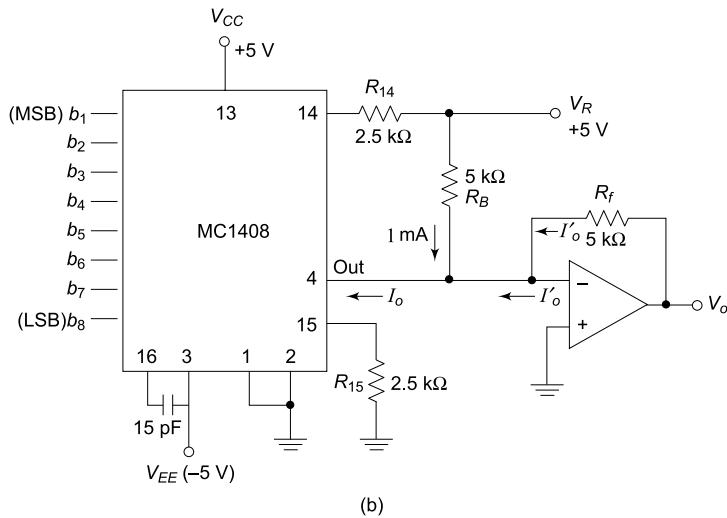
$$I_o = \frac{5 \text{ V}}{2.5 \text{ k}\Omega} \left( \sum_{i=1}^8 b_i \times 2^{-i} \right) = 2 \text{ mA} \times \frac{255}{256} = 1.992 \text{ mA} \quad (11.19)$$

Therefore, the current output is 1 LSB value less than the full-scale reference current of 2 mA. Then, the output voltage  $V_o$  for the full-scale input of 11111111 is

$$V_o = 2 \text{ mA} \times \left( \frac{255}{256} \right) \times 5 \text{ k}\Omega = 9.961 \text{ V}$$



(a)



(b)

**Fig. 11.18** MC1408 D/A converter circuit diagram for (a) Unipolar output and (b) Bipolar output

The IC 1408 can also be calibrated for operating with bipolar output voltage levels from  $-5\text{V}$  to  $+5\text{V}$  as shown in Fig. 11.18(b). This is achieved by connecting resistor  $R_B$  between  $V_R$  and output pin 4.

The resistor  $R_B$  provides a current of  $\frac{V_R}{R_B} = 1 \text{ mA}$  to the output. This is in the direction opposite to that of the current generated by the input signal. Therefore, the output current for bipolar operation becomes

$$I'_o = I_o - (V_R/R_B) = (V_R/R_{14}) \left( \sum_{i=1}^8 b_i \times 2^{-i} \right) - (V_R/R_B)$$

When the binary input word is 00000000, the output is given by

$$V_o = I'_o \times R_f = [I_o - (V_R/R_B)] R_f = (0 - 5 \text{ V}/5 \text{ k}\Omega) \times 5 \text{ k}\Omega = -5 \text{ V}$$

For the binary input word 10000000, the output  $V_o$  becomes

$$\begin{aligned} V_o &= I'_o \times R_f = [I_o - (V_R/R_B)] R_f = [(V_R/R_{14})(d_1/2) - (V_R/R_B)] R_f \\ &= [(5 \text{ V}/2.5 \text{ k}\Omega)(1/2) - (5 \text{ V}/5 \text{ k}\Omega)] \times 5 \text{ k}\Omega = (1 \text{ mA} - 1 \text{ mA}) \times 5 \text{ k}\Omega = 0 \text{ V} \end{aligned}$$

Similarly, for the binary input word of 11111111, the output  $V_o$  is given by

$$\begin{aligned} V_o &= [(V_R/R_{14})(255/256) - (V_R/R_B)] R_f = (1.992 \text{ mA} - 1 \text{ mA}) \times 5 \text{ k}\Omega \\ &= 0.992 \text{ mA} \times 5 \text{ k}\Omega = +4.960 \text{ V} \end{aligned}$$

### Example 11.7

For the circuit of Fig. 11.18(a), calculate the output voltage  $V_o$  for digital input word of

- (i) 00000000
- (ii) 01111111
- (iii) 10000000
- (iv) 11111111

**Solution** The value of current for 1 LSB is  $8 \mu\text{A}$ . Then, the full-scale current  $I_{FS} = 8 \mu\text{A} \times 255 = 2.04 \text{ mA}$ .

- (i) For digital input of 00000000,  $I_o = 8 \mu\text{A} \times 0 = 0$

$$I'_o = 2.040 \text{ mA} - 0 = 2.04 \text{ mA}$$

$$\text{Therefore, } V_o = (0 - 2.04 \text{ mA}) (5 \text{ k}\Omega) = -10.20 \text{ V}$$

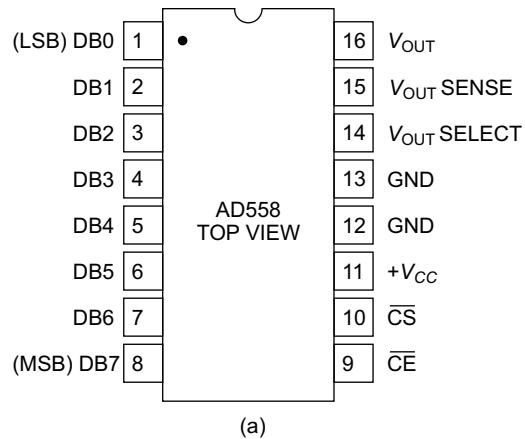
Similarly, the values of  $I_o$ ,  $I'_o$  and  $V_o$  calculated for (ii), (iii) and (iv) are summarised in Table. 11.1.

**Table 11.1** Analog outputs for Example 11.7 (ii) to (iv)

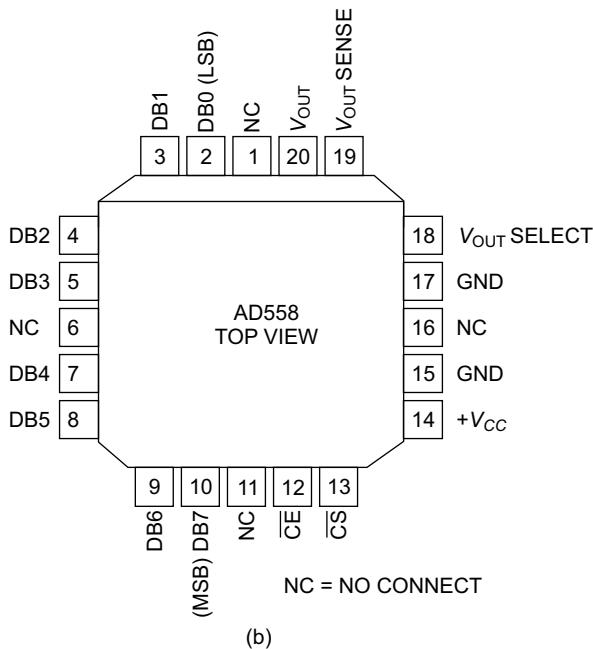
	Digital Inputs								Analog Outputs		
	$b_8$	$b_7$	$b_6$	$b_5$	$b_4$	$b_3$	$b_2$	$b_1$	$I_o$ (mA)	$I'_o$ (mA)	$V_o$ (V)
Negative full-scale	0	0	0	0	0	0	0	0	0	2.040	-10.20
Negative zero	0	1	1	1	1	1	1	1	1.016	1.024	-0.040
Positive zero	1	0	0	0	0	0	0	0	1.024	1.016	0.040
Positive full-scale	1	1	1	1	1	1	1	1	2.040	0	10.20

## **11.8 AD558 MICROPROCESSOR COMPATIBLE D/A CONVERTER**

The AD558 is an 8-bit microprocessor compatible D/A converter. It is available in a laser-trimmed, passivated chip form as shown in Figs. 11.19(a) and (b).



(a)

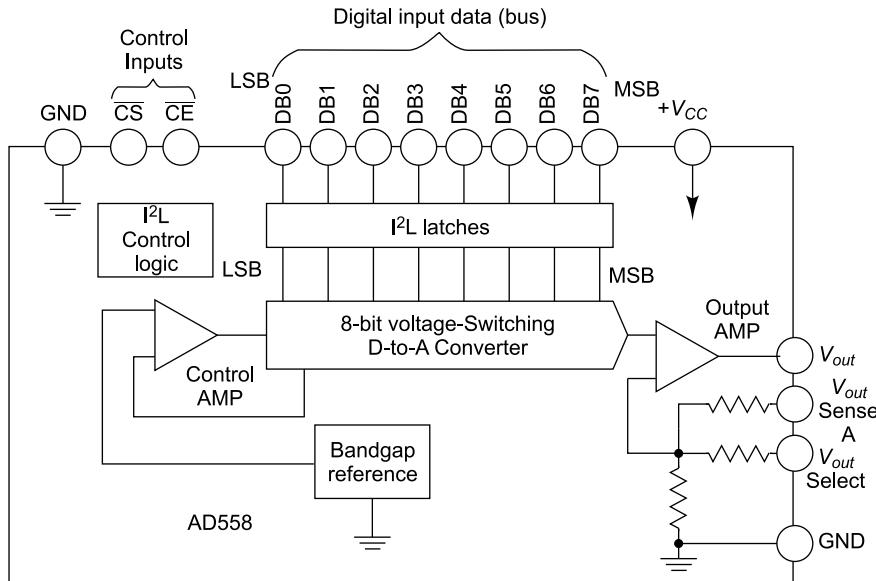


**Fig. 11.19** (a) and (b) AD558 Pin diagrams

An output voltage of maximum range  $V_o = 0$  to 9.961 V is obtained from the circuit. It can operate continuously or it can be controlled by a microprocessor. It contains an on-board precision reference voltage, latches for retaining the digital inputs when made available at the data bus of the microprocessor, and select terminals. The IC contains an op-amp whose output voltage level is pin-programmable for output ranges of either 0 to 1.56 V, or 0 to 10 V.

### 11.8.1 Circuit Description

The AD558 consists of four major functional blocks fabricated on a single monolithic chip as shown in Fig. 11.20. The main D/A converter section uses eight equally weighted current sources, which are switched into a silicon-chromium thin-film  $R/2R$  resistor ladder network. This gives a direct and unbuffered 0 mV to 400 mV output voltage range. PNP transistors form the D/A converter switches. This allows direct positive voltage logic interface and a zero-based output range.



**Fig. 11.20** AD558 functional block diagram

The high speed output buffer amplifier is operated in the non-inverting mode and the gain is determined by user connections at the output range select pin. The gain-setting application resistors are thin-film laser-trimmed resistors. This assures precise initial calibration of the two output ranges, 0V to 2.56 V and 0 V to 10 V. The amplifier output stage is an NPN transistor with passive pull-down for zero-biased output capability with a single power supply. The internal precision voltage reference is of the bandgap type. This design produces a reference voltage of 1.2 V and may be operated from a single, low voltage logic power supply.

The microprocessor interface logic consists of an 8-bit data latch and control circuitry. The control logic allows the latches to be operated from a decoded microprocessor address and write signals. If the application does not involve a microprocessor or data bus, wiring  $\overline{CS}$  and  $\overline{CE}$  to ground renders the latches *transparent* for direct D/A converter access.

### 11.8.2 Functions of Individual Pins

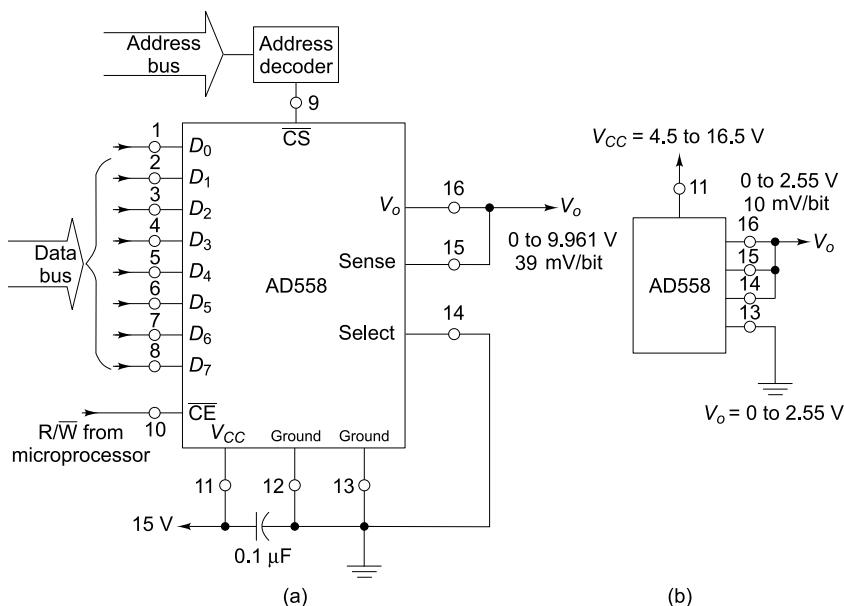
**Power supply** Pin 11 acts as the power supply ( $V_{CC}$ ) terminal and operates with a minimum of +4.5 V and a maximum of +16.5 V. The pins 12 and 13 are digital and analog grounds respectively. This feature allows the user to have individual analog and digital grounds for the system connecting them at only

one point. Commonly, the pins 12 and 13 are joined together. A  $0.1\ \mu\text{F}$  bypass capacitor is connected between  $V_{CC}$  and pin 12 or 13.

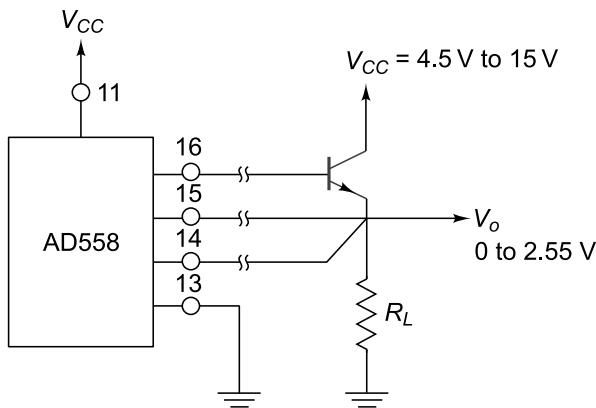
**Digital inputs** The digital input terminals  $D_0$  through  $D_7$  are made available at pins 1 through 8 where  $D_0$  is the LSB and  $D_7$  is the MSB. The inputs are TTL and CMOS compatible. When the AD558 is selected by the microprocessor, the digital input pins connect the data bus of the microprocessor to the internal *memory latching register*. This condition is called *transparent*. When not selected, the latching register is essentially disconnected from the data bus and it retains the previous word written into the latching register. This condition is called *latching*.

**Logic circuitry** During operation, the microprocessor selects the IC with *chip-select* signal ( $\overline{CS}$ ) at control pin 9, and sends a *write* command through the *chip-enable* ( $\overline{CE}$ ) pin 10. If a logic 1 is applied at either ( $\overline{CS}$ ) or ( $\overline{CE}$ ), the digital inputs are in the *latched* mode and they are disconnected from the data bus. If both ( $\overline{CS}$ ) and ( $\overline{CE}$ ) are logic 0, the AD558 inputs are *transparent* and the input memory latch register is connected to the data bus. The microprocessor can now write data into the D/A converter. The D/A conversion is made and the operation is done in approximately 200 ns.

**Analog output** The analog output voltage  $V_o$  is available at pin 16 with respect to the analog ground at pin 13. Pin 14 is called  $V_o$  *gain select*. The output is programmed for 0 to 9.961 V range when connected with ground at pin 13 as shown in Fig. 11.21(a). It is wired to pins 15 and 16 to get an output voltage range of 0 to 2.55 V as shown in Fig. 11.21(b). The *Sense* terminal 15 allows remote load-voltage sensing to nullify the effects of IR drops in long leads to the load resistor. It is also used for current boosting as shown in Fig. 11.21(c). In the current boost transistor circuit, the terminals 14 and 15 are extended to load  $R_L$  to eliminate the  $V_{BE}$  drop.



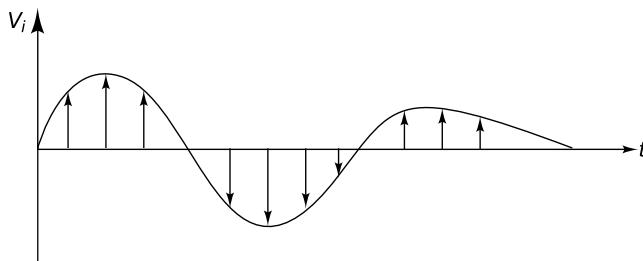
**Fig. 11.21** AD558 connection diagram programmed for (a)  $V_o = 0$  to 9.961 V, and (b)  $V_o = 0$  to 2.55V



**Fig. 11.21 (c) Current boost transistor circuit**

## 11.9 SAMPLING PROCESS

Figure 11.22 shows the graphical representation of sampled input signal over time. The result of the sampling process is a series of the sampling instants and the amplitude of the signal at that instant of time. If the sampling is done at a constant rate, the resulting amplitude values may be used to reconstruct the signal. The accuracy of the conversion process will depend on two factors, namely, how frequently was the sampling done and the accuracy and resolution of the sample measurement.



**Fig. 11.22 Sampling the input signal over time**

**Shannon's sampling theorem** The minimum sampling rate used with any system bears great importance. Only a finite number of samples can be taken at any time, and a loss of information could result in due to inadequate sampling frequency. The Shannon's sampling theorem establishes the theoretical basis for all the discrete sampling operations carried out on analog signals.

Shannon's sampling theorem states that if a signal is sampled for all time at a rate more than twice the highest frequency, it can be exactly reconstructed from the samples. If sampling is done at a rate higher than twice the highest frequency, the aliases do not overlap and the original signal can be recovered. If sampling is done at a slower rate than twice the frequency, then aliases would overlap. Assuming the signal has a spectrum with frequency components extending from dc to a maximum frequency of  $f_i$  Hz, the Shannon's

sampling theorem states that the minimum possible sampling rate above which a bandpass signal can be recovered from the samples is

$$f_s > 2f_i \text{ Hz}$$

For example, an audio signal ranging from dc to 20 kHz could theoretically be reconstructed by taking uniformly spaced samples at a rate of 40,000 samples/second. In practice, the sampling rate is always preferred to be higher than the theoretical minimum value and normally, 3 to 4 times the highest frequency of the signal.

### Example 11.8

A system employs a 16-bit word for representing the input signal. If the maximum output voltage is set to 2 V, calculate the resolution of the system and its dynamic range.

**Solution** A 16-bit word represents  $2^{16}$  or 65,536 levels. These levels are equally spaced across the 2V range. Then, each step is given by

$$\text{Step size} = \frac{2 \text{ V}}{65536} = 30.52 \mu\text{V}$$

Therefore, the system can resolve voltage changes as low as  $30.52 \mu\text{V}$ .

The *dynamic range* of a system represents the *ratio of the largest value obtainable to the smallest value*. Therefore,

$$\text{Dynamic range} = \frac{2 \text{ V}}{30.52 \mu\text{V}} = 65536, \text{ i.e. } 20 \log_{10} 65536 \approx 96 \text{ dB}$$

The dynamic range may also be calculated using the formula:

$$\text{Dynamic range} \approx 6 \text{ dB} \times \text{Number of bits} = 6 \text{ dB} \times 16 \text{ bits} = 96 \text{ dB}.$$

**Aliasing error** When a signal  $f_i$  is sampled at a rate lower than  $2f_i$ , *aliasing error* occurs. The *aliasing error* is a phenomenon in which, the frequencies appear to be different from their true values and the signal cannot be recovered correctly.

It is not always possible to exactly identify the frequency content of random data signals. Therefore, it is a common practice to pass the analog signals through a low-pass filter known as *prefilter* before sampling. The filter characteristics are designed such that it can reject all components equal to or greater than half the sampling rate. Without such a filter in the circuit, spurious input components outside the range of frequency of the signal could be shifted into the signal frequency range through the sampling and aliasing processes.

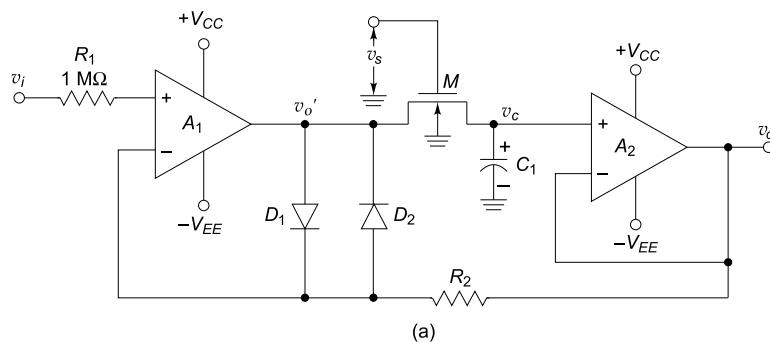
## 11.10 HIGH SPEED SAMPLE-AND-HOLD CIRCUIT

The basic principle of Sample-and-Hold circuit is dealt with in Sec. 5.7. Figure 11.23(a) shows a Sample-and-Hold circuit for high speed of operation. The MOS transistor  $M$  shown is an analog switch capable of switching by logic levels, such as that from TTL. It alternately connects and disconnects the capacitor  $C_1$  to the output of op-amp  $A_1$ . Diodes  $D_1$  and  $D_2$  are inverse-parallel connected. They prevent op-amp  $A_1$  from getting into saturation when the transistor  $M$  is OFF. This makes the operation of the circuit faster. Hence, the output of op-amp  $A_1$  will be  $v'_o(t) \approx v_i(t) - 0.7\text{V}$  when  $v_i(t) < v_o(t)$ , and  $v'_o(t) \approx v_i(t) + 0.7\text{V}$  when  $v_i(t) > v_o(t)$ .

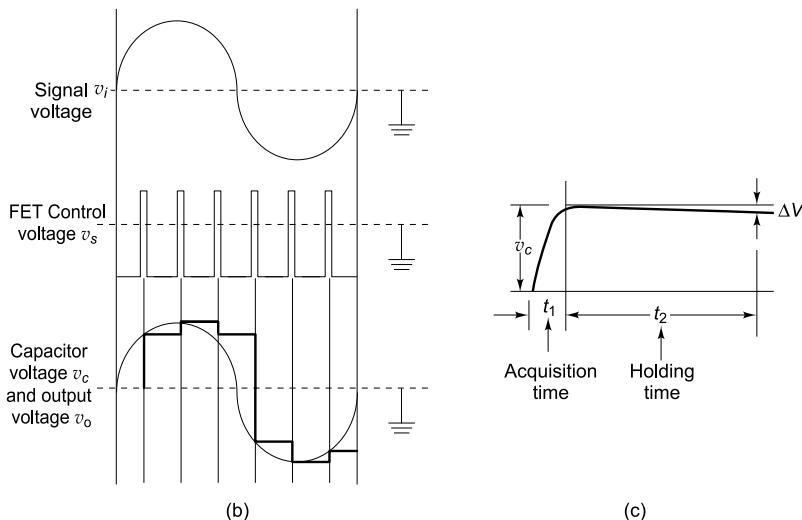
When transistor  $M$  is ON, the op-amps  $A_1$  and  $A_2$  act as voltage followers. The waveforms shown in Fig. 11.23(b) illustrate the operation of the circuit. The transistor  $M$  is alternately switched ON and OFF

by the control voltage  $v_s$  at its gate terminal. Note that the voltage  $v_s$  is to be higher than the threshold voltage of the FET. When the transistor switch  $M$  is ON for a short interval of time, the capacitor  $C_1$  quickly charges or discharges to the value of the analog signal at that instant. In other words, when input  $v_i$  is larger than capacitor voltage  $v_c$  and the transistor  $M$  is OFF, it rapidly charges to the level of  $v_i$  the instant  $M$  switches ON. Similarly, if  $v_c$  is initially greater than  $v_i$ , then  $C_1$  rapidly discharges to the level of  $v_i$  when  $M$  becomes ON.

When  $M$  is OFF, only the input bias current of op-amp  $A_2$  and the gate – source reverse leakage current of FET are effective in discharging the capacitor. Hence, the sampled voltage is held constant by  $C_1$  until the next *sampling instant* or *acquisition time*. Figure 11.23(c) shows the *sampling* or *acquisition time*  $t_1$  and *holding time*  $t_2$ . During the sampling time  $t_1$ ,  $C_1$  is charged through the FET channel resistance  $R_{DS(ON)}$ , and the charging time  $t_1 = 5R_{DS(ON)}C_1$  when the capacitor charges to 0.993 of input voltage. During the hold time  $t_2$ , the capacitor partially discharges. This is called *hold-mode droop*. To avoid



**Fig. 11.23 (a)** Sample-and-Hold circuit



**Fig. 11.23 (b)** Signal voltage, control voltage and output voltage waveforms  
**(c)** Capacitor voltage waveform

this, the op-amp  $A_2$  must have very low input bias current, the capacitor should have a low leakage dielectric and  $M$  must have very low reverse leakage current between its gate and source terminals. The low channel resistance  $R_{DS(ON)}$  is desirable for the FET to achieve faster charging and discharging of  $C_1$ .

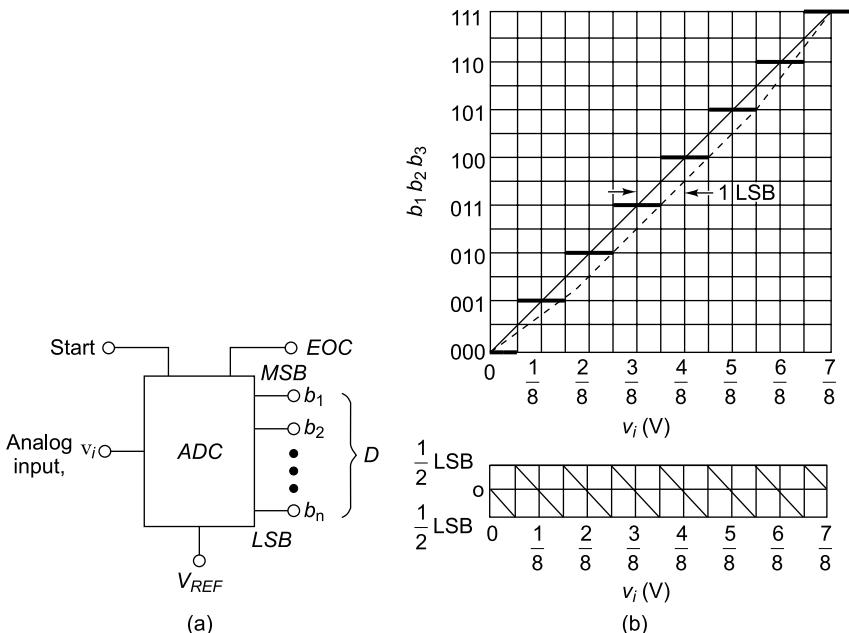
## 11.11 A/D CONVERTERS

An A/D converter does the inverse function of a D/A converter. It converts an analog signal into its equivalent  $n$ -bit binary coded digital output signal. The analog input is sampled at a frequency much higher than the maximum frequency component of the input signal. The digital output from an A/D converter can be in serial or parallel form.

The A/D converter accepts an analog input  $v_i$  and produces an output binary word  $b_1, b_2 \dots b_n$  of fractional value  $D$  such that

$$D = b_1 2^{-1} + b_2 2^{-2} + \dots + b_n 2^{-n} \quad (11.20)$$

where  $b_1$  is the MSB and  $b_n$  is the LSB. The symbolic representation of an  $n$ -bit A/D converter is shown in Fig. 11.24 (a). Two additional control pins START input and End of Conversion (EOC) output are provided with A/D converters. The START input initiates the conversion and the EOC announces when the conversion is complete. The output can be of parallel or serial form. Usually latches, control logic and buffers are provided to enable interfacing of the A/D converter to microprocessors or LCD/LED displays directly.

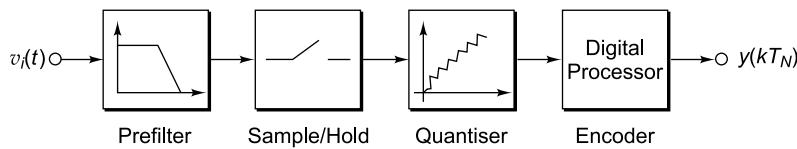


**Fig. 11.24** A/D converter: (a) Symbolic representation (b) Ideal transfer characteristics and quantisation noise for a 3-bit A/D converter

Figure 11.24(b) shows the ideal characteristics of a 3-bit A/D converter with  $V_{FS} = 1.0$  V where  $V_{FS}$  is the full-scale analog voltage. The A/D conversion process divides the analog input into  $2^n$  intervals.

These intervals are called *code ranges* and all the values of  $v_i$  falling within a code range are represented by the particular code. For instance, the code 110 corresponding to  $v_i = \frac{6}{8}$  V represents all inputs of value  $\frac{6}{8} \pm \frac{1}{16}$  V. Hence, the output can err by  $\pm \frac{1}{2}$  LSB.

The general block diagram of an A/D converter is shown in Fig. 11.25. It consists of an antialiasing filter or prefilter, Sample-and-Hold amplifier, a quantiser and an encoder. The prefilter avoids the aliasing of high frequency signals. The Sample-and-Hold circuit holds the input analog signal into the A/D converter at a constant value during the conversion time. The quantiser segments the reference voltage signal into subranges. Typically, for an  $n$ -bit digital output code, there are  $2^n$  subranges. The digital processor forms the encoder circuit which encodes the subrange into the corresponding digital bits. Therefore, the analog input signal is converted into an equivalent digital output code within the *conversion time*.



**Fig. 11.25** General block diagram of an A/D converter

## 11.12 SPECIFICATIONS OF A/D CONVERTER

Some important specifications, namely, accuracy, differential linearity, conversion time, input voltage range and resolution of A/D converters are discussed below.

**Resolution** The *resolution* refers to the finest minimum change in the signal which is accepted for conversion, and it is decided with respect to the *number of bits*.

It can be defined as  $\text{resolution} = 1/2^n$ , where  $n$  is the number of digital output word bits. The ratio of the full-scale input voltage range  $V_{FS}$  to the resolution gives the minimum change of input voltage which can cause a change of 1 LSB at the output. This can be expressed as

$$\Delta v_i \text{ for 1 LSB} = \frac{V_{FS}}{2^n} \quad (11.21)$$

where  $V_{FS}$  is the full-scale input voltage range.

If the number of bits used to represent a signal is larger, then the resolution improves. For example, if an 8-bit word is used, a maximum of 256 distinct values are available. If a maximum analog signal amplitude of 1V is used, then each step in the word represents  $\frac{1V}{256} = 3.9\text{mV}$ . If 16 bits are used for the same 1 V range, then each step would produce  $1\text{V}/65536 = 15.26\text{\mu V}$ .

The digital output starts at 0 for an A/D converter. Therefore, the maximum full-scale input voltage which will cause the output to be all logic 1s is 1 LSB less than the full-scale voltage range.

$$v_{iFS} = V_{FS} - 1 \text{ LSB} \quad (11.22)$$

where  $v_{iFS}$  is the maximum input voltage which can cause all 1's at the output.

## Example 11.9

---

An 8-bit A/D converter accepts an input voltage signal of range 0 to 10 V.

- What is the minimum value of the input voltage required to generate a change of 1 LSB?
- What input voltage will generate all 1s at the A/D converter output?
- What is the digital output for an input voltage of 4.8 V?

### Solution

(a) From Eq. (11.21), 1 LSB =  $\frac{10\text{V}}{2^8} = 39.1\text{ mV}$

(b) From Eq. (11.22),  $v_{iFS} = 10\text{V} - 39.1\text{ mV} = 9.961\text{ V}$ .

(c) The digital output for an applied input voltage of 4.8V is given by

$$D = \frac{4.8\text{V}}{39.1\text{mV}} = 122.76 \approx 123$$

Converting this to binary gives the digital output for an 8-bit A/D converter to be 01111011.

**Quantisation error** A digital error in an A/D converter is based on the resolution of the digital system. In A/D conversion, a continuous analog voltage is represented by an equivalent set of digital numbers. When the digital numbers are converted back to analog voltage by a D/A converter, the output is a staircase waveform, which is a discontinuous signal composed of a number of discrete steps. The smallest digital step is due to the LSB and it can be made smaller only by increasing the number of bits in the digital representation. This error is called *quantisation error*, or *digitizing error* and it is commonly the bit. As shown in Fig. 11.24(b) the digital output is 011 for all values of  $\frac{3}{8}\text{V} \pm \frac{1}{2}\text{ LSB}$ . Therefore there is an uncertainty about the exact value of  $v_i$  when the output is 011. This uncertainty is called the *quantisation error* and its value is  $\pm \frac{1}{2}\text{ LSB}$ .

Increasing the number of bits of A/D converter results in finer resolution and smaller quantisation error.

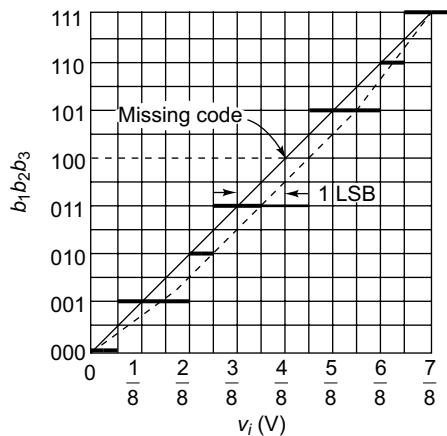
**Analog error** Analog error in an A/D converter is mainly due to variations in the dc switching point of the comparator. The variations in switching are mainly due to offset, gain and linearity error of the operational amplifier used in the comparator. The other sources of analog error are the resistors in the A/D converter, the reference voltage source and the ripple and noise introduced by the circuit components.

**Linearity error** This is an important measure of A/D converter performance. It is defined as a measure of the variation in voltage step size. This indicates the difference between the transitions for a minimum step of input voltage change. This is normally specified as a fraction of 1 LSB.

**Differential Nonlinearity (DNL) error** The analog input levels that trigger any two successive output codes should differ by 1 LSB ( $\text{DNL} = 0$ ) for an A/D converter. Any deviation from 1 LSB value is defined as DNL error.

The counter type and continuous type A/D converters normally have better differential linearity than successive approximation type A/D converters.

**Integral Nonlinearity (INL) error** Figure 11.26 shows an actual A/D converter characteristic with a missing code. The dotted curve represents the locus of the midpoints of the actual input step voltage ranges.



**Fig. 11.26** A/D converter characteristic with a missing code

This line is called the *code centre line*. The maximum deviation of the code centre line from the straight line passing through the end points of the ideal characteristics after nulling the offset and gain errors is called *Integral Nonlinearity error* (INL).

**Dither** The performance of A/D converters can be improved using *dither*. This is a very small amount of random noise (white noise) which is added to the input before A/D conversion. Its amplitude is set to half of the LSB value. Its effect is to cause the state of the LSB to randomly oscillate between 0 and 1 in the presence of very low levels of input, rather than sticking at a fixed value. Instead of the signal simply getting cut-off altogether at this low level (which is only being quantised to a resolution of 1 bit), it extends the effective range of signals that the A/D converter can convert, at the expense of a slight increase in noise. Thus, the quantisation error is diffused across a series of noise values which is far less objectionable than a hard cut-off. The result is an accurate representation of the signal over time. A suitable filter at the output of the system can recover this small signal variation.

**Conversion time** The time required for an A/D converter to convert an analog input value into its equivalent digital data is called the *conversion time*.

**Input voltage range** It is the range of voltage that an A/D converter can accept as its input without causing any overflow in the digital output.

## 11.13 CLASSIFICATION OF A/D CONVERTERS

The A/D converters (ADC) can be classified based on their operational features as follows.

**Type I** The A/D converters can be classified into two groups as

- (a) Programmed A/D converters
- (b) Non-programmed A/D converters

In programmed A/D converters, the conversion is made in a fixed number of steps, with equal time intervals. For example, successive approximation type of A/D converter is a typical example of the programmed type of A/D converter.

The non-programmed A/D converters may require a sequence of steps initially, and the time interval of the sequence of steps depends only on the response time of the conversion circuitry. The integrating type A/D converters fall in this category.

**Type II** The A/D converters are classified into two groups as

- (a) Closed-loop or feedback type A/D converters
- (b) Open-loop type A/D converters

In closed-loop or the feedback type A/D converters, the analog voltage generated internally as a function of digital input is fed back to one input of the comparator. This voltage is compared with the analog voltage under conversion. When the input voltage and the feedback voltages are equal, the conversion is said to be complete. All D/A converter based A/D converters belong to this category.

In open-loop converters, a direct comparison is made between the analog input voltage and a set of reference analog voltages. The result of the comparison forms a digital word at the output. The flash type A/D converters are typical examples of open-loop converters.

**Type III** The A/D converters are classified into two groups as

- (a) Capacitor – charging type A/D converters
- (b) Discrete voltage comparison type A/D converters

The capacitor charge-balancing type of A/D converter operates on the principle of charging the capacitor at a rate proportional to the input voltage, while simultaneously pulling out discrete charge packets out of the capacitor at a rate such that the net charge flow is always zero. The capacitor balancing integrating type of A/D converters belong to this category.

Discrete voltage comparison type employs the principle of generation of discrete voltages whose levels are equivalent to digital words. The comparison for these discrete voltage levels is then made with the analog input voltage to determine the equivalent digital word. A/D converters based on weighted capacitor of D/A converters fall under this category.

**Type IV** The A/D converters are classified into two groups based on their conversion techniques as

- (a) Direct type A/D converters
- (b) Integrating type A/D converters.

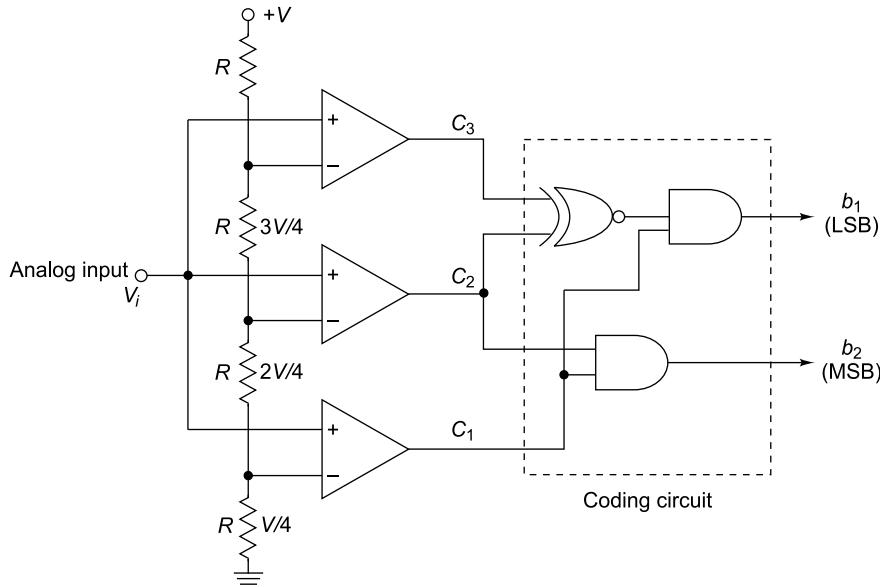
The direct type A/D converters compare a given analog signal with an internally generated equivalent analog signal. Flash (comparator) type A/D converter, Counter type A/D converter, Tracking or Servo operated A/D converter and Successive approximation A/D converter are direct type of A/D converters.

The integrating type of A/D converters performs the A/D conversion in an indirect manner. It is a special class of converter which uses either a reference voltage, or integrates the signal during the conversion process. Therefore, they do not require S/H circuit at the input. The process of integrating the signals also improves the signal-to-noise ratio for certain type of analog signals. The integrating A/D converters are suitable only for very low frequency signals. For example, many of the digital voltmeters employ an integrating A/D converter in the circuit. The charge balancing type and dual slope A/D converters fall in this category.

### **11.13.1 Simultaneous Type (Flash Type) A/D Converter**

The simultaneous type A/D converter is based on comparing an unknown analog input voltage with a set of reference voltages. To convert an analog signal into a digital signal of  $n$  output bits ( $2^n - 1$ ) number of comparators are required. For example, a 2-bit A/D converter requires 3 or ( $2^2 - 1$ ) comparators, while

a 3-bit converter needs 7 or  $(2^3 - 1)$  comparators. The block diagram of a 2-bit simultaneous type A/D converter is shown in Fig. 11.27.



**Fig. 11.27** Block diagram of 2-bit simultaneous type A/D converter

As shown in Fig. 11.27, the three op-amps are used as comparators. The non-inverting inputs of all the three comparators are connected to the analog input voltage. The inverting input terminal of the op-amps are connected to a set of reference voltages  $V/4$ ,  $2V/4$  and  $3V/4$  respectively, which are obtained using a resistive divider network and power supply  $+V$ .

The output of a comparator is in *positive saturation state* when the voltage at the non-inverting input terminal is more than the voltage at the inverting terminal and it is in *negative saturation state* otherwise. When the analog input voltage is less than  $V/4$ , the voltage at the non-inverting terminals of the three comparators is less than their respective inverting input voltages, and hence, the comparator outputs are  $C_1 C_2 C_3 = 000$ . When the analog input is between  $V/4$  and  $V/2$ , the comparator outputs are  $C_1 C_2 C_3 = 100$ . Table 11.2 shows the comparator outputs for different ranges of analog voltage and their corresponding digital outputs.

**Table 11.2** Comparator and digital outputs for a 2-bit simultaneous type A/D converter

Analog input voltage ( $V_i$ )	Comparator Outputs			Digital Outputs	
	$C_1$	$C_2$	$C_3$	$b_2$	$b_1$
$0 \leq V_i \leq V/4$	0	0	0	0	0
$V/4 \leq V_i \leq V/2$	1	0	0	0	1
$V/2 \leq V_i \leq 3V/4$	1	1	0	1	0
$3V/4 \leq V_i \leq V$	1	1	1	1	1

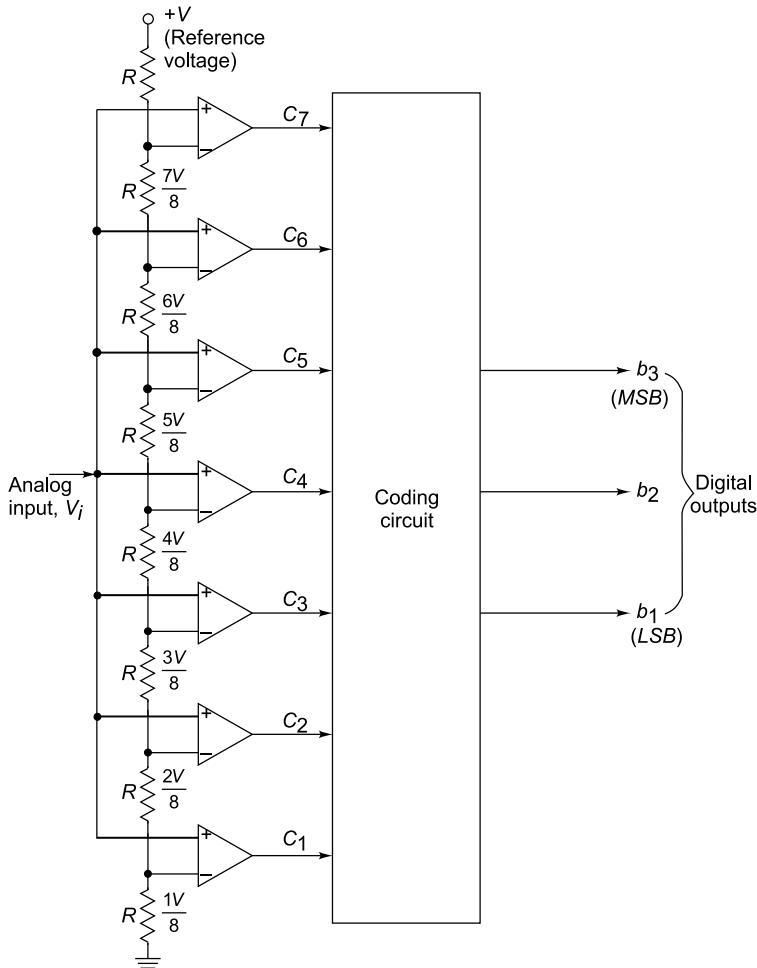
Since there are four ranges of analog input voltages, this can be coded using a 2 bit digital output ( $b_2, b_1$ ) as shown in Table 11.2. The coding circuit for encoding the three comparator outputs into two digital outputs is shown inside the dotted square of Fig. 11.27 using the simplified expressions for  $b_1$  and  $b_2$  as discussed below.

From Table 11.2, logic expressions for  $b_2$  and  $b_1$  can be written as

$$b_2 = C_1 C_2 \overline{C_3} + C_1 C_2 C_3 = C_1 C_2 (\overline{C_3} + C_3) = C_1 C_2 \quad (11.23)$$

$$b_1 = C_1 \overline{C_2} \overline{C_3} + C_1 C_2 C_3 = C_1 (\overline{C_2} \oplus C_3) \quad (11.24)$$

Similarly, a 3-bit A/D converter can be constructed using seven ( $2^3 - 1$ ) comparators as shown in Fig. 11.28. The comparator and digital outputs for eight different ranges of analog input voltage are given in Table 11.3.

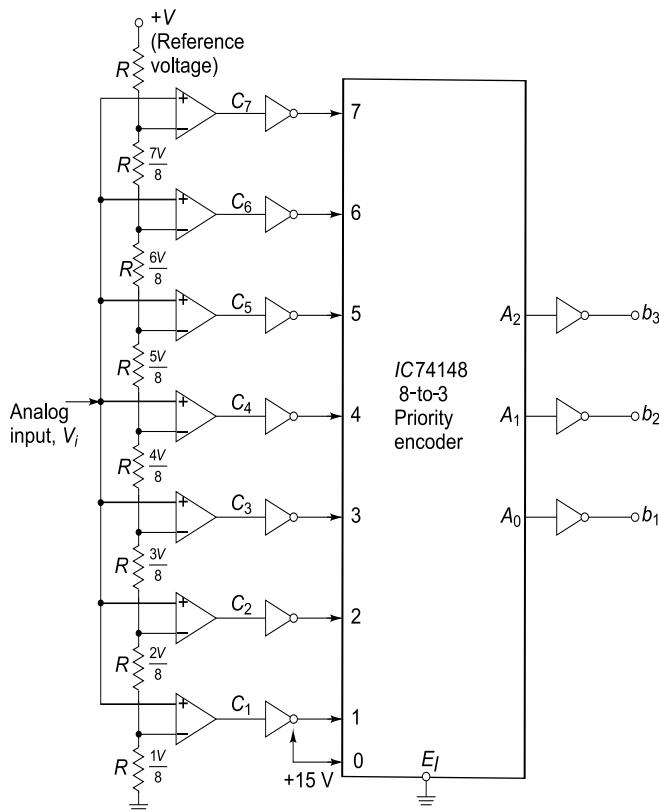


**Fig. 11.28** Block diagram of 3-bit simultaneous type A/D converter

**Table 11.3** Comparator and digital outputs for 3-bit simultaneous type A/D converter

Analog input voltage ( $V$ )	Comparator Outputs							Digital Outputs		
	$C_1$	$C_2$	$C_3$	$C_4$	$C_5$	$C_6$	$C_7$	$b_3$	$b_2$	$b_1$
$0 \leq V_i \leq V/8$	0	0	0	0	0	0	0	0	0	0
$V/8 \leq V_i \leq 2V/8$	1	0	0	0	0	0	0	0	0	1
$V/8 \leq V_i \leq 3V/8$	1	1	0	0	0	0	0	0	1	0
$V/8 \leq V_i \leq 4V/8$	1	1	1	0	0	0	0	0	1	1
$V/8 \leq V_i \leq 5V/8$	1	1	1	1	0	0	0	1	0	0
$V/8 \leq V_i \leq 6V/8$	1	1	1	1	1	0	0	1	0	1
$V/8 \leq V_i \leq 7V/8$	1	1	1	1	1	1	0	1	1	0
$V/8 \leq V_i \leq V$	1	1	1	1	1	1	1	1	1	1

From Table 11.3, it is clear that the logic expressions for ( $b_3$ ,  $b_2$  and  $b_1$ ) are complex due to their dependence on seven input variables ( $C_1$ ,  $C_2$ , ...  $C_7$ ). Hence, the coding circuit is implemented using a priority encoder. The IC 74148 is an 8 to 3 priority encoder with active LOW inputs and outputs. Since the comparator outputs are active HIGH, they are connected to the inputs of encoder through inverters and the outputs of encoder are inverted once again to get active HIGH digital outputs  $b_3$ ,  $b_2$  and  $b_1$  as shown in Fig. 11.29.

**Fig. 11.29** Logic diagram of 3-bit simultaneous type A/D converter

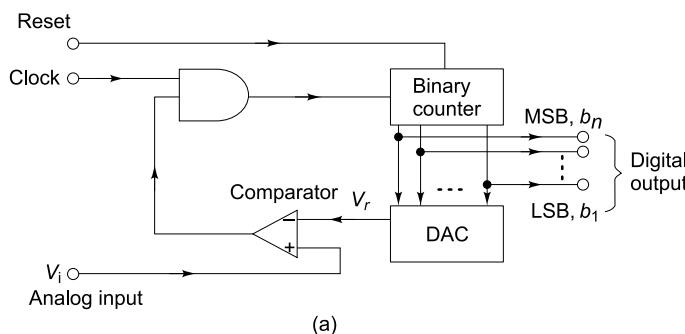
### Advantages

- (i) Simultaneous type A/D converter is the fastest because A/D conversion is performed simultaneously through a set of comparators. Hence, it is also called *flash type* A/D converter. Typical conversion time is 100 ns or less.
- (ii) The construction is simple and easier to design.

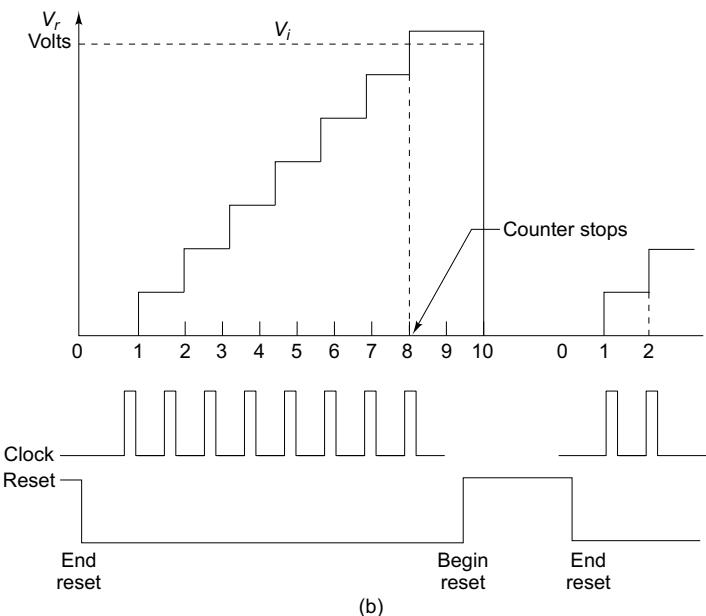
**Disadvantages** The simultaneous type A/D converter is not suitable for A/D conversion with more than 3 or 4 digital output bits. It is because of the fact that  $(2^n - 1)$  comparators are required for an  $n$ -bit A/D converter and the number of comparators required doubles for each added bit.

### 11.13.2 Counter Type A/D Converter

The counter type A/D converter is constructed using only one comparator with a variable reference voltage. The variable reference voltage can be obtained by a sequence counter and a D/A converter. The block diagram for an  $n$ -bit counter type A/D converter is shown in Fig. 11.30(a).



**Fig. 11.30** Counter type A/D converter (a) Block diagram



**Fig. 11.30** Counter type A/D converter (b) Its output staircase waveform

The operation of the counter type A/D converter is as follows. The  $n$ -bit binary counter is initially set to 0 by the *Reset* switch which is normally active LOW. Therefore, the digital output is zero and the analog equivalent  $V_r$  is also 0. When Reset signal is released (HIGH), the clock pulses gated through the AND gate are counted by the binary counter. The D/A converter converts the digital output to an analog voltage and supplies it as the inverting input to the comparator. The output of the comparator enables the AND gate to pass the clock. The number of counted pulses increases with time and the analog input  $V_r$  is a rising staircase waveform as shown in Fig. 11.30(b).

The counting will continue until the reference voltage  $V_r$  equals and just rises more than  $V_i$ . Then the comparator output becomes LOW and this disables the AND gate from passing the clock. The counting stops at the instance  $V_r > V_i$ , and at that instant the digital output of the comparator represents the analog input voltage  $V_i$ . Then the clock is inhibited, the counter stops its progress and the conversion is said to be complete. The numbers stored in the  $n$ -bit counter is the equivalent  $n$ -bit digital data for the given analog input voltage.

In this A/D converter, the counter advances by one count for every clock pulse, and therefore, the clock speed decides the conversion speed. For example, if a 100 kHz clock is used in an 8-bit A/D converter,

the counter advances for every step and it will take  $2.56 \text{ ms}$  (i.e.  $2^8 \times \frac{1}{100 \text{ kHz}} = 2.56 \text{ ms}$ ) to reach the full-scale digital output (i.e.  $2^8 \times 10 \mu\text{s} = 256 \text{ ms}$ ). Normally, the time required to reach one half of the full-scale voltage is called *average conversion* time. Hence, the average conversion time of the above A/D converter is  $1.28 \text{ ms}$ .

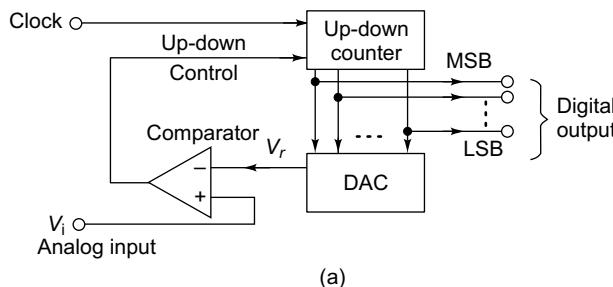
### Advantages

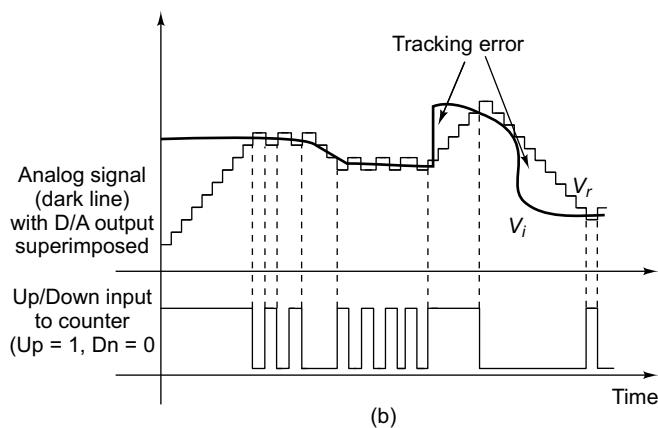
- (i) The counter type A/D converter is very simple and needs less hardware compared to the simultaneous type A/D converter.
- (ii) This is suitable for digitising applications with high resolution.

**Disadvantages** In counter type A/D converter, the conversion time is very long, variable and proportional to the amplitude of the analog input voltage. Since the counter always counts from 0 through a normal sequence, a maximum of  $2^n$  counts are required to convert a full-scale analog input voltage. Hence, for an  $n$ -bit A/D converter, the average conversion time is  $2^n/2 = 2^{n-1}$  times the clock period, which can be very long for large value of  $n$ .

### 11.13.3 Continuous Type (Servo Tracking) A/D Converter

The main drawback of very long conversion time of the counter type A/D converter can be eliminated by counting from the previously counted value, instead of resetting the counter for each conversion. This requires an UP/DOWN counter mechanism and additional control circuitry as shown in the continuous or servo tracking A/D converter of Fig. 11.31(a).





**Fig. 11.31** Continuous or Servo tracking A/D converter: (a) Circuit diagram  
(b) Analog input and digital output waveform

The output of the D/A converter which is the variable reference voltage  $V_r$  is connected to the inverting input of the comparator and the non-inverting input of the comparator is connected to the unknown analog input voltage  $V_i$ . When the analog input voltage  $V_i$  is greater than the variable reference voltage  $V_r$ , the output of the comparator is in HIGH state. The counter is then made to count UP, and the D/A converter output increases. The new  $n$ -bit digital data is converted and compared with the unknown analog voltage. The process of counting-up continues until  $V_r$  is less than  $V_i$ . When  $V_r$  becomes equal and just more than  $V_i$ , the comparator output becomes LOW, and the counter starts counting DOWN. The process continues with the digital output moving UP and DOWN about the correct final digital value. The converted digital data is available in the  $n$ -bit counter.

Figure 11.31(b) shows the waveforms of (i) the analog input signal, (ii) the UP/DOWN input signal to the counter, and (iii) the D/A converter output superimposed on (i) and (ii) to show the response characteristics of the converter.

In practice, the analog input voltage is within 1 LSB of variable reference voltage leading to oscillation between two adjacent digital values. This can be eliminated by adjusting the comparator in such a way that the comparator output (UP/DOWN) line will not reach HIGH unless the analog input voltage is higher than the variable reference voltage by (1/2) LSB.

**Advantage** The continuous type A/D converter is faster than the counter type A/D converter as the conversion starts from the previous counted value instead of resetting the counter every time.

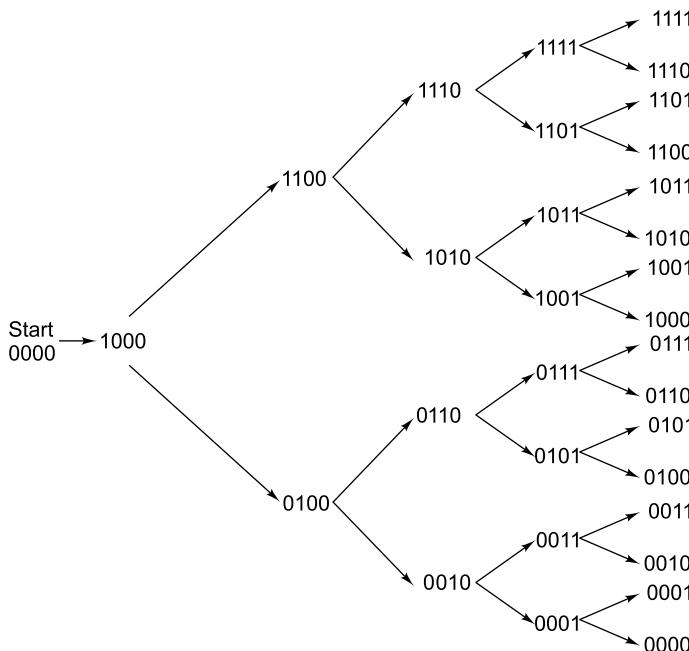
#### Disadvantages

- (i) Additional logic is required to control the circuit for performing UP/DOWN counting operations.
- (ii) Conversion time is variable and it also depends on the last converted value.
- (iii) The tracking continues efficiently as long as the analog input changes slowly. When the analog input changes rapidly, the tracking cannot be achieved in tune with the change in analog input. This is called *the tracking error* and is shown in Fig. 11.31(b).

#### 11.13.4 Successive Approximation Type A/D Converter

The conversion time is maintained constant in successive approximation type A/D converter, and it is proportional to the number of bits in the digital output, unlike the counter and continuous type A/D converters.

The basic principle of this A/D converter is that the unknown analog input voltage is approximated against an  $n$ -bit digital value by trying one bit at a time, beginning with the MSB. The principle of successive approximation process for a 4-bit conversion is shown in Fig. 11.32.



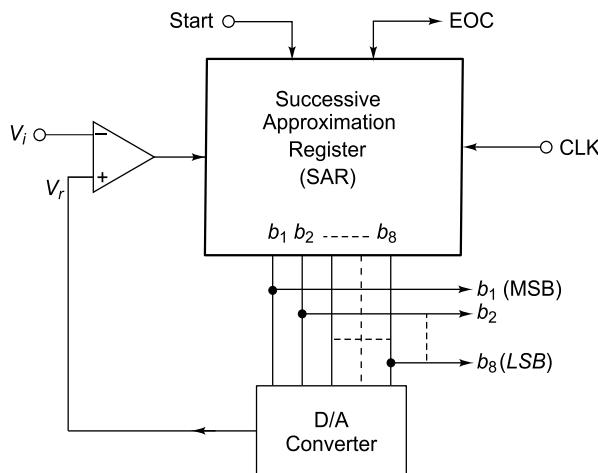
**Fig. 11.32** Successive approximation principle for 4-bit digital output

This type of A/D converter operates by successively dividing the voltage range by half, as explained in the following steps.

- (i) The MSB is initially set to 1 with the remaining three bits set as 0. The digital equivalent is compared with the unknown analog input voltage.
- (ii) If the analog input voltage is higher than the digital equivalent, the MSB is retained as 1 and the second MSB is set to 1. Otherwise, the MSB is reset to 0 and the second MSB is set to 1.
- (iii) Comparison is made as given in step 1 to decide whether to retain or reset the second MSB. The third MSB is set to 1 and the operation is repeated down to LSB and by this time, the converted digital value is available in the SAR.

From Fig. 11.32, it can be seen that the conversion time is constant (i.e., four cycles for 4-bit A/D converter) for various digital outputs. This method uses a very efficient search strategy to complete an  $n$ -bit conversion in just  $n$ -clock periods. Therefore, for an 8-bit successive approximation type A/D converter, the conversion requires only 8 cycles, irrespective of the amplitude of analog input voltage.

The functional block diagram of successive approximation type A/D converter is shown in Fig. 11.33. The circuit employs a *successive approximation register* (SAR) which finds the required value of each successive bit by *trial and error* method. The output of the SAR is fed to an  $n$ -bit D/A converter. The analog output equivalent of the D/A converter is applied to the non-inverting input of the comparator, while the other input of the comparator is connected with an unknown analog input voltage  $V_i$  under conversion. The comparator output is used to activate the successive approximation logic of SAR.



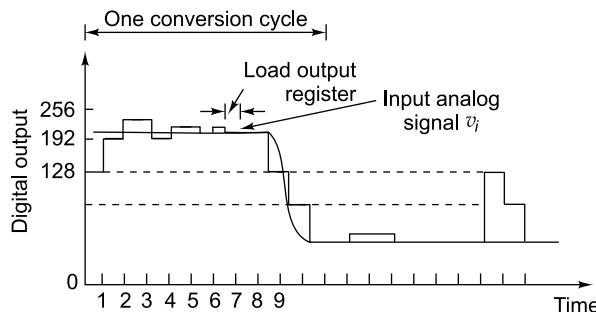
**Fig. 11.33** Functional block diagram of successive approximation type A/D converter

When the START command is applied, the SAR sets the MSB ( $b_1$ ) of the digital signal, while the other bits are made zero, so that the trial code becomes 1 followed by zeros. For example, for an 8-bit A/D converter the trial code is 10000000. The output of the SAR is converted into analog equivalent  $V_r$  and gets compared with the input signal  $V_i$ . If  $V_i$  is greater than the D/A converter output, then the trial code 10000000 is less than the correct digital value. The MSB is retained as 1 and the next significant bit is made 1 and the testing is repeated. If the analog input  $V_i$  is now less than the D/A converter output, then the value 11000000 is greater than the exact digital equivalent. Therefore, the comparator resets the second MSB to 0 and proceeds to the next most significant bit. This process is repeated for all the remaining lower bits in sequence until all the bit positions are tested. The EOC signal is sent out when all the bits are scanned and the value of D/A converter output just crosses  $V_i$ .

Table 11.4 shows the flow of conversion sequence and Fig. 11.34 shows the output response with the associated waveforms. It can be observed that the D/A converter output voltage gets successively closer to the analog input voltage  $V_i$ . For an 8-bit A/D converter, it requires 8 pulses to compute the output irrespective of the value of the analog input.

**Table 11.4** Successive approximation conversion sequence

Correct digital representation	Successive approximation register (SAR) output $V_i$ at different stages in the conversion	Comparator output
11010100	10000000	1 (initial output)
	11000000	1
	11100000	0
	11010000	1
	11011000	0
	11010100	1
	11010110	0
	11010101	0
	11010100	



**Fig. 11.34** Output response for an analog input

### Example 11.10

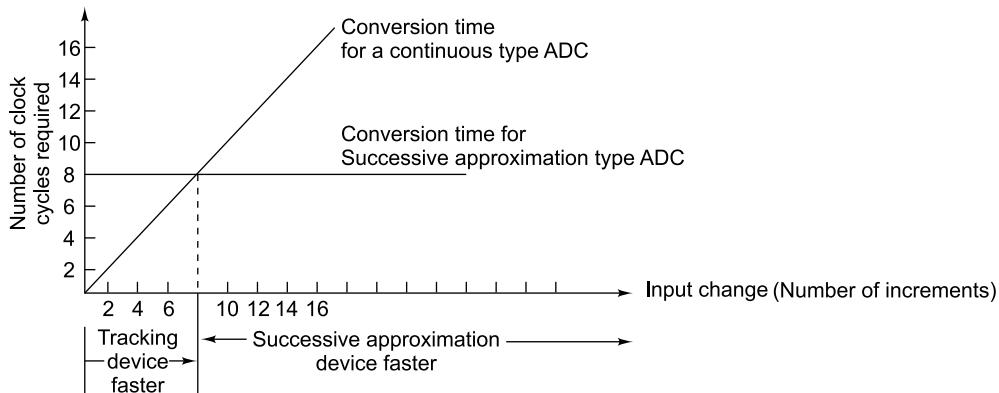
An 8-bit successive approximation A/D converter is driven by a 2 MHz clock signal. Find the conversion time required.

**Solution** The time for one clock pulse =  $\frac{1}{2 \text{ MHz}} = 0.5 \mu\text{s}$ .

The time required to perform the calculation is the sum of (i) the time required for resetting SAR before performing the conversion, and (ii) the time required for performing the conversion. Therefore, the total number of clock pulses required for the conversion is given by

$$(8 + 1 = 9) \text{ clock cycles} = 9 \times 0.5 \mu\text{s} = 4.5 \mu\text{s}$$

A comparison between an 8-bit continuous type A/D converter and an 8-bit successive approximation A/D converter is shown in Fig. 11.35. Generally the successive approximation technique is more versatile and superior. Only  $n$  number of comparisons are needed for an A/D conversion process for an  $n$ -bit digital output.



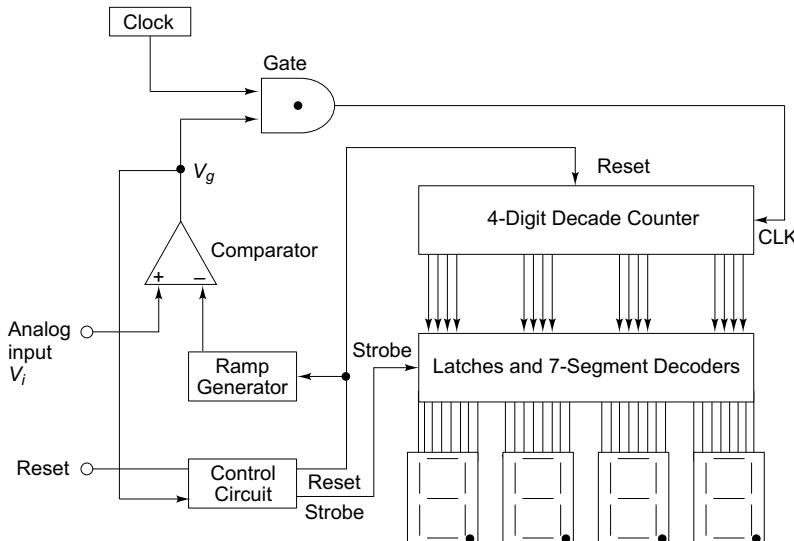
**Fig. 11.35** Speed comparison of successive approximation and tracking A/D converters

Successive approximation ICs are available as monolithic circuits. The AD7582 from Analog Devices Corporation provides a 28-pin DIP CMOS package for 12-bit A/D conversion using successive approximation technique.

### 11.13.5 Single Slope Type A/D Converter

If short conversion time is not important, one can consider single or dual slope type A/D converter. These converter techniques are based on comparing the unknown analog input voltage with a reference voltage that begins at 0V and increases linearly with time. The time required for the reference voltage to reach the value of unknown analog input voltage is proportional to the amplitude of unknown analog input voltage. This time period can be measured using a digital counter.

The block diagram of single slope type A/D converter is shown in Fig. 11.36.



**Fig. 11.36** Block diagram of single slope type A/D converter

The main circuit of this converter is a ramp generator, which, on receiving a RESET from the control circuit increases linearly with time from 0 V to a maximum voltage  $V_m$ . For example, if  $V_m = 10$  V and it takes 1 ms to move from 0 V to 10 V, then the slope is 10 V/ms. Such a ramp generator can be either an op-amp based integrator circuit or a D/A converter driven by a sequence binary counter, whose output waveform is a staircase increasing linearly.

The operation of this converter is explained as follows. Assume that a positive analog input voltage  $V_i$  is applied at the non-inverting input of the comparator. Now, when a RESET signal is applied to the control logic, the 4-digit decade counter resets to 0 and the ramp voltage begins to increase. Since  $V_i$  is positive, the comparator output is in HIGH state. This allows the CLK pulse to pass to the input of the 4-digit counter through the AND gate and the counter is incremented. This process continues until the analog input voltage is greater than the ramp generator voltage. When the ramp generator voltage is equal to the analog input voltage, the comparator output becomes negatively saturated or logic 0 and the clock is prevented from passing through the gate, ceasing the counter operation. Then, the control circuit generates a STROBE signal, which latches the counter value in the 4-digit latch, which is displayed on 7-segment displays. The displayed value is then equivalent to the amplitude of analog input voltage.

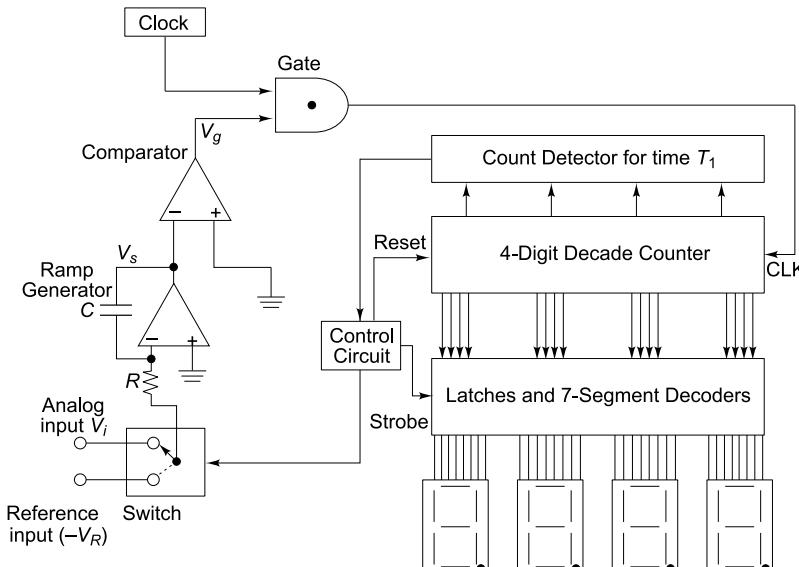
For example, if CLK value is 1 MHz and the slope of the ramp generator is 1V/ms, the 4-digit decade counter reaches its full-scale value, i.e. 9999 in 9999  $\mu$ s (i.e., 9.999ms). It means when the time is 9.999 ms, the ramp generator voltage reaches 9.999 V. So, this single slope type A/D converter can display any analog input value from 0 V to 9.999 V. If  $V_i = 5.62$  V, the counter requires 5620 clock pulses to advance from 0000 to 5620, the ramp voltage rising to 5.62 V. Therefore, at the end of conversion, the

display will be 5620. Now, by activating the decimal point of most significant seven segment display, it will directly read as 5.620 V.

The single slope converter has a disadvantage due to the component value errors and the clock errors. The integrated output voltage is a function of the product of R and C. Therefore, changes in the value of capacitance and resistance due to temperature affect the integrated output and introduce errors. The drift in clock frequency also causes errors.

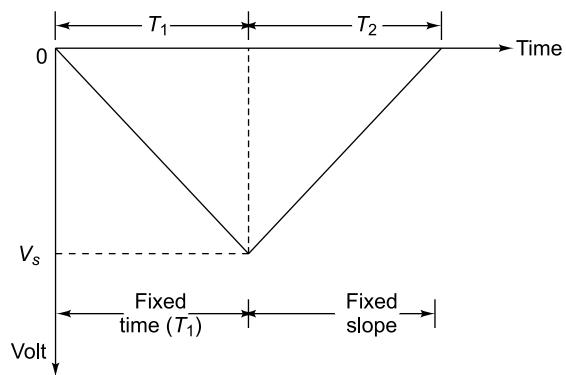
### 11.13.6 Dual Slope Type A/D Converter

In dual slope type A/D converter, the integrator generates two different ramps, one with the unknown analog input voltage  $V_i$  as the input, and another with a known reference voltage ( $-V_R$ ) as the input. Hence, it is called *dual slope* type A/D converter. Its logic diagram is shown in Fig. 11.37(a) and the dual ramp output waveform in Fig. 11.37(b).



**Fig. 11.37 (a)** Logic diagram of dual slope type A/D converter

The operation of dual slope type A/D converter is explained as follows. Assume that the 4-digit decade counter is initially reset to 0000, the ramp output  $V_s$  is reset to 0V, analog input voltage is positive, and the input to the ramp generator or integrator is switched to the unknown analog input voltage. Since the positive analog input voltage is connected to the inverting input of the integrator, the integrator output  $V_s$  is a negative ramp while the comparator output  $V_g$  is positive, and the CLK is passed through the AND gate. This results in counting-up of the 4-digit decade counter.



**Fig. 11.37(b)** Dual ramp output waveform

The negative ramp will proceed for a fixed time period  $T_1$ , which is determined by a count detector for the time period  $T_1$ . At the end of fixed time period  $T_1$ , the ramp voltage is given by

$$-V_s = \frac{V_i}{RC} \times T_1 \quad (11.25)$$

where  $RC$  is the time constant of the ramp generator circuit.

When the counter reaches the fixed count at time period  $T_1$ , the count detector gives a signal to the control circuit which in turn resets the counter to 0 and switches the integrator input to a negative reference voltage ( $-V_R$ ). Now, the ramp generator begins at  $-V_s$  and increases upward until it reaches 0 V. During this time, the counter gets advanced. When  $V_s$  reaches 0 V, the comparator output will become 0 and the CLK is inhibited from passing through the AND gate. Now, the conversion cycle is said to be completed and the positive ramp voltage is given by

$$V_s = -\left( \frac{-V_R}{RC} \times T_2 \right) \quad (11.26)$$

where  $V_R$  and  $RC$  are constants and the time period  $T_2$  is variable.

Since the ramp generator voltage starts at 0 V, decreasing down to  $-V_s$  and then increasing up to 0 V, the amplitude of negative and positive ramp voltages can be equated as follows:

$$-\frac{V_i}{RC} \times T_1 = \frac{V_R}{RC} \times T_2 \quad (11.27)$$

$$-V_i = V_R \times \frac{T_2}{T_1} \quad (11.28)$$

From the above equation, it is clear that the unknown analog input voltage is proportional to the time period  $T_2$ , because  $V_R$  is a known reference voltage and  $T_1$  is the predetermined time period. Also, the contents of the 4-digit decade counter at the end of conversion reflect the variable time period  $T_2$ .

For example, consider the frequency of CLK is 1 MHz, the reference voltage is  $-1.0$  V, the fixed time period  $T_1$  is 1 ms and the  $RC$  time constant is set at  $RC = 1$  ms. Assuming the unknown analog input voltage amplitude as  $V_i = 5$  V, during the fixed time period  $T_1$  the integrator output  $V_s$  will go down to

$$V_s = \frac{-V_i}{RC} \times T_1 = \frac{-5}{1} \times 1 \text{ ms} = -5 \text{ V}$$

Then, during the time period  $T_2$ ,  $V_s$  will integrate all the way back to 0 V.

That is,

$$T_2 = \frac{V_s}{V_R} \times RC = \frac{5}{1} \times 1 \text{ ms} = 5 \text{ ms} = 5000 \mu\text{s}$$

Hence, the 4-digit counter value is 5000, and by activating the decimal point of MSD seven segment displays, the display can directly read as 5V.

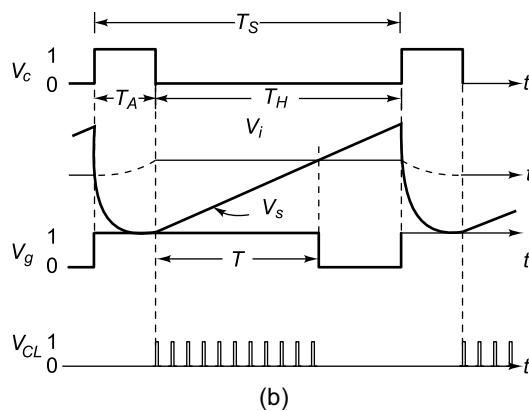
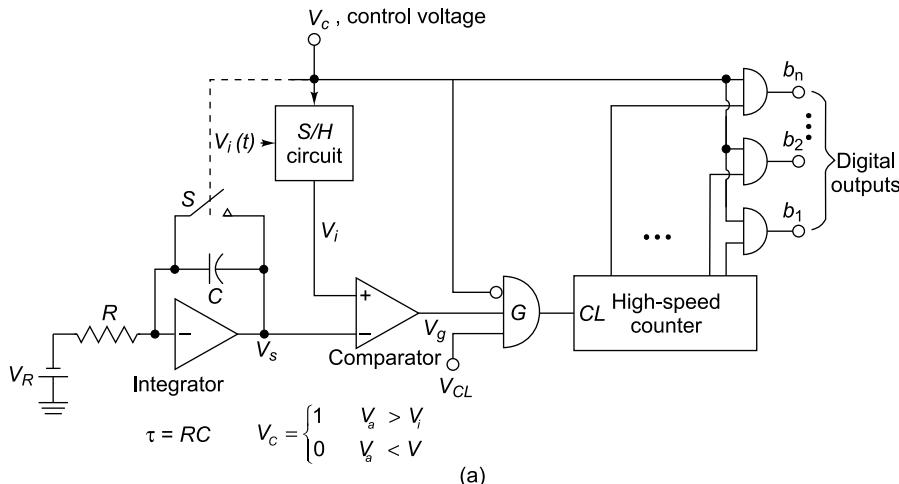
### 11.13.7 Analog-to-Digital Converter using Voltage-to-Time Conversion

An analog signal can be converted into digital signal by counting the pulses from a variable frequency source whose frequency is dependent on the analog input signal value. The counting is done for a fixed period of time. Alternatively, the pulses from a fixed frequency source can be counted for a variable period of time, and the time period is then dependent on the analog signal under conversion.

Figure 11.38(a) shows such an A/D converter. It employs an integrator, a Sample-and-Hold (S/H) circuit, a voltage comparator and a high-speed counter. A negative reference voltage  $V_R$  is applied to the integrator,

which integrates the voltage  $V_R$  and provides a positive polarity output. The analog signal input under conversion  $V_i(t)$  is sampled at a rate fixed by the control voltage  $V_c$ , and the sampled signal at any instant  $V_i$  is applied as input to the non-inverting terminal of comparator. The integrator output  $V_s$  is connected to the inverting input of comparator.

When the integrated voltage  $V_s$  is less than the analog voltage sample  $V_i$  as shown in Fig. 11.38 (b), the comparator output is at *positive* saturation, or at logic 1. A fixed frequency clock  $V_{CL}$  is applied to the high-speed counter through the AND gate G. The AND gate is enabled for the duration from  $t = 0$  when  $V_i = 0$  to the time  $t = T$  when  $V_s = V_i$ .



**Fig. 11.38** A/D converter using voltage-to-time converter: (a) Functional block diagram (b) Input and output waveforms

We know that  $V_s = \frac{V_R t}{\tau}$  where the time constant is given by  $\tau = RC$  for the integrator.

Therefore, at time  $t = T$  when  $V_s = V_i$ , we can infer

$$T = \frac{\tau V_i}{V_R} \quad (11.29)$$

Assuming  $F_C$  is the clock frequency, the count output  $N$  obtained during the time interval 0 to  $T$  is given by

$$N = F_c T = \frac{\tau F_C V_i}{V_R} \quad (11.30)$$

Hence, the count value  $N$  is proportional to  $V_i$ .

Figure 11.38(b) shows the waveforms of the sampling control voltage  $V_c$ , output of comparator  $V_g$  and the clock output CL. The operation of the circuit can be analysed as follows.

The Sample-and-Hold circuit samples the positive input voltage  $V_i(t)$  for every  $T_A$ . Then the sampled voltage  $V_i$  is held for a time duration indicated by  $T_H$  in Fig. 11.38(b). During the period  $T_H$ , the switch  $S$  is held *open*, and the integrator operates with its output following a ramp voltage waveform  $V_s$ . When  $V_s < V_i$ , the comparator output  $V_g$  is at logic 1, and the gate  $G$  is enabled, with  $V_c$  in 0 state. This continues for a time interval  $T$  and during this time, the clock pulses are passed by the gate  $G$  to the high-speed counter. Thus the digital output of the counter is directly proportional to  $T$ . During the time interval  $T_A$ , the gate is disabled, and the digital output is read from the counter. The switch  $S$  is closed during  $T_A$ , and the capacitor discharges, resetting  $V_s$  to 0 V thus starting a new conversion.

## 11.14 ADC080X SERIES A/D CONVERTERS

### 11.14.1 General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters. They basically use a differential potentiometric ladder arrangement. These converters are designed for operation with processors such as 8080 with their TRI-STATE output latches directly driving the data bus. These A/D converters appear like memory locations or I/O ports to the microprocessor and hence no interfacing logic is needed. Differential analog voltage inputs enhance the common-mode rejection ratio (CMRR) property. The voltage reference input can also be adjusted to allow encoding smaller analog voltage ranges to 8-bits of resolution.

The important features of these ICs are

- (i) they are compatible with 8080 processor and its derivatives
- (ii) no interfacing logic is needed
- (iii) its access time is very low of the order of 135 ns
- (iv) an easy interface to all microprocessors and it can operate in *stand-alone* mode
- (v) it can handle differential analog voltage inputs
- (vi) it has an on-chip clock generator
- (vii) its 0 V to 5 V analog input voltage range with single 5 V supply and
- (viii) no zero adjustment is required

### 11.14.2 Functional Description

The ADC0801 contains the circuit equivalent of the  $256R$  network. Analog switches are sequenced by successive approximation logic to match the analog difference input voltage  $V_{IN}(+) - V_{IN}(-)$  to a corresponding tap on the  $R$  network. The most significant bit (MSB) is tested first and after 8 comparisons (64 clock cycles), an 8-bit binary code (11111111 = full-scale) is transferred to an output latch. This is indicated by an interrupt line, which is asserted with a HIGH to LOW transition.

The pin configuration and functional diagram of the A/D converter ADC0801 are shown in Figs. 11.39 and 11.40 respectively. The conversion process of the converter is started by having  $\overline{CS}$  and  $\overline{WR}$  simultaneously low. This sets the *start* flip-flop (FF). The resulting 1 level resets the 8-bit shift register, resets the Interrupt (INTR) FF and inputs a 1 to the D flip-flop FF1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this 1 to the  $Q$  output of FF1. The AND gate G1 logically ANDs this 1 output with a clock signal and provides a *Reset* signal to the start FF. If the *set* signal is no longer present (either  $\overline{WR}$  or  $\overline{CS}$  is a logic 1), then the start FF is *reset* and the 8-bit shift register can have the 1 clocked in, which starts the conversion process. If the set signal were to be still present, this reset pulse would have no effect (both outputs of the start FF would momentarily be at a 1 level) and the 8-bit shift register would continue to be held in

$\overline{CS}$	1	20	$V_{CC}(\text{OR } V_{REF})$
$\overline{RD}$	2	19	CLK R
$\overline{WR}$	3	18	DB0 (LSB)
CLK IN	4	17	DB1
$\overline{INTR}$	5	16	ADC 0801
$V_{IN(+)}$	6	15	DB2
$V_{IN(-)}$	7	14	DB3
A GND	8	13	DB4
$V_{REF}/2$	9	12	DB5
D GND	10	11	DB6
			DB7(MSB)

Fig. 11.39 ADC0801 pin configuration

#### The ADC0801

##### Dual-in line and small outline (SO) Packages

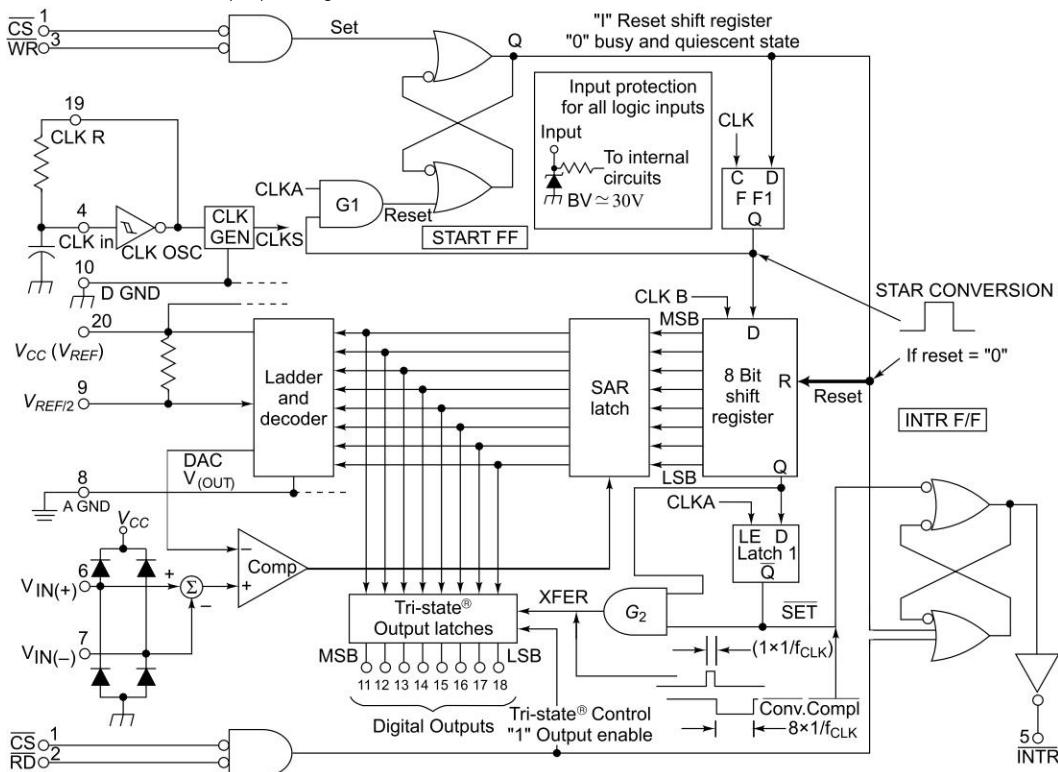


Fig. 11.40 ADC0801 functional diagram

the Reset mode. Therefore, this logic allows for wide  $\overline{CS}$  and  $\overline{WR}$  signals and the converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start FF. After the 1 is clocked through the 8-bit shift register (which completes the SAR search), it appears as the input to the D-type latch LATCH 1. As soon as this 1 is output from the shift register, the AND gate G2 causes the new digital word to transfer to the TRI-STATE output latches. When LATCH 1 is subsequently enabled, the  $Q$  output makes a *high-to-low* transition which causes the INTR FF to set. An inverting buffer then supplies the  $\overline{INTR}$  input signal. This SET control of the INTR FF remains low for 8 of the external clock periods (as the internal clocks run at 1/8 of the frequency of the external clock). If the data output is continuously enabled ( $\overline{CS}$  and  $\overline{RD}$  both held low), the  $\overline{INTR}$  output will still signal the end of conversion (by a *high-to-low* transition), because the SET input can control the  $Q$  output of the INTR FF even though the RESET input is constantly at a 1 level in this operating mode. This  $\overline{INTR}$  output will therefore stay low for the duration of the SET signal, which is 8 periods of the external clock frequency.

When operating in the *free-running* or continuous conversion mode (INTR pin tied to  $\overline{WR}$  and  $\overline{CS}$  wired low), the START FF is set by the *high-to-low* transition of the  $\overline{INTR}$  signal. This resets the SHIFT REGISTER which causes the input to the D-type latch LATCH 1 to go low. As the latch enable input is still present, the Q output will go HIGH, which then allows the INTR FF to be reset. This reduces the width of the resulting  $\overline{INTR}$  output pulse to only a few propagation delays (approximately 300 ns). When data is to be read, the combination of both  $\overline{CS}$  and  $\overline{RD}$  being low will cause the INTR FF to be reset and the TRI-STATE output latches will be enabled to provide the 8-bit digital outputs.

### 11.14.3 Digital Control Inputs

The digital control inputs ( $\overline{CS}$ ,  $\overline{RD}$  and  $\overline{WR}$ ) meet standard TTL logic voltage levels. For non-microprocessor based applications, the  $\overline{CS}$  input (pin 1) can be grounded and the standard A/D *Start* function is obtained by an active low pulse applied at the  $\overline{WR}$  input (pin 3) and the *Output Enable* function is caused by an active low pulse at the  $\overline{RD}$  input (pin 2).

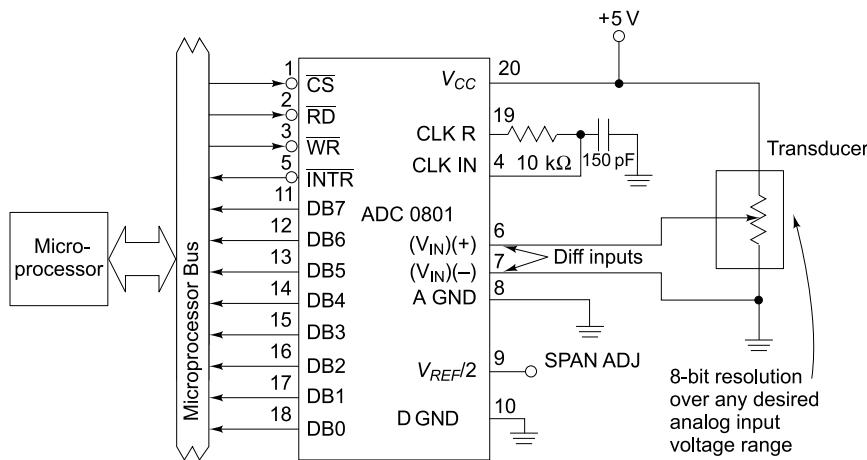
### 11.14.4 Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D converter has the additional flexibility of operation by analog differential voltage input. The  $V_{IN}(-)$  input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading. This is also useful in 4 mA–20 mA current loop conversion. In addition, common-mode noise can be reduced by the use of differential input. The time interval between sampling  $V_{IN}(+)$  and  $V_{IN}(-)$  is 4.5 clock periods.

### 11.14.5 Microprocessor Interfacing

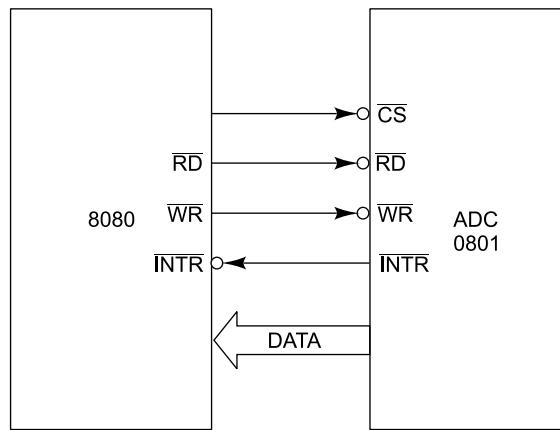
Figure 11.41 shows a general interface connection for a typical application circuit using a microprocessor. The A/D converter can be mapped into memory space (using standard memory address decoding for  $\overline{CS}$  and memory  $\overline{RD}$  and memory  $\overline{WR}$  strobes) or it can be controlled as an *I/O* device by using the I/O R and I/O W strobes and decoding the address bits  $A_0$  to  $A_7$  (or address bits  $A_8$  to  $A_{15}$  as they will contain the same 8-bit address information) to obtain the  $\overline{CS}$  input. Using the *I/O* space provides 256 additional

addresses and may allow a simpler 8-bit address decoder but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D converter should be mapped into memory space.



**Fig. 11.41** Typical application circuit

Figure 11.42 shows the A/D converter interfaced to the microprocessor 8080 through the control signals  $\overline{CS}$ ,  $\overline{RD}$ ,  $\overline{WR}$  and  $\overline{INTR}$  control lines and data bus.



**Fig. 11.42** Microprocessor 8080 interface connection diagram

## 11.15 OVER-SAMPLING A/D CONVERTERS

Analog circuitry forms the most important part of a data converter. The resolution and speed of the data conversion are limited by the component mismatches and nonlinearity of the components, drift, ageing, noise, dynamic limitations and parasitics. Hence, over-sampling converters employing more complex

digital circuitries are used. They sample the analog signal at a rate much higher (typically 64 times) than the sampling rates normally required with Nyquist converters.

### 11.15.1 Delta Modulation (DM)

Delta modulation (DM) developed in the 1940s is a differential pulse-code modulation (DPCM) technique, in which the derivative of the signal is quantised. When signal variations between the subsequent sample periods are very small, the word length of the quantisers can be reduced. With very high over-sampling rates, the changes between sample periods are made very small, and the quantiser can be reduced to low-bit. A 1-bit DPCM coder is known as a delta modulator (DM). In other words, DM codes the differences in the signal amplitude instead of the signal amplitude itself.

The delta modulation A/D converter has the following processes:

- (i) The analog signal is approximated with a series of segments.
- (ii) Each segment of the approximated signal is compared with the original analog wave to determine the increase or decrease in relative amplitude.
- (iii) The decision process for establishing the state of successive bits is determined by this comparison.
- (iv) Only the state related to change of information is sent, and a no-change condition causes the modulated signal to remain at the same 0 or 1 state of the previous sample.

Examples of delta modulation technique are:

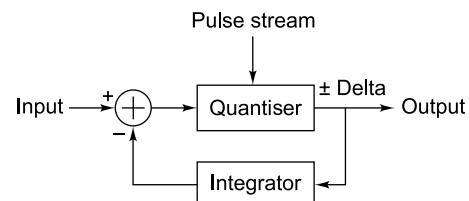
- (i) Continuously variable slope delta modulation,
- (ii) Sigma-delta modulation, and
- (iii) Differential modulation.

Delta modulation (DM) may be viewed as a simplified form of DPCM in which a two level (1-bit) quantiser is used in conjunction with a fixed first-order predictor.

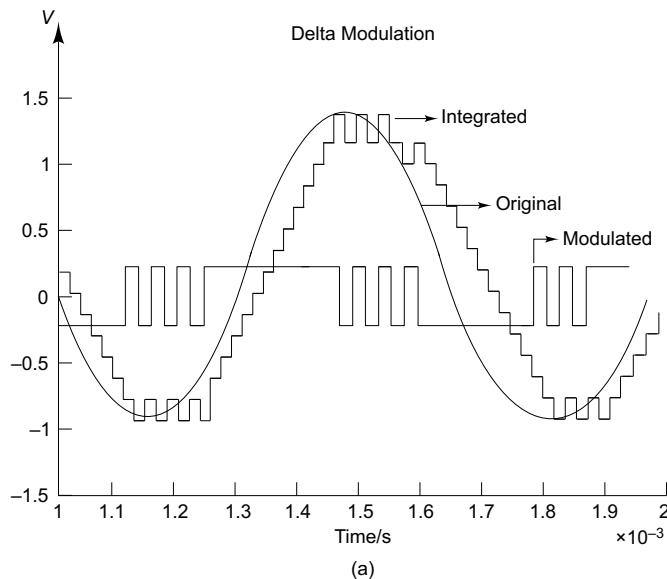
A delta-modulation encoder is shown in Fig. 11.43. It is known as a single integration modulator. The input signal is compared with the integrated output pulses and the delta (difference) signal is applied to the quantiser. The quantiser generates a positive pulse when the difference signal is *negative*, and it generates a negative pulse when the difference signal is *positive*. This difference signal moves the integrator step-by-step closer to the present value of input, tracking the derivative of the input signal.

For example, consider a 1.5 kHz sinusoidal input signal with maximum amplitude of 1V and delta is chosen to be 0.125 which is equivalent to quantisation using 4-bits with 16 quantisation levels. To achieve a resolution equivalent to the 4-bit quantisation at a sampling rate of 4 kHz requires an over-

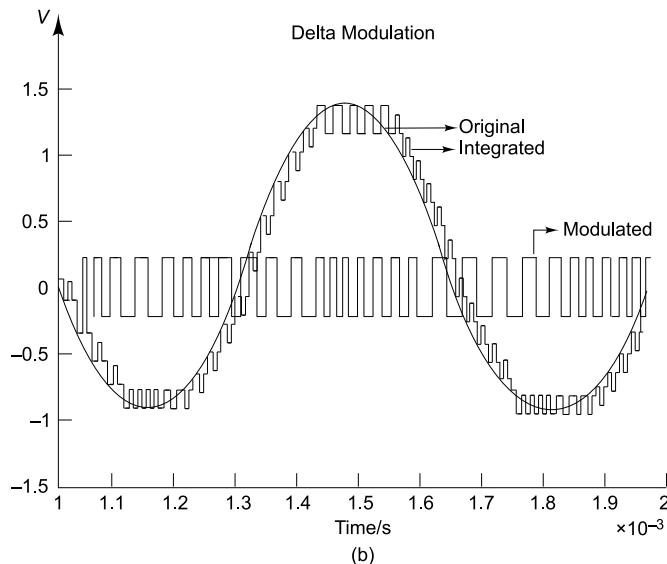
sampling ratio of 16, i.e.  $\frac{4^2}{1^2} \times 4 \text{ kHz} = 64 \text{ kHz}$ . Figures 11.44(a) and (b) show integrator output depicting the comparative tracking efficiency of 16 times over-sampled and 32 times over-sampled signals respectively. The delta modulation decoder integrates the modulated signal and filters the output of the integrator with the use of a low-pass filter.



**Fig. 11.43** Delta modulation encoder



(a)

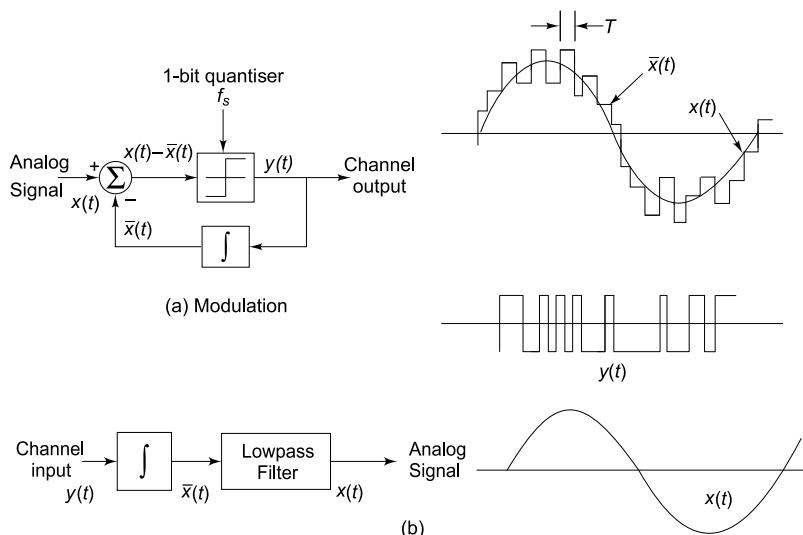


(b)

**Fig. 11.44** DM signal: (a) 16 times over-sampled, and (b) 32 times over-sampled

Figures 11.45(a) and (b) show the block diagrams of the delta modulation/demodulation structure for the A/D conversion process. The delta modulation is based on quantising the change in the signal from sample-to-sample rather than the absolute value of the signal at each sample. Since the output of the integrator in the feedback loop of Fig. 11.45(a) tries to predict the input  $X(t)$ , the integrator works as a predictor. The prediction error term  $X(t) - \bar{X}(t)$  in the current prediction is quantised and it is used to make the next prediction. The quantised prediction error which is the delta modulation output is integrated in the receiver just as it is in the

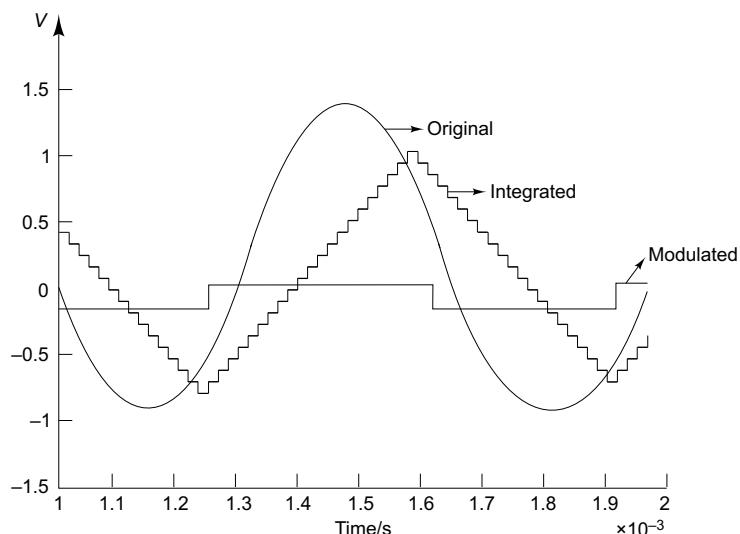
feedback loop. That is, the receiver predicts the input signals as shown in Fig. 11.45(a). The predicted signal is smoothed with a low pass filter.



**Fig. 11.45** (a) Delta modulation (b) Demodulation

The delta modulators exhibit slope overload for rapidly raising input signals, and their performance is thus dependent on the frequency of the input signal. In theory, the spectrum of quantisation noise of the prediction error is flat and the noise level is set by the 1-bit comparator.

**Slope overload distortion** The slope overload distortion is introduced due to the use of a step size delta that is too small to follow some portions of the waveform with a steep slope. It can be reduced by increasing the step size. The typical output waveforms with slope distortion are shown in Fig. 11.46.



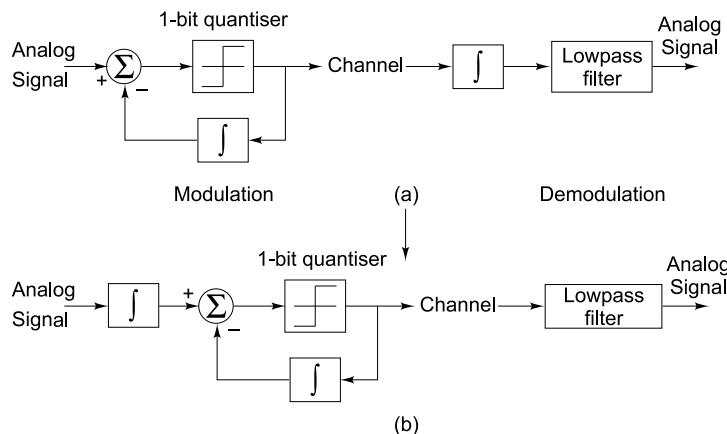
**Fig. 11.46** Slope overload

**Granular noise** The granular noise results from using a step size that is too large in parts of the waveform having a small slope. The granular noise can be reduced by decreasing the step size.

An alternative solution is to employ a variable step size that adapts itself to the short-term characteristics of the source signal. Here, the step size is increased when the waveform has a steep slope and decreased when the waveform has a relatively small slope. This strategy is called Adaptive DM (ADM). The sigma-delta modulation is an extension of the delta modulation.

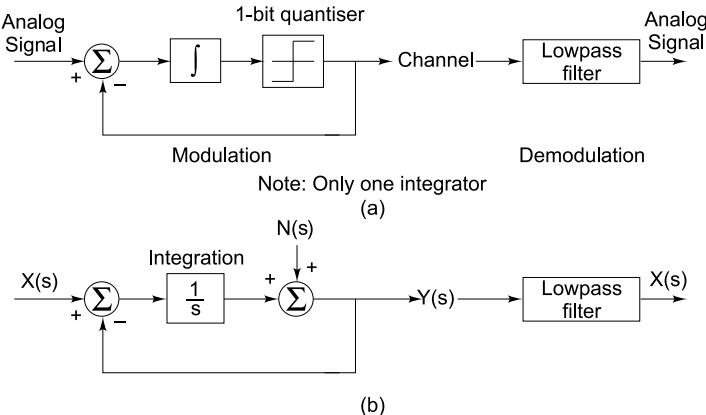
### 11.15.2 Sigma-Delta ( $\Sigma - \Delta$ ) Modulator

Delta modulation requires two integrators for modulation and demodulation processes as shown in Fig. 11.47(a). Since integration is a linear operation, the second integrator can be moved before the modulator without altering the overall input/output characteristics. Furthermore, the two integrators in Fig. 11.47(a) can be combined into a single integrator by the linear operation property as shown in Fig. 11.47(b).



**Fig. 11.47** Sigma-Delta modulation from Delta Modulation: (a) Modulator and Demodulator  
(b) Its equivalent

The arrangement shown in Fig. 11.48(a) is called a Sigma-Delta ( $\Sigma - \Delta$ ) Modulator and its S-domain equivalent is shown in Fig. 11.48(b). This structure can be considered as being a *smoothed version* of a 1-bit delta modulator.

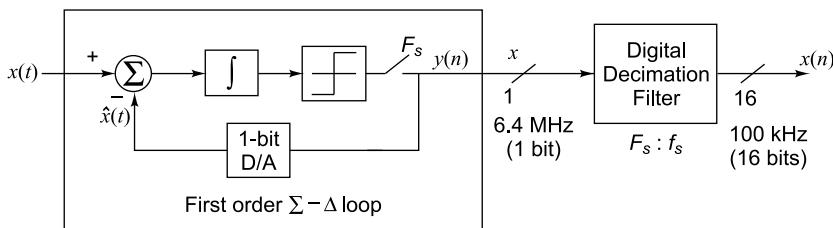


**Fig. 11.48** Sigma-Delta modulation: (a) Block diagram (b) s-domain equivalent

The name Sigma-Delta modulator comes from the principle of placing the integrator (sigma) before the delta modulator. Sometimes, the  $(\Sigma - \Delta)$  modulator is referred to as an *interpolative coder*. The quantisation noise characteristic or the noise performance of such a coder is frequency dependent in contrast to the delta modulation. This noise-shaping property is important in signal processing applications such as digital audio and communication. Like delta modulators, the  $(\Sigma - \Delta)$  modulators use a simple and coarse quantiser (comparator). However, unlike delta modulators, these systems encode the integral of the signal itself and thus their performance is insensitive to the rate of change of the signal.

Figure 11.49 shows the block diagram of a first-order over-sampled  $(\Sigma - \Delta)$  A/D converter. The 1-bit digital output from the modulator is supplied to a digital decimation filter which yields a more accurate representation of the input signal at the output sampling rate of  $F_s$ . It consists of an analog difference node, an integrator, a 1-bit quantiser (A/D converter) and a 1-bit D/A converter in a feedback path. The modulator output has only 1-bit (two levels) of information, i.e. 1 or  $-1$ . The modulator output  $y(n)$  is converted to  $\hat{x}(t)$  by a 1-bit D/A converter.

The input to the integrator in the modulator is the difference between the input signal  $x(t)$  and the quantised output value  $y(n)$  converted back to the predicted analog signal  $\hat{x}(t)$ . Provided that the D/A converter is perfect, and neglecting signal delays, this difference between the input signal  $x(t)$  and the feedback signal  $\hat{x}(t)$  at the integrator input is equal to the quantisation error. This error is summed up in the integrator and then quantised by the 1-bit D/A converter. Although the quantisation error at every sampling instance is large due to the coarse nature of the two level quantiser, the action of the  $(\Sigma - \Delta)$  modulator loop is to generate a  $\pm 1$  output which can be averaged over several input sample periods to produce a very precise result. The averaging is performed by the decimation filter which follows the modulator as shown in Fig. 11.49.



**Fig. 11.49** Block diagram of a first-order Sigma-Delta A/D converter

The sigma-delta A/D converters are used in high-resolution and moderate speed applications such as digital audio, digital telephony and low-frequency instrumentation designs. The resolution obtainable with typical A/D converters is from 16 to 24 bits. It is to be noted that an amount of latency is introduced in the digital filter/decimator stage, while computing and passing the information from input to output through various stages of its filter.

Thus, the sigma-delta converters suffer from limitations in real time applications and multiplexed applications aimed for cost reduction.

## SUMMARY

- Data converters convert one form of data into another form.
- Sampling is the process of acquiring the values of a signal at discrete points of time.

- ❑ Analog signal is the signal defined over a continuous period of time, and the amplitude of which may assume a continuous range of values.
- ❑ Quantisation is the process of representing a variable by a finite set of discrete values.
- ❑ Discrete time signal is the one that is defined at particular point of time.
- ❑ Digital signal is a function, in which the time and amplitude are quantised.
- ❑ D/A Converter (DAC) converts digital data into its equivalent analog data.
- ❑ A/D converter (ADC) converts analog data into its equivalent digital data.
- ❑ The important specifications of D/A converter are accuracy, offset voltage, monotonicity, resolution and settling time.
  - Absolute accuracy is the maximum deviation of the output from the ideal value expressed in fractions of 1 LSB
  - Offset voltage or offset error is the small output voltage that is nullified by translating the actual A/D converter characteristics up or down so that it goes through the origin
  - Full-scale error is the maximum deviation of the output value from its ideal value expressed in percentage of full-scale
  - Linearity error is the maximum deviation in step size from the ideal step size. Expensive D/A converters have full-scale and linearity errors as low as 0.001% of full-scale while general purpose D/A converters have in the range of 0.01 to 0.1%
  - Linearity of a D/A converter is defined as the precision with which the digital input is converted into analog output and the linearity error measures the deviation of the output from the fitted straight line passing through the measured output points
  - DNL (Differential Nonlinearity Error) error is the difference between the ideal and the measured output responses for successive D/A converter codes
  - INL (Integral Nonlinearity Error) is the deviation of an actual transfer function from a straight line
  - Monotonicity of a D/A converter refers to the capability of its output value increasing uniformly as the binary inputs are incremented from one value to the next
  - Resolution of D/A converter is defined as the smallest change that can occur in the analog output as a result of a change in the digital input and % resolution =  $\frac{\text{step size}}{\text{full scale}} \times 100$  and % resolution =  $\frac{1}{(2^n - 1)} \times 100$  for an  $n$ -bit digital input
  - The time needed for a D/A converter output to settle down to within  $\pm(1/2)$  LSB of the final value for a given digital input is the settling time
  - Types of D/A converters are (i) weighted resistor type (ii)  $R$ - $2R$  ladder type (iii) voltage mode  $R$ - $2R$  ladder type and (iv) inverted or current mode  $R$ - $2R$  ladder type.
  - For a voltage output D/A converter, the output is

$$V_o = KV_{FS} (b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \dots + b_n 2^{-n}).$$

- ❑ For a weighted resistor D/A converter, the output voltage is given by  $V_o = I_o R_f = \frac{V_R}{R} [b_1 2^{-1} + b_2 2^{-2} + \dots + b_n 2^{-n}]$ . When  $V_R$  is made variable, the D/A converter becomes a multiplying D/A converter (MDAC).
- ❑ The main disadvantage of binary weighted D/A converter is the need of wide range of resistor values as given by  $2^0 R + 2^1 R + \dots + 2^7 R$  for an 8-bit converter.
- ❑  $R$ - $2R$  ladder D/A converter uses resistors of only two values, i.e.  $R$  and  $2R$ .
- ❑ The output voltage for an  $n$ -bit  $R$ - $2R$  ladder D/A converter is

$$V_o = \frac{V_R}{2^1} + \frac{V_R}{2^2} + \frac{V_R}{2^3} + \dots + \frac{V_R}{2^n} \text{ or } V_o = \frac{V_R}{2^n} (b_1 2^{n-1} + b_2 2^{n-2} + \dots + b_n 2^0).$$

- Advantages of  $R$ - $2R$  type D/A converters are possibility of accurate selection of resistors  $R$  and  $2R$ , and the binary word length can be increased by adding required number of  $R$ - $2R$  sections.
- The advantages of the inverted  $R$ - $2R$  ladder type of D/A converter are
  - They eliminate the varying power dissipation values of weighted resistor and  $R$ - $2R$  ladder types of D/A converters by changing current through the resistors as the input data changes
  - The stray capacitances do not affect the speed of response of the circuit due to the constant ladder node voltages and hence speed performance is improved
- The output voltage  $V_o$  of the inverted  $R$ - $2R$  ladder type of D/A converter is given by
 
$$V_o = -V_R(b_1 2^{-1} + b_2 2^{-2} + \dots + b_n 2^{-n}).$$
- BJT and MOS transistors can be used as switches in D/A converters and they act as efficient switches due to their negligible resistance when they are operated in saturation.
- Transmission gate, formed by parallel connection of the PMOS and NMOS transistors is used as efficient switch and it overcomes the limitation of NMOS types which pass a voltage, that is less than  $V_R$  by one threshold voltage drop, or the limitation of PMOS types, which pass a minimum voltage of one threshold voltage.
- CD4066 and CD4051 from RCA are IC MOSFET switches.
- Monolithic D/A converters consisting of  $R$ - $2R$  ladder network with switches and the feedback resistors are available for 8, 10, 12, 14 and 16 bit binary word lengths. MC1508/MC1408 series of 8-bit monolithic D/A converters provide high-speed performance at low cost.
- Hybrid D/A converters from DATEL Inc. are available for current and voltage outputs.
- The IC MC1508/MC1408 uses  $R$ - $2R$  ladder type D/A conversion method.
- Laser-trimmed and passivated IC AD558 is an 8-bit microprocessor compatible D/A converter with an output voltage of maximum range  $V_o = 0$  to 9.961V and the output voltage level is pin-programmable for either 0 to 1.56V or 0 to 9.961V.
- Shannon's sampling theorem states that if a signal is sampled for all time at a rate more than twice the highest frequency, it can be exactly reconstructed from the samples.
- The A/D converter accepts an analog input 0 to  $v_i$  and produces an output binary word  $b_1, b_2 \dots b_n$  of fractional value  $D$  such that  $D = b_1 2^{-1} + b_2 2^{-2} + \dots + b_n 2^{-n}$ .
- The digital output from an A/D converter can be in serial or parallel form.
- Some definitions related to A/D conversion process are:
  - The conversion time is the time needed for converting the analog input signal into an equivalent digital output code
  - The resolution is the finest minimum change in the signal which is accepted for conversion, and is given by  $\text{resolution} = 1/2^n$ , where  $n$  is the number of bits of digital output word
  - The *quantisation error* is  $\pm \frac{1}{2}$  LSB and increasing the number of bits of an A/D converter results in finer resolution and smaller quantisation error
  - Analog error in an A/D converter is due to offset, gain and linearity error of the operational amplifier used in the comparator, resistors, the reference voltage source and the ripple and noise introduced by other circuit components
  - Linearity Error is defined as a measure of the variation in voltage step size normally specified as a fraction of 1 LSB
  - Differential Nonlinearity (DNL) Error is any deviation from 1 LSB value that may occur in two successive output codes
  - Integral Nonlinearity (INL) Error is the maximum deviation of the code centre line from the straight line passing through the end points of the ideal characteristics after nulling the offset and gain errors

- Dither is a very small amount of random noise which is added to the input before A/D conversion and its amplitude is set to half of the LSB value and it extends the effective range of signals that the A/D converter can convert at the expense of a slight increase in noise
  - The time required for an A/D converter to convert an analog input value into its equivalent digital data is called the conversion time.
  - Input voltage range is the range of voltage that an A/D converter can accept as its input without causing any overflow in the digital output
- The A/D converters (ADC) can be classified as follows
- based on their operational features as
    - ◆ Programmed A/D converters
    - ◆ Non-programmed A/D converters
  - based on their constructional features as
    - ◆ Closed-loop or feedback type A/D converters
    - ◆ Open-loop type A/D converters
  - based on the treatment of signal as
    - ◆ Capacitor – charging type A/D converters
    - ◆ Discrete voltage comparison type A/D converters
  - based on their conversion techniques as
    - ◆ Direct type A/D converters
    - ◆ Integrating type A/D converters
- The simultaneous type or flash type A/D converter compares an unknown analog input voltage with a set of reference voltages. It is the fastest A/D conversion method, since it is performed simultaneously through a set of comparators.
- The simultaneous type A/D converter is not suitable for A/D conversion with more than 3 or 4 digital output bits since  $(2^n - 1)$  comparators are required for an  $n$ -bit A/D converter and the number doubles for each added bit.
- The counter type A/D converter has its count advancing by one count for every clock pulse and, therefore, the clock speed decides the conversion speed. But, the counter type A/D converter is simple and needs less hardware, it is suitable for digitising applications with high resolution. The main disadvantages are very long and variable conversion time.
- The continuous type A/D converter is faster than the counter type as the conversion starts from the previous counted value using an UP/DOWN counter mechanism instead of resetting the counter every time. The disadvantages are the additional logic required to control the circuit, the variable conversion time which depends on the last converted value and the inefficient tracking for rapidly changing analog inputs resulting in tracking error.
- The successive approximation type A/D converter has constant conversion time and it is proportional to the number of bits in the digital output. The basic principle of successive approximation type A/D converter is that the unknown analog input voltage is approximated against an  $n$ -bit digital value by trying one bit at a time, beginning with the MSB. Successive approximation register (SAR) finds the required value of each successive bit by trial and error method.
- AD7582 from Analog Devices Corporation is a 28-pin DIP CMOS package for 12-bit A/D conversion using successive approximation technique. ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters.
- Single Slope Type A/D Converter compares the unknown analog input voltage with a reference voltage that begins at 0 V and increases linearly with time. The disadvantage of single slope converter is the component value errors and the clock errors.

- The dual slope type A/D converter generates two different ramps, one with the unknown analog input voltage as the input, and another with a known reference voltage as the input.
- An analog signal can be converted into digital signal by counting the pulses from a variable frequency source whose frequency is dependent on the analog input signal value for use as A/D converter using Voltage-to-Time conversion. The count output  $N$  obtained during the time interval 0 to  $T$  is given by  $N = F_C T = \frac{\tau F_C V_i}{V_R}$ . It can be mapped into memory space of a microprocessor and microprocessor compatible A/D converters can be realised.
- Over-sampling converters employ more complex digital circuits and they overcome the limitations such as component mismatches and nonlinearity of the components, drift, ageing, noise, dynamic limitations and parasitics found in the other converters.
- Delta modulation (DM) was developed in the 1940s and it is a differential pulse-code modulation (DPCM) technique where the derivative of the signal is quantised.
- The delta modulation A/D converter has the following processes:
  - The analog signal is approximated with a series of segments
  - Each segment is compared with the original analog wave to determine the increase or decrease in amplitude
  - The decision process for establishing the state of successive bits is determined by this comparison
  - The state related to change is sent, and a no-change condition causes the modulated signal to remain at the same 0 or 1 state of the previous sample
- The delta modulators show slope overload for fast input signals, and their performance is dependent on input signal frequency.
- The Sigma-Delta ( $\Sigma - \Delta$ ) modulator is also referred to as an interpolative coder. It comes from the principle of placing the integrator (sigma) before the delta modulator.
- The sigma-delta A/D converters find use in high-resolution and moderate speed applications such as digital audio, digital telephony, and low-frequency instrumentation designs.
- The sigma-delta converters suffer from limitations in real-time applications due to the latency introduced in the digital filter/decimator stage, while computing and passing the information from input to output through various stages of the filter.

## REVIEW QUESTIONS

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1. What do you mean by data converters?
2. Define D/A conversion.
3. Distinguish full-scale error and linearity error of a D/A converter.
4. Describe the various specifications of a D/A converter.
5. What do you understand by offset error in a D/A converter?
6. Define (i) Monotonicity and (ii) Settling time of a D/A converter.
7. What is meant by the resolution of a D/A converter?
8. A system uses a 16-bit word to represent the input signal. If the maximum peak-to-peak voltage at the output is set for 5V, find the resolution of the system and the dynamic range.
9. A 16-bit D/A converter has an output of voltage range from 0 to 2.55 V. Find the resolution of the system.
10. A 4-bit D/A converter has a resolution of 10 mV/bit. Find the analog output voltage for the inputs (a) 1010 and (b) 0001.
11. How many bits are required to design a D/A converter, that can have a resolution of 5 mV? The ladder has +8V full scale.

12. Determine the output voltage produced by a 4-bit DAC whose output voltage range is 0 to 10 V, when the input binary number is 0110.
13. List the essential parts of a D/A converter.
14. What is the principle of multiplying D/A converters? Explain.
15. Define the process of sampling. What is its use?
16. Write a note on Shannon's sampling theorem.
17. Draw a fundamental Sample-and-Hold circuit. What factors contribute to the *hold mode droop* in this circuit?
18. Explain the operation of a Sample-and-Hold integrated circuit with a neat figure showing the principle of operation.
19. Explain the 4-bit weighted resistor type D/A converter in detail.
20. What are the limitations of weighted resistor type D/A converter?
21. How many resistors are required for an 8-bit weighted resistor D/A converter? What are those resistance values, assuming the smallest resistance is  $R$ ?
22. What are the advantages of  $R$ - $2R$  ladder type D/A converter over weighted resistor type?
23. Explain a 4-bit  $R$ - $2R$  ladder type D/A converter in detail.
24. What is the advantage of inverted  $R$ - $2R$  ladder network D/A converter over  $R$ - $2R$  ladder D/A converter?
25. The inverted  $R$ - $2R$  ladder shown in Fig. 11.10 has  $R = R_f = 22 \text{ k}\Omega$  and  $V_R = 12 \text{ V}$ . Calculate the total current delivered to the op-amp and the output voltage when the binary input is 1110.
26. Differentiate between current-mode and voltage-mode  $R$ - $2R$  ladder D/A converters. Explain.
27. Explain the functional diagram and operating principle of a D/A converter IC.
28. Explain a microprocessor compatible D/A converter IC.
29. Why are the electronic switches necessary in D/A converters?
30. Describe various types of electronic switches used in D/A converters.
31. What is the need for A/D converter?
32. What are the different types of A/D converters?
33. How do you classify the A/D converters based on their operational features?
34. Describe various specifications of an A/D converter.
35. Determine the resolution of an 8-bit A/D converter for a 10V input range.
36. What do you mean by quantisation error in an A/D converter?
37. Define aliasing error.
38. What are the sources of analog error in an A/D converter?
39. What is meant by differential linearity of an A/D converter?
40. Define the conversion time of an A/D converter.
41. What is the resolution of an A/D converter?
42. What is the minimum quantisation error that can be achieved in an A/D converter?
43. An 8-bit A/D converter accepts an input voltage signal of range 0 to 12 V.
  - (i) What is the minimum value of the input voltage required to generate a change of 1 LSB?
  - (ii) What input voltage will generate all 1s at the A/D converter output?
  - (iii) What is the digital output for an input voltage of 6 V?
44. Explain a typical simultaneous type A/D converter in detail.
45. Design a 3-bit simultaneous type A/D converter.
46. What are the limitations of simultaneous type A/D converter?
47. What are servo-tracking A/D converters? Why are they called so? How is it better than counter type A/D converter?
48. Which type of A/D converter is faster? Why?
49. What is Flash type A/D converter? Why is it called so?
50. With a neat block diagram, explain the counter type A/D converter in detail.

51. What are the advantages of counter type A/D converter?
52. Explain continuous type A/D converter with a neat block diagram.
53. What are the advantages and disadvantages of continuous type A/D converter?
54. What are the advantages of continuous type A/D converter over counter type A/D converter?
55. Describe the successive approximation A/D conversion principle.
56. With a neat block diagram, explain successive approximation type A/D converter in detail.
57. Explain the construction and working of single slope type A/D converter in detail.
58. Describe the operation of dual slope A/D converter with necessary diagrams.
59. Distinguish between single slope and dual slope types of A/D converters.
60. What are over-sampling converters?
61. Explain delta modulators and demodulators.
62. What is a delta modulation encoder?
63. Explain the principle of delta modulators.
64. What are the types of delta modulators?
65. Define slope overload distortion and granular noise.
66. Explain the operation of sigma-delta modulator for A/D conversion with a neat figure.
67. What is first order sigma-delta D/A converter?
68. Define dither. What is its use?
69. Explain the principle of operation and functional diagram of any one A/D converter IC.
70. Explain a microprocessor compatible ADC IC with its functional diagram.
71. An 8-bit D/A converter has a resolution of 10 mV. Find the full-scale voltage and the output voltage when the input is 1100000.
72. What is the maximum resistor ratio used in a 12-bit binary-weighted D/A converter circuit?
73. For a 4-bit  $R-2R$  ladder D/A converter assume that the full-scale voltage is 10 V. Calculate the step change in output voltage when the input changes from 1001 to 1110.

# Special Function Integrated Circuits

# 12

## 12.1 INTRODUCTION

A number of amplifiers and integrated circuits designed for specific applications are available as monolithic ICs. This chapter deals with special purpose amplifiers such as tuned amplifier, audio amplifier and video amplifier. The operational features and application aspects of the special function integrated circuits, namely, voltage-to-frequency and frequency-to-voltage converters, opto-coupler, isolation amplifier, fibre-optic and compander ICs are also discussed.

## 12.2 VOLTAGE-TO-FREQUENCY AND FREQUENCY-TO-VOLTAGE CONVERTERS

A *Voltage-to-Frequency* (V/F) converter produces an output signal whose frequency at any instant is a function of the external control input voltage. The output signal may be a sine-wave, a square-wave or a train of pulses. The ideal characteristic of V/F converter is shown in Fig. 12.1(a), and it is represented by  $f_o = k_v V_i$  where  $k_v$  is the *sensitivity* of V/F converter in Hertz per Volt. The V/F converter provides a simple form of *analog-to-digital* conversion also. The term Voltage Controlled Oscillator (VCO) is synonymous with V/F converter. But, V/F converters have more stringent performance requirements, namely

- (i) wider dynamic range (4 decades or more)
- (ii) ability to operate at higher frequencies typically in the range of MHz
- (iii) low linearity errors (less than 0.1% deviation) and
- (iv) high accuracy and stability at high temperatures and at varying supply voltages

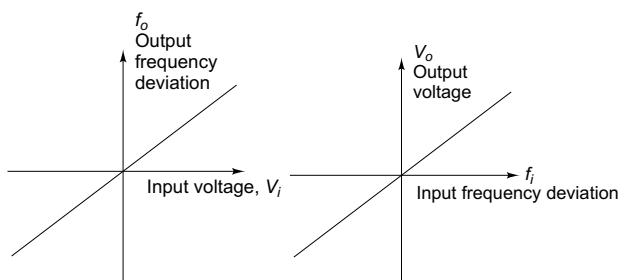
A *Frequency-to-Voltage* (F/V) converter produces an output voltage, whose amplitude is a function of frequency of the input signal. The input may be a sine-wave, a square-wave or a pulse train. The F/V converter is essentially an *FM detector* or *discriminator*.

An ideal F/V converter produces an analog signal represented by the relation

$$V_o = k_f f_i$$

where  $k_f$  is the *sensitivity* of F/V converter in Volts per Hertz. The ideal conversion characteristic of an F/V converter is shown in Fig. 12.1(b).

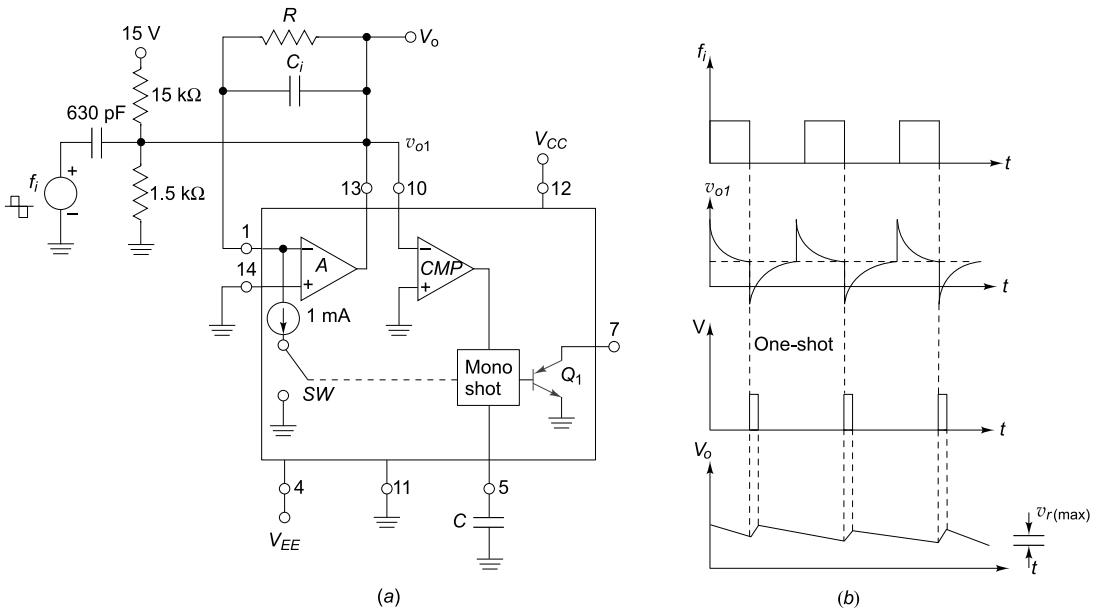
The F/V converters are used as tachometer in motor speed control and rotational speed measurement. The two types of F/V converters are (i) Pulse-integrating F/V converters, and (ii) Phase-locked-loop F/V converters.



**Fig. 12.1** Ideal characteristics of (a) V/F Converter, and (b) F/V Converter

### 12.2.1 IC VFC32 Frequency-to-Voltage Converter

Figure 12.2(a) shows the circuit of F/V converter using the VFC32 V/F converter from Burr Brown. The input frequency is applied to the comparator *CMP* and the output is derived from the op-amp *A*. The resistor *R* acts as a feedback resistor. The capacitor  $C_i$  enables charge-balancing.



**Fig. 12.2** (a) F/V converter using VFC32 (b) Input and output characteristics

A *high-pass* network is connected at the input to accommodate TTL and CMOS compatible signals. It provides proper conditioning for the input signal and helps in accommodating inputs of TTL and CMOS type. For each negative spike of  $v_{o1}$ , the comparator *CMP* triggers the one-shot multivibrator, which has a threshold of 7.5 V and a charging current of 1 mA. The output of multivibrator closes the switch *SW*,

pulling 1 mA out of  $C_i$  for a duration  $T_H$ , where  $T_H = \frac{Cv_i}{I} = \frac{C \times 7.5}{1 \times 10^{-3}}$ . This action causes  $V_o$  to build up and inject via  $R$ , and it continues until the current pulled out of the summing input of op-amp  $A$  in 1 mA packets is exactly counter-balanced by that injected by  $V_o$  through  $R$  continuously.

Assume  $f_i$  to be the input frequency. Then the pulsed current is given by  $f_i \times 1 \text{ mA} \times T_H$  and the continuous counter-balancing current is given by  $\frac{V_o}{R}$ . That is,

$$V_o = 10^{-3} \times T_H \times R \times f_i \quad (12.1)$$

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$$T_H = \frac{C \times 7.5}{1 \times 10^{-3}}, \text{ the output voltage } V_o = 7.5 R C f_1$$

where  $f_i$  is in Hertz,  $V_o$  in Volts,  $R$  in Ohms and  $C$  in Farads. This indicates that the output  $V_o$  is proportional to the input frequency  $f_i$ . The waveforms at various nodes of *frequency-to-voltage* converter are shown in Fig. 12.2(b).

The maximum duty cycle recommended by the datasheet is 25% and this determines the value of  $C$ . The value of  $R$  determines the full scale value of  $V_o$ . Input offset voltage of op-amp  $A$  is to be nulled and this avoids the degradation of the conversion efficiency at low frequency ranges.

It is to be pointed out that, between successive closures of switch  $SW$ , the resistor  $R$  will cause  $C_i$  to discharge to a certain value. This creates ripples in output voltage  $V_o$ . The maximum ripple voltage is

$$v_{r(\max)} = \frac{(1\text{mA})T_H}{C_i} \quad (12.2)$$

Therefore,

$$v_{r(\max)} = \frac{7.5 \times C}{C_i}.$$

This shows that increasing the value of  $C_i$  reduces the magnitude of ripple voltage. But very large  $C_i$  degrades the circuit response to a rapid change in  $f_o$ , since the response is determined by the time constant  $\tau = RC_i$ . Hence, an optimum value of  $C_i$  is to be chosen to meet the conflicting demand.

### 12.2.2 Voltage-to-Frequency Converter using VFC32

VFC32 can be used for *Voltage-to-Frequency* conversion. This IC uses *charge balancing* technique. The process of charging and discharging results in a train of charge pulses, whose frequency is directly proportional to the input signal as given by  $f_o = kV_i$ .

A basic block diagram with the external connections for V/F conversion is shown in Fig. 12.3(a). The op-amp  $A$  converts the input  $V_i$  to a current as given by  $I_i = V_i/R$  which flows into its summing junction. The value of  $R$  is selected such that  $I_i$  is always less than 1 mA. When the switch  $SW$  is *open*, the current  $I_i$  flows into the capacitor  $C_i$  and charges it, causing the node  $v_{o1}$  to ramp downward as shown by line  $ab$  of Fig. 12.3(b). When  $v_{o1}$  reaches zero, the comparator  $CMP$  triggers and sends a triggering signal to one-shot multivibrator that closes the switch  $SW$  and also turns the transistor  $Q$  ON for a time interval  $T_H$  set by capacitor  $C$ . The monostable multivibrator uses a threshold of 7.5 V and a charging current of 1 mA, thus giving

$$T_H = \frac{7.5 \times C}{1 \times 10^{-3}} \quad (12.3)$$

When the switch  $SW$  closes, a net current of magnitude  $(1\text{mA} - I_i)$  flows out of the summing junction of op-amp  $A$ . Therefore, during the time  $T_H$ , the  $v_{o1}$  ramps upward by an amount given by

$$\Delta v_{o1} = (1\text{mA} - I_i)T_H/C_i \quad (12.4)$$

This is shown as line  $bc$  in the Fig. 12.3(b). When the one-shot times out, the switch  $SW$  is again opened, and  $v_{o1}$  continues ramping downward at a rate determined by input current  $I_i$ . The time duration  $T_L$  taken for  $v_{o1}$  to return to zero is given by

$$T_L = C_i \Delta v_{o1}/I_i \quad (12.5)$$

$T_L$  and  $T_H$  are related as given by

$$I_i T_L = (1\text{mA} - I_i)T_H$$

That is,

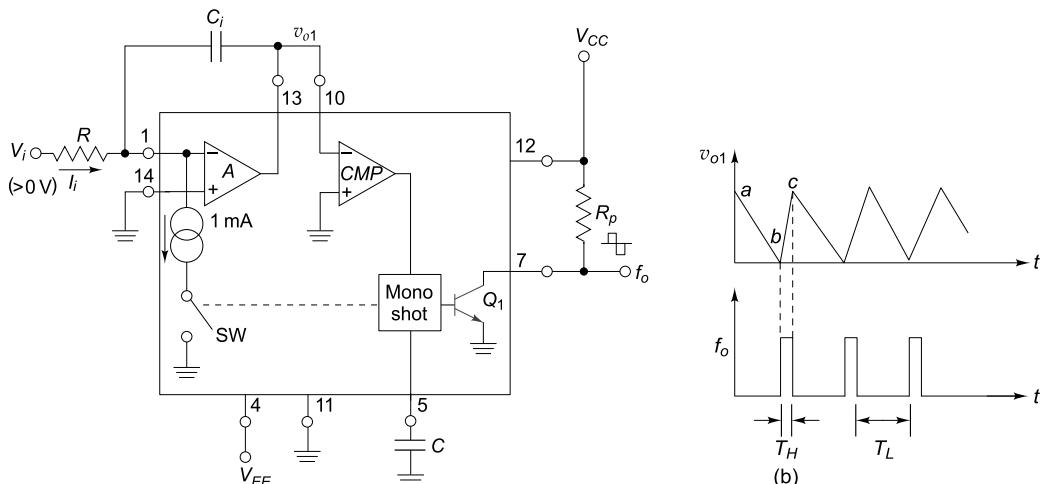
$$T_L + T_H = (1\text{mA})T_H/I_i \quad (12.6)$$

Combining Eqs. (12.3) with (12.6), and letting  $I_i = V_i/R$  and  $f_o = 1/(T_L + T_H)$  gives

$$f_o = \frac{V_i}{7.5RC} \quad (12.7)$$

where  $f_o$  is in Hertz,  $V_i$  in volt,  $R$  in  $\Omega$  and  $C$  in farad. Equation (12.7) shows that  $f_o$  is linearly proportional to  $V_i$ .

The duty cycle  $D (\%) = 100 \times \frac{V_i}{R \times 1 \text{ mA}}$  which shows that the duty cycle  $D$  is proportional to  $V_i$ . For good linearity, the datasheets recommend a maximum duty cycle of 25%, which corresponds to an  $I_i(\text{max})$  of 0.25 mA. Therefore, the capacitance  $C_i$  can be chosen arbitrarily.



**Fig. 12.3 (a)** Voltage-to-frequency Converter using VFC32   **(b)** Input and output characteristics

The VFC32 offers 6-decades of dynamic range with typical linearity errors of 0.005%, 0.025% and 0.05% of full-scale reading for corresponding frequencies of 10 kHz, 100 kHz and 500 kHz.

## 12.3 9400 SERIES VOLTAGE-TO-FREQUENCY AND FREQUENCY-TO-VOLTAGE CONVERTERS

The 9400 series of ICs, namely, 9400, 9401 and 9402 manufactured by Teledyne Inc. can be used for *voltage-to-frequency* and *frequency-to-voltage* conversions. They are designed for producing pulse and square-wave output in the frequency range of 1 Hz to 100 kHz. The input can be either current or voltage and the output is compatible with logic circuits. The 9400 is available in 14-pin DIP and ceramic packages. The features and applications of the IC 9400 series are as given below:

### Voltage-to-Frequency Converter

#### Choice of Guaranteed Linearity:

TC9401	0.01%
TC9400	0.05%
TC9402	0.25%

dc to 100 kHz (F/V) or 1 Hz to 100 kHz (V/F)

Low power dissipation	27 mW Typ.
Single/Dual supply operation	+ 8 V to + 15 V or $\pm 4$ V to $\pm 7.5$ V
Gain temperature stability	$\pm 25 \text{ ppm}^{\circ}\text{C}$ (Typ.)
Programmable Scale Factor	

### Frequency-to-Voltage Converter

Operation	dc to 100 kHz
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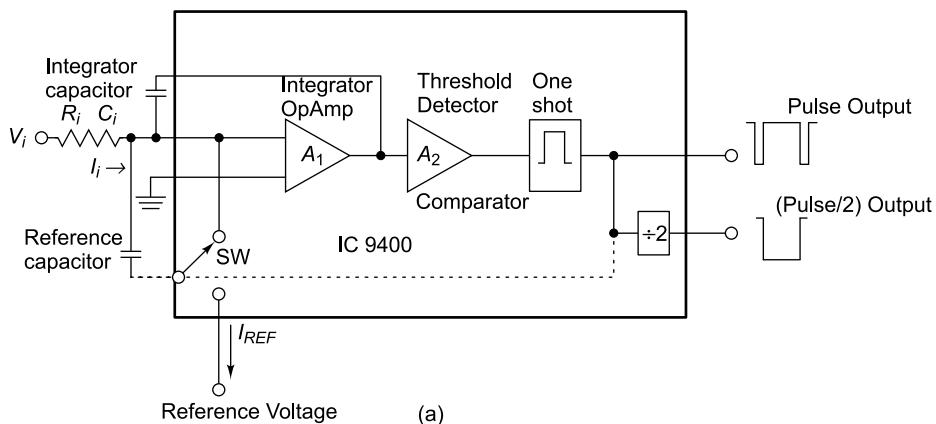
### Choice of Guaranteed Linearity:

TC9401	0.02%
TC9400	0.05%
TC9402	0.25%

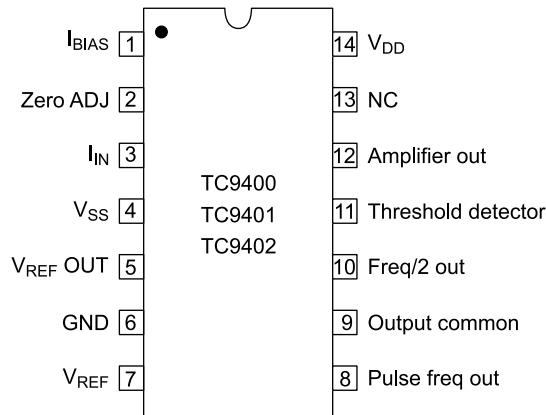
Programmable Scale Factor

### Pin Configuration

The block diagram and pin diagram of IC 9400 are shown in Fig. 12.4(a) and (b). The detailed internal block is shown in Fig. 12.5(a) inside the dotted lines. The pin 11 (*Threshold Detect*) is connected to the non-inverting input terminal of the threshold detector/comparator and it is also connected to output of *on-chip op-amp A*<sub>1</sub> in the V/F mode, and it acts as input when used in F/V mode. Pin 8 gives pulse output  $f_o$  whose frequency is proportional to the input voltage. Pin 10 is a frequency *divide-by-2* output. It provides a square-wave output that is one-half of that available at pin 8. The outputs at pins 8 and 10 are *open-collector types* and need *pull-up resistors*. Pin 9 acts as common terminal for the outputs  $f_o$  and  $f_o/2$  at pins 8 and 10. The pin 6 acts as *input ground*.



(a)



**Fig. 12.4** (a) Block diagram of IC 9400 (b) Pin diagram

A resistor  $R_{BIAS}$  is connected between pins 1 and 4. It is normally  $100 \text{ k}\Omega \pm 10\%$ . Pin 12 gives the output of the *on-chip* op-amp  $A_1$  in V/F mode and a voltage proportional to the frequency input when operated in F/V mode. A zero adjustment is available at pin 2. Pin 3 forms the inverting input terminal of op-amp  $A_1$  and it acts as the *summing junction* in V/F mode. The input current  $I_{IN}$  is  $10 \mu\text{A}$ . A reference voltage  $V_{REF}$  from a standard voltage source or from the  $V_{EE}$  supply is applied at pin 7. The  $V_{REF}$  voltage can be made available as output at pin 5. The IC contains a *charge control* circuit with an externally connected capacitor  $C_{ref}$  between pins 3 and 5 as shown in Fig. 12.5(a).

When  $C_{ref}$  charges, pin 5 connects to  $V_{REF}$  at pin 7. Pins 14 and 4 are positive and negative supply pins respectively. Pin 13 is left unconnected. The IC is fabricated in low-power CMOS technology for achieving low input bias and offset currents with low power dissipation.

### 12.3.1 Voltage-to-Frequency Converter using IC 9400

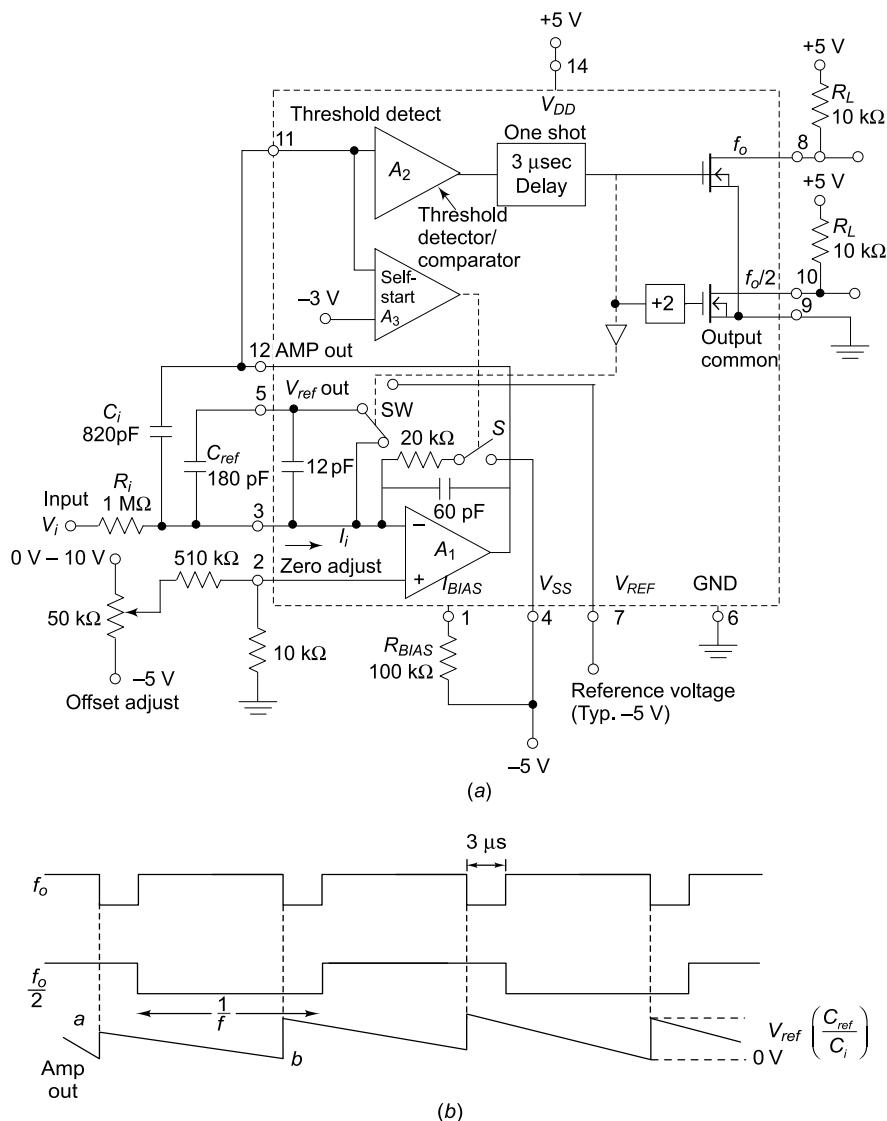
The circuit diagram and connection diagram of V/F converter using 9400 are shown in Figs. 12.5(a) and (b). The input voltage  $V_i$  is connected to the inverting input terminal of the op-amp through the resistor  $R_i$ . The resistor  $R_i$  converts the  $V_i$  to  $I_{IN}$ . The integrating capacitor  $C_i$  integrates this current and it is shown as a linearly decreasing voltage at the output of the op-amp as shown by points *a* and *b* in Fig. 12.5(b). The threshold detector/comparator sets the lower limit of the output swing. When the point *b* is just reached, the threshold detector triggers the one-shot, which now operates the switch SW to connect  $V_{REF}$  to the reference comparator  $C_{ref}$ . This action causes the reference voltage to be applied to the reference capacitor  $C_{ref}$  for a sufficient time to charge to the reference voltage, reducing the (–) charge on the integrating capacitor by a fixed amount of  $Q = C_{ref} \times V_{REF}$ . This causes the output of op-amp to

increase by a finite amount  $V_{REF} \times \frac{C_{ref}}{C_i}$  as indicated in Fig. 12.5(c).  $C_{ref}$  is shorted out at the end of the

charging period, which dissipates the stored charge. When point *b* is just reached, the threshold detector triggers the one-shot, which operates the switch SW to connect  $V_{REF}$  to reference capacitor  $C_{ref}$ . This continuous charging and discharging of  $C_i$  by the input voltage and the corresponding balancing action by the fixed charges of the reference voltage  $V_{REF}$  repeats. When the input voltage is high, the number of reference pulses required to maintain balance increases, thereby increasing the output frequency. The change in frequency is linear with respect to the voltage input, due to fixed charge increments.

The IC TC9400 contains a *self-start* circuit using op-amp  $A_3$ , which ensures that the V/F converter is initialised properly. During *power-on*, if the output of op-amp  $A_1$  is below the threshold and  $C_{ref}$  is charged, a positive voltage step will not be occurring. When this happens, the self-start op-amp  $A_3$  triggers switch S ON. Then the output of op-amp  $A_1$  will start decreasing until it crosses the  $-3 \text{ V}$  threshold level of the self-start comparator as shown in Fig. 12.5(b). When it crosses the  $-3 \text{ V}$  level, the threshold detector triggers the one-shot and the output is forced to go positive until the IC is in its normal operating mode.

The typical values for a  $10 \text{ kHz}$  full scale output frequency for a maximum input of  $10 \text{ V}$  is shown in Fig. 12.5(a). The waveforms at the pins 8, 10 and 12 are shown in Fig. 12.5(b).



**Fig. 12.5** Voltage-to-Frequency Converter using IC TC9400: (a) Block diagram  
(b) Output waveforms

**V/F converter design information** The voltage-to-frequency converter can be designed by identifying the design parameters as discussed below.

#### (i) Input/Output Relationships

The output frequency ( $f_o$ ) is related to the analog input voltage ( $V_i$ ) by the transfer equation given by

$$f_o = \frac{V_i}{R_i} \times \frac{1}{(V_{REF})(C_{ref})}$$

### (ii) External Component Selection

**Input Resistor  $R_i$ :** The value of resistor  $R_i$  is given by

$$R_i = \frac{V_{i(FULL-SCALE)}}{10\mu A}$$

The value of this component is chosen to give a full-scale input current of approximately  $10\mu A$ . In practice, the value of  $R_i$  typically would be trimmed to obtain full-scale frequency at  $V_i$  full scale. Metal film resistors with 1% tolerance or better are recommended for high-accuracy applications because of their thermal stability and low-noise generation.

**Integrating Capacitor  $C_i$ :** The exact value of  $C_i$  is not critical but it is related to  $C_{ref}$  by the relationship

$$3C_{ref} \leq C_i \leq 10C_{ref}$$

Improved stability and linearity are obtained when  $C_i \geq 4 C_{ref}$ . Low-leakage types are recommended, although mica and ceramic devices can be used in applications where their temperature limits are not as clear as possible.

**Reference Capacitor  $C_{ref}$ :** The value of  $C_{ref}$  is not critical, and it is designed for maximum full-scale output frequency.

### (iii) Supply points $V_{DD}$ , $V_{SS}$

The power supply of  $\pm 5$  V with 0.05% line and load regulations is used for high-accuracy requirements. A disc capacitor of  $0.1\mu F$  is used for decoupling located near the power connection lead.

### (iv) Adjustment Procedure

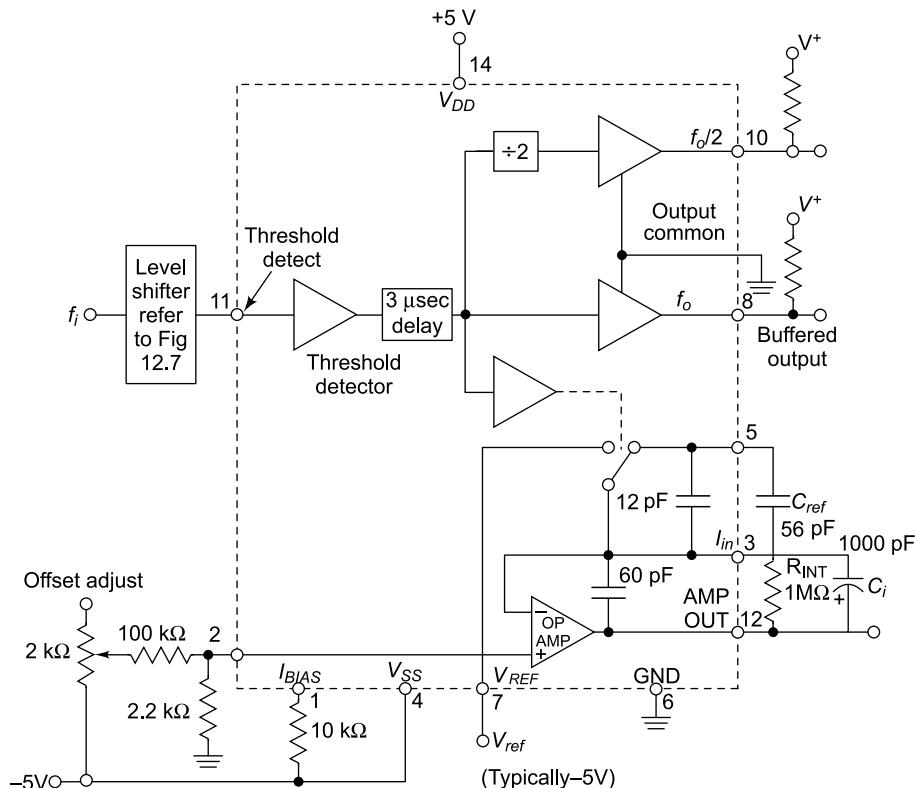
Figure 12.5(a) shows the circuit for trimming the zero output frequency with the use of the *Zero Adjust* terminal at pin 2, when the input voltage is zero. Full scale may be trimmed by adjusting  $C_i$ ,  $R_i$ ,  $V_{REF}$  or  $C_{ref}$ . The recommended procedure for achieving a full-scale frequency of  $10\text{ kHz}$  is as follows:

- (i) Set  $V_i$  to  $10\text{ mV}$  and trim the *Zero Adjust* circuit for obtaining a  $10\text{ Hz}$  output frequency.
- (ii) Set  $V_i$  to  $10\text{ V}$  and trim  $R_i$ ,  $V_{REF}$  or  $C_{ref}$  for obtaining a  $10\text{ kHz}$  full-scale output frequency.

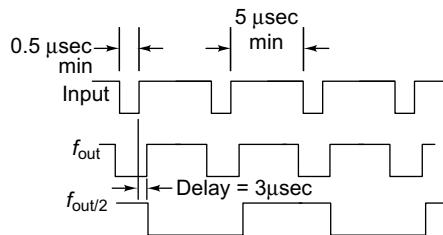
## 12.3.2 Frequency-to-Voltage Converter using IC 9400

The circuit diagram of the F/V converter using IC9400 is shown in Fig. 12.6(a). The input frequency  $f_i$  is applied to the *threshold detector* input (non-inverting terminal) of the on-chip comparator at pin 11. The threshold detector/comparator has an inbuilt hysteresis of  $\pm 200\text{ mV}$ . The input signal amplitude is set by the hysteresis of  $\pm 200\text{ mV}$  of the comparator. Therefore the input signal amplitude must be greater than the hysteresis value to trigger the comparator.

The output voltage is related to the input frequency by the relation  $V_o = (V_{REF} C_{ref} R_i) f_i$ . The factor  $R_i C_i$  determines the response time for a change in input voltage. The signals  $f_o$  and  $(f_o/2)$  are available at pins 10 and 8 for some applications. The output of the comparator is applied to the output transistor through a  $3\mu s$  delay network. Therefore, a  $3\mu s$  delay is introduced on the raising edge of the  $f_o$  signal as shown in Fig. 12.6(b). The pins 8 and 10 are grounded when they are not used. The circuit can accept input frequencies with a positive pulse width of at least  $5\mu s$  and negative pulse width of  $>0.5\mu s$  as shown in Fig. 12.6(b).



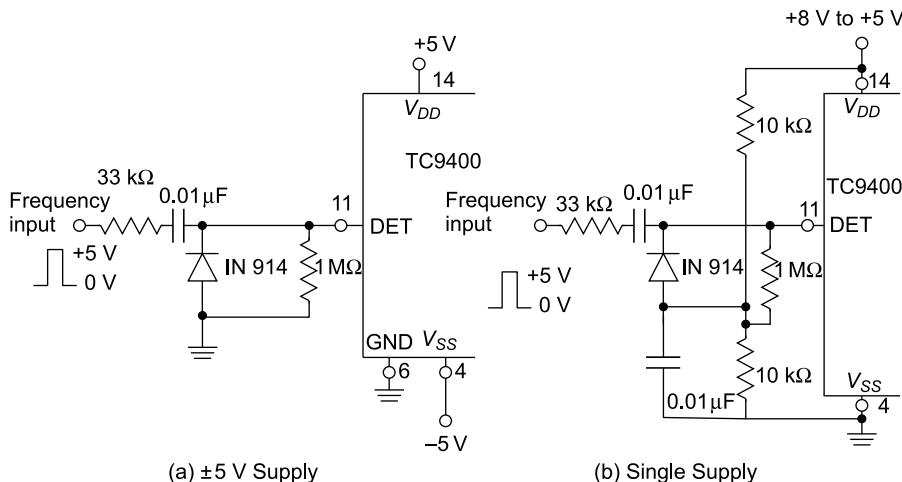
**Fig. 12.6** (a) Circuit diagram of F/V converter using IC 9400



**Fig. 12.6** (b) Digital output waveforms of F/V converter

**Input voltage levels** The input frequency applied to the Threshold Detector input (Pin 11) is approximately of voltage amplitude  $(V_{DD} + V_{SS})/2 \pm 400$  mV. Input voltage at Pin 11 ranges from  $V_{DD}$  to about 2.5 V below the threshold. If the voltage goes more than 2.5 V below the threshold, the V/F mode startup comparator will turn ON and corrupt the output voltage. The Threshold Detector input has about 200 mV of hysteresis. In  $\pm 5$  V applications, the minimum input voltage levels for the TC9400 are  $\pm 400$  mV. If the frequency source being measured is unipolar, such as the signals from TTL or CMOS operating from a +5 V source, then an *ac*-coupled level shifter circuit is used. Figures 12.7(a) and (b) show the frequency input level shifter circuit for a dual power supply and unipolar power supply. The resistive divider ensures that the input threshold will track the supply voltages. The clamp diode prevents

the input from going far in the negative direction to turn ON the startup comparator. The forward voltage of the diode decreases by  $2.1 \text{ mV}^{\circ}\text{C}$ . Therefore, two diodes in series are recommended for operation at high ambient temperature.



**Fig. 12.7** Frequency input level shifter (a)  $\pm 5 \text{ V}$  supply, and (b) Unipolar power supply

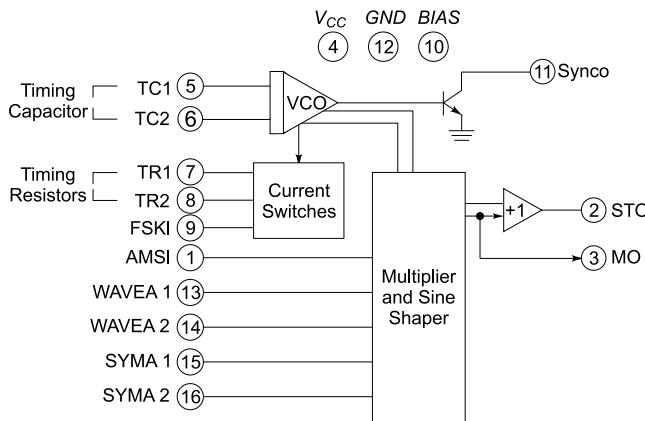
## 12.4 XR-2206 FUNCTION GENERATOR

The XR-2206 from Exar is a function generator which generates triangular and square waveforms. It also consists of a logarithmic wave-shaper for converting the triangular wave to sine-wave. Its features are:

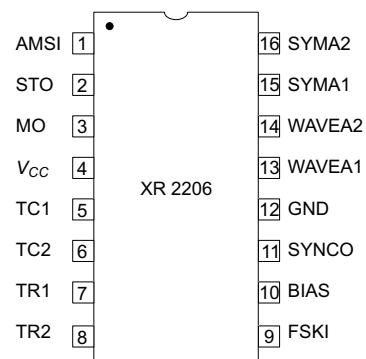
- (i) Low sine-wave distortion : 0.5%, Typical
- (ii) Excellent temperature stability : 20 ppm/ $^{\circ}\text{C}$ , Typ.
- (iii) Wide sweep range : 2000:1, Typical
- (iv) Low supply sensitivity : 0.01%/V, Typ.
- (v) Linear amplitude modulation
- (vi) TTL compatible FSK controls
- (vii) Wide supply voltage range : 10V to 26V
- (viii) Adjustable duty cycle : 1% to 99%

The XR-2206 function generator is used in waveform generation, sweep generation, AM/FM generation, V/F conversion, FSK generation and voltage controlled oscillator circuit of Phase-Locked Loop.

**System description** Figures 12.8(a) and (b) show the internal pin diagram and block diagram of the XR-2206 function generator respectively. It comprises four functional blocks, namely, a voltage-controlled oscillator (VCO), an analog multiplier, a sine-wave shaper, a unity gain buffer amplifier and a set of current switches. The VCO produces an output frequency proportional to an input current, set by a resistor connected from the timing terminals to ground. With two timing pins, two discrete output frequencies can be independently produced for FSK generation applications by using the FSK input control pin. This input controls the *current switches*, which select the current through one of the timing resistors and routes it to the VCO.



**Fig. 12.8 (a)** Block diagram of XR2206



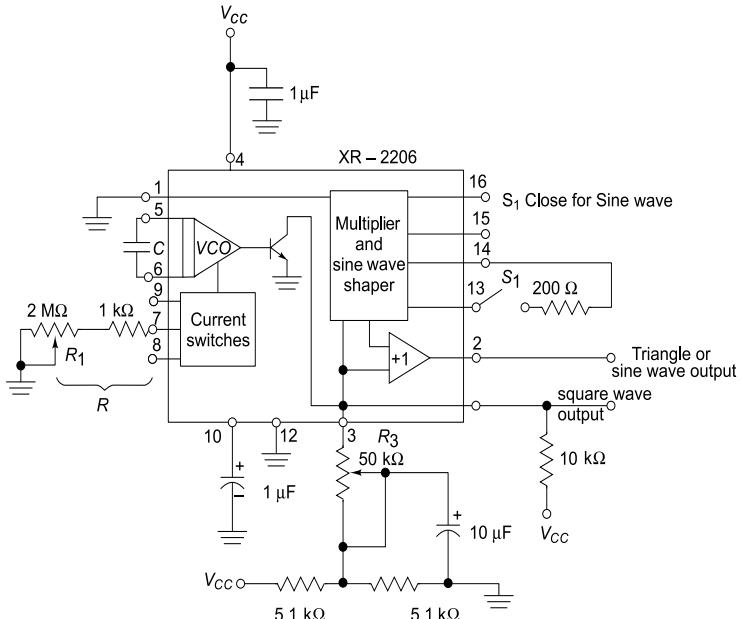
**Fig. 12.8 (b)** Pin configuration of XR2206

An emitter-coupled *current controlled oscillator* (CCO) is used for triangular and sine-wave generation. The CCO parameters are designed to produce an oscillation of frequency  $f_o = \frac{1}{RC}$ .

The operating frequency range is from 0.01 Hz to 1 MHz with a thermal stability of 20 ppm/ $^{\circ}\text{C}$ . The recommended range for  $R$  is from 1 k $\Omega$  to 2 M $\Omega$  and the optimum range is 4 k $\Omega$  to 200 k $\Omega$ . Providing a variable resistor  $R$  allows a frequency sweep of 2000:1. The  $R_{SYM}$  and  $R_{THD}$  provide symmetry and distortion adjustments respectively.

The connection diagram of a low distortion sine-wave generation circuit using XR-2206 is shown in Fig. 12.9. The amplitude and offset voltage for the sine-wave are set by the resistive network connected externally at pin 3. The sine-wave offset voltage is given by  $V_{CC}/2$  for the component values shown in Fig. 12.9.

The triangular waveform may be generated by avoiding the smoothing and rounding action. This is achieved by leaving the pins 13 and 14 open-circuited. The offset of the triangular wave is equal to that of the sine-wave and its peak is approximately twice larger. The square-wave output at pin 11 is of open-collector type and hence a pull-up resistor is needed.



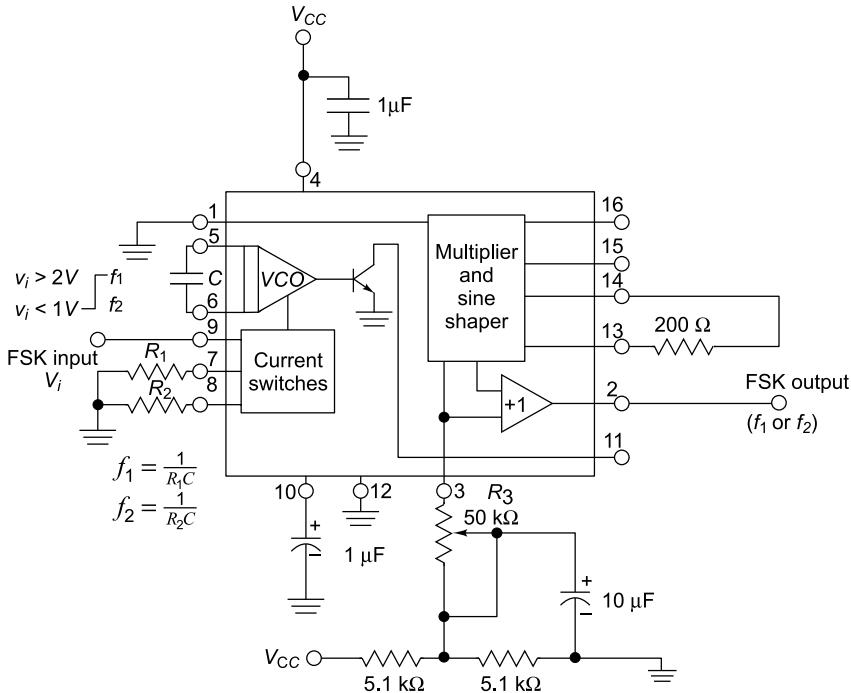
**Fig. 12.9** Sine-wave generation using XR-2206

#### **12.4.1 Sinusoidal FSK Generator using XR-2206**

The use of XR-2206 for FSK generation is shown in Fig. 12.10. Two separate timing resistors  $R_1$  and  $R_2$  are connected at pins 7 and 8. When the FSK control signal input at pin 9 is driven high, or left open-circuited, the resistor  $R_1$  becomes active and the circuit oscillates at  $f_1 = \frac{1}{R_1 C}$ . When the pin 9 is

driven low, the resistor  $R_2$  becomes active and the circuit oscillates at  $f_2 = \frac{1}{R_2 C}$ . Therefore, the circuit

can be designed to key between the two frequencies, namely, the *mark* and *space* frequencies. The two frequencies are set independently by the resistors  $R_1$  and  $R_2$ .

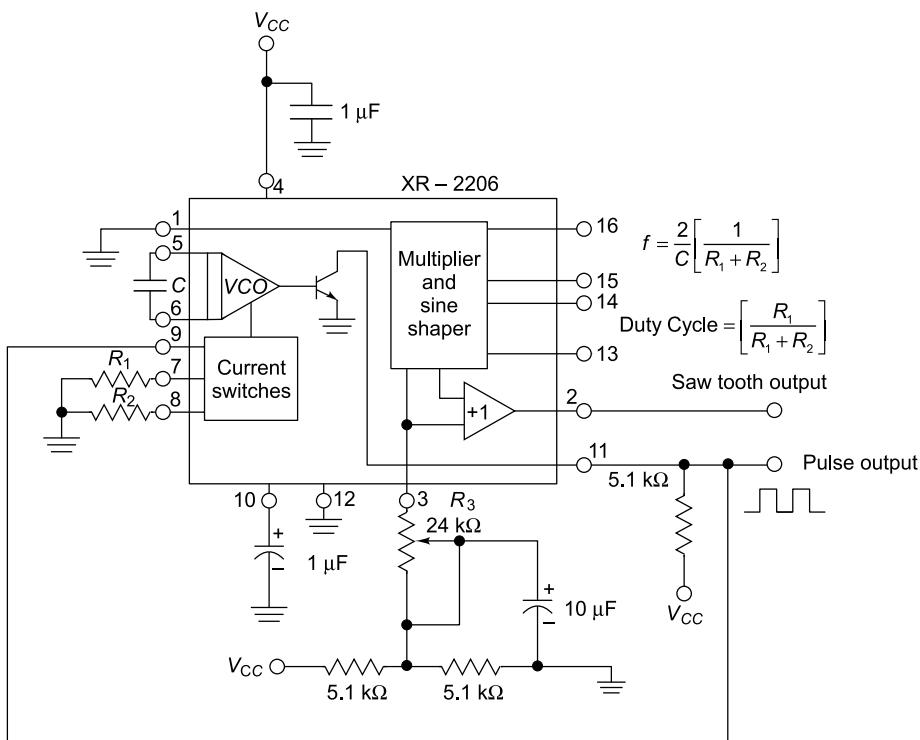


**Fig. 12.10** Sinusoidal FSK generator using XR-2206

The frequency shift keying is widely used for transmitting data over telecommunication links. If the FSK control signal is obtained from the square-wave output at pin 11, the resistors  $R_1$  and  $R_2$  will become active on alternate half cycles of oscillation. This arrangement can be used for generating saw-tooth or pulse waveforms also.

### **12.4.2 Pulse and Ramp Waveform Generation**

The pulse and ramp waveform generations using XR-2206 is shown in Fig. 12.11. In this mode of operation, the FSK keying input terminal (Pin 9) is shorted to the square-wave output (Pin 11) and the circuit automatically *frequency-shift keys* itself between two separate frequencies during the positive-going and negative-going output waveforms. The pulse width and duty cycle can be adjusted for a range of 1% to 99% by the selection of  $R_1$  and  $R_2$ . The values of  $R_1$  and  $R_2$  should be in the range of  $1\text{ k}\Omega$  to  $2\text{ M}\Omega$ .



**Fig. 12.11** Pulse and ramp generation using XR-2206

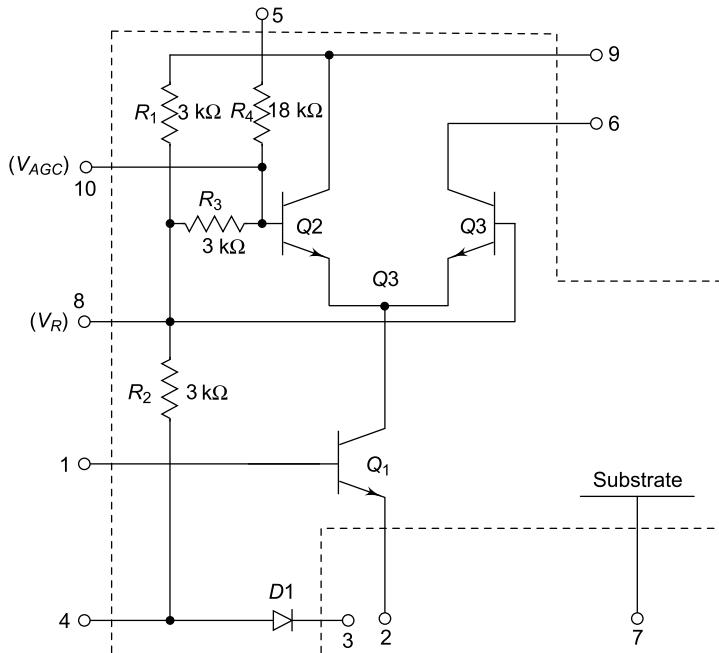
## 12.5 INTEGRATED CIRCUIT TUNED AMPLIFIER

The simplified circuit of the monolithic integrated circuit MC1550G from Motorola Semiconductor Inc. is shown in Fig. 12.12. It consists of a differential amplifier stage forming the basic building block, Automatic Gain Control (AGC) circuit, an amplitude modulator and a video amplifier.

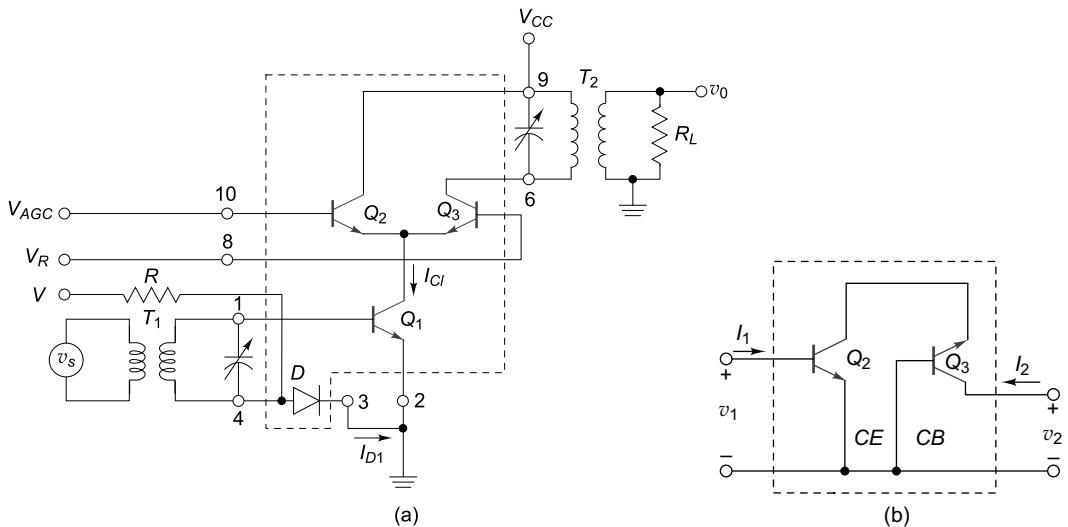
Figure 12.13(a) shows the schematic of the tuned amplifier circuit using MC1550G with external connections. The input signal  $v_i$  to be amplified is supplied to the base of transistor  $Q_1$  through the tuned transformer  $T_1$ . The output  $v_o$  from the circuit is taken across the load resistor  $R_L$  connected at the secondary of tuned transformer  $T_2$  in the collector circuit of  $Q_3$ . The transistors  $Q_1$  and  $Q_3$  in Fig 12.13(b) form a cascode pair consisting of common emitter and common base (CE-CB) configurations. These cascode-connected transistors amplify the input signal applied at the base of  $Q_1$ . The input resistance and the current gain of the cascode circuit is the same as that of the common emitter stage, and the output resistance is that offered by the common-base stage. The reverse open circuit voltage amplification of the pair is given by  $h_r \approx h_{re} h_{rb} \approx 10^{-7}$ . This extremely minimal value of  $h_r$  obtained through the cascode transistor pair combination enables this circuit to be very useful in tuned amplifier design. This feature also makes the reverse internal feedback very low. The process of tuning is simplified, and the oscillations are reduced. It results in improved stability of the amplifier.

The automatic gain control is provided by the application of voltage  $V_{AGC}$  at pin 10. From the theory of differential amplifier, it is known that if  $V_{AGC}$  is greater than  $V_R$  at pin 8 by a minimum of 120 mV, then  $Q_3$  is *cut-off* and transistor  $Q_1$  passes the current to  $Q_2$ . When  $Q_3$  is *cut-off*, its transconductance

becomes zero, and the gain  $A_v = \frac{v_o}{v_i}$  is also zero. On the other hand, when  $V_{AGC}$  is less than  $V_R$ , by at least 120 mV,  $Q_2$  is *cut-off* and  $Q_3$  conducts passing the current to  $Q_1$ . This increases the transconductance of  $Q_3$  resulting in increased voltage gain  $A_V$ .



**Fig. 12.12** MC1550G Integrated Circuit Tuned Amplifier



**Fig. 12.13** (a) Tuned amplifier consisting of  $Q_1-Q_3$  with gain control by  $Q_2$  (b) Cascode pair

The ability to vary the value of  $A_V$  by changing the voltage  $V_{AGC}$  makes this amplifier more advantageous. The input impedance of  $Q_1$  remains constant, and the input circuit is not detuned.

The biasing is provided by the resistor  $R$  using the voltage  $V$ , and it passes a current  $I_D$  through the diode  $D$  making it the base bias current of transistor  $Q_1$ .

## 12.6 AUDIO POWER AMPLIFIER

The amplifier receives an input from a signal source or from a transducer and gives out an amplified signal to the output device. Small signal amplifiers are generally voltage amplifiers. They supply larger and amplified signals to their output loads. For instance, the IC 741 op-amp can supply power in the range of 310 mW to 670 mW at a typical operating voltage of  $\pm 15$  V and load current of 25 mA. The current supplied by 741 will decrease, if the circuit is designed for a larger load.

The typical audio applications require much higher currents, which could not be delivered by general purpose op-amps. The power of the order of few watts to tens of watts is to be supplied to such loads. This is achieved by using discrete or monolithic power transistors at the output of the op-amp, or by using specialised ICs designed for the purpose. This section covers the basic features of such audio power amplifiers followed by a typical monolithic audio power amplifier, namely, IC LM380.

### 12.6.1 Features of an Audio Power Amplifier

The audio power amplifier amplifies an audio signal. The input signal for an audio amplifier is obtained from any transducer, which can be a microphone or a tape-head. It produces an ac output voltage in the audio frequency range with a specific impedance value. The input impedance of the amplifier is made greater (10 times or more), so that the transducer is not loaded. The amplified output signal from audio power amplifier is fed to output transducers such as speakers, head-phone sets or some recording devices. The output impedance of the audio power amplifier is ideally zero and supplies the required amount of power. Based on the power rating, the audio amplifier can be classified into three classes, namely:

- (i) Low power audio amplifier – 0 to 50 mW
- (ii) Medium power audio amplifier – 50 mW to 500 mW and
- (iii) High power audio power amplifier – More than 500 mW

The design of heat sink for the IC determines the amount of power deliverable by an amplifier. The *Power Conversion Efficiency* of the amplifier is defined as  $\eta = \frac{P_{ac}}{P_{dc}}$  where  $P_{ac}$  is the ac output power at the load and  $P_{dc}$  is the dc input supplied to the amplifier by the dc input supply.

### 12.6.2 Classification and Operation of Power Amplifiers

The operating point of the transistor circuit is fixed by selecting proper biasing. Based on the position of the Q-point on the load line, some classifications of the power amplifiers are Class A power amplifier, Class B Power amplifier and Class AB power amplifier with push-pull output stages.

**Class A power amplifier** The class A power amplifier has its output stage biased in the active region of operation. Therefore, the current flows continuously for the entire cycle of the input signal, and the amplifier operates during  $360^\circ$  of input signal. The maximum power conversion efficiency is 25%. Therefore, a maximum of 25% of the total dc power is converted to ac power and gets delivered to the load. To avoid the amplifier entering into non-linear regions during operation which may cause distortion, the output swing is limited to 50–80% of the total active region.

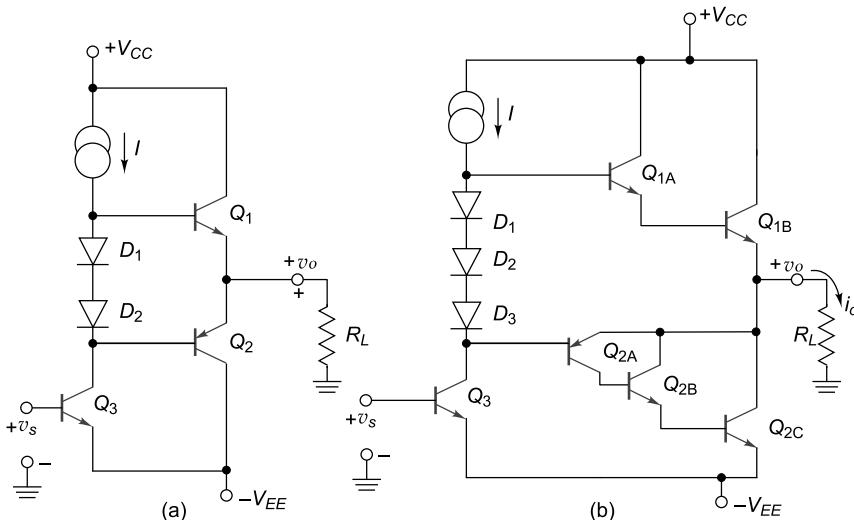
**Class B power amplifier** The output stage of class B power amplifier is biased at near *cut-off* so that the conduction occurs only for one half or  $180^\circ$  of the input signal. The *quiescent current* is zero, thereby resulting in higher power efficiency than the Class A operation. The output stage normally consists of two transistors connected in *push-pull* arrangement. The output of the push-pull operated transistors are combined to reconstruct a full cycle of the waveform. Each transistor operates in class B mode and conducts during alternate half cycles.

The maximum power conversion efficiency is 78.5%. The output swing can be reduced to avoid distortion at the cost of efficiency. The class B amplifier has a limitation in the form of cross-over distortion, which is due to very low, and almost null-gain of the transistors in the cut-off region.

If the transistors are biased slightly into the active region making the conduction angle more than  $180^\circ$ , then, the circuits are called class AB amplifiers.

**Class AB power amplifier with push-pull output stages** A simple class AB complementary push-pull emitter follower output stage is shown in Fig. 12.14(a). The transistors  $Q_1$  and  $Q_2$  form the *push-pull* output stage. The transistor  $Q_3$  operates as a common-emitter amplifier stage. The current source  $I$  acts as an active load. The voltage drop across  $D_1$  and  $D_2$  provide the base bias for  $Q_1$  and  $Q_2$ . The diodes  $D_1$  and  $D_2$  can be realised using transistors.

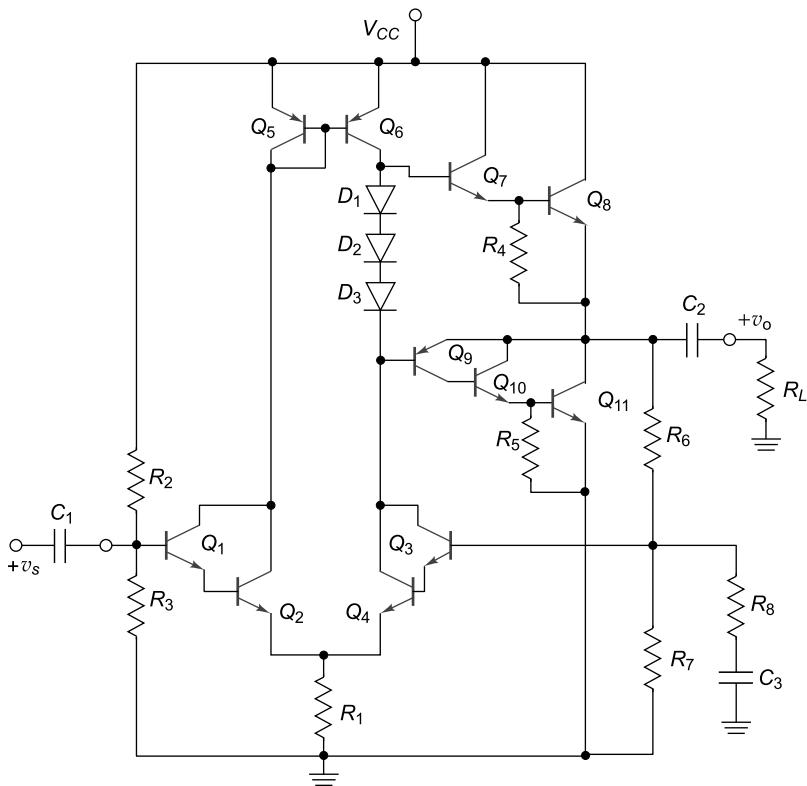
Figure 12.14(b) shows the class AB power amplifier using Darlington push-pull output stage. The transistors  $Q_{1A}$  and  $Q_{1B}$  form an *NPN* Darlington emitter follower for sourcing current to the load resistor  $R_L$ . The transistors  $Q_{2A}$ ,  $Q_{2B}$  and  $Q_{2C}$  form a composite *PNP* Darlington pair. The effective current gain of the compound transistor equals the product of the individual gains of the three transistors. This high gain makes-up for the low current gain of monolithic *PNP* transistors.



**Fig. 12.14** Circuit diagram of Class AB power amplifier using  
(a) Push-pull output stage, and (b) Darlington output stage

### 12.6.3 Single Supply Audio Power Amplifier

Figure 12.15 shows a typical circuit of a single supply audio power amplifier consisting of a Darlington differential amplifier input stage, a current mirror active load and a class AB Darlington emitter follower complementary *push-pull* output stage.



**Fig. 12.15** Single supply audio power amplifier

The transistors  $Q_1$  through  $Q_4$  form the input stage with an active load of  $Q_5$  and  $Q_6$  constituting the current mirror. The quiescent current of the differential amplifier is controlled by resistor  $R_1$  connected at the emitter junction terminals of  $Q_2$  and  $Q_4$ . The potential divider formed by  $R_2$ - $R_3$  supplies the voltage bias for the input stage. The output of this stage is fed to the emitter follower output stage, formed by the transistors  $Q_9$  through  $Q_{11}$ , which is a composite PNP Darlington emitter follower. The transistors  $Q_7$  and  $Q_8$  form a Darlington emitter follower and source the current to the load. Diodes  $D_1$ ,  $D_2$  and  $D_3$  are connected to facilitate class AB operation. Resistors  $R_4$  and  $R_5$  allow the transistors  $Q_7$  and  $Q_9$ - $Q_{10}$  composite pair to get an operating point with higher quiescent current level. They also provide path for the rapid removal of the charges trapped in the base region of the transistors. The resistors  $R_6$  and  $R_7$  provide dc feedback from the output to the base of the transistor  $Q_3$ . This stabilises the quiescent output voltage level at the desired value. The ac feedback is achieved by means of the resistor  $R_8$  with a large value capacitance  $C_3$  whose reactance is small in comparison with  $R_8$  over the usable frequency range.

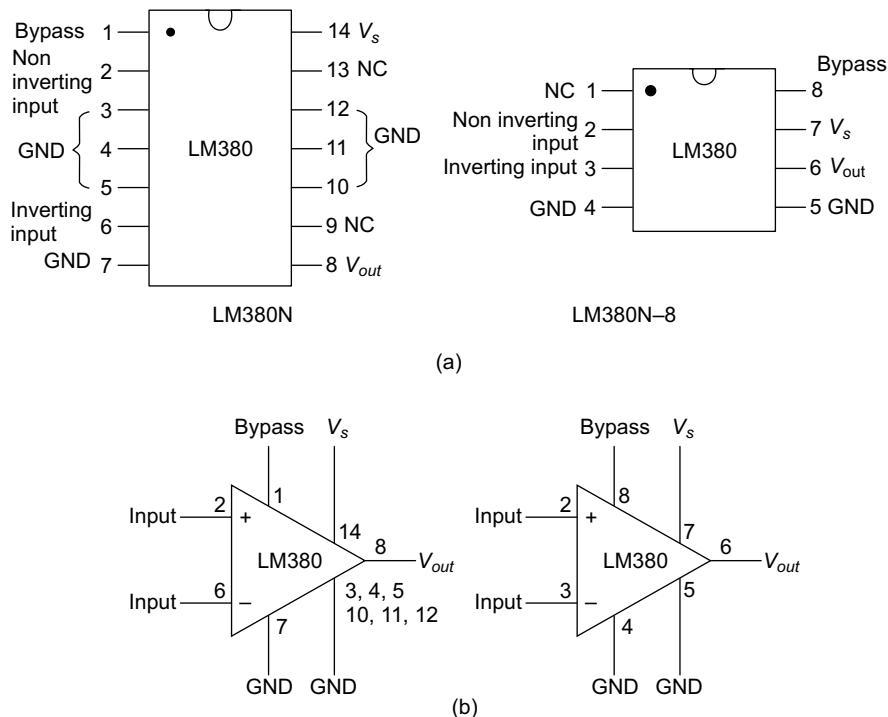
#### 12.6.4 LM380 Audio Power Amplifier

The LM380 from National Semiconductor is an audio power amplifier. The features of LM380 are as follows:

- (i) It has a wide operating supply voltage range from 5 V to 20 V.
- (ii) It operates with low quiescent power drain.
- (iii) Voltage gain of 34 dB can be achieved.

- (iv) It can deliver high peak current of 1.3 A maximum.
- (v) It has a unique, ground referenced or ac coupled input stage.
- (vi) High input impedance of the order of  $150\text{ k}\Omega$  is made available.
- (vii) It has low distortion (Total Harmonic Distortion 0.2%).
- (viii) The quiescent output voltage at one-half of the supply voltage is possible.
- (ix) The standard dual-in-line packages (8-pin and 14-pin) are available.
- (x) It can operate at temperature of  $0^\circ\text{C}$  to  $70^\circ\text{C}$ .
- (xi) A bandwidth of 100 kHz typically at an output power of 2 W and load of  $8\ \Omega$  is possible.

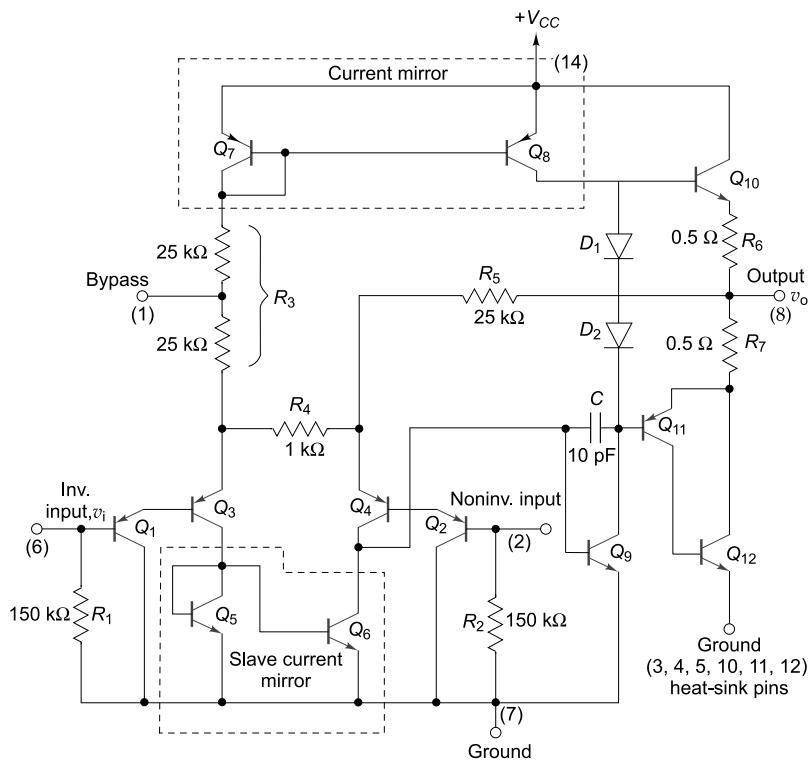
Figures 12.16(a) and (b) show the pin diagram and symbolic representation of LM380 audio power amplifier for the 14-pin and 8-pin DIP types. The heat sink is provided by a copper lead frame attached with the centre three pins on both sides, namely, pins 3, 4, 5, 10, 11 and 12 of the package.



**Fig. 12.16** LM380 Audio Power Amplifier: (a) Pin diagrams (b) Symbolic representation

**Circuit Description of LM380** The internal schematic diagram of LM380 is shown in Fig. 12.17. It consists of four stages, namely,

- (i) PNP emitter follower
- (ii) Differential amplifier
- (iii) Common emitter amplifier and
- (iv) Quasi-complementary emitter follower



**Fig. 12.17** Schematic diagram of LM380 audio power amplifier

The transistors  $Q_1$  and  $Q_2$  form the first PNP emitter follower input stage. Its output drives the  $Q_3$ - $Q_4$  PNP differential pair. The choice of PNP transistors for the input stage makes it possible to use a direct-coupled input to either inverting (pin 6) or non-inverting terminal (pin 2).

The transistors  $Q_5$  and  $Q_6$  act as collector loads for the PNP differential pair  $Q_3$ - $Q_4$ . The transistor  $Q_7$  and resistor  $R_3$  determine the current in PNP-differential pair. The transistors  $Q_7$  and  $Q_8$  form a current mirror and this establishes the collector current of  $Q_9$ . A single ended output from the differential amplifier is taken at the collector of  $Q_6$  and it is connected as input at the base of transistor  $Q_9$ .

The transistor  $Q_9$  forms the common-emitter amplifier stage.  $D_1$ ,  $D_2$  and  $Q_8$  act as an active current source load. The capacitor  $C$  connected between base and collector of  $Q_9$  provides the internal compensation. This enables an upper cut-off frequency of 100 kHz at 2 W for 8 Ω loads.

The output stage is a *quasi-complementary* pair emitter follower stage. It is formed by the NPN transistors  $Q_{10}$  and  $Q_{12}$ . Note that  $Q_{11}$  and  $Q_{12}$  produce a compound PNP transistor. It has the characteristics of a PNP transistor and the power capability of NPN transistor. A dc feedback is introduced to the emitter of  $Q_4$  through the resistor  $R_5$ . This stabilises the output. When the output  $v_o$  increases, the current flowing through  $R_5$  to the emitter of  $Q_4$  also increases. This increases the base bias of transistor  $Q_9$  which in turn causes its collector current to increase. This action reduces the base voltage of  $Q_{10}$ , and hence the output  $v_o$  is reduced.

Analysing the circuit of Fig 12.17 and assuming equal  $V_{EB}$  for all the transistors, the emitter current of  $Q_3$  is

$$I_3 \approx \frac{V - V_{EB7} - V_{EB3} - V_{EB1}}{R_3} \approx \frac{V - 3V_{EB}}{R_3}$$

The emitter current  $I_4$  of transistor  $Q_4$  is given by

$$I_4 = \frac{v_o - V_{EB4} - V_{EB2}}{R_5} \approx \frac{v_o - 2V_{EB}}{R_5}$$

where  $v_o$  is the output voltage, and the drop across  $R_2$  is neglected. Equating the currents  $I_3$  and  $I_4$ , and assuming that  $R_3 = 2R_5$ , we get

$$v_o = \frac{1}{2}V + \frac{1}{2}V_{EB}$$

Therefore, the output is biased at half of the power supply voltage. This provides the maximum output voltage swing. The current through  $R_4$  is  $\frac{v_i}{R_4}$ . The current due to output voltage  $v_o$  through  $R_5$  is  $\frac{v_o}{R_5}$ .

The sum of these currents enters the collector node of  $Q_6$ . The collector current of  $Q_3$  is approximately  $\frac{v_i}{R_3}$ . Since  $Q_5$  and  $Q_6$  form a *slave current mirror*, the current through  $Q_6$  entering the collector node is

$\frac{v_i}{R_4}$ . Therefore, at the collector node of  $Q_6$ ,

$$\frac{v_i}{R_4} + \frac{v_o}{R_5} + \frac{v_i}{R_4} = 0$$

This gives,  $\frac{v_o}{v_i} = -2\frac{R_5}{R_4} = -2\frac{25 \times 10^3}{1 \times 10^3} = -50$

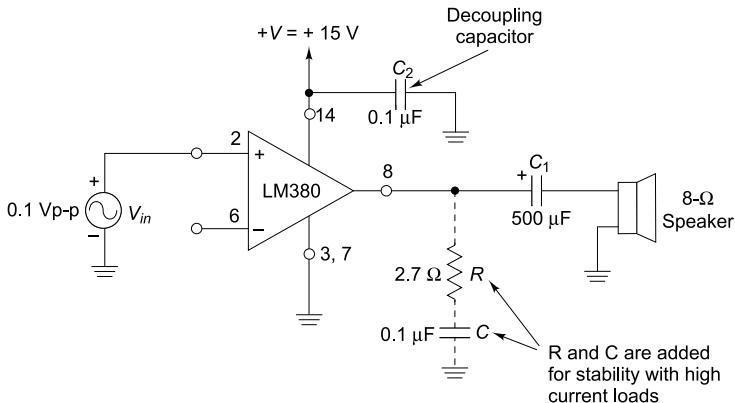
Thus the overall internal gain of the amplifier is 50.

Another commonly used audio power amplifier is LM384 that offers power up to 5 W.

### 12.6.5 Applications

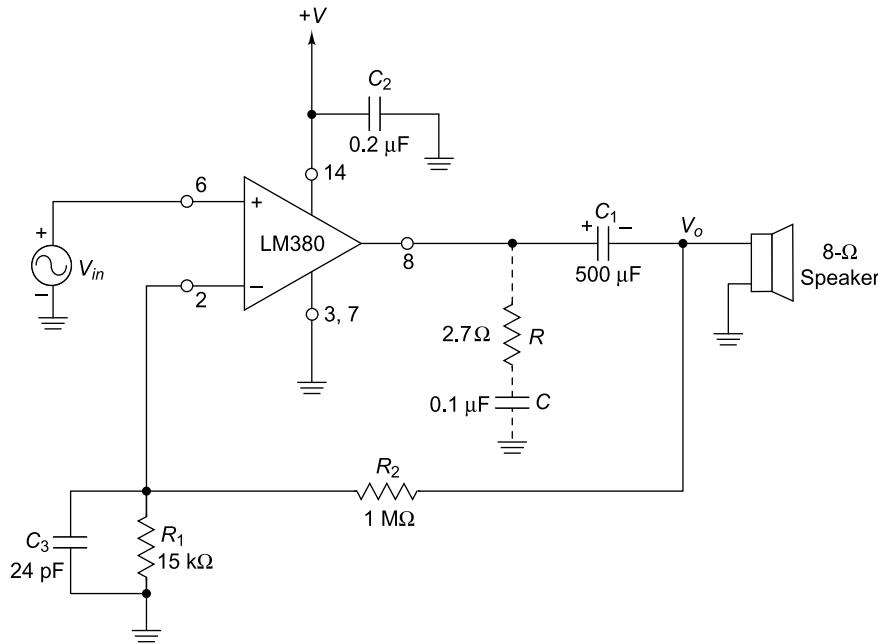
LM380 is used for applications such as audio power amplifier, high gain audio amplifier, intercom system and bridge amplifier.

**Audio power amplifier** The circuit diagram of an audio power amplifier using LM380 is shown in Fig. 12.18. The IC is connected in non-inverting mode of operation. The inverting input terminal may be either connected to ground or left open. The supply voltage is decoupled by connecting a capacitor  $C_2$  between the +ve terminal and ground. A compensating  $RC$  network is connected at the output terminal for achieving stability. This eliminates 5 to 10 MHz oscillations in an RF sensitive environment.



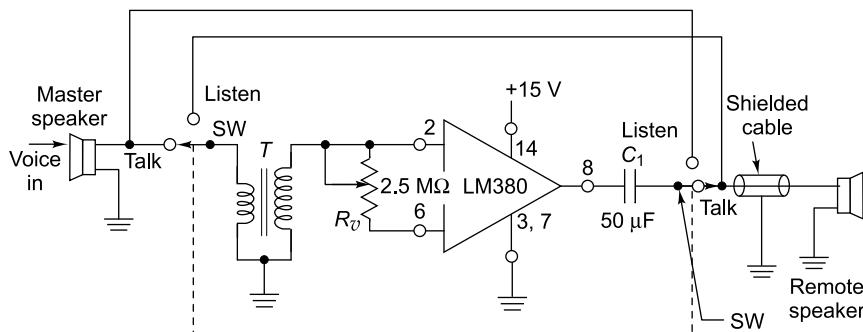
**Fig. 12.18** LM380 Audio power amplifier

**High gain audio amplifier** The gain of the LM380 audio amplifier is fixed internally at 50. But, gain values up to 300 are achievable with the use of external components. Figure 12.19 shows the LM380 configured for a gain of 200 using positive feedback.



**Fig. 12.19** High Gain Audio power amplifier using LM380

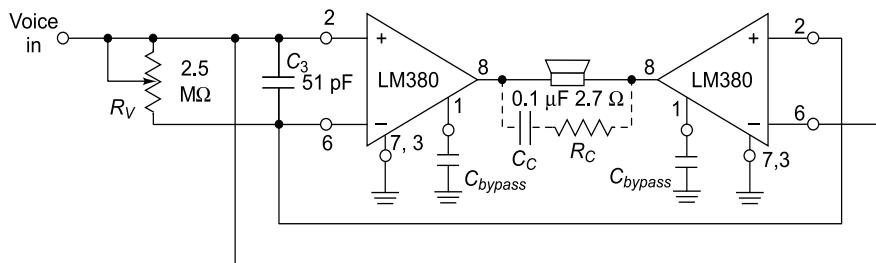
**Intercom system** The IC LM380 can be used for a simple intercom system as shown in Fig. 12.20. Permanent magnetic speakers are used at both ends. Hence they also act as microphones. The master action defines the *talk* and *listen* modes during operation. When the switch *SW* is in *Talk* mode as shown in Fig 12.20, the master speaker acts as *microphone*. The step-up transformer *T* amplifies the signal. When the switch *SW* is in *Listen* mode, the actions of remote and master speakers are interchanged.



**Fig. 12.20** Intercom system using LM380

The overall gain of the circuit in both the modes is the same and the *turns-ratio* of the transformer  $T$  decides the internal gain of the device. The resistor  $R_V$  controls the internal gain of LM380 and provides a common-mode volume control. A maximum gain of 1250 is possible for the circuit, with a device gain of 50 and a transformer turns-ratio of 25.

**Bridge amplifier** When the output power required cannot be supplied by a single audio amplifier, a bridge configuration with the use of two audio amplifiers can be employed as shown in Fig. 12.21. This provides a supply voltage swing of twice that of a single audio amplifier. Therefore, the power capability of the circuit increases by a factor of four compared to an audio amplifier using single IC.



**Fig. 12.21** Bridge Amplifier Circuit using LM380

However, the package power dissipation characteristics impose limitations to the maximum power delivery capacity of the IC. In such cases, the maximum power to the load can be only twice that of a single amplifier.

## 12.7 VIDEO AMPLIFIER

The video or wideband amplifiers are designed to provide a relatively flat *gain versus frequency* response characteristics for the range of frequencies required to transmit video information. The frequency range is generally from 20 Hz to several MHz. The television applications require bandwidths of the order of 4 to 6 MHz. Bandwidths of the order of 50 MHz are also needed for some applications.

The low frequency applications of op-amp demand open-loop voltage gains of the order of 100,000 (100 dB) to 1,000,000 (120 dB). The op-amp is normally operated in a closed-loop configuration, and high open-loop gain is desirable to obtain high closed-loop gain values. This high loop gain provides large input impedance, very small output impedance and it also minimises the gain error.

The high voltage gains are achieved at the cost of reduced frequency response characteristics. In order to stabilise the amplifier against an oscillatory response, the open-loop frequency response is studied from a very low frequency at around 10 Hz. The principal technique that is applied to obtain such large bandwidth is trading-off gain for increased bandwidth. This is accomplished by the use of reduced load resistance for various gain stages of the amplifier. Negative feedback is also employed for the purpose. In many video amplifiers, both the techniques, namely, reduced load resistance and negative feedback are employed simultaneously.

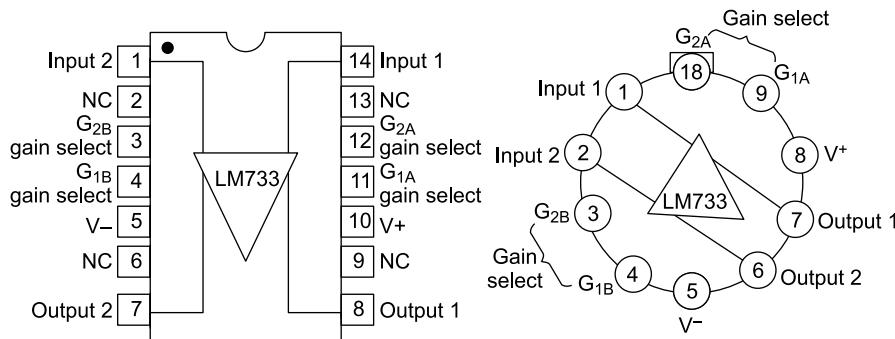
### 12.7.1 Type 733 Video Amplifier

A popular type of IC video amplifier is the type 733(LM733 and  $\mu$ A733). It is a two-stage, differential input, differential output and wideband video amplifier. The use of internal series-shunt feedback gives wide bandwidth with low phase distortion and high gain stability. The emitter-follower outputs provide a high current drive and low impedance. Its 120 MHz bandwidth and selectable gains of 10, 100 and 400, without need for frequency compensation, make it a very useful circuit for memory element drivers, pulse amplifiers and wideband linear gain stages.

The pin diagrams of 14-pin DIP and 10-pin Metal Can packages are shown in Fig. 12.22.

The salient features of the IC are as follows:

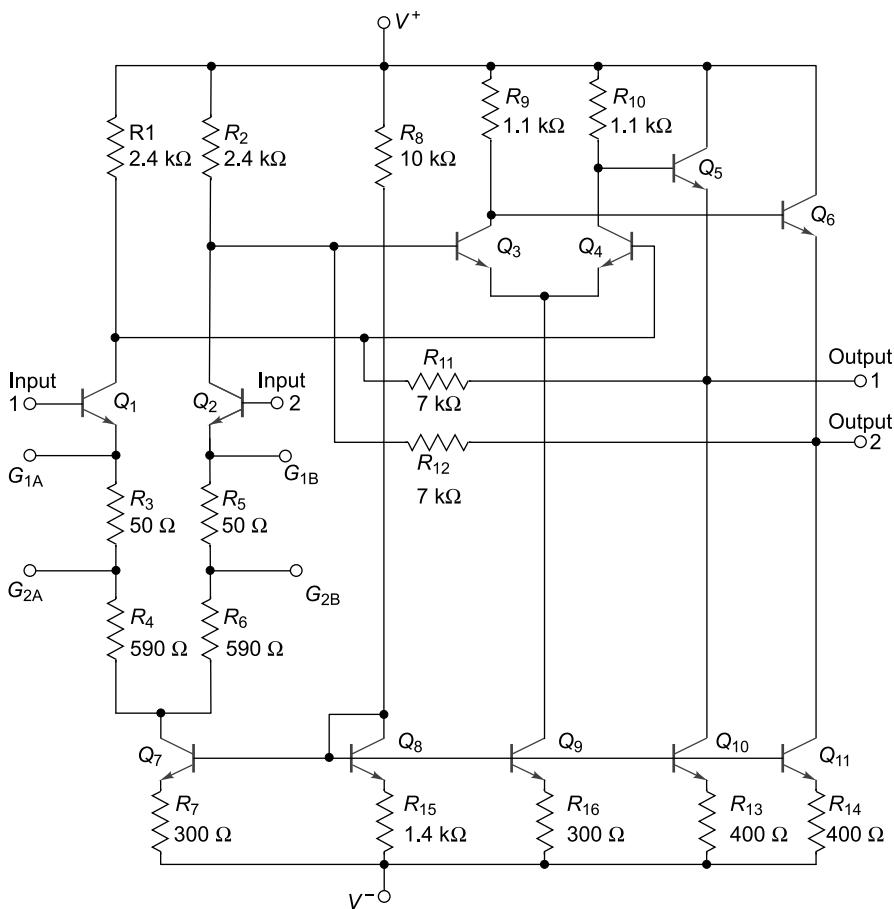
- (i) It has a wide bandwidth of 120 MHz.
- (ii) It offers an input resistance of  $250\text{ k}\Omega$ .
- (iii) Gains of 10, 100 and 400 are selectable.
- (iv) External frequency compensation is not required.
- (v) It provides high common mode rejection ratio at high frequencies.



**Fig. 12.22** Pin diagram of 14-pin DIP and 10-pin Metal Can packages

The Type 733 Video Amplifier finds use in the magnetic tape systems, disk file memories, thin and thick film memories, woven and plated wire memories and wideband video amplifiers.

**Internal circuit diagram and operation** The internal circuit diagram of Type 733 monolithic video amplifier is shown in Fig. 12.23. It consists of two cascaded BJT differential amplifiers and a balanced emitter follower stage. The wide bandwidth is achieved by the use of low value load resistances for the two differential amplifier stages and the use of internal feedback loops. It has a differential input and output. Therefore, both single-ended and balanced input signals may be connected for amplification. Single ended and balanced outputs are also obtainable from the circuit.



**Fig. 12.23** Type 733 monolithic video amplifier

The input stage comprises transistors  $Q_1$ ,  $Q_2$  and the load resistors  $R_1$  and  $R_2$ . The transistor  $Q_7$  provides current-sink biasing for the first differential stage. Resistors  $R_3$  through  $R_6$  provide the *negative feedback* path within the first stage. The second stage formed by  $Q_3$  and  $Q_4$  is driven by the balanced output available from the first stage. Resistors  $R_9$  and  $R_{10}$  act as load resistors for the second differential stage. The transistor  $Q_9$  provides the current-sink bias. The balanced outputs from the second stage drive two emitter follower stages realised by  $Q_5$  and  $Q_6$  respectively.  $Q_{10}$  and  $Q_{11}$  act as current sink bias for the emitter followers.

The resistors  $R_{11}$  and  $R_{12}$  provide the negative feedback from the output terminals to the balanced input terminals of the second stage. The diode-connected transistor  $Q_8$  along with resistors  $R_8$  and  $R_{15}$  provides the overall biasing for the circuit, by driving the current sink biasing transistors  $Q_7$ ,  $Q_9$ ,  $Q_{10}$  and  $Q_{11}$  for all the stages of the amplifiers.

The external gain adjustment for the amplifier can be done by modifying the amount of series feedback connected in the first stage. This is accomplished by externally interconnecting resistor taps ( $G_{1A}$ ,  $G_{1B}$ ) and ( $G_{2A}$ ,  $G_{2B}$ ). Variable gain values can be obtained by connecting variable resistors across the resistor

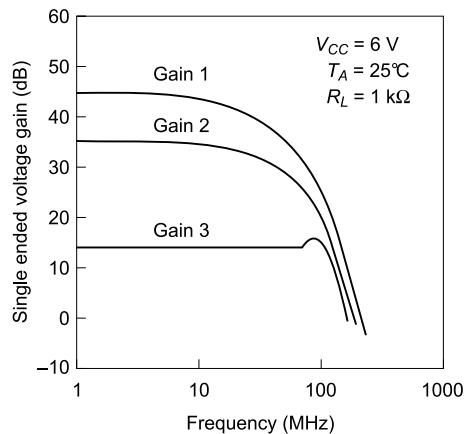
taps. The frequency response characteristics of the video amplifier are shown in Fig. 12.24 for different values of gain for a supply of  $\pm 6$  V.

The IC 733 offers fixed gain values of 400, 100 and 10 for bandwidths of 40 MHz, 90 MHz and 120 MHz respectively.

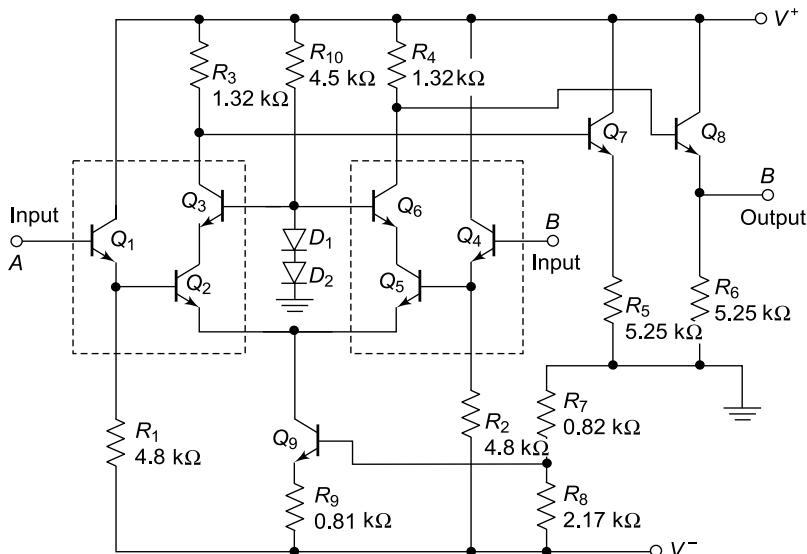
The wideband amplifier HA-2539 is available from Harris semiconductor. It has a gain-bandwidth value of 600 MHz, and a full power bandwidth of 9.5 MHz while driving a  $1000\ \Omega$  load with 20 V peak-to-peak voltage swing.

### 12.7.2 Type 3040 Video Amplifier

The monolithic video amplifier IC 3040 from RCA uses a differential cascode configuration in the input stage. The internal circuit diagram is shown in Fig. 12.25. The input stage is formed by CC-CE/Cascode compound connection of transistors  $Q_1$ ,  $Q_2$  and  $Q_3$  operated in common-collector, common-emitter and common-base configurations respectively. This compound configuration is in turn connected to a symmetrical configuration consisting of transistors  $Q_4$ ,  $Q_5$  and  $Q_6$ . These compound transistor structures are shown within the dotted lines. The common collector or emitter follower stages formed by transistor  $Q_7$  and  $Q_8$  provide a low impedance differential output from the circuit.



**Fig. 12.24** Frequency response characteristics



**Fig. 12.25** RCA3040 monolithic video amplifier

The IC 3040 can accept single ended or balanced input signals. Single ended or balanced output voltages can be obtained at the output. The transistor  $Q_9$  provides current sink-biasing for the differential

stage. The resistors  $R_3$  and  $R_4$ , act as load resistors for this differential stage. The resistors  $R_5$  and  $R_6$  bias the emitter follower transistors  $Q_7$  and  $Q_8$ . The diodes  $D_1$  and  $D_2$  with the resistor  $R_{10}$  provide a dc bias voltage for the transistors  $Q_2$ ,  $Q_3$ ,  $Q_5$  and  $Q_6$ . The bias voltage for the current sink transistor  $Q_9$  is applied by the voltage divider using the resistors  $R_7$  and  $R_8$ . Hence the collector current (quiescent current) of  $Q_9$  is determined by the bias voltage and resistor  $R_9$ .

The overall mid-frequency voltage gain of the IC 3040 is around 110, which is obtained with a balanced output voltage. When a single ended input or a balanced input is applied, the input will be split evenly between the two halves of the circuit. Therefore, the voltage applied to each half of the circuit is  $V_i/2$  and the corresponding output is  $V_o/2$ . A full swing output voltage of  $V_o$  can be obtained by taking a balanced output and an output of  $V_o/2$  can be taken from a single ended output with a corresponding gain of 55.

The IC 3040 exhibits very large gain-bandwidth product due to its cascode gain stage and emitter-follower input and output stages. The typical 3 dB bandwidth for the video amplifier CA3040 is 55 MHz.

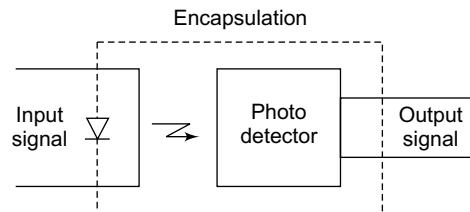
## 12.8 OPTO-COUPLES

An opto-coupler is a solid state component in which the light emitter, the light path and the light detector are all enclosed within the component and cannot be changed from outside. As the opto-coupler provides electrical isolation between two circuits, it is also called an *opto-isolator*. An opto-isolator allows signal transfer without the use of coupling wires, capacitors or transformers. It can couple digital (logic 1 or 0) or analog (continuously variable) signals.

The schematic representation of an opto-coupler is shown in Fig. 12.26. An opto-coupler, also called an opto-electronic coupler, generally consists of an infrared LED and a photo-detector such as PIN photo diode for fast switching, photo transistor Darlington pair, or photo-SCR combined in a single package. Opto-isolators transduce input voltage to a proportional light intensity by using LEDs. The light is transduced back to output voltage using light sensitive devices. GaAs LEDs are used to provide spectral matching with the silicon sensors.

The wavelength response of each device is made to be as identical as possible to permit the highest possible measure of coupling. There is a transparent insulating cap between each set of elements embedded in the structure to permit efficient passage of light. They are designed with very small response time such that they can be used to transmit data in MHz range of frequencies.

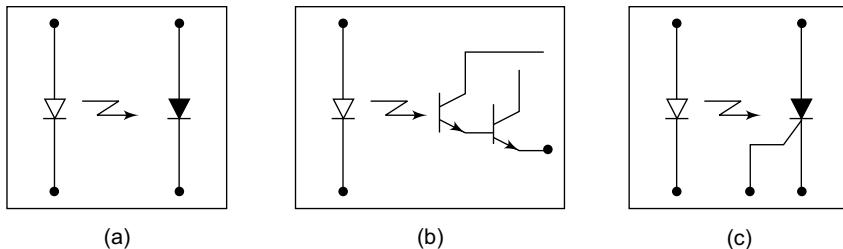
The rigid structure of this package permits one-way transfer of electrical signal from the LED to the photo-detector, without any electrical connection between the input and output circuitry. The extent of isolation between the input and output depends on the kind of material in the light path and on the distance between the light emitter and light detector. A significant advantage of the opto-isolator is its high isolation resistance, of the order of  $10^{11} \Omega$ , with the isolation voltages up to 2500 V achievable between the input and output signals. This feature allows it to be used as an interface between high voltage and low voltage systems. Application of this device includes the interfacing of different types of logic circuits and their use in *level-and-position-sensing* circuits.



**Fig. 12.26** Schematic representation of opto-coupler

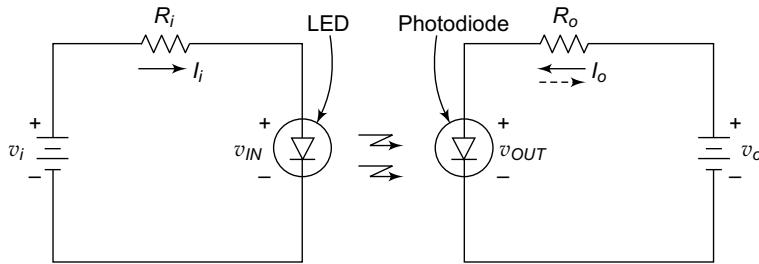
In an opto-isolator, the power dissipations of LED and phototransistor are almost equal and  $I_{CEO}$  is measured in nano-amperes. The relative output current is almost constant when the case temperature varies from 25 to 75°C. The  $V_{CE}$  voltage of the photo transistor affects the resulting collector current only very slightly. The switching time of opto-isolator decreases with increased current, and for some devices it is exactly the reverse.

The schematic diagrams of the opto-couplers using a photodiode, photo Darlington pair and photo-SCR are illustrated in Fig. 12.27.



**Fig. 12.27** Schematic representation of opto-couplers using (a) Photodiode, (b) Photo-Darlington pair, and (c) Photo-SCR

Figure 12.28 shows the basic circuit arrangement for the use of an opto-coupler. The source  $v_i$  and series resistor  $R_i$  determine the forward current  $I_i$  through the LED. Therefore, the light emitted from the LED depends on the signal  $v_i$ . This light incident on the photo diode generates a reverse current in the output circuit through the resistor  $R_o$ . Therefore the drop across the resistor  $R_o$  is proportional to the input voltage, and it varies proportionately with change in input signal source.



**Fig. 12.28** Basic circuit arrangement for the use of opto-coupler

### 12.8.1 Characteristics of Opto-Couplers

The important characteristics of an opto-coupler are given below:

**Collector-emitter voltage** This is the maximum voltage that can be applied across collector and emitter of the receiving phototransistor (*no light* when it is turned OFF) before it may break-down.

**Creepage distance** This is physically a measure of how far a spark would have to travel around the outer side of the package to get from one side to the other. If the package has contaminants on it

such as solder flux, or dampness, then a lower-resistance path will be created for noise signals to travel along the surface.

**Forward current** This is the current passing through the transmitting LED. Typically an opto-isolator will require about 5 mA to turn the output transistor ON.

**Forward voltage** This is the voltage that is dropped across the LED when it is turned ON by the input signal  $v_i$ . The LEDs drop typically 1 to 2 Volts, whereas the silicon diodes drop about 0.7 V.

**Collector dark current** This is the current that can flow through the output photo transistor when it is turned OFF.

**Collector-emitter saturation voltage** This is the voltage available between the collector and emitter when the output transistor is fully turned ON (saturated).

**Isolation resistance** This is the resistance from a pin on the input side to a pin on the output side. It must be very high to offer good isolation between the input and output sides of opto-coupler.

**Response time** The rise and fall times are the time durations that the output voltage requires to rise from zero to maximum and to fall from maximum to zero respectively. The rise time is dependent on the load resistor. Therefore, this value is always quoted for a fixed load resistor.

When the opto-couplers are used with pulse-width modulated (PWM) signals for applications such as speed control of motors, the response time of the opto-coupler, and the rise and fall time of the signals are the criteria for the selection of the opto-couplers.

**Cut-off frequency** This is effectively the highest frequency of square-wave that can be applied to the opto-isolator. It is actually the frequency at which the output voltage becomes half the maximum amplitude. This determines the operating bandwidth of the opto-coupler and it is related to the rise and fall times.

**Current transfer ratio** The input current is the forward current of LED that generates the emission of light, which is detected by photo diode, photo Darlington or photo-SCR to produce the output current. The ratio of output current  $I_o$  to the input current  $I_i$  is called the *current transfer ratio* (CTR). The different CTR ratings of the opto-couplers are shown in Table 12.1. This factor also depends on the proximity between LED and photo transistor and their efficiencies.

**Table 12.1** Current transfer ratios of opto-couplers

<b>Device</b>	<b>Current Transfer Ratio</b>
LED-Photo diode	0.01 – 0.03
LED-Transistor	0. – 1
LED-Darlington	1 – 5
IRED-Transistor	10 – 15
GaAs IRED-Transistor	100 – 2000

## 12.8.2 Opto-Coupler ICs

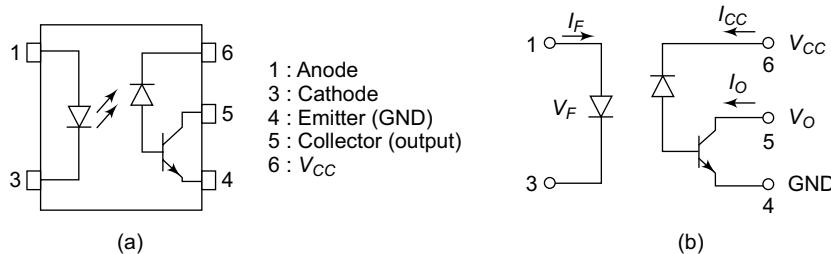
The opto-coupler ICs are available in a variety of packages, with the most common being the six-pin mini DIP.

**TLP112 opto-coupler** The Type TLP112 from Toshiba is a mini-Flat coupler, which is suitable for surface mount assembly. It consists of a GaAlAs light emitting diode, optically coupled to a high speed detector of a single-chip photodiode-transistor assembly.

The important features are:

- (i) An isolation voltage of 2500V rms (min) can be achieved
- (ii) Switching speeds of  $t_{pHL} = 0.8 \mu s$ ,  $t_{pLH} = 2 \mu s$ (max) is possible
- (iii) It is TTL compatible

The pin configuration and the input-output terminals are shown in Fig. 12.29(a) and (b) respectively.

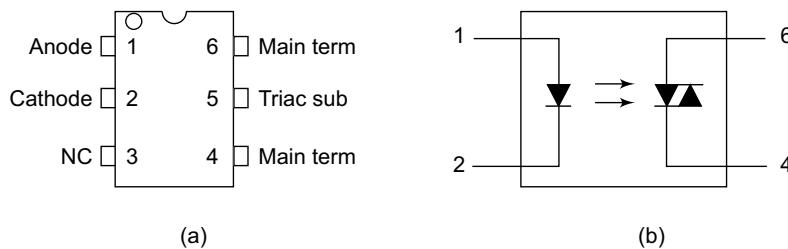


**Fig. 12.29** TLP112 Opto-coupler: (a) Pin configuration (b) Input-output terminals

**MOC3009-MOC3012 series opto-couplers** The MOC3009 series opto-couplers consist of Gallium-Arsenide-Diode Infrared source and an optically coupled silicon Triac driver. It can provide 250 V driver output, with an electrical isolation of 7500 V peak. The IC is available in standard 6-pin Plastic DIP as shown in Fig. 12.30. It is directly interchangeable with MOC3009, MOC3010, MOC3011 and MOC3012.

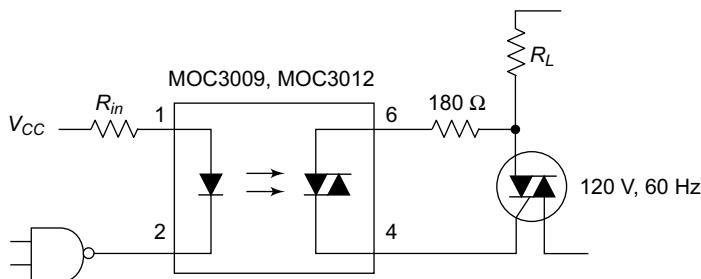
The typical applications are Solenoid/Valve controls, Lamp ballasts, Interfacing microprocessors to 115 V ac peripherals, Motor controls and Incandescent lamp dimmers.

The pin configuration and the logic diagram of the MOC3009-MOC3012 Series ICs are shown in Figs. 12.30(a) and (b) respectively.

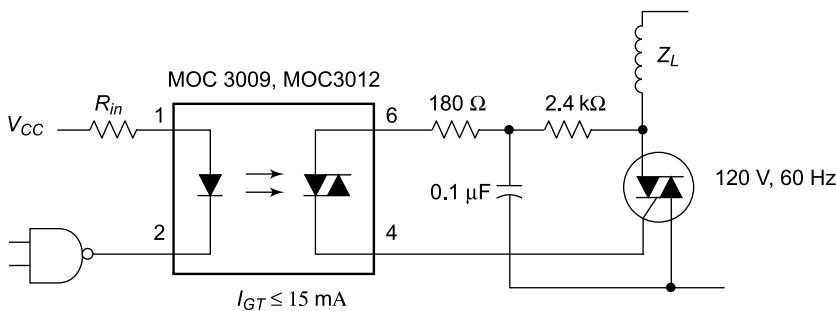


**Fig. 12.30** MOC3009-MOC3012 Series Opto-couplers:  
(a) Pin configuration (b) Logic diagram

The typical application circuits for resistive load and inductive load using MOC3009 are shown in Figs. 12.31(a) and (b) respectively.



**Fig. 12.31 (a)** Use of MOC3009 for resistive load



**Fig. 12.31 (b)** Use of MOC3009 for inductive load

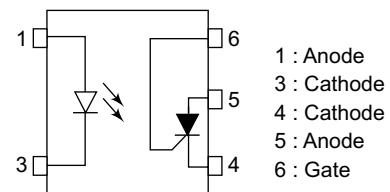
**TLP141G Opto-coupler** The Type TLP141G from Toshiba is a mini-Flat opto-coupler, which is suitable for surface mount assembly. It consists of a GaAs Infra Red Emitting Diode (IRED), optically coupled to a high-speed detector of photo-thyristor.

The important features of this opto-coupler are as follows:

- (i) Peak off-state voltage : 400 V (min.)
- (ii) Trigger LED current : 10 mA (max.)
- (iii) On-state current : 150 mA (max.) and
- (iv) Isolation voltage : 2500 V rms (min.)

Its main applications are programmable controllers, ac output module and solid state relay.

Its pin configuration and terminals are shown in Fig. 12.32.



**Fig. 12.32** TLP141G Opto-coupler Pin Configuration

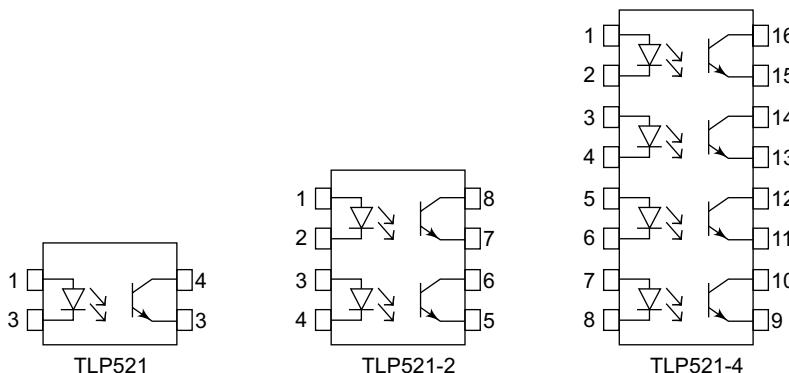
**TLP521, TLP521-2, TLP521-4 series of opto-couplers** The TLP521, TLP521-2, TLP521-4 series of opto-couplers consist of infrared light emitting diodes and NPN silicon photo transistors in space efficient dual in line plastic packages.

The important features of these series of opto-couplers are:

- (i) It has a high current transfer ratio, with a minimum obtainable value of 50%.
- (ii) High isolation voltages of 5.3 kV<sub>RMS</sub> and 7.5 kV<sub>peak</sub> are achievable
- (iii) It has a high BV<sub>CEO</sub>, with a minimum value of 55 V

The main applications of opto-couplers are computer terminals, industrial system controllers, measuring instruments and signal transmission between systems of different potentials and impedances.

The package details and the internal component details are shown in Fig. 12.33.



**Fig. 12.33** TLP521, TLP521-2, TLP521-4 Series of Opto-couplers

The main advantages of opto-couplers are:

- (i) The electrical isolation achieved between input and output is of the order of several Mega Ohms. This characteristic makes the device useful in high voltage applications where the voltages between the input and output are several thousand Volts.
- (ii) The response time of opto-couplers is so small that they can be used for data applications involving Mega Hertz range of pulse frequencies.
- (iii) They are capable of wideband signal transmission.
- (iv) Easy interfacing with logic devices is possible.
- (v) They are compact and portable.
- (vi) They are more efficient than isolation transformers and relays.
- (vii) The problems such as noise, transients and contact bounce etc. are completely eliminated.

## 12.9 ISOLATION AMPLIFIER

The isolation amplifier is an amplifier in which, there is no physical contact between the input and output sections. These amplifiers are used in applications requiring very large common-mode voltage difference between the input and output sections. Several thousand Volts can exist between the two sections while using such isolation amplifiers. Signal transmission (across the isolation barrier) is accomplished through an optical coupler, which acts as a 1:1 current translator. Current at the input of the device is replicated on the output side of the coupler. The isolated output current ( $I_o$ ) is forced to flow through RF by the summing node action of the output op-amp.

They find use in medical instrumentation applications, where the patient must be isolated and protected from leakage currents. Most of the isolation amplifiers are hybrid ICs and consist of an input amplifier, a GaAs Light-Emitting Diode (LED), a silicon photo diode and an output amplifier. The input signal modulates the light output of the LED. The light emitted by the LED is detected by the photo-diode and converted to an electrical signal.

One of the main requirements of an isolation amplifier is its linearity of input-output characteristics. The inherent nonlinear current-input to light-output characteristics of the LED is the cause of the nonlinearity of

isolation amplifier. Various opto-electronic devices and their circuits are being devised to obtain high degree of linearity in optically coupled analog signal transmission systems. Typical isolation amplifier chips are ISO100, 3450-3455 series from Burr-Brown, and AD293 and AD294 from Analog Devices.

### 12.9.1 IC ISO100 Isolation Amplifier

The IC ISO100 is an optically coupled isolation amplifier. It offers high accuracy, linearity and good stability against time and temperature. This is achieved by coupling light from an LED back to the input with negative feedback as well as forwarding the output. It needs careful directional matching of optical components.

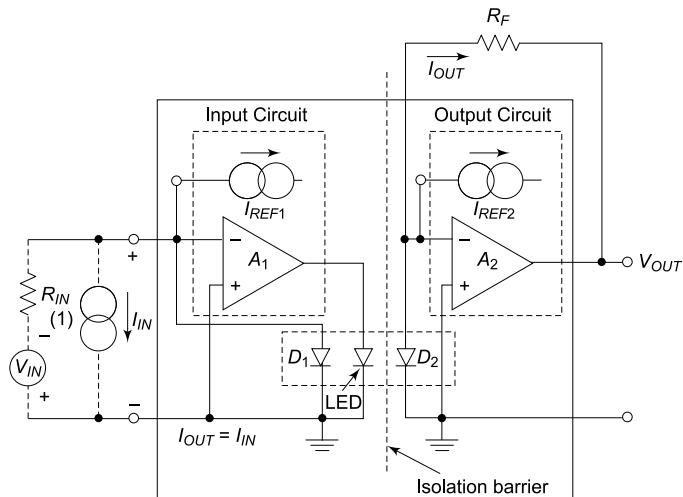
The main features of the isolation amplifier ISO100 are as follows:

Supply voltage	:	$\pm 18$ V
Isolation voltage	:	ac peak or dc 750 V
Input current	:	$\pm 1$ mA
Storage temperature range	:	-40°C to 100°C
Soldering lead temperature	:	+300°C
Output short-circuit duration	:	Continuous to ground
Leakage	:	0.3 $\mu$ A (max) at 240 V/60 Hz
Bandwidth	:	60 kHz
18-pin DIP package	:	

**Operation of ISO100** The ISO100 has several modes of operation, namely, unipolar or bipolar, voltage or current input, and inverting or non-inverting. Figure 12.34(a) and (b) show the simplified block diagram and pin diagram of ISO100. It can be considered as a unity gain current amplifier. Its output flows into a current-to-voltage converter. Hence, it is inherently a current input device. An isolation barrier exists between the input and output circuits of the IC. Therefore, signal transmission across the barrier is accomplished through an optical coupler. The current at the input of the device is replicated as  $I_{OUT}$  at the output side of the device. This output current  $I_{OUT}$  is forced to flow

through the feedback resistor  $R_F$ . This is achieved by the action of the summing node of the output op-amp. The non-inverting input of the IC ISO100 is connected to the inverting input of the op-amp  $A_1$ . The two stages of inversion for the input signal compensate each other, thus producing a true output signal.

The transfer function of the IC ISO100 is given by  $\frac{V_{OUT}}{V_{IN}} = \frac{R_F}{1 + A_{GE}}$  where  $A_{GE}$  is the gain error. It is defined as the deviation of the ratio,  $\frac{I_{IN}}{I_{OUT}}$  from unity. It can thus be considered as the *coupling error*.



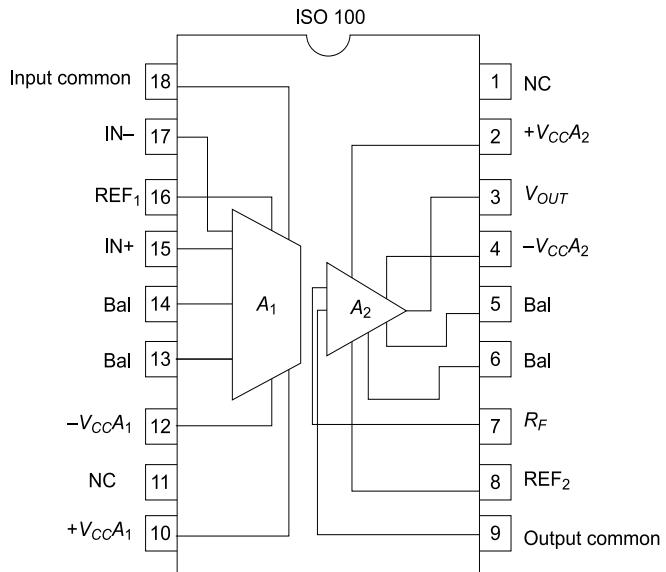
Note : (1) A negative input signal is required in the unipolar mode

**Fig. 12.34 (a) Block diagram of ISO100 Iso-amplifier**

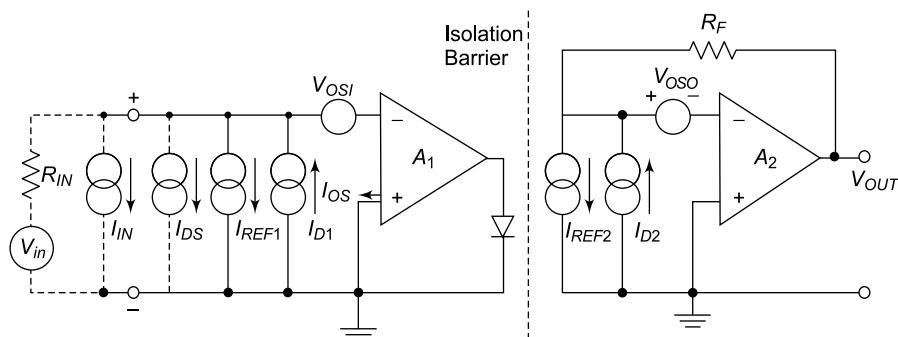
The optical coupler shown in Fig. 12.34(a) consists of a matched pair of photo diodes and an LED. This makes the signal transmission possible from input to output. The diode  $D_1$  forms negative feedback path in combination with LED. The diode  $D_2$  receives the optical signal across the isolation barrier.

The basic mode of operation is unipolar due to the use of LED and in such unipolar modes, only negative input currents are allowed. Bipolar operation is achieved by internally offsetting the input from its zero value. The two matched current sources  $I_{REF1}$  and  $I_{REF2}$  are used for this purpose. Connecting the current source  $I_{REF1}$  on the input side of the coupler makes the amplifier operate at mid-scale, and connecting an equal current source  $I_{REF2}$  on the output side shifts the output voltage level back to zero. This allows passing input current of either polarity to the IC.

The dc Error model used to represent ISO100 is shown in Fig. 12.35. The element  $I_{OS}$  is called the offset current. It is defined as the input current required for making the output voltage zero. In unipolar mode of operation,  $I_{OS}$  indicates the mismatches in the optical paths. In bipolar operation, it shows the mismatch between  $I_{REF1}$  and  $I_{REF2}$ . The  $I_{OS}$  is sensitive to temperature, supply voltage, common mode voltage and ISO mode voltage. The voltages  $V_{OSI}$  and  $V_{OSO}$  model the voltage-offsets at the inputs of each op-amp.  $I_{D1}$  and  $I_{D2}$  represent the current generated by the photo-diodes  $D_1$  and  $D_2$  respectively.



**Fig. 12.34 (b)** Pin configuration of ISO100 Iso-amplifier



**Fig. 12.35** dc Error model of ISO100

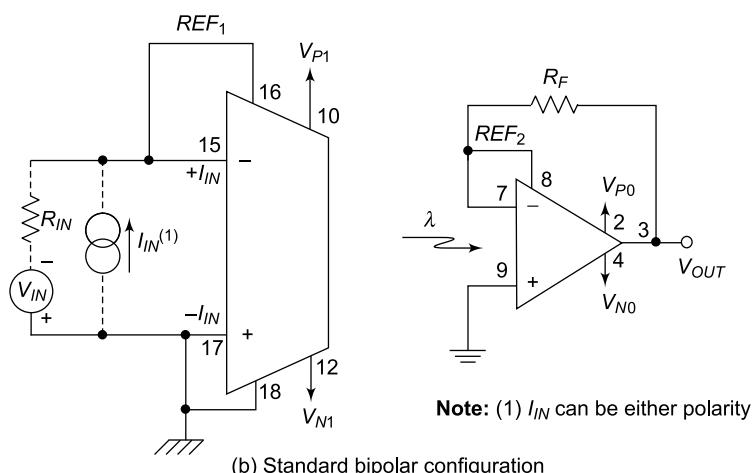
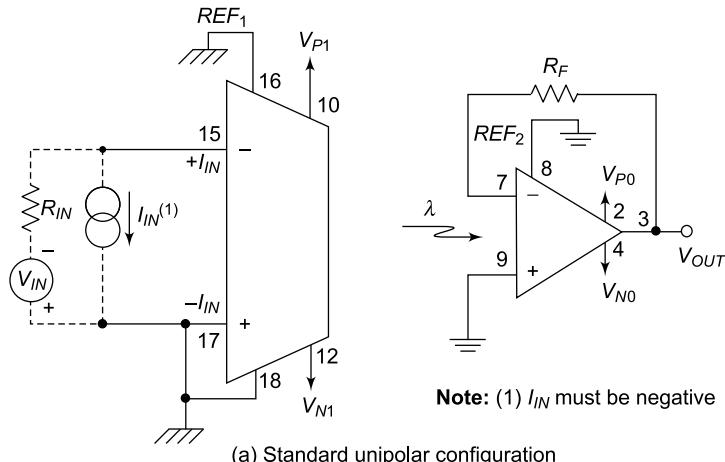
The two currents  $I_{D1}$  and  $I_{D2}$  are related as  $I_{D2} = I_{D1}(1 + A_{GE})$  where  $A_{GE}$  is the gain error. The transfer function for the voltage mode is

$$V_o = R_F \left[ \left( \frac{V_{IN}}{R_{IN}} + \frac{V_{OS1}}{R_{IN}} - I_{REF1} + I_{OS} \right) (1 + A_{GE}) + I_{REF2} \right] + V_{OSO}$$

The transfer function equation for the input current is

$$V_o = R_F [I_{IN} - I_{REF1} + I_{OS}] (1 + A_E)$$

Figures 12.36(a) and (b) show the standard configurations of use for ISO100. Figure 12.36(a) shows the arrangement for unipolar operation. This mode functions for negative inputs only as shown. Figure 12.36(b) shows the use of internal references to provide bipolar operation. It is to be noted that the power supply connections  $V_{P1}$ ,  $V_{N1}$ ,  $V_{P0}$  and  $V_{N0}$  to the input and output stages are isolated.



**Fig. 12.36** Standard configurations

## 12.9.2 Application Information

The advantages of ISO100 are its small size, low offset, low drift, wide bandwidth, ultra low leakage and low leakage. The precautions to be observed while designing the ISO are as follows:

- (i) Input common and IN lines at Pins 17 and 18 must be grounded through separate lines. This is to avoid any large *dc* current flowing in input common feedback to signal input.
- (ii) Shielded or twisted pair cables are preferred at the input for long lines.
- (iii) The external capacitance across the isolation barrier is to be minimised.
- (iv) Leakage and arcing are to be avoided. This can be done by spacing the isolation barrier, external components and conductor patterns far apart.
- (v) The current  $I_1$  should be greater than 200A to keep internal LED ON.
- (vi) The maximum output voltage swing is determined by  $I_1$  and  $R_F$

$$V_{swing} = I_{1(MAX)} \times R_F$$

## 12.9.3 AD293 and AD294 Isolation Amplifiers

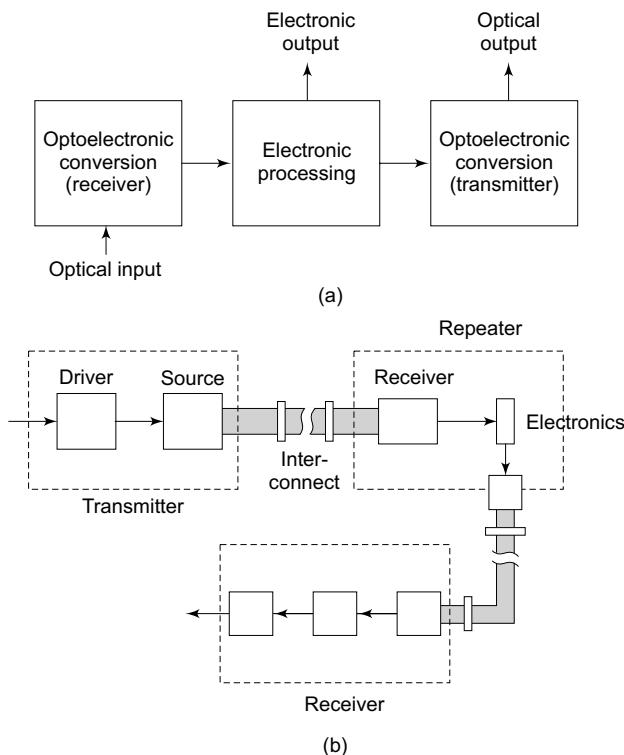
These are transformer coupled hybrid isolation amplifiers. They consist of dc-dc converter to supply dc power to the input section. The common mode voltage is 2500 V peak for the AD293 device and 8000 V peak for the AD294 device. Therefore these ICs are suitable for medical instrumentation applications. They also have high degree of linearity with a non-linearity of 0.05% at a maximum. This is made possible with the use of the negative feedback of the input amplifier. The feedback voltage is provided by a feedback winding available in the transformer. The CMRR obtainable in these ICs is 115 dB and the small-signal bandwidth is 2.5 kHz for a gain in the range of 1 to 100.

## 12.10 FIBRE-OPTIC INTEGRATED CIRCUITS

Opto-electronics and opto-electronic devices have undergone tremendous progress in recent years. Optics provides the advantages of large bandwidth, parallelism and reconfigurable characteristics. Electronic devices provide active components in information handling systems. Thus opto-electronic integrated circuits involve the integration of electronic and optical components, and optical interconnects. The fibre forms an optical interconnect medium. Such an interconnect medium provides a large bandwidth, high-speed data transmission, and immunity against mutual interference and cross-talk. They are unaffected by capacitive loading effects also. It results in size reduction, reduced power of system and increased fan-out capability.

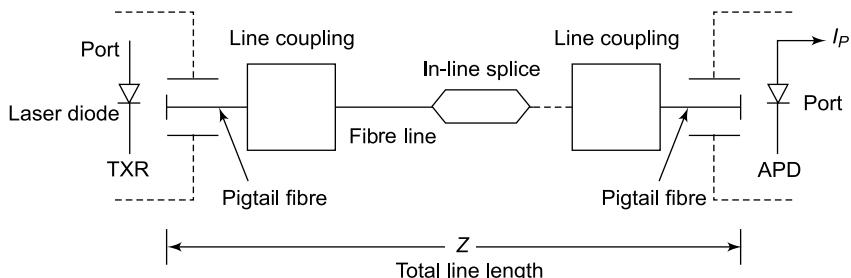
Figure 12.37(a) shows the block diagram of an Opto-Electronic Integrated Circuit (OEIC). It combines the functions of optical detection, electronic functions such as switching and amplification and light transmission.

Figure 12.37(b) shows the essential elements and major components of a two-link fibre-optic communication facility. The transmitting end consists of an optical transmitter such as an LED or a laser diode source with driver, coupled to the fibre. The LED or laser diode turns ON and OFF according to the bit stream to be sent. The repeaters receive the signal from first link. The signal is amplified, reshaped, retimed and then retransmitted to the next link. The repeater consists of an avalanche photo-diode, or PIN diode, which senses the attenuated and dispersed train of light pulses. Then the pulses are processed before being sent to the second link. The receiver at the receiving end converts the incoming light pulses to electrical pulses. The electrical pulses are regenerated and distributed.



**Fig. 12.37** (a) Block diagram of Opto-Electronic-Integrated Circuit (OEIC)  
(b) Major components of a fibre-optic communication facility

In a fibre-optic link, the total loss suffered by the fibre and all the connectors and splices along the length of the fibre optic communication path must not exceed a certain minimum value. The minimum acceptable received optical power  $P_r$  is dependent on the type of detector and allowable error rate. Assume a total light flux of power  $P_t$  is emitted from the optical source as shown in Fig. 12.38. Only part of the light is sent through the fibre, due to the inefficiency of coupling the diode to fibre end. This results in a part loss of  $L_{pt}$ . Similarly, the connector on the other end of the fibre introduces an insertion loss of  $L_C$ . The light passing through the fibre encounters losses due to absorption and leakage, which can be considered as  $ZL_f$  where  $L_f$  is the rate of loss and  $Z$  is the length of the fibre. The splice loss of  $L_S$  for each of  $N_S$  splices is also introduced.



**Fig. 12.38** Elements in the fibre-optic link

At the receiving end, the digital line connector shown feeds the light from the fibre into the avalanche photo diode. This introduces a second part loss  $L_{pr}$  and a second connector loss  $L_C$ . The *loss budget* for the communication link is then,

$$P_t - P_r = M + L_{pt} + L_{pr} + N_C L_C + N_S L_S + ZL_f$$

Therefore, the maximum length of link  $Z$  is determined and limited by the losses.

### 12.10.1 MAX 3738 Laser Driver IC

The MAX3738 laser driver IC is available in a  $4 \text{ mm} \times 4 \text{ mm}$ , 24 pin thin QFN package, and it can be operated over a range of  $-40^\circ\text{C}$  to  $185^\circ\text{C}$  temperature range. The pin diagram of this laser driver IC is shown in Fig. 12.39.

Its key features are as follows:

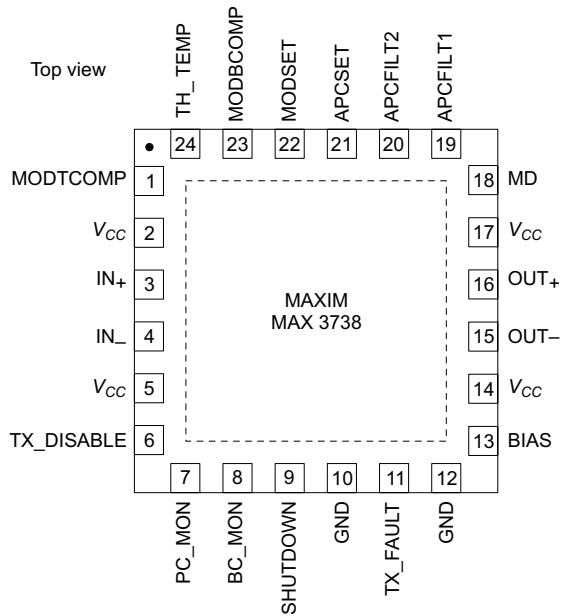
- (i) Single  $+3.3 \text{ V}$  power supply
- (ii)  $47 \text{ mA}$  power supply current
- (iii)  $85 \text{ mA}$  modulation current
- (iv)  $100 \text{ mA}$  Bias Current
- (v) Automatic Power Control (APC)
- (vi) Modulation compensation
- (vii) On-chip temperature compensation
- (viii) Self-biased inputs for ac-coupling
- (ix) Ground-referenced current monitoring
- (x) Laser shutdown and alarm outputs
- (xi) Enable control and laser safety feature

The typical applications of MAX3738 laser driver are:

- (i)  $1 \text{ Gbps}/2 \text{ Gbps}$  fibre channel SFF/SFP and GBIC transceivers
- (ii) Gigabit Ethernet SFF/SFP and transceiver modules and
- (iii) Multirate OC-24 to OC-48 FEC transceivers

The MAX3738 is a laser driver designed for multirate transceiver modules. The IC can work for data ranges from  $1 \text{ Gbps}$  to  $2.7 \text{ Gbps}$ . The lasers are dc-coupled to the IC for reducing the component count. It also helps in multirate operation. Laser extinction control (ERC) is provided in the IC. This combines the features of automatic power control (APC) and modulation compensation. It also has built-in thermal compensation. The APC loop helps to maintain the average optical power constant. Modulation compensation enhances the modulation current in proportion to the bias current. These control loops maintain a constant optical extinction ratio over temperature ranges and extended lifetime.

The MAX3738 accepts differential input signals also. The modulation current range can be from  $5 \text{ mA}$  to  $60 \text{ mA}$  (up to  $85 \text{ mA}$  when ac-coupled). This makes the MAX3738 an ideal driver for driving FP/DFB lasers in fibre optic modules. The external resistor set the required current levels for laser. Transmit disable control (TX-DISABLE) single-point fault tolerance bias current monitoring and photo current monitoring features are also provided.



**Fig. 12.39** Pin diagram of MAX3738 Laser Driver

## 12.11 ELECTRICAL CHARACTERISTICS

The typical values are  $V_{CC} = +2.97$  V to  $+3.63$  V and  $TA = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ . The default conditions assumed in the Table 12.2 are  $V_{CC} = +3.3$  V,  $I_{BIAS} = 60$  mA,  $I_{MOD} = 60$  mA,  $TA = +25^\circ\text{C}$ .

**Table 12.2**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Power Supply</b>						
Supply Current	$I_{CC}$		47	60		mA
Power-Supply Noise Rejection	PSNR	$f \leq 1\text{Hz}$ , 100 mA <sub>P-P</sub>	33			dB
<b>I/O Specifications</b>						
Differential Input Swing	$V_{ID}$		0.2	2.4		VP-P
Common-Mode Input	$V_{CM}$		1.7		$V_{CC}$ $V_{ID}/4$	V
<b>Laser Bias</b>						
Bias-Current-Setting Range			1	100		mA
Bias Off Current		TX_DISABLE = high		0.1		mA
Bias-Current Monitor Ratio		$I_{BIAS}/I_{BC\_MON}$	62	76	90	mA/mA
<b>Laser Modulation</b>						
Modulation Current-Setting Range	$I_{MOD}$		5	85		mA
Output Edge Speed		20% to 80%	$5 \text{ mA} \leq I_{MOD} \leq 85 \text{ mA}$	65	80	ps
Output Overshoot/Undershoot				$\pm 6$		%
Random Jitter				0.62	1.3	psRMS
Deterministic Jitter		2.7 Gbps, $5 \text{ mA} \leq I_{MOD} \leq 85 \text{ mA}$		18	40	psP-P
		1.25 Gbps, $5 \text{ mA} \leq I_{MOD} \leq 85 \text{ mA}$		20	41	
		622 Mbps, $5 \text{ mA} \leq I_{MOD} \leq 85 \text{ mA}$		24	46	
		155 Mbps, $5 \text{ mA} \leq I_{MOD} \leq 85 \text{ mA}$		45	100	
Modulation-Current Temperature Stability			$5 \text{ mA} \leq I_{MOD} \leq 10 \text{ mA}$	$\pm 175$	$\pm 600$	ppm/ $^\circ\text{C}$
			$10 \text{ mA} \leq I_{MOD} \leq 85 \text{ mA}$	$\pm 125$	$\pm 480$	
Modulation-Current-Setting Error		15_ load, $TA = +25^\circ\text{C}$	$5 \text{ mA} \leq I_{MOD} \leq 10 \text{ mA}$		$\pm 20$	%
			$10 \text{ mA} < I_{MOD} \leq 85 \text{ mA}$		$\pm 15$	
Modulation Off Current		TX_DISABLE = high		0.1		mA

Ref: Maxim IC MX3738 datasheet

Table 12.3 indicates the parameters related to various monitor and control features of IC MAX3738.

**Table 12.3**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Automatic Power and Extinction Ratio Controls</b>						
Monitor-Diode Input Current Range	$I_{MD}$	Average current into the MD pin	18	1500		$\mu A$
MD Pin Voltage				1.4		V
MD Current Monitor Ratio		$I_{MD}/I_{PC\_MON}$	0.85	0.93	1.15	$mA/mA$
APC Loop Time Constant		$C_{APC\_FILT} = 0.01 \mu F, \Delta I_{MD}/\Delta I_{BIAS} = 1/70$		3.3		$\mu s$
APC Setting Stability				$\pm 100$	$\pm 480$	ppm/ $^{\circ}C$
APC Setting Accuracy		$TA = +25^{\circ}C$			$\pm 15$	%
$I_{MOD}$ Compensation-Setting Range by Bias	$K$	$K = \Delta I_{MOD}/\Delta I_{BIAS}$	0	1.5		$mA/mA$
$I_{MOD}$ Compensation-Setting Range by Temperature	$TC$	$TC = \Delta I_{MOD}/\Delta T$	0	1.0		$mA/{}^{\circ}C$
Threshold-Setting Range for Temperature Compensation	$T_{TH}$		+10	+60		${}^{\circ}C$
<b>Laser Safety and Control</b>						
Bias and Modulation Turn-Off Delay		$C_{APC\_FILT} = 0.01 \mu F, \Delta I_{MD}/\Delta I_{BIAS} = 1/80$		5		$\mu s$
Bias and Modulation Turn-On Delay		$C_{APC\_FILT} = 0.01 \mu F, \Delta I_{MD}/\Delta I_{BIAS} = 1/80$		600		$\mu s$
Threshold Voltage at Monitor	$V_{REF}$		1.14	1.3	1.39	V
<b>Interface Signals</b>						
TX_DISABLE Input High	$V_{HI}$		2.0			V
TX_DISABLE Input Low	$V_{LO}$	$R_{PULL} = 45 k\Omega$ (typ)		0.8		V
TX_DISABLE Input Current		$V_{HI} = V_{CC}$		15		$\mu A$
		$V_{LO} = V_{GND}$		-70		
TX_FAULT Output Low		Sinking 1 mA, open collector		0.4		V
Shutdown Output High		Sourcing 100 $\mu A$	$V_{CC} - 0.4$			V
Shutdown Output Low		Sinking 100 $\mu A$		0.4		V

Ref: Maxim IC MX3738 datasheet

### 12.11.1 Pin Description of IC MAX3738

Table 12.4 shows the pin description of the laser-driver IC.

**Table 12.4** *Pin description of IC MAX3738*

Pin	Name	Function
1	MODTCOMP	Modulation-Current Compensation from Temperature. A resistor connected at this pin is used to set the temperature coefficient of the modulation current when it is above the threshold temperature. The terminal can be left open if zero temperature compensation is preferred.
2, 5, 14, 17	$V_{CC}$	+3.3 V Supply Voltage connection
3	IN+	Non-inverted Data Input
4	IN-	Inverted Data Input
6	TX_DISABLE	Transmitter Disable. The laser output is enabled when this pin is asserted low.
7	PC_MON	Photodiode-Current Monitor Output. The current out of this pin develops a ground-referenced voltage across an external resistor that is proportional to the monitor diode current.
8	BC_MON	Bias-Current Monitor Output. Current out of this pin develops a ground-referenced voltage across an external resistor that is proportional to the bias current.
9	SHUTDOWN	Shutdown Driver Output. Voltage output to control an external transistor for optional shutdown circuitry.
10, 12	GND	Ground
11	TX_FAULT	Open-Collector Transmit Fault Indicator
13	BIAS	Laser Bias-Current Output
15	OUT-	Inverted Modulation-Current Output. $I_{MOD}$ flows into this pin when input data is low.
16	OUT+	Non-inverted Modulation-Current Output. $I_{MOD}$ flows into this pin when input data is high.
18	MD	Monitor Photodiode Input. This pin is connected to the anode of a monitor photodiode. A capacitor to ground can be used to filter the high-speed AC monitor photocurrent.
19	APCFILT1	A capacitor (CAPC) to be connected between pin 19 (APCFILT1) and pin 20 (APCFILT2) to set the dominant pole of the APC feedback loop.
20	APCFILT2	
21	APCSET	A resistor connected from this pin to ground sets the desired average optical power. The total capacitive load at the APCSET pin can be a maximum of 10 pF.

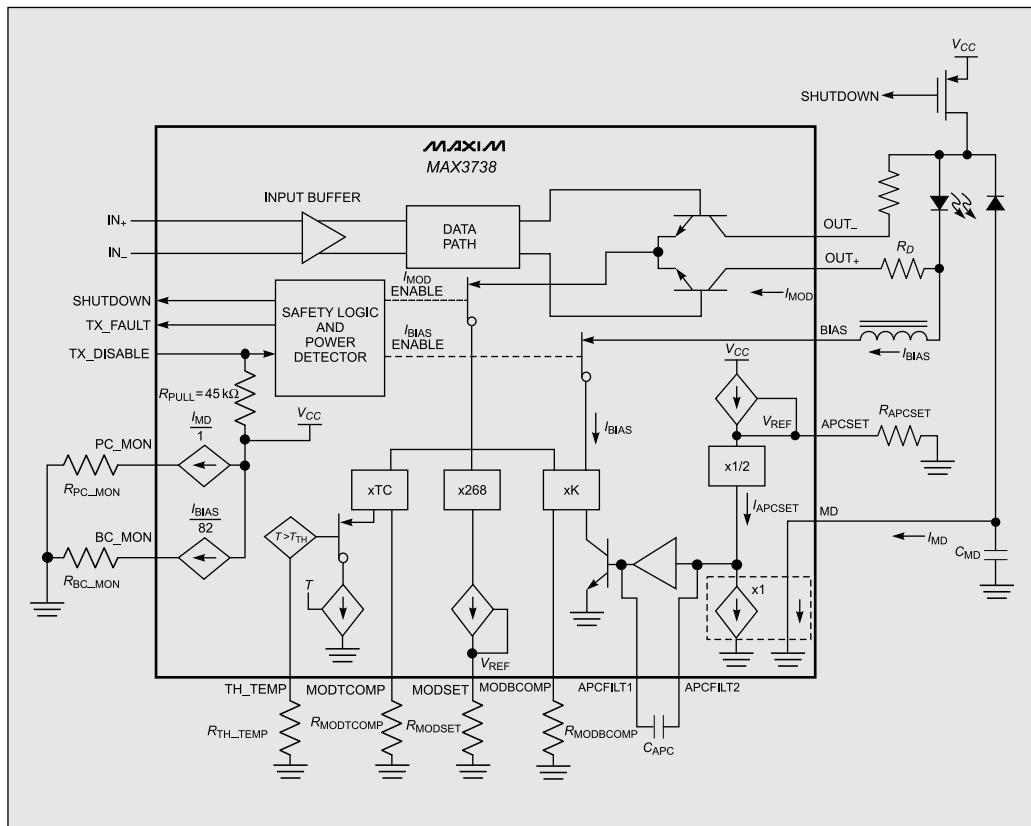
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22	MODSET	A resistor connected from this pin to ground sets the desired constant part of the modulation current.
23	MODBCOMP	Modulation-Current Compensation from Bias. It couples the bias current to the modulation current.
24	TH_TEMP	Threshold for Temperature Compensation. A resistor at this pin programs the temperature above which compensation is added to the modulation current.
—	EP	Exposed Pad. The exposed pad is to be soldered to the circuit board ground terminal for expected thermal and electrical performance.

The datasheet of IC MAX3738 available at

<http://datasheets.maximintegrated.com/en/ds/MAX3738.pdf> can be referred to for obtaining more information in test circuits and characterisation.

**Description of the internal blocks** The IC MAX3738 laser driver consists of three main parts, namely, (1) a high-speed modulation driver (2) biasing block with Extinction Ratio Control (ERC) and (3) safety circuitry. The functional diagram of the IC is shown in Fig. 12.40.



**Fig. 12.40** Functional diagram of IC MAX3738

**High-speed modulation driver** The high-speed modulation driver output stage is composed of a high-speed differential pair and a programmable modulation current source. The IC is optimised for driving a  $15\ \Omega$  load. The minimum instantaneous voltage required at OUT– is 0.7 V for modulation current values of up to 60 mA, and 0.75 V for obtaining currents from 60 mA to 85 mA.

A damping resistor ( $R_D$ ) is required to interface with the laser diode. The combined resistance due to the damping resistor and the Equivalent Series Resistance (ESR) of the laser diode must equal  $15\ \Omega$ . To further damp the aberrations caused by laser diode parasitic inductance, an  $RC$  shunt network may be required.

At high data rates, any capacitive load at the cathode of a laser diode degrades its optical output performance. Since the BIAS output is directly connected to the laser cathode, one needs to minimise the parasitic capacitance associated with the pin through the use of an inductor, which can isolate the BIAS pin parasitics from affecting the laser cathode.

**Extinction ratio control** The extinction ratio ( $r_e$ ) is the laser on-state power divided by the off-state power. Extinction ratio remains constant when the peak-to-peak and the average power values are held constant. The extinction ratio is given by

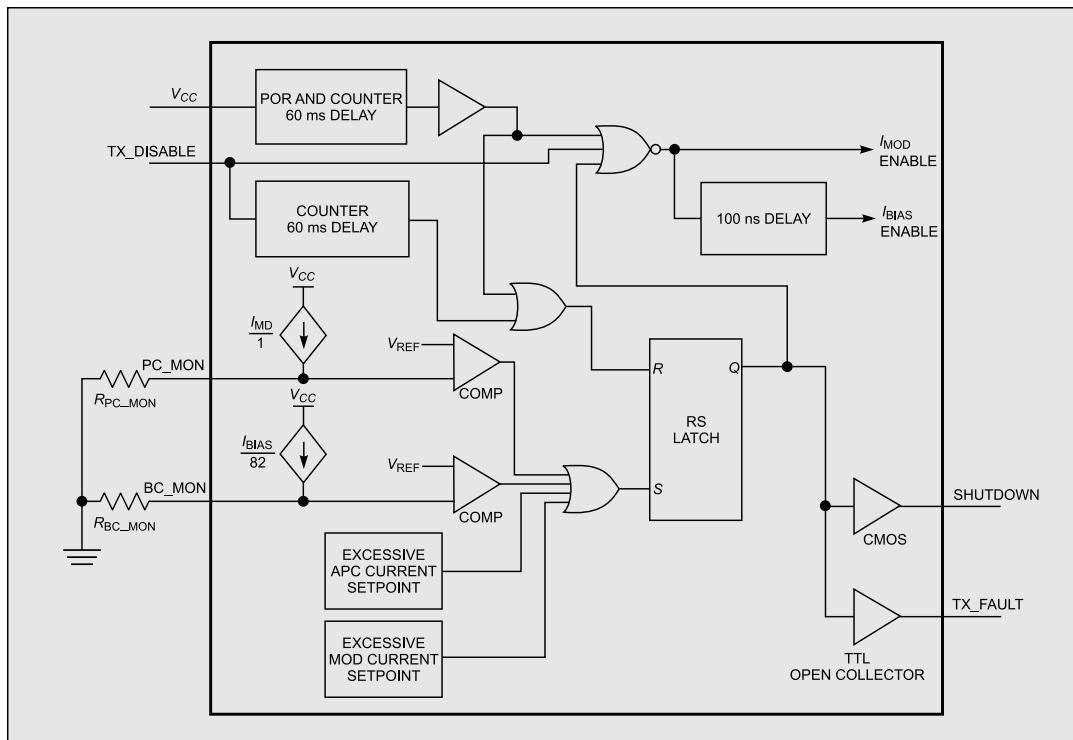
$$r_e = (2P_{AVG} + P_{P-P}) / (2P_{AVG} - P_{P-P})$$

Average power is regulated using APC. It keeps constant current from a photodiode coupled to the laser. Peak-to-peak power  $P_{P-P}$  is maintained by compensating the modulation current for reduced slope efficiency ( $\eta$ ) of laser over time and temperature. Slope efficiency decreases more rapidly as temperature increases. The MAX3738 provides additional temperature compensation as temperature increases past a user-defined threshold ( $T_{TH}$ )

Typical fault conditions of the IC could be

1. If any of the I/O pins are shorted to GND or  $V_{CC}$  terminals and the bias current or the photocurrent goes beyond the programmed threshold value.
2. End-of-life (EOL) condition pertaining to the laser diode.
3. Laser cathode when grounded, the photocurrent exceeds the programming threshold.
4. No feedback for the APC loop due to broken interconnection, defective monitor photodiode, or when the bias current exceeds the programmed threshold.

**Safety circuitry** The safety circuitry shown in Fig. 12.41 contains a disable input (TX\_DISABLE), a latched fault output (TX\_FAULT), and fault detectors. This circuitry part monitors during the operation of the laser driver and forces a shutdown if a fault is detected. The TX\_FAULT pin should be pulled high with a  $4.7\ k\Omega$  to  $10\ k\Omega$  resistor to  $V_{CC}$  as required by the SFP MSA. A single-point fault can be a short to  $V_{CC}$  or GND. The transmit fault condition is latched until reset by a toggle or TX\_DISABLE or  $V_{CC}$ . The laser driver offers redundant laser diode shutdown through the optional shutdown. This shutdown transistor prevents a single-point fault at the laser from creating an unsafe condition.



**Fig. 12.41** Simplified safety circuit

**Safety circuitry current monitors** The MAX3738 features monitors (BC\_MON, PC\_MON) for bias current ( $I_{BIAS}$ ) and photocurrent ( $I_{MD}$ ). The monitors are realised by mirroring a fraction of the currents and developing voltages across external resistors connected to ground. Voltages greater than  $V_{REF}$  at PC\_MON or BC\_MON result in a fault state. On-chip isolation resistors are included to reduce the number of components needed to implement this function.

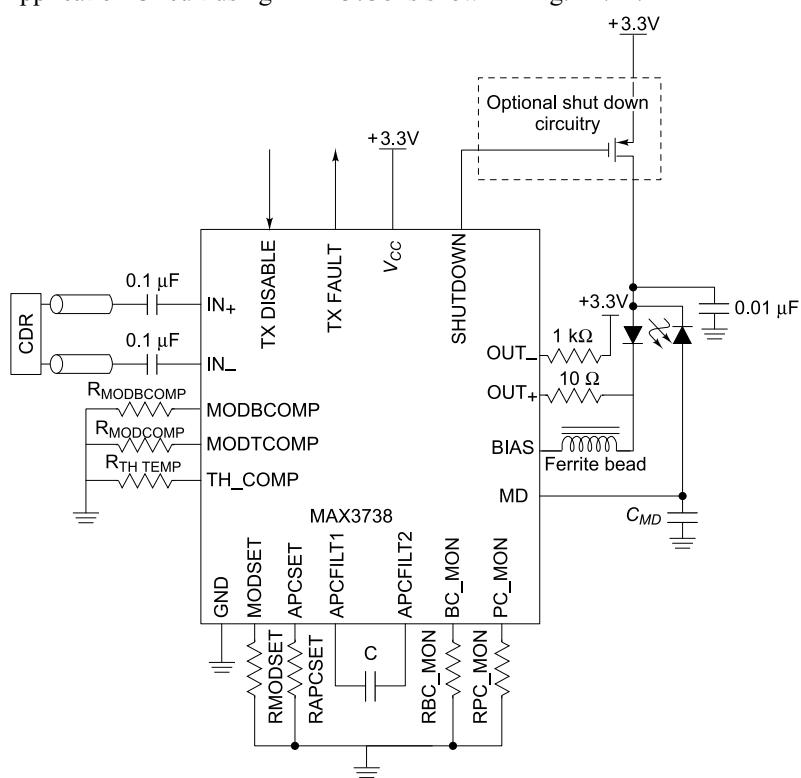
**Design procedure** When designing a laser transmitter, the optical output is usually expressed in terms of average power and extinction ratio. Table 12.5 shows relationships that are helpful in converting between the optical average power and the modulation current. These relationships are when the mark density and duty cycle of the optical waveform are 50%. For a desired laser average optical power ( $P_{AVG}$ ) and optical extinction ratio ( $r_e$ ), the required bias and modulation currents can be calculated using the equations in Table 12.5. Proper setting of these currents requires knowledge of the laser to monitor transfer ( $P_{MON}$ ) and slope efficiency ( $\eta$ ).

**Table 12.5** Optical power relations

Parameter	Symbol	Relation
Average Power	$P_{AVG}$	$P_{AVG} = (P_0 + P_1)/2$
Extinction Ratio	$R_e$	$r_e = P_1/P_0$
Optical Power of a One	$P_1$	$P_1 = 2P_{AVG} \times r_e/(r_e + 1)$
Optical Power of a Zero	$P_0$	$P_0 = 2P_{AVG}/(r_e + 1)$
Optical Amplitude	$P_{P-P}$	$P_{P-P} = P_1 - P_0$
Laser Slope Efficiency	$H$	$\eta = P_{P-P}/I_{MOD}$
Modulation Current	$I_{MOD}$	$I_{MOD} = P_{P-P}/\eta$
Threshold Current	$I_{TH}$	$P_0 \text{ at } I I_{TH}$
Bias Current (AC-Coupled)	$I_{BIAS}$	$I_{BIAS} I_{TH} + I_{MOD}/2$
Laser to Monitor Transfer	$P_{MON}$	$I_{MD}/P_{AVG}$

**Layout considerations** To minimise loss and crosstalk, the connections between the MAX3738 output and the laser diode are kept as short as possible. Good high-frequency layout techniques and multilayer boards with uninterrupted ground plane are to be preferred to minimise EMI and crosstalk. Circuit boards should be made using low-loss dielectrics. Controlled-impedance lines for data inputs, as well as the module output are to be employed.

A Typical Application Circuit using MAX3738 is shown in Fig. 12.42.

**Fig. 12.42** Connection diagram of MAX3738 Laser Driver

The MAX3286/MAX3296 series of ICs are high speed laser drivers for fibre optic transmitters. They are optimised for Gigabit Ethernet applications.

## 12.12 COMPANDER INTEGRATED CIRCUITS

While designing an audio system, the basic requirements are based on two factors, namely (i) sound quality and (ii) data rate. Based on these factors, a trade-off between the sound quality and data rate are normally made. A *high-fidelity music* needs very good sound quality with high data rate, while the *telephone communication* requires a natural sounding speech with a low data rate. A *compressed speech* has a tolerable sound quality with a very low data rate.

### 12.12.1 Companding

The *data rate* factor is important in communication, since this decides the cost of transmitting the signal. *Companding* is a process by which the transmission bit rate of a signal is minimised by compressing it before transmission and expanding it after reception to retrieve the original signal. It is a fundamental data compression technique and it requires minimal processing, allowing signals with a large dynamic range to be transmitted over facilities that have a smaller dynamic range capability. Companding reduces the noise and crosstalk levels also at the receiver. This forms a part of pulse code modulation process, where analog signal values are logically transformed to discrete scale step values on a non-linear scale.

Many compander ICs are available from IC manufacturers. Typical ICs are IC SL5020/P, SL5015/P, TA31103 and IC MM1077.

The IC MM1077 is used in cordless telephone equipment. It incorporates compressor / expander circuits. Using this IC, significant noise reduction can be achieved without complex external circuitries.

Figure 12.43(a) shows the functional block diagram of IC MM1077. The pin diagram and pin assignments are shown in Fig. 12.43(b). At the transmission end, the dynamic range of audio signals is compressed by the compressor circuit. The compressor unit consists of the mike amplifier, compressor, limiter circuit, data amplifier and a mute circuit.

The mike amplifier is connected directly to a microphone. The gain of mike amplifier can be adjusted through an external resistor. The internal limiter circuit prevents over-modulation. Data amplifiers (0dB amplification) help in transmission of data signals without compression. The compressor mute switch enables switching between audio signals and data signals.

The expander unit comprises an input amplifier, an expander and a mute circuit. The input amplifier has all the input and output signals drawn out as external pins. Hence, it can be used freely as an amplifier, filter amplifier or data amplifier. When the expander unit is used as a data amplifier, the expander *mute* switch is *set*.

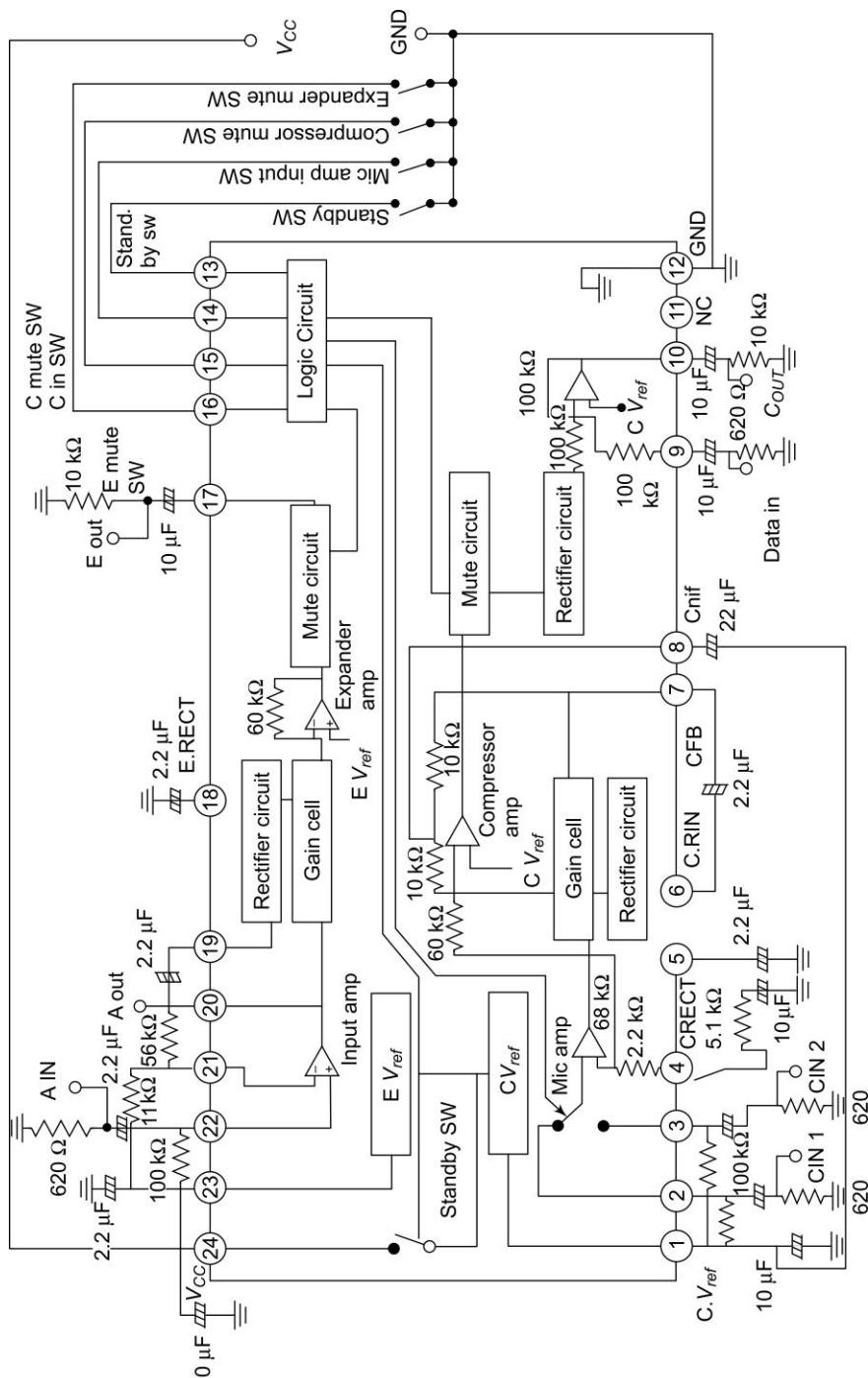
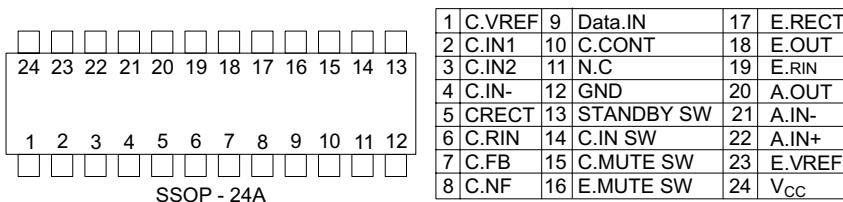


Fig. 12.43 (a) Functional block diagram of IC MM1077

**Fig. 12.43 (b)** Pin diagram and pin assignments of IC MM1077

The important features of IC MM1077 are:

- (i) It can be operated at low voltage 2 V
- (ii) Internal mute function is available
- (iii) Internal limiter function is provided
- (iv) The compressor input can be switched between MIC and LINE
- (v) Internal standby function is possible
- (vi) Data input and output pins are drawn out and
- (vii) Independent mute circuit is available

The major applications of compander ICs are in cordless telephones and other mobile communication devices.

Table 12.6 shows the electrical characteristics of the IC MM1077. The measurement conditions indicates the default values assumed, such as,  $T_a = 25^\circ\text{C}$ ,  $V_{CC} = 3\text{ V}$  and  $f_m = 1\text{ kHz}$ .

**Table 12.6** Electrical characteristics of IC MM1077

<b>Item</b>	<b>Symbol</b>	<b>Measurement conditions</b>	<b>Min.</b>	<b>Typ.</b>	<b>Max.</b>	<b>Units</b>	
Compressor unit	Consumption current	$I_{CC}$	No signal		4.0	6.0	mA
	Standby current consumption	$I_{SCC}$			0	10	$\mu\text{A}$
	Threshold voltage	$V_{th}$		0.40	0.65	0.80	V
	Input reference level	$V_{INC}$	$V_{OC} = 100\text{ mVrms}$ , $V_{IN} = 0\text{ dB}$	8.0	13.5	18.0	mVrms
	Gain error*	$G_{c1}$	$V_{IN} = -20\text{ dB}$	-0.5	0	0.5	dB
		$G_{c2}$	$V_{IN} = -40\text{ dB}$	-1.0	0	1.0	dB
	Distortion	THDc	$V_{IN} = 0\text{ dB}$		0.3	1.0	%
	Output noise voltage	$V_{nc}$	No signal (CCITT)		2.5	5.0	mVrms
	Mute attenuation	Attc	$V_{IN} = 0\text{ dB}$ , C.MUTE SW : ON	40	50		dB
	Limit voltage	$V_{limc}$	THD = 10%	700	800	900	$\text{mV}_{\text{p-p}}$
	DATA pin voltage gain	$G_{DATA}$	C.MUTE SW : ON, $V_{IN} = 0\text{ dB}$	-0.5	0	0.5	dB
	DATA pin maximum output	VD max.	C.MUTE SW : ON, THD = 10%	800	900		mVrms
	Crosstalk	CTc	$\text{EXP}V_{IN} = 0\text{ dB}$	28	33		dB
	Ripple rejection ratio	RRc	$V_R = 100\text{ mVrms}$ , $f_R = 1\text{ kHz}$	18	23		dB

**Contd.**

	Input reference level	$V_{INe}$	$V_{oe} = 100 \text{ mVrms}, V_{IN} = 0 \text{ dB}$	25	35	50	mVrms
Gain error difference*	Ge1	$V_{IN} = -10 \text{ dB}$	-0.5	0	0.5	dB	
	Ge2	$V_{IN} = -20 \text{ dB}$	-1.0	0	1.0	dB	
	Ge3	$V_{IN} = -30 \text{ dB}$	-1.5	0	1.5	dB	
Distortion	THDe	$V_{IN} = 0 \text{ dB}$		0.15	1.0	%	
Maximum output voltage	Ve max.	THD = 10%	600	800			mVrms
Output noise voltage	Vne	No signal (CCITT)		20	40	$\mu\text{Vrms}$	
Mute attenuation	Atte	$V_{IN} = 0 \text{ dB}, \text{C.MUTE SW : ON}$	60	70			dB
Input amp voltage gain	GI	$V_{IN} = 0 \text{ dB}$	14.6	15.6	16.6		dB
Input amp maximum output	Ve0 max.	THD = 10%	0.90	1.10			Vrms
Crosstalk	CTe	$\text{COMP} V_{IN} = 0 \text{ dB}$	60	75			dB
Ripple rejection ratio	RRe	$V_R = 100 \text{ mVrms}, f_R = 1 \text{ kHz}$	50	60			dB

\*Gain error difference =  $(V_{OUT}(\text{dBv}) + 20 \text{ dB}) - V_{IN}(\text{dB}) \times G(\text{dB})$

G : COMP = 0.5, EXP = 2 (Ref: Mitsumi Comander IC MM1077 data sheet)

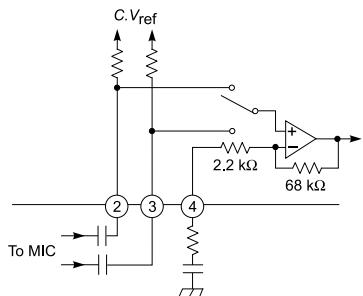
The functional description of the major modules of the comander IC MM1077 is given below:

**Compressor unit** The compressor unit consists of the mike amplifier, compressor, limiter circuit, data amplifier, and mute circuit. The mike amp gain can be adjusted through an external resistance, and so the mike amp can be connected directly to a microphone. An internal limiter circuit is provided. This prevents overmodulation. Furthermore, a 0 dB data amplifier is also provided that enabled the transmission of data signals without compression. Switching between audio signals and data signals is possible using the compressor mute switch.

**Expander unit** The expander unit consists of an input amplifier, expander and the mute circuit. The input amplifier makes available all the input and output signals at necessary pins. They can be used freely as an amplifier, filter amplifier, or data amplifier. When used as a data amplifier, the expander mute switch can be set such that the expander output is nearly silent. The compressor unit mike amplifier is exposed to circuits outside the IC through the positive and negative input pins. The positive input pin is connected to  $C. V_{ref}$  by through bias resistance of  $100 \text{ k}\Omega$ , so that no external bias is needed.

## 12.12.2 Application Circuit Configurations of Comander IC

**Microphone amplifier** The compressor unit mike amp is exposed to circuits outside the IC via positive and negative input pins, namely, pin 2 and pin 3. The positive input pin is connected to  $C. V_{ref}$  by a bias resistance of  $100 \text{ k}\Omega$ . Hence, no external bias is needed. When pin 4 is open the gain is the lowest, and an input voltage of approx.  $13.5 V_{rms}$  is the reference level. When the external resistance is  $0 \Omega$ , the gain is set to the maximum value. The internal configuration is shown in Fig. 12.44.



**Fig. 12.44** Microphone amplifier circuit

**Rectifier unit** Figure 12.45 shows the rectifier circuit. The product of the external capacitance value and the internal resistance ( $10\text{ k}\Omega$ ) determines the time constant for the attack and release times.

**Compressor amplifier** The compressor amp requires that the dc gain remains to be unity and the ac gain be of infinite value. In order to satisfy this prerequisite, the ac feedback is eliminated and only dc feedback is used. This is realised by using a capacitor that eliminates any ac components connected to pin 8. The cutoff frequency is determined by the product with the internal resistance ( $100\text{ k}\Omega$ ). The circuit configuration of the compressor amplifier is shown in Fig. 12.46.

**Compressor data amplifier** The data amplifier shown in Fig. 12.47 uses an inverting amplifier structure. The internal input resistance is  $100\text{ k}\Omega$ , and the dc bias voltage is set to be 1.3 V. The compressor mute switch provided at pin 10 is used to switch between data signals and audio signals as required.

**Expander input amplifier** Figure 12.48 depicts the expander input amplifier structure. The positive and negative input pins and the output pin are exposed to circuitry outside the IC. The expander input amp can be employed as a signal amplifier, a buffer amplifier, and a filter amp. The signal from this output pin of the amplifier can be observed, without letting the data signals pass through the expander. When the expander mute switch is turned on, this signal can be prevented from appearing at the expander output.

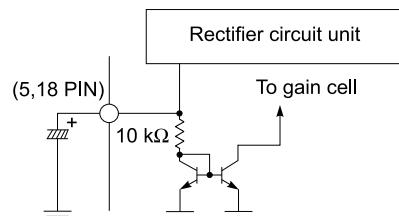
### **12.12.3 Compander IC MM1100**

This IC was developed for use in mobile communication equipment. It is a compander IC incorporating *compressor/expander* circuits for significant noise reduction effects without complicated external circuitry. On the transmission side, the dynamic range of audio signals is compressed by the compressor circuit; on the receiving side, the expander expands the signals. As a result, the dynamic range over the transmission channel is reduced logarithmically by one-half.

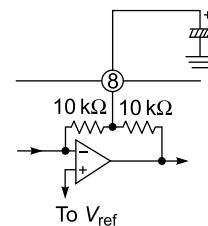
The features of the IC are:

- (i) It can be operated with voltages down to 2.4 V
  - (ii) Unwanted radio waves are suppressed from compression and expansion circuits
  - (iii) The consumption current is normally 2.8 mA.

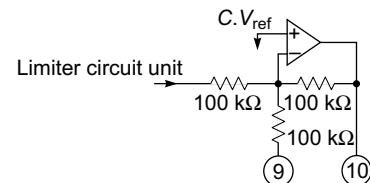
The applications of the IC are in cordless telephones and various mobile communication services.



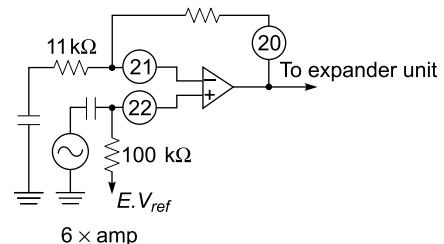
**Fig. 12.45** Rectifier unit



**Fig. 12.46** Compressor circuit configuration

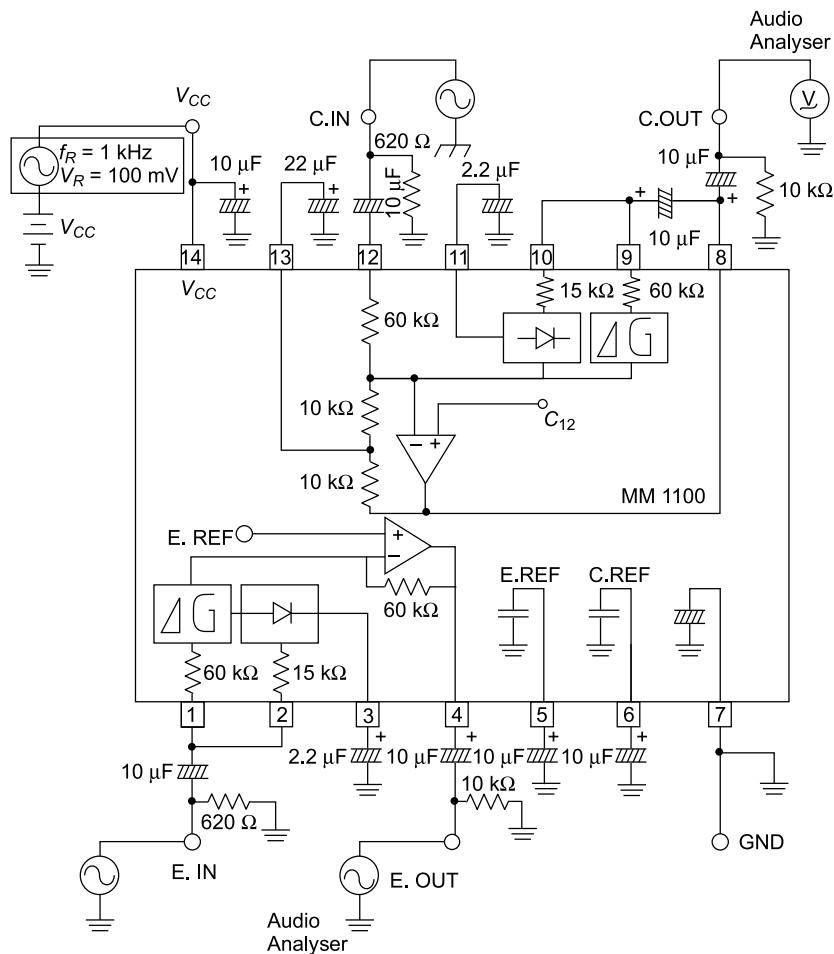


**Fig. 12.47** Compressor data amplifier

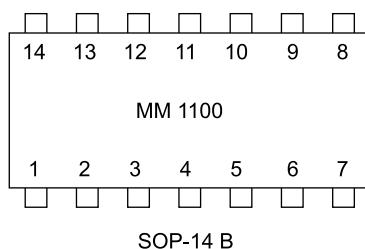


**Fig. 12.48** Expander input amplifier

Figure 12.49(a) shows the functional block diagram of IC MM1100. The pin diagram and pin assignments are shown in Fig. 12.49(b).



**Fig. 12.49** (a) Functional block diagram of IC MM1100



1	E.GIN	8	C.OUT
2	E.RIN	9	C.GIN
3	E.RECT	10	C.RIN
4	E.OUT	11	C.RECT
5	E.REF	12	C.IN
6	C.REF	13	C.NF
7	GND	14	Vcc

**Fig. 12.49** (b) Pin diagram and pin assignment of IC MM1100

## SUMMARY

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- ❑ Voltage-to-frequency and frequency-to-voltage converter, opto-coupler, isolation amplifier, fibre-optic and compander ICs are the special function integrated circuits discussed.
- ❑ A Voltage-to-Frequency (V/F) converter produces an output signal whose frequency at any instant is a function of the external control input voltage and it is represented by  $f_o = k_v V_i$  where  $k_v$  is the sensitivity of V/F converter in Hz/V.
- ❑ A Frequency-to-Voltage (F/V) converter produces an output voltage whose amplitude is a function of frequency of the input signal and is given by  $V_o = k_f f_i$ .
- ❑ A Frequency-to-Voltage converter is an FM detector or discriminator. The two types of (F/V) converters are Pulse-integrating and Phase-locked-loop F/V converters.
- ❑ VFC32 from Burr Brown is a F/V converter. It uses *charge balancing* technique for *Voltage-to-Frequency* conversion.
- ❑ The VFC32 offers 6-decades of dynamic range with linearity errors of 0.005%, 0.025% and 0.05% of full scale for 10 kHz, 100 kHz and 500 kHz frequencies.
- ❑ The 9400 series of ICs from Teledyne Inc. available in 14-pin DIP and ceramic packages can be used for voltage-to-frequency and frequency-to-voltage conversions.
- ❑ XR-2206 from Exar is a function generator that can generate triangular and square waveforms. It consists of a logarithmic wave-shaper for converting the triangular wave to sine-wave.
- ❑ XR-2206 consists of a voltage-controlled oscillator (VCO), an analog multiplier, a sine-wave shaper, a unity gain buffer amplifier and a set of current switches.
- ❑ MC1550G from Motorola Semiconductor Inc. consists of a differential amplifier stage, Automatic Gain Control (AGC) circuit, an amplitude modulator and a video amplifier.
- ❑ Small signal amplifiers are generally voltage amplifiers. They supply larger and amplified signals to their output loads.
- ❑ LM380 is a specialised IC designed for typical audio applications requiring higher currents and more power of the order of few watts to tens of watts to load.
- ❑ The output impedance of the audio power amplifier is ideally zero.
- ❑ The audio amplifier can be classified based on the power rating into
  - Low power audio amplifier –0 to 50 mW
  - Medium power audio amplifier –50 mW to 500 mW and
  - High power audio amplifier – More than 500 mW
- ❑ Power Conversion Efficiency is defined as  $\eta = \frac{P_{ac}}{P_{dc}}$  where  $P_{ac}$  is the ac output power at the load and  $P_{dc}$  is the *dc* input supplied to the amplifier.
- ❑ The class A power amplifier operates during  $360^\circ$  of input signal and the maximum power conversion efficiency is 25%.
- ❑ The class B power amplifier is biased at near cut-off so that the conduction occurs only for one half or  $180^\circ$  of the input signal. The maximum power conversion efficiency is 78.5%.
- ❑ The output stage normally consists of two transistors connected in *push-pull* arrangement.
- ❑ The class B amplifier has cross-over distortion limitation.
- ❑ When the transistors are biased slightly into the active region conducting for more than  $180^\circ$ , then the class B power amplifier is called class AB amplifiers.
- ❑ LM380 from National Semiconductor is an audio power amplifier with the following features:
  - It has a wide operating supply voltage range from 5 V to 20 V with low quiescent power drain, high peak current of 1.3 A and a voltage gain of 34 dB
  - It has a unique, ground referenced or ac coupled input stage with high input impedance of the order of  $150\text{ k}\Omega$
  - It has low distortion (Total Harmonic Distortion 0.2%)
  - The standard dual-in-line packages (8-pin and 14-pin) which can operate at temperature of  $0^\circ\text{C}$  to  $70^\circ\text{C}$  are available
  - A bandwidth of 100 kHz typically at an output power of 2 W and load of  $8\text{ }\Omega$  is possible

- Heat sink for LM380 is provided by a copper lead frame attached with the centre three pins on both sides.
- LM380 is used for applications such as audio power amplifier, high gain audio amplifier, intercom system and bridge amplifier.
- Audio power amplifier LM384 can offer power up to 5 W.
- Video or wideband amplifiers provide a relatively flat gain versus frequency response characteristics for video frequencies from 20 Hz to several MHz.
- The high voltage gains are achieved at the cost of reduced frequency response characteristics or trading-off gain for increased bandwidth that is accomplished by the use of reduced load resistance or by the use of negative feedback.
- IC 733 is a two-stage, differential input, differential output and wideband video amplifier with internal series-shunt feedback offering wider bandwidth of around 120 MHz with low phase distortion and stable and selectable gains of 10, 100 and 400.
- 733 Video Amplifier finds use in the magnetic tape systems, disk file memories, thin and thick film memories, woven and plated wire memories and wideband video amplifiers.
- HA-2539 from Harris semiconductor is a wideband amplifier with a gain-bandwidth of 600 MHz, and a full power bandwidth of 9.5 MHz while driving a  $1000\ \Omega$  load with 20 V peak-to-peak voltage swing.
- RCA 3040 is a monolithic video amplifier from RCA that can work with single or balanced input signals employing a differential cascode input stage. It can provide single or balanced output. The overall mid-frequency voltage gain is around 110. The IC 3040 exhibits very large gain-bandwidth product and typical 3 dB bandwidth of 55 MHz.
- An opto-coupler or an opto-isolator is a solid state device in which the light emitter, the light path and the light detector are closed and that provides electrical isolation between two circuits. It can couple digital (logic 1 or 0) or analog (continuously variable) signals.
- The opto-couplers are constructed using a photodiode, photo Darlington pair or photo-SCR. Some of the important opto-couplers considered are type TLP112 from Toshiba which is a mini-Flat coupler consisting of GaAlAs light emitting diode, optically coupled to a high speed detector of a single-chip photodiode-transistor assembly, MOC3009 series opto-couplers consist of Gallium-Arsenide-Diode Infrared source and an optically coupled silicon Triac driver that can provide 250V driver output, with an electrical isolation of 7500V peak available in standard 6-pin Plastic DIP directly interchangeable with MOC3009, MOC3010, MOC3011 and MOC3012, type TLP141G suitable for surface mount assembly consisting of a GaAs Infra Red Emitting Diode (IRED) and optically coupled to a high-speed photo-thyristor detector. The TLP521, TLP521-2, TLP521-4 series of opto-couplers consist of infrared light emitting diodes and NPN silicon photo transistors in space efficient DIP plastic packages.
- The main applications of opto-couplers are computer terminals, industrial system controllers, measuring instruments and signal transmission systems of different operating voltages and characteristic impedances.
- The main advantages of opto-couplers are the electrical isolation of several thousand volts, very small response time that makes it usable in data applications of Mega Hertz range of pulse frequencies, capable of wideband signal transmission, easy interfacing capability, portable, shows better efficiency than isolation transformers and relays, and the ambient condition problems such as noise, transients and contact bounce etc. are completely eliminated.
- The isolation amplifier achieves no physical contact between the input and output. It is used in applications requiring very large common-mode voltage difference of the order of several thousand volts between the input and output sections and linearity. This isolation barrier is accomplished through an optical coupler acting as a 1:1 current translator. Most of the isolation amplifiers are hybrid ICs consisting of an input amplifier, a GaAs Light-Emitting Diode (LED), a silicon photo diode and an output amplifier.
- Typical isolation amplifier chips are ISO100, 3450–3455 series from Burr-Brown and AD293 and AD294 from Analog Devices. They are used in medical instrumentation, where the patient must be isolated and protected from leakage currents.
- MAX3738 laser driver IC is a high speed laser driver for fibre optic transmitters that are optimised for Gigabit Ethernet applications. It is used in

- 1Gbps / 2Gbps fibre channel SFF / SFP and GBIC transceivers
  - Gigabit Ethernet SFF / SFP and transceiver modules
  - Multirate OC-24 to OC-48 FEC transceivers
- Companding* is a fundamental data compression technique, which compresses the data before transmission and expands it after reception to retrieve the original signal. This process minimises the transmission bit rate of a signal and it reduces the noise and crosstalk levels at the receiver. Typical compander ICs are IC SL5020/P, SL5015/P, TA31103 and IC MM1077.

## REVIEW QUESTIONS

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1. Explain the ideal characteristics of V/F and F/V converters.
2. Briefly describe the application of V/F and F/V converters.
3. Write notes on V/F converter and its applications.
4. Explain the operational features of IC VFC32 for F/V and V/F conversions.
5. Explain the operational features of IC TC9400 for F/V and V/F conversions.
6. Draw the block diagram of IC 9400 and explain the operation of individual blocks.
7. Explain the operation of IC 9400 with unipolar and bipolar supply voltages.
8. Explain the operation of voltage-to-frequency and frequency-to-voltage converters using IC TC9400.
9. Explain the use of level shifters with IC 9400 for bipolar and single supply operations.
10. Explain the operation of XR-2206 function generator with a neat block diagram
11. Explain the use of XR-2206 for
  - (a) Sinusoidal signal generation
  - (b) FSK generation and
  - (c) Pulse and ramp waveform generation
12. What are tuned amplifiers?
13. Explain the operation of tuned amplifier using MC1550G.
14. What is the range of audio frequency?
15. Classify power amplifiers and explain them briefly.
16. Design a class A single-ended power amplifier and explain its operation.
17. Explain the operation of single supply audio amplifier.
18. List down the features of LM380 audio power amplifier.
19. Explain with neat circuit diagrams, the following applications of IC LM380:
  - (a) Audio amplifier
  - (b) High gain audio amplifier
  - (c) Intercom system
  - (d) Bridge amplifier
20. With necessary diagrams, describe a monolithic IC power amplifier. What are its advantages over conventional power amplifiers?
21. Describe two applications of a monolithic IC power amplifier.
22. What is meant by video amplifier?
23. Describe the features of ICs used for video amplification.
24. What are the advantages of the IC video amplifier over discrete circuit video amplifiers?
25. State the special features of the video amplifier IC.
26. What are the design considerations to be met while designing a video amplifier?
27. Explain the operation of a typical video amplifier circuit.
28. Comment on the frequency response of video amplifier.
29. Draw the block diagram of a typical IC audio amplifier and briefly explain its salient features.
30. What are the features of IC 733 video amplifier?

31. Explain the internal circuit diagram of IC 733 video amplifier.
32. What are the features of CA3040 video amplifier?
33. Explain the internal circuit diagram of CA3040 video amplifier.
34. Explain in brief any one IC chip used in a colour TV receiver.
35. What are opto-couplers/opto-isolators?
36. Describe the operation of opto-coupler.
37. List the applications of opto-coupler.
38. What are the characteristics of opto-coupler?
39. Define Current Transfer Ratio of an opto-coupler.
40. Explain the features of opto-coupler ICs.
41. Write a note on opto-coupler ICs and their packaging.
42. Describe the features of opto-coupler ICs using
  - (a) LED-Photo transistor
  - (b) LED-Photodiode
  - (c) IRED-Thyristor and
  - (d) IRED-Triac
43. What is an isolation amplifier?
44. Explain the applications of isolation amplifier.
45. Explain any one isolation amplifier IC with the help of a block diagram.
46. Draw the internal block diagram of ISO100 and explain its operation.
47. Draw the dc Error model of ISO100, and explain the individual current components you find in the IC.
48. Explain the standard operating configurations of ISO100.
49. Write short notes on fibre-optic ICs.
50. Define *loss-budget* in the design of fibre-optic communication link.
51. Explain the operation of a Laser driver transceiver IC with a block diagram.
52. Define companding.
53. What are the advantages of companding?
54. What are the features of a compander IC?
55. List the applications of compander.
56. Write a detailed note on any one of the compander ICs.
57. Design a V/F converter using IC VFC 32 to yield a full-scale output frequency of 200 kHz for a full-scale input voltage of 10 V.
58. Design a frequency to voltage converter using IC VFC 32 for a full scale output of 10 V for a full-scale input frequency of 100 kHz with a maximum ripple of 10 mV.
59. The V/F converter of Fig. 12.5(a) is initially adjusted for 8 kHz of full-scale output frequency  $f_o$ . Calculate the output frequencies  $f_o$  and  $f_o/2$  when the input signal  $v_1 = 2$  V.
60. A class-A amplifier is needed to deliver an ac power output of 6 W. What is the minimum power rating of the amplifier? Also, determine the minimum power rating of the dc supply connected to the amplifier.

# Advanced Operational Amplifiers

## 13.1 INTRODUCTION

The op-amps are extensively used in electronic systems. The op-amps can be configured in several forms using the bipolar junction transistors, unijunction transistors, MOS transistors and combinations of them for specialised applications. The all-BJT op-amp  $\mu$ A741 and its circuit configurations and characteristics have been discussed in Chapter 3. In this chapter, the basic circuit configurations for forming larger analog circuits using the transistors such as JFET and MOSFET which are fabricated as integrated circuits are dealt with. The CMOS op-amps, BiCMOS op-amps, JFET op-amps and the widely used operational transconductance amplifier (OTA) are discussed.

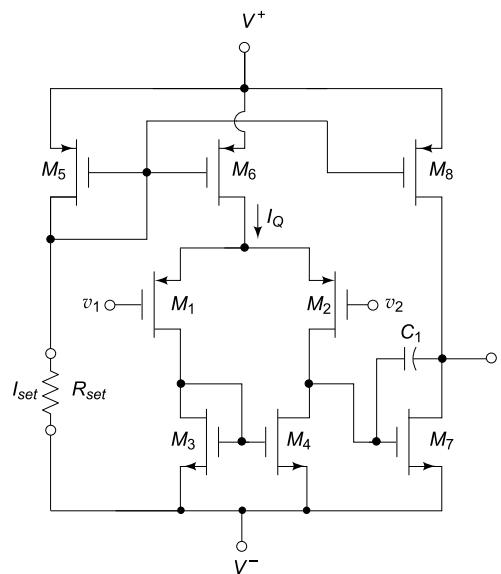
## 13.2 CMOS OPERATIONAL AMPLIFIER

The bipolar op-amp IC 741 is capable of sourcing and sinking large load currents. This is facilitated by the emitter-follower output stage which achieves very low output resistance and this characteristic was used in IC 741 for minimising the loading effects.

On the other hand, the CMOS op-amps are normally designed for particular applications, wherein only a few picofarads of capacitive loads are required to be driven. Therefore, most of the CMOS op-amps do not require a low resistance output stage. When the op-amp input terminals are not connected directly to the IC external terminals, they do not need electrostatic input protection devices also. The folded cascode op-amp involving a current mirror CMOS design is presented in this section.

### 13.2.1 Description of the Circuit

Figure 13.1 shows a simplified circuit diagram of an all-CMOS op-amp MC14573. The PMOS transistors  $M_1$  and  $M_2$  form the input differential pair, and the NMOS transistors  $M_3$  and  $M_4$  form the active load of the differential pair. The differential amplifier input stage is biased by the transistors  $M_5$  and  $M_6$  which form the current mirror. The reference current for the current mirror is determined by an external resistor  $R_{set}$ .



**Fig. 13.1** Simplified circuit of CMOS op-amp MC14573

The second stage acting as the output stage consists of the common-source connected transistor  $M_7$ . The transistor  $M_8$  provides the bias current acting as the active load for the transistor  $M_7$ . An internal compensation capacitor  $C_1$  is connected between the drain and gate of transistor  $M_7$  to provide stability.

### 13.2.2 DC Analysis of MC14573

Considering that the transistors  $M_5$  and  $M_6$  are matched, the reference current and the bias current of the input-stage are given by

$$I_{set} = I_Q = \frac{V^+ - V^- - V_{SG5}}{R_{set}} \quad (13.1)$$

From the basic MOS transistor theory and its square law equation, the reference current and source-to-gate voltage are given by

$$I_{set} = K_{p5} (V_{SG5} + V_{Thp})^2 \quad (13.2)$$

where  $V_{Thp}$  is the threshold voltage for the PMOS transistor  $M_5$ , and  $K_{p5}$  is its conductance parameter.

### 13.2.3 Small-Signal Analysis

The small-signal differential voltage gain of the input stage is given by

$$A_d = \sqrt{2K_{p1}I_Q} (r_{o2} \parallel r_{o4}) \quad (13.3)$$

where  $r_{o2}$  and  $r_{o4}$  are the output resistances of transistors  $M_2$  and  $M_4$  respectively. The input impedance of the second stage is infinite due to the gate-channel oxide insulator. Therefore, it results in zero loading effect by the second stage. Assuming the channel length parameter coefficient  $\lambda$  to be the same for all transistors, we have

$$r_{o2} = r_{o4} = \frac{1}{\lambda I_D} \quad (13.4)$$

where  $I_D$ , the quiescent drain current in  $M_2$  and  $M_4$ , is given by  $I_D = \frac{I_Q}{2}$ .

The gain of the second stage is

$$A_{v2} = g_{m7} (r_{o7} \parallel r_{o8}) \quad (13.5)$$

where

$$g_{m7} = 2\sqrt{K_{n7}I_{D7}} \quad (13.6)$$

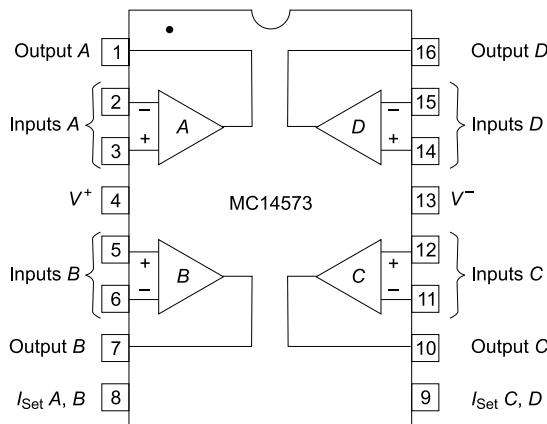
and the resistances

$$r_{o7} = r_{o8} = \frac{1}{\lambda I_{D7}} .$$

Equation (13.5) indicates that there is no loading effect due to an external load connected at the output.

### 13.2.4 Specifications of the IC MC14573

The pin diagram of the quad low-power op-amp is shown in Fig. 13.2.



**Fig. 13.2** Pin diagram of quad op-amp MC14573

It consists of four op-amps configured using CMOS devices in a monolithic structure. The operating current is programmable using the resistor connected at pin 9 and it is set by the resistor  $R_{set}$  connected between  $V_{SS}$  and any one or both of the  $I_{set}$  pins 8 and 9. This makes the IC versatile for making a trade-off between the power dissipation and slew rate characteristics. The op-amps are internally compensated.

The set current for each op-amp pair of the comparator is given by  $I_{set} = \frac{V^+ - V^- - 1.5V}{R_S}$ , where  $R_S$  represents the single programming resistor. When two programming resistors are employed, the set currents are given by  $I_{set} = \frac{V^+ - V^- - 1.5V}{2R_S}$ . The total device current is typically thirteen times that of  $I_{set}$  per pair when the outputs are in *low* state, whereas it is five times  $I_{set}$  per pair when the outputs are in *high* state. When the op-amps are employed in the linear region, the device current is set between the values of five and thirteen times  $I_{set}$ .

While using a single op-amp, the  $I_{set}$  terminal for the pair is normally tied to  $V_{DD}$  for achieving minimum power consumption. For minimising the power consumption of the unused pair of comparators, it is preferable to use a high value set resistor  $R_S$  with the inputs connected to a voltage that will force the output to  $V_{DD}$ . It is to be noted that increasing the value of  $I_{set}$  for comparators will decrease the propagation delay. The normally obtainable maximum output voltage  $V_{OH}$  for a given value of load resistor  $R_L$  with respect to  $V_{SS}$  is given by

$$V_{OH} = 4 \times I_{Set} \times R_L - 0.05V$$

The typical op-amp slew rate (SR) value achievable for MC14573 is given by  $SR \approx 0.041I_{set}$ .

The MC14574 and MC14575 also fall in the family of quad op-amps and comparators. These ICs are excellent building blocks for consumer, industrial, automotive and instrumentation applications. Some applications of these ICs are in active filters, voltage reference circuits, waveform generator circuits, ADCs and comparator circuits. These ICs are usable in both line and battery operated applications.

### 13.3 BiFET AND BiMOS CIRCUITS

The fabrication technologies employing ion implantation techniques permit the fabrication of JFETs, MOSFETs and BJTs on the same substrate as a single chip. The terminologies BiFET and BiMOS normally refer to the ICs fabricated by this process. All of the BiFET or BiMOS op-amps use the FET as the input stage followed by the BJTs for the internal gain stages and output stages. Therefore, they

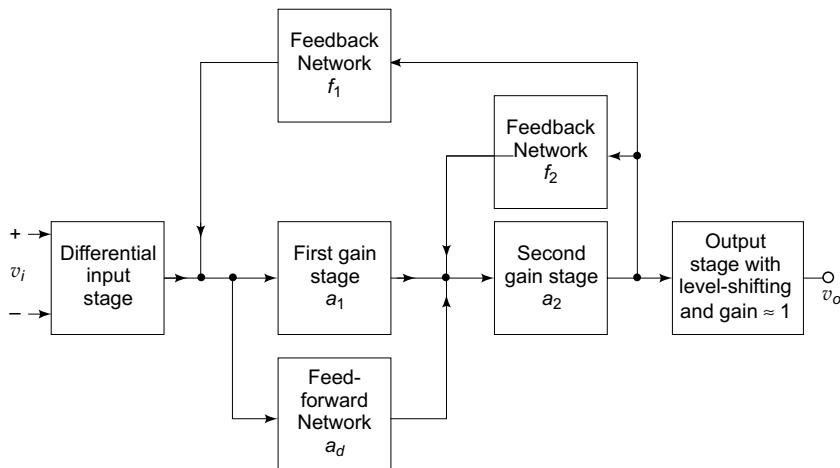
achieve the advantages of both the bipolar and MOSFET devices for the same circuit. The main advantage of MOSFETs is their very high input impedance. Hence, when the MOSFETs form the input differential pair of an op-amp, the input bias currents achieved are extremely small. However, the equivalent noise of the input stage may be greater than that of an all-BJT op-amp.

The amplifiers with FET input stages evolved in the 1970s and by the next decade commercial ICs were commonly available in the market. This is due to the advantageous and onerous features shown by the FET differential input stages, namely, the higher differential mode input resistance, lower input current, reduced input offset currents and higher slew rates to name a few. The higher input resistance of an FET is due to the very high gate to source resistance, which is nearly an open circuit as against the  $r_\pi$  of the bipolar transistors. It is normally four orders of magnitude larger than that of the BJTs. The input bias current of the FET is the reverse saturation current  $I_{SS}$  of the gate to channel junctions in reverse biased condition. This is normally much smaller than the base current of a BJT while assuming equal values of collector and drain currents ( $I_C = I_{DS}$ ) for the two types of transistors. Since the input current  $I_{in} = I_{GSS}$  is very small, the offset current that is generated due to device mismatches is also very small than those arising in BJT based circuits. The MOSFET differential stages augment in further reducing these quantities, since the leakage current through the gate oxide is still smaller than  $I_{GSS}$  of the JFETs. For equal values of  $I_C$  and  $I_{DS}$ , the value of  $g_m$  of an FET is smaller than that of a BJT. Hence, the smaller value of  $g_m$  results in an increased slew rate in an FET. On the other hand, the lower value of  $g_m$  makes the differential mode gain  $A_{DM}$  of FETs less than that of BJT circuits. This limitation is overcome in the BiFET and BiMOS op-amp designs by incorporating three stage architectures as made available in AD611 type of ICs. Finally, the additional advantage of FET input stage is the lower noise effects, which makes the FETs configuring lower noise, low voltage and low power devices as compared to BJTs.

### 13.3.1 Three Stage Op-Amp

Most of the high frequency and the BiFET (BiMOS) op-amps normally constitute three gain stages, viz. a differential amplifier input stage, two gain stages incorporated with the level-shifter stages and an output stage, which is normally an emitter-follower stage. The architecture of a typical three stage op-amp is shown in Fig. 13.3. Since the use of the three stages facilitate higher open-loop gain, the  $g_m$  of the differential stage can be reduced, which results in improved slew rate as given by

$$SR = 8\pi V_T f_G$$



**Fig. 13.3** Three-stage op-amp architecture

where  $V_T$  is Volt equivalent of temperature  
 $f_G$  is unity gain bandwidth

Moreover, the three-stage architecture with feedback can be designed to have higher values of the gain-crossover frequency  $f_G$  than are commonly obtainable in two-stage op-amps. Therefore, both the slew-rate and unity gain bandwidth performance characteristics of the op-amp are increased.

Since each of the stages contribute for a dominant pole in the open-loop amplifier, the stabilisation and compensation become more difficult. Therefore, feedback network circuits are necessitated for achieving frequency compensation in the amplifier. Typically, each of these circuits is formed by RC networks rather than the single capacitor. This overall feedback loop  $f_1$  around both the gain stages is used to obtain a dominant pole in the open-loop transfer function. The inner feedback loop  $f_2$  is designed to make the pole of second gain stage the non-dominant pole of the amplifier. A zero in the amplifier transfer function is introduced by the feed-forward network. The positive phase shift produced by this zero improves the phase margin of the stage and it also helps in stabilising the amplifier. In addition, the positive phase shift attempts in increasing the gain-crossover frequency  $f_G$ . The LM118 from National Semiconductor is a three-stage op-amp with a unity gain bandwidth of 15 MHz and a slew rate of 50 V/ $\mu$ s.

The following section discusses the CA3140 BiCMOS op-amp. Many of the features of this op-amp are similar to those of the IC 741.

### 13.3.2 Circuit Description

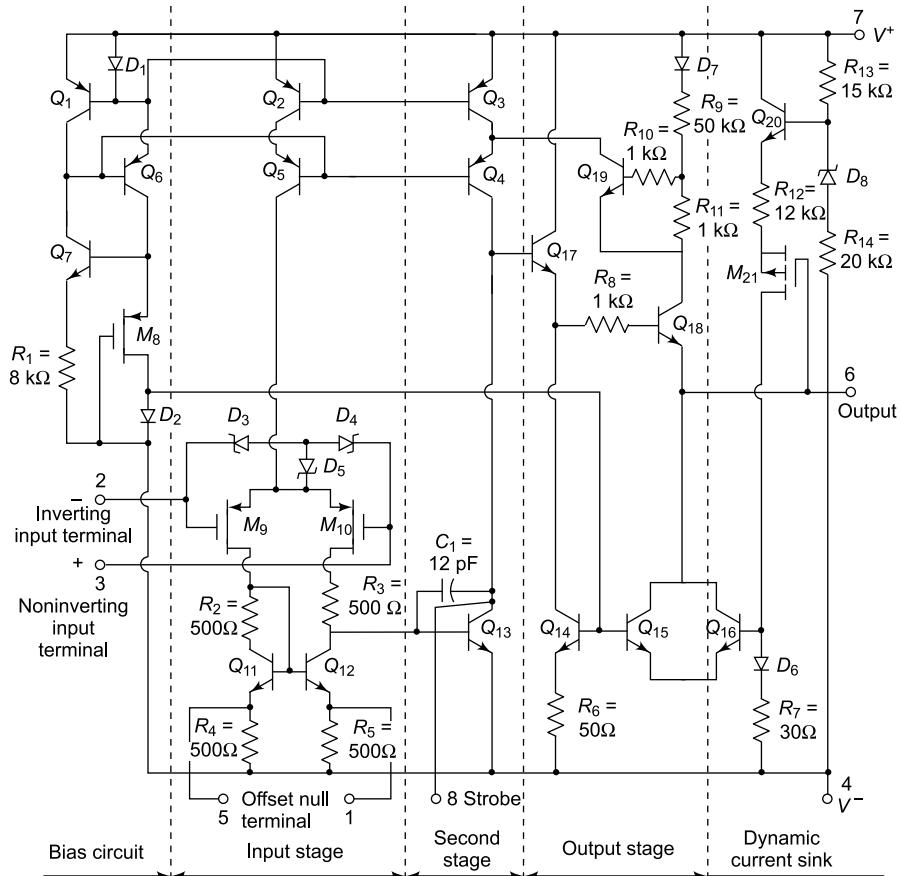
Figure 13.4 shows the basic equivalent circuit of the CA3140 op-amp. The op-amp consists of three basic stages, namely, the input differential stage, the gain stage and the output stage. The circuit also consists of the bias circuit that establishes the dc bias currents in the op-amp and a dynamic current sink. Typical supply voltages used for the IC are  $V^+ = 15$  V and  $V^- = -15$  V.

**Input differential amplifier** The input differential pair consists of *P*-channel MOS transistors  $M_9$  and  $M_{10}$ , and transistors  $Q_{11}$  and  $Q_{12}$  form the active load for the diff-amp. A single-sided output at the collector of  $Q_{12}$  acts as the input to the next gain stage. Two offset null terminals are also provided for offset null facility.

The MOS transistors are very susceptible to electrostatic charges. For example, electrostatic voltage can be accidentally induced on the gate of a MOSFET even during routine handling. These voltages may be large enough to induce breakdown in the gate oxide, thus destroying the device. Therefore, necessary protection of the input against electrostatic damage is provided by the Zener diodes  $D_3$ ,  $D_4$  and  $D_5$ . When the gate voltage becomes sufficiently high, the diodes facilitate a discharge path for the electrostatic charge, thereby protecting the gate oxide from breakdown.

**Bias circuit** The dc current biasing is provided by the bias circuit and quiescent current in all stages (except the dynamic current sink) of the CA3140 is dependent upon bias current flow in  $R_1$ . The function of the bias circuit is establishing and maintaining a constant current flow through  $D_1$ ,  $Q_6$ ,  $M_8$  and  $D_2$ . Here,  $D_1$  and  $D_2$  are diode connected transistors.  $D_1$  is connected in parallel with the base-emitter junctions of  $Q_1$ ,  $Q_2$  and  $Q_3$ .  $D_1$  may be considered as a current sampling diode that senses the emitter current of  $Q_6$  and it automatically adjusts the base current of  $Q_6$  (via  $Q_1$ ) to maintain a constant current through  $Q_6$ ,  $M_8$  and  $D_2$ . The base currents in  $Q_2$  and  $Q_3$  are also determined by constant current flow through  $D_1$ . Furthermore, current in diode connected transistor  $Q_2$  establishes the currents in transistors  $Q_{14}$  and  $Q_{15}$ . The combination of  $Q_6$  and  $Q_7$  pair makes the bias current independent of the

power supply voltages. Diodes  $D_1$  and  $D_2$  are diode-connected transistors. The transistor  $Q_1$  and diode  $D_1$  being matched devices make the currents in the two branches of the bias circuit equal, and the value of current is set by  $Q_7$ ,  $R_1$  and  $M_8$ .



**Fig. 13.4** CA3140 BiCMOS op-amp equivalent circuit

**Gain stage** Most of the voltage gain in the CA3140 is provided by the second amplifier stage, consisting of bipolar transistor  $Q_{13}$  and its cascode-connected load resistance provided by bipolar transistors  $Q_3$  and  $Q_4$ . On-chip phase compensation is provided by  $C_1$ , which is found sufficient for a majority of the applications. Additional Miller-Effect compensation can be accomplished by introducing a small capacitor between Terminals 1 and 8. Terminal 8 is also used to strobe the output stage into quiescence condition. When Terminal 8 is tied to the negative supply point at Terminal 4, the output Terminal 6 swings low, i.e. approximately to Terminal 4 potential.

**Output stage** The CA3140 series circuits employ a broadband output stage that can sink loads to the negative supply to complement the capability of the PMOS input stage while operating near the negative rail. Quiescent current in the emitter-follower cascade circuit ( $Q_{17}$ ,  $Q_{18}$ ) is established by transistors ( $Q_{14}$ ,  $Q_{15}$ ) whose base currents are *mirrored* to current flowing through diode  $D_2$  in the bias circuit

section. When CA3140 operates such that the output Terminal 6 is sourcing current, the transistor  $Q_{18}$  functions as an emitter-follower for sourcing current from the positive supply ( $V^+$  at Terminal 7) via  $D_7$ ,  $R_9$ , and  $R_{11}$ . Under these conditions, the collector potential of  $Q_{13}$  is sufficiently high to permit the necessary flow of base current to emitter follower  $Q_{17}$  which, in turn drives  $Q_{18}$ .

When CA3140 operates such that the output Terminal 6 is sinking current to the negative supply ( $V^-$ ) bus, the transistor  $Q_{16}$  acts as the current sinking element. Transistor  $Q_{16}$  is mirror-connected to  $D_6$ ,  $R_7$  with current fed by way of  $M_{21}$ ,  $R_{12}$  and  $Q_{20}$ . The transistor  $Q_{20}$ , in turn, is biased by current flow through  $R_{13}$ , Zener  $D_8$  and  $R_{14}$ . The dynamic current sink is controlled by voltage level sensing. The output Terminal 6 is quiescently established at the potential midpoint between the  $V^+$  and  $V^-$  supply rails. When output current-sinking mode operation is required, the collector potential of transistor  $Q_{13}$  is driven below its quiescent level, thus causing  $Q_{17}$ ,  $Q_{18}$  to decrease the output voltage at Terminal 6. Therefore, the gate terminal of PMOS transistor  $Q_{21}$  is displaced towards the negative supply, thereby reducing the channel resistance of  $Q_{21}$ . As a consequence, there is rise in the current flow through  $Q_{20}$ ,  $R_{12}$ ,  $Q_{21}$ ,  $D_6$ ,  $R_7$ , and the base of  $Q_{16}$ . As a result,  $Q_{16}$  sinks current from Terminal 6 in response to the incremental change in output voltage caused by  $Q_{18}$ . This sink current flows regardless of load, and any excess current is internally supplied by the emitter-follower formed by  $Q_{18}$ . Short circuit protection of the output circuit is provided by  $Q_{19}$  that is driven into conduction by the high voltage drop developed across  $R_{11}$  under output short-circuit conditions. Then, the collector of  $Q_{19}$  diverts current from  $Q_4$  thereby reducing the base current drive from  $Q_{17}$  and limiting current flow in  $Q_{18}$  to the short circuited load terminal.

### 13.3.3 DC Analysis

The basic bias circuit of CA3140 BiCMOS op-amp is shown in Fig. 13.5. The current mirror formed by the matched devices  $Q_1$  and  $D_1$  ensures that the two branch currents  $I_1$  and  $I_2$  are equal. The  $P$ -channel MOSFET  $M_8$  is to operate in saturation region. Hence, it is necessary to satisfy the condition

$$V_{SD} > V_{SG} - |V_{Th}| \quad (13.7)$$

From Fig. 13.5, we find

$$V_{SG} = V_{SD} + |V_D|$$

i.e.  $V_{SD} = V_{SG} - |V_D|$  (13.8)

From the above two equations, we have

$$V_{SG} - V_D > V_{SG} - |V_{Th}| \quad (13.9)$$

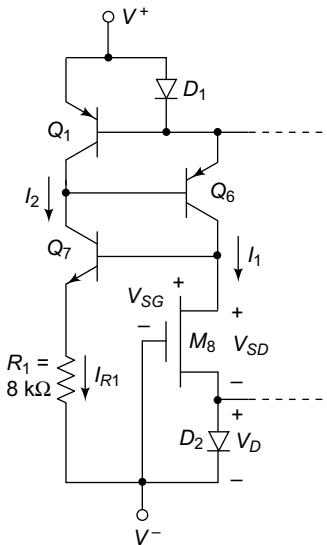
This indicates that  $|V_{Th}| > V_D$ . Here, for  $M_8$  to remain biased in the saturation region, the magnitude of the threshold voltage must be greater than the diode voltage.

From the left side of the bias circuit, the current is expressed by

$$I_2 \equiv I_{R1} = \frac{V_{SG} - V_{BE7}}{R_1} \quad (13.10)$$

and from the right side of the circuit, we have

$$I_1 = k_p \left( V_{SG} - |V_{Th}| \right)^2 \quad (13.11)$$



**Fig. 13.5** Bias circuit of CA3140 BiCMOS op-amp

Hence, Eqs. (13.10) and (13.11) develop the currents and voltages in this bias circuit.

Transistors  $Q_1$  through  $Q_6$  along with diode  $D_1$  of Fig. 13.4 are all matched devices. Hence,  $I_{C5} = I_{C4}$ . The current in  $D_2$  sets the diode voltage, which also biases  $Q_{14}$  and  $Q_{15}$ .

### 13.3.4 Small-signal Analysis

The small-signal voltage gain of the CA3140 op-amp can be analysed as follows.

**Input stage** The small-signal differential voltage gain for the CMOS op-amp is given by

$$A_d = \sqrt{2k_p I_{Q5}} (r_{o10} \| R_{act1} \| R_{i2}) \quad (13.12)$$

where  $I_{Q5}$  is the bias current supplied by  $Q_2$  and  $Q_5$ ,  $r_{o10}$  is the output resistance seen looking into the drain of  $M_{10}$ ,  $R_{act1}$  is the active load resistance and  $R_{i2}$  is the input resistance of the gain stage.

**Gain stage** The small-signal voltage gain for the second stage is given by

$$|A_{v2}| = g_{m13} (r_{o13} \| R_{o4} \| R_{i3}) \quad (13.13)$$

where  $R_{i3}$  is the input resistance of the output stage and  $R_{o4}$  is the output resistance of  $Q_3$  and  $Q_4$  cascode configuration. The transistor  $Q_{17}$  at the input of the output stage is connected as an emitter-follower which means that  $R_{i3}$  is typically in the range of megohms. The output resistance  $R_{o4}$  of the cascode configuration is also typically in the megohm range.

The voltage gain of the second stage is defined by

$$|A_{v2}| \approx g_{m13} r_{o13} \quad (13.14)$$

**Overall gain** The overall voltage gain of the IC is the product of the values of individual gain factors as given by

$$A_v = A_d A_{v2} A_{v3} \quad (13.15)$$

where  $A_{v3}$  is the voltage gain of the output stage. Assuming  $A_{v3} \approx 1$  for the emitter-follower output stage, then the typical value of the gain of CA3140 op-amp is around 100,000.

### Frequency response

The IC CA3140 op-amp is internally compensated using Miller compensation technique by introducing a dominant pole as in the case of IC 741 op-amp. The feedback capacitor  $C_1$  of 12pF is connected between the collector and base of  $Q_{13}$  as shown in Fig. 13.5. Using Miller's theorem, the effective input capacitance of the second stage is given by

$$C_i = C_1 (|1 + A_{v2}|) \quad (13.16)$$

The low-frequency dominant pole is

$$f_{PD} = \frac{1}{2\pi R_{eq} C_i} \quad (13.17)$$

where  $R_{eq}$  is the equivalent resistance seen between the input node of second stage and ground. This resistance is dominated by the input resistance to  $Q_{13}$ , so that

$$R_{eq} \approx R_{i2} = r_{\pi13} \quad (13.18)$$

### 13.3.5 Specifications of IC CA3140

- MOSFET input stage
- Very high input impedance – 1.5 TΩ (Typical)

- Very low input current –10 pA (Typical) at  $\pm 15V$
- Wide common mode input voltage range
- Output swing complements input common mode range
- Directly replaces industry type 741 in most applications

### Applications

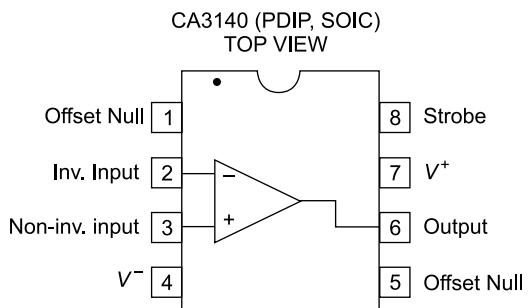
- Ground-Referenced single supply amplifiers in automobile and portable instrumentation
- Sample-and-Hold Amplifiers
- Long duration timers/multivibrators
- Photocurrent Instrumentation
- Peak detectors
- Active filters
- Comparators
- Interface in 5V TTL Systems and Other Low Voltage Systems
- All standard operational amplifier applications
- Function generators
- Tone controls
- Power supplies
- Portable instruments
- Intrusion alarm systems

The pin-out diagram of IC CA3140 is shown in Fig. 13.6.

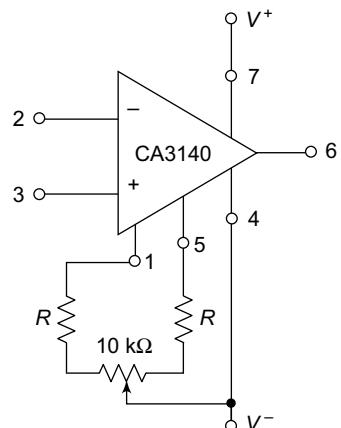
The important features of IC CA3140 with wide dynamic range of input and output characteristics with the most desirable high input impedance characteristics are achieved in CA3140 by the use of its unique design based on the PMOS bipolar process. Input common mode voltage range and output swing capabilities are complementary, allowing operation with the single supply down to 4V. The wide dynamic range of these parameters also means that this device is suitable for many single supply applications, where one input is driven below the potential of terminal 4. The phase sense of the output signal must be maintained, which is one of the most important consideration in comparator applications.

**Output circuit considerations** Excellent interfacing with TTL circuitry is easily achievable with a single 6.2V Zener diode connected to terminal 8. This connection assures that the maximum output signal swing will not go more positive than the Zener voltage minus two base-to-emitter voltage drops within CA3140. These voltages are independent of the supply voltage.

**Offset voltage nulling** The input offset voltage can be nulled by connecting a  $10\text{ k}\Omega$  potentiometer between terminals 1 and 5 and connecting its wiper arm to terminal 4 as shown in Fig. 13.7.



**Fig. 13.6** Pin diagram of CA3140



**Fig. 13.7** Offset voltage nulling

The specifications of BiCMOS op-amp CA3140 is shown in Table 13.1.

**Table 13.1** Specifications of BiCMOS op-amp

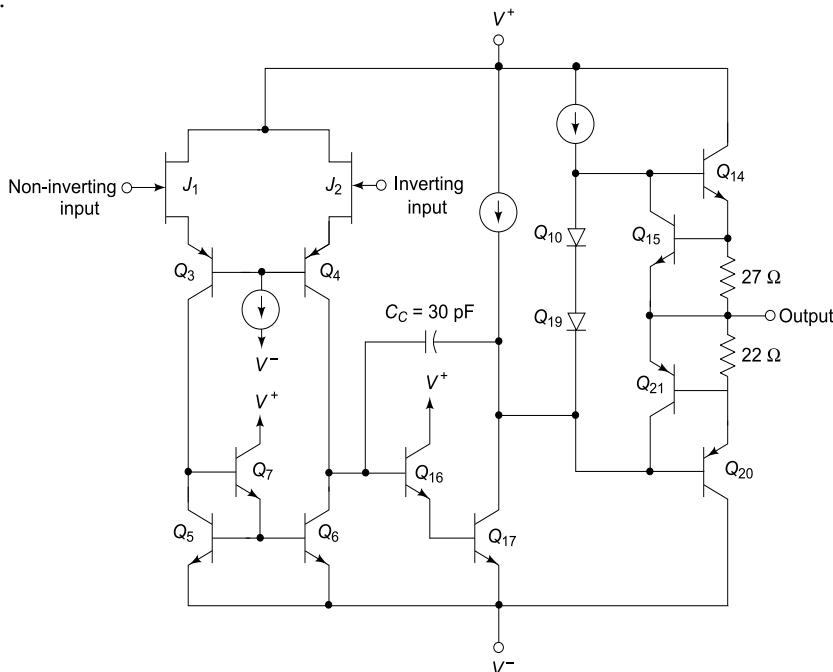
Parameter	Minimum	Typical	Maximum	Units
Input bias current		10		pA
Open-loop gain	20000	100000	50	V/V
Unity-gain frequency		4.5		MHz

## 13.4 JFET OPERATIONAL AMPLIFIERS

The important advantage of employing MOSFETs as input devices in a BiCMOS op-amp is that extremely small input bias currents can be achieved. However, MOSFET gates at outside terminals of an IC are to be protected against electrostatic damage. Typically, this is accomplished by using back-biased diodes on the input, as was shown in Fig. 13.4. Unfortunately, the input op-amp bias currents are then determined by the leakage currents of the protection diodes. This means that small input bias currents cannot be fully realised. JFETs as the input devices also provide the advantage of achieving low input currents, and they do not necessitate the use of electrostatic protection devices also. Input gate currents in a JFET are usually less than 1 nA, and are often of the order of 10 pA. Additionally, the JFETs offer greatly enhanced noise properties.

### 13.4.1 Hybrid FET Operational Amplifier LH0022/42/52 Series

Figure 13.8 shows a simplified circuit diagram of the IC LH0022/42/52 series of op-amps. It uses a pair of JFETs as the input differential pair and general layout of circuit is essentially the same as that of the popular 741 op-amp.



**Fig. 13.8** Equivalent circuit diagram of LH0022/42/52 series JFET Op-Amps

The input differential amplifier stage consists of transistors  $J_1$ ,  $J_2$ ,  $Q_3$  and  $Q_4$  with the N-channel JFETs  $J_1$  and  $J_2$  operating as source-follower. The differential output signal of  $J_1$  and  $J_2$  acts as input to the common-base amplifier constructed by  $Q_3$  and  $Q_4$ , and they provide a large voltage gain. Transistors  $Q_5$ ,  $Q_6$  and  $Q_7$  operate as the active load for the input stage.

The gain stage comprises  $Q_{16}$  and  $Q_{17}$  connected in Darlington pair configuration. This stage also houses a 30pF compensation capacitor. The output stage consists of the complementary push-pull emitter-follower circuit of  $Q_{14}$  and  $Q_{20}$ . Transistors  $Q_{14}$  and  $Q_{20}$  are biased slightly *on* by diodes formed by  $Q_{10}$  and  $Q_{19}$  for minimising the crossover distortion. Transistors  $Q_{15}$  and  $Q_{21}$  and the associated 27 $\Omega$  and 22 $\Omega$  resistors provide the short-circuit protection.

The specifications of LH0042C op-amp is shown in Table 13.2. The very large differential-mode input resistance and the low input bias currents of the JFET op-amp can be noted.

**Table 13.2** Specifications of LH0042C op-amp

Parameter	Minimum	Typical	Maximum	Units
Input bias current		15	50	pA
Differential-mode input resistance		$10^{12}$		$\Omega$
Input capacitance		4		pF
Open-loop gain ( $R_L = 1\text{ k}\Omega$ )	25000	100000		V/V
Unity-gain frequency		1		MHz

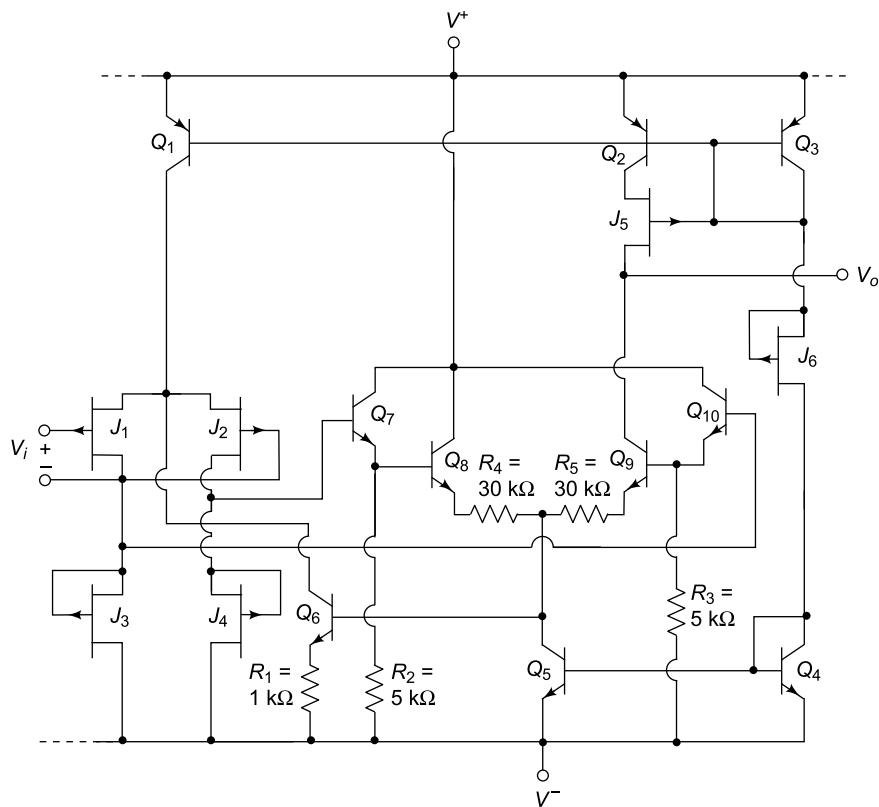
### 13.4.2 Hybrid FET Op-Amp LF155 Series

Another typical model of an op-amp using JFET is the IC LF155. A simplified circuit diagram of the IC is given in Fig. 13.9. The input stage of the BiFET op-amp consists of *P*-channel JFETs  $J_1$  and  $J_2$  biased by the bipolar transistor  $Q_1$ . The active load for the input differential amplifier consists of the *P*-channel JFETs, namely,  $J_3$  and  $J_4$  with  $V_{GS} = 0$ . A two-sided output from the input diff-amp stage is connected to a second diff-amp stage comprising the Darlington pairs  $Q_7$  through  $Q_{10}$ . The gain stage is biased by bipolar transistor  $Q_5$ . The cascode configuration of  $J_5$  and  $Q_2$  act as the active load for the gain stage.

The circuit uses a common-mode feedback loop in the bias circuit. The base drive for  $Q_6$  is applied from the collector of  $Q_5$ . When the drain voltages of  $J_1$  and  $J_2$  go high, the Darlington second stage provides more drive for the base voltage of  $Q_6$ . The current in  $Q_6$  then rises, reducing the drain currents in  $J_1$  and  $J_2$ , since  $I_{C1}$  is constant. Smaller drain currents cause the voltages at  $J_1$  and  $J_2$  to decrease, which stabilises the drain voltages.

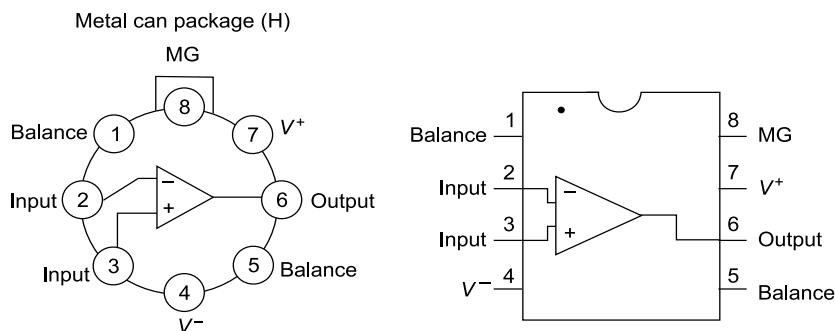
JFET  $J_6$  operates as a current source establishing a reference current in  $Q_3$ ,  $Q_4$  and  $J_6$ . The reference current produces the bias currents in the current mirrors ( $Q_4 - Q_5$ ) and ( $Q_1 - Q_2 - Q_3$ ).

In this BiFET op-amp, the advantages of both JFET and bipolar transistors are found. The JFET input devices provide very high input impedance, normally in the range of  $10^{12}$  ohms. The current-connected transistor  $J_6$  allows the reference bias current to be monitored without the use of a resistor. Use of the bipolar transistors in the second stage provides higher transconductance values as compared to JFETs, thereby achieving a higher second-stage gain.

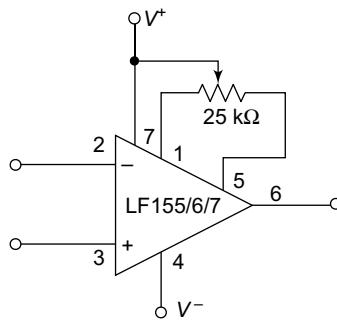


**Fig. 13.9** Equivalent circuit of LF155 BiFET op-amp input stage

The pin diagrams of 8-pin CAN package and DIP of IC LF155 are shown in Fig. 13.10. The circuit arrangement for offset null adjustment is shown in Fig. 13.11. The offset adjustment is made using a 25 kΩ potentiometer with the wiper connected to the positive supply at Pin 7. For potentiometer with temperature coefficient of 100 ppm/°C or less, the additional drift component is required to be adjusted as  $\approx 0.5 \text{ mV/}^{\circ}\text{C}/\text{mV}$ . The typical overall drift is around 5 mV/°C.



**Fig. 13.10** Pin diagrams of IC LF155



**Fig. 13.11** Offset Null adjustment of IC LF155

The specifications of the IC LF155A, LF156A and LF157A series are

- Low input bias current of 30 pA
- Low input offset current of 3 pA
- High input impedance of the order of  $10^{12} \Omega$
- Low input offset voltage of 1 mV
- Low input offset voltage temperature drift of value 3 mV/ $^{\circ}\text{C}$
- Low input noise current to the tune of  $0.01 \text{ pA}/\sqrt{\text{Hz}}$
- High common-mode rejection ratio up to 100 dB
- Large dc voltage gain of 106 dB

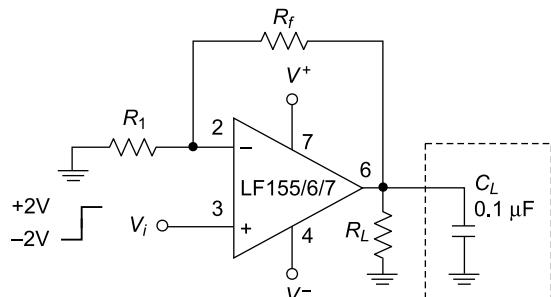
The advantages of LF155A, LF156A and LF157A are:

- It is inexpensive
- It is rugged and allow free handling compared against MOSFET input devices
- Can be used with photocell amplifiers, sample and hold circuits and for low noise applications using either high or low source impedance values and very low 1/f corner frequencies
- It has an offset adjustment facility that does not degrade the drift or common-mode rejection capability
- It can drive large output capacitive loads of around 5,000 pF
- It contains internal compensation and large differential input voltage capability

The LF155/6/7 series of devices have large reverse breakdown voltages from gate to source and drain that eliminates the need of the use of clamps across the inputs. Therefore, even large differential input voltages can be easily handled without a large increase in input current. The maximum differential input voltage is independent of the supply voltages.

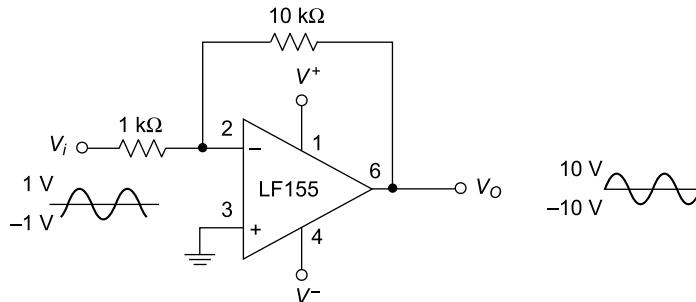
However, care is to be taken so that the input voltages never exceed the negative supply, since this will cause large currents to flow resulting in a destroyed circuit.

The unique output stage design of these op-amps paves way for using these amplifiers for driving large capacitive loads up to  $0.01 \mu\text{F}$  with good stability characteristics with overshoot of a maximum of 20%, settling time of less than 5  $\mu\text{s}$ . A typical circuit arrangement for driving a large capacitive load is shown in Fig. 13.12.



**Fig. 13.12** LF155 Driving a large capacitive load

Figure 13.13 shows the use of LF157 for wideband amplification with distortion less than 1% and a 20 V(pp) output voltage swing and bandwidth of 500 kHz.



**Fig. 13.13** LF157 used as a large power bandwidth amplifier

## 13.5 PROGRAMMABLE TRANSCONDUCTANCE AMPLIFIER (OPERATIONAL TRANSCONDUCTANCE AMPLIFIER)

A voltage to current converter is inherently an amplifier that is capable of producing a current proportional to an applied input voltage. Thus, a voltage to current converter using op-amp is an amplifier which produces an output current that is dependent on the input voltage. The proportionality constant of the circuit is called the *transconductance* of the amplifier circuit, and hence, such circuits are called *transconductance amplifiers*. Due to their wide use in a variety of applications, they are normally called *programmable transconductance* or *operational transconductance amplifiers* (PTA or OTA). Specially designed single chip transconductance amplifier ICs are available in the market. These ICs are widely used in the design of programmable amplifiers and integrators in audio processing and electronic music synthesis applications. They also find use as current switches in sample-and-hold applications. The widely used OTAs are CA3080 from RCA, LMI3600/3700 from National Semiconductor and NE5517 from Signetics.

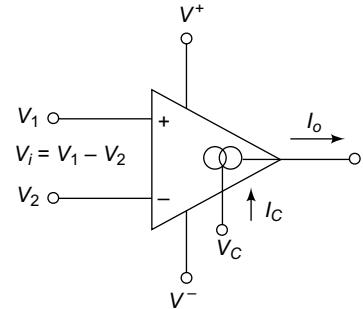
Figure 13.14 shows the schematic representation of an OTA. The constant of proportionality or the *transconductance* is expressed as

$$I_o = g_m V_i = g_m (V_1 - V_2) \quad (13.19)$$

In the programmable transconductance amplifier, the transconductance can be varied by changing the voltage  $V$  or current  $I$ .

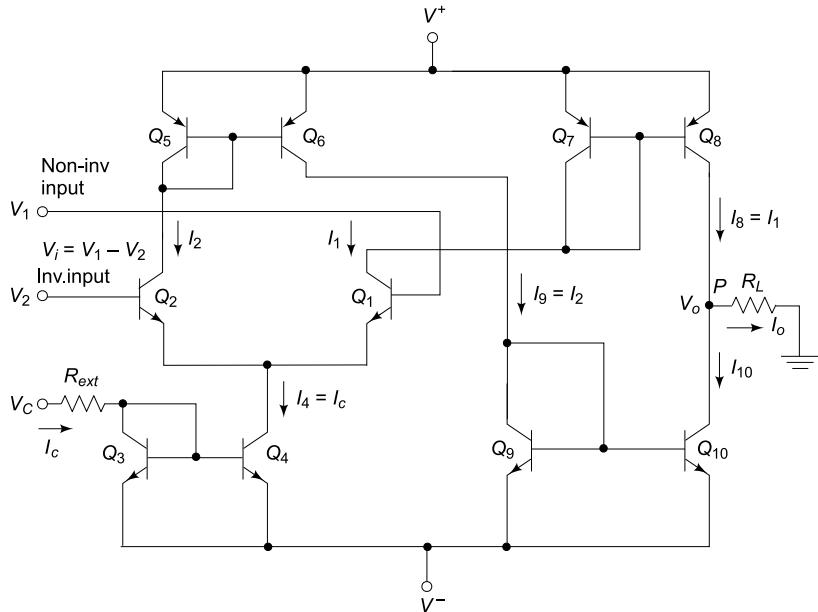
### 13.5.1 Circuit Diagram of OTA

A simplified circuit schematic of an OTA is shown in Fig. 13.15. The transistors  $Q_1$  and  $Q_2$  form a differential input pair. The current mirror formed by the transistors  $Q_3 - Q_4$  accept the control current  $I_C$ , that is externally adjustable by an externally connected resistor  $R_{ext}$  with a control voltage  $V_C$ . Due to current mirroring action of  $Q_3 - Q_4$ , the current  $I_4 = I_C$ . The current  $I_4$  is divided at the emitter terminals



**Fig. 13.14** Schematic representation of an OTA

of  $Q_2$  and  $Q_1$ . Therefore, we have  $I_1 + I_2 = I_4$ . The current mirror formed by  $Q_5$  and  $Q_6$  duplicates  $I_2$  to produce  $I_9 = I_2$ . The current  $I_2$  is replicated again by the current mirror formed by  $Q_9 - Q_{10}$  to offer  $I_9 = I_2 = I_{10}$ . The current mirror  $Q_7 - Q_8$  duplicates  $I_1$  to give  $I_8 = I_1$ .



**Fig. 13.15** Simplified schematic diagram of OTA

Using Kirchhoff's Current Law at output node  $P$ , we get

$$I_o = I_8 - I_{10} = I_1 - I_2$$

Thus, the voltage gain  $A_v$  can be expressed as

$$A_v = \frac{V_o}{V_i} = \frac{I_o R_L}{V_i} = g_m R_L \quad (13.20)$$

The transconductance  $g_m$  of the circuit can be calculated as follows:

$$I_1 = I_S \exp\left(\frac{V_1}{V_T}\right) \quad (13.21)$$

and

$$I_2 = I_S \exp\left(\frac{V_2}{V_T}\right) \quad (13.22)$$

where  $I_S$  is reverse saturation current of transistors  $Q_1$  and  $Q_2$  assumed to be equal and  $V_T$  is thermal voltage of the junction.

$$I_c = I_1 + I_2 = I_S \left[ \exp\left(\frac{V_1}{V_T}\right) + \exp\left(\frac{V_2}{V_T}\right) \right] \quad (13.23)$$

or

$$I_S = \frac{I_c}{\exp\left(\frac{V_1}{V_T}\right) + \exp\left(\frac{V_2}{V_T}\right)} \quad (13.24)$$

$$I_1 = I_S \exp\left(\frac{V_1}{V_T}\right) = \frac{I_C \exp\left(\frac{V_1}{V_T}\right)}{\exp\left(\frac{V_1}{V_T}\right) + \exp\left(\frac{V_2}{V_T}\right)} \quad (13.25)$$

and

$$I_2 = I_S \exp\left(\frac{V_2}{V_T}\right) = \frac{I_C \exp\left(\frac{V_2}{V_T}\right)}{\exp\left(\frac{V_1}{V_T}\right) + \exp\left(\frac{V_2}{V_T}\right)} \quad (13.26)$$

$$I_1 - I_2 = \frac{I_C \left[ \exp\left(\frac{V_1}{V_T}\right) - \exp\left(\frac{V_2}{V_T}\right) \right]}{\exp\left(\frac{V_1}{V_T}\right) + \exp\left(\frac{V_2}{V_T}\right)} \quad (13.27)$$

Multiplying both numerator and denominator by  $\exp\left[-\left(\frac{V_1-V_2}{2}\right)\right]$

$$\begin{aligned} I_o &= I_1 - I_2 = \frac{I_C \left[ \exp\left(\frac{V_1-V_2}{2V_T}\right) - \exp\left(\frac{V_1-V_2}{2V_T}\right) \right]}{\exp\left(\frac{V_1-V_2}{2V_T}\right) + \exp\left(\frac{V_1-V_2}{2V_T}\right)} \\ &= I_C \tan h\left(\frac{V_1-V_2}{2V_T}\right) \end{aligned} \quad (13.28)$$

A plot of output current  $I_o$  as a function of  $(V_1 - V_2)$  is shown in Fig. 13.16. A transconductance amplifier basically computes a *tan-hyperbolic*. It operates linearly for a very small range of inputs and smoothly transits to saturation. The transconductance is given by

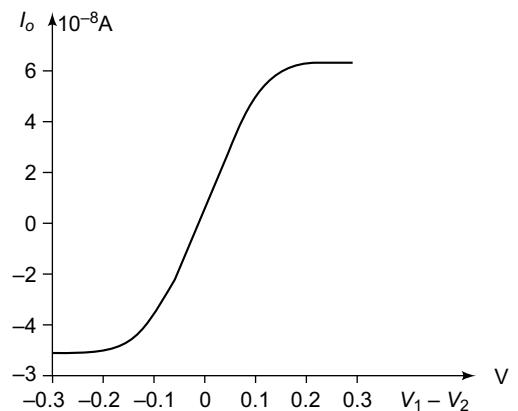
$$g_m = \left| \frac{\partial I_o}{\partial V_{in}} \right| = \frac{I_o}{2 V_T}$$

with the assumption that for small difference of  $V_1 - V_2$ ,

$$\tan h\left(\frac{V_1-V_2}{2V_T}\right) \approx \frac{V_1-V_2}{2V_T}$$

Then, the voltage gain  $A_v$  becomes

$$A_v = g_m R_L = \frac{I_C R_L}{2 V_T} \quad (13.29)$$



**Fig. 13.16** Transfer characteristics of OTA

Thus, the voltage gain of the OTA circuit can be externally controlled by the control current  $I_c$ .

### 13.5.2 Operational Transconductance Amplifier CA3080

Figure 13.17 shows the basic schematic connection of the widely used CA3080 OTA. The transconductance parameter or the gain ( $g_m$ ) of the circuit is controlled by the current  $I_c$  driven into pin 5. At room temperature

$$g_m = \frac{I_c}{2 V_T} = \frac{I_c}{2 \times 26 \text{ mV}} = \frac{19.2}{V} I_c$$

where  $V_T = 26 \text{ mV}$  at room temperature and  $V$  represents Volt as *per unit* indication.

The unit of transconductance  $g_m$  is Siemens. This relationship holds linearly for  $0.1 \mu\text{A} < I_c < 400 \mu\text{A}$ .

It is known that

$$I_o = g_m V_i = g_m (V_1 - V_2)$$

Thus, we can write

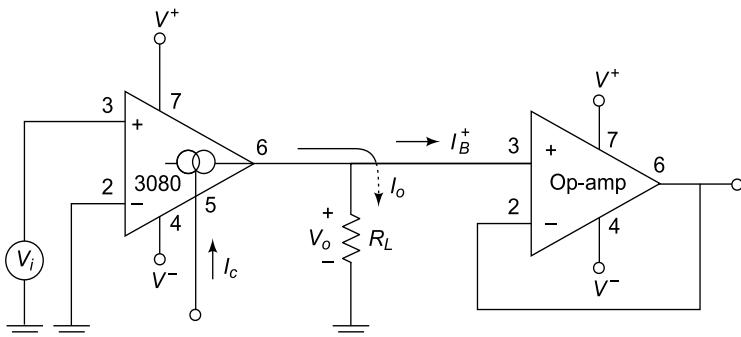
$$I_o = \left( \frac{19.2}{V} I_c \right) V_i \quad (13.30)$$

For IC CA3080, the equation shown is linear for  $I_c < 400 \mu\text{A}$  and  $V_i < 20 \text{ mV}$ . For input voltage values  $V_i$  greater than  $20 \text{ mV}$ , it will no longer remain linear. Therefore, the input voltage should be curtailed to less than  $20 \text{ mV}$  of value. Another limitation is, due to the fact that the input signals are fed directly into the bases of the first stage, it results in input impedances of the order of  $10 \text{ k}\Omega$  to  $30 \text{ k}\Omega$  only. Hence, normally voltage followers using op-amp should be used to avoid loading or to buffer the input signals, thereby producing better impedance matching characteristics.

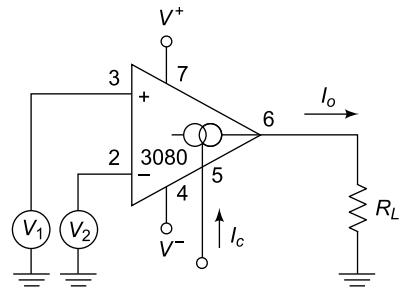
### 13.5.3 Basic OTA Voltage Amplifier

A basic OTA voltage amplifier is shown in Fig. 13.18. At room temperature, the output current is  $I_o = (19.2 I_c) V_i$  per Volt. Assuming the entire  $I_o$  flows into the load resistor  $R_L$  (i.e.  $I_B^+ \ll I_o$ ), then the voltage  $V_o$  across  $R_L$  is given by

$$V_o = I_o R_L = \left( \frac{19.2 I_c}{V} \right) V_i R_L$$



**Fig. 13.18** Basic OTA voltage amplifier circuit



**Fig. 13.17** Schematic of CA3080 OTA

From the above equation, it is observed that the output voltage is determined by the input  $V_i$  and the load resistor  $R_L$ . The voltage gain can be varied by changing  $R_L$ . Normally, a voltage follower is used to avoid loading effects and the voltage buffer is preferred to have the bias current ( $I_B^+$ ) much smaller than the value of  $I_o$ . The output is also determined by the control current  $I_c$ . Figure 13.19 shows various ways of setting the control current  $I_c$ . Figure 13.19(a) shows a fixed current  $I_c$  obtained by connecting a resistance  $R_{ext}$  between the terminal 5 and ground, whose control current  $I_c$  can be written as,

$$I_c = \frac{|V^-| - 0.6 \text{ V}}{R_{ext}}$$

where 0.6 V is the forward voltage drop of the diode connected transistor  $Q_3$  of Fig. 13.19(b). It shows the  $I_c$  controlled by a control voltage  $V_c$  where the value of  $I_c$  is given by

$$I_c = \frac{V_c + |V^-| - 0.6 \text{ V}}{R_{ext}}$$

The control current  $I_c$  can also be set directly with the use of a current source as shown in Fig. 13.19(c). The current source can be constructed with an FET, a BJT or an op-amp based one or an IC current source such as another 3080 connected as a current source.

The OTA can also realise a programmable resistor whose resistance is set by the control current  $I_c$  and the resistance is obtained by

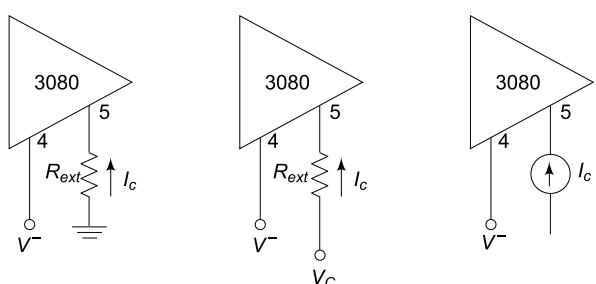
$$R = \frac{V_i}{I_o} = \frac{V}{19.2 I_c} = \frac{10.3 \times 10^{-3}}{I_c}.$$

This gives

$$I_o = \frac{19.2}{V} I_c V_i$$

and

$$R = \frac{V_i}{I_o} = \frac{V}{19.2 I_c} = \frac{10.3 \text{ mV}}{I_c} \quad (13.31)$$



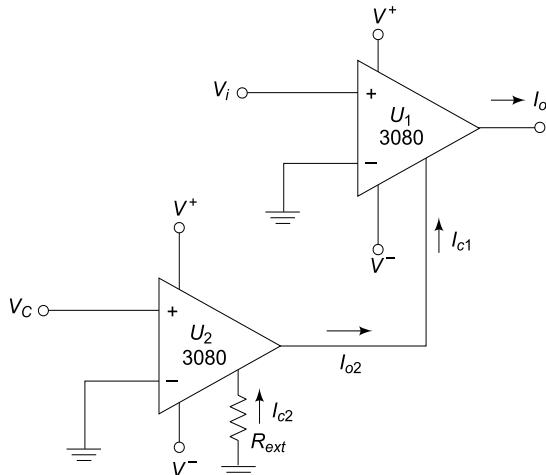
**Fig. 13.19** Circuits for setting control current  $I_c$  using  
 (a) Grounded connection,  
 (b) Control voltage,  
 (c) Current source

### 13.5.4 Electronically Tuned Resistor using OTAs

Figure 13.20 shows an electronically tuned resistor using two OTAs. The resistance expression for the circuit can be arrived at as given by the following:

$$\begin{aligned} \text{For } U_2, \quad I_{c2} &= \frac{|V^-| - 0.6 \text{ V}}{R_{ext}} \approx \frac{|V^-|}{R_{ext}} \\ \text{or} \quad I_{c1} &= I_{o2} = \frac{19.2}{V} \times I_{c2} \times V_c = \frac{19.2}{V} \times \frac{|V^-| - 0.6 \text{ V}}{R_{ext}} \\ \text{For } U_1, \quad I_{c1} &= I_{o2} \\ \text{and} \quad I_o &= \frac{19.2}{V} I_{c1} V_i \end{aligned} \quad (13.32)$$

$$\begin{aligned}
 &= \left( \frac{19.2}{V} \right) \left[ \left( \frac{19.2}{V} \right) \frac{|V^-|}{R_{ext}} V_c \right] V_i \\
 &= \left[ \left( \frac{19.2}{V} \right)^2 \frac{|V^-|}{R_{ext}} \right] V_c V_i \\
 R = \frac{V_i}{I_o} &= \frac{R_{ext}}{(369/V^2)|V^-|V_c} \tag{13.33}
 \end{aligned}$$

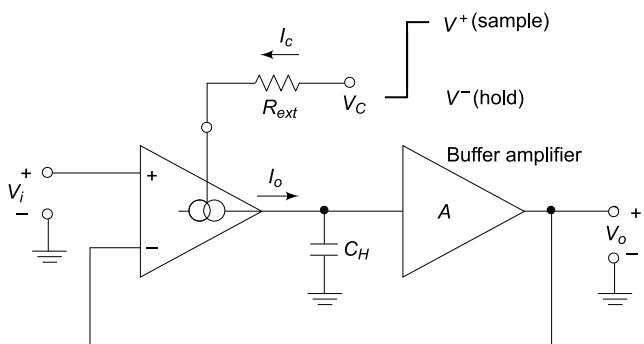


**Fig. 13.20** Electronically tunable resistor using two OTAs

Therefore, the circuit of Fig. 13.20 can be considered as a voltage controlled resistance whose value is set in accordance with the equation shown above. However,  $V_i$  must be limited to be less than 20 mV and  $I_o$  must be less than 400  $\mu$ A.

### 13.5.5 Sample-and-Hold Circuit using OTA

The application of operational transconductance amplifier in sample-and-hold circuit is shown in Fig. 13.21. The control terminal is biased to ON ( $= V^+$ ) and OFF ( $= V^-$ ) conditions for sampling and holding the input signal across a holding capacitor  $C_H$  for a voltage equal to  $V_i$ . During the hold mode, the control voltage  $V_c$  is kept high or at  $V^+$ , and the output from the transconductance amplifier charges the holding capacitor  $C_H$  for a voltage equal to  $V_i$ . During the hold mode,  $I_c$  is reduced to zero and the output of the OTA is virtually an open circuit such that the sampled input voltage is held on to the holding capacitor  $C_H$ . The decay of the voltage available across  $C_H$  during the hold mode depends on the output impedance offered by the OTA and the input resistance of the buffer stage.



**Fig. 13.21** Sample-and-hold circuit using OTA

The basic disadvantage of OTA is the severe restrictions imposed on the voltage and current magnitudes obtainable. Another limitation is that when the control current  $I_c$  is adjusted to vary gain or resistance, many other parameters of the amplifier such as offset voltage, input bias current and slew rate are also disturbed unwarranted. These limitations can be overcome by the use of input and output buffers and frequency compensating techniques. Temperature also affects the performance of the OTA with the proportionality constant of 10.2 per Volt which is valid only for room temperature applications. It may be noted that the OTA performance depends on temperature.

### 13.5.6 Active Filters using Operational Transconductance Amplifier

The OTA can be used for constructing active filters due to its good controllability features with voltage-variable control through the  $I_{ABC}$  input. The controlled parameter can be the midband gain of the circuit or OTA-based active filters can employ the external bias setting for locating the critical frequency or 3dB frequency of the filter. The circuit can be designed for independent gain and critical frequency setting also. The shape of the filter response can also be preserved using OTA based filters.

Figure 13.22 shows a simple first-order lowpass filter with one pole corresponding to a roll-off rate of  $-20$  dB/decade. The voltage gain over whole of the frequency range, and the  $-3\text{dB}$  frequency is given by

$$\frac{V_o}{V_i} = \frac{g_m}{sC + g_m} \quad (13.34)$$

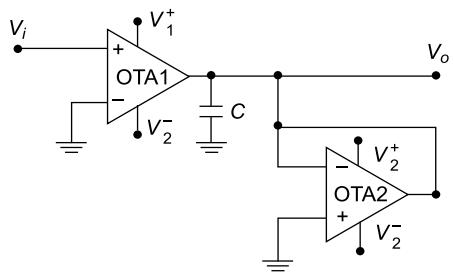
$$f_{3\text{dB}} = \frac{g_m}{2\pi C} \quad (13.35)$$

The OTA 2 shown in the circuit is configured as a voltage variable resistor that sets the variable cut-off frequency.

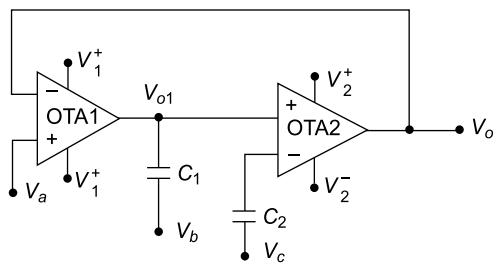
Figure 13.23 shows a second-order filter circuit with three voltage control terminals using OTAs. By selective grounding of two of the terminals, lowpass, highpass, bandpass, or notch filter responses can be realised. The critical or centre frequency can be set by varying the transconductance  $g_m$  of the two OTAs connected in the circuit. These filters are called adjustable frequency constant-Q filters, since they preserve the value of Q even when the critical frequencies are shifted. The general relationship between the output voltage and the three control voltages can be derived as follows:

$$I_{o1} = g_{m1}(V_1^+ - V_1^-) = g_{m1}(V_a - V_{o1})$$

$$V_{c1} = I_{o1}X_{C1} + V_b = V_2^+ = \frac{I_{o1}}{sC_1} + V_b$$



**Fig. 13.22** First order lowpass filter using OTA



**Fig. 13.23** Second order lowpass filter using OTA

$$I_{o2} = g_{m2} \left( V_2^+ - V_2^- \right) = g_{m2} \left( \left( \frac{I_{o1}}{sC_1} + V_b \right) - V_{o1} \right)$$

$$V_{o1} = \frac{I_{o2}}{sC_2} + V_C$$

Substituting  $I_{o2}$  and  $I_{o1}$  from above, we get

$$V_{o1} = \frac{g_{m1}g_{m2}(V_a - V_{o1})}{s^2C_1C_2} + \frac{g_{m2}}{sC_2}(V_b - V_{o1}) + V_c$$

Rearranging and solving, we get

$$V_{o1} = \frac{g_{m1}g_{m2}V_a + sC_1g_{m2}V_b + s^2C_1C_2V_C}{s^2C_1C_2 + sC_1g_{m2} + g_{m1}g_{m2}} \quad (13.36)$$

Here,  $I_{o1}$  and  $I_{o2}$  are the output currents for the first and second OTAs respectively. A specific type of filter can be obtained with the use of the following settings:

- Set  $V_i = V_a$  and have  $V_B$  and  $V_C$  grounded.
- Set  $g_{m1} = g_{m2} = g_m$ .
- Divide by  $C_1C_2$  in both numerator and denominator for achieving a standard biquadratic form.

Hence,

$$\frac{V_{o1}}{V_a} = \frac{\frac{g_m^2}{C_1C_2}}{s^2 + \frac{sg_m}{C_2} + \frac{g_m^2}{C_1C_2}}$$

This expression can be written in the form of the standard biquadratic circuit.

$$\frac{V_{o1}(s)}{V_a(s)} = \frac{\omega_o^2}{s^2 + s\left(\frac{\omega_o}{Q}\right) + \omega_o^2}$$

Therefore, the circuit with a particular control voltage settings represents a lowpass filter whose critical frequency is

$$f_o = \frac{g_m}{2\pi\sqrt{C_1C_2}}$$

and a constant  $Q = \sqrt{\frac{C_2}{C_1}}$ .

The following transfer functions can also be obtained from the control voltage settings as given by

- $V_i = V_b$ ;  $V_a$  and  $V_c$  grounded  $\Rightarrow$  Bandpass filter.
- $V_i = V_c$ ;  $V_a$  and  $V_b$  grounded  $\Rightarrow$  Highpass filter.
- $V_i = V_a = V_c$ ;  $V_b$  grounded  $\Rightarrow$  Notch filter.

## SUMMARY

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- ❑ CMOS op-amps are normally designed for particular on-chip applications, wherein only a few picofarads of capacitive loads are required to be driven. Therefore, most of the CMOS op-amps do not require a low resistance output stage.
- ❑ MC14573 consists of four op-amps configured using CMOS devices in a monolithic structure.
- ❑ Typical op-amp slew rate (SR) achievable for MC14573 is  $SR \approx 0.04 I_{set}$ .
- ❑ The MC14574 and MC14575 are quad op-amps and comparators, and they are used as building blocks for consumer, industrial, automotive and instrumentation applications. Other applications of these ICs are in active filters, voltage reference circuits, waveform generator circuits, ADCs and comparator circuits.
- ❑ BiFET (BiMOS) op-amps use FET as input stage that result in very high input impedance.
- ❑ The equivalent noise of the BiFET input stage may be greater than that of an all-BJT op-amp.
- ❑ FET differential input stages offer higher differential mode resistance, lower input current, reduced input offset currents and higher slew rates.
- ❑ BiFET (BiMOS) op-amps normally constitute three gain stages, viz. a differential amplifier input stage, two gain stages with the level-shifters and an emitter-follower output stage.
- ❑ CA3140 op-amp consists of three basic stages of the input differential stage, the gain stage and the output stage.
- ❑ Typical values of the gain for CA3140 op-amp are around 100,000.
- ❑ CA3140 op-amp is internally compensated using Miller compensation technique and the low-frequency dominant pole is  $f_{PD} = \frac{1}{2\pi R_{eq} C_i}$ .
- ❑ Some of the applications of CA3140 are
  - Ground-Referenced single supply amplifiers in automobile and portable instrumentation
  - Sample-and-Hold Amplifier
  - Long duration timers/multivibrators
  - Photocurrent Instrumentation
  - Peak detectors and comparators
  - Active filters
  - Function generators
  - Portable instruments
  - Intrusion alarm systems
- ❑ The input offset voltage can be nulled by connecting a  $10\text{ k}\Omega$  potentiometer between Terminals 1 and 5.
- ❑ MOSFET gates at outside terminals of an IC are to be protected against electrostatic damage.
- ❑ JFET op-amps have very large differential-mode input resistance and low input bias currents.
- ❑ The JFET input devices provide very high input impedance, normally in the range of  $10^{12}$  ohms.
- ❑ LF155/6/7 series are op-amps with JFET inputs having large reverse breakdown voltages from gate to source and drain that eliminates the use of clamps across the inputs.
- ❑ LF157 can be used for wideband amplification of 500 kHz with distortion less than 1% and a 20 Vp-p output voltage swing.
- ❑ Transconductance amplifiers produce an output current that is dependent on the input voltage with the proportionality constant of the circuit called the transconductance.
- ❑ The widely used OTAs are CA3080 from RCA, LMI3600 / 3700 from National semiconductor and NE5517 from Signetics.
- ❑ The constant of proportionality or the transconductance is expressed as  $I_o = g_m V_i = g_m(V_1 - V_2)$ .
- ❑ The voltage gain A is  $A_v = g_m R_L = \frac{I_c R_L}{2 V_T}$ .

- OTA can also realise a programmable resistor whose resistance is set as given by  $R = \frac{V_i}{I_o} = \frac{V}{19.2I_o} = \frac{10.3 \text{ mV}}{I_c}$ .
- The OTA performance depends on temperature. Some of its applications are voltage amplifiers, electronically tunable resistor, Sample-and-Hold circuits and active filters using OTA.

## REVIEW QUESTIONS

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1. What are the important features of CMOS op-amps?
2. What are the advantages of CMOS op-amps over BJT op-amps?
3. List the features of IC MC14573.
4. Explain the operation of IC MC14573.
5. What are the important stages of CMOS IC?
6. Perform the dc and ac analysis of IC MC14573.
7. What are BiFET and BiMOS circuits? Compare the features with BJT and CMOS op-amps.
8. Explain the three stage architecture of a BiMOS op-amp with a neat diagram.
9. What are the stages of IC CA3140 BiCMOS op-amp? Explain their functions.
10. Explain the active load used for the input differential amplifier stage of IC CA3140.
11. How is offset null provided in IC CA3140?
12. What is the need of a bias circuit?
13. Explain the dynamic current sink circuit of IC CA3140.
14. Perform the dc and ac analysis of IC CA3140.
15. Comment on the Miller compensation achieved in IC CA3140.
16. List the important specifications of IC CA3140.
17. What are the normal applications of IC CA3140?
18. List the features and advantages of JFET op-amps.
19. Draw the equivalent circuit of LH0022/42/52 series JFET op-amps and explain the operation.
20. List the features of hybrid op-amp LF155 series.
21. How is the offset null adjustment arrangement different in IC LF155? Draw the circuit and explain.
22. What are the advantages of LF155 op-amp?
23. Draw a circuit using LF155 for driving a large capacitive load and explain.
24. Draw the circuit of a large power bandwidth op-amp using LF157 and explain its operation.
25. What is a transconductance amplifier?
26. Why are the programmable transconductance amplifiers called so?
27. Draw the simplified schematic diagram of OTA and explain how the voltage gain is achieved.
28. Explain how to control the voltage gain of OTA externally?
29. Explain a basic voltage amplifier using the OTA CA3080 with circuit diagram.
30. Draw the various arrangements for setting the control current for OTA applications.
31. How is an electronically tunable resistor configured using OTAs and explain with a neat diagram.
32. Draw a sample-and-hold circuit using OTA and explain the operation.
33. What are the advantages and disadvantages of OTA?
34. Explain the operation of first order active filter using OTA with a neat circuit diagram.
35. Explain the operation of second order active filter using OTA with a neat circuit diagram.
36. What are the advantages of obtaining an active filter using OTA over the use of general purpose op-amps?

# Simulation using PSpice

14

## 14.1 INTRODUCTION

Many computer software packages have been developed to enhance and aid in the design and analysis of electronic circuits. SPICE, an acronym for Simulation Program with Integrated Circuit Emphasis, is a very important, powerful and the most widely used computer programs for the simulation of electrical and electronic circuits. Since any change in the IC design at a later stage of fabrication is expensive, the design procedure using SPICE in the prefabrication phase is very important and it can minimise the design error as well as cost.

The circuits for simulation may consist of resistors, capacitors, inductors, mutual inductors along with independent and dependent voltage and current sources, lossless and lossy transmission lines, switches, uniformly distributed RC lines, and the most common semiconductor devices, namely, diodes, BJTs, JFETs, MESFETs and MOSFETs. These are available as built-in models, and the user is needed to specify only the important model parameter values with the model name. This chapter introduces the basic capabilities of one of the SPICE tools, namely, the PSpice, where the prefix *P* stands for personal computer. It can perform nonlinear dc, nonlinear transient, linear ac analysis and other types of simulations.

## 14.2 OVERVIEW OF THE SPICE

The development of SPICE covers a period of around 30 years. During the mid-1960s, the program ECAP developed at IBM served as the starting point of the development of program CANCER at the University of California (UC) at Berkeley in late 1960s. Based on CANCER, SPICE was developed at Berkeley in the early 1970s. SPICE2 is an improved version of SPICE that was developed during the mid-1970s at UC-Berkeley.

The algorithms of SPICE2 are general in nature as given in Section 14.1, and they are robust and powerful for simulating electrical and electronic circuits. The SPICE2 has become a standard industry tool for circuit simulations and the development of SPICE2 was supported by public funds at UC-Berkeley, and the program is in the public domain, available in various versions for the good use of the student community at large and for research applications. SPICE3, which is another variant of SPICE2, is introduced especially for supporting the computer-aided design (CAD) research program at UC-Berkeley. Since it became an industry standard, it is now referred simply as SPICE. The input syntax for SPICE is in a free-format language style, and it does not require data to be entered in fixed column locations, and the syntax and semantic structure of SPICE are easy to follow. SPICE assumes reasonable default values for unspecified circuit parameters, and it performs a considerable amount of error checking to ensure that a circuit has been entered correctly.

PSpice employing the same algorithm as SPICE2 is a member of the SPICE family and it is equally useful for simulating all types of circuits in a wide range of applications. In both PSpice and SPICE, a circuit is submitted by statements that are stored in a file called the circuit file or the netlist file, where the circuit elements are identified by the models of the elements connected between the marked nodes. The circuit file is read by the SPICE simulator. Each statement is a self-contained and independent one and the statements do not interact with each other. SPICE (or PSpice) statements are easy to learn, decipher and employ. A schematic editor can be used to draw the circuit and create a schematic file, which can then be exported as a netlist to PSpice for running the simulation.

### 14.2.1 Types of SPICE

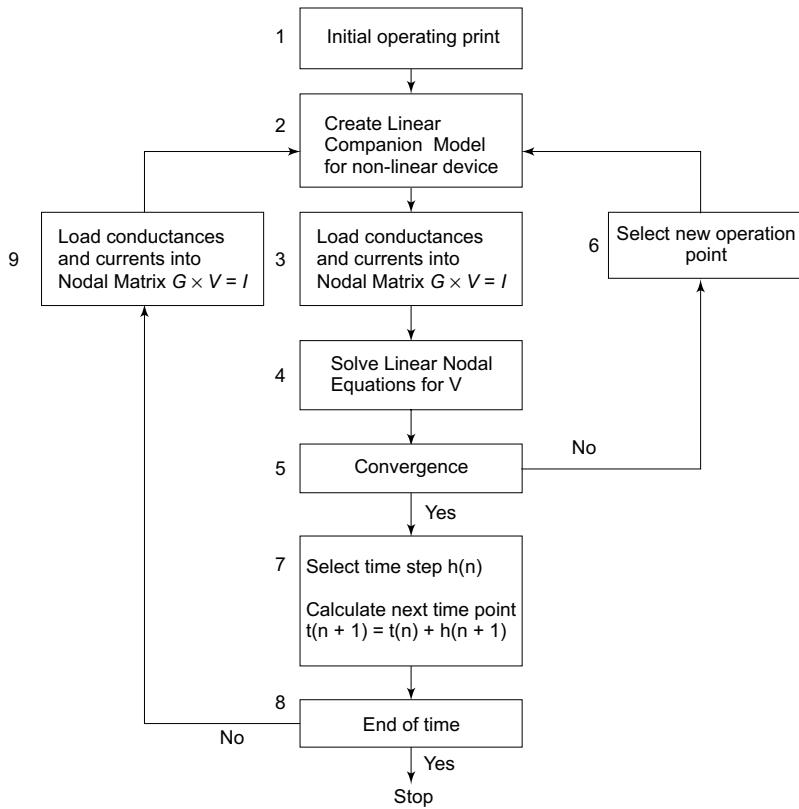
Many versions of SPICE are available in the market for the student community and for industrial applications at large. A person familiar with any one SPICE software can work with any other version of SPICE software easily. Some of the SPICE software are:

- HSPICE from Synopsis designed for IC design with models derived from the specific foundries
- PSpice from MicroSim – One of the most widely used computer programs for analog circuit analysis which works with Windows, Linux, OS/2, Macintosh and UNIX. The evaluation software is downloadable from [www.cadence.com/orcad/](http://www.cadence.com/orcad/)
- Cadence Spice from Cadence Design Inc. designed for IC design with models derived from the specific foundries
- IS-SPICE from Intusoft Inc. – which includes SPICE simulation, analog and mixed signal circuit design tools, transformer design and test programme development
- SPICE-Plus from Analog Design Tools
- AIM-Spice – A version of SPICE and is the most popular analog circuit simulator with a student version obtainable from the website [www.aimspice.com](http://www.aimspice.com)
- BSIM3 and BSIM4 from University of California, Berkeley
- Electronics Workbench Software which offers a professional circuit design solution with a library of integrated tools that includes schematic capture, simulation, layout and auto-routing for PCBs and programmable logic devices such as FPGA and CPLD.

The block diagram of the overview of SPICE algorithm is given in Fig. 14.1.

The main features of the algorithm are:

1. The *nodal analysis* forms the heart of any SPICE programming, as indicated by the blocks 3 and 4. This is accomplished by formulating the Nodal Matrix and solving the nodal equations for the circuit parameters.
2. The inner loop consisting of blocks 2 to 6 identifies the solution for *Non-Linear* circuits. The non-linear devices are replaced by equivalent linear models. Much iteration may be needed before the calculations result in *convergence* to the correct solution.
3. The outer loop indicated by steps 7 to 9 along with the inner loop performs a transient analysis, that creates the equivalent linear models for energy-storage components for capacitors, inductors etc. and selecting the appropriate time points.



**Fig. 14.1** Overview of SPICE Algorithm

### 14.3 GENERAL STRUCTURE AND CONVENTIONS

The circuit to be simulated is described in SPICE as a *netlist* with the use of a set of element lines that define the circuit topology or the circuit structure, and the element values to be connected in the circuit. A set of control lines defining the model parameters and the run controls also form a part of the SPICE program or the netlist. The first line always indicates the title or reference to the circuit, and the last line is the end of the program, namely the *.END*. The order of the remaining lines is arbitrary.

Each element in the circuit is identified by an element line that consists of the element name, the nodes of the circuit between which the element is to be connected followed by the value of the parameters determining the electrical characteristics of the circuit element. The first letter such as M, R, C, L, etc. used with the element name specifies the type of element.

The general format for the SPICE element types is given below. All the components start with a particular character. For example, a capacitor name always starts with C, whereas a resistor model always begins with the letter R and the name may contain one or more characters. Hence, R, R1, RSE, ROUT and R3AC2ZY are all valid resistor names. Fields on a line are separated by one or more blank spaces, a comma, an *equal* (=) sign, or a left or right parenthesis, and any extra spaces are ignored. A line may be continued by entering a + (plus) in column 1 of the succeeding line. A *name* field must begin with a letter (A through Z) and it cannot consist of any delimiters. A *number* field may be an integer field, a floating point field or an integer or floating point number followed by an integer exponent or either an integer or a floating point number.

### 14.3.1 Title, End and Comment

#### 1. Title

**Examples:**

*SUMMING AMPLIFIER CIRCUIT*

*ADDER CELL*

This statement is the first card in the input file or the SPICE netlist. Its contents are printed *verbatim* as the heading for each section of output.

#### 2. END

**Example:**

.END

This statement must always be the last line in the input file. The period (.) is an integral part of the name.

#### 3. COMMENT

General form: \* (Followed by the comment text)

**Examples:**

\* *FEED BACK NETWORK*

The asterisk in the first column indicates that this line is a comment line. Comments may be placed anywhere in the circuit description.

### 14.3.2 Brief Summary of Devices and Statements used in SPICE

A brief reference to the devices and some of the statements used in the SPICE software is made below.

The parameters enclosed by braces { } are required to identify the device and the parameter enclosed in square brackets [ ] are optional. Parameters followed by an asterisk { }\* should be repeated as necessary. Each SPICE vendor may have additional parameters and command structures that are unique to their version of SPICE. The commonly used notations by most of the SPICE versions are considered for discussion.

Node names may consist of arbitrary character strings. The datum or the ground node must be named '0'. The circuit cannot contain a loop of voltage sources and/or inductors and cannot contain a cut-set of current sources and/or capacitors. Each node in the circuit must have a dc path to ground. Every node must have atleast two connections except for transmission line nodes (to permit unterminated transmission lines) and MOSFET substrate nodes.

To make it more evident, all the model statements are given in upper case letters.

#### Rules for circuit description

1. Node identifiers or numbers must be non-negative integers.
2. The ground node (0 Volts) must be numbered zero.
3. Device names can be up to 8 characters in length.
4. The first letter of a device name identifies the device type. For example, 'R' for resistor, 'C' for capacitor , 'M' for MOSFET, 'V' for independent voltage source and 'I' for independent current source.
5. Values can be expressed as integers or floating point numbers. The following abbreviations are normally employed:
 

(i) tera: $1 \times 10^{12}$	(iv) kilo: $1 \times 10^3$	(vii) nano: $1 \times 10^{-9}$
(ii) giga: $1 \times 10^9$	(v) milli: $1 \times 10^{-3}$	(viii) pico: $1 \times 10^{-12}$
(iii) mega: $1 \times 10^6$	(vi) micro: $1 \times 10^{-6}$	(ix) femto: $1 \times 10^{-15}$
6. Comments can be inserted into the circuit description by beginning the statement with an asterisk '\*' as the first character

## Element Statements

### 1. Resistors

General form:

*R\_NAME N1 N2 VALUE <TC = TC1, <TC2>>*

#### Examples:

*R1 1 2 100*

*RC1 12 17 1K TC = 0.001, 0.015*

N1 and N2 are the two element nodes. VALUE is the resistance (in ohms) and may be positive or negative but not zero. TC1 and TC2 are the (optional) temperature coefficients; if not specified, zero is assumed for both. The value of the resistor as a function of temperature is given by:

$$\begin{aligned} \text{value}(TEMP) = & \text{value}(TNOM)*(1+TC1*(TEMP-TNOM) \\ & +TC2*(TEMP-TNOM)^{**2})) \end{aligned}$$

### 2. Capacitors and inductors

General form:

*C\_NAME N+ N- VALUE <IC=INCOND>*

#### Examples:

*C1 13 0 1UF*

*CBYPASS 5 7 10U IC=3V*

*LLINK 1 34 1UH*

*LCOIL 3 5 10U IC=15.7mA*

N+ and N- are the positive and negative element nodes, respectively. VALUE is the capacitance in Farads or the inductance in Henries.

For the capacitor, the (optional) initial condition is the initial (time-zero) value of capacitor voltage (in Volts). For the inductor, the (optional) initial condition is the initial (time-zero) value of inductor current (in Amps) that flows from N+ through the inductor, to N-.

**Nonlinear capacitors and inductors can be described in SPICE as follows:**

General form:

*C\_NAME N+ N- POLY C0 C1 C2 ... <IC=INCOND>*

*LYYY N+ N- POLY L0 L1 L2 ... <IC=INCOND>*

C0 C1 C2 ... (and L0 L1 L2 ...) are the coefficients of a polynomial describing the element value. The capacitance is expressed as a function of the voltage across the element, while the inductance is a function of the current through the inductor. The value is computed as

$$\text{value}=C0+C1*V+C2*V^{**2}+\dots$$

$$\text{value}=L0+L1*I+L2*I^{**2}+\dots$$

where V is the voltage across the capacitor and I the current flowing in the inductor.

### 3. Coupled (Mutual) inductors

General form:

*K\_NAME L1 L2 VALUE*

#### Examples:

*K43 LA LB 0.23*

*KX L1 L2 0.3*

*L1* and *L2* are the names of the two coupled inductors, and *VALUE* is the coefficient of coupling, *K*, which must be greater than 0 and less than or equal to 1.

#### 4. Transmission lines (lossless)

General form:

*T\_NAME N1 N2 N3 N4 Z0=VALUE <TD=VALUE> <F=FREQ+<NL=NRMLEN>>*  
*<IC=V1, I1, V2, I2>*

#### Example:

*T1 1 0 2 0 Z0=50 TD=10NS*

N1 and N2 are the nodes at port 1, and N3 and N4 are the nodes at port 2. Z0 is the characteristic impedance. The length of the line may be expressed in either of the two forms. The transmission delay TD may be specified directly (as TD = 10 ns, for example). Alternatively, a frequency F may be given, together with NL, the normalised electrical length of the transmission line with respect to the wavelength in the line at frequency F. If a frequency is specified, and NL is omitted, a value of 0.25 is assumed (i.e., the frequency is assumed to be the quarter-wave frequency). Note that although both forms for expressing the line length are indicated as optional, one of the two must be specified, and also note that, this element models only one propagating mode. If all four nodes are distinct in the actual circuit, then two modes may be excited. To simulate such a situation, two transmission line elements are required. The (optional) initial condition specification consists of the voltage and current at each of the transmission line ports. The SPICE uses a default transient time step, which does not exceed half of the minimum transmission line delay. Therefore, very short transmission lines (compared with the analysis time frame) will cause long run times.

### Sources

#### (a) Linear dependent sources

SPICE allows circuits to contain linear dependent sources characterised by any of the four equations

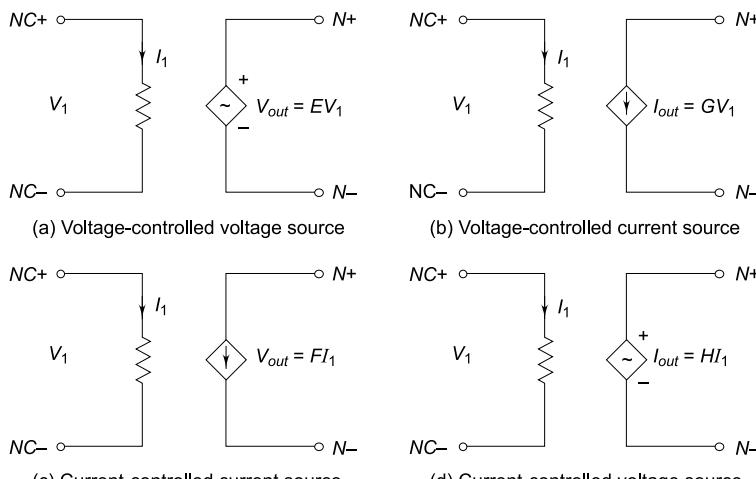
$$I = G*V,$$

$$V = E*V,$$

$$I = F*I,$$

$$V = H*I$$

where *G*, *E*, *F*, and *H* are constants representing transconductance, voltage gain, current gain and transresistance respectively. Figures 14.2(a) to (d) show the dependent sources used in the SPICE software.



**Fig. 14.2** Dependent sources (a) Voltage controlled voltage source

(b) Voltage controlled current source (c) Current controlled current source  
 and (d) Current controlled voltage source

**1. Linear voltage-controlled voltage sources**

General form:

*E\_NAME N+ N- NC+ NC- VALUE*

**Example:**

*E1 2 3 14 1 2.0*

N<sub>+</sub> is the positive node, and N<sub>-</sub> is the negative node. NC<sub>+</sub> and NC<sub>-</sub> are the positive and negative controlling nodes, respectively. VALUE is the voltage gain. The schematic representation is shown in Fig. 14.2(a).

**2. Linear voltage-controlled current sources**

General form:

*G\_NAME N+ N- NC+ NC- VALUE*

**Example:**

*G1 2 0 5 0 0.1MMHO*

N<sub>+</sub> and N<sub>-</sub> are the positive and negative nodes, respectively. Current flow is from the positive node through the source to the negative node. NC<sub>+</sub> and NC<sub>-</sub> are the positive and negative controlling nodes, respectively. VALUE is the transconductance (in mhos). The schematic representation is shown in Fig. 14.2(b).

**3. Linear current-controlled current sources**

General form:

*F\_NAME N+ N- VNAM VALUE*

**Example:**

*F1 13 5 VSENS 5*

N<sub>+</sub> and N<sub>-</sub> are the positive and negative nodes, respectively. Current flow is from the positive node, through the source, to the negative node. VNAM is the name of a voltage source through which the controlling current flows. The direction of positive controlling current flow is from the positive node, through the source, to the negative node of VNAM. VALUE is the current gain. The schematic representation is shown in Fig. 14.2(c).

**4. Linear current-controlled voltage sources**

General form:

*H\_NAME N+ N- VNAM VALUE*

**Example:**

*HX5 17 VZ 0.5K*

N<sub>+</sub> and N<sub>-</sub> are the positive and negative nodes, respectively. VNAM is the name of a voltage source through which the controlling current flows. The direction of positive controlling current flow is from the positive node, through the source, to the negative node of VNAM. VALUE is the transresistance in ohms. The schematic representation is shown in Fig. 14.2(d).

**(b) Independent sources**

General form:

*V\_NAME N+ N- <<DC> DC/TRAN VALUE>  
+<AC <ACMAG <ACPHASE>>>*

*IYYY N+ N- <<DC> DC/TRAN VALUE> <AC <ACMAG +<ACPHASE>>>*

### Examples:

*VCC 10 0 DC 6*

*VIN 13 2 0.001 AC 1 SIN(0 1 1MEG)*

*ISRC 23 21 AC 0.333 45.0 SFFM(0 1 10K 5 1K)*

*VMEAS 12 9 DC 6*

N<sup>+</sup> and N<sup>-</sup> are the positive and negative nodes, respectively. Note that voltage sources need not be grounded. Positive current is assumed to flow from the positive node, through the source, to the negative node. A current source of positive value will force current to flow out of the N<sup>+</sup> node, through the source, and into the N<sup>-</sup> node. Voltage sources, in addition to being used for circuit excitation act as *ammeters* for SPICE. Therefore, zero valued voltage sources may be inserted into the circuit for the purpose of measuring current. They will not have any effect on the circuit operation, since they represent short-circuits.

DC/TRAN is the dc and transient analysis value of the source. If the source value is zero both for dc and transient analyses, this value may be omitted. If the source value is time-invariant (e.g. a power supply), then the value may optionally be preceded by the letters DC.

ACMAG is the ac magnitude and ACPHASE is the ac phase. The source is set to this value in the ac analysis. If ACMAG is omitted following the keyword AC, a value of unity is assumed. If ACPHASE is omitted, a value of zero is assumed. If the source is not an ac small-signal input, then the keyword AC and the ac values are omitted.

Any independent source can be assigned a time-dependent value for transient analysis. If a source is assigned a time dependent value, the time-zero value is used for dc analysis. There are five independent source functions: pulse, exponential, sinusoidal, piece-wise linear and single-frequency FM. If parameters other than source values are omitted or set to zero, the default values will be assumed. TSTEP is the printing increment and TSTOP is the final time.

### 5. Pulse voltage source PULSE (V1 V2 TD TR TF PW PER)

The typical structure of the waveform of a pulse voltage source is shown in Fig. 14.3(a).

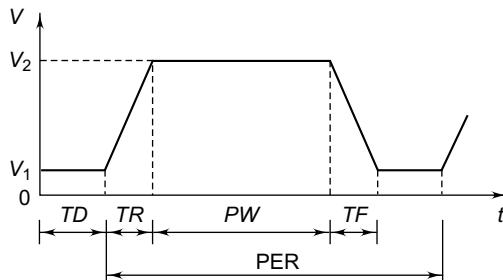
### Examples:

*VIN 3 0 PULSE(-1 1 2NS 2NS 2NS 50NS 100NS)*

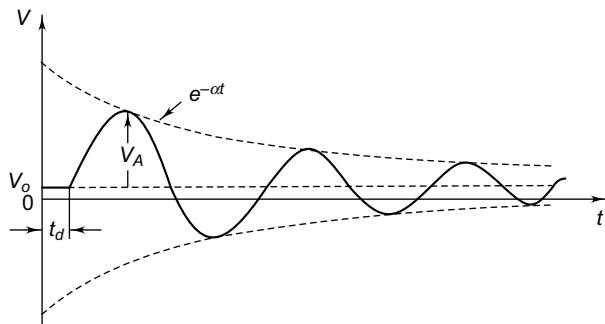
Parameters	Default values	Units
<i>V1 (initial value)</i>		Volts
<i>V2 (pulsed value)</i>		Volts
<i>TD (delay time)</i>	0.0	seconds
<i>TR (rise time)</i>		TSTEP seconds
<i>TF (fall time)</i>		TSTEP seconds
<i>PW (pulse width)</i>		TSTOP seconds
<i>PER(period)</i>		TSTOP seconds

## 6. Sinusoidal voltage source SIN(VO VA FREQ TD THETA)

The typical structure of the waveform of a sinusoidal voltage source is shown in Fig. 14.3(b).



**Fig. 14.3 (a) Pulse waveform**



**Fig. 14.3 (b) Sinusoidal voltage waveform**

Examples:

VIN 3 0 SIN(0 1 100MEG 1NS 1E10)

Parameters	Default value	Units
VO (offset)		Volts
VA (amplitude)		Volts
FREQ (frequency)	1/TSTOP	Hz
TD (delay)	0.0	seconds
THETA (damping factor)	0.0	1/second

## 7. Exponential voltage source EXP (V1 V2 TD1 TAU1 TD2 TAU2)

Examples:

VIN 3 0 EXP(-4 -1 2NS 30NS 60NS 40NS)

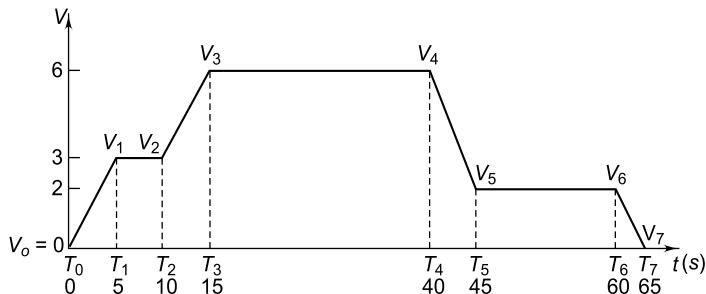
Parameters	Default value	Units
V1 (initial value)		Volts
V2 (pulsed value)		Volts
TD1 (rise delay time)	0.0	seconds
TAU1 (rise time constant)	TSTEP	seconds
TD2 (fall delay time)	TD1+TSTEP	seconds
TAU2 (fall time constant)	TSTEP	seconds

## 8. Piece-wise linear voltage source PWL( $T_1$ , $V_1 \dots$ )

**Example:**

`VSTEP 7 5 PWL (0 0 5s 3 10s 3 15s 6 40s 6 45s 2 60s 2 65s 0)`

The typical structure of the waveform of a piece-wise linear voltage source is shown in Fig. 14.3(c).



**Fig. 14.3 (c) Piece-Wise linear voltage waveform**

**Parameters and default values** Each pair of values ( $T_i$ ,  $V_i$ ) specifies that the value of the source is  $V_i$  (in Volts) at time  $= T_i$ . The value of the source at intermediate values of time is determined by using linear interpolation on the input values.

## 9. Single frequency FM voltage source

`(SFFM(VO VA FC MDI FS)`

**Examples:**

`V1 12 0 SFFM(0 1M 20K 5 1K)`

Parameters	Default value	Units
<i>VO</i> (offset)		Volts
<i>VA</i> (amplitude)		Volts
<i>FC</i> (carrier frequency)	1/TSTOP	Hz
<i>MDI</i> (modulation index)		
<i>FS</i> (signal frequency)	1/TSTOP	Hz

### 14.3.3 Semiconductor Devices

The models for the semiconductor devices that are included in the SPICE program require several parameter values and the devices are often defined by the set of device model parameters. Therefore, a set of device model parameters as given by the fabrication facilities are defined on a separate statement called `.MODEL` statement and it is assigned a unique model name. Each device element statement consists of the device name, the nodes or terminals to which the device is connected and the model name.

#### 1. Junction diode

General form:

`D_NAME N+ N- MNAME <AREA> <OFF> <IC=VD>`

**Examples:**

`DB 2 10 DIODE1`

`DCLMP 3 7 DMOD 3.0 IC=0.2`

$N^+$  and  $N^-$  are the positive and negative terminals of the diode respectively. MNAME is the model name, AREA is the area factor, and OFF indicates an (optional) starting condition on the device for dc analysis. If the area factor is omitted, a default value of 1.0 is assumed. The area factor used on the diode, BJT or JFET device cards determines the number of equivalent parallel devices of a specified model.

## 2. Bipolar Junction Transistor (BJT)

General form:

*Q\_NAME NC NB NE <NS> MNAME <AREA> <OFF> <IC=VBE,VCE>*

### Examples:

*Q2 10 24 13 QMOD IC=0.6, 5.0*

*Q50 11 26 4 20 MOD1*

NC, NB and NE are the collector, base and emitter nodes, respectively. NS is the (optional) substrate node. If unspecified, *Ground* is used. MNAME is the model name, AREA is the area factor, and OFF indicates an (optional) initial condition on the device for the dc analysis. If the area factor is omitted, a value of 1.0 is assumed.

## 3. Junction Field Effect Transistor (JFET)

General form:

*J\_NAME ND NG NS MNAME <AREA> <OFF> <IC=VDS,VGS>*

### Examples:

*J1 7 2 3 JM1 OFF*

ND, NG and NS are the drain, gate and source nodes, respectively.

## 4. Metal Oxide Semiconductor Field Effect Transistor

General form:

*M\_NAME ND NG NS NB MNAME <L=VAL> <W=VAL>  
+ <AD=VAL> <AS=VAL> <PD=VAL> <PS=VAL> <NRD=VAL>  
+ <NRS=VAL> <OFF> <IC=VDS,VGS,VBS>*

### Examples:

*M1 2 5 0 20 TYPE1*

*M3 2 17 7 10 MODN L=5U W=2U*

*M5 2 6 8 20 MODP 5U 2U*

*M1 2 19 13 20 NMOD L=10U W=5U AD=100P AS=100P PD=40U +PS=40U*

ND, NG, NS and NB are the drain, gate, source, and bulk (substrate) nodes, respectively. MNAME is the model name. L and W are the channel length and width, in metres. AD and AS are the areas of the drain and source diffusions, and PD and PS are the perimeter values of the drain and source diffusions in metres.

## 5. .MODEL card

General form:

*.MODEL MNAME TYPE(PNAME1=PVAL1 PNAME2=PVAL2 ... )*

**Example:**

```
.MODEL MOD1 NPN BF=50 IS=1E-13 VBF=50
```

The .MODEL card specifies a set of model parameters that will be used by one or more devices. MNAME is the model name, and type is one of the following seven types:

<i>NPN</i>	<i>NPN BJT model</i>
<i>PNP</i>	<i>PNP BJT model</i>
<i>D</i>	<i>Diode model</i>
<i>NJF</i>	<i>N-channel JFET model</i>
<i>PJF</i>	<i>P-channel JFET model</i>
<i>NMOS</i>	<i>N-channel MOSFET model</i>
<i>PMOS</i>	<i>P-channel MOSFET model</i>

Parameter values are defined by identifying the parameter name for each model type, followed by an *equal* sign and the parameter *value*. Model parameters are assigned the default values, when not mentioned.

## 14.4 BASIC ANALYSES TYPES

### 14.4.1 DC Analysis

The DC analysis is used to evaluate the circuit performance in response to a DC source. DC Analysis is performed either to calculate a DC Operating Point or a DC Sweep. An operating point is required for the initial solution to a transient analysis or as a bias point for an AC analysis. The DC Sweep does exactly as the name implies - performs the DC analysis multiple times, as one sweeps a selected component parameter across a defined range. All energy storage components like capacitors, inductors and semiconductor charge mechanisms are ignored for this analysis.

The dc analysis portion of SPICE determines the dc operating point of the circuit with inductors shorted and capacitors opened. A dc analysis is automatically performed prior to a transient analysis to determine the transient initial conditions, and prior to an ac small-signal analysis to determine the linearized, small-signal models for nonlinear devices. If required, the dc small-signal value of a transfer function (ratio of output variable to input source), input resistance and output resistance can also be computed as part of the dc solution. The dc analysis can also be used to generate dc transfer curves. A specified independent voltage or current source is stepped over a user-specified range and the dc output variables are stored for each sequential source value. If requested, SPICE will also determine the dc small-signal sensitivities of specified output variables with respect to circuit parameters. The dc analysis options are specified on the .DC, .TF, .OP and .SENS control cards. If one desires to see the small-signal models for nonlinear devices in conjunction with a transient analysis operating point, then the .OP card must be provided. The dc bias conditions will be identical for each case, but the more comprehensive operating point information is not available for print, when transient initial conditions are computed.

One of the simpler tasks for SPICE is performing DC analysis on *Linear* circuits. Only two of the blocks are actually needed: Load the Nodal Matrix (3) and solve the Nodal Equations (4) using Gaussian Elimination in the SPICE algorithm. One important point to be noted is that the nodal analysis works for a system of linear equations.

For *Non-Linear* circuits, SPICE needs to create equivalent linear models for the non-linear devices. The loop (blocks 1–6) iteratively finds the exact solution as follows: guess an operating point, create equivalent linear models and solve the nodal matrix for the circuit voltages. Then, choose a new operating

point based on the new voltages and start all over again. The SPICE stops when the changes in circuit voltages and currents have fallen below some limit, from one iteration to the next, and then the solution is said to have converged. This is known as the Raphson-Newton solution of non-linear circuits.

### **.DC**

General form:

```
.DC V1 VSTART VSTOP VINC [SRC2 START2 STOP2 INCR2]
```

#### **Examples:**

```
.DC VIN 0.25 5.0 0.25
```

```
.DC VDS 0 10 .5 VGS 0 5 1
```

```
.DC VCE 0 10 .25 IB 0 10U 1U
```

This statement defines the dc transfer curve source and sweep limits. SRCNAM is the name of an independent voltage or current source. VSTART, VSTOP and VINCR are the starting, final and incrementing values respectively. The first example will cause the value of the voltage source VIN to be swept from 0.25 Volts to 5.0 Volts in increments of 0.25 Volts. A second source (SRC2) may optionally be specified with associated sweep parameters. In this case, the first source will be swept over its range for each value of the second source. This option can be useful for obtaining semiconductor device output characteristics.

### **.TF**

General form:

```
.TF OUTVAR INSRC
```

#### **Examples:**

```
.TF V(5,3) VIN
```

```
.TF I(VLOAD) VIN
```

This command defines the small-signal output and input for the dc small-signal analysis. OUTVAR is the small-signal output variable and INSRC is the small-signal input source. If this statement is included, SPICE will compute the dc small-signal value of the transfer function (output/input), input resistance, and output resistance. For the first example, SPICE would compute the ratio of V(5, 3) to VIN, the small-signal input resistance at VIN, and the small-signal output resistance measured across nodes 5 and 3.

### **.OP**

General form:

```
.OP
```

The inclusion of this command in an input file will force SPICE to determine the dc operating point of the circuit with inductors shorted and capacitors opened. A dc analysis is automatically performed prior to a transient analysis to determine the transient initial conditions, and prior to an ac small-signal analysis to determine the linearized, small-signal models for nonlinear devices.

SPICE performs a dc operating point analysis if no other analyses are requested.

### **.SENS**

General form:

```
.SENS OV1 <OV2 ... >
```

**Example:**

.SENS V(9) V(4,3) V(17) I(VCC)

If a .SENS statement is included in the input netlist, SPICE will determine the dc small-signal sensitivities of each specified output variable with respect to every circuit parameter. It is to be noted that for large circuits, large amounts of output can be generated.

### **14.4.2 AC Small Signal Analysis**

The ac small-signal portion of SPICE computes the ac output variables as a function of frequency. The program first computes the dc operating point of the circuit and determines linearised, small-signal models for all of the nonlinear devices included in the circuit. The resultant linear circuit is then analysed over a user-specified range of frequencies. The desired output of an ac small-signal analysis is usually a transfer function (voltage gain, transimpedance, etc). If the circuit has only one ac input, it is convenient to set that input to unity and zero phase, so that output variables have the same value as the transfer function of the output variable with respect to the input.

#### **.AC**

General form:

.AC DEC ND FSTART FSTOP  
 .AC OCT NO FSTART FSTOP  
 .AC LIN NP FSTART FSTOP

#### **Examples:**

.AC DEC 10 1 10K  
 .AC DEC 10 1K 100MEG  
 .AC LIN 100 1 100HZ

DEC stands for decade variation, and ND is the number of points per decade. OCT stands for octave variation, and NO is the number of points per octave. LIN stands for linear variation, and NP is the number of points. FSTART is the starting frequency, and FSTOP is the final frequency. When this statement is included in the circuit file, the SPICE will perform an ac analysis of the circuit over the specified frequency range. It can be noted that at least one independent source must be specified with an ac value.

The generation of white noise by resistors and semiconductor devices can also be simulated with the ac small-signal portion of SPICE. Equivalent noise source values are determined automatically from the small-signal operating point of the circuit, and the contribution of each noise source is added at a given summing point. The total output noise level and the equivalent input noise level are determined at each frequency point. The output and input noise levels are normalised with respect to the square root of the noise bandwidth and have the units Volts/root Hz or Amps/root Hz. The output noise and equivalent input noise can be printed or plotted in the same fashion as other output variables. No additional input data are necessary for this analysis.

The distortion characteristics of a circuit in the small signal mode can be simulated as a part of the ac small-signal analysis. The analysis is performed assuming that one or two signal frequencies are imposed at the input.

#### **.NOISE**

General form:

.NOISE OUTV INSRC NUMS

**Example:**

.NOISE V(5) VIN 10

This command controls the noise analysis of the circuit. The noise analysis is performed in conjunction with the ac analysis. OUTV is an output voltage which defines the summing point. INSRC is the name of the independent voltage or current source which is the noise input reference. NUMS is the summary interval. SPICE will compute the equivalent output noise at the specified output as well as the equivalent input noise at the specified input. The output noise and the equivalent input noise may also be printed and/or plotted.

### 14.4.3 Transient Analysis

The transient analysis portion of SPICE computes the transient output variables as a function of time over a time interval specified by the user. The initial conditions are automatically determined by a dc analysis. All sources such as power supplies that are not time dependent are set to their dc value. For large-signal sinusoidal simulations, a Fourier analysis of the output waveform can be specified to obtain the frequency domain Fourier coefficients. The transient time interval and the Fourier analysis options are specified on the *.TRAN* and *.FOURIER* control lines.

To perform a transient analysis for *linear circuits*, SPICE completes the outer loop only, ignoring blocks 2 and 5 in the spice algorithm of Fig. 14.1. After the initial operating point is found, the energy-storage components (capacitors, inductors, semiconductor junctions) are transformed into linear companion models. For *non-linear circuits*, SPICE completes the Non-Linear loop (2–6) at each time point of the transient analysis.

The SPICE dynamically adjusts the time step for two reasons, namely, to improve accuracy and to reduce long simulation times. The time step will be reduced when circuit voltages and currents are changing rapidly. Accuracy generally improves with a smaller time step. On the other hand, for slowly changing signals, the time step can be increased, and this avoids long simulation.

#### **.TRAN**

General form:

.TRAN TSTEP TSTOP <TSTART <TMAX>> <UIC>

**Examples:**

.TRAN 1NS 100NS

.TRAN 1NS 1000NS START = 500NS

.TRAN 10NS 1US UIC

*TSTEP* is the printing or plotting increment for line-printer output. For use with the post-processor, *TSTEP* is the suggested computing increment. *TSTOP* is the final time, and *TSTART* is the initial time. If *TSTART* is omitted, it is assumed to be zero. The transient analysis always begins at time zero. *TMAX* is the maximum step size that SPICE will use (for default, the program chooses either *TSTEP* or (*TSTOP*-*TSTART*)/50.0, whichever is smaller).

*TMAX* is useful when one wishes to guarantee a computing interval which is smaller than the printer increment *TSTEP*.

*UIC* (*use initial conditions*) is an optional keyword which indicates that the user does not want SPICE to solve for the quiescent operating point before beginning the transient analysis. If this keyword is specified, SPICE uses the values specified using *IC=...* on the various elements as the initial transient condition and proceeds with the analysis. If the *.IC* card has been specified, then the node voltages on the *.IC* command are used to compute the initial conditions for the devices.

**.FOUR**

General form:

*.FOUR FREQ OV1 <OV2 OV3 ...>*

**Examples:**

*.FOUR 100K V(5)*

This statement controls whether SPICE performs a Fourier analysis as a part of the transient analysis. FREQ is the fundamental frequency, and OV1, ..., are the output variables for which the analysis is desired. The Fourier analysis is performed over the interval, where TSTOP is the final time specified for the transient analysis, and period is one period of the fundamental frequency. The dc component and the first nine components are determined. For maximum accuracy, TMAX (see the .TRAN command) should be set to period/100.0 (or less for very high-Q circuits).

#### 14.4.4 Pole-Zero Analysis

The pole-zero analysis computes the poles and/or zeros in the small-signal AC transfer function. The program first computes the DC operating point and then determines the linearised, small-signal models for all the non-linear devices in the circuit. This circuit is then used to find the poles and zeros of the transfer function.

Two types of transfer functions are allowed, namely, of the form *output voltage/input voltage* or, of the form *output voltage/input current*. These two types of transfer functions cover all the cases and one can find the poles/zeros of functions like input/output impedance and voltage gain. The input and output ports are specified as two pairs of nodes. The pole-zero analysis works efficiently with resistors, capacitors, inductors, linear-controlled sources, independent sources, BJTs, MOSFETs, JFETs and diodes. Transmission lines are not supported.

#### 14.4.5 Small Signal Distortion Analysis

The distortion analysis computes the steady-state harmonic and intermodulation products for small input signal magnitudes. If signals of a single frequency are specified as input to the circuit, the complex values of the second and third harmonics are determined at every point in the circuit. If there are signals of two frequencies input to the circuit, the analysis finds out the complex values of the circuit variables as the sum and difference of the input frequencies, and as the difference of the smaller frequency from the second harmonic of the larger frequency.

Distortion analysis is supported for the non-linear devices such as diodes, BJT, JFET, MOSFETs and MESFETs. All linear devices are automatically supported by distortion analysis. If there are switches present in the circuit, the analysis continues to be accurate, provided the switches do not change state under the small excitations used for distortion calculations.

### 14.5 OTHER STATEMENTS

#### *.IC - Initial transient conditions*

*.IC { {vnode} } = {value} }*

**Examples:**

.IC V(2)=3.4 V(102)=0

**.MODEL – Device model**

.MODEL {name} {type}

Type name	Dev name	Dev type
CAP	C_name	capacitor
IND	L_name	inductor
RES	R_name	resistor
D	D_name	diode
NPN	Q_name	NPN bipolar
PNP	Q_name	PNP bipolar
NJF	J_name	N-channel JFET
PJF	J_name	P-channel JFET
NMOS	M_name	N-channel MOSFET
PMOS	M_name	P-channel MOSFET
VSWITCH	S_name	voltage controlled switch

**Examples:**

.MODEL RMAX RES (R=1.5 TC=.02 TC2=.005)

.MODEL QDRIV NPN (IS=1e-7 BF=30)

**NODESET – Initial bias point guess**

.NODESET { {node}={value} }

**Example:**

.NODESET V(2)=3.4 V(3)=-1V

**.PRINT – Print output**

General form:

.PRINT PRTYPE OV1 <OV2 ... OV8>

**Examples:**

.PRINT TRAN V(6) I(VIN)

.PRINT AC VM(4,2) VR(5) VP(5,3)

.PRINT DC V(2) I(VSRC) V(3,19)

.PRINT NOISE INOISE

.PRINT DISTO HD3 SIM2(DB)

This statement defines the contents of a tabular listing of one to eight output variables. PRTYPE is the type of the analysis (DC, AC, TRAN, NOISE or DISTO) for which the specified outputs are desired.

**.PLOT**

General form:

*.PLOT PL\_TYPE OV1 <(PLO1,PHI1)> <OV2 <(PLO2,PHI2)> ... OV8>*

**Examples:**

*.PLOT DC V(4) V(5) V(1)*

*.PLOT TRAN V(17,5) V(2,5) I(VIN) V(17)*

*.PLOT AC VM(5) VM(3,2) VDB(7) VP(5)*

*.PLOT DISTO HD2 HD3(R) SIM2*

*.PLOT TRAN V(5,3) V(8) V(7)*

This statement defines the contents of one plot with one to eight output variables. The optional plot limits (PLO, PHI) may be specified after any of the output variables. All output variables to the left of a pair of plot limits (PLO, PHI) will be plotted using the same lower and upper plot bounds.

**.PROBE**

*.PROBE [output variable names]*

**Examples:**

*.PROBE*

*.PROBE V(3) VM(2) I(VIN)*

This PSPICE Command saves simulation output of the variables listed.

**.SUBCKT—Subcircuit definition**

A subcircuit consists of SPICE elements that are defined and referenced in a fashion similar to device models. The subcircuit is defined in the input deck by grouping of element cards. Then, the program automatically inserts the group of elements, whenever the subcircuit is referenced.

General form:

*.SUBCKT SUB\_CIRCUIT\_NAME N1*

**Example:**

*.SUBCKT INV 1 2*

**.ENDS**

General form:

**.ENDS****Example:**

*.ENDS INV*

This statement forms the last line of any subcircuit definition.

**Subcircuit calls**

General form:

*X\_NAME\_OF\_SUBCKT N1 SUBNAM*

**Example:**

X1 24 17 INV

Subcircuits are used in SPICE by specifying pseudo-elements beginning with the letter X, followed by the circuit nodes to be employed in introducing the subcircuit.

## **14.6 CONTROL STATEMENTS**

### **.TEMP**

General form:

.TEMP < T1 >

**Example:**

.TEMP -55.0 25.0 125.0

This command specifies the temperatures at which the circuit is to be simulated, where T1, T2 etc. specify the different temperatures in degree C. Temperatures less than -223.0 deg C are ignored. Model data are specified at TNOM. If .TEMP command is omitted, the simulation will be performed at a temperature equal to TNOM.

### **.WIDTH**

General form:

.WIDTH IN=COLUMN OUT=COLUMN

**Example:**

.WIDTH IN=72 OUT=133

COLUMN is the last column read from each line of input, and it sets the print width. The default value for COLUMN is 80. The permissible limits for the output print width are from 80 to 133.

### **.OPTIONS**

General form:

.OPTIONS OPT1 OPT2 ... (or OPT=OPTVAL ...)

**Example:**

.OPTIONS ACCT LIST NODE

This command allows the user to reset program control and user options for specific simulation purposes.

The following sections deal with the ORCAD PSPICE simulation programs written as a netlist along with a brief introduction for the use of Schematic Capture feature. OrCAD PSpice A/D models the behaviour of a circuit containing any mix of analog and digital devices. Using OrCAD for design entry, the PSpice A/D is a software-based breadboard of our circuit, which we can use to test and modify our designs before connecting or assembling the hardware. It works well with both analog and digital circuits for simulation.

## 14.7 USING SCHEMATIC CAPTURE FEATURE OF ORCAD TO PREPARE FOR SIMULATION

**Schematic** is a design entry program meant to prepare the circuit for simulation. This makes it possible to simulate the circuits using the operational steps of

- placing and connecting part symbols
- defining component values and other attributes
- defining input waveforms
- enabling one or more analyses and
- identifying the points in the circuit where we want to see results

**Probe** Probe is a graphical results analyser. When PSpice A/D completes the simulation, Probe plots the waveform results so that we can visualize the circuit behaviour and determine the validity of the design. Taken together, PSpice A/D simulation and Probe waveform analysis is an iterative process.

**The general files needed for simulation** To simulate the design, the PSpice A/D identifies the following:

- the parts or the components in the circuit and how they are interconnected
- what are the analyses to be run
- the simulation models that correspond to the components in the circuit
- the stimulus definitions with which the tests are done

This information is provided in various data files, some generated by Schematics and others from libraries, and some others are user-defined.

**Netlist file** The netlist file contains the list of device names, values and how they are connected with other devices using the node names. The name that Schematics generates for this file is *schematic\_name.net*.

**Circuit file** The circuit file contains commands describing how to run the simulation. This file also refers to other files that contain netlist, model, stimuli and any other user-defined information that apply to the simulation. The name that Schematics generates for this file is *schematic\_name.cir*.

**Model library** A model library is a file that contains the electrical definition of one or more parts. PSpice A/D uses this information to determine how a part will respond to different electrical inputs.

These definitions take the form of either :

- (a) *.model parameter set*, which defines the behaviour of a part by fine-tuning the underlying model built into PSpice A/D, or
- (b) *.subcircuit netlist*, which describes the structure and function of the part by interconnecting other parts and primitives.

The model library has a *.lib* extension.

When needed, the models can be created by the users manually using the model editor in Schematics or some other text editor, or automatically by using the parts utility provided in SPICE.

**Changing model parameters** While using Schematic Capture, it may be necessary to change some specific parameters of an element, i.e., a different beta factor ( $\beta_F$ ) for a transistor. From “Edit” menu, “Model” submenu can be chosen, followed by “Edit Instance Model”. Then, the model can be saved and used for the application program.

**Probe data file** The Probe data file contains the simulation results in a format that the Probe can read. Probe reads this file automatically and displays the waveforms reflecting circuit response at nets, pins and

parts that are marked in the schematic (cross-probing). The simulation can be set up so that the Probe displays the results as the simulation progresses or after the simulation completes. Once Probe has read the Probe data file and displays the initial set of results, more waveforms can be added to perform post-simulation analysis of the data.

**PSpice output file** The PSpice output file is an ASCII text file that contains:

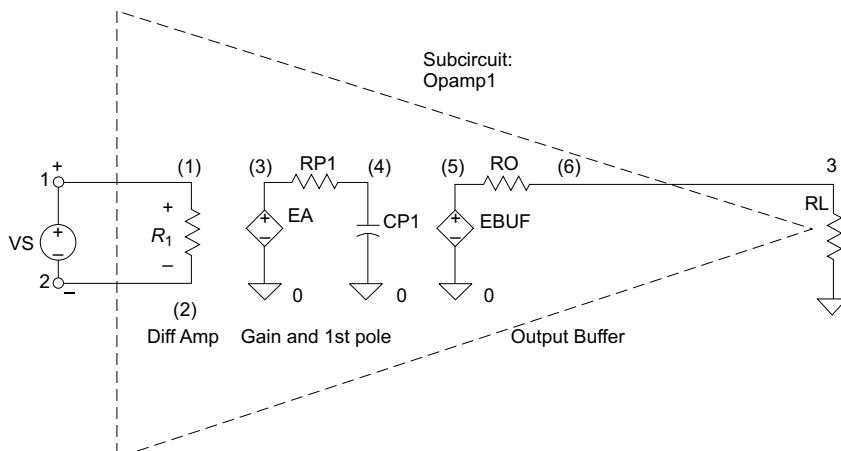
- the netlist representation of the circuit
  - the PSpice command syntax for simulation commands and options (like the enabled analyses)
  - simulation results
  - warning and error messages for problems encountered during read-in or simulation
- Its content is determined by:
- the types of analyses run
  - the options selected for running PSpice A/D
  - the simulation control symbols (like VPRINT1 and VPLOT1) that are placed and connected to nets in the schematic.

**Shortcuts** The shortcuts that the user uses while programming with the ORCAD PSPICE are as follows:

- |   |        |
|---|--------|
| • To save after <i>each</i> editing:                | Ctrl+S |
| • To simulate ( <i>after saving each editing</i> ): | F11    |
| • To rotate an element, i.e. a resistor:            | Ctrl+R |
| • To get a new part from the “Draw” menu:           | Ctrl+G |
| • To copy an element instead of pulling from menu:  | Ctrl+C |
| • To paste element into place:                      | Ctrl+V |
| • To draw connecting wires:                         | Ctrl+W |
| • To discontinue using element:                     | Esc    |

## 14.8 SIMULATION EXAMPLES

The following examples employ the SPICE model of a typical 741 op-amp as shown in Fig. 14.4(a). The model is identified using a *.MODEL* statement in the circuit file.



**Fig. 14.4 (a) The basic op-amp model**

### Op-amp model

The three basic stages of an op-amp are (i) a differential amplifier, (ii) a voltage gain stage with single-pole frequency roll-off, and (iii) an output buffer.

The subcircuit models the following behaviours defined by:

Input impedance	RI
Differential Gain	EA
Single Pole Frequency	RP1, CP1
Output Impedance	RO

### Open-loop frequency response

The open-loop response indicates the performance of the op-amp. Two important features are

- i. DC Gain
- ii. First-Pole Frequency,  $f_{p1}$  – the frequency where the open-loop gain begins to fall. A direct result of  $f_{p1}$  and the *DC Gain* is the Unity-Gain Frequency  $f_u$  which is the frequency where the open-loop gain falls to 1 V/V. The greater the value of  $f_u$ , the faster the op-amp can respond. Unity-Gain Frequency is given by

$$f_u = \text{DCGAIN} \times f_{p1}$$

where the pole frequency is formed by a simple RC filer

$$f_{p1} = \frac{1}{2\pi \times RP1 \times CP1}$$

**Simulation note** The op-amp model is created from several simple SPICE devices. The differential input and DCGAIN stage are implemented by a Voltage-Controlled Voltage Source (VCVS) named EGAIN. The device

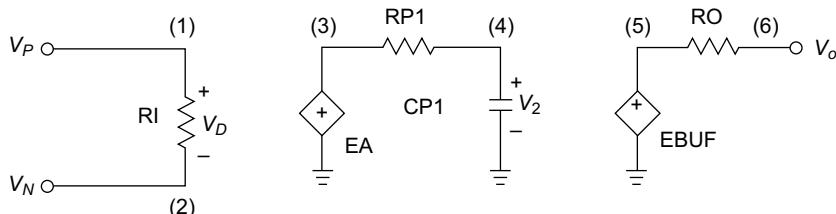
*EA* 3 0 1 2 100K

follows the syntax

*E*{name} {+output} {-output} {+control} {-control} {gain}

that creates a voltage source having positive and negative output terminals at nodes 3 and 0. The source is controlled by the voltage at positive and negative sense leads 1 and 2. This voltage is then multiplied by the gain 100k and applied at the output terminals. The output buffer EBUF is simply another VCVS.

**Op-amp subcircuit definition** The internal circuit of the op-amp device as shown in Fig. 14.4(b) is defined by a subcircuit in the examples. The statement XOA1 0 2 4 OA indicates to the PSpice that the op-amp device OA is described by the subcircuit XOA1 for the op-amp A1.



**Fig. 14.4 (b)** Internal circuit equivalent of op-amp

The components of the device are listed between the statements .SUBCKT OP-AMP1 1 2 6 and .ENDS. During the simulation, nodes 1, 2 and 6 of the subcircuit connect to nodes 0, 2 and 4 of the main circuit, respectively. It can be noticed that, the internal nodes and component names of a subcircuit are separate from those in the main circuit.

**Spice file** A typical PSpice file appears as shown below.

```

OA.CIR - OP-AMP MODEL SINGLE-POLE
  * The voltage source VS applied between terminals 1 and 0 with an ac
  * voltage of amplitude 1V
    VS      1      0      AC      1
  * The op-amp OA is called as a subcircuit across terminals 1, 0 and 3
    XOP      1      0      3      OA
  * Resistance RL of value 1Kilo Ohm between the terminals 3 and 0
    RL      3      0      1K
  *
  * OP-AMP OA MACRO MODEL, SINGLE-POLE
  * connections: non-inverting input
  *                                | inverting input
  *                                |     |     output
  *                                |     |
  .SUBCKT OA      1      2      6
  *
  * INPUT IMPEDANCE
  RI      1      2      10MEG
  * DC GAIN=100K AND POLE1=100HZ
  * UNITY GAIN = DCGAIN X POLE1 = 10MHZ
  EA      3      0      1      2      100K
  RP1     3      4      1K
  CP1     4      0      1.5915UF
  *
  * OUTPUT BUFFER AND RESISTANCE
  EBUF    5      0      4      0      1
  RO      5      6      10
  .
  .ENDS
  *
  * AC ANALYSIS
  .AC      DEC      5      1      100MEG
  * PRINT RESULTS
  .PLOT AC VM(3)
  .PROBE
  .
  .END

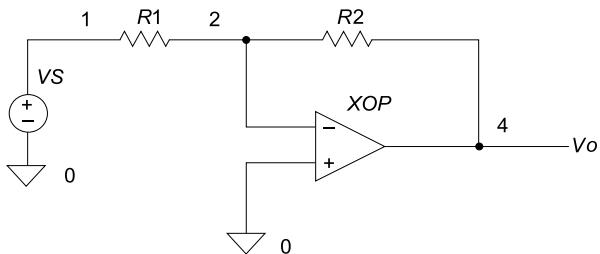
```

## Example 14.1

### Op-Amp Inverting Amplifier

The circuit diagram of an inverting amplifier is shown in Fig. 14.5(a). The voltage gain of the circuit is given by the ratio of the feedback resistor  $R_2$  to input resistor  $R_1$ . Then, the output voltage can be expressed as

$$V_O = - V_S \frac{R_2}{R_1}$$



**Fig. 14.5 (a)** Inverting amplifier circuit diagram

The netlist for the circuit shown below it is

saved as `inv_amp_circuit.cir`. The simulation is started using the *open simulation* command from the File Menu of the ORCAD PSpice A/D program. The simulation is then run using the *Run* command from the Simulation Menu. The outputs are then observed from the output probe window using the Add Trace command from the Trace Menu. Additional plots can be added to the window using Add Plot to Window from Plot Menu.

Then, the input  $V(1)$  and output  $V(4)$  are plotted from the transient analysis as shown in Fig. 14.5. The waveforms are obtained with  $V_s = 1V$  (p-p),  $R_1 = 5k\Omega$  and  $R_2 = 10k\Omega$ , the amplifier produces an inverted  $2V$ p-p output at  $V(4)$  as shown in Fig. 14.5(b).

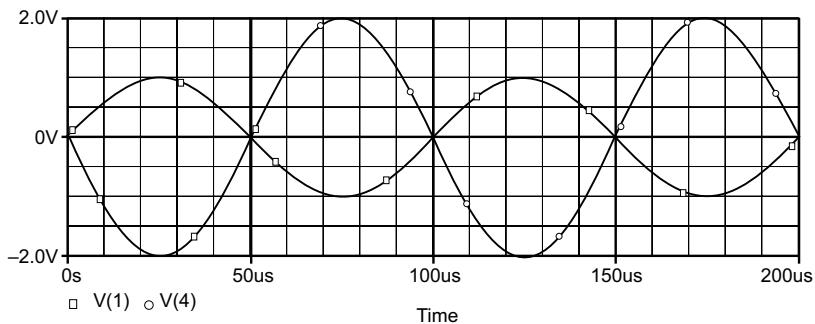
### Spice file

```

INVERTING AMPLIFIER USING OP-AMP
*
VS 1 0 AC 1 SIN(0V 1VPEAK 10KHZ)
*
R1 1 2 5K
R2 2 4 10K
XOA1 0 2 4 OA
*
* OP-AMP MACRO MODEL, SINGLE-POLE
* connections: non-inverting input
* | inverting input
* | | output
* |
.SUBCKT OA 1 2 6
*
* INPUT IMPEDANCE
RIN 1 2 10MEG
*
* GAIN BW PRODUCT = 10MHZ
* DC GAIN (100K) AND POLE 1 (100HZ)
EGAIN 3 0 1 2 100K
RP1 3 4 1 K
CP1 4 0 1.5915UF
*
* OUTPUT BUFFER AND RESISTANCE
EBUFFER 5 0 4 0 1
ROUT 5 6 10
.ENDS
*
* ANALYSIS
.AC DEC 5 1K 10MEG

```

```
.TRAN      5US      0.2MS
* PRINT RESULTS
.PRINT AC V(1) V(4)
.PRINT TRAN V(1) V(4)
.PROBE
.END
```

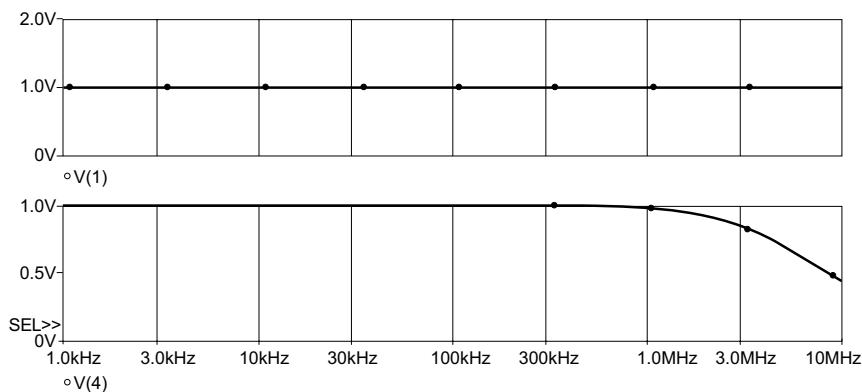


**Fig. 14.5 (b)** Inverting amplifier input and output waveforms

The gain of the amplifier circuit can be changed by selecting a different value for R<sub>2</sub>. The circuit file can be edited with the new R<sub>2</sub> value. Saving the file and running a new simulation produces the output amplified by the ratio as set by the feedback resistor and input resistor.

**Virtual ground** The *virtual ground* can be identified by probing at the negative input terminal of op-amp. It can be seen that the *negative input V(2)* is very small regardless of the input or output voltage and it is so small that it can be assumed to be at *virtually* a ground potential.

**Bandwidth** To analyse the bandwidth of the amplifier, the simulation is run with R<sub>1</sub>=R<sub>2</sub>=5 kΩ and the AC analysis of the circuit is done and the response characteristics is shown in Fig. 14.6. The flat portion of the magnitude VM(4) curve indicates the frequencies within the bandwidth where the circuit is capable of amplifying. Beyond the bandwidth of the amplifier, the response of the circuit decreases.



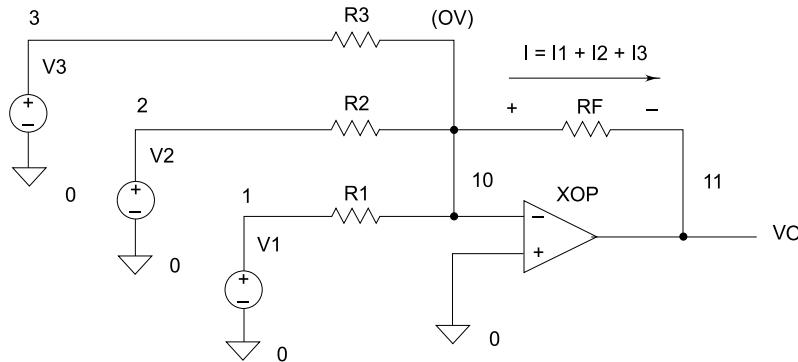
**Fig. 14.6** Frequency response characteristics

The circuit can be simulated with increased gain factors which would lead to reduction in bandwidth. Increasing the gain reduces the bandwidth and hence, a trade-off between gain and bandwidth is to be made.

## Example 14.2

### Summing Amplifier

The summing amplifier is used to add several signals together. An audio mixer is a typical example of adding waveforms pertaining to sounds from different channels. The gain of the adder can be varied for selective inputs. It is to be noted that the circuit also inverts the input signals. The circuit diagram of a summing amplifier is shown in Fig. 14.7.



**Fig. 14.7** Circuit of a summing amplifier

**Summing action** The principle of the circuit is to keep the potential of the negative terminal and the positive terminal very close to each other. In Fig. 14.7 shown, the negative terminal is kept close to 0 V which is called the virtual ground. Therefore, the op-amp essentially keeps one leg of R1, R2 and R3 at a 0 V potential. This makes it easy to write the currents in these resistors as given by

$$I_1 = V_1 / R_1$$

$$I_2 = V_2 / R_2$$

$$I_3 = V_3 / R_3$$

The current I flowing in RF according to Kirchhoff's Current law is given by

$$I = I_1 + I_2 + I_3$$

Therefore, the output is given by

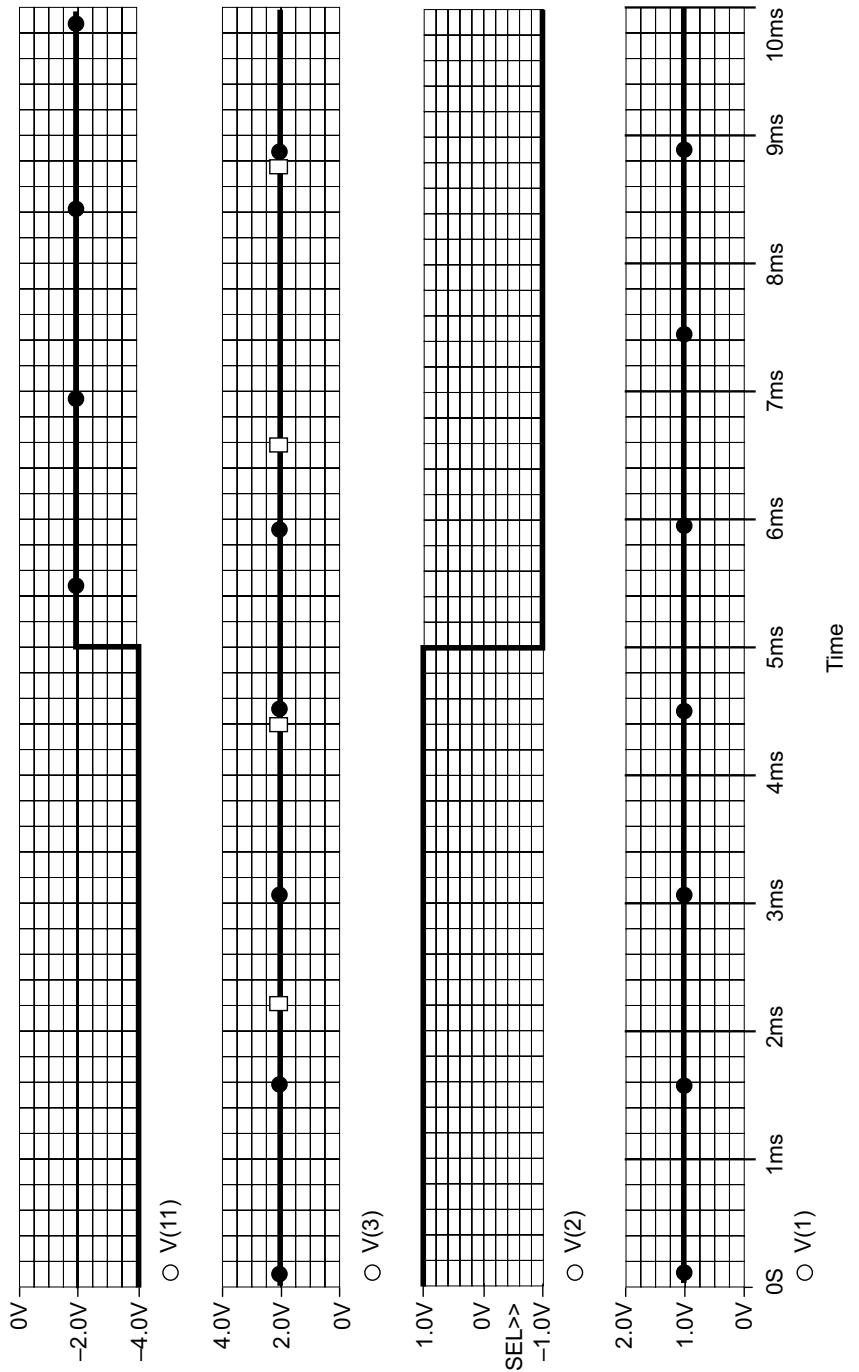
$$V_O = -RF \times I$$

$$\text{or } V_O = -RF (V_1 / R_1 + V_2 / R_2 + V_3 / R_3)$$

$$= -(V_1 \times RF / R_1 + V_2 \times RF / R_2 + V_3 \times RF / R_3)$$

In the circuit shown in Fig. 14.7, three waveforms namely, sine, square and triangle are added and the individual gain control for the three inputs are also made by the selection of the resistors connected to them.

The circuit file of Fig. 14.7 is written and saved as sum\_amp.cir and the simulation is run, assuming  $R_1=R_2=R_3=RF=10\text{ k}\Omega$ , and hence, the gain for the three inputs are the same and is given by  $-10\text{ k}\Omega / 10\text{ k}\Omega = -1$ . The output waveforms obtained for the values shown in the circuit and DC input voltages of 1 V and 2 V respectively at Pin 1 and 3 of the circuit and a piecewise linear voltage at Pin 2 are shown in Fig. 14.8.



**Fig. 14.8** Input and output waveforms

For achieving varied gains for the three inputs, choose different values of R2 and R3.

### Spice file

```
SUM_AMP.CIR - OP-AMP SUMMING AMPLIFIER
*
V1      1      0      DC      1V
V2      2      0      PWL(0MS 1V 5MS 1V 5.01MS -1V 10MS -1V)
V3      3      0      DC      2V
*
* INPUT RESISTANCES
R1      1      10     10K
R2      2      10     10K
R3      3      10     10K
* FEEDBACK RESISTANCES
RF      11     10     10K
*
* OP-AMP
XOA1    0      10     11     OA
*
* OP-AMP MACRO MODEL, SINGLE-POLE
* connections:      non-inverting input
*                      |      inverting input
*                      |      |      output
*                      |      |      |
.SUBCKT OA           1      2      6
*
* INPUT IMPEDANCE
RIN      1      2      10MEG
* GAIN BW PRODUCT = 10MHZ
* DC GAIN (100K) AND POLE 1 (100HZ)
EGAIN    3      0      1      2      100K
RP1      3      4      1K
CP1      4      0      1.5915UF
*
* OUTPUT BUFFER AND RESISTANCE
EBUFFER   5      0      4      0      1
ROUT      5      6      10
.ENDS
*
* TRANSIENT ANALYSIS FOR 10 MS AT A TIME STEP OF 50US
.TRAN      50US  10MS
*
* PRINT RESULTS
.PLOT      TRAN  V(11)
.PRINT     TRAN  V(11)
.PROBE
.END
```

### Example 14.3

#### Transimpedance Amplifier (Current-to-Voltage Amplifier)

For applications such as high-speed fibre-optic receivers, the current from the sensors are to be converted to a useful wide range voltage. The *transimpedance amplifier*, which is also called as the *current-to-voltage converter* can be employed in such applications.

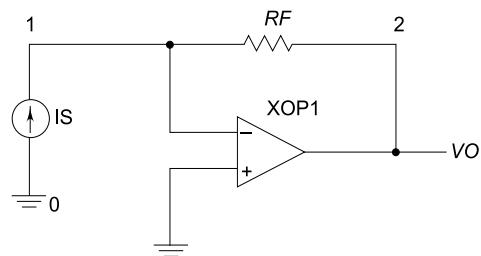
The two important principles used in the design of the circuit are

- The current flows through the feedback resistor RF only, since no current can enter the op-amp.
- One terminal of resistor RF is held at ground potential, called *virtual ground* (0V). And, since the non-inverting input is connected to ground, the inverting input along with RF is also held at 0V.

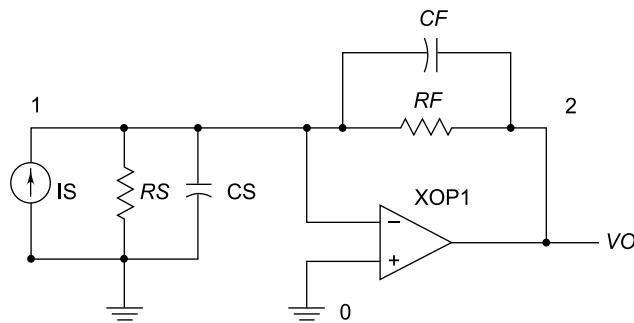
Then, the output  $V_o$  can be described simply as the voltage across the resistor VRF.

$$V_o = V_{RF} = IS \times RF$$

Figure 14.9 shows the circuit diagram with the current source IS delivering a 10  $\mu A$  pulse (20  $\mu s$  wide) to the transimpedance amp. A practical I to V converter circuit using sensor resistance can be drawn as shown in Fig. 14.10.



**Fig. 14.9** Transimpedance amplifier circuit diagram

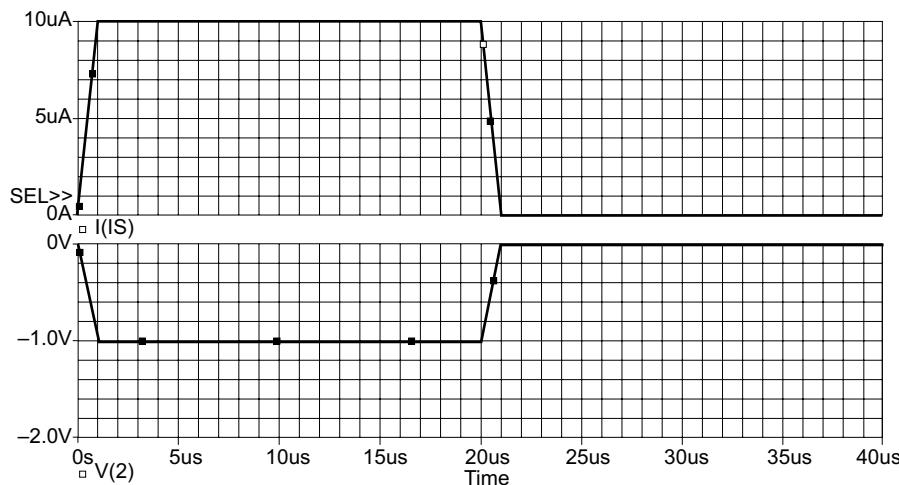


**Fig. 14.10** Practical transimpedance amplifier

The source resistance RS and the capacitance CS produces undesirable *low-pass* filtering effect in the feedback path from output to input. This is compensated by adding a capacitor CF in the feedback path. The netlist is shown below.

**Spice file** The netlist shown below is edited as a text file and is saved with the \*.cir extension. The simulation output is shown in Fig. 14.11.

```
TRANS_IMP.CIR - OP-AMP TRANSIMPEDANCE AMPLIFIER
* SENSOR
IS 0 1 AC 1 PWL(0US 0UA 1US 10UA 20US 10UA 21US 0 40US 0)
RS      1      0      500K
CS      1      0      100PF
*
```



**Fig. 14.11** The input current and output voltage waveforms

```

* TRANSIMPEDANCE AMPLIFIER
RF      1      2      100K
*CF      1      2      2PF
XOA1      0      2      4      OA
*
* OP-AMP MACRO MODEL, SINGLE-POLE
connections:      non-inverting input
*                      |      inverting input
*                      |      |      output
*                      |      |      |
.SUBCKT OA      1      2      6
* INPUT IMPEDANCE
RIN      1      2      10MEG
* GAIN BW PRODUCT = 10MHZ
* DC GAIN (100K) AND POLE 1 (100HZ)
EGAIN      3      0      1      2      100K
RP1       3      4      1K
CP1       4      0      1.5915UF
* OUTPUT BUFFER AND RESISTANCE
EBUFFER     5      0      4      0      1
ROUT      5      6      10
.ENDS
* TRANSIENT ANALYSIS FOR 40US
* DURATION WITH 200NS TIME STEP
* AC ANALYSIS FOR FREQUENCY UPTO 10MHZ
.TRAN      200NS      40US
.AC      DEC      10 100 10MEG
* PRINT RESULTS
.PRINT      TRAN      V(2)

```

```
.PRINT      AC      VM (2)
.PROBE
.ENDS
*
```

### Example 14.4

#### Op-Amp Differentiator

The differentiator generates *an output voltage proportional to the rate of change of the input voltage*. This property of differentiators leads to the applications such as extracting edges from square-waves, converting sine -waves into cosines and changing triangle waves into square-waves.

Figure 14.12 shows the circuit of a differentiator using op-amp. Since the inverting input is at virtual ground, the input voltage  $V_S$  drops across  $C_1$ , producing an input current proportional to the rate of change of the input voltage.

$$i = C_1 dV_S/dt$$

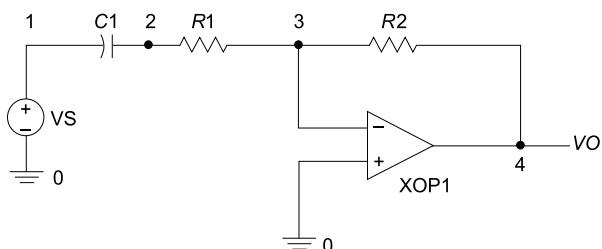
Since no current can flow into the op-amp through the inverting input terminal, the current  $i$  must flow through  $R_2$ , thereby creating the output voltage that is given by

$$V_O = -iR_2$$

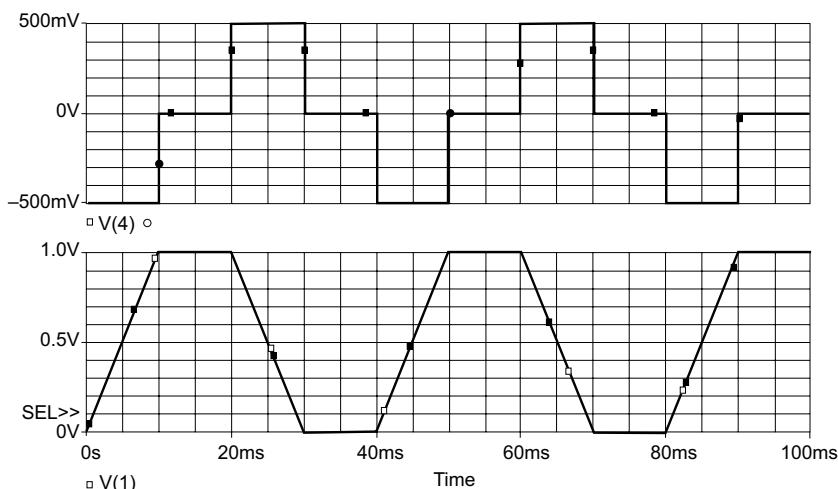
Substituting for  $i$ , we get

$$V_O = -C_1 R_2 dV_S/dt$$

Using a typical value for the components shown in Fig. 14.12, the simulation can be run using the netlist shown below. The transient response output of the simulation is shown in Fig. 14.13.



**Fig. 14.12** Op-amp differentiator circuit



**Fig. 14.13** The input trapezoidal step and the output waveforms

$$VO = -C1R2dVS/dt$$

$$= \frac{-10 \times 10^{-9} \times 500 \times 103 \times 1}{10 \times 10^{-3}} = 0.5V$$

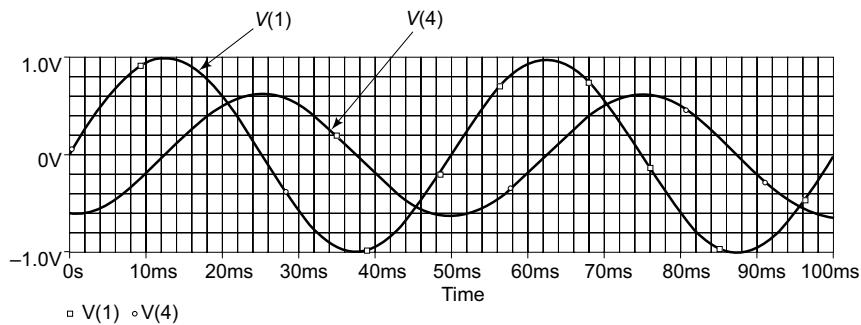
### Spice file

```

OP-AMP DIFFERENTIATOR
*
* TRAPEZOIDAL WAVE
VS1      1      0      PULSE(0V 1V 0MS 10MS 10MS 10MS 40MS)
* SINEWAVE
* VS2      1      0      SIN(0V 1V 20HZ)
* 1 VRMS FOR AC ANALYSIS
* VS3      1      0      AC      1
*
C1      1      2      10NF
R1      2      3      5K
R2      3      4      500K
XOA1    0      3      4      OA
*
* OP-AMP MACRO MODEL, SINGLE-POLE
* connections: non-inverting input
*                                |   inverting input
*                                |   |   output
*                                |   |   |
.SUBCKT OA      1      2      6
* INPUT IMPEDANCE
RIN      1      2      10MEG
* GAIN BW PRODUCT = 10MHZ
* DC GAIN (100K) AND POLE 1 (100HZ)
EGAIN    3      0      1      2      100K
RP1      3      4      1K
CP1      4      0      1.5915UF
* OUTPUT BUFFER AND RESISTANCE
EBUFFER   5      0      4      0      1
ROUT     5      6      10
.ENDS
*
* TRANSIENT ANALYSIS
.TRAN      1MS      100MS
*
* PRINT RESULTS
.PLOT      TRAN      V(1)      V(4)
.PROBE
.END

```

As another example, applying a sine-wave (*VS2*) to the differentiator's input, generates *cosine* output as shown in Fig. 14.14. If input is defined by  $VS = A \sin \omega t$ , then  $dVS/dt = \omega A \cos \omega t$ . Extending this equation to the circuit, we get



**Fig. 14.14** A sine input and a cosine output waveforms

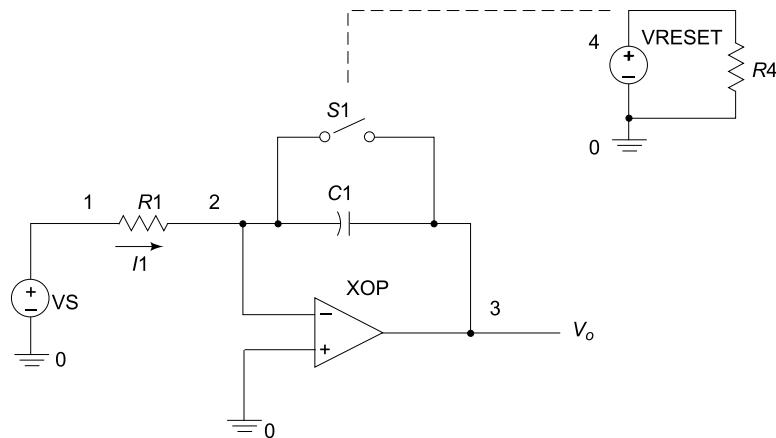
$$\begin{aligned}
 VO &= -C_1 R_2 dVs/dt \\
 &= -C_1 R_2 \omega A \cos \omega t \\
 &= -10 \times 10^{-9} \times 500 \times 10^3 \times 2 \times \pi \times 20 \times 1 \times \cos \omega t \\
 &= -0.628 \cos \omega t
 \end{aligned}$$

Introduction of the resistor  $R_1$  avoids the ringing and oscillation produced by the feedback circuit. At high frequencies, the capacitor  $C_1$  looks like a short compared to  $R_1$ . Hence, the circuit now looks like the basic inverting amplifier that is stable.

### Example 14.5

#### Op-Amp Integrator

The circuit diagram of an integrator is shown in Fig. 14.15. The current  $I_1$  that flows through  $R_1$  gets integrated across capacitor  $C_1$ . Then, the output voltage  $VO$  is the voltage across  $C_1$ . One of the main applications of the integrator is in the generation of a ramp voltage. This is done by placing a fixed voltage at  $V_S$  that forces a constant current through  $R_1$ . Then, the capacitor integrates this current, thereby generating a ramping voltage.



**Fig. 14.15** Integrator circuit diagram with RESET signal

**Use as a ramp generator** The circuit essentially integrates the input current  $I_s = V_s/R_1$  across the capacitor  $C_1$ . After a time interval  $T$ , the output is the capacitor voltage that is given by

$$VO = - \frac{1}{C1} \int_0^T \frac{VS}{R1} dt$$

If a constant voltage is applied at the input, the output voltage increases steadily, thus producing a ramp. The output voltage of the ramp can be derived from the equation

$$VO = - \frac{1}{C1} \times \frac{VS}{R1} \times T$$

Figure 14.15 shows the circuit with the values of  $VS = -1$ , and  $R1 = 10 \text{ k}\Omega$  and  $C1 = 10 \text{ nF}$ . The circuit is simulated using the netlist shown below, and the voltage at the output node is shown in Fig. 14.16. The switch control voltage VRESET connected at  $V(4)$  turns the switch OFF and ON to fix the timing for integration.

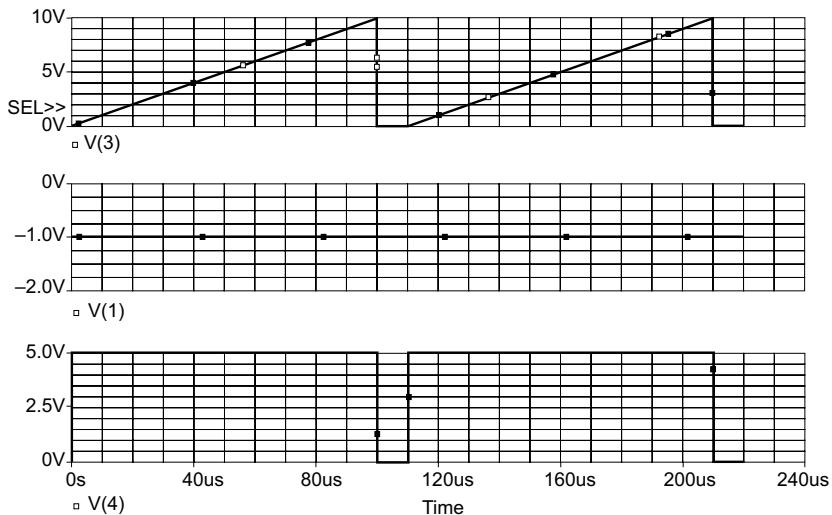
### Spice file

```

OPAMP_INT.CIR - OP-AMP INTEGRATOR
*
* CONTROL VOLTAGE FOR S1
VRESET    4    0      PULSE(0V 5V 0 0.1US 0.1US 100US 110US)
R4        4    0      1MEG
*
* INPUT VOLTAGE
VS        1    0      DC      -1
*
R1        1    2      10K
C1        2    3      1000PF
S1        2    3    40  SRES
*
.MODEL     SRES  VSWITCH(VON=0 VOFF = 5
+ RON = 100 ROFF = 10 MEG
*
XOA1      0    2    3      OA
*
* OP-AMP MACRO MODEL, SINGLE-POLE
* connections: non-inverting input
*                                |   inverting input
*                                |   |   output
*                                |   |   |
.SUBCKT OA          1    2    6
*
* INPUT IMPEDANCE
RIN       1    2      10MEG
* GAIN BW PRODUCT = 10MHZ
* DC GAIN (100K) AND POLE 1 (100HZ)
EGAIN     3    0    1    2      100K
RP1       3        4      1K
CP1       4        0      1.5915UF
* OUTPUT BUFFER AND RESISTANCE
EBUFFER   5    0    4    0      1
ROUT      5        6      10
.ENDS
* ANALYSIS

```

```
.TRAN      1US      220US
* PRINT RESULTS
.PLOT      TRAN      V(1)      V(3)
.PRINT     TRAN      V(1)      V(3)
.PROBE
.END
```

**Fig. 14.16** Output, Input and RESET signal waveforms**Example 14.6***Opamp Peak Detector Circuit*

```
*
VIN      1 0  DC 0 V PWL(0S, -5 V 1MS, -2.5 V 2MS, 2.5 V 3MS, -5 V 4MS, 7 V
5MS, -5 V)
*
* REFER TO FIG. 5.18(a).
* OP-AMP A1 OPERATES DURING NEGATIVE HALF CYCLE OF vi

XOP1 1 2 3 OPAMP1
R    2      5      2K
D1   2      3      D1N4148
D2   3      4      D1N4148
CH   4      0      1U

*OP-AMP2 OPERATES DURING POSTIVE HALF CYCLE OF vi
XOP2      4      5      5      OPAMP1
*
* OPAMP MACRO MODEL, SINGLE-POLE WITH 15 V OUTPUT CLAMP
* connections:      non-inverting input
*                  |      inverting input
*                  |      |      output
*                  |      |      |
```

```

.SUBCKT OPAMP1           1   2       6
* INPUT IMPEDANCE
RIN 1      2      10MEG
* DC GAIN=100K AND POLE1=100HZ
* UNITY GAIN = DCGAIN X POLE1 = 10MHZ
EGAIN     3      0      1      2 100K
RP1      3      4      100K
CP1      4      0      0.0159UF
* OUTPUT BUFFER AND RESISTANCE
EBUFFER   5      0      4      0 1
ROUT      5      6      10
.ENDS
*
* DIODE MODEL
.model      D1N4148      D (Is=0.1p Rs=16 CJO=2p Tt=12n Bv=100 Ibv=0.1
* TRANSIENT ANALYSIS
.TRAN      0.1MS 6MS      0S      0.1US
* PRINT RESULTS
.PRINT     TRAN    V(1)    V(5)
.PROBE
.END

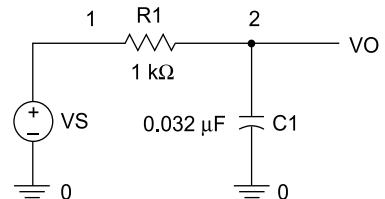
```

## Example 14.7

### Simple RC Low-Pass Filter

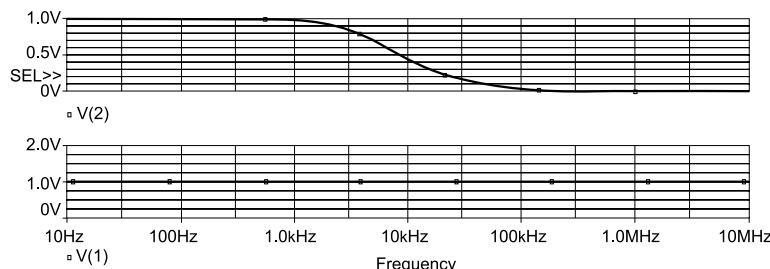
Figure 14.17(a) shows the simple circuit of a filter circuit for simulation with PSPICE and to plot the results. The circuit passes the desired low frequency signals and blocks the undesired high frequency signals. The frequency beyond which the filter blocks the high frequency components is called the *cut-off frequency* which is determined as given by the expression

$$f_c = \frac{1}{2\pi \times R1 \times C1}$$

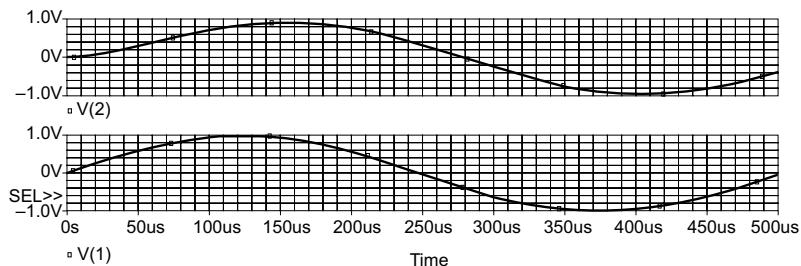


**Fig. 14.17 (a)** Low-Pass filter circuit diagram

Assuming  $R1 = 1\text{ k}\Omega$  and  $C1 = 0.032\text{ }\mu\text{F}$ , we get  $f_c = 5\text{ kHz}$ . The simulation is run and the AC (frequency) sweep result is plotted for the output magnitude  $VM(2)$  and phase  $VP(2)$ . The netlist of the circuit is shown below for the nodes indicated in Fig. 14.17(a). The waveforms shown in Fig. 14.17(b) and (c) indicate the original and filtered signals using the simple RC low-pass filter for AC and transient analyses.



**Fig. 14.17 (b)** Small signal AC Characteristics

**Fig. 14.17 (c) Transient characteristics****Spice file**

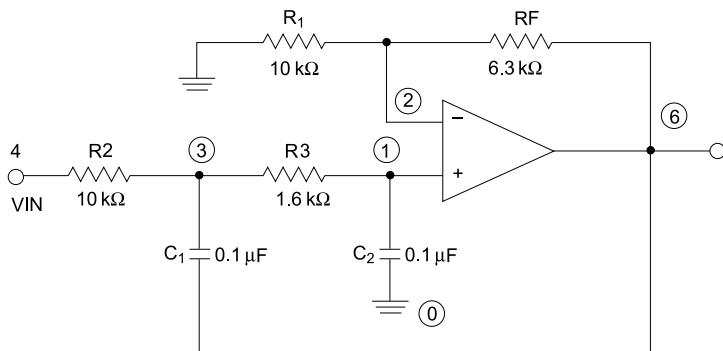
```

LPFILTER1.CIR - SIMPLE RC LOW-PASS FILTER
*
VS      1      0      AC      1      SIN(0    1      2KHZ)
*
R1      1      2      1K
C1      2      0      0.032UF
*
* AC ANALYSIS FOR 10MHZ FREQUENCY RANGE IN STEPS OF 10Hz
FROM
.AC    DEC      5      10      10MEG
.TRAN    5US    500US
* PRINT RESULTS
.PRINT    AC      VM(2)      VP(2)
.PLOT    AC      VM(2)      VP(2)
.PRINT    TRAN      V(1)      V(2)
.PLOT    TRAN      V(1)      V(2)
.PROBE
.END

```

**Example 14.8****Second-order Butterworth Low-Pass Filter**

Figure 14.18 (a) shows the second order low pass Butterworth filter using op-amp. The frequency response of a second order Butterworth low pass filter can be obtained using the SPICE netlist file shown below and the frequency response characteristics is shown in Fig. 14.18(b).

**Fig. 14.18 (a) Second-order low pass Butterworth filter**

**Spice file**

```

OPAMP LOW PASS BUTTERWORTH FILTER
* AC VOLTAGE SOURCE
VIN      4      0      AC      1      SIN(0  1      2KHZ)
** FILTER CIRCUIT
R1      2      0      10K
RF      2      6      6.3K
R2      4      3      10K
R3      3      1      1.6K
C1      3      6      0.1U
C2      1      0      0.1U
XOA     1      2      6      OA
*
* OPAMP MACRO MODEL, SINGLE-POLE WITH 15V OUTPUT CLAMP
* connections: non-inverting input
*                                | inverting input
*                                |           | output
*                                |           |   |
*.SUBCKT OA          1      2      6
* INPUT IMPEDANCE
RIN      1      2      10MEG
* DC GAIN=100K AND POLE1=100HZ
* UNITY GAIN = DCGAIN X POLE1 = 10MHZ
EA      3      0      1      2      100K
RPI     3      4      100K
CP1     4      0      0.0159UF
* OUTPUT BUFFER AND RESISTANCE
EBUF     5      0      4      0      1
RO      5      6      10
.ENDS
.AC DEC 20 1HZ 10kHz
.PRINT      AC      VM(6)  VP(6)
.PROBE
.END

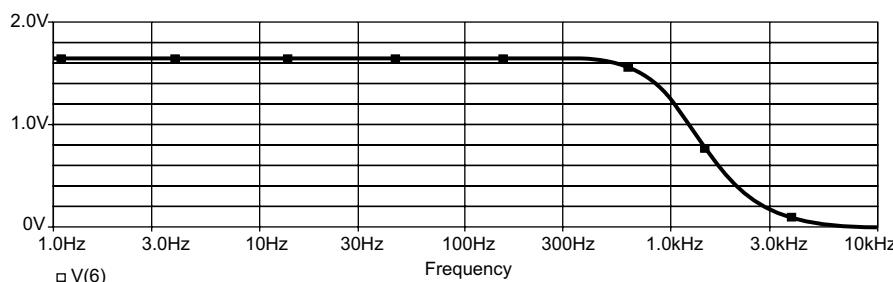
```

The theoretical value of the upper cut-off frequency  $F_H$  and the pass band gain  $A_0$  can be calculated as given by

$$F_H = 1/(2\pi R C) \text{ where } R = R_2 = R_3 = 1.5\text{KOHM}$$

$$\text{and } \text{GAIN } A_0(\text{DB}) = 20 \log(1 + RF/R1)$$

The output from simulation is shown in Fig. 14.18(b) and it can be compared with the theoretical values.

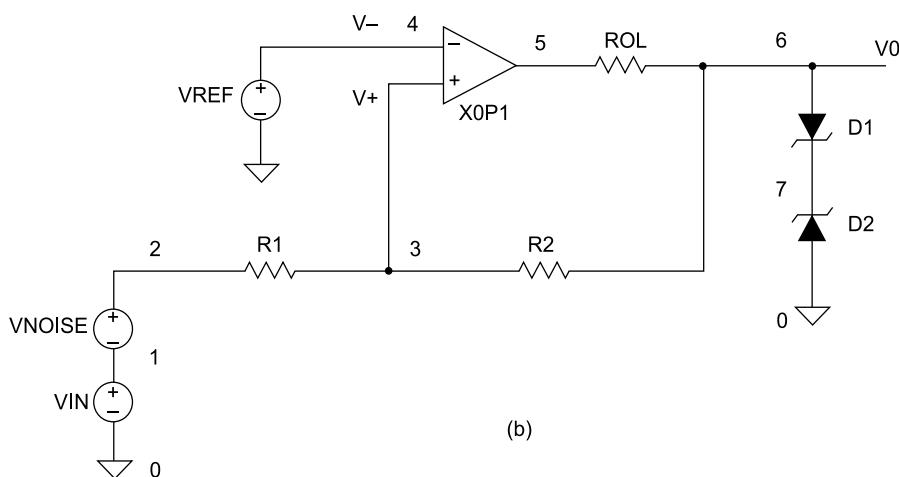
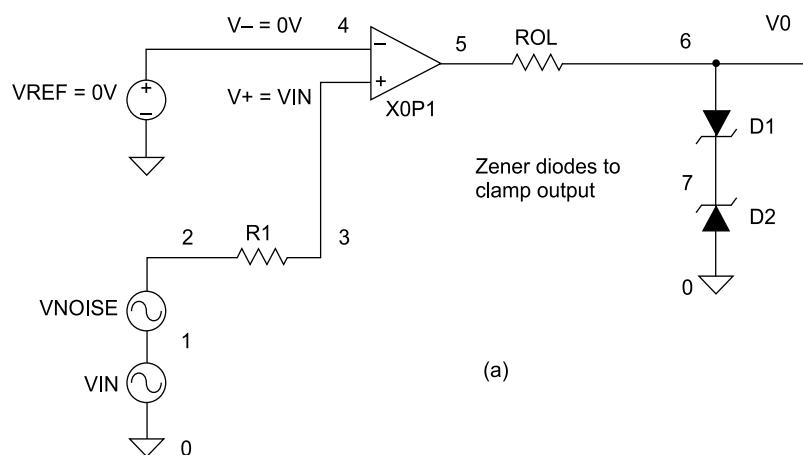


**Fig. 14.18 (b)** Output waveform of second-order low pass filter

## Example 14.9

### Op-amp Comparator with Hysteresis

Figure 14.19(a) shows the basic comparator circuit. This can be used to compare two voltages or to convert an AC sine wave to a square wave. This signal will serve as a clock to drive counters for a 24 hour time clock. However, the simple circuit responds to the small glitches or ambient noise in the AC line and causes inadvertent variations in the output. Hence, a comparator with better noise immunity is used as shown in Fig. 14.19(b) which employs the hysteresis characteristics achieved through positive feedback in the circuit from output to input.



**Fig. 14.19 (a) Op-amp basic comparator circuit**

**(b) Op-amp practical comparator with hysteresis**

The two threshold voltages as fixed by the circuit components are

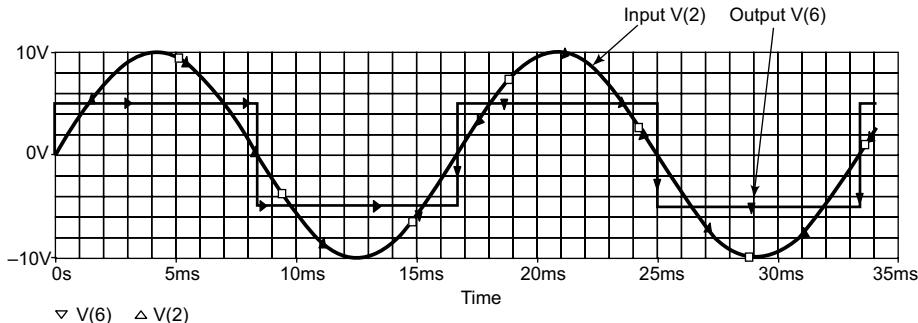
$$V_{th} (\text{Upper}) = -V_N \cdot R_1 / R_2$$

$$V_{th} (\text{Lower}) = -V_P \cdot R_1 / R_2$$

When the input rises above the threshold voltage, ( $V_{IN} > V_{th} \text{ Upper}$ ), we get a *positive* output saturation voltage. The Zener diodes limits the output voltage swing from the saturation voltage levels of the op-amp to the two Zener voltage values. When the input voltage falls below the threshold level ( $V_{IN} < V_{th} \text{ Lower}$ ), we get the *negative* output saturation voltage. It can be recalled that the positive and negative saturation levels are the positive and negative power supply voltages less than 1V approximately.

A reference voltage  $V_{REF}$  can also be added to the negative input of the op-amp, and this helps in varying the threshold levels in positive and negative values. The comparator can also be constructed as a positive and negative comparator by inverting the voltages applied at the inverting and non-inverting inputs of the op-amp.

**Spice file** The netlist of the circuit is shown below and is stored with a .cir extension and simulated. The output waveform obtained is shown in Fig. 14.20.



**Fig. 14.20** Input and output waveforms

#### OPAMP COMPARATOR WITH HYSTERESIS

```

*
VIN      1      0      SIN(0V 10VPEAK 60HZ)
VNOISE   2      1      SIN(0V 2VPEAK 2.5KHZ)
* TRY WITH 2V NOISE PEAK AND VERIFY THE RESULT
* VNOISE2  1                  SIN(0V 2VPEAK 2.5KHZ)
*
* COMPARATOR
R1      2      3      1K
R2      3      6      5K
ROL    5      6      1000
D1      7      6      DZ1
D2      7      0      DZ2
*
* REFERENCE VOLTAGE

```

```

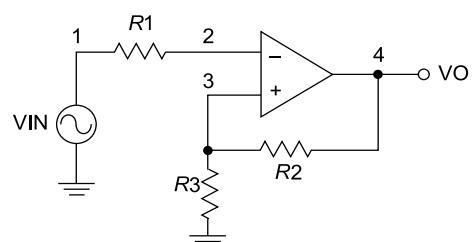
VREF   4      0      0V
XOA    3      4      5      OA
*
* OPAMP MACRO MODEL, SINGLE-POLE WITH 15V OUTPUT +CLAMP
* connections: non-inverting input
*           | inverting input
*           |           | output
*           |           |
.SUBCKT OA      1      2      6
* INPUT IMPEDANCE
RI     1      2      10MEG
* DC GAIN=100K AND POLE1=100HZ
* UNITY GAIN = DCGAIN X POLE1 = 10MHZ
EA     3      0      1      2      100K
RP1    3      4      100K
CP1    4      0      0.0159UF
* ZENER LIMITER
D1     4      7      DZ0
D2     0      7      DZ0
* OUTPUT BUFFER AND RESISTANCE
EBUF   5      0      4      0      1
RO     5      6      10
*
* 15V ZENER DIODE MODEL
.model DZ0  D(Is=0.05u Rs=0.1 Bv=15 Ibv=0.05u)
.ENDS
*
* ZENER DIODE MODEL
.model DZ1  D(Is = 0.05u Rs = 0.1 Bv = 4.3 Ibv = 0.05u)
.model DZ2  D(Is = 0.05u Rs = 0.1 Bv = 4.3 Ibv = 0.05u)
*
* TRANSIENT ANALYSIS
.TRAN      0.1MS      34MS
*
* PRINT RESULTS
.PRINT TRAN      V(2)      V(6)
.PROBE
.END

```

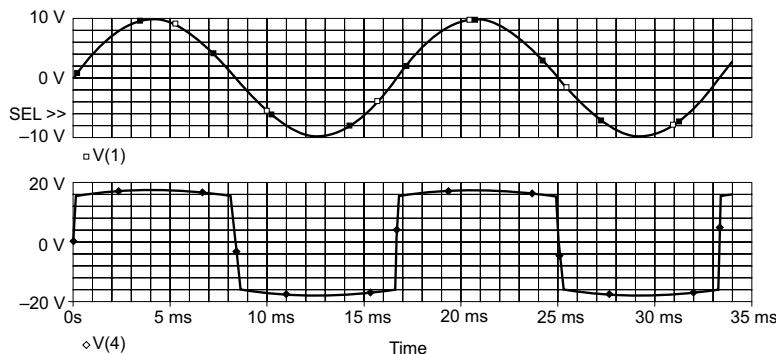
### Example 14.10

Schmitt Trigger using op-amp

The basic comparator is used in open-loop mode that is vulnerable to false triggering at the output even due to a few tens of millivolts peak of the input. The Schmitt Trigger avoids such an unwanted triggering. Figure 14.21 shows the inverting Schmitt trigger circuit. The PSpice netlist given below is simulated and the input and output waveforms are shown in Fig. 14.22.



**Fig. 14.21** Schmitt trigger circuit



**Fig. 14.22** Input and output waveforms

#### SCHMITT\_TRIGGER.CIR

```

VIN      1      0      SIN (0V 10VPEAK 60HZ)
R1       1      2      1K
R2       4      3      50K
R3       3      0      1K
XOA2    2      3      4      OPAMP1
*
* OPAMP MACRO MODEL, SINGLE-POLE WITH 15V OUTPUT
* CLAMP
* connections:      non-inverting input
*                      |      inverting input
*                      |      |      output
*                      |      |
.SUBCKT OPAMP1      1      2      6
* INPUT IMPEDANCE
RIN     1      2      10MEG
* DC GAIN=100K AND POLE1=100HZ
* UNITY GAIN = DCGAIN X POLE1 = 10MHZ
EGAIN    3      0      1      2      100K
RP1      3      4      100K
CP1      4      0      0.0159UF
* ZENER LIMITER
D1       4      7      DZ0
D2       0      7      DZ0
* OUTPUT BUFFER AND RESISTANCE
EBUFFER   5      0      4      0      1
ROUT5     6      10
*
*
* 15V ZENER DIODE MODEL
.model DZ0  D(Is=0.05u Rs=0.1 Bv=15 Ibv=0.05u)
.ENDS
*
* ZENER DIODE MODEL
.model DZ1  D(Is = 0.05u Rs = 0.1 Bv = 4.3 Ibv = 0.05u)
.model DZ2  D(Is = 0.05u Rs = 0.1 Bv = 4.3 Ibv = 0.05u)
*
```

```

* ANALYSIS
.TRAN          0.1MS      34MS
*
* VIEW RESULTS
.PRINT TRAN      V(2)      V(6)
.PLOT TRAIN V(1) V(4)
.PROBE
.END

```

### Example 14.11

#### Instrumentation Amplifier using 3 Op-amps

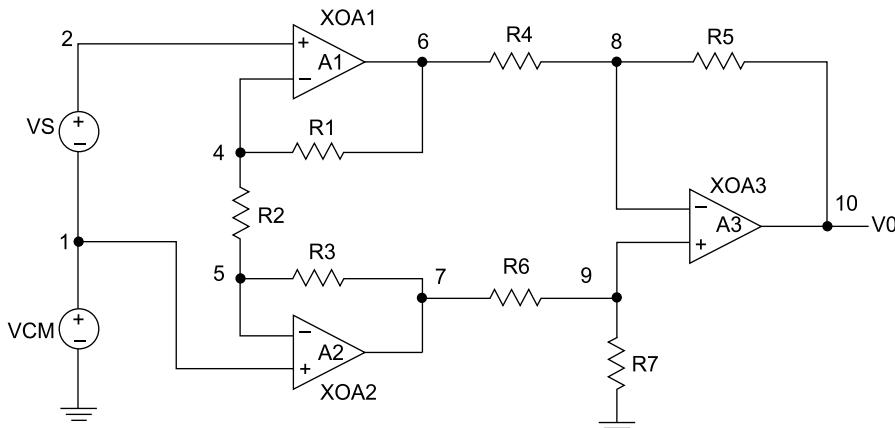
The instrumentation amplifiers basically consist of buffering amplifiers for the two inputs A1 and A2, and a basic differential amplifier formed by A3. The differential amplifier makes it possible to employ the sensors in measurement systems. A sensor produces a minimum amount of some form of electrical signal between its terminals. However, there are some applications requiring neither of the terminals to be connected to the ground potential of the measuring circuit. The terminals may be biased at a high potential or a possible noise voltage may override the signal levels. The differential amplifier used in the instrumentation amplifier senses the signal by directly measuring the difference between the two terminals of the sensor.

The buffer amplifiers A1 and A2 provide the necessary gain, and they also isolate the sensor resistance and the circuit resistances from each other.

**Signal Gain** The instrumentation amplifier offers two useful functions namely, the amplification of the difference between the two inputs and they reject the common mode signal at the inputs. The op-amps A1 and A2 provide the signal gain and the op-amp A3 normally forms a differential gain of 1. Therefore the overall gain is given by

$$\frac{V_O}{V_S} = \left( 1 + 2 \frac{R_1}{R_2} \right) \frac{R_5}{R_1}$$

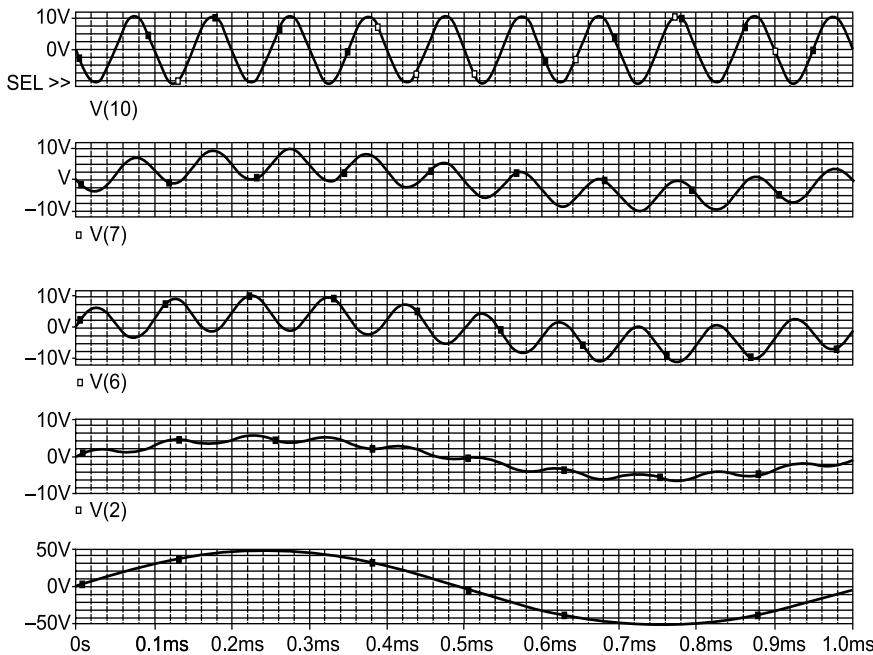
where  $R_1=R_3$  and  $\frac{R_5}{R_4} = \frac{R_7}{R_6}$  for the circuit shown in Fig. 14.23.



**Fig. 14.23** Instrumentation amplifier using 3 op-amps

### Spice file

The Spice netlist for a 3 op-amp instrumentation amplifier is shown below and the output waveforms as obtained at the output with a sinusoidal input of 10 kHz and 1 kHz of amplitudes 1 V and 5 V peak-to-peak respectively is shown in Fig. 14.24.



**Fig. 14.24** Input and output signals

```

INSTAMP1.CIR - 3 OPAMP INSTRUMENTATION AMPLIFIER
*
VS          2      1      SIN(0    1      10kHz)
VCM         1      0      SIN(0    5      1kHz)
*
* BUFFERED AMPLIFIER
XOA1        2      4      6      OA
R1          4      6      10K
R2          4      5      2K
R3          5      7      10K
XOA2        1      5      7      OA
*
* DIFFERENTIAL AMPLIFIER
R4          6      8      10K
R5          8      10     10K
R6          7      9      10K
R7          9      0      10K
XOA3        9      8      10     OA
*
* OPAMP MACRO MODEL, SINGLE-POLE WITH 15V OUTPUT
* CLAMP

```

```

* connections:      non-inverting input
*                   |      inverting input
*                   |      |      output
*                   |      |      |
*.SUBCKT OA          1      2      6
* INPUT IMPEDANCE
RIN    1      2      10MEG
* DC GAIN=100K AND POLE1=100HZ
* UNITY GAIN = DCGAIN X POLE1 = 10MHZ
EA     3      0      1      2      100K
RP1    3      4      100K
CP1    4      0      0.0159UF
* OUTPUT BUFFER AND RESISTANCE
EBUF    5      0      4      0      1
RO      5      6      10
.ENDS
* TRANSIENT ANALYSIS FOR 1MS WITH A TIME STEP OF
* 0.01MS
.TRAN          0.01MS      1.0MS
* PRINT RESULTS
.PLOT TRAN      V(2)      V(10)
.PRINT TRAN     V(2)      V(10)
.PROBE
.END

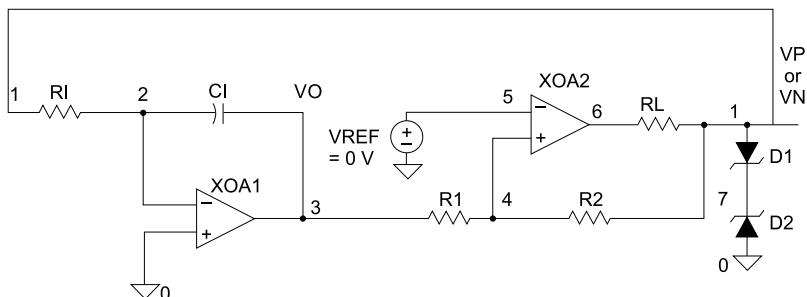
```

### **Example 14.12**

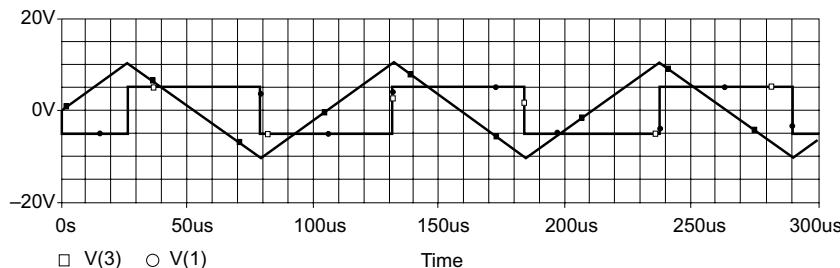
## *Triangular Wave Generator*

The circuit diagram of a triangular wave generator using 2 op-amps A1 and A2 is shown in Fig. 14.25. This circuit provides a triangular waveform at Pin 6 of op-amp A2 with +ve and -ve saturation voltages as set by the Zener diodes D1 and D2, and a triangular wave at the output pin of op-amp XOA1.

The capacitor C1 acts as the integrating capacitor of the integrator circuit formed by op-amp A1. Therefore, the frequency of the triangular wave signal is determined by the resistor R1 and the Capacitor C1 in coordination with the comparator formed by the op-amp XOA2. The comparator sets the upper and lower threshold voltages with the use of potential divider circuit formed by the resistors R1 and R2, and Zener diodes D1 and D2. The netlist for an op-amp triangular wave generator is given below. The triangular and square-wave outputs are shown in Fig. 14.26.



**Fig. 14.25** Triangular wave generator circuit



**Fig. 14.26** Triangular and square-wave outputs of triangular wave generator

### Spice file

```

OP_TRI_GEN.CIR - OPAMP TRIANGULAR WAVE GENERATOR
*
* INTEGRATOR
RI      1      2      12.5K
CI      3      2      0.001UF      IC=0.1
XOA1    0      2      3      OA
*
* COMPARATOR WITH HYSTERESIS
R1      3      4      20K
R2      4      1      10K
XOA2    4      5      6      OA
RL      6      1      1000
D1      1      7      DZ1
D2      0      7      DZ1
*
* REFERENCE VOLTAGE
VREF    5      0      0V
*
* OPAMP MACRO MODEL, SINGLE-POLE WITH 15V OUTPUT
* CLAMP
* connections:      non-inverting input
*                      |      inverting input
*                      |      |      output
*                      |      |      |
.SUBCKT    OA    1      2      6
* INPUT IMPEDANCE
RI          1      2      10MEG
* DC GAIN=100K AND POLE1=100HZ
* UNITY GAIN = DCGAIN X POLE1 = 10MHZ
EA      3      0      1      2      100K
RP1      3      4      100K
CP1      4      0      0.0159UF
* ZENER LIMITER
D1          4      7      DZLIM
D2          0      7      DZLIM
* OUTPUT BUFFER AND RESISTANCE

```

```

EBUF      5     0     4     0     1
RO        5     6     10
*
* ZENER TO LIMIT OPAMP OUTPUT SWING (+/- 15v)
.model DZLIM      D(Is=0.05u Rs=0.1 Bv=14.3 Ibv=0.05u)
.ENDS
*
* ZENER TO LIMIT COMPARATOR OUTPUT SWING
.model DZ1       D(Is=0.05u Rs=0.1 Bv=4.3 Ibv=0.05u)
*
* TRANSIENT ANALYSIS
.TRAN      500NS      300US
*
* PRINT RESULTS OF TRANSIENT ANALYSIS
.PRINT TRAN      V(3)    V(1)
.PROBE
.END

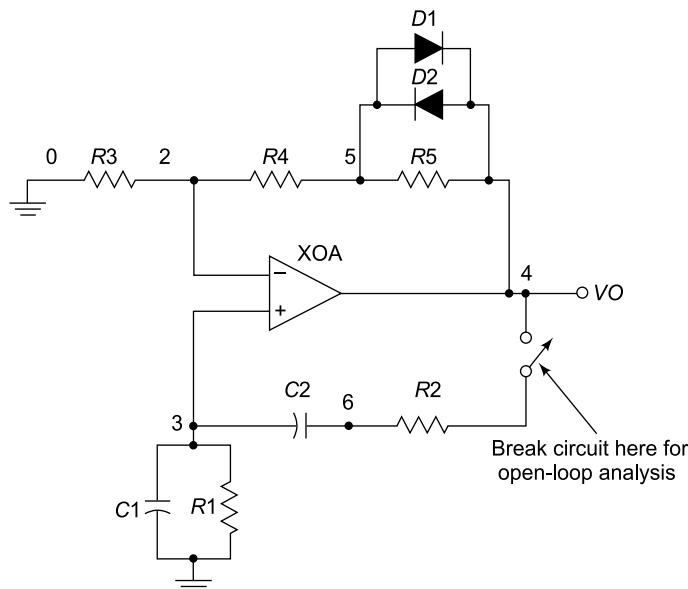
```

### Example 14.13

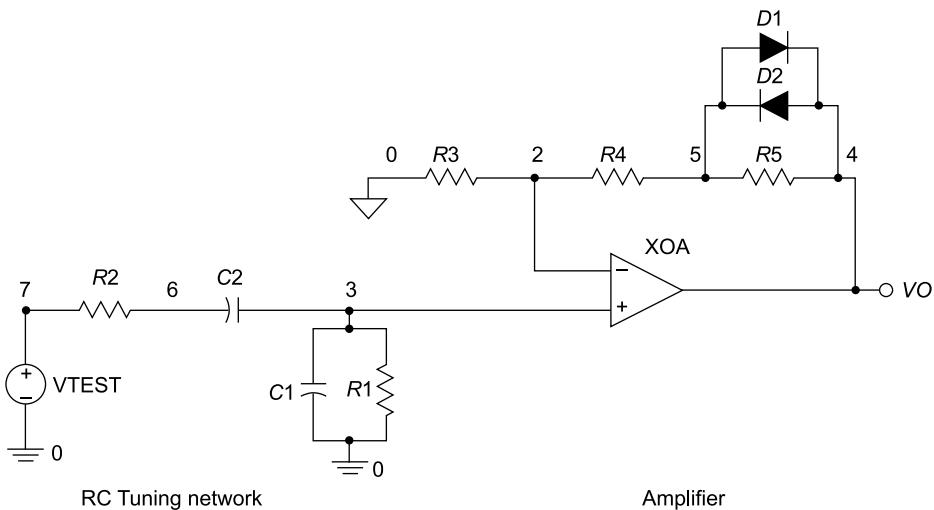
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#### Wien Bridge Oscillator

The Wien Bridge oscillator circuit using op-amp is shown in Fig. 14.27. When the AC gain around the opened loop is 1 V/V and the total phase shift achieved is  $-360$  or  $0$  deg, the circuit will oscillate at that particular frequency. The oscillator can be tested by opening the connection at the test point for finding its open-loop circuit diagram is shown in Fig. 14.28.



**Fig. 14.27** Wien Bridge Oscillator circuit diagram to study open-loop analysis



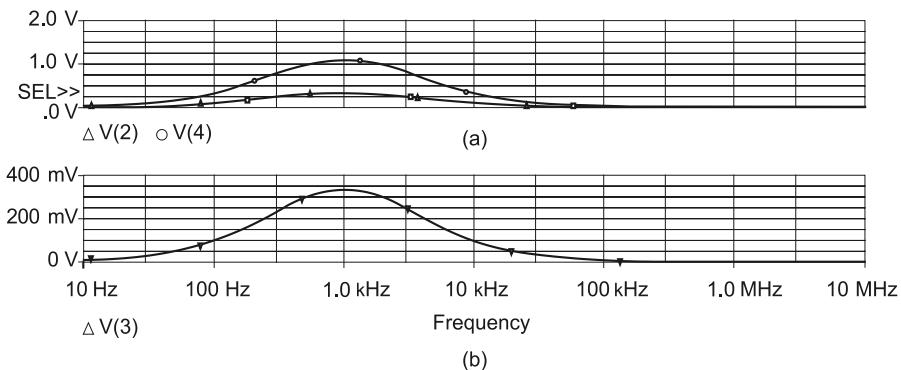
**Fig. 14.28** Wien Bridge Oscillator circuit diagram

The two basic sections of the Wien-bridge oscillator are the RC tuning network and the op-amp amplifier. The RC network is characterised by a centre frequency as given by

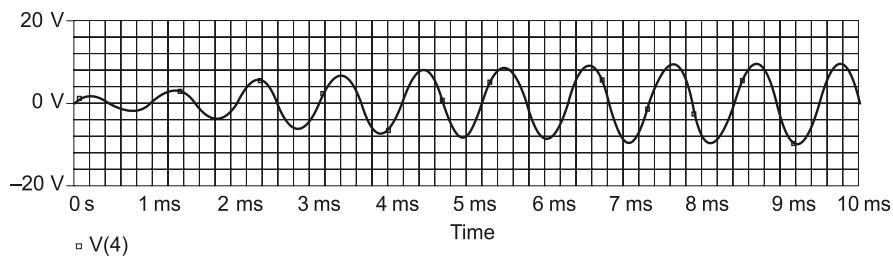
$$fO = \frac{1}{2\pi \times R \times C}$$

When  $R=R_1=R_2$  and  $C=C_1=C_2$ , at the centre frequency, the phase shift becomes 0 and the magnitude reaches a peak of  $1/3$  V.

The netlist shown below is stored with \*.cir extension. The PSPICE simulation is run and the trace at V(3) is shown in Fig. 14.29(a). For the given values of  $R1=R2=10k\Omega$  and  $C1=C2=16nF$ , the centre frequency is seen to be approximately 1kHz. The phase is shown in Fig. 14.29 (b). The spice netlist for the oscillator circuit with the closed-loop can be stored with a \*.cir extension and the simulation is run for the transient analysis and the frequency output plot at V(4) is shown in Fig. 14.30.



**Fig. 14.29** (a) and (b) Frequency and Phase response characteristics



**Fig. 14.30** Oscillation frequency output

The design of the circuit can be made for different oscillation frequencies by setting the values of resistors and capacitors.

### Spice file

```

WIEN-BRIDGE OSCILLATOR OPEN-LOOP ANALYSIS
*
VTEST      7      0      AC      1
*
* RC TUNING
R2          7      6      10 K
C2          6      3      16 NF
R1          3      0      10 K
C1          3      0      16 NF
* NON-INVERTING OPAMP
R3          0      2      10 K
R4          2      5      18 K
XOA         3      2      4      OA
* AMPLITUDE STABILIZATION
R5          5      4      5K
D1          5      4      D1N914
D2          4      5      D1N914
.model      D1N914 D(Is=0.1p Rs=16 CJO=2p Tt=12n Bv=100
+Ibv=0.1p)
*
* OPAMP MACRO MODEL, SINGLE-POLE WITH 15V OUTPUT
* CLAMP
* connections:      non-inverting input
*                      |      inverting input
*                      |      |      output
*                      |      |      |
.SUBCKT    OA     1      2      6
* INPUT IMPEDANCE
RIN         1      2      10MEG
* GAIN BW PRODUCT = 10MHZ
* DC GAIN (100K) AND POLE 1 (100HZ)
EGAIN       3      0      1      2      100K
RP1         3      4      1K

```

```

CP1      4      0      1.5915UF
* OUTPUT BUFFER AND RESISTANCE
EBUFFER 5      0  4      0      1
ROUT    5      6      10
.ENDS
*
* ANALYSIS
.AC      DEC 10 10 10MEG
* VIEW RESULTS
.PRINT AC      VM(3) VP(3)
.PLOT   AC      VM(3) VP(3)
.PROBE
.END

```

### **Spice file**

```

OPAMP WIEN-BRIDGE OSCILLATOR
*
* CURRENT PULSE TO START OSCILLATIONS
IS      0      3      PWL(0US 0MA 10US 0.1MA 40US
+ 0.1MA 50US 0MA 10MS 0MA)
*
* RC TUNING
R2      4      6      10K
C2      6      3      16NF
R1      3      0      10K
C1      3      0      16NF
* NON-INVERTING OPAMP
R3      0      2      10K
R5      2      5      18K
XOP    3  2  4      OPAMP1
* AMPLITUDE STABILIZATION
R6      5      4      5K
D1      5      4      D1N914
D2      4      5      D1N914
*
.model  D1N914 D(Is=0.1p Rs=16 CJO=2p Tt=12n Bv=100
+Ibv=0.1p)
*
* OPAMP MACRO MODEL, SINGLE-POLE WITH 15V OUTPUT
* CLAMP
* connections:      non-inverting input
*                  |      inverting input
*                  |      |      output
*                  |      |      |
.SUBCKT OA 1 2 6
* INPUT IMPEDANCE
RIN      1      2      10MEG
* GAIN BW PRODUCT = 10MHZ
* DC GAIN (100K) AND POLE 1 (100HZ)
EGAIN    3  0  1  2      100K

```

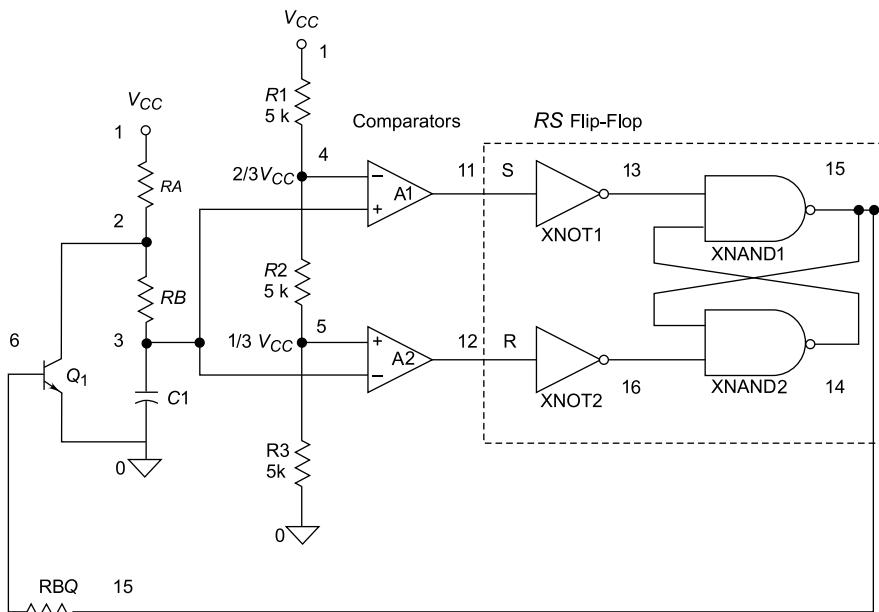
```

RP1          3          4          1K
CP1          4          0          1.5915 UF
* OUTPUT BUFFER AND RESISTANCE
EBUFFER      5  0  4  0  1
ROUT         5          6          10
.ENDS
*
* ANALYSIS
.TRAN      0.05MS 10MS
*
* VIEW RESULTS
.PRINT    TRAN      V(4)
.PLOT      TRAN      V(4)
.PROBE
.END

```

**Example 14.14***555 Timer-IC Simulation*

The circuit shown in Fig. 14.31 simulates the timer IC 555 for an astable multivibrator operation. The op-amps A1 and A2 form the upper and lower comparators. The RS flip-flop is formed by the use of two invertors and two NAND gates. The discharge transistor Q1 is connected with the output of the flip-flop. The charging path is formed by the resistors RA and RB and the discharge is done through the resistor RA and the discharge transistor Q1.



**Fig. 14.31** The detailed IC timer circuit for simulation

Figure 14.32 shows a simplified schematic of Fig. 14.31. The Spice circuit netlist is formed and saved with a \*.cir extension. The simulation output shown in Fig. 14.33 is obtained for the component values shown in the netlist below.

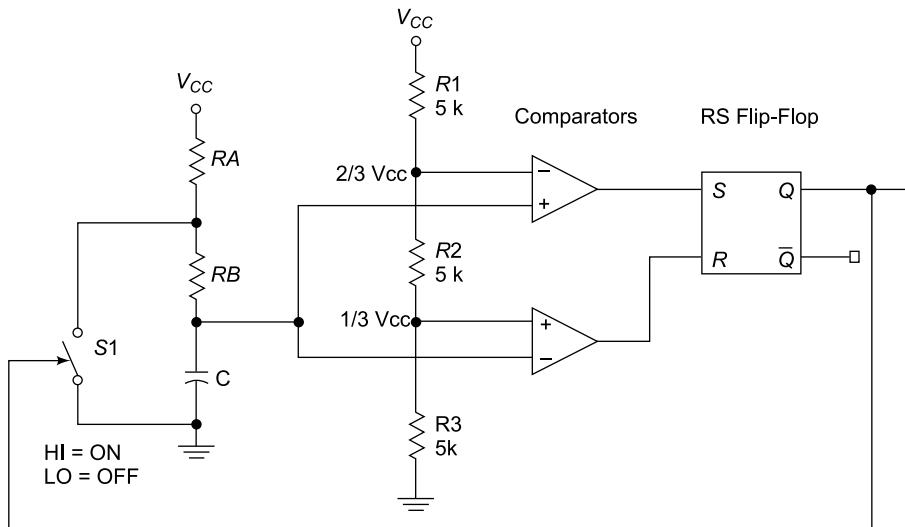
### Spice file

```
555_TIMER1.CIR - ASTABLE MODE
```

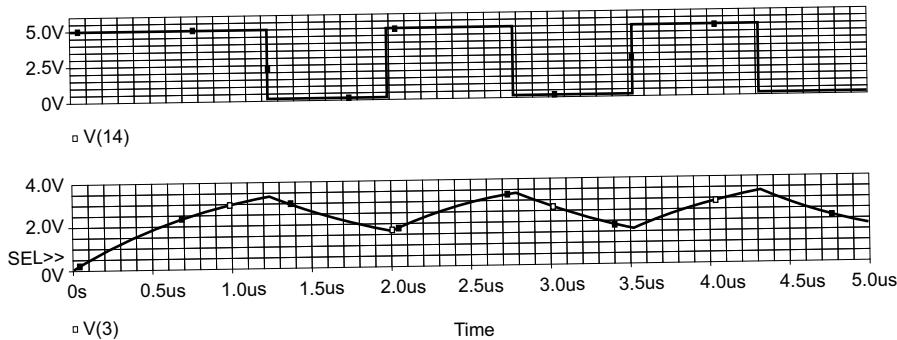
```
*
```

```
VCC 1 0 5V
```

```
*
```



**Fig. 14.32** Block schematic of Timer IC 555



**Fig. 14.33** The timer output and the charging and discharging waveforms

```
* EXTERNAL TIMING COMPONENTS
```

```
RA 1 2 1K
```

```
RB 2 3 10K
```

```
C1 3 0 100PF
```

```
*
```

```
* DISCHARGE TRANSISTOR
```

```

Q1      2      6      0      QNOM
RBQ    15     6      15K
*
* 1/3 AND 2/3 VCC DIVIDER
R1      1      4      5K
R2      4      5      5K
R3      5      0      5K
*
* COMPARATORS
XCMPI 3      4      11      COMP1
XCMPI 5      3      12      COMP1
*
* RS FLIP-FLOP
XNOT1   11     13      NOT1
XNOT2   12     16      NOT1
XNAND1  13     14      15      NAND1
XNAND2  15     16      14      NAND1
*
* SUBCIRCUITS AND MODELS
*
.SUBCKT NAND1  2      3      4
* TERMINALS A B OUT VCC
RL      3      4      500
CL      3      0      10PF
S1      3      5      10      SW
S2      5      0      20      SW
.ENDS
*
.SUBCKT NOT1   3      4
* TERMINALS A OUT VCC
RL      3      4      500
CL      3      0      10PF
S1      30     10      SW
.ENDS
*
* OPAMP MACRO MODEL, SINGLE-POLE WITH 15V OUTPUT
* CLAMP
* connections:      non-inverting input
*                      |      inverting input
*                      |      |      output
*                      |      |      |
.SUBCKT OA      1      2      6
* INPUT IMPEDANCE
RIN      1      2      10MEG
* GAIN BW PRODUCT = 10MHZ
* DC GAIN (100K) AND POLE 1 (100HZ)
EGAIN    3      0      1      2      100K
RP1      3      4      1K
CP1      4      0      1.5915UF
* OUTPUT BUFFER AND RESISTANCE

```

```

EBUFFER      5    0    4    0    1
ROUT        5          6          10
.ENDS
*
.SUBCKT COMP1      1    2    5
* TERMINALS: 1-INPUT+, 2-INPUT-, 5-OUTPUT
* DIFF AMP WITH HYSTERESIS
EDIFF 3    0    VALUE = { V(1) - V(2) + V(5)/500 }
* LOW-PASS FILTER
RP1   3    4    200
CP1   4    0    100PF
* LIMITER
EOUT  5    0    TABLE {V(4)} = (-1MV 0V) (1MV, 5V)
.ENDS
*
.MODEL     SW     VSWITCH(VON = 3 VOFF = 2 RON = 10
+ROFF = 100K)
.model    QNOM    NPN(BF = 100)
*
* ANALYSIS ****
*.TRAN      500NS      5US      UIC
* THE INITIAL CONDITIONS FOR THE NODES
*.IC V(15)=0V V(14)=5V V(3)=0V
*
* PRINT RESULTS
*.PRINT      TRAN V(3) V(14)
*.PROBE
.END

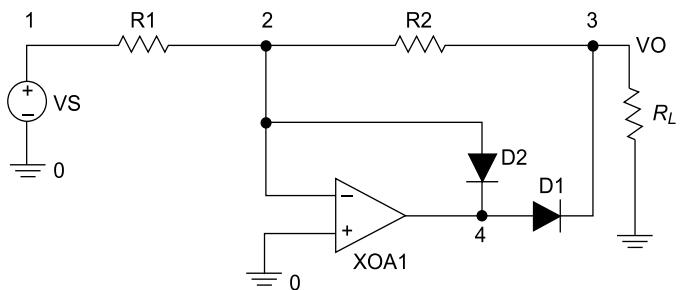
```

### Example 14.15

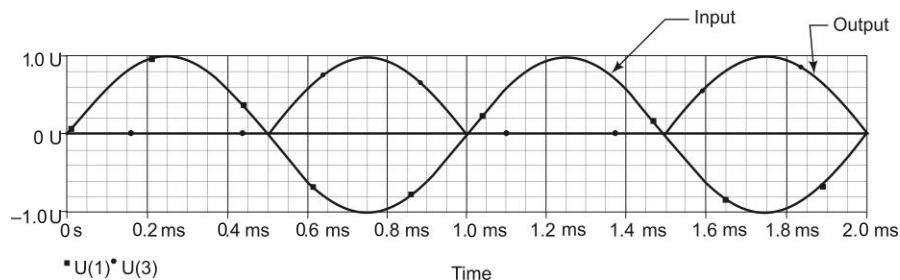
#### Op-amp Precision Half-wave Rectifier

Rectifiers using op-amp are used in applications involving measurement of signals of low strength, with voltages of the order of microvolts and to rectify AC voltage signal of value less than the forward or cut-in voltage of a diode. The advantage of op-amp circuits lies in their ability to compensate for non-linear devices in the feedback loop. Combining the rectifying action of a diode with the accuracy of an op-amp, precision half-wave and full-wave rectifiers can be constructed. Figure 14.34 shows the circuit diagram of an inverting half-wave rectifier using an op-amp.

The diode in series with the output terminal of the op-amp acts as the rectifying diode. The netlist of the circuit is shown below with the input and output waveforms as shown in Fig. 14.35.



**Fig. 14.34** Precision half-wave rectifier circuit



**Fig. 14.35** Input and output waveforms of the half-wave rectifier

It can be noted that, to change the gain of the rectified output voltage, the feedback and input resistance values can be changed, and for varying the polarity of the output waveform, the diodes can be interchanged for their polarities.

### PSpice file

```

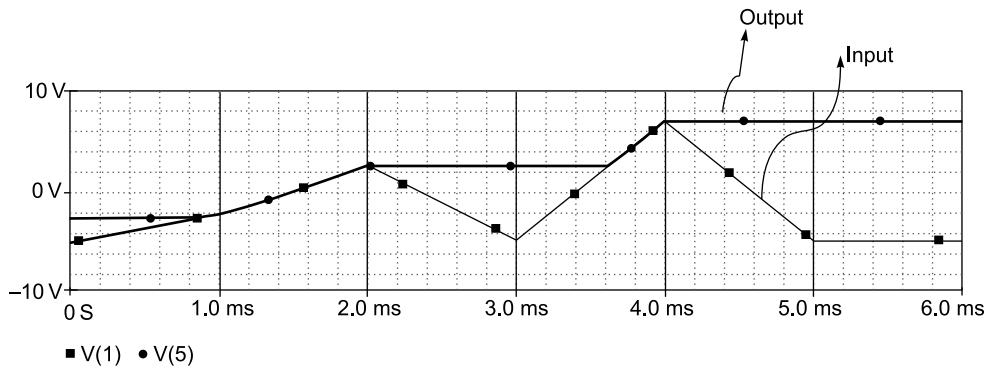
OP_HW_RECTIFIER.CIR - OPAMP HALF-WAVE RECTIFIER
*the input sinusoidal signal of 1kHz frequency with 1V peak
VS      1      0      SIN(0V 1VPEAK 1KHZ)
*
* HALF WAVE RECTIFIER
R1      1      2      10K
R2      2      3      10K
XOA1    0      2      4      OA
D1      4      3      D1N4148
D2      2      4      D1N4148
*
RL      3      0      100K
*
*
* SIMPLE DIODE RECTIFIER USIND DIODE
D3      1      5      D1N4148
RL2    5      0      100K
*
* DIODE MODEL
.model   D1N4148      D(Is=0.1p Rs=16 CJO=2p Tt=12n Bv=100
+Ibv=0.1p)
*
*
*
* OPAMP MACRO MODEL, SINGLE-POLE WITH 15V OUTPUT CLAMP
* connections:      non-inverting input
*                  |      inverting input
*                  |      |      output
*                  |      |      |
.SUBCKT OA 1 2 6
* INPUT IMPEDANCE
RIN     1 2 10MEG
* GAIN BW PRODUCT = 10MHZ

```

```

* DC GAIN (100K) AND POLE 1 (100HZ)
EGAIN      3  0    1   2   100K
RP1        3      4      1K
CP1        4      0     1.5915UF
* OUTPUT BUFFER AND RESISTANCE
EBUFFER    5  0    4   0   1
ROUT       5  6    10
.ENDS
*
* TRANSIENT ANALYSIS
.TRAN      5US 2000US 0US 5US
*.TRAN     0.1US 20US 0US 0.1US
*
* VIEW RESULTS
.PRINT    TRAN      V(1) V(3)
.PROBE
.END

```



**14.36** Input and output waveforms of peak detector

## SUMMARY

---

- ❑ SPICE is the acronym for Simulation Program with Integrated Circuit Emphasis.
- ❑ The nodal analysis forms the heart of any SPICE programming.
- ❑ The netlist is described in SPICE as a set of element lines that define the circuit topology and the element values to be connected.
- ❑ A set of control lines defines the model parameters.
- ❑ The first line always indicates the title or reference to the circuit, and the last line is the end of the program *.END*.
- ❑ Rules for circuit description are
  - Node identifiers or numbers must be non-negative integers
  - The ground node (0 Volts) must be numbered zero
  - Device names can be up to 8 characters in length
  - The first letter of a device name identifies the device type. For example, ‘R’ for resistor, ‘C’ for capacitor, ‘M’ for MOSFET, ‘V’ for independent voltage source and ‘I’ for independent current source
  - Values can be expressed as integers or floating point numbers. The following abbreviations are normally employed:

tera :  $1 \times 10^12$

kilo :  $1 \times 10^3$

nano :  $1 \times 10^{-9}$

giga :  $1 \times 10^9$       milli :  $1 \times 10^{-3}$       pico :  $1 \times 10^{-12}$   
 mega :  $1 \times 10^6$       micro :  $1 \times 10^{-6}$       femto :  $1 \times 10^{-15}$

- Comments can be inserted into the circuit description by beginning the statement with an asterisk '\*' as the first character
- The components in Spice are identified as follows:
  - Resistors  
R\_NAME N1 N2 VALUE <TC=TC1<,TC2>>
  - Capacitors  
C\_NAME N+ N- VALUE <IC=INCOND>
  - Inductors  
K\_NAME L1 L2 VALUE
  - Transmission Lines  
 $T\_NAME\ N1\ N2\ N3\ N4\ Z0=VALUE\ <TD=VALUE>\ <F=FREQ+\<NL=NRMLEN>>+\<IC=V1,\ II,\ V2,\ I2>$
- The sources are identified as follows:
  - Linear Dependent Sources  
 $i=g^*v, v=e^*v, i=f^*i, v=h^*I$   
where g, e, f and h are constants representing transconductance, voltage gain, current gain and transresistance respectively.
  - Linear Voltage-Controlled Current Sources G\_NAME N+ N- NC+ NC- VALUE
  - Linear Voltage-Controlled Voltage Sources  
E\_NAME N+ N- NC+ NC- VALUE
  - Linear Current-Controlled Current Sources  
F\_NAME N+ N- VNAM VALUE
  - Linear Current-Controlled Voltage Sources  
H\_NAME N+ N- VNAM VALUE
  - Independent Sources  
V\_NAME N+ N- <<DC> DC/TRAN VALUE> <AC <ACMAG +<ACPHASE>>> IYYY N+ N- <<DC> DC/TRAN VALUE> +<AC <ACMAG <ACPHASE>>>
  - Pulse Voltage Source  
PULSE (V1 V2 TD TR TF PW PER)
  - Sinusoidal Voltage Source  
SIN(VO VA FREQ TD THETA)
  - Exponential Voltage Source  
EXP (V1 V2 TD1 TAU1 TD2 TAU2)
  - Piece-wise Linear Voltage Source  
PWL(T1 V1 ..... )
  - Single Frequency FM Voltage Source  
SFFM(VO VA FC MDI FS)
- The semiconductor devices are identified typically by the model parameters as follows:
  - Junction Diode  
D\_NAME N+ N- MNAME <AREA> <OFF> <IC=VD>
  - Bipolar Junction Transistor  
Q\_NAME NC NB NE <NS> MNAME <AREA> <OFF> <IC=VBE, VCE>
  - Junction Field Effect Transistor (JFET)  
J\_NAME ND NG NS MNAME <AREA> <OFF> <IC=VDS, VGS>
  - Metal Oxide Semiconductor Field Effect Transistor  
M\_NAME ND NG NS NB MNAME <L=VAL> <W=VAL> <AD=VAL> +<AS=VAL><PD=VAL><PS=VAL>

- ❑ A typical model card is identified by
  - .MODEL Card  
 $.MODEL MNAME TYPE(PNAME1=PVAL1 PNAME2=PVAL2 \dots)$
- ❑ BASIC ANALYSES TYPES
  - DC Analysis
    - .DC
    - .TF
    - .OP
    - .SENS
  - ❑ AC Small Signal Analysis
    - .AC
    - .NOISE
  - ❑ Transient Analysis
    - .TRAN
    - .FOUR
  - ❑ Pole-Zero Analysis
  - ❑ Small Signal Distortion Analysis
  - ❑ Other statements:
    - .IC – Initial Transient Conditions  
 $.IC \{ \{node\} = \{value\} \}$
    - .MODEL – Device Model.  
 $.MODEL \{name\} \{type\}$
    - .NODESET – Initial bias point guess.  
 $.NODESET \{ \{node\}=\{value\} \}$
    - .PRINT – Print Output  
 $.PRINT PRTYPE OV1 <OV2 \dots OV8>$
    - .PLOT  
 $.PLOT PL\_TYPE OV1 <(PLO1,PHI1)> <OV2 <(PLO2,PHI2)> \dots +OV8>$
    - .PROBE  
 $.PROBE [output variable names]$
    - .SUBCKT – Subcircuit Definition  
 $.SUBCKT SUB_CIRCUIT_NAME N1$
    - .ENDS  
 $.ENDS$
    - Subcircuit Calls  
 $X\_NAME\_OF\_SUBCKT N1 SUBNAM$
- ❑ CONTROL STATEMENTS
  - .TEMP  
 $.TEMP <TI >$
  - .OPTIONS  
 $.OPTIONS OPT1 OPT2 \dots (or OPT = OPTVAL \dots)$
- ❑ Schematic is a design entry program available to prepare the circuit for simulation. It involves the following steps :
  - placing and connecting part symbols
  - defining component values and other attributes
  - defining input waveforms
  - enabling one or more analyses
  - identifying the points in the circuit where we want to see results
- ❑ Probe is a graphical results analyser. When PSpice A/D completes the simulation, Probe plots the waveform results.

The general files associated with simulation are Netlist file, Circuit file, Model library, Probe data file and PSpice output file.

The shortcuts that the user uses while programming with the ORCAD PSPICE are as follows:

■ To save after <i>each</i> editing:	Ctrl+S
■ To simulate ( <i>after saving each editing</i> ):	F11
■ To rotate an element, i.e. a resistor:	Ctrl+R
■ To get a new part from the “Draw” menu:	Ctrl+G
■ To copy an element instead of pulling from menu:	Ctrl+C
■ To paste element into place:	Ctrl+V
■ To draw connecting wires:	Ctrl+W
■ To discontinue using element:	Esc

The three basic stages in the model of an op-amp are (i) a differential amplifier, (ii) a voltage gain stage with single-pole frequency roll-off and (iii) an output buffer. The behaviours are defined as follows:

Input Impedance	RI
Differential Gain	EA
Single Pole Frequency identified by	RP1, CP1
Output Impedance	RO

The op-amp OA Subcircuit definition is given by

```
* OP-AMP OA MACRO MODEL, SINGLE-POLE
* connections:      non-inverting input
*                      |      inverting input
*                      |      |      output
*                      |      |
.SUBCKT      OA   1       2       6
* INPUT IMPEDANCE
RI          1       2       10MEG
* DC GAIN=100K AND POLE1=100HZ
```

```
* UNITY GAIN = DCGAIN X POLE1 = 10MHZ
EA          3       0       1       2       100K
RP1         3       4       1K
CP1         4       0       1.5915UF
* OUTPUT BUFFER AND RESISTANCE
EBUF        5       0       4       0       1
RO          5       6       10
.ENDS
```

## REVIEW QUESTIONS

---

1. What is SPICE? Where is it used?
2. Give an overview of the SPICE algorithm and explain.
3. What are the major devices available in any SPICE software? Name them and list the corresponding element cards.
4. What are the types of analysis that can be carried out with SPICE software?
5. Produce the important features DC analysis, AC analysis, Transient analysis, and pole-zero analysis.
6. What are the types of outputs obtainable from SPICE? List them and explain how to control the outputs.
7. Explain the schematic capture feature of ORCAD software.
8. What is a ‘netlist’?

**Note:** Use the op-amp model introduced in the text for the following questions.

9. Using Example 14.1 design an op-amp inverting amplifier for a gain of (a) 20 and (b) 10. Identify the component values.
10. Design a variable gain inverting amplifier using op-amp for a range of 1 to 10. Use a single potentiometer and a fixed resistor. Identify the values and run the PSPICE analysis.
11. Design a circuit for the expression  $V_o = V_1 + V_2 + V_3$ . Produce the netlist and simulate.
12. An ideal op-amp as shown in Fig. 14.7 is to be used with inputs,  
$$V_1 = 1V, V_2 = 2V \text{ and } V_3 = 10V$$
  
(a) When  $R_1 = 10\text{ k}\Omega$ ,  $R_2 = 2\text{k }\Omega$   $R_3 = 10\text{ k}\Omega$  and  $R_f = 10\text{ k}\Omega$  find the output voltage using PSPICE. Compare the result with that obtained theoretically. (b) Run the PSPICE analysis with  $R_1 = R_2 = R_3 = 10\text{ k}\Omega$ , observe the results and comment on the output.
13. For the differentiator circuit shown in Fig. 14.12, neglect the values of  $R_1$ , assume  $C = 5\text{ }\mu\text{f}$  and  $R_2 = 20\text{ k}\Omega$  and for the same input as given in Example 14.4, run the PSPICE analysis and verify the output. Then, using  $C = 50\text{ }\mu\text{f}$  and  $R_2 = 10\text{ k}\Omega$  run the analysis again. Explain the difference between the two results.
14. Run the PSPICE analysis for the circuit shown in Fig. 14.15 for the source  $v_i$  as given by  $\sin(01\text{ V }10\text{Hz})$ . Use  $R_1 = 1\text{ }\Omega$ .  $C_1 = 2\text{ fF}$ . Assume zero initial conditions.
15. Design a first order low pass filter using op-amp with a cut-off frequency of  $f_0 = 5\text{ kHz}$ . Use standard components for the circuit. Run the PSPICE analysis and verify the design.
16. Referring to Example 14.7 construct a high pass filter by interchanging  $R_2$  and  $R_3$  with  $C_1$  and  $C_2$ . Verify the theoretical and practical values of lower cut-off frequency of the high-pass filter.
17. Design an instrumentation amplifier for a gain of 1000. Use standard components. Run the PSPICE analysis and verify the results with 1 mV sinusoidal input signal of frequency 1 kHz.
18. Run the PSPICE analysis for the IC timer circuit shown in Fig. 14.29 and prepare the netlist for wave output with duty cycle of 50%. Verify the results with theoretical values.
19. Design a precision half-wave rectifier circuit and simulate for an input of 2 kHz sinusoidal clock with 100 mV amplitude. Design for the maximum amount of gain possible. Identify the resistor values.
20. Use SPICE software to identify the response of the following inputs to the integrator circuit. (a) Sinusoidal input of 100 kHz frequency and amplitude of 1 V, (b) square wave input of 100 kHz frequency and amplitude of 1 V, and (c) triangular wave of 100 kHz frequency and amplitude of 1 V. Assume 0 V dc offset for the above signals.
21. Use SPICE software to identify the response of the following inputs to the differentiator circuit.  
(a) Sinusoidal input of 100 kHz frequency and amplitude of 1 V, (b) square wave input of 100 kHz frequency and amplitude of 1 V, and (c) triangular wave of 100 kHz frequency and amplitude of 1 V. Assume 0 V dc offset for the above signals.



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