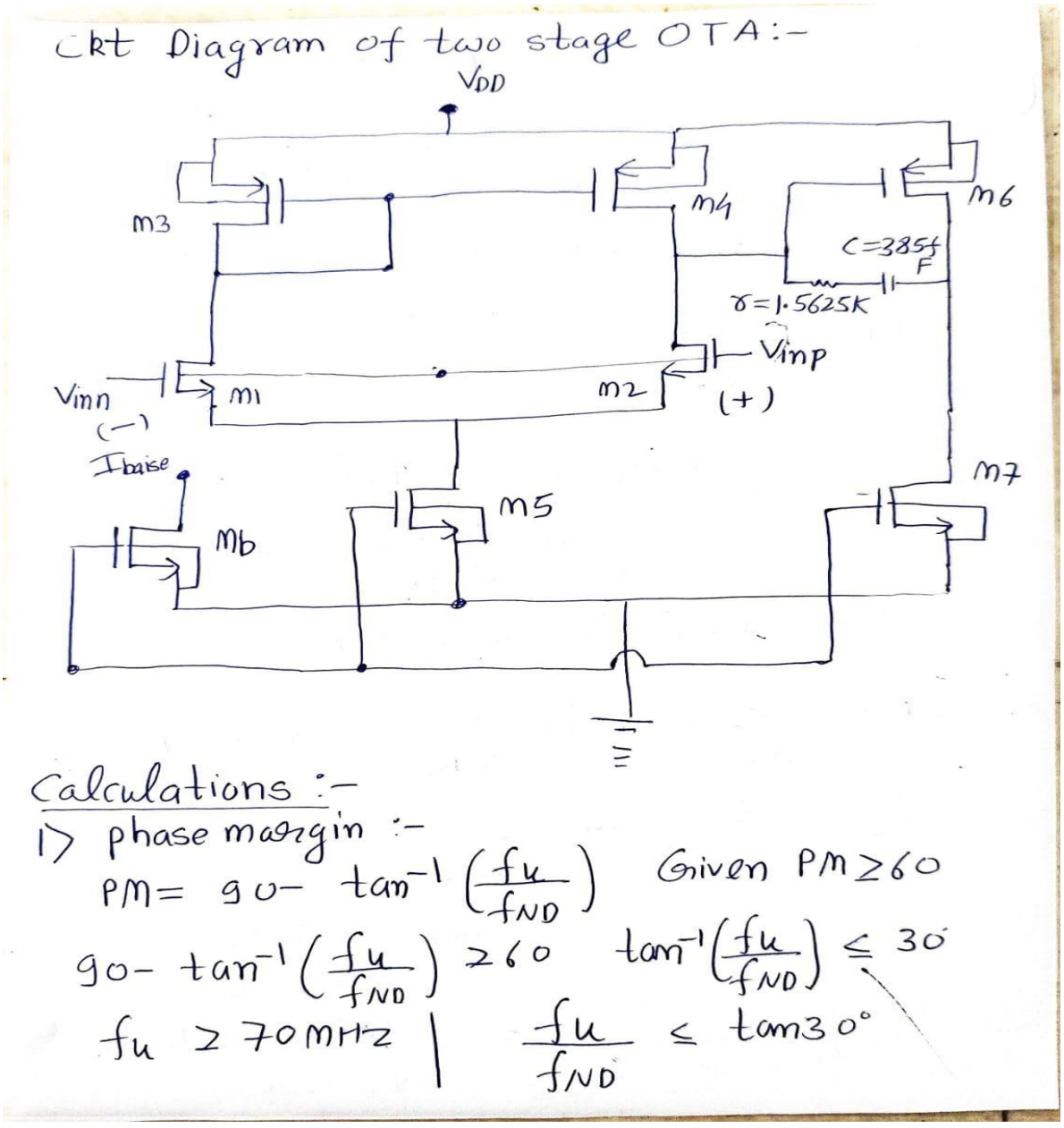
EE 518 Analog IC Design Lab
Design a 2 stage OTA

Submitted by
Pooja Kumari
Roll No:234102318

k

1. Hand Calculations



Calculations :-

1> phase margin :-

$PM = 90 - \tan^{-1}\left(\frac{f_u}{f_{ND}}\right)$ Given $PM \geq 60$

$90 - \tan^{-1}\left(\frac{f_u}{f_{ND}}\right) \geq 60$ $\tan^{-1}\left(\frac{f_u}{f_{ND}}\right) \leq 30$

$f_u \geq 70\,MHz$ | $\frac{f_u}{f_{ND}} \leq \tan 30°$

$f_{ND} \geq \sqrt{3} f_u \Rightarrow f_{ND} = 70\sqrt{3}$

$= 121.24 MHz$

$f_{ND} = \frac{g_{m6}}{2\pi C_L} \Rightarrow g_{m6} = 2\pi C_L f_{ND}$

$g_{m6} = 2\pi \times 121.24\mu s = 762\mu S$

(2) $g_{m6} = \frac{2I_{oss}}{V_{dsat6}} = \frac{2I_{oss}}{0.3} \Rightarrow I_{oss} = \frac{0.3}{2} g_{m6}$

$I_{oss} = \frac{0.3}{2} \times 762\mu s = 114.3\mu A$

(3) $I_{oss} = I_{ss}\left(1 + \frac{C_L}{C_C}\right) = I_{ss} + (SR)C_L$

$= I_{ss} + 60 \Rightarrow I_{ss} = 543\mu A$

(4) $SR = \frac{I_{ss}}{C_L} \Rightarrow C_C = \frac{I_{ss}}{SR} = 0.905 pF$

(5) $R_z = \frac{1}{g_{m6}}\left(1 + \frac{C_L}{C_C}\right) = 2.76 k\Omega$

(6) $2\pi f_u = g_{m1}/C_C \Rightarrow g_{m1} = 2\pi f_u C_C$

$= 398\mu S$

(7) $\left(W/L\right)_1 = \frac{g_{m1}^2}{I_{ss} \cdot k_n m_t} = \frac{398^2}{543 \times 286} = 10.2$

(8) $g_{m7} = \frac{2I_{oss}}{V_{dsat7}} = 762\,\mu S$

(9) $\left(\frac{W}{L}\right)_7 = \frac{g_{m7}}{2I_{oss}\,k_n\,l_{vt}} = \frac{762^2}{2\times 1143\times 303}$

$= 19.49 \approx 20$

(10) $\frac{54.3}{\left(\frac{W}{L}\right)_5} = \frac{1143}{20} \Rightarrow \left(\frac{W}{L}\right)_5 = 95$

(11) $\frac{54.3}{\left(\frac{W}{L}\right)_5} = \frac{10}{\left(\frac{W}{L}\right)_B} \Rightarrow \left(\frac{W}{L}\right)_B = 1.75$

(12) $\left(\frac{W}{L}\right)_6 = \frac{g_{m6}^2}{2k_p I_{oss}} = \frac{762^2}{2\times 32\times 1143} = 79.4 \approx 80$

(13) $\left(\frac{W}{L}\right)_{3,4} = \frac{I_{ss}}{2I_{oss}} \times \left(\frac{W}{L}\right)_6 = 18.86 \approx 20$

(14) $48dB \Rightarrow 260 = \frac{g_{m1}\,g_{m6}}{\frac{I_{ss}}{2}\cdot I_{oss}\cdot(\lambda_n+\lambda_p)^2}$

let $\lambda_n = \lambda_p = \lambda$

$\lambda^2 = \frac{298\times 762}{54.3\times 1143\times 2\times 260} = 0.307$

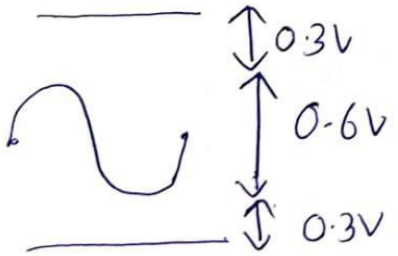
So, $l_{vt} \rightarrow 0.585\times 45 = 0.307\times L_n$

$\Rightarrow L_n = 90\,nm$

$0.41 \times 45 = 0.307 \times L_p \quad L_p = 60nm$

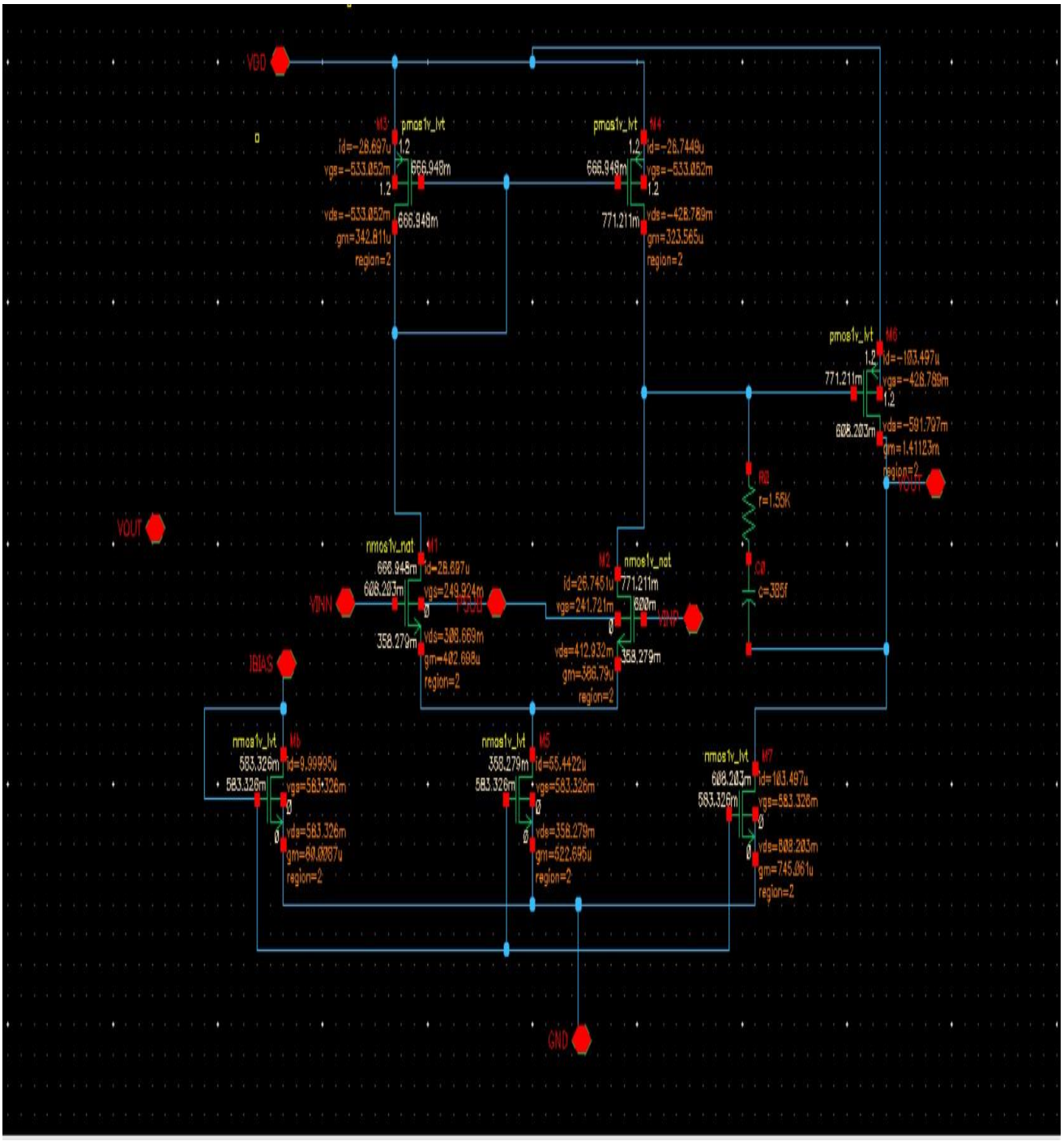
$nat \rightarrow \quad 0.694 \times 300 = 0.307 \times L_{nat}$

$\Rightarrow L_{nat} = 680nm$

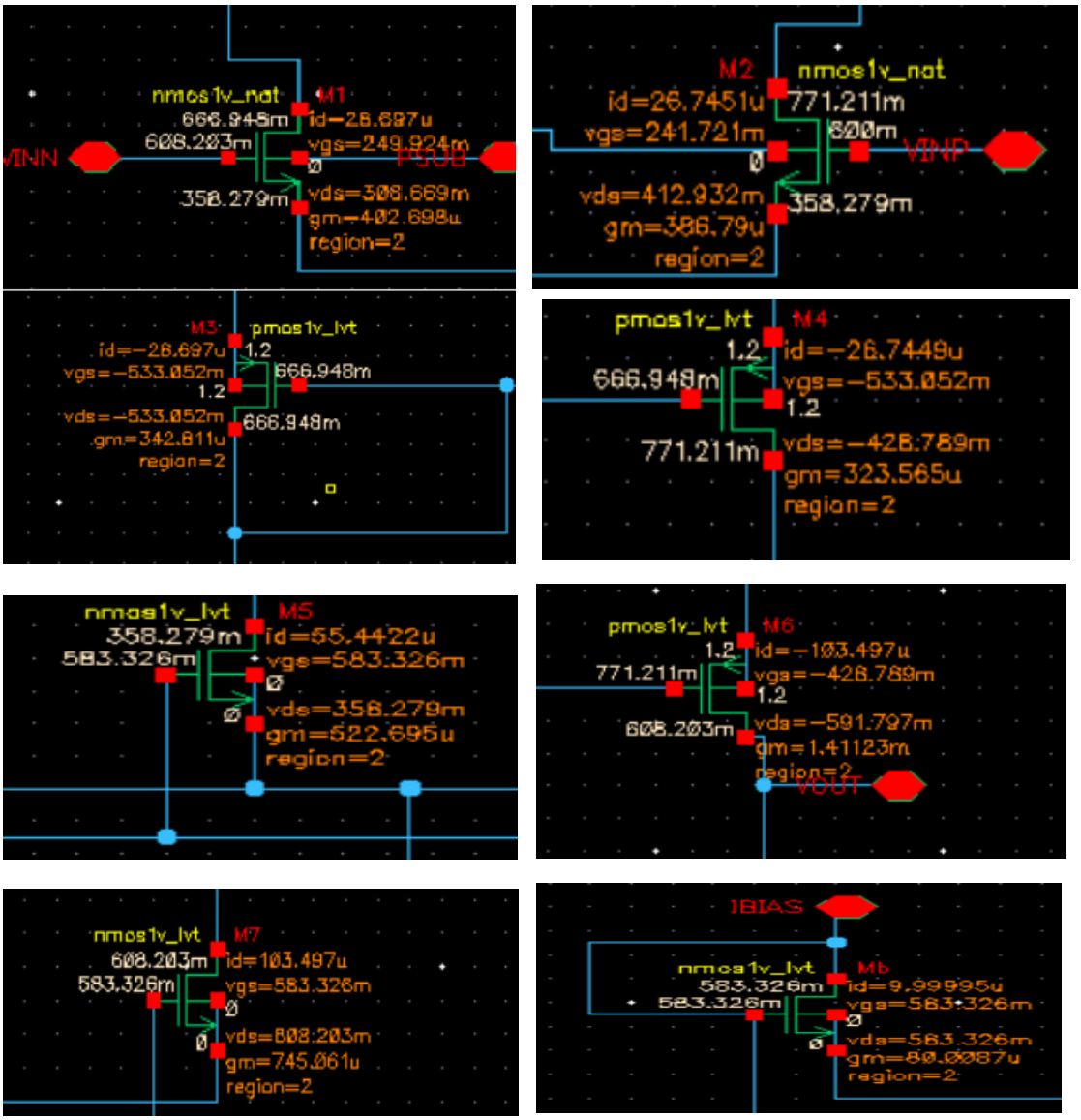


2. DC Operating Point

Screenshot of schematics with operating point annotation of each transistor:

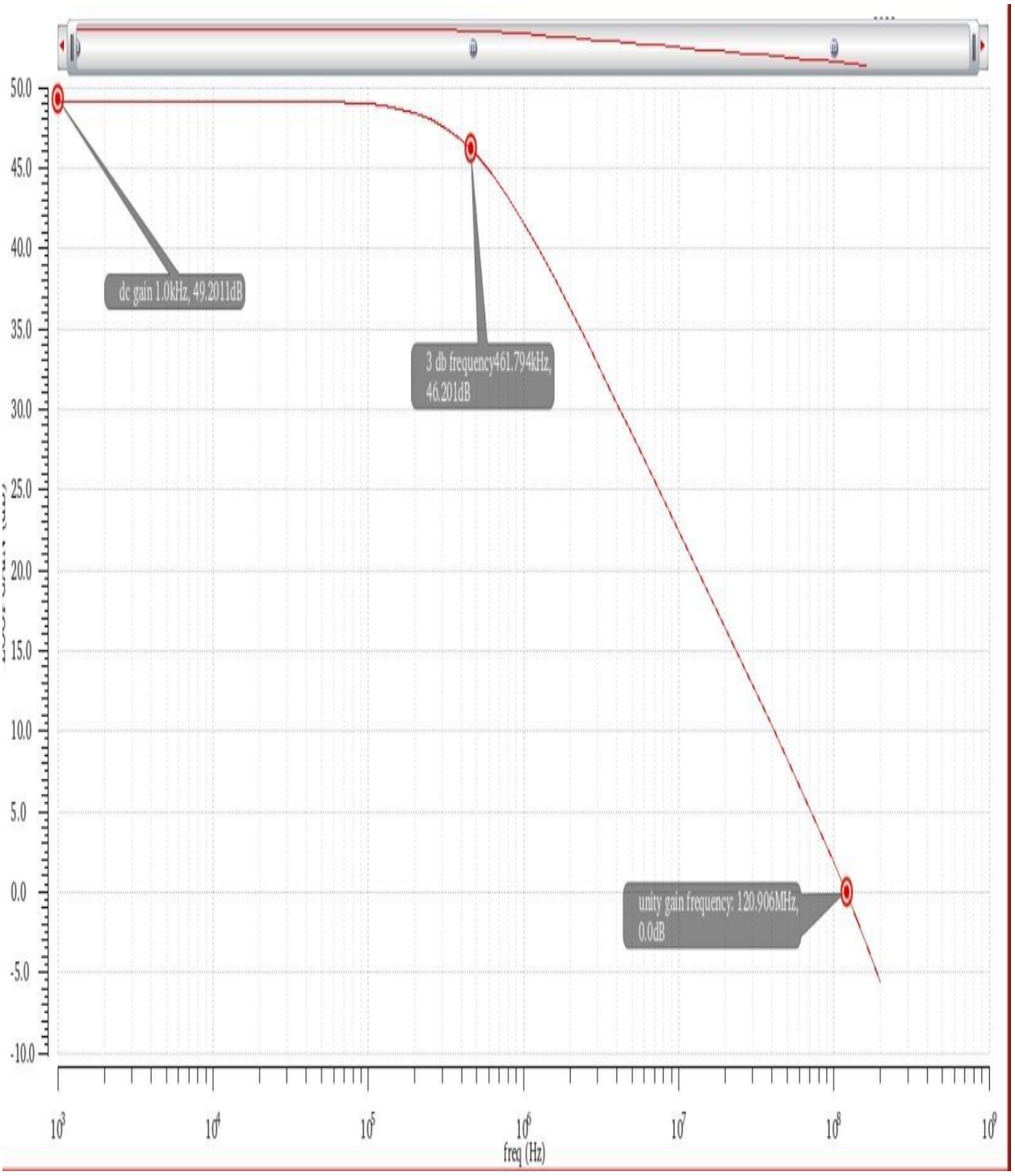


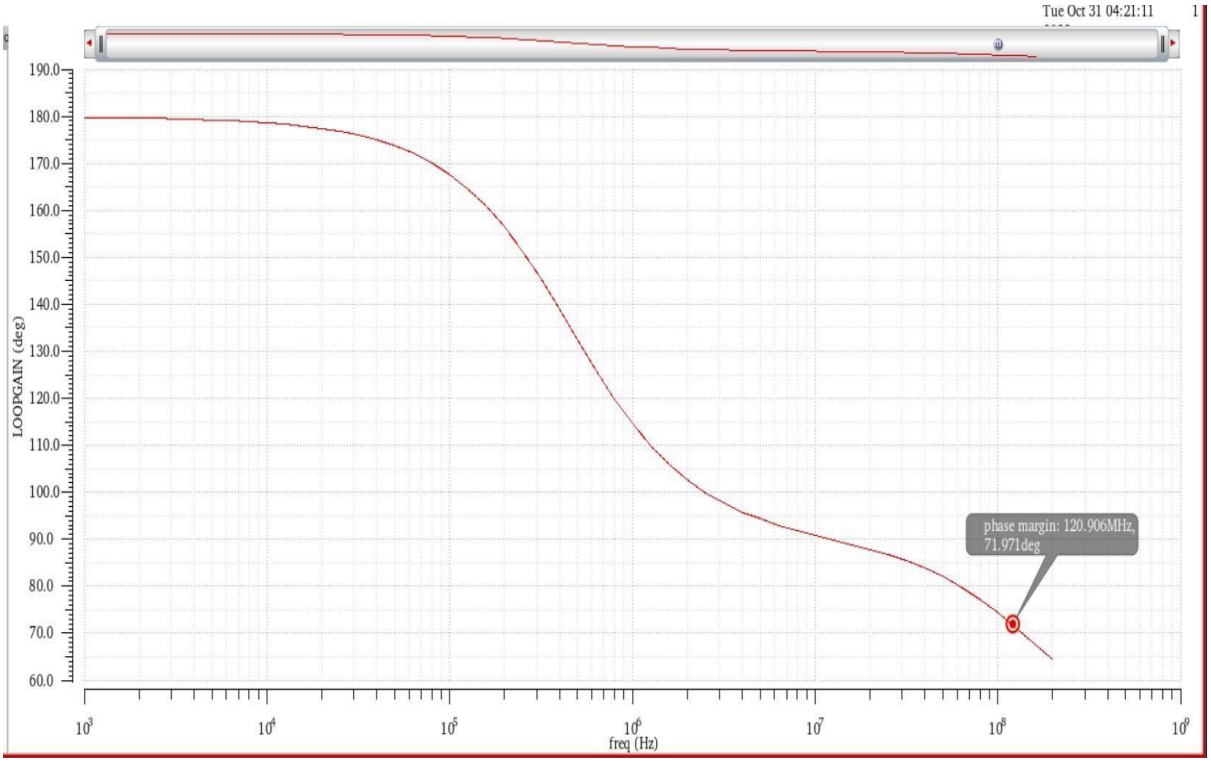
a screenshot of the schematic showing region of operation of all the transistors:



3.Stability Analysis:

1.screenshot clearly showing the DC Gain, f-3dB (-3dB frequency) and unity-gain frequency and phase margin.


50.0
45.0
40.0
35.0
30.0
25.0
20.0
15.0
10.0
5.0
0.0
-5.0
-10.0
dc gain 1.0kHz, 49.2011dB
3 db frequency461.794kHz, 46.201dB
unity gain frequency: 120.906MHz, 0.0dB
10^3
10^4
10^5
10^6
10^7
10^8
10^9
freq (Hz)



2.screenshot of Stability Summary.

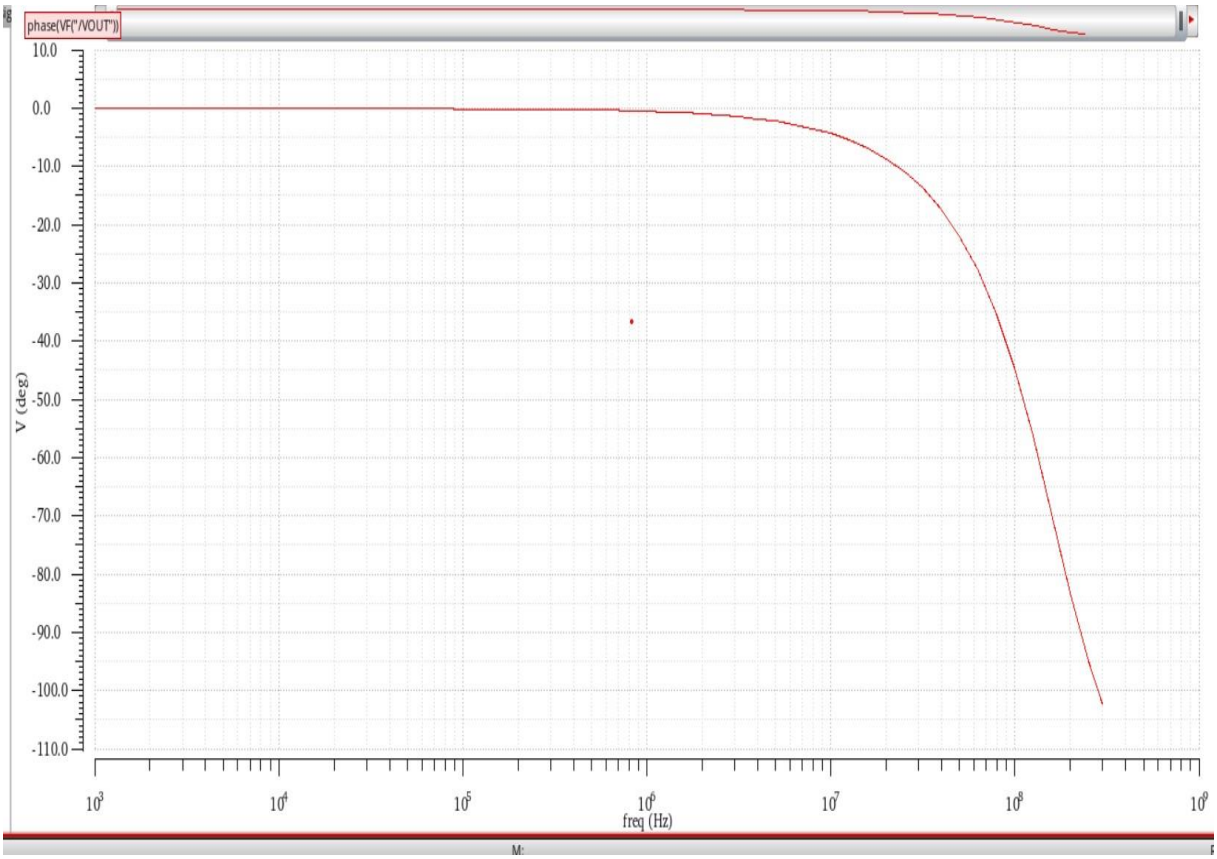
Stability Summary - circuit "TB_STB_LG" with loop probe "IPRB0"

Design_Point	PM(deg)	@Freq(Hz)	GM(dB)	@Freq(Hz)
1	71.978	120.56M	nan	nan

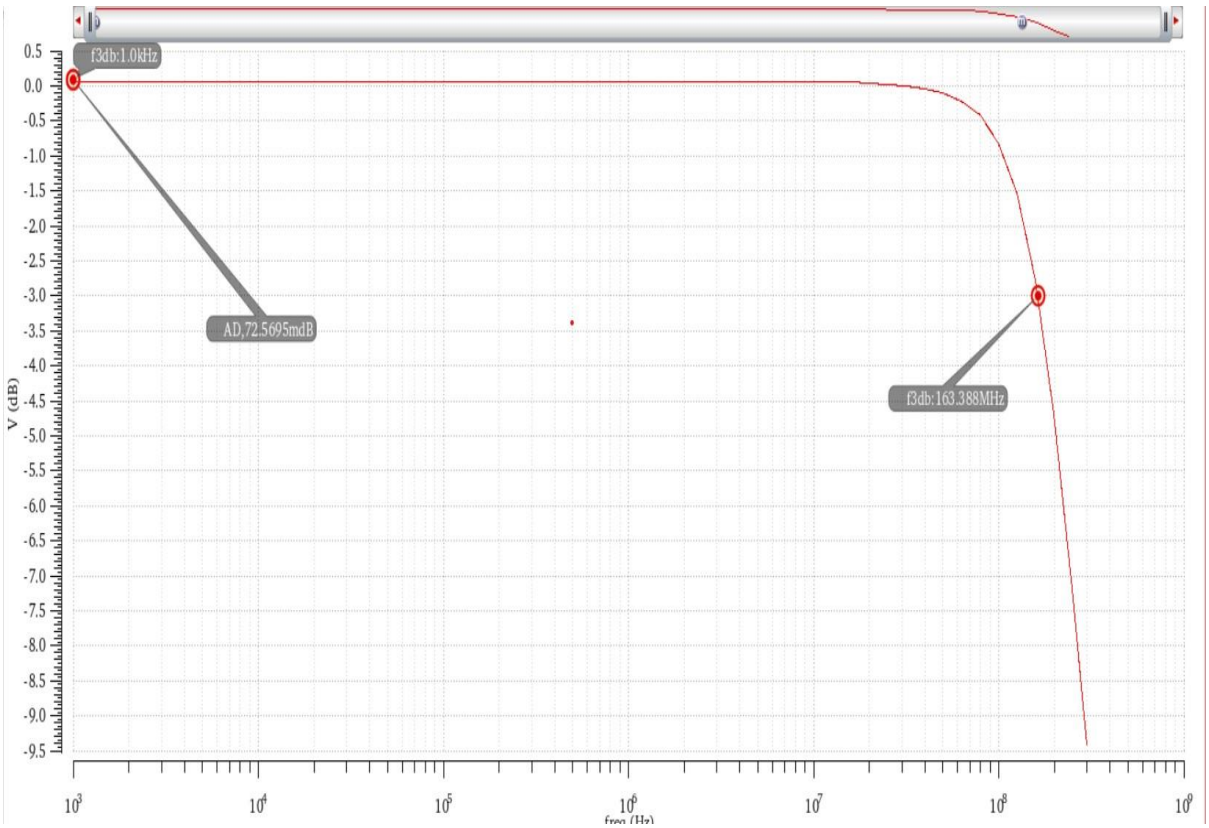
4.AC Analysis: Differential Gain

Plot the Closed Loop gain and phase plot:

PHASE PLOT:



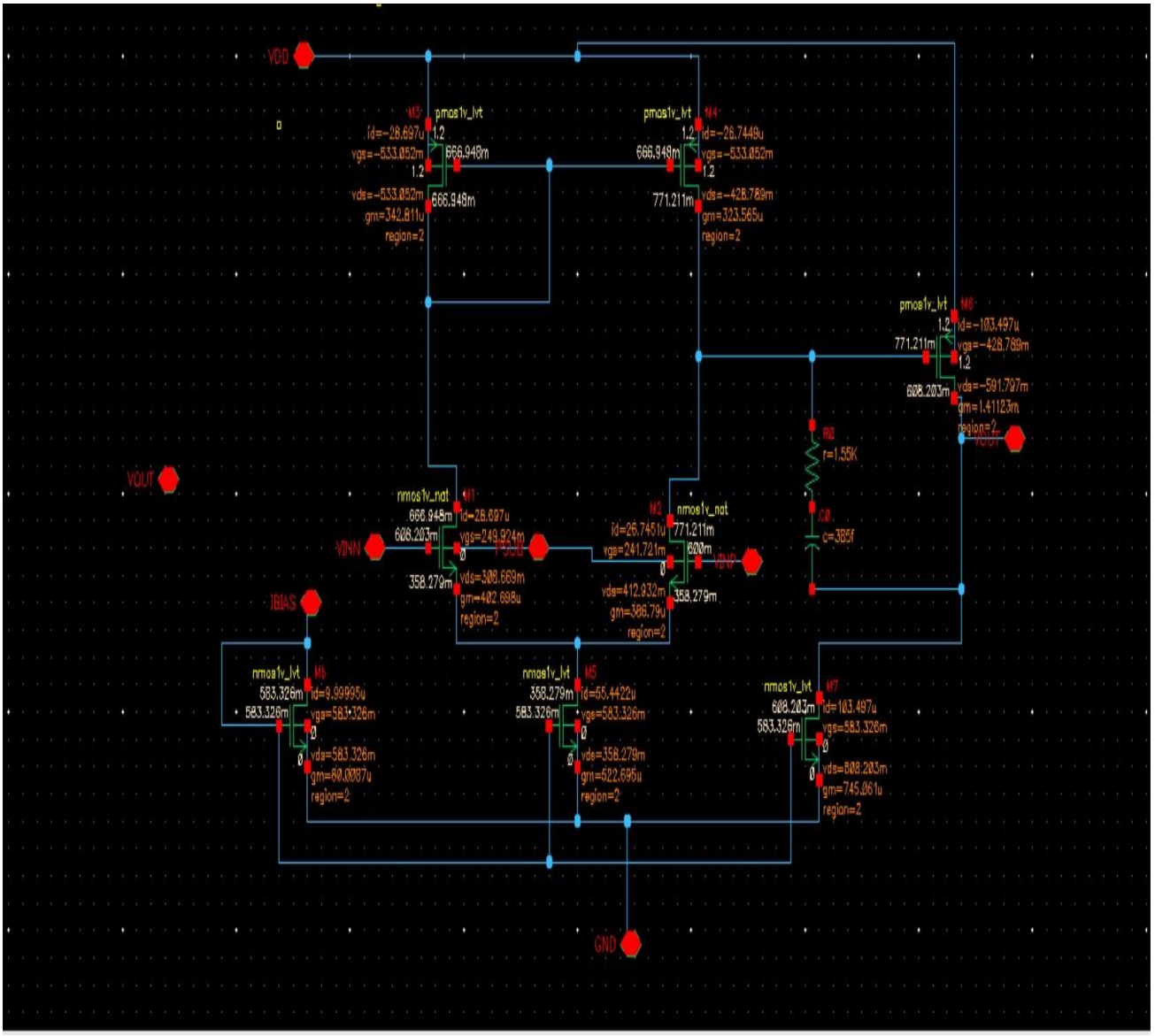
GAIN PLOT:

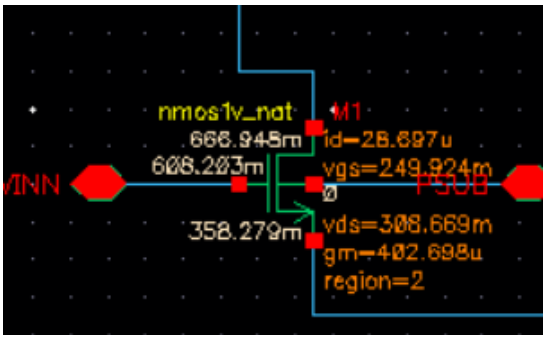


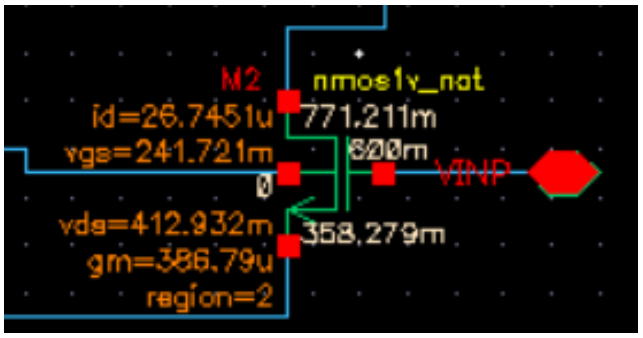
show the input referred systematic offset:

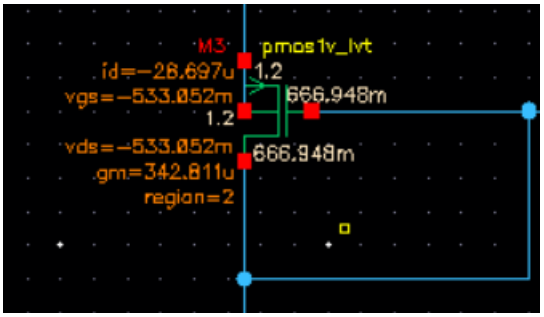
EE618_CP1_23M1195:TB_AC_DM:1	dB20(VF("/VOUT"))				
EE618_CP1_23M1195:TB_AC_DM:1	phase(VF("/VOUT"))				
EE618_CP1_23M1195:TB_AC_DM:1	Input reffered offset	-8.203m			

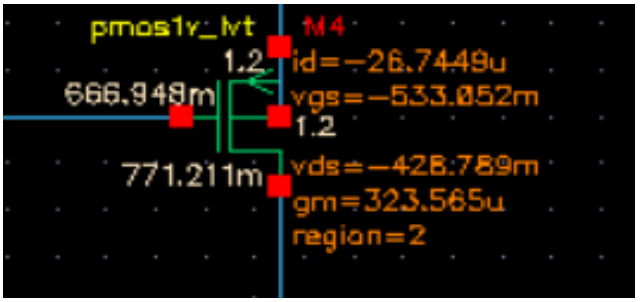
Take a screenshot of the schematic with DC operating points annotated for each transistor:

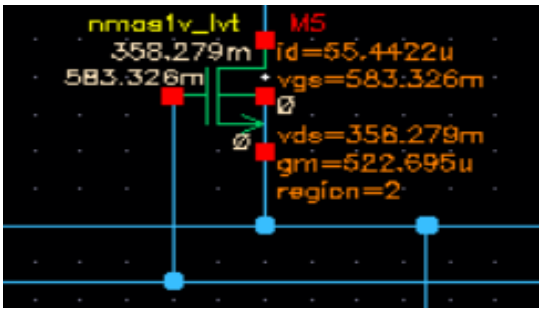


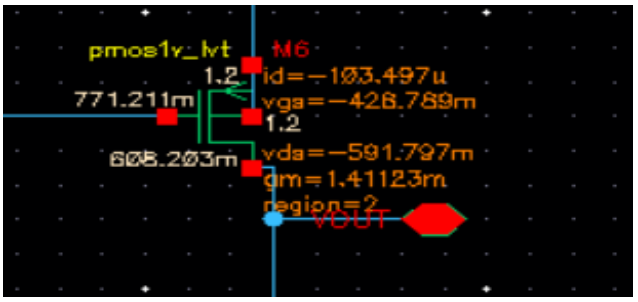


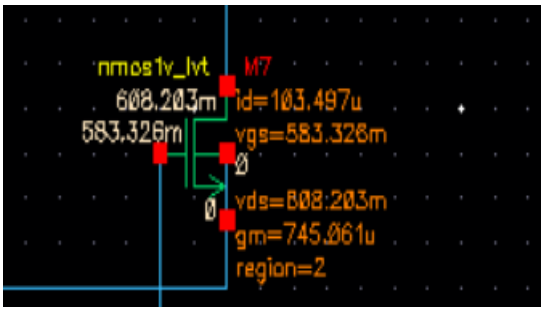


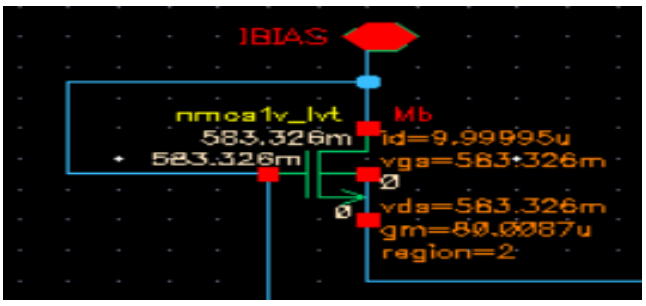








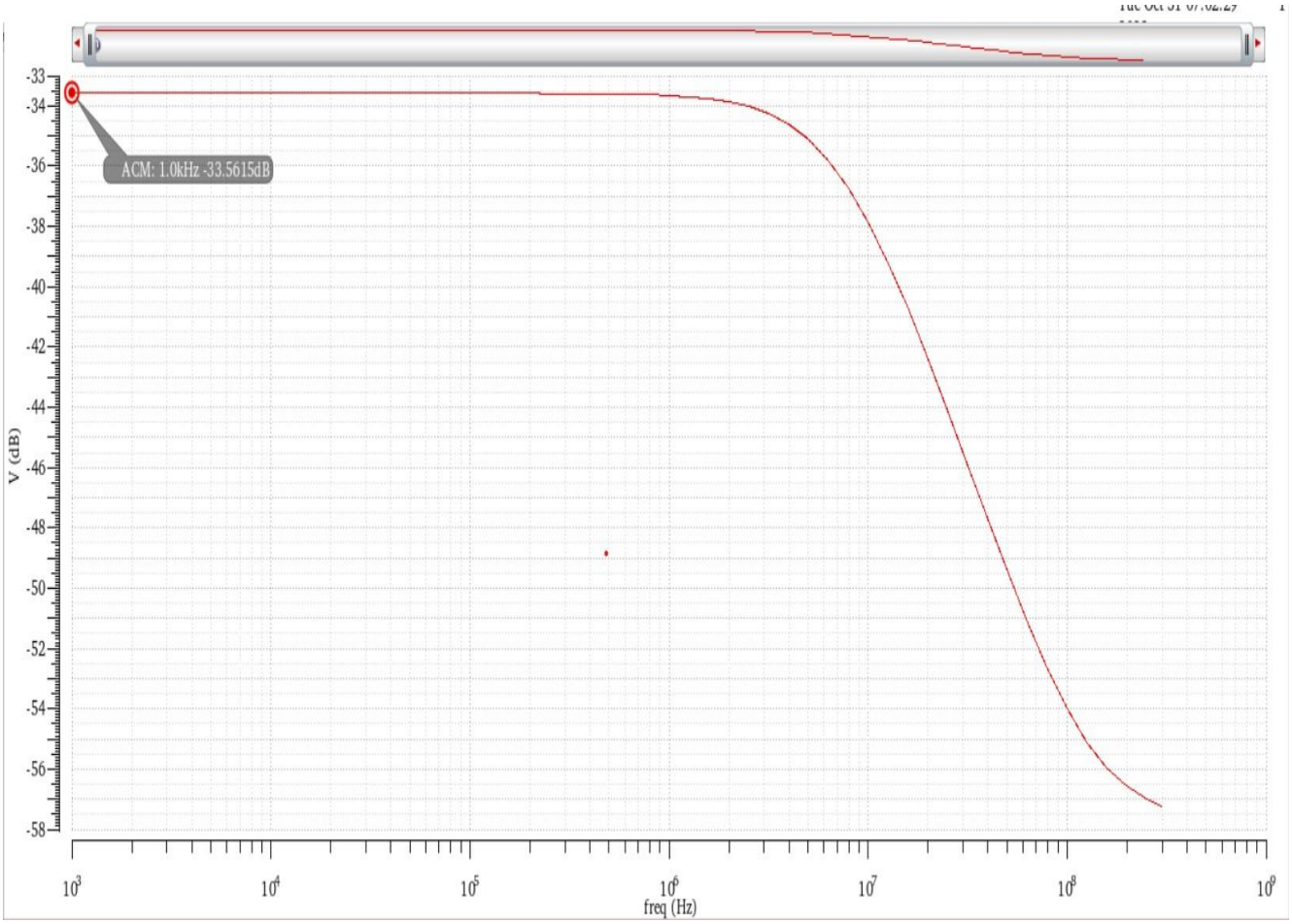




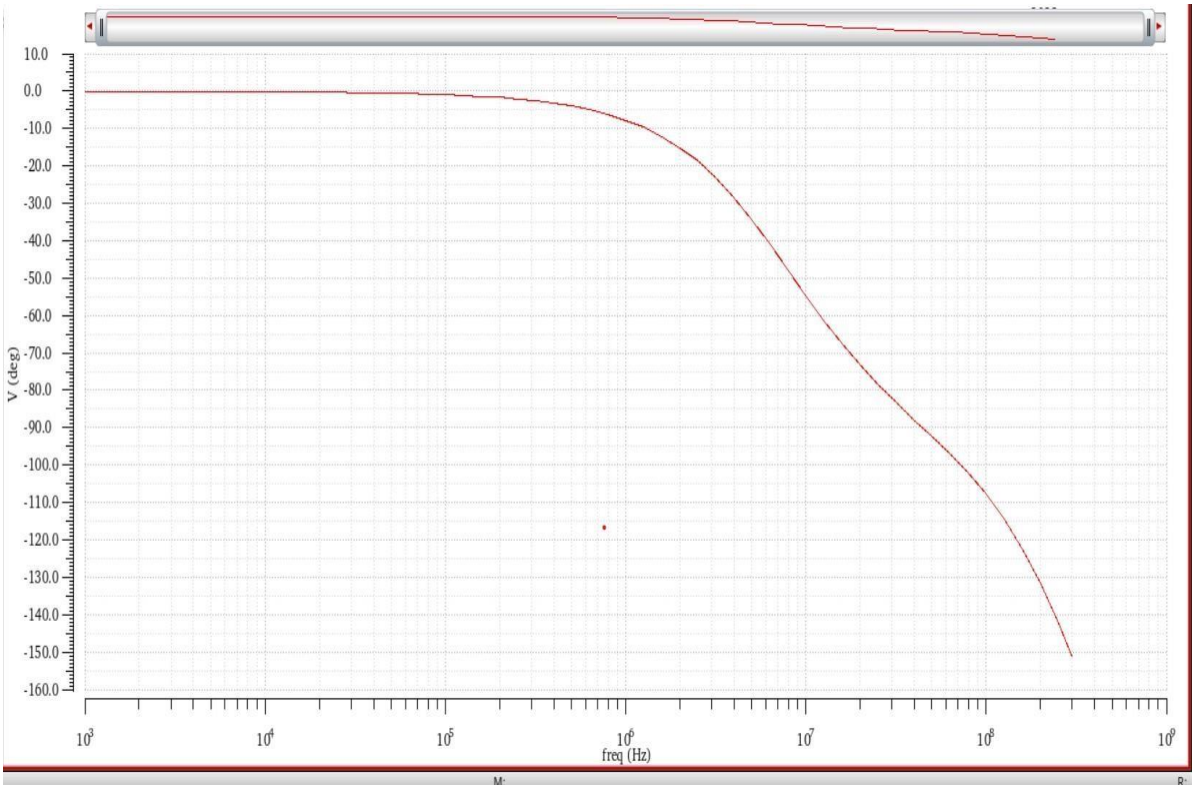
5. AC Analysis: Common Mode Gain

Plot the open loop CM gain of the OTA with clear labels:

COMMON MODE GAIN:



COMMON GAIN PHASE PLOT:



Report the CMRR of the OTA by using the differential gain simulated earlier:

CMRR CALCULATION:

DIFFERENTIAL MODE GAIN=42.569 dB

COMMON MODE GAIN=-33.562 dB

CMRR=76.13 dB

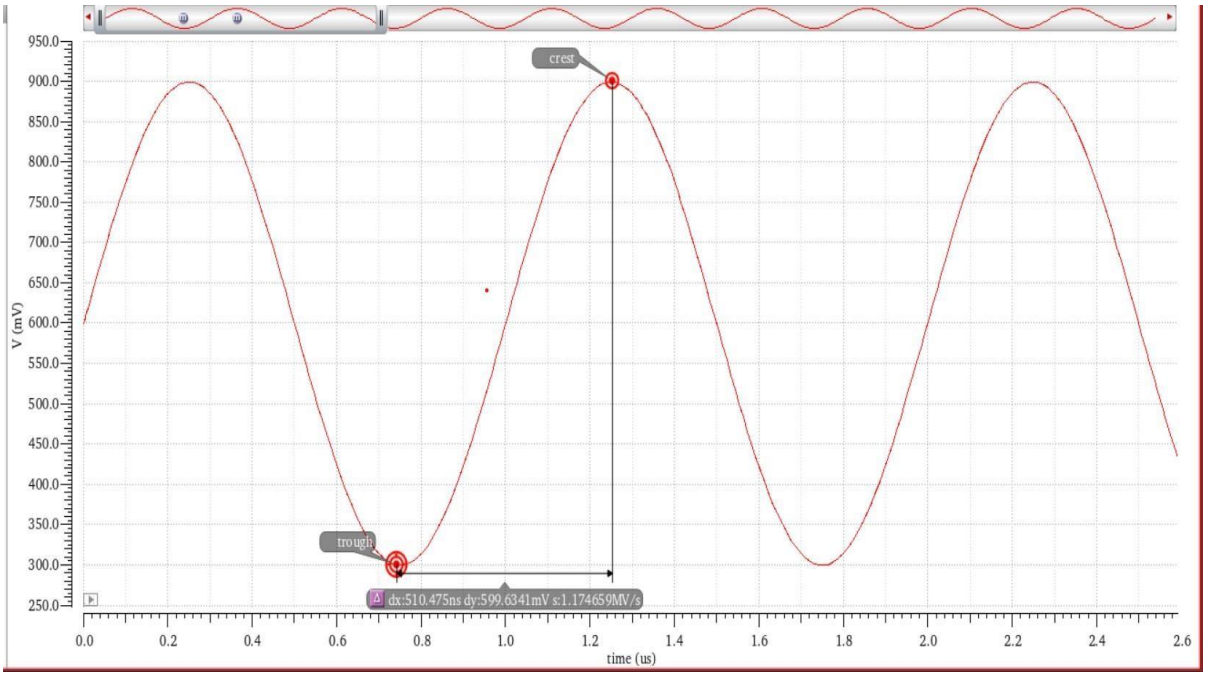
EE618_CP1_23M1195:TB_AC_CM:1	dB20(VF("/VOUT"))				
EE618_CP1_23M1195:TB_AC_CM:1	phase(VF("/VOUT"))				
EE618_CP1_23M1195:TB_AC_CM:1	ACM (in dB)	-33.56			

6. Transient Analysis: Sinusoidal Input

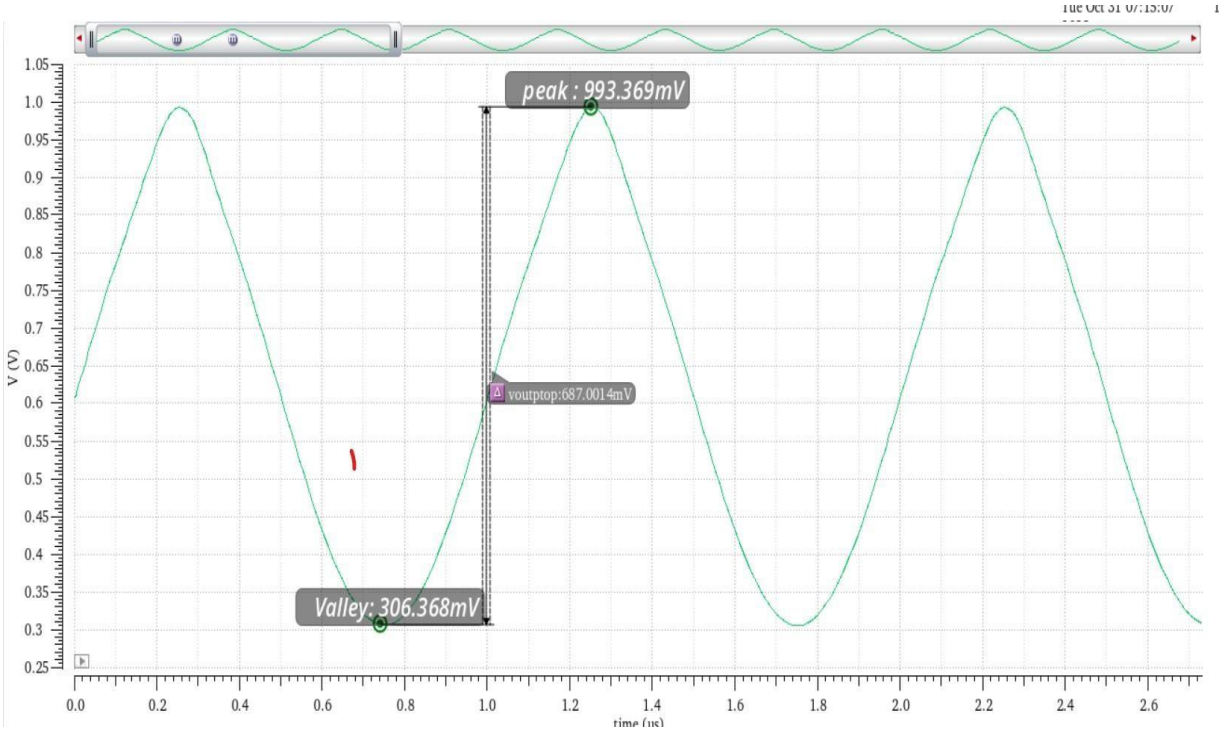
Plot the input and output transient waveform clearly annotating the peak voltages and take a screenshot of the same.

Test	Output	Nominal	Spec	Weight	Pass/Fail
EE618_CP1_23M1195:TB_TRAN_SIN:1	/VOUT				
EE618_CP1_23M1195:TB_TRAN_SIN:1	/VINP				
EE618_CP1_23M1195:TB_TRAN_SIN:1	VOUT (peak-peak)	687.5m			
EE618_CP1_23M1195:TB_TRAN_SIN:1	VIN (peak-peak)	600m			

INPUT TRANSIENT WAVEFORM:



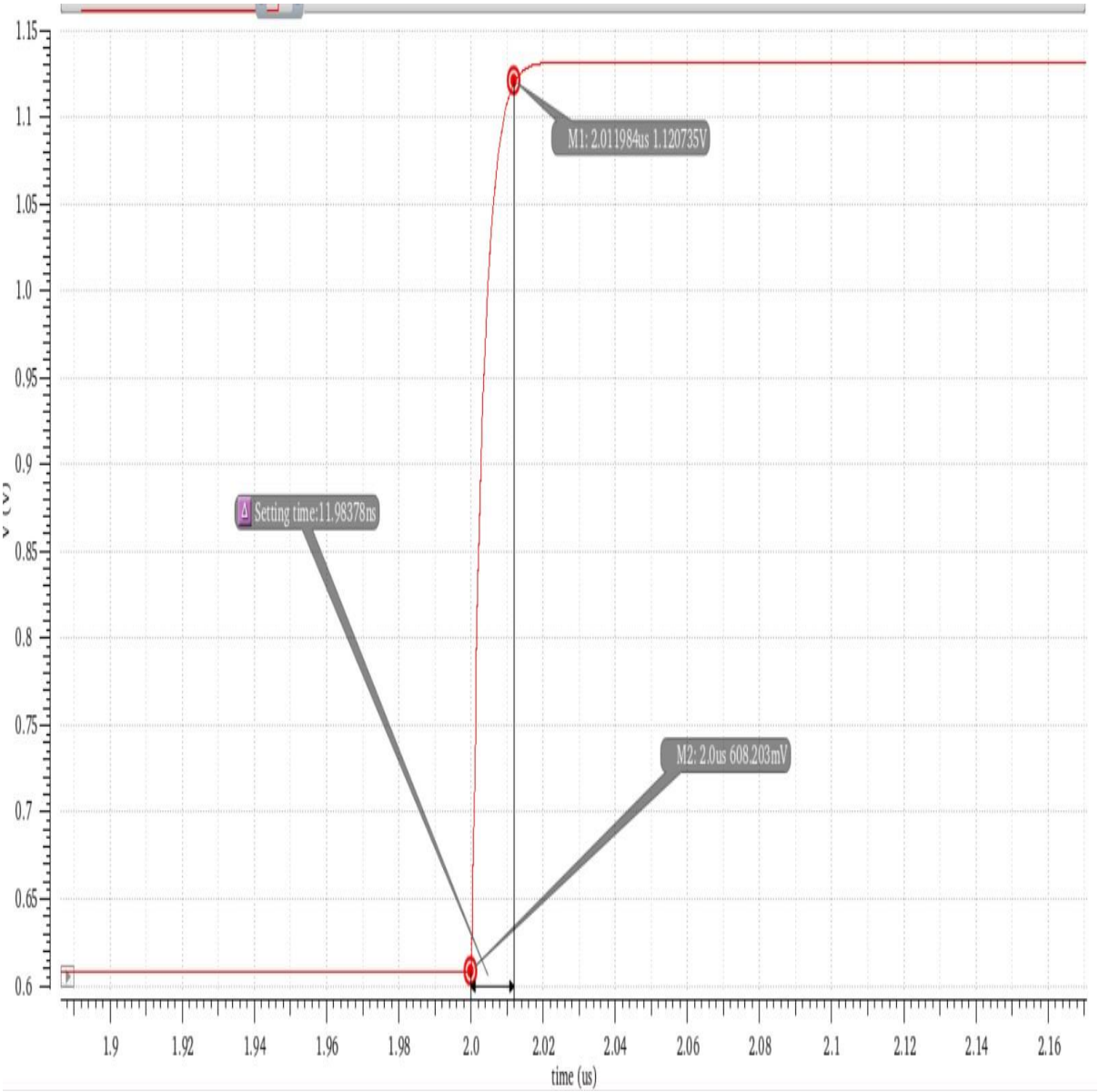
OUTPUT TRANSIENT WAVEFORM:



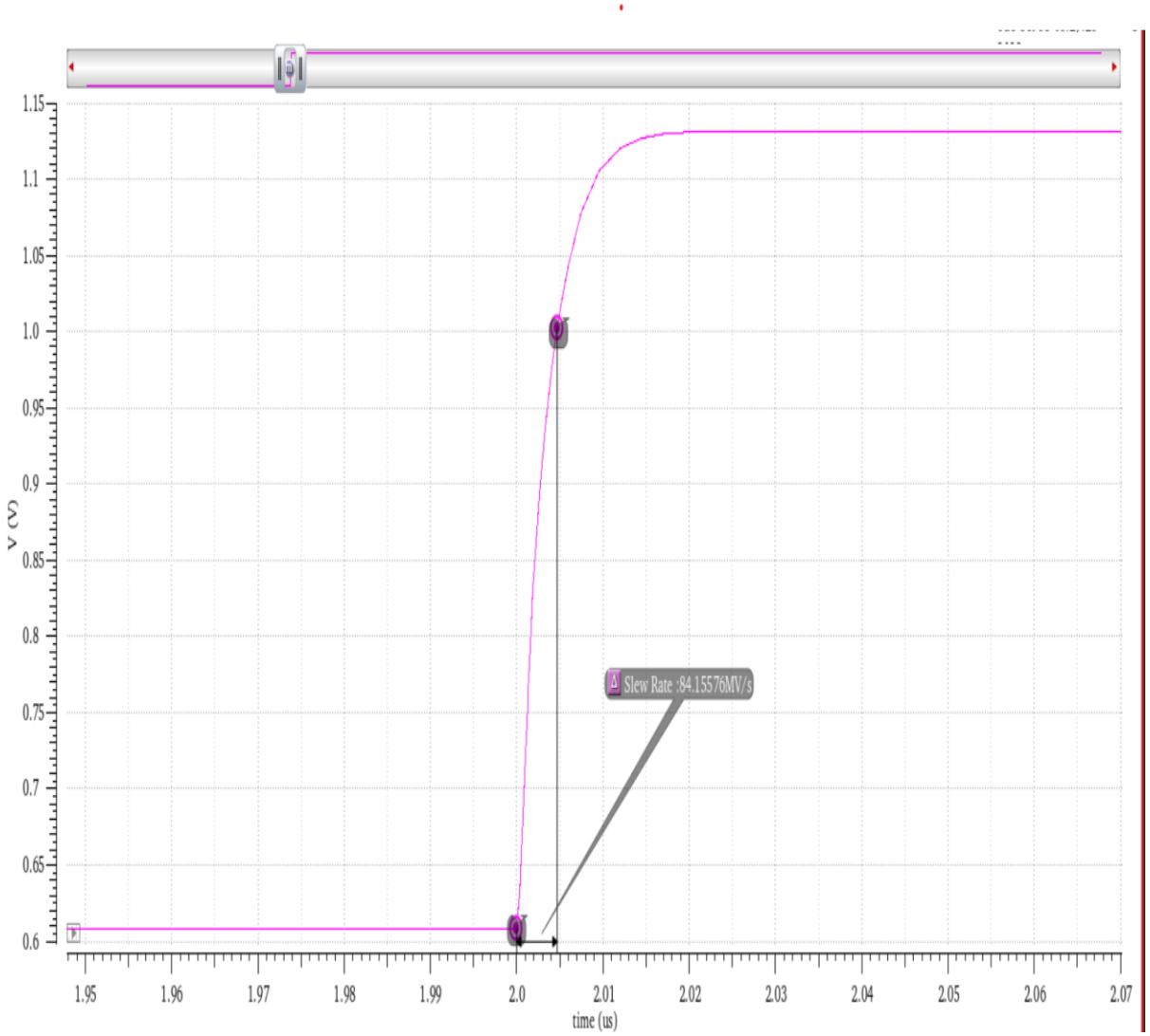
7.Transient Analysis: Step Input

Measure the slew rate and clearly show the output plot in the slewing region with cursors. ○ Measure and report the settling time, ts for 1% accuracy.

PLOT OF SETTLING TIME (1% ACCURACY):



SLEW RATE PLOT:



8. Noise Analysis

Show the input referred noise PSD from 10kHz to 300MHz band. Clearly show the input referred noise in the plot (with marker) at 1MHz and 10 MHz.

Report the integrated noise and noise contributions.

NOISE SUMMARY:

Device	Param	Noise Contribution	% Of Total
/I0/M4	fn	4.55553e-08	26.19
/I0/M2	fn	4.33853e-08	23.76
/I0/M1	fn	4.27377e-08	23.05

Spot Noise Summary (in V/sqrt(Hz)) at 100K Hz Sorted By Noise Contributors
Total Summarized Noise = 8.90143e-08
Total Input Referred Noise = 8.82737e-08
The above noise summary info is for noise data

Device	Param	Noise Contribution	% Of Total
/I0/M4	id	5.54822e-09	15.68
/I0/M2	fn	5.45849e-09	15.18
/I0/M2	id	5.37772e-09	14.73

Spot Noise Summary (in V/sqrt(Hz)) at 10M Hz Sorted By Noise Contributors
Total Summarized Noise = 1.40117e-08
Total Input Referred Noise = 1.39037e-08
The above noise summary info is for noise data

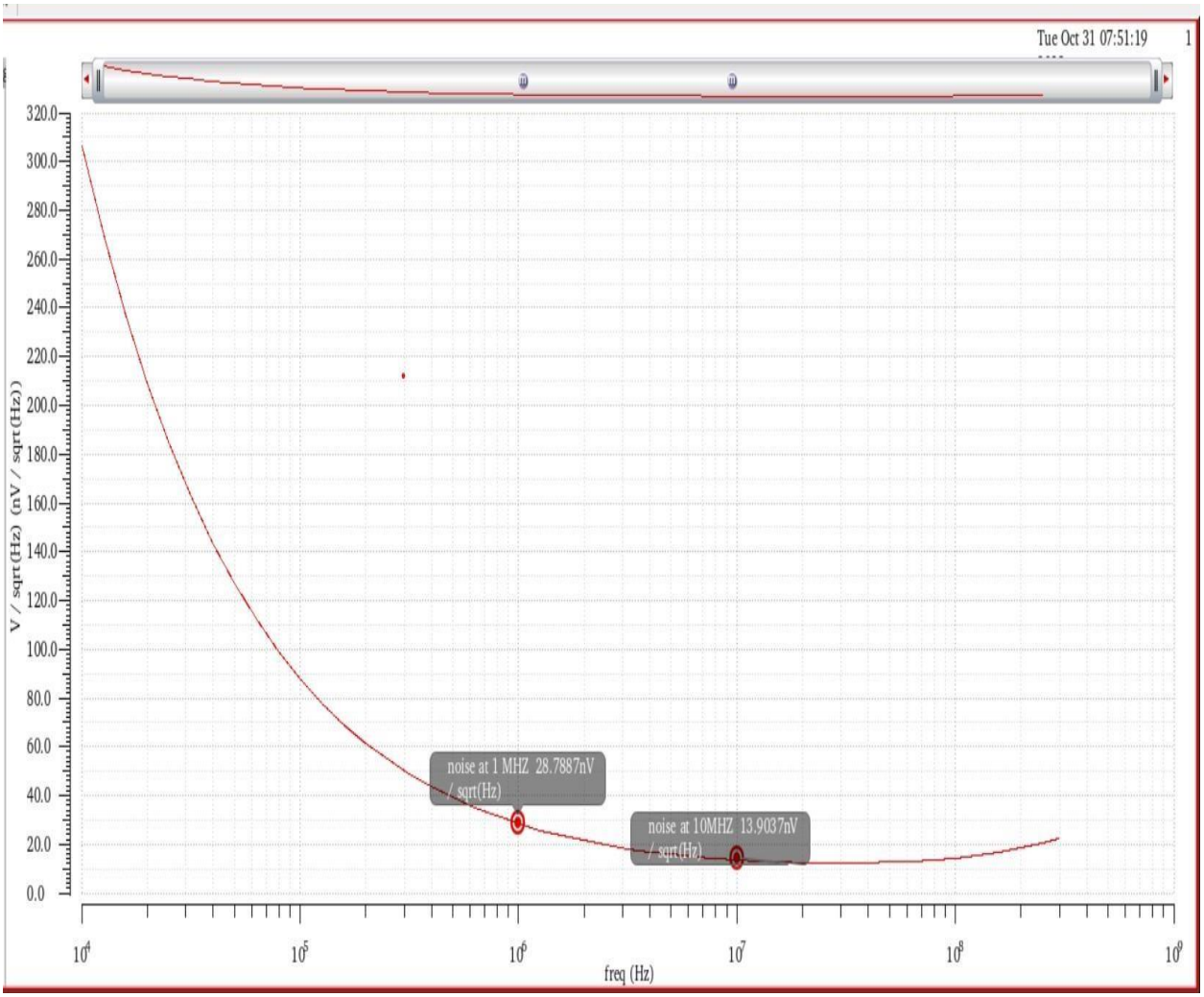
Device	Param	Noise Contribution	% Of Total
/I0/Mb	fn	9.96346e-05	21.23
/I0/M4	id	7.33754e-05	11.52
/I0/M2	id	7.06065e-05	10.66

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Summarized Noise = 0.000216229
Total Input Referred Noise = 0.000309028
The above noise summary info is for noise data

Device	Param	Noise Contribution	% Of Total
/I0/Mb	fn	9.96346e-05	21.23
/I0/M4	id	7.33754e-05	11.52
/I0/M2	id	7.06065e-05	10.66

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Summarized Noise = 0.000216229
Total Input Referred Noise = 0.000309028
The above noise summary info is for noise data

INPUT REFERRED NOISE PLOT:

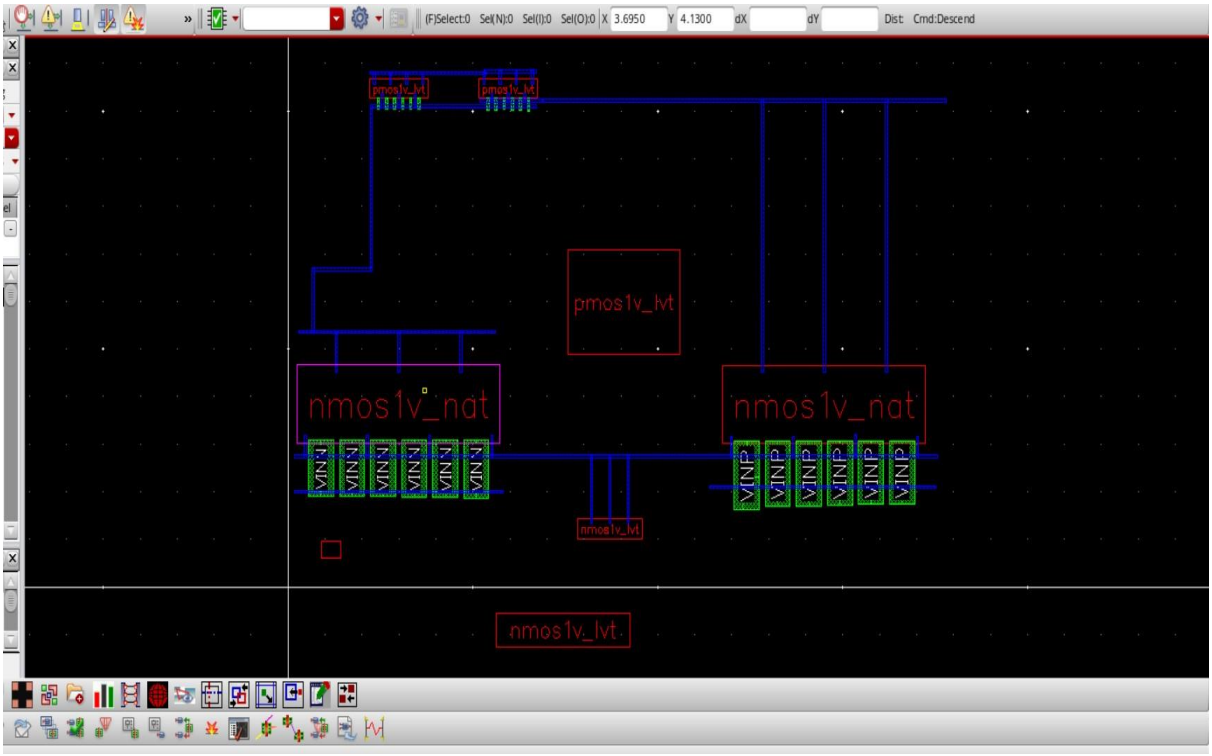


9.Summary of Results Obtained

Q.No	Parametres	Value(unit)
2.	Power Consumption	202.73uW
3.	DC Gain	49.201dB
	f-3 dB	461.794KHz
	Unity Gain Frequency	120.906MHz
	Phase Margin	71.978 deg
4.	Closed Loop Gain	72.569mdB
	f-3dB	163.388MHz
	Input Referred Offset (DC Analysis)	-8.203 mV
5.	Common Mode Gain	-33.562dB

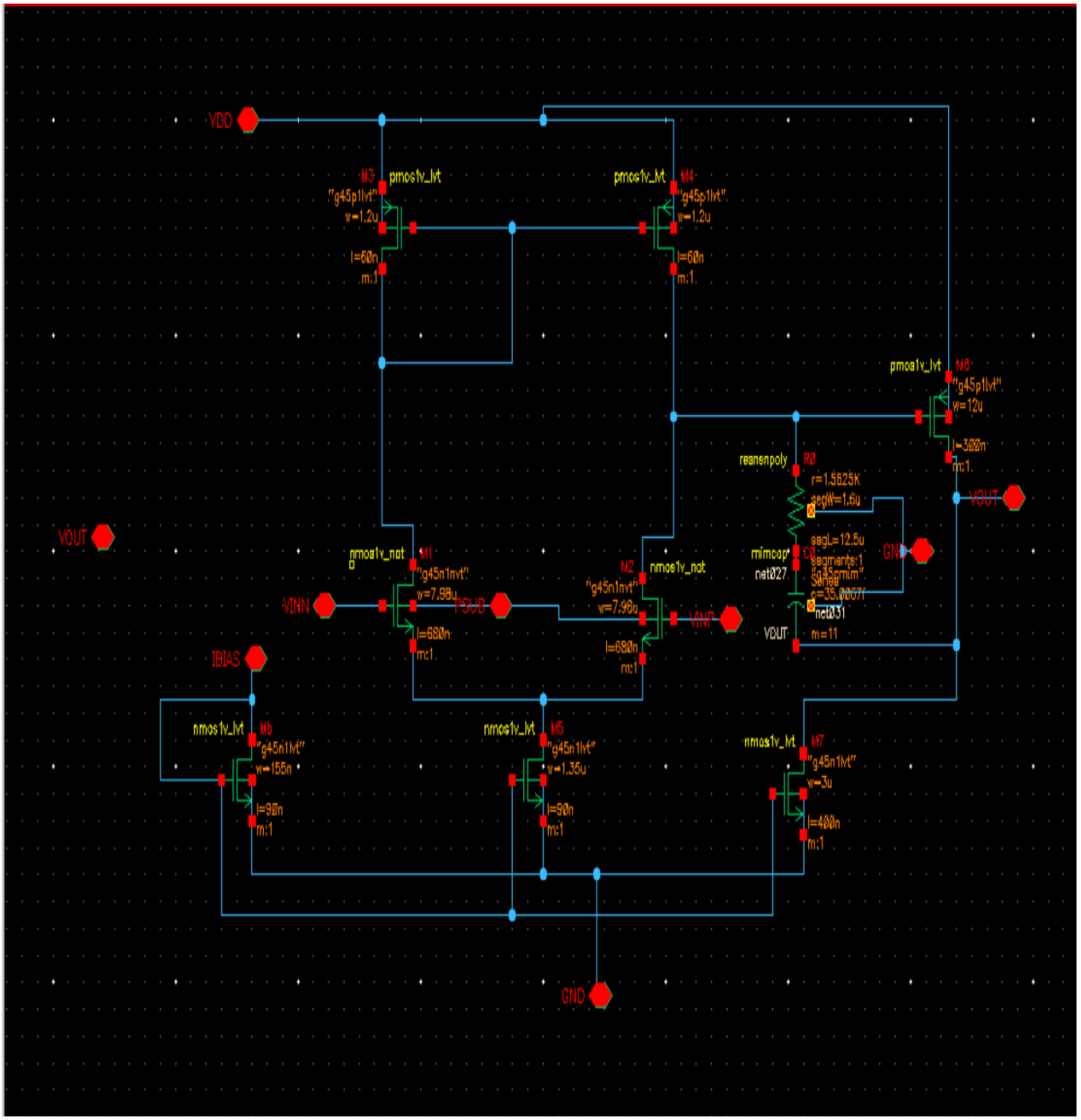
	CMRR	76.13dB
6.	Output Swing (Vpk-pk)	687.7mV
7.	Slew Rate	84.15576V/us
	Settling Time(1% accuracy)	11.98378 us
8.	Input Referred Spot Noise (at 1MHz)	28.788nV/sqrt(Hz)
	Input Referred Spot Noise (at 10 MHz)	13.903nV/sqrt(Hz)
	Total Summarized Noise	0.000216229V
	Total Input Referred Noise	0.000309028V

Layout:

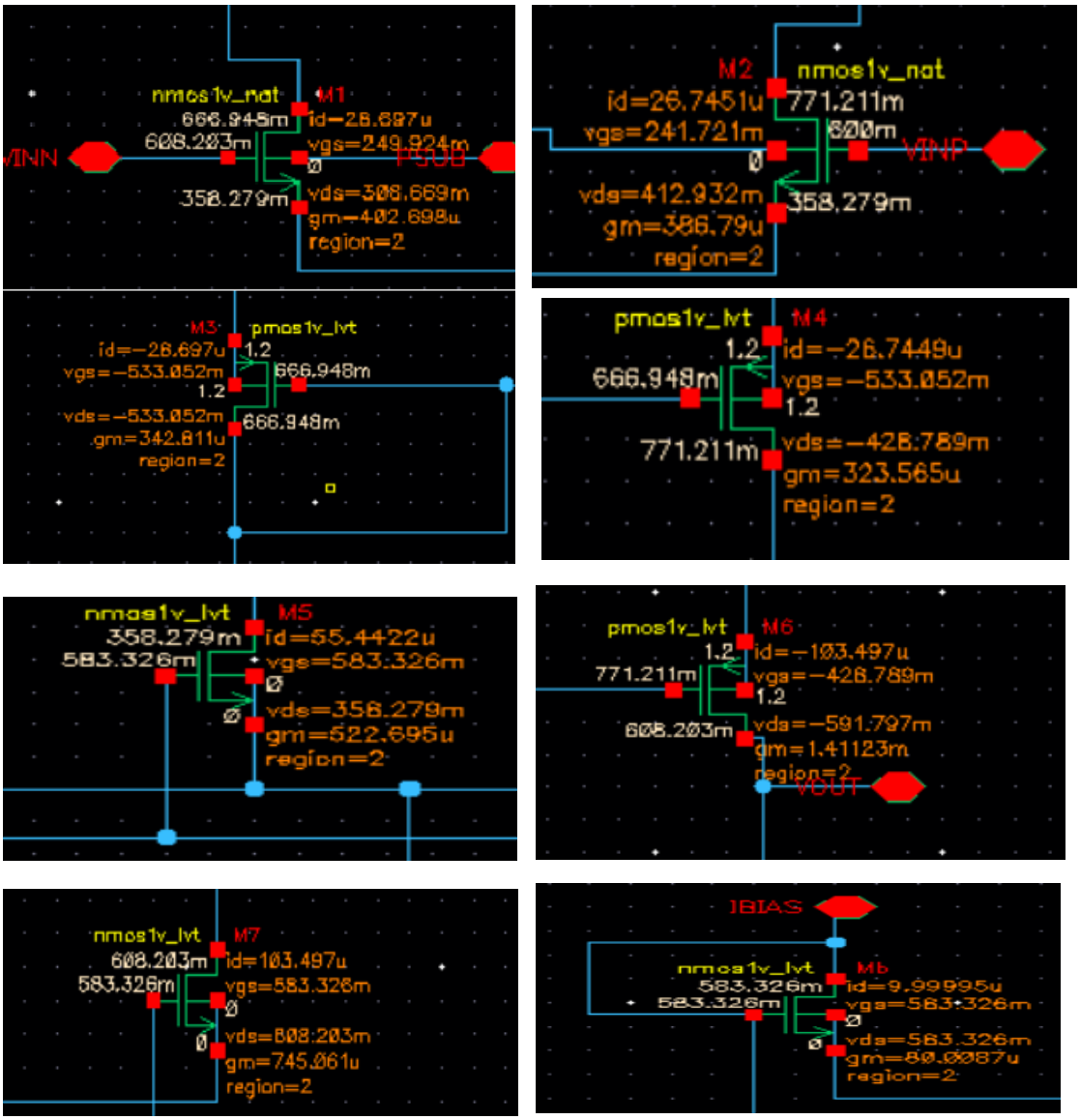


2. DC Operating Point

Screenshot of schematics with operating point annotation of each transistor:

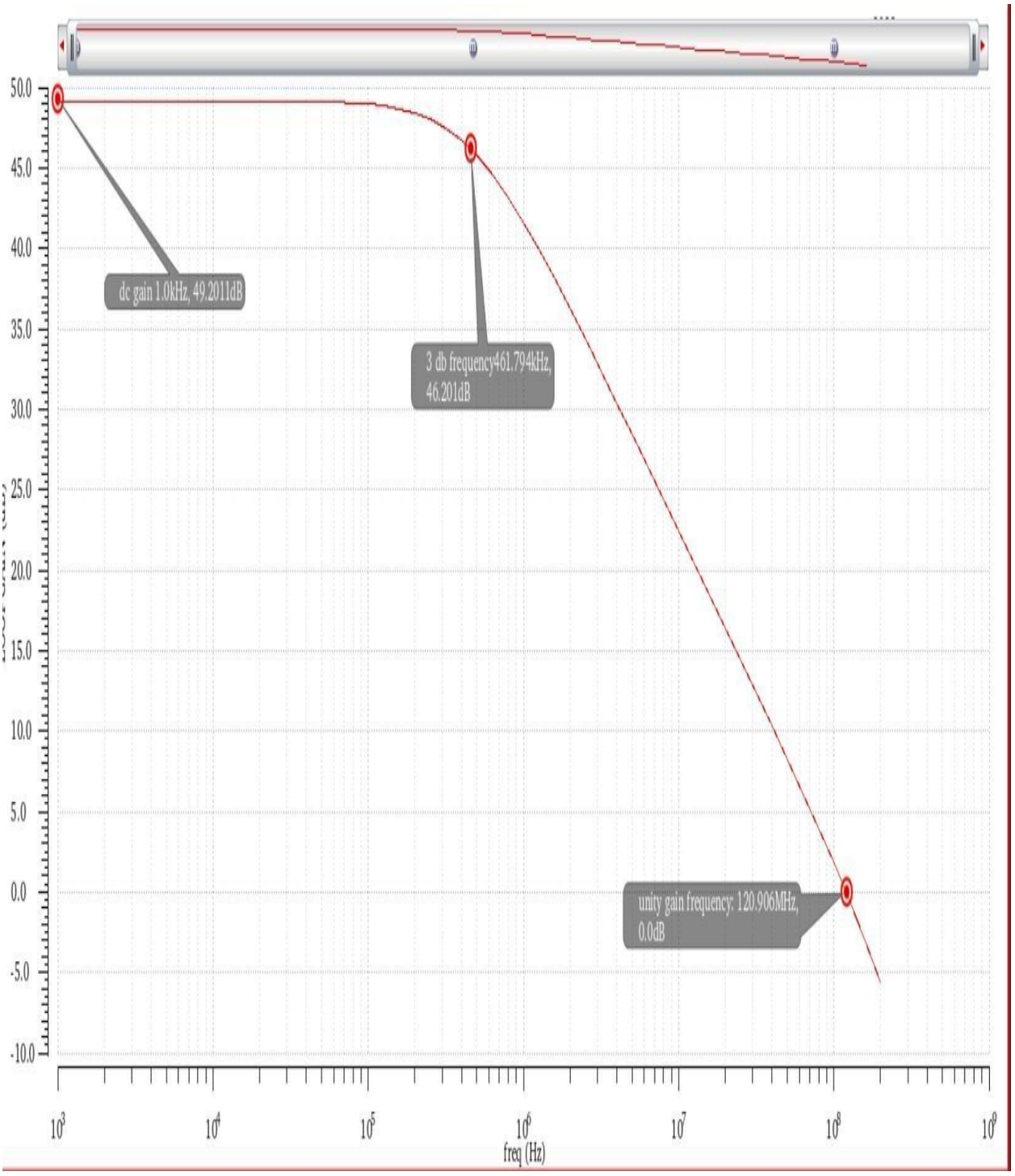


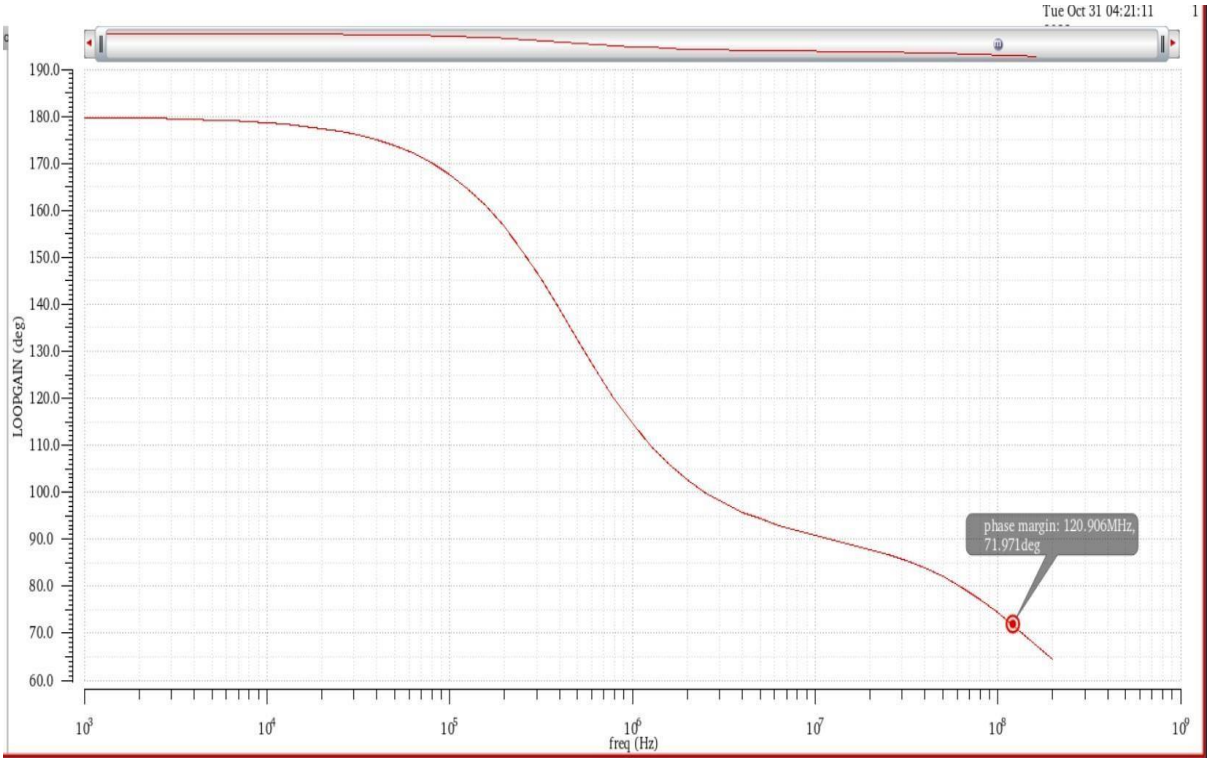
a screenshot of the schematic showing region of operation of all the transistors:



3.Stability Analysis:

1.screenshot clearly showing the DC Gain, f-3dB (-3dB frequency) and unity-gain frequency and phase margin.


50.0
45.0
40.0
35.0
30.0
25.0
20.0
15.0
10.0
5.0
0.0
-5.0
-10.0
dc gain 1.0kHz, 49.2011dB
3 db frequency461.794kHz, 46.201dB
unity gain frequency: 120.906MHz, 0.0dB
10^3
10^4
10^5
10^6
10^7
10^8
10^9
freq (Hz)



2.screenshot of Stability Summary.

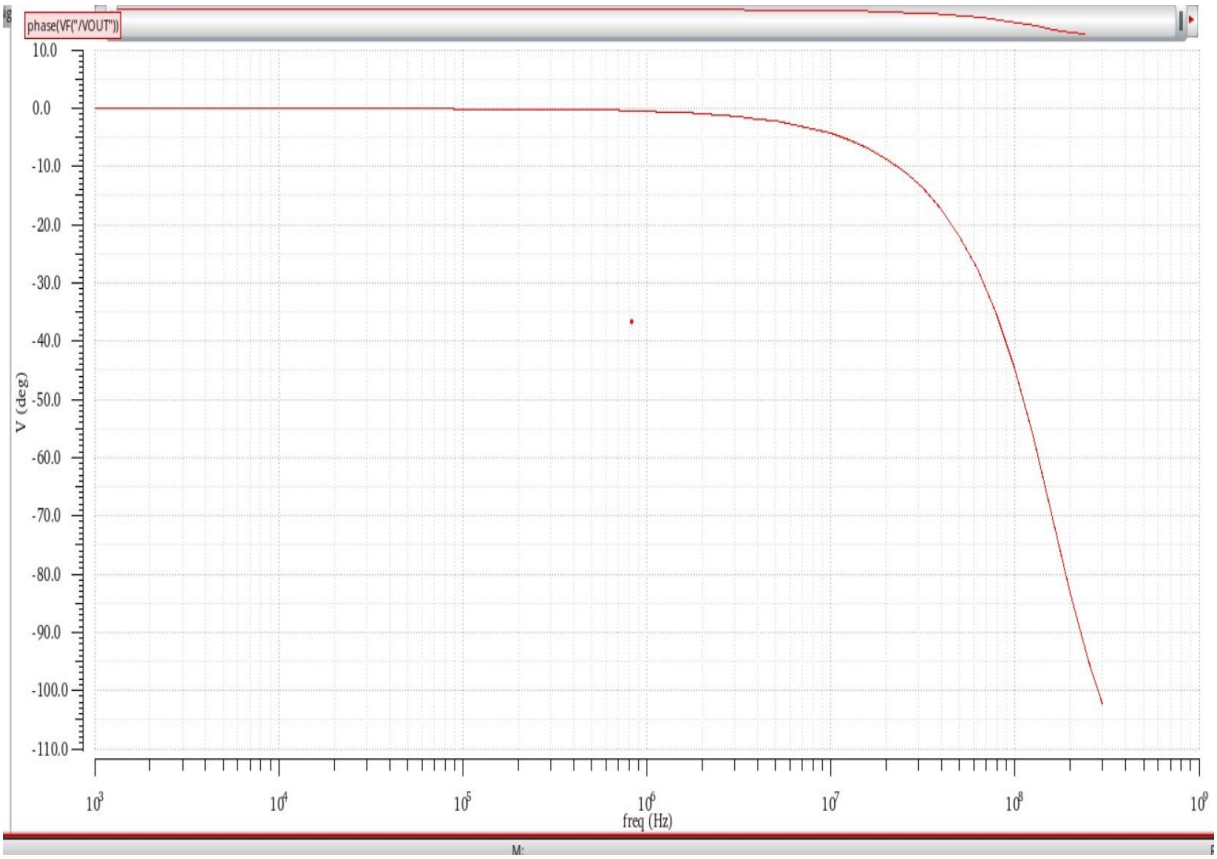
Stability Summary - circuit "TB_STB_LG" with loop probe "IPRB0"

Design_Point	PM(deg)	@Freq(Hz)	GM(dB)	@Freq(Hz)
1	71.978	120.56M	nan	nan

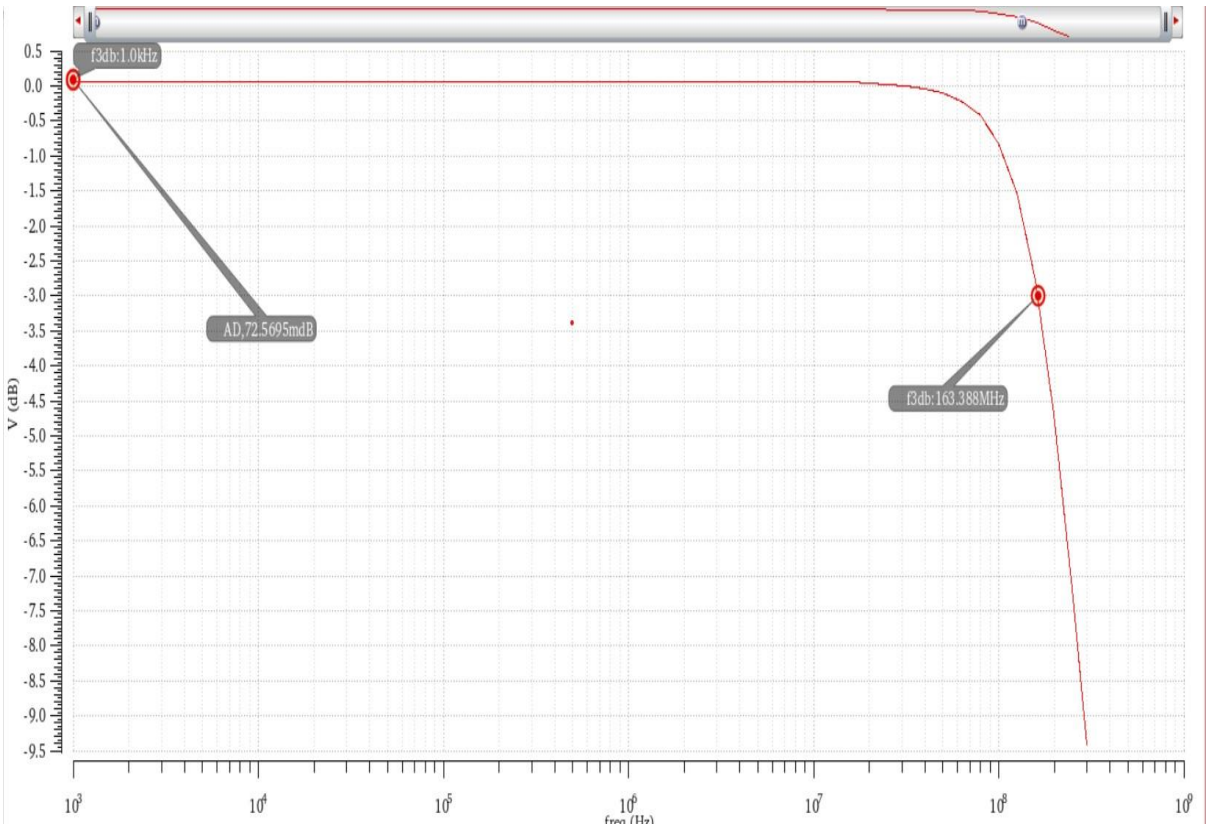
4.AC Analysis: Differential Gain

Plot the Closed Loop gain and phase plot:

PHASE PLOT:



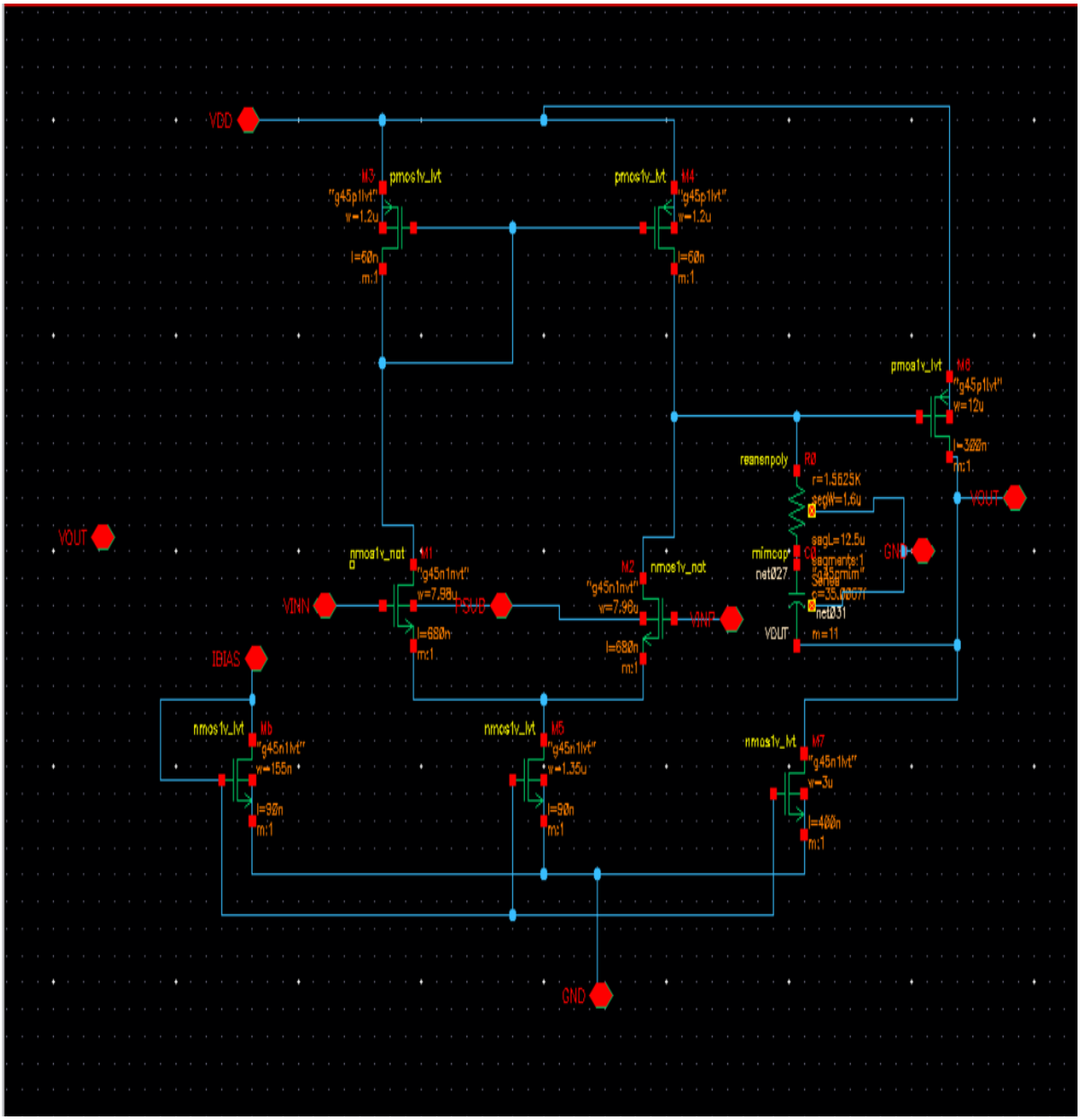
GAIN PLOT:

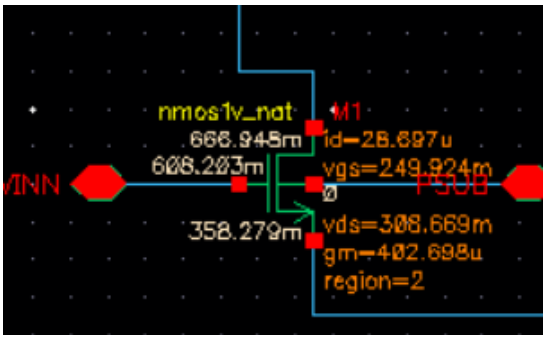


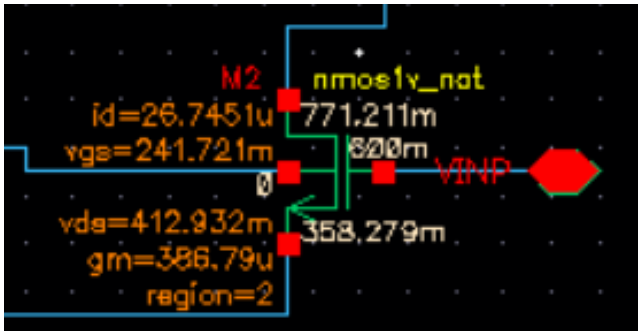
show the input referred systematic offset:

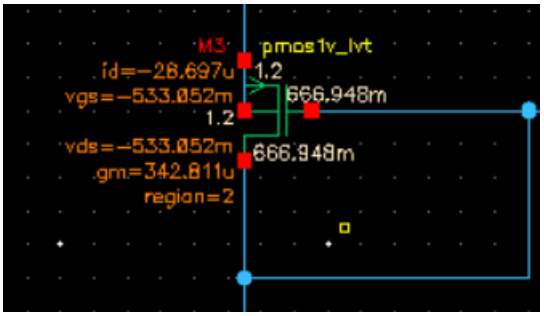
EE618_CP1_23M1195:TB_AC_DM:1	dB20(VF("/VOUT"))				
EE618_CP1_23M1195:TB_AC_DM:1	phase(VF("/VOUT"))				
EE618_CP1_23M1195:TB_AC_DM:1	Input reffered offset	-8.203m			

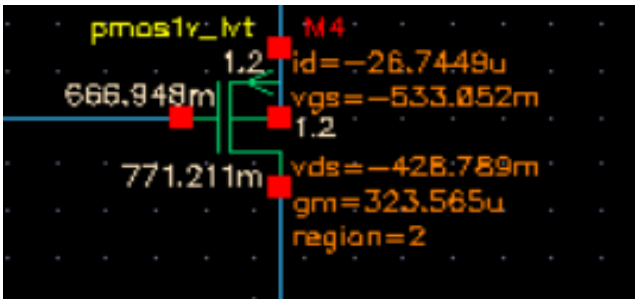
Take a screenshot of the schematic with DC operating points annotated for each transistor:

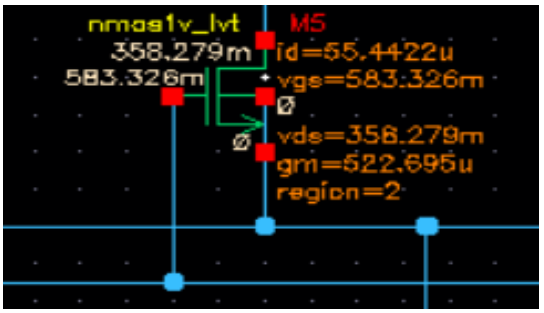


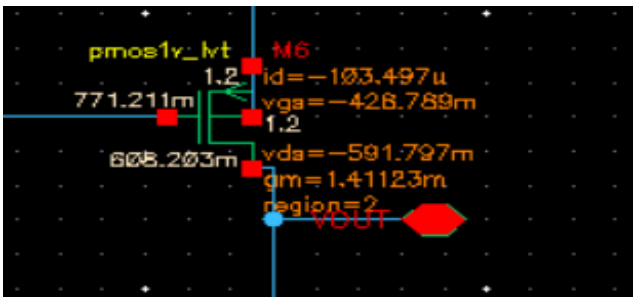


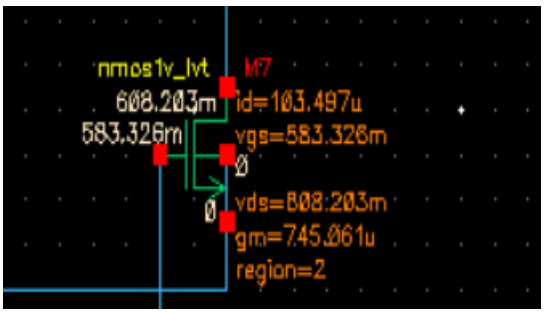


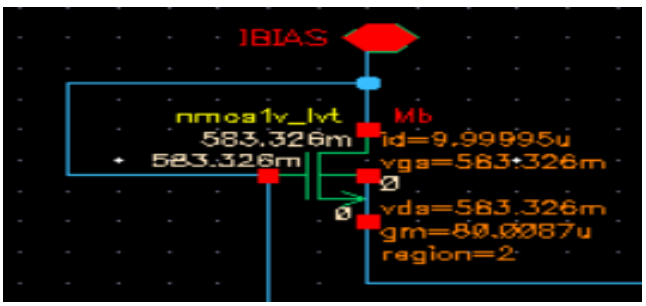








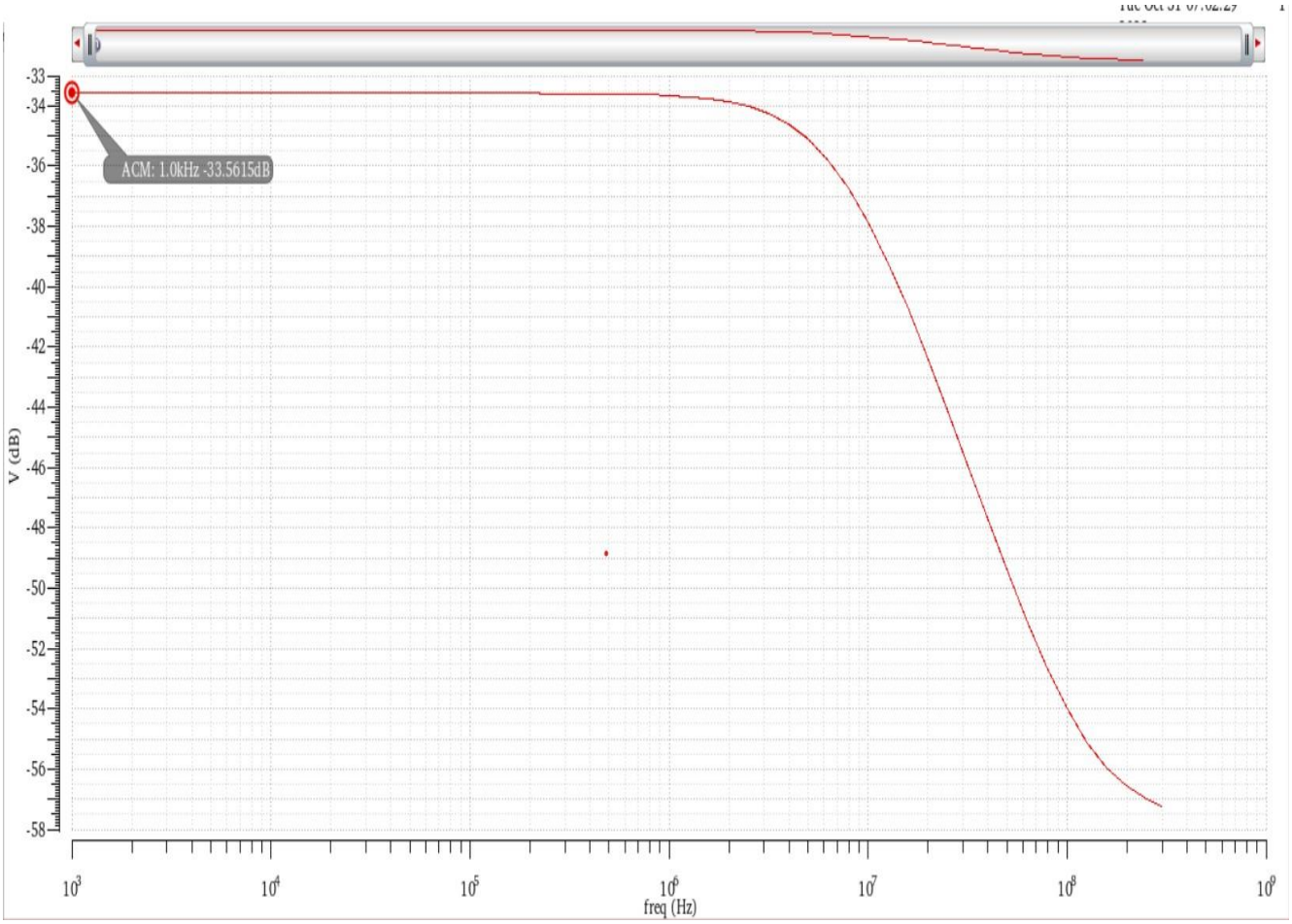




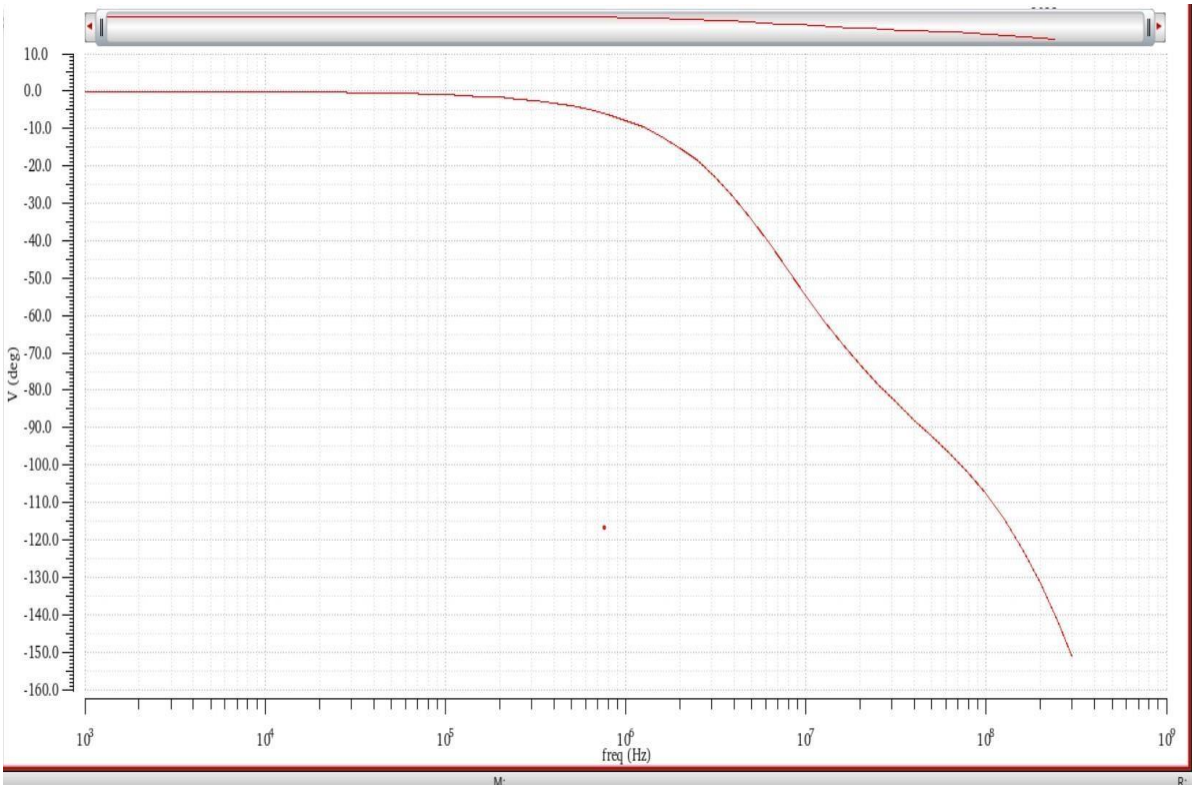
5.AC Analysis: Common Mode Gain

Plot the open loop CM gain of the OTA with clear labels:

COMMON MODE GAIN:



COMMON GAIN PHASE PLOT:



Report the CMRR of the OTA by using the differential gain simulated earlier:

CMRR CALCULATION:

DIFFERENTIAL MODE GAIN=42.569 dB

COMMON MODE GAIN=-33.562 dB

CMRR=76.13 dB

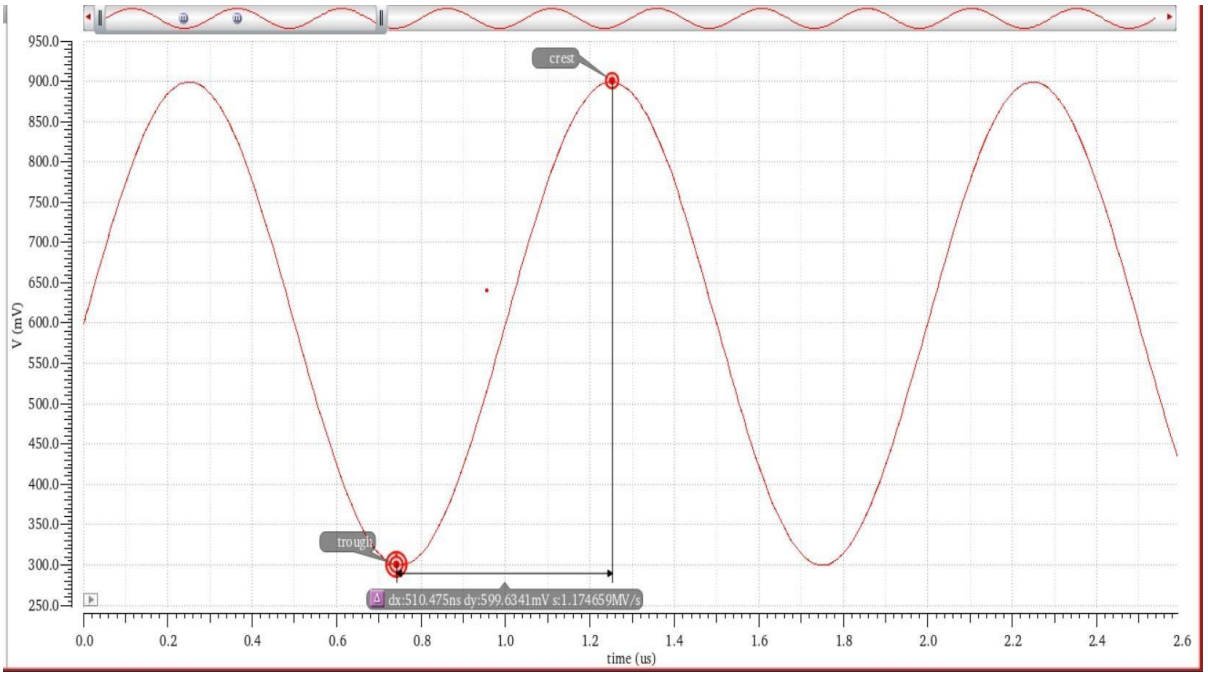
EE618_CP1_23M1195:TB_AC_CM:1	dB20(VF("/VOUT"))				
EE618_CP1_23M1195:TB_AC_CM:1	phase(VF("/VOUT"))				
EE618_CP1_23M1195:TB_AC_CM:1	ACM (in dB)	-33.56			

6. Transient Analysis: Sinusoidal Input

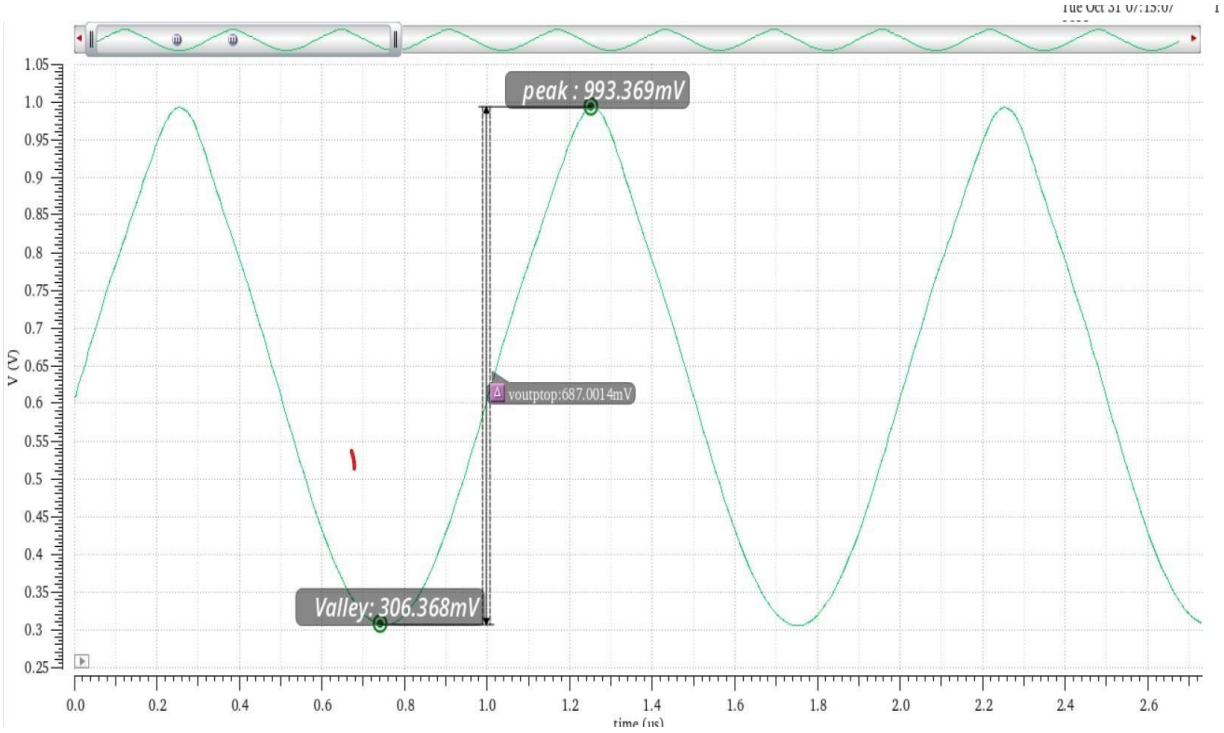
Plot the input and output transient waveform clearly annotating the peak voltages and take a screenshot of the same.

Test	Output	Nominal	Spec	Weight	Pass/Fail
EE618_CP1_23M1195:TB_TRAN_SIN:1	/VOUT				
EE618_CP1_23M1195:TB_TRAN_SIN:1	/VINP				
EE618_CP1_23M1195:TB_TRAN_SIN:1	VOUT (peak-peak)	687.5m			
EE618_CP1_23M1195:TB_TRAN_SIN:1	VIN (peak-peak)	600m			

INPUT TRANSIENT WAVEFORM:



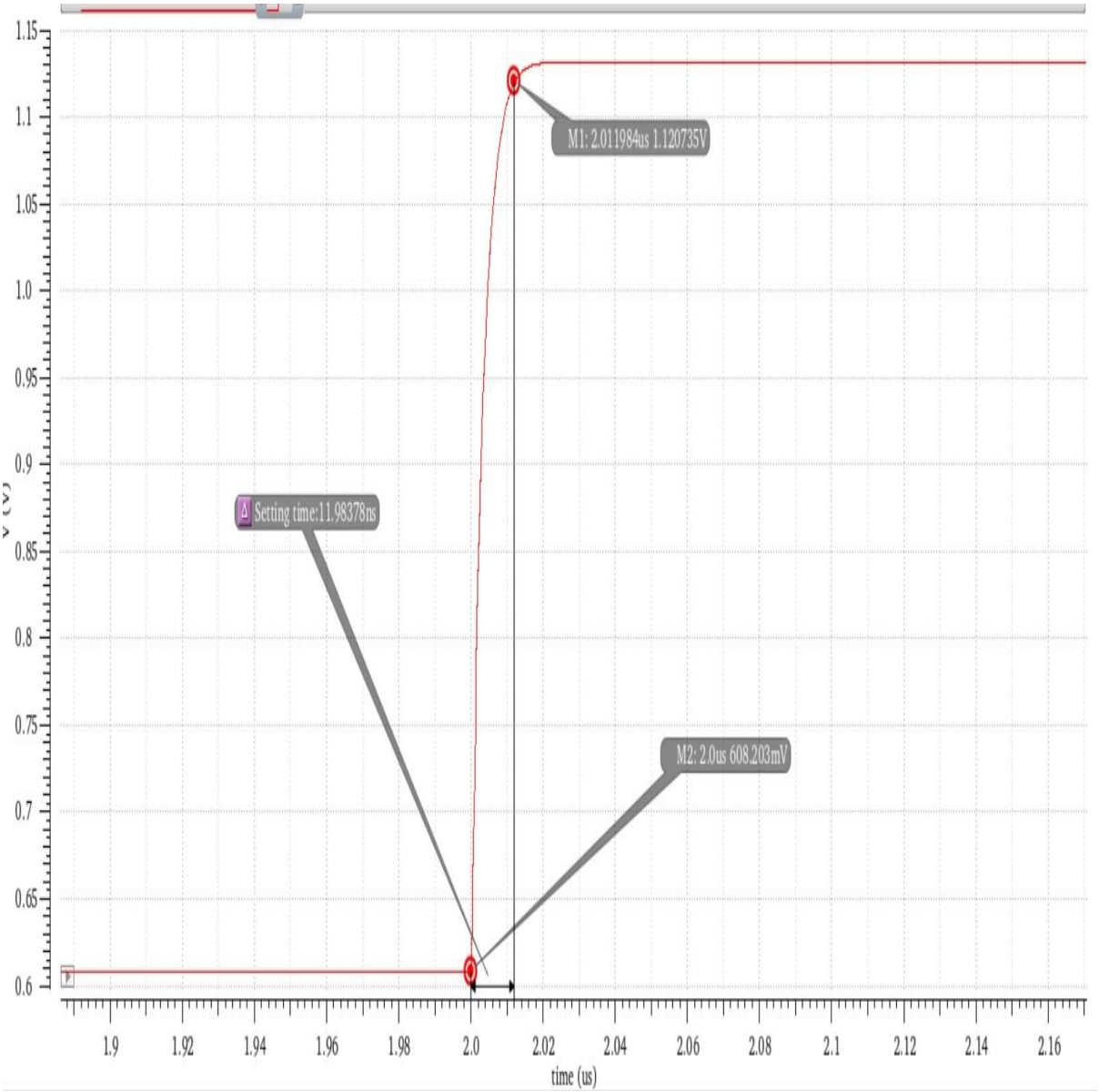
OUTPUT TRANSIENT WAVEFORM:



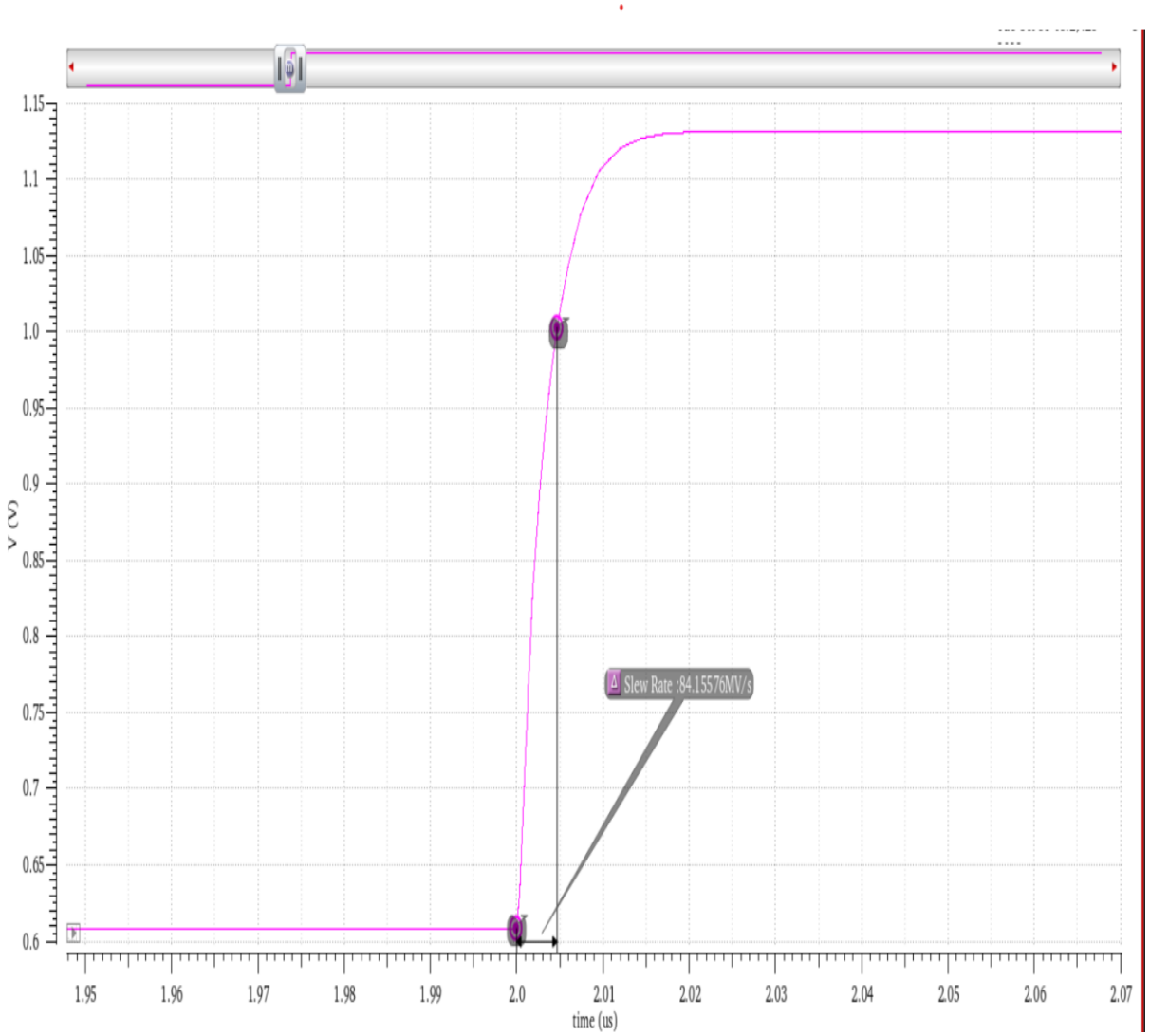
7.Transient Analysis: Step Input

Measure the slew rate and clearly show the output plot in the slewing region with cursors. ○ Measure and report the settling time, ts for 1% accuracy.

PLOT OF SETTLING TIME (1% ACCURACY):



SLEW RATE PLOT:



8. Noise Analysis

Show the input referred noise PSD from 10kHz to 300MHz band. Clearly show the input referred noise in the plot (with marker) at 1MHz and 10 MHz.

Report the integrated noise and noise contributions.

NOISE SUMMARY:

Device	Param	Noise Contribution	% Of Total
/I0/M4	fn	4.55553e-08	26.19
/I0/M2	fn	4.33853e-08	23.76
/I0/M1	fn	4.27377e-08	23.05

Spot Noise Summary (in V/sqrt(Hz)) at 100K Hz Sorted By Noise Contributors
Total Summarized Noise = 8.90143e-08
Total Input Referred Noise = 8.82737e-08
The above noise summary info is for noise data

Device	Param	Noise Contribution	% Of Total
/I0/M4	id	5.54822e-09	15.68
/I0/M2	fn	5.45849e-09	15.18
/I0/M2	id	5.37772e-09	14.73

Spot Noise Summary (in V/sqrt(Hz)) at 10M Hz Sorted By Noise Contributors
Total Summarized Noise = 1.40117e-08
Total Input Referred Noise = 1.39037e-08
The above noise summary info is for noise data

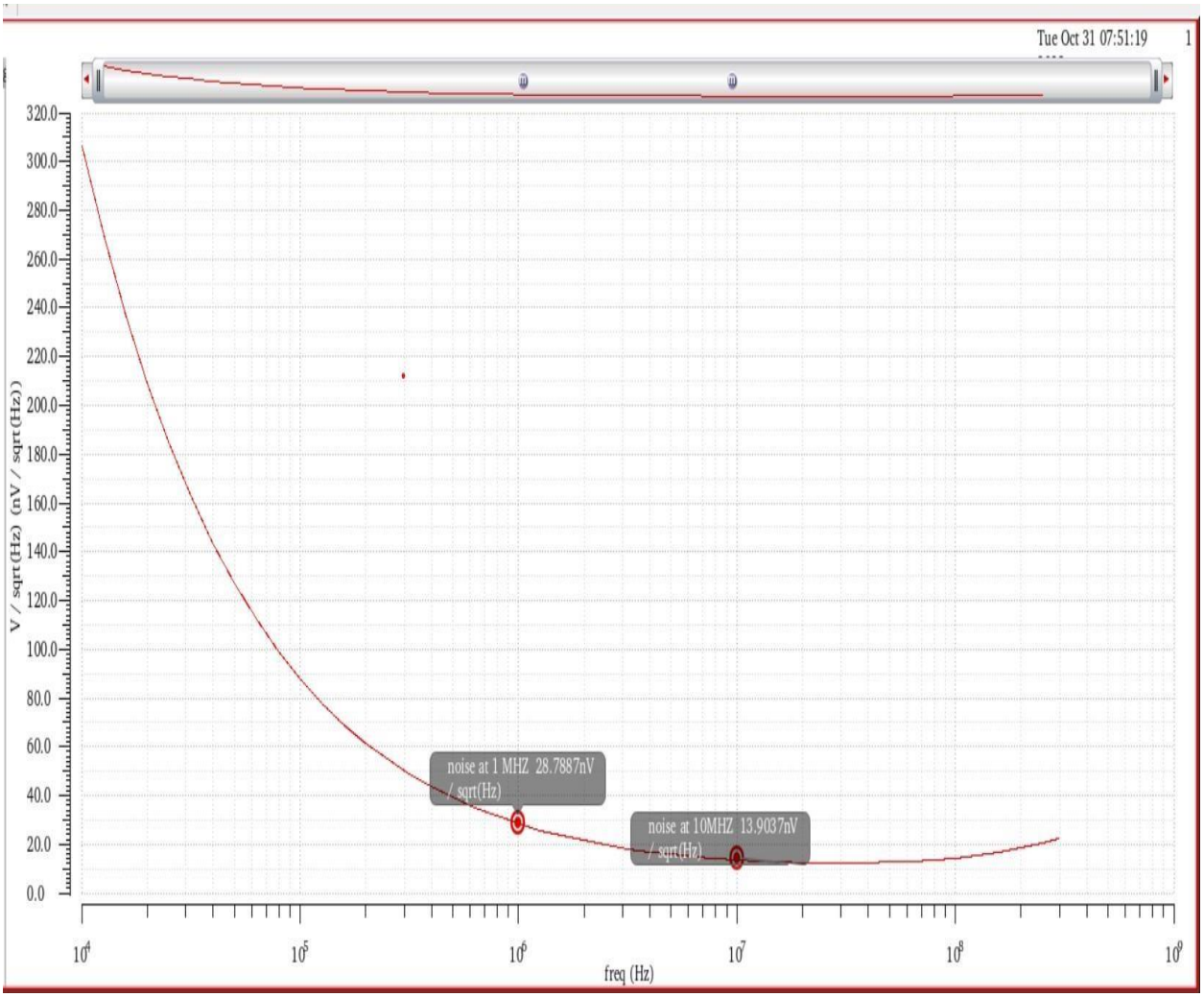
Device	Param	Noise Contribution	% Of Total
/I0/Mb	fn	9.96346e-05	21.23
/I0/M4	id	7.33754e-05	11.52
/I0/M2	id	7.06065e-05	10.66

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Summarized Noise = 0.000216229
Total Input Referred Noise = 0.000309028
The above noise summary info is for noise data

Device	Param	Noise Contribution	% Of Total
/I0/Mb	fn	9.96346e-05	21.23
/I0/M4	id	7.33754e-05	11.52
/I0/M2	id	7.06065e-05	10.66

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Summarized Noise = 0.000216229
Total Input Referred Noise = 0.000309028
The above noise summary info is for noise data

INPUT REFERRED NOISE PLOT:



Summary of results obtained:

Q.No	Parameters	Layout Results	Schematic Results
2	Power Consumption	200.1uW	202.73uW
3	DC gain	49.238dB	49.201dB
	f-3dB	420.126KHz	461.794KHz
	Unity Gain frequency	110.913MHz	120.906MHz
	Phase margin	72.002 deg	71.978 deg

4	Closed Loop Gain	73.221mdB	72.569mdB
	f-3dB	151.216MHz	163.388MHz
5	Common-mode gain	-35.611dB	-33.562dB
	CMRR	78.11dB	76.13dB
	Input referred offset (DC analysis)	-8.296mV	-8.203mV
6	Output Swing (Vpk – pk)	685.02mV	687.7mV
7	Slew rate	82.32154V/us	84.15576V/us
	Settling Time (1% accuracy)	13.26584us	11.98378 us
8	Input referred spot noise (at 0.1 MHz)	28.916nV/sqrt(Hz)	28.788nV/sqrt(Hz)
	Input referred spot noise (at 10 MHz)	14.019nV/sqrt(Hz)	13.903nV/sqrt(Hz)
	Total Summarized noise	0.000223118V	0.000216229V
	Total Input Referred Noise	0.000339019V	0.000309028V

Observation:

As we see the above table we can directly identify some parameters are increased and some parameters are decreased.

Reason:

There are several reasons why the post-layout simulation values of parameters such as gain, noise, and unity gain frequency may differ from your pre-layout expectations. Here are some common factors to consider:

1. Parasitic Components:

- Capacitance: Parasitic capacitances can significantly affect the bandwidth and speed of the circuit.

- Resistance: Parasitic resistances can affect the overall gain and frequency response.

2. Mismatch:

- Mismatch in transistor parameters due to variations in fabrication processes can lead to differences in performance between transistors. This can impact gain and other parameters.

3. Layout Effects:

- The physical layout of the components can introduce additional parasitic elements that were not considered in the schematic. For example, interconnect capacitance and resistance can affect the circuit behavior.

4. Loading Effects:

- The post-layout simulation may include the effects of loading from other components or blocks in the system that were not accurately represented in the pre-layout simulations.

5. Power Supply and Temperature Variations:

- Differences in power supply voltage or temperature during post-layout simulation can affect the characteristics of the transistors and, consequently, the overall circuit performance.

6. Model Accuracy:

- The accuracy of the models used for simulation can impact the results. Ensure that you are using accurate models that represent the behavior of the components in the technology process you are designing for.

7. Simulation Settings:

- Check the simulation settings, including convergence criteria and simulation time. In some cases, increasing the simulation time may reveal transient effects that were not captured in shorter simulations.

8. Extraction Method:

- The extraction method used for obtaining parasitic elements from the layout can also contribute to differences. Make sure the extraction method is appropriate for your design.

To troubleshoot this issue, you may want to perform a detailed analysis, including extraction of parasitics from the layout, and compare these with your pre-layout expectations. Additionally, reviewing the layout and simulation setup parameters can help identify specific factors contributing to the differences.