

Assignment - 1

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Date : 29-8-25

Q-1. Convert 11110000.1011 Binary number into decimal Number System

$$\begin{array}{cccccccccccc} \rightarrow & 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 & . & 1 & 0 & 1 & 1 \\ & 2^6 & 2^5 & 2^4 & 2^3 & 2^2 & 2^1 & 2^0 & & & 2^{-1} & 2^{-2} & 2^{-3} & 2^{-4} & 2^{-5} \\ \rightarrow & (120.71875)_{10} \end{array}$$

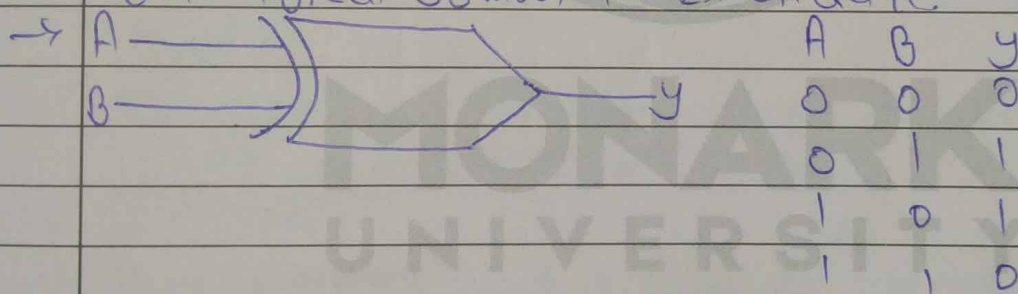
Q-2. Convert AFB_2 hex number in to octal number system

$$\rightarrow (AFB_2)_{16} = (\quad)_8$$

$$\begin{array}{cccc} A & F & B & 2 \\ 001 & 010 & 1111 & 0010 \\ \boxed{} & \boxed{} & \boxed{} & \boxed{} \\ 1 & 2 & 7 & 6 & 2 \end{array}$$

$$(127662)_8$$

Q-3. Draw logical Symbol for Ex-OR gate.



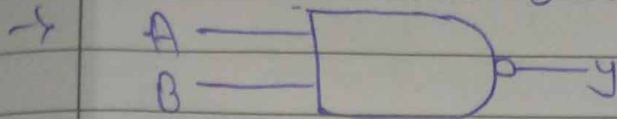
Q-4. Find is complement of 100101.

\rightarrow 1's complement means invert each Bit.
100101 \rightarrow 011010

Q-5. Define Don't Care.

\rightarrow Don't care conditions are input to a logic circuits are inputs to a logic circuit or a function that do not effect the output.

Q-6. Draw the logic symbol For NAND Gate.



A	B	y
0	0	1
0	1	1
1	0	1
1	1	0

Q-7. State De-morgan's Theorems.

→ De Morgan's Theorems are fundamental law in Boolean algebra that explain how to simplify logic expression by distributing a negation over an operation.

→ There are 2 Theorems:

(1) Theorem 1: The complement of sum of variables is equal to the product of their individual complement. → $\overline{A + B} = \overline{A} \cdot \overline{B}$

→ That a NOR Gate is equal to and AND Gate with inverted inputs.

(2) Theorem 2: The complement of a Product of Variable is equal to the Sum of their individual complements

→ $\overline{A \cdot B} = \overline{A} + \overline{B}$

→ That a NAND gate is equal to OR gate with inverted input.

Q-8. Find 2's complement of 1110000101.

→

$$\begin{array}{r}
 1110000101 \\
 \xrightarrow{\text{1's complement}} 0001111010 \\
 + 1 \\
 \hline
 0001111011 \rightarrow 2's \text{ complement}
 \end{array}$$

Assignment 2

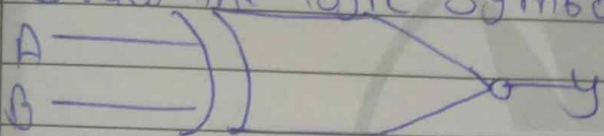
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Date : 30-8-23

Q-1. Draw the Truth table of NOR Gate.

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

2. Draw the logic Symbol For Ex-NOR Gate.

	A	B	Y
	0	0	1
	0	1	0
	1	0	0
	1	1	1

3. give Three examples of SOP.

→ (1) $y = A + B$ → This is the simplest form

→ It's the same as OR gate

→ It is a Sum of two single variable Product

(2) $z = AB + C$ → This expression combines two terms a Product (A and B) and a single variable

→ The expression says the output is True if either (A and B) is True, or if C is True.

(3) $F = \overline{A}B + B\overline{C}$ → This expression has 2 Product Terms. The first term is and The second.

First term (Not 'A' and 'B')

Second term (Not 'B' and 'C')

4. Add :- $11100000 + 11100000$

$$\begin{array}{r} \rightarrow 01110000 \\ + 11100000 \\ \hline 10101000 \rightarrow \text{Answer} \end{array}$$

5. Subtract $(10010 - 1001)$ using 1's complement and 2's complement method

\rightarrow 1's complement of $1001 = 0110$

$$\begin{array}{r} \rightarrow 10010 \\ + 01100 \\ \hline 11110 \end{array}$$

\rightarrow 1's complement of $11110 = 00001$

\rightarrow 2's complement of $1001 = 01101$

$$\begin{array}{r} \rightarrow 10010 \\ + 01101 \\ \hline 11111 \end{array}$$

\rightarrow 2's complement of $11111 = 00001$

\rightarrow 1's complement answer = 00001

\rightarrow 2's complement answer = 00001

6. $y = \sum m(0, 1, 2, 5, 13, 15)$ Draw the K-MAP and find minimized logical expression

$$\begin{array}{c|cccc} \rightarrow & AB & 00 & 01 & 11 & 10 \\ \hline 00 & 1 & 1 & 0 & 1 \\ 01 & 0 & 1 & 0 & 0 \\ 11 & 0 & 0 & 1 & 0 \\ 10 & 0 & 0 & 1 & 0 \end{array}$$

$$y = \bar{A}\bar{B}\bar{D} + \bar{A}\bar{C}D + A\bar{B}D$$

Q-7. State and Prove De-Morgan Theorems with the help of truth table.

→ The complement of sum of variable is equal to the product of their individual complements.

→ Formula : $\overline{A+B} = \overline{A} \cdot \overline{B}$

→ Proof using a Truth table : 1st Theorem.

→ the Two sides of the equation $\overline{A+B}$ and $\overline{A} \cdot \overline{B}$ are equivalent if their truth table outputs are identical for all possible input combinations.

→	A	B	A+B	$\overline{A+B}$	\overline{A}	\overline{B}	$\overline{A} \cdot \overline{B}$
	0	0	0	1	1	1	1
	0	1	1	0	1	0	0
	1	0	1	0	0	1	0
	1	1	1	0	0	0	0

→ The output columns for $\overline{A+B}$ and $\overline{A} \cdot \overline{B}$ are same.

→ Second Theorem :

→ The complement of a product of variables is equal to the sum of their individual complements.

→	A	B	A.B	$\overline{A.B}$	\overline{A}	\overline{B}	$\overline{A} + \overline{B}$
	0	0	0	1	1	1	1
	0	1	0	1	1	0	1
	1	0	0	1	0	1	1
	1	1	1	0	0	0	0

→ $\overline{A.B} = \overline{A} + \overline{B}$

- 8 Write a short note on Rom.
- Rom is type of Memory that store data Permanently, its contents are set during the manufacturing Process and cannot be changed or erased by the user.
 - Non-Volatile? Rom is Non-Volatile Meaning it Retains the Stored information even when the Power is turned off.
 - Types of Rom:
 - (1) P Rom (Programmable Rom)
 - (2) E Rom (Erasable P Rom)
 - (3) EE Rom (Electrically Erasable P Rom)
 - use to store essential software that controls the hardware.

Assignment-3

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Date : 31-8-25

Q-1. Convert the expression $y = AB + A\bar{C} + BC$ into the Standard Form

→ Missing Term : $\bar{A}B(C + \bar{C}) + A\bar{C}(B + \bar{B}) + BC(A + \bar{A})$
 $= ABC + AB\bar{C} + A\bar{C}B + A\bar{C}\bar{B} + BCA + B\bar{C}\bar{A}$
 $= ABC + AB\bar{C} + A\bar{C}B + B\bar{C}\bar{A}$
 SOP is $ABC + AB\bar{C} + A\bar{C}B + B\bar{C}\bar{A}$

Q-2. Prove That $(A+C)(A+D)(B+C)(B+D) = AB + CD$

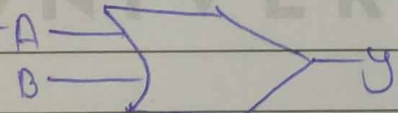
→ $(A+C)(A+D)(B+C)(B+D) = AB + CD$

$(A+C)(A+D) = A.A + A.D + C.A + C.D$
 $= A + AD + CA + CD$
 $= A + CD$

→ First Part = $(A+C)(A+D) = A + CD$

→ Second Part $(B+C)(B+D) = B + CD$
 $= A + CD \cdot B + CD$
 $= AB + CD$
 $= LHS = RHS$

Q-3. Draw the logic symbol and Truth table for all gates.

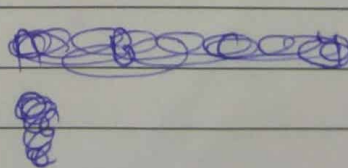
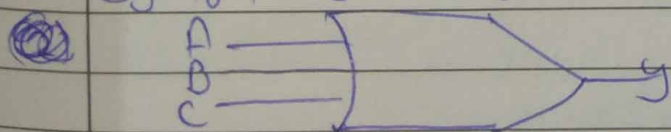
Q1) OR Gate : 

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

 ← Truth table

Symbol : Two variable

Symbol : 3 variable

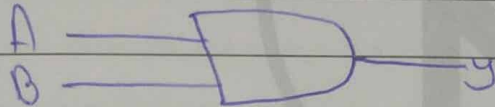


Truth table :

A	B	C	y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

(2) And Gate :

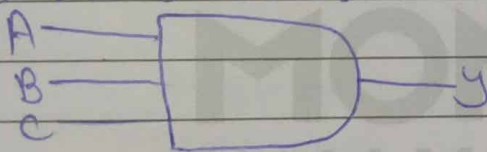
Symbol : 2 Variable



Truth table :

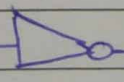
A	B	y
0	0	0
0	1	0
1	0	0
1	1	1

Symbol : 3 Variable



Truth table :

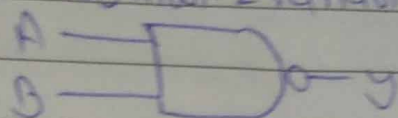
A	B	C	y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

(3) Not Gate : symbol : A —  — y

Truth table :

A	y
0	1
1	0

(4) NAND Gate: Symbol: 2 Variable



Truth table: A B y

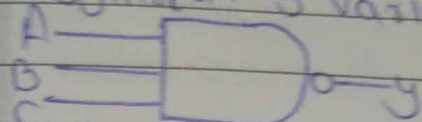
0 0 1

0 1 1

1 0 1

1 1 0

Symbol: 3 Variable



Truth table:

A B C y

0 0 0 1

0 0 1 1

0 1 0 1

0 1 1 1

1 0 0 1

1 0 1 1

1 1 0 1

1 1 1 0

-4 Explain minterm and maxterm

→ minterm: Minterm are also known as Canonical Product term

→ A minterm is Product (AND) Term that contains all the Variable of a Function

→ A value of the Minterm is '1' for exactly one unique combination of the input variable

→ Maxterm: Maxterm are also known as Canonical sum term.

→ A Maxterm is Sum (OR) Term That also contains all the Variable of a function

→ A Maxterm evaluates to '0' for exactly one unique combination of the input variable

2-5. Subtract $10010 - 10011$ using 2's complement method.
 $10011 \rightarrow 01100 \rightarrow 1's \text{ complement}$

$+ 1$

$01101 \rightarrow 2's \text{ complement}$

$\rightarrow 10010 \rightarrow \text{invert each Bit}$

$+ 01101$
 $11111 \rightarrow 00000$

$11111 \rightarrow 00000 \text{ means } -1$

6. Explain R-S and D-Flip Flop.

\rightarrow R-S Flip-Flop: The R-S (Reset-Set) Flip-Flop, also known as an R-S latch, is the simplest types of Flip-Flop.

\rightarrow It has two inputs R and S, and two outputs Q and \bar{Q} which are always complements of each other.

\rightarrow It can be built using either NAND gates or NOR Gates.

\rightarrow D Flip-Flop: The D (Data or Delay) Flip-Flop is an improved version of R-S Flip-Flop that eliminated the invalid state.

\rightarrow It has a single data input, D, and a clock input, CLK.

\rightarrow The D Flip-Flop transfers the value of the D input to the output at a specific movement in time, determined by the clock signal.

Q-7. Explain 2 to 4 line Decoder.

→ Truth table :-

		2x4 Binary Decoder					
A	B			Q ₀	Q ₁	Q ₂	Q ₃
0	0			1	0	0	0
0	1			0	1	0	0
1	0			0	0	1	0
1	1			0	0	0	1

→ A 2 to 4 line Decoder is combination of logic circuit that convert a 2-bit Binary input into one of 4 unique output lines.

→ It has 2 input and 4 outputs.

-8. Reduce The expression: $y = A + B(CA\bar{C} + (B + \bar{C})D)$

$$y = A + B(CA\bar{C} + (B + \bar{C})D)$$

$$y = A + B(CA\bar{C} + BD + \bar{C}D)$$

$$y = A + BAC + BBD + B\bar{C}D$$

$$y = A + BAC + BD + B\bar{C}D$$

$$y = A + AC(B\bar{C}) + BD + B\bar{C}D$$

$$y = A + BD + B\bar{C}D$$

$$y = A + BD(1 + \bar{C})$$

$$1 + \bar{C} = 1$$

$$y = A + BD(1)$$

$$\boxed{y = A + BD}$$

Assignment - 4

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Date : 1-9-25

Q-1. Conversion?

(1) Binary to Hexadecimal - $(1011011011)_2$

→ Use '8421' rule:

$\begin{matrix} 8 & 4 & 2 & 1 & 8 & 4 & 2 & 1 & 8 & 4 & 2 & 1 \\ 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 0 & 1 & 1 \end{matrix}$

= $\boxed{2DB}$

(2) Hex to Decimal - $(2DB)_{16}$

→ $(2DB)_{16}$

$$= (2 \times 16^2) + (B \times 16^1) + (11 \times 16^0)$$

$$= 512 + 208 + 11$$

= $\boxed{(731)_{10}}$

(3) Octal to Hex - $(756.603)_8$

→ $(756.603)_8$

$$= \underline{111} \underline{101} \underline{110} . \underline{110} \underline{000} \underline{011}$$

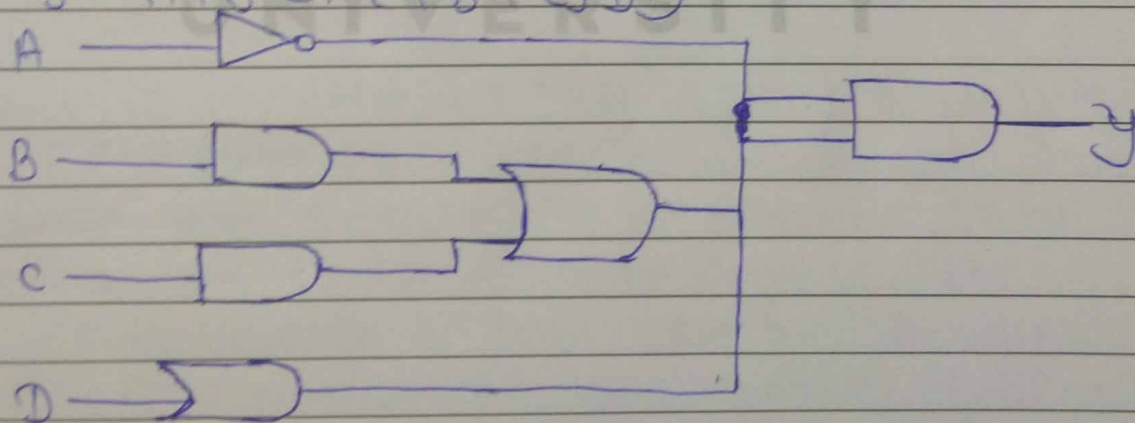
$$= \underline{1} \underline{1110} \underline{1110} . \underline{1100} \underline{0001} \underline{1}$$

$$= \underline{1} \underline{E} \underline{E} . \underline{C} \underline{1} \underline{8}$$

= $\boxed{(1EE.C18)_{16}}$

Q-2. Draw the logic circuit of $y = A + B(Ac + (B + \bar{C})D)$.

→ $y = A + B(Ac + B + \bar{C})D$



Q-3. Compare SOP and POS.

SOP	POS
(1) Sum of Product	(1) Product of sum
(2) Each Product term represent a min term.	(2) Each Sum term represent a Max term.
(3) Design using AND-OR Gate	(3) Design using OR-AND Gate
(4) $F = AB + \bar{A}C$	(4) $F = (A+B)(\bar{A}+D)$

Q-4. using K-MAP Realize The following expression using minimum number of gates. $y = \sum m(1, 3, 4, 5, 7, 9, 11, 13, 15)$

→

	CD	00	01	11	10
AB	00	0	1	1	0
	01	1	1	1	0
	10	0	1	1	0
	11	0	1	1	0

→ $y = D + \bar{A}B\bar{C}$

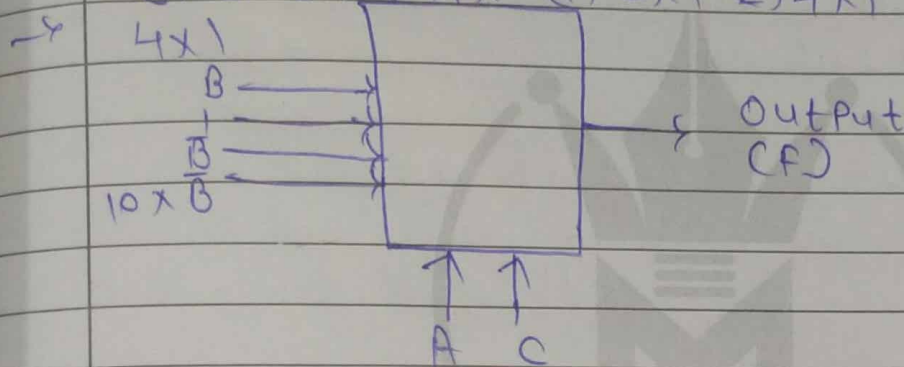
Q-5. What is Multiplexer? Explain Types of multiplexer.

→ A multiplexer (mux) is combinational logic circuit that selects one of several input lines and routes it to a single output line.

→ It often called a 'Data Selector' because it acts like a switch that chooses a specific input to pass through to the output.

- A mux has 2^n input lines, n select lines, and one output line.
- The value of the select lines determines which of the 2^n input lines is connected to the single output.

→ Types of Mux: (1) 2×1 (2) 4×1 (3) 8×1 (4) 16×1

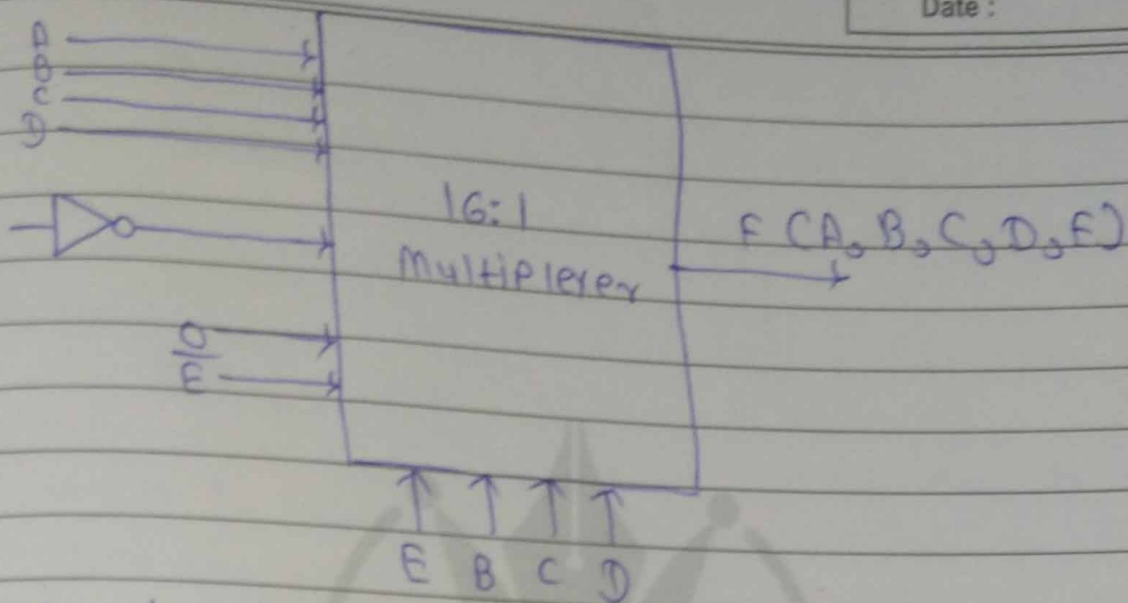


→ Truth table

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Q-6. Implement the following function using 16×1 multiplexer. $F(A, B, C, D, E) = \sum m(2, 4, 5, 7, 10, 14, 15, 16, 17, 25, 30, 31)$.

→



Q-7. Define K-MAP and Explain structure For Three and Four-Variable K-MAP.

→ 3 Variable K-MAP:-

→ A 3-Variable K-MAP is a grid with $2^3=8$ cells.

→ The Variables are typically arranged with two Variables defining the rows and the third Variable defining the column.

→ the Variables are ordered according to gray code (00, 01, 10, 11) where only one Bit changes Between Adjacent cells.

→ The MAP is 2×4 grid or a 4×2 grid.

→ 4 Variable K-MAP:-

→ A 4 variables K-MAP is a grid with $2^4=16$ cells.

Typically arranged in 4×4 grid.

→ The rows and columns are Defined by Pairs of Variables, with each Pair following The gray Code Sequence.

→ This structure allows For grouping of cells in groups of 2, 4, 8 or 16.

Q-8. classify Memory.

→ There are Two main Types (1) Primary Memory
(2) Secondary Memory

(1) Primary Memory:

→ Primary Memory is also known as main memory is the computer's working memory.

→ It's Directly accessible by the central Processing unit (CPU) and is used to hold data and Programs that are currently being Processed.

→ It is generally much faster but more expensive than Secondary Memory.

→ 2 Types of Primary Memory: (1) RAM
(2) ROM

(2) Secondary Memory:

→ Secondary Memory, also called auxiliary memory, is non-volatile storage used for long-term data Program storage.

→ It is not directly Accessible by the CPU.

→ Data must first be loaded into Primary Memory.

→ It is much slower and cheaper than Primary Memory.

→ Types: (1) HDD
(2) SSD
(3) Optic storage