SCHOOL OF COMPUTING AND I

II B.Tech. IV Semester; Second- Sessional E

Branch: CSE / IT /CCE

(OPEN BOOK EXAMINATION)

Course Code: CS1401

Course Name : Operating Systems

Max. Marks : 20 Durati

Instructions:

- All questions are compulsory
- Missing data if any can be suitably assumed
- Two books and one notebook / spiral bound is allowed

1. Three concurrent processes X, Y, and Z execute three different code segments that access and update certain shared variables. Process X executes the P operation (i.e., wait) on semaphores a, b and c; process Y executes the P operation on semaphores b, c and d; process Z executes the P operation on semaphores c, d, and a before entering the respective code segments. After completing the execution of its code segment, each process invokes the V operation (i.e., signal) on its three semaphores. All semaphores are binary semaphores initialized to one. Write the sequence of P operations on semaphores a, b, c and d that should be followed by processes X, Y and Z, so that the system would be deadlock free. [3]

2. Write the solution of Readers-Writers problem using monitors. [4]

3. Consider a system with five processes P_0 through P_4 and four resource types A,B,C and D. Resource type A has 16 instances, type B has 23 instances, type C has 27 instances and type D has 4 instances. Suppose that the following snapshot of the system has been taken at a given time:

Process	*Resources Allocated*	*Maximum Resources Required*
	A B C D	*A B C D*
P_0	4 1 0 0	6 5 6 0
P_1	2 3 6 0	2 5 6 0
P_2	4 5 3 1	6 5 3 2
P_3	2 1 0 0	2 1 0 0
P_4	0 0 0 1	0 5 7 1

Answer the following using Banker's algorithm.

a. What is the content of matrix *Need*? [1]

b. Is the system in a safe state? If yes, write the safe sequence. [2]

c. If a request from process P_4 arrives for (0, 2, 4, 0), can the request be granted immediately? [3]

4. Consider a simple paging system with following parameters: 2^{32} bytes of logical memory; page size of 4KB; 2^{10} frames in physical address space. Answer the following:

a. How many bits are in a physical address?

b. How many bytes in a frame?

c. How many entries are required in the page table?

d. How many bits in the physical address specify the frame? [4]

5. On a paging system, consider that associative registers (TLB) hold the most active page entries and the full page table is stored in main memory. The TLB access time is 10 nsec and memory access time is 100 nsec. What hit ratio is required to achieve an effective memory access time of 150 nsec? [3]