SCHOOL OF COMPUTING AND IT
IV Semester B. Tech Make up Examination, July 2017
Branch: CSE / IT /CCE
(OPEN BOOK EXAMINATION)

Subject Code: CS1401
Subject Name : Operating Systems
Max. Marks: 80 **Duration: 3 hours**

Instructions:

- Answer any FIVE full questions. Numbers in [] indicates marks.
- Missing data if any can be suitably assumed
- Two books and one notebook / spiral bound book is allowed.

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1. Consider the following set of processes with the estimated CPU bursts given in milliseconds, and lower priority numbers corresponding to highest CPU priority (1 is the highest).

Process	Burst Time	Priority	Arrival Time
P1	10	3	0
P2	1	1	1
P3	2	3	2
P4	1	4	3
P5	5	2	4

   a) Draw four Gantt charts that illustrates the execution of these processes using these scheduling algorithms: Non-preemptive SJF, Preemptive SJF, Priority and Round Robin (time quantum=2) [8]
   b) Calculate the waiting time of each process for each of the scheduling algorithm [4]
   c) Calculate the turnaround time of each process for each of the scheduling algorithm [4]

2. A) Consider a logical address space of 32 pages of 2048 words each, mapped onto a physical memory of 8 frames.
   a) How many bits are needed for addressing the total logical address? [2]
   b) How many bits are needed to indicate the page number? [2]
   c) How many bits are needed for addressing the physical address? [2]
   d) What is the effect of allowing more than one entry in a page table (each entry belongs to a process) to point to the same frame in physical memory. [2]

   B) A computer with a 32-bit address uses a two-level page table. Virtual addresses are split into a 9-bit top-level page table field, an 11-bit second-level page table field, and an offset.
   a) How large are the pages [4]
   b) How many pages are there in the address space? [4]

3. A). How many page faults occur for optimal, FIFO and LRU page replacement algorithm for the following reference string, with four page frames in memory? [12]

   1,2,3,4,5,3,4,1,6,7,8,7,8,9,7,8,9,5,4,5,4,2.

   B). Consider a memory system with a TLB access time of 10ns and a memory access time of 200ns, including the time to check the TLB. What hit rate H would we need in order to achieve an effective access time 10% greater than the cache access time? [4]

4. Consider the following snapshot of a system.

Process	Allocation	Max	Available
	A,B,C,D	A,B,C,D	A,B,C,D
P0	0,0,1,2	0,0,1,2	1,5,2,0
P1	1,0,0,0	1,7,5,0	
P2	1,3,5,4	2,3,5,6	
P3	0,6,3,2	0,6,5,2	
P4	0,0,1,4	0,6,5,6	

Answer the following using banker's algorithm.

a) What is the content of matrix need? [2]
b) Derive the safe sequence. [8]
c) If the request (0, 4, 2, 0) for resources (A,B,C,D) respectively from process P1 arrives, Can the request be granted immediately. [6]

5. Disk requests come into the disk driver for cylinders: 10, 22, 20, 2, 40, 6, 38 in that order. The disk has 60 total cylinders and the disk head is currently positioned over cylinder 20. A seek takes 6 milliseconds per cylinder moved. What is the sequence of reads and total seek time using each of the following algorithms:- a) FCFS, b) SSTF, c) LOOK, d) SCAN [16]

6. (A). Two processes X and Y need to access a critical section. Consider the following synchronization construct used by both the processes. Does the following solution satisfy entire three requirements of critical section problem? Justify your answer. [8]

```
Process X
while (true) {
   varP = true;
   while (varQ == true)
   {  /* Critical Section */
      varP = false;
   }}
```

```
Process Y
while (true) {
   varQ = true;
   while (varP == true)
   {  /* Critical Section */
      varQ = false;
   }}
```

(B). Write a Program to create two processes to run a loop in which one process adds all even numbers and the other adds all the odd numbers in a series of numbers from 1-20. (Hint: use fork ( )) [8]