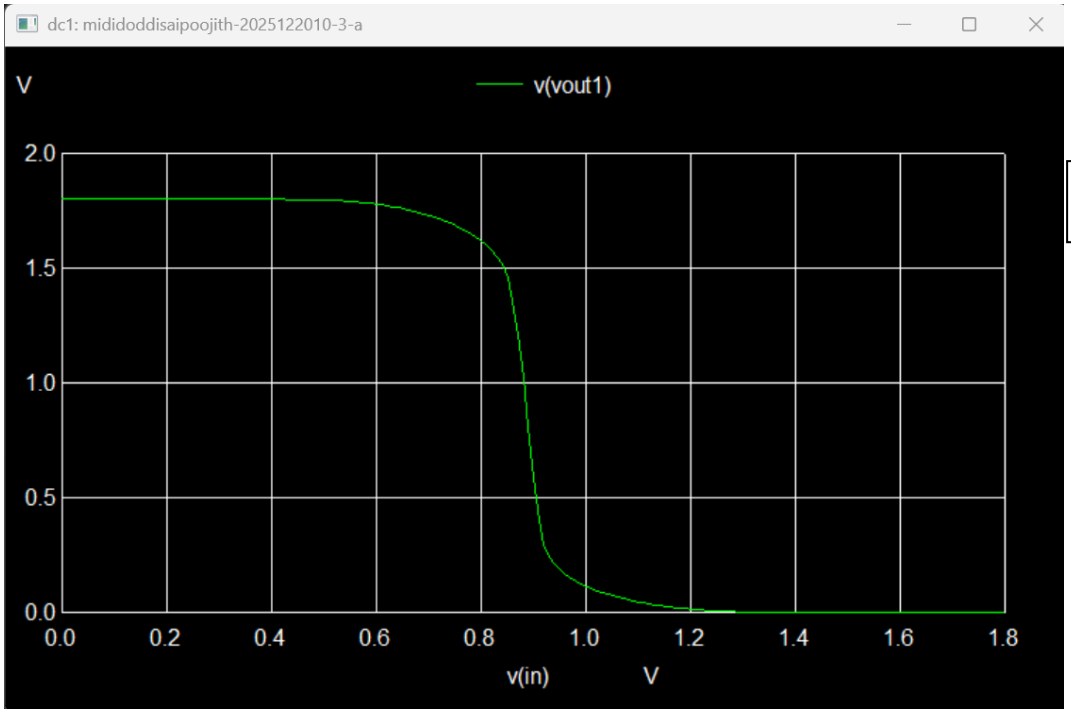
3-A

Netlist used

Q_3_a.spice

```
* CMOS Inverter VTC Simulation (VTC of inverter-1)
.include TSMC_180nm.txt
.param Wn = 18u
.param Wp = {2.5*Wn}
.param L = 0.18u
.global gnd
.subckt inverter in out vdd gnd Wn={Wn} Wp={Wp} L={L}
M1 out in gnd gnd CMOSN W={Wn} L={L}
M2 out in vdd vdd CMOSP W={Wp} L={L}
.ends inverter
Vdd vdd gnd 1.8
Vin in gnd 0
Xinv1 in vout1 vdd gnd inverter Wn={Wn} Wp={Wp} L={L}
Xinv2 vout1 vout2 vdd gnd inverter Wn={Wn} Wp={Wp} L={L}
.control
dc Vin 0 1.8 0.01
run
set curplottitle="mididoddisaipoojith-2025122010-3-A"
plot v(vout1) vs v(in)
.endc
.end
```

simulation data



VTC of inverter-1 (I1)

When a CMOS inverter drives another identical inverter, the input of the second inverter acts as a capacitive load on the first. Thus, the VTC of the first inverter remains essentially the same as a single CMOS inverter, with only a slight effect due to loading. The overall shape is unchanged.

3-B

Netlist used

```
Q_3_b.spice
1   * CMOS Inverter (to find the noise margin parameters)
2   .include TSMC_180nm.txt
3   .param Wn = 18u
4   .param Wp = {2.5*Wn}
5   .param L = 0.18u
6   .global gnd
7   .subckt inverter in out vdd gnd Wn={Wn} Wp={Wp} L={L}
8   M1 out in gnd gnd CMOSN W={Wn} L={L}
9   M2 out in vdd vdd CMOSP W={Wp} L={L}
10  .ends inverter
11  Vdd vdd gnd 1.8
12  Vin in gnd 0
13  Xinv1 in vout1 vdd gnd inverter Wn={Wn} Wp={Wp} L={L}
14  Xinv2 vout1 vout2 vdd gnd inverter Wn={Wn} Wp={Wp} L={L}
15  .control
16  dc Vin 0 1.8 0.002
17  run
18  let dV = deriv(v(vout1))
19  meas dc VIL  find v(in)    when dV=-1 cross=1
20  meas dc VOH  find v(vout1) when dV=-1 cross=1
21  meas dc VIH  find v(in)    when dV=-1 cross=2
22  meas dc VOL  find v(vout1) when dV=-1 cross=2
23  let NMH = VOH - VIH
24  let NML = VIL - VOL
25  print VIL VOH VIH VOL
26  print NMH NML
27  plot v(vout1) vs v(in)
28  .endc
29  .end
```

simulation data

```
vil = 7.456705e-01
voh = 1.689961e+00
vih = 1.002331e+00
vol = 1.114904e-01
nmh = 6.876300e-01
nml = 6.341801e-01
ngspice 1 ->
```

3-b $V_{Tn} = 0.54V = |V_{Tp}|$

$$V_{IL} = \frac{3V_{DD} + 5V_{Tn} - 3|V_{Tp}|}{8}$$

$$= \frac{3V_{DD} + 2V_{Tn}}{8} = \frac{3(1.8) + 2(0.54)}{8}$$

$$\boxed{V_{IL} = 0.81}$$

$$V_{OH} = \frac{7V_{DD} + V_{Tn} + |V_{Tp}|}{8}$$

$$\boxed{V_{OH} = 1.71V}$$

$$V_{IH} = \frac{5V_{DD} + 3V_{Tn} - 5|V_{Tp}|}{8} \qquad V_{OL} = \frac{V_{DD} - V_{Tn} - |V_{Tp}|}{8}$$

$$\boxed{V_{IH} = 0.99V} \qquad \boxed{V_{OL} = 0.09V}$$

$$NM_L = V_{IL} - V_{OL} \Rightarrow \boxed{NM_L = 0.72V}$$

$$NM_H = V_{OH} - V_{IH} \Rightarrow \boxed{NM_H = 0.72V}$$

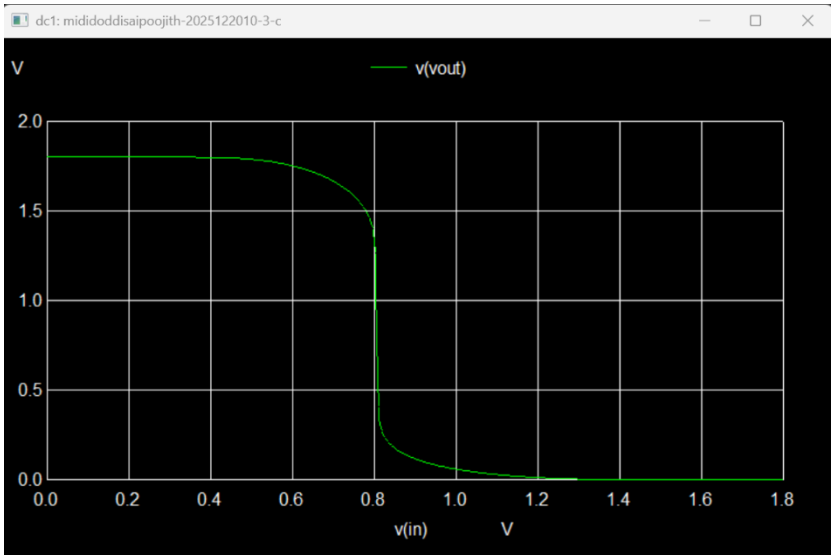
Resons for Different Noise margin values

9) The formula we were using, derived by assuming no velocity saturation, no mobility degradation, no channel-length modulation, ~~AC~~ but in practical those effects will be there so we will get slightly different noise margin parameters.

3-C

simulation data

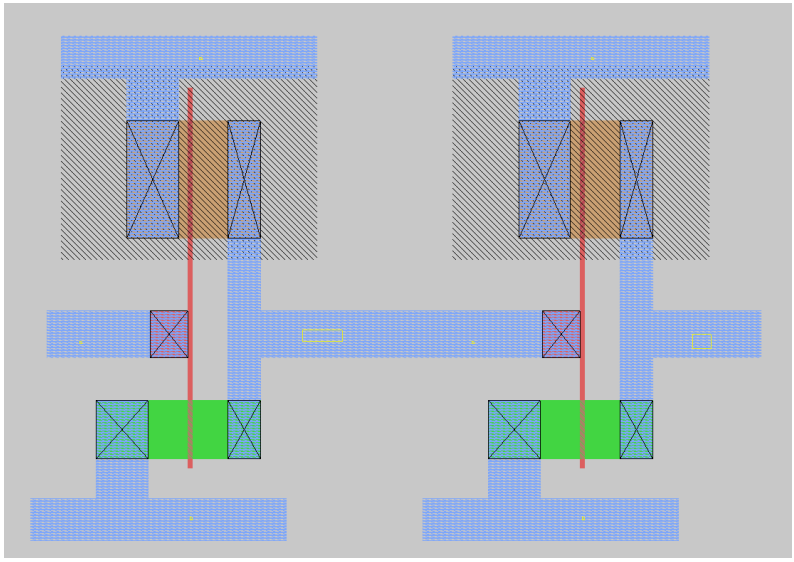
```
vil  = 6.741419e-01
voh  = 1.694980e+00
vih  = 8.860775e-01
vol  = 1.287589e-01
nmh  = 8.089025e-01
nml  = 5.453830e-01
ngspice 1 ->
```



Netlist used

```
Q_3_c.spice
.include TSMC_180nm.txt
Vdd vdd 0 1.8
Vin in  0  0
M1000 vout in  vdd vdd CMOSP w=50u l=2u
+ ad=1.45n pd=0.158m as=1.3n ps=0.152m
M1002 vout in  0   0  CMOSN w=25u l=2u
+ ad=0.725n pd=0.108m as=0.975n ps=0.128m
M1001 voutf vout vdd vdd CMOSP w=50u l=2u
+ ad=1.45n pd=0.158m as=1.3n ps=0.152m
M1003 voutf vout 0   0  CMOSN w=25u l=2u
+ ad=0.725n pd=0.108m as=0.975n ps=0.128m
C1   vout  vdd   0.30108f
C2   voutf vout  0.04038f
C4   vout  vdd   0.00805f
C5   vout  vdd   0.30108f
C7   voutf 0     0.96422f
C8   vdd   0     1.6689f
C9   vout  0     3.67844f
C10  vout  0     8.97733f
C11  vout  0     8.97733f
.dc Vin 0 1.8 0.002
.control
run
let dV = deriv(v(vout))
meas dc VIL  find v(in)    when dV=-1 cross=1
meas dc VOH  find v(vout)  when dV=-1 cross=1
meas dc VIH  find v(in)    when dV=-1 cross=2
meas dc VOL  find v(vout)  when dV=-1 cross=2
let NMH = VOH - VIH
let NML = VIL - VOL
print VIL VOH VIH VOL NMH NML
set curplottitle="mididoddisaipoojith-2025122010-3-C"
plot v(vout) vs v(in)
.endc
```

MAGIC layout



3-C	V_{IL}	V_{OH}	V_{IH}	V_{OL}	NM_H	NM_L	
pre-layout	0.74	1.68	1.00	0.11	0.68	0.63	(V)
post-layout	0.67	1.69	0.88	0.12	0.80	0.54	(V)

↳ The difference b/w pre-layout and post-layout noise margins is due to parasitic capacitances and resistances extracted from layout. In post-layout case, these effect the VTC, which in turn alters V_{OH}, V_{OL}, V_{IL}, V_{IH}. So noise margin parameters change.

4-A

(4-a) From 3-b

$V_{Tn} = |V_{Tp}| = 0.54$

$V_{OH} = 1.071\,V$ $\quad V_{IL} = 0.81\,V$

$V_{IH} = 0.99\,V$ $\quad V_{OL} = 0.09\,V$

(9)

$$\frac{k_p \tau_{rise}}{C_L} = \frac{2[V_{eL} + |V_{tp}|]}{k_p (V_{DD} - V_{iL} - |V_{tp}|)^2} + \ln\left(\frac{V_{DD} + V_{OH} - 2V_I - 2|V_{tp}|}{V_{DD} - V_{OH}}\right) \Big/ (V_{DD} - V_{iL} - |V_{tp}|)$$

$$\Rightarrow \frac{k_p \tau_{rise}}{C_L} = \frac{2[0.81 + 0.54]}{(1.8 - 0.81 - 0.54)^2} + \ln\left(\frac{1.8 + 1.071 - 1.62 - 1.08}{1.8 - 1.071}\right) \Big/ (1.8 - 0.81 - 0.54)$$

$$= 18.18$$

$$\therefore \frac{k_p \tau_{rise}}{C_L} = 18.18$$

9-1)

$$\frac{k_n \tau_{fall}}{C} = \frac{2(V_{DD} - V_{IH} + V_{tn})}{(V_{IH} - V_{tn})^2} + \ln\left(\frac{2(V_{IH} - V_{tn}) - V_{OL}}{V_{OL}}\right) \Big/ (V_{IH} - V_{tn})$$

$$\Rightarrow \frac{k_n \tau_{fall}}{C} = \frac{2 \cdot (1.8 - 0.99 + 0.54)}{(0.99 - 0.54)^2} + \ln\left(\frac{2(0.99 - 0.54) - 0.09}{0.09}\right) \Big/ (0.99 - 0.54)$$

$$= 18.21$$

$$\therefore \frac{k_p \tau_{rise}}{C_L} = 18.18$$

$$\frac{k_p \tau_{fall}}{C} = 18.21$$

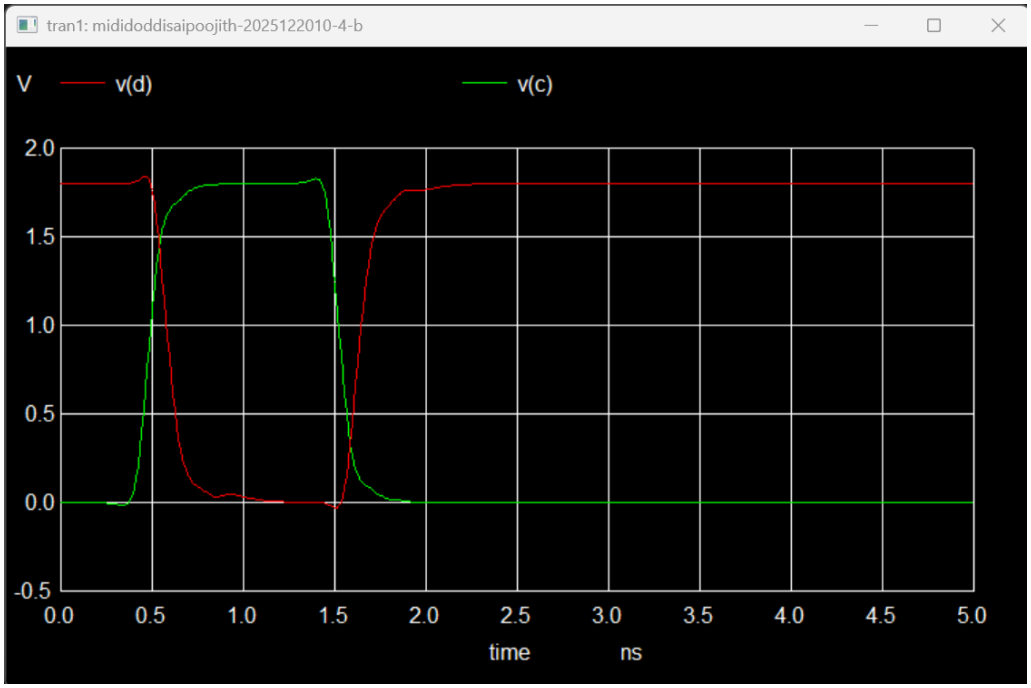
4-B

Netlist used

Q_4_b.spice

```
* FO4 Inverter Chain Example (Measure Rise/Fall Times at C and D)
.include TSMC_180nm.txt
.param Wn=1.8u
.param Wp={2.5*Wn}
.param L=0.18u
.global gnd
.subckt inverter in out vdd gnd Wn={Wn} Wp={Wp} L={L}
M1 out in gnd gnd CMOSN W={Wn} L={L}
M2 out in vdd vdd CMOSP W={Wp} L={L}
.ends inverter
Vdd vdd gnd 1.8
Vin A gnd PWL(0n 0V 0.5n 1.8V 1.1n 1.8V 1.5n 0V 5n 0V)
Xinv1 A  B vdd gnd inverter Wn={Wn}      Wp={Wp}      L={L}
Xinv2 B  C vdd gnd inverter Wn={4*Wn}    Wp={4*Wp}    L={L}
Xinv3 C  D vdd gnd inverter Wn={16*Wn}   Wp={16*Wp}   L={L}
Xinv4 D  E vdd gnd inverter Wn={64*Wn}   Wp={64*Wp}   L={L}
Xinv5 E  F vdd gnd inverter Wn={256*Wn}  Wp={256*Wp}  L={L}
Cload F gnd 1p
.control
tran 10p 5n
set curplottitle="mididoddisaipoojith-2025122010-4-B"
plot v(C) v(D)
meas tran trC TRIG v(C) VAL=0.18 RISE=1 TARG v(C) VAL=1.62 RISE=1
meas tran tfC TRIG v(C) VAL=1.62 FALL=1 TARG v(C) VAL=0.18 FALL=1
meas tran trD TRIG v(D) VAL=0.18 RISE=1 TARG v(D) VAL=1.62 RISE=1
meas tran tfD TRIG v(D) VAL=1.62 FALL=1 TARG v(D) VAL=0.18 FALL=1
print trC tfC trD tfD
.endc
.end
```

simulation data




```
trc  =  1.615056e-10
tfc  =  1.524097e-10
trd  =  1.865704e-10
tfd  =  1.671252e-10
ngspice 1 ->
```

The delays at node C and node D are not equal. The delay is proportional to the ratio C(ext)/C(in) . Since the effective external capacitance at node D is larger than that at node C, the delay observed at D is greater than the delay at C.

4-C

Netlist used

Q_4_c.spice

```
* FO4 Inverter Chain (measure propagation delays for I3 and I4)
.include TSMC_180nm.txt
.param Wn=1.8u
.param Wp={2.5*Wn}
.param L=0.18u
.subckt inverter in out vdd gnd Wn={Wn} Wp={Wp} L={L}
M1 out in gnd gnd CMOSN W={Wn} L={L}
M2 out in vdd vdd CMOSP W={Wp} L={L}
.ends inverter
Vdd vdd 0 1.8
Vin A 0 PWL(0n 0V 0.5n 1.8V 1.1n 1.8V 1.5n 0V 5n 0V)
Xinv1 A  B vdd 0 inverter Wn={Wn}       Wp={Wp}       L={L}
Xinv2 B  C vdd 0 inverter Wn={4*Wn}     Wp={4*Wp}     L={L}
Xinv3 C  D vdd 0 inverter Wn={16*Wn}    Wp={16*Wp}    L={L}
Xinv4 D  E vdd 0 inverter Wn={64*Wn}    Wp={64*Wp}    L={L}
Xinv5 E  F vdd 0 inverter Wn={256*Wn}   Wp={256*Wp}   L={L}
Cload F 0 1p
.control
tran 10p 5n
plot v(C) v(D)
meas tran tplh_i3 TRIG v(C) VAL=0.9 RISE=1 TARG v(D) VAL=0.9 RISE=1
meas tran tphl_i3 TRIG v(C) VAL=0.9 FALL=1 TARG v(D) VAL=0.9 FALL=1
meas tran tplh_i4 TRIG v(D) VAL=0.9 RISE=1 TARG v(E) VAL=0.9 RISE=1
meas tran tphl_i4 TRIG v(D) VAL=0.9 FALL=1 TARG v(E) VAL=0.9 FALL=1
let tpd_i3 =(tplh_i3 + tphl_i3)/2
let tpd_i4 =(tplh_i4 + tphl_i4)/2
print tpd_i3 tpd_i4
.endc
.end
```

simulation data

```
tpd_i3 = 1.045171e-10
tpd_i4 = 1.355980e-10
ngspice 1 ->
```

Inverter	t_{pd} (s)	t_{pd} (ns)
I3	1.045171×10^{-10}	0.105 ns
I4	1.355980×10^{-10}	0.136 ns

The propagation delays of inverters I3 and I4 are not the same. Inverter I3 shows a smaller delay compared to I4 because I3 is closer to the driving node and experiences less effective loading, while I4 sees additional capacitive loading and propagation through more stages. Since delay is proportional to the external load capacitance, the larger loading at node D4 increases its delay. Hence, tpd(I4) is greater than tpd(I3).

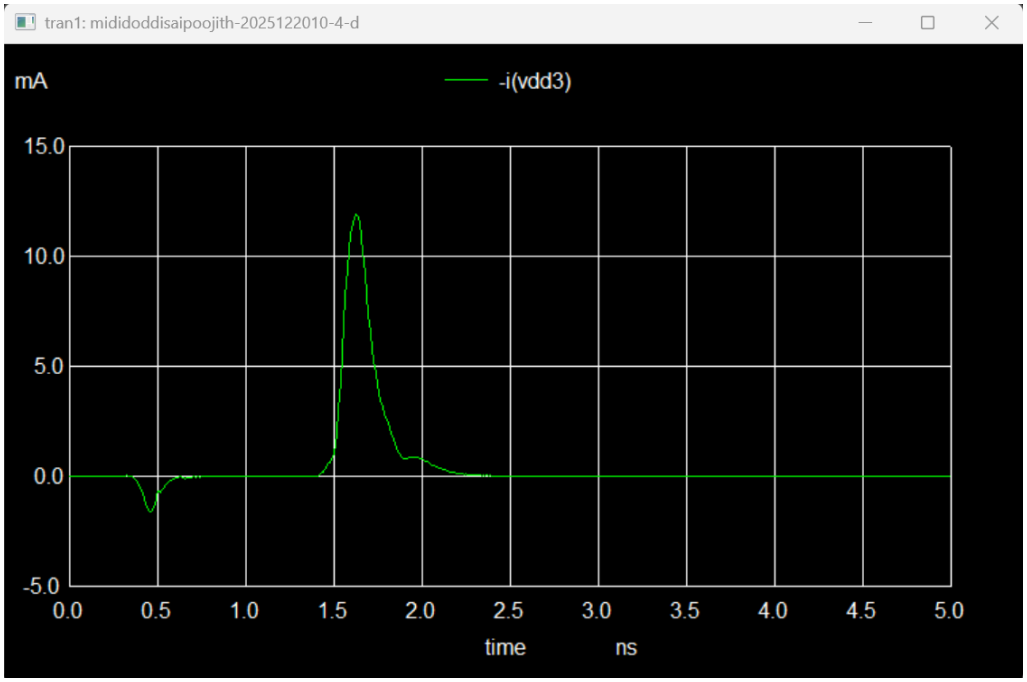
4-D

Netlist used

Q_4_d.spice

```
*CMOS Inverter Chain (IDD)
.include TSMC_180nm.txt
.param Wn=1.8u
.param Wp={2.5*Wn}
.param L=0.18u
.subckt inverter in out vdd vss Wn={Wn} Wp={Wp} L={L}
M1 out in vss vss CMOSN W={Wn} L={L}
M2 out in vdd vdd CMOSP W={Wp} L={L}
.ends inverter
Vdd vdd 0 1.8
Vin A 0 PWL(0n 0V 0.5n 1.8V 1.1n 1.8V 1.5n 0V 5n 0V)
Xinv1 A B vdd 0 inverter Wn={Wn} Wp={Wp} L={L}
Xinv2 B C vdd 0 inverter Wn={4*Wn} Wp={4*Wp} L={L}
VDD3 vdd3 0 1.8
VSS3 gnd3 0 0
Xinv3 C D vdd3 gnd3 inverter Wn={16*Wn} Wp={16*Wp} L={L}
Xinv4 D E vdd 0 inverter Wn={64*Wn} Wp={64*Wp} L={L}
Xinv5 E F vdd 0 inverter Wn={256*Wn} Wp={256*Wp} L={L}
Cload F 0 1p
.control
tran 10p 5n
set curplottitle="mididoddisaipoojith-2025122010-4-D"
plot -I(VDD3)
.endc
.end
```

simulation data



The supply current waveform of inverter I3 represents the dynamic current drawn from the source during switching. When the input switches, both the NMOS and PMOS conduct simultaneously for a short duration, creating a direct path from VDD to gnd. These effects result in a sharp positive current spike. Once the output reaches a stable logic level, the conduction path is cut off and the supply current drops back close to zero. A small negative dip is also observed in the waveform, which occurs because during certain transitions a portion of the charge stored in the output or parasitic capacitances flows back into the supply rail through the PMOS device.

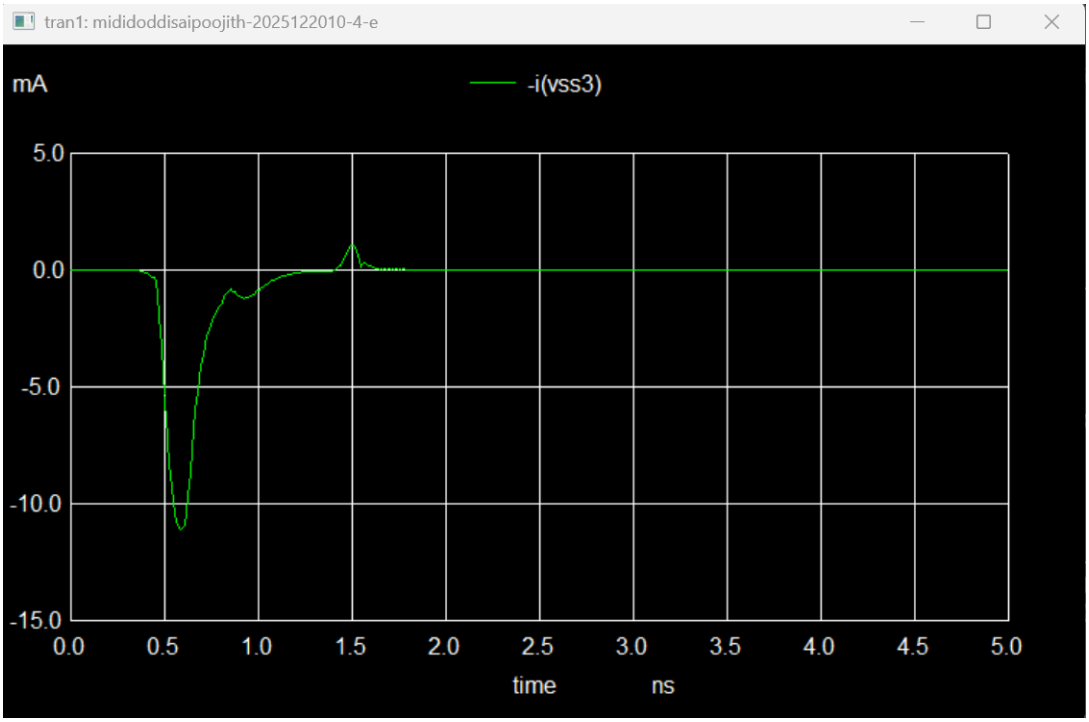
4-E

Netlist used

Q_4_e.spice

```
*CMOS Inverter Chain (ISS)
.include TSMC_180nm.txt
.param Wn=1.8u
.param Wp={2.5*Wn}
.param L=0.18u
.subckt inverter in out vdd vss Wn={Wn} Wp={Wp} L={L}
M1 out in vss vss CMOSN W={Wn} L={L}
M2 out in vdd vdd CMOSP W={Wp} L={L}
.ends inverter
Vdd vdd 0 1.8
Vin A 0 PWL(0n 0V 0.5n 1.8V 1.1n 1.8V 1.5n 0V 5n 0V)
Xinv1 A B vdd 0 inverter Wn={Wn} Wp={Wp} L={L}
Xinv2 B C vdd 0 inverter Wn={4*Wn} Wp={4*Wp} L={L}
VDD3 vdd3 0 1.8
VSS3 gnd3 0 0
Xinv3 C D vdd3 gnd3 inverter Wn={16*Wn} Wp={16*Wp} L={L}
Xinv4 D E vdd 0 inverter Wn={64*Wn} Wp={64*Wp} L={L}
Xinv5 E F vdd 0 inverter Wn={256*Wn} Wp={256*Wp} L={L}
Cload F 0 1p
.control
tran 10p 5n
set curplottitle="mididoddisaipoojith-2025122010-4-E"
plot -I(VSS3)
.endc
.end
```

simulation data



The ground current waveform of inverter I3 represents the transient current flowing into the ground during switching. When the input changes, the NMOS device conducts strongly, discharging the output node to ground and creating a sharp negative current spike (negative because current is defined entering the ground node). Once the output stabilizes, the direct discharge path is cut off and the current returns close to zero. A small positive bump is also seen, which arises from charge redistribution in the output and parasitic capacitances, where some stored charge flows back from the ground node.

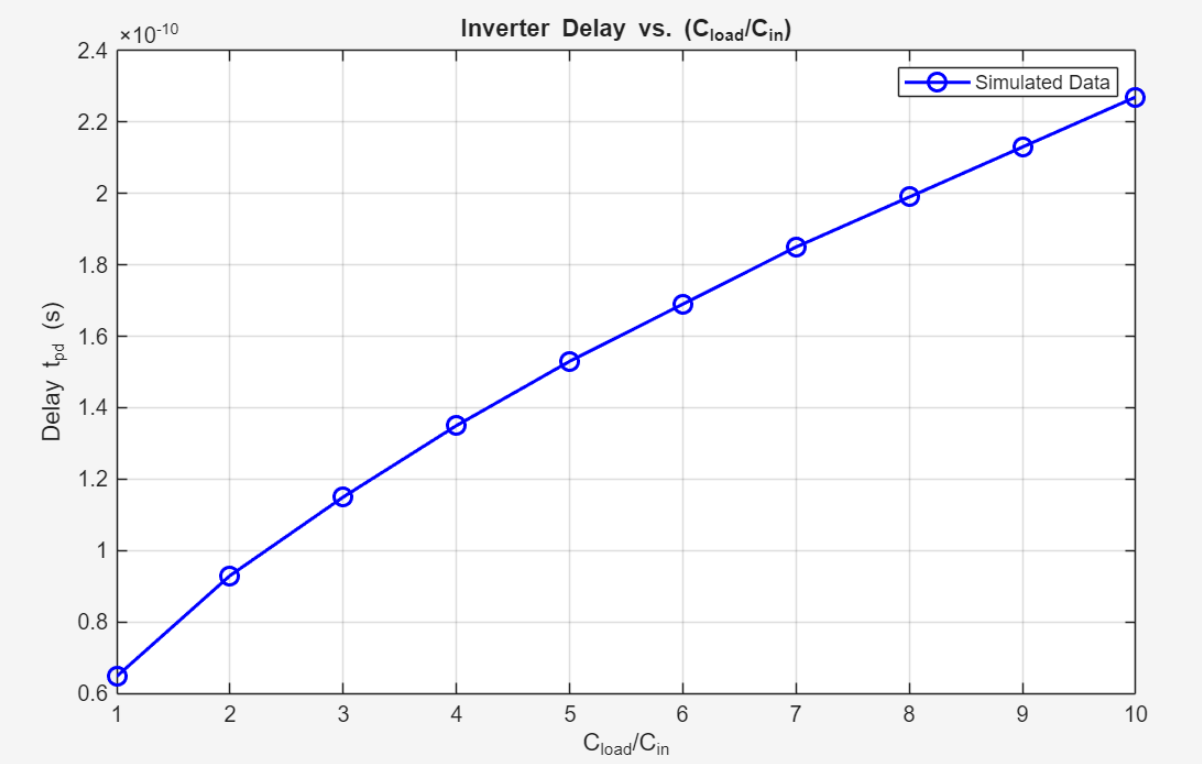
5

Netlist used

Q_5.spice

```
.include TSMC_180nm.txt
.param Wn=1.8u
.param Wp={2.5*Wn}
.param L=0.18u
.subckt inverter in out vdd gnd Wn={Wn} Wp={Wp} L={L}
M1 out in gnd gnd CMOSN W={Wn} L={L}
M2 out in vdd vdd CMOSP W={Wp} L={L}
.ends inverter
Vdd vdd 0 1.8
Vin A 0 PWL(0n 0V 0.5n 1.8V 1.1n 1.8V 1.5n 0V 5n 0V)
Xinv1 A B vdd 0 inverter Wn={Wn} Wp={Wp} L={L}
.param scale=1
Xinv2 B C vdd 0 inverter Wn={scale*Wn} Wp={scale*Wp} L={L}
.control
tran 10p 5n
meas tran tplh TRIG v(A) VAL=0.9 RISE=1 TARG v(B) VAL=0.9 RISE=1
meas tran tphl TRIG v(A) VAL=0.9 FALL=1 TARG v(B) VAL=0.9 FALL=1
let tpd =(tplh + tphl)/2
print tpd
.endc
.end
```

simulation data




```
Delay unit = 1.75e-11 s per unit Cload/Cin
absolute Parasitic delay = 5.92e-11 s
```

For delay characterization, the test circuit consists of two cascaded CMOS inverters. The first inverter acts as the device under test, and its output delay is measured with respect to its input. The second inverter is connected as a load, and its transistor widths are scaled to vary the effective load capacitance Cload, presented to the first inverter. Since the input capacitance of the first inverter, Cin , is fixed, the ratio Cload/Cin can be controlled by adjusting the scaling factor of the second inverter. A pulse input is applied to the first inverter to find the propagation delay. tpd is then obtained for each load condition. By plotting tpd versus Cload/Cin, the delay is verified to follow the logical effort form tpd=p+g.(Cload/Cin), where the intercept p represents the absolute parasitic delay of the inverter and the slope g corresponds to the delay unit.

6-A

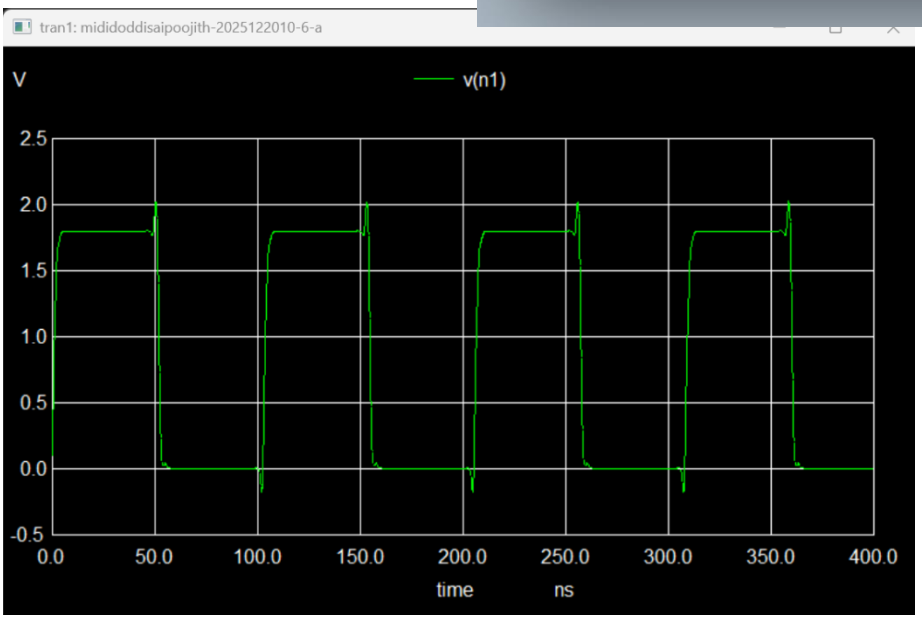
Netlist used

```
.include TSMC_180nm.txt
.param Wn = 10u
.param Wp = 25u
.param L  = 2u
.param VDD = 1.8
.global gnd
.subckt inverter in out vdd gnd Wn={Wn} Wp={Wp} L={L}
M1 out in gnd gnd CMOSN W={Wn} L={L}
M2 out in vdd vdd CMOSP W={Wp} L={L}
.ends inverter
Vdd vdd gnd {VDD}
X1  n1  n2  vdd gnd inverter Wn={Wn} Wp={Wp} L={L}
X2  n2  n3  vdd gnd inverter Wn={Wn} Wp={Wp} L={L}
X3  n3  n4  vdd gnd inverter Wn={Wn} Wp={Wp} L={L}
X4  n4  n5  vdd gnd inverter Wn={Wn} Wp={Wp} L={L}
X5  n5  n6  vdd gnd inverter Wn={Wn} Wp={Wp} L={L}
X6  n6  n7  vdd gnd inverter Wn={Wn} Wp={Wp} L={L}
X7  n7  n8  vdd gnd inverter Wn={Wn} Wp={Wp} L={L}
X8  n8  n9  vdd gnd inverter Wn={Wn} Wp={Wp} L={L}
X9  n9  n10 vdd gnd inverter Wn={Wn} Wp={Wp} L={L}
X10 n10 n11 vdd gnd inverter Wn={Wn} Wp={Wp} L={L}
X11 n11 n12 vdd gnd inverter Wn={Wn} Wp={Wp} L={L}
X12 n12 n13 vdd gnd inverter Wn={Wn} Wp={Wp} L={L}
X13 n13 n14 vdd gnd inverter Wn={Wn} Wp={Wp} L={L}
X14 n14 n15 vdd gnd inverter Wn={Wn} Wp={Wp} L={L}
X15 n15 n16 vdd gnd inverter Wn={Wn} Wp={Wp} L={L}
X16 n16 n17 vdd gnd inverter Wn={Wn} Wp={Wp} L={L}
X17 n17 n18 vdd gnd inverter Wn={Wn} Wp={Wp} L={L}
X18 n18 n19 vdd gnd inverter Wn={Wn} Wp={Wp} L={L}
X19 n19 n20 vdd gnd inverter Wn={Wn} Wp={Wp} L={L}
X20 n20 n21 vdd gnd inverter Wn={Wn} Wp={Wp} L={L}
X21 n21 n22 vdd gnd inverter Wn={Wn} Wp={Wp} L={L}
X22 n22 n23 vdd gnd inverter Wn={Wn} Wp={Wp} L={L}
X23 n23 n24 vdd gnd inverter Wn={Wn} Wp={Wp} L={L}
X24 n24 n25 vdd gnd inverter Wn={Wn} Wp={Wp} L={L}
X25 n25 n26 vdd gnd inverter Wn={Wn} Wp={Wp} L={L}
X26 n26 n27 vdd gnd inverter Wn={Wn} Wp={Wp} L={L}
X27 n27 n28 vdd gnd inverter Wn={Wn} Wp={Wp} L={L}
X28 n28 n29 vdd gnd inverter Wn={Wn} Wp={Wp} L={L}
X29 n29 n30 vdd gnd inverter Wn={Wn} Wp={Wp} L={L}
X30 n30 n31 vdd gnd inverter Wn={Wn} Wp={Wp} L={L}
X31 n31 n1  vdd gnd inverter Wn={Wn} Wp={Wp} L={L}
.ic V(n1)=0.1
.control
tran 0.1n 0.4u
set curplottitle="mididoddisaipoojith-2025122010-6-A"
plot v(n1)
meas tran Tperiod TRIG v(n1) VAL=0.9 RISE=2  TARG v(n1) VAL=0.9 RISE=
meas tran tpdHL TRIG v(n1) VAL=0.9 FALL=3 TARG v(n2) VAL=0.9 FALL=3
meas tran tpdLH TRIG v(n1) VAL=0.9 RISE=3 TARG v(n2) VAL=0.9 RISE=3
let Davg =((tpdHL+tpdLH)/2)
print Tperiod
print Davg
.endc
.end

```

simulation data

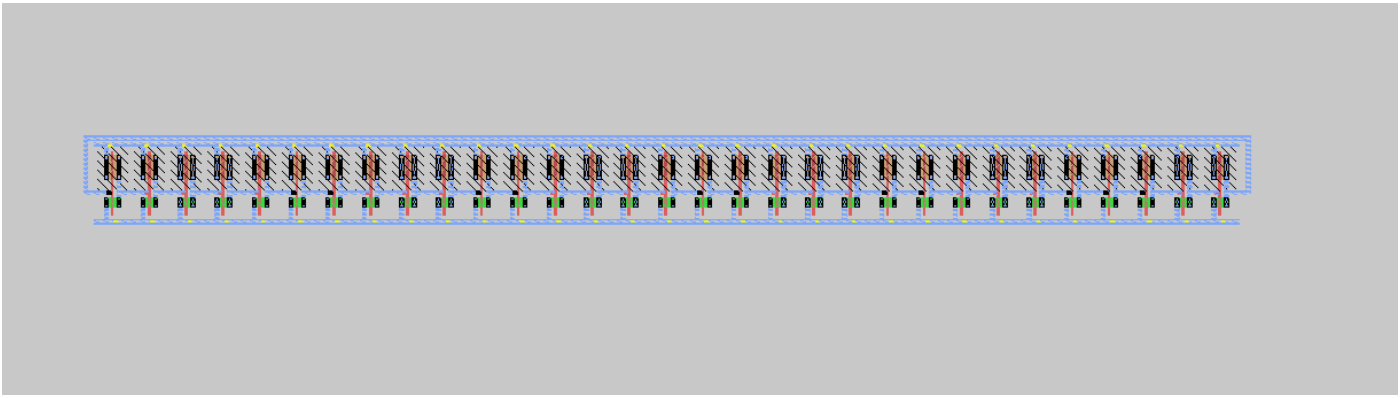
```
fro = 9.732265e+06
delay = 1.657195e-09
ngspice 1 ->
```

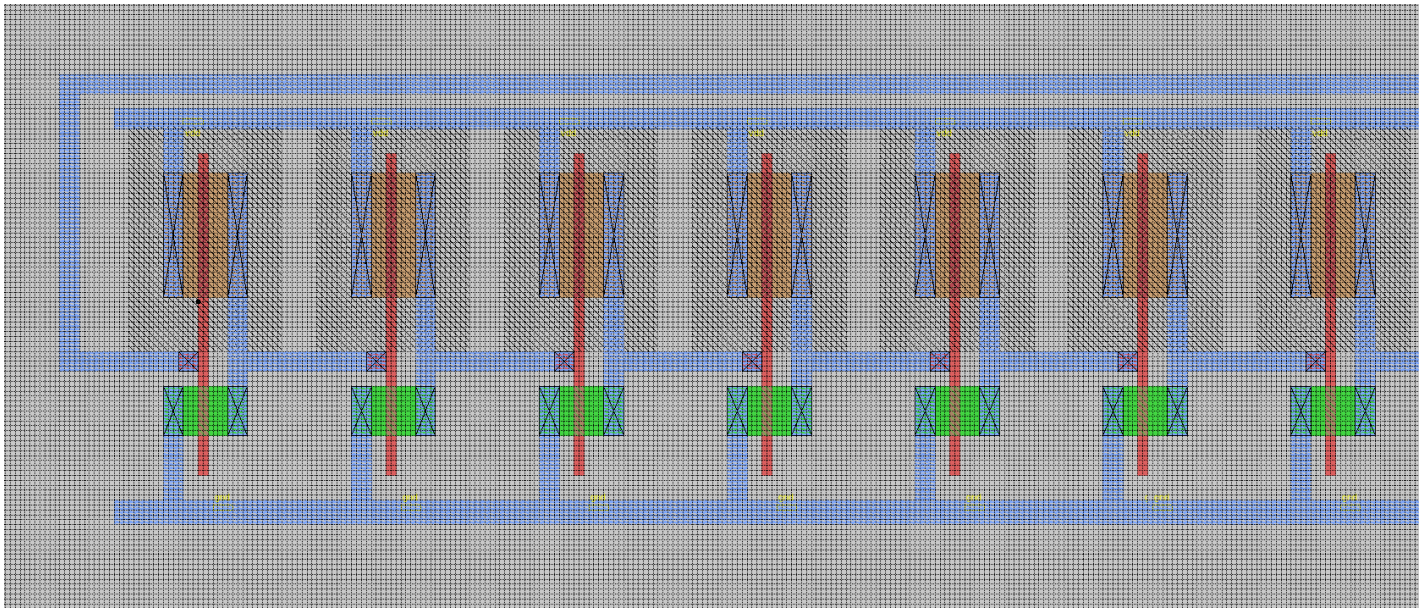


From the NGSPICE simulation, the delay obtained directly from inverter propagation delay measurement is approximately equal to T/62, where T is the oscillation period of the 31-stage ring oscillator. This confirms the theoretical relation fRO=1/(62D)

6-B

MAGIC layout





6-C

Extracted from magic

Ubuntu-24.04 > home > poojith > magic > inv_final.spice

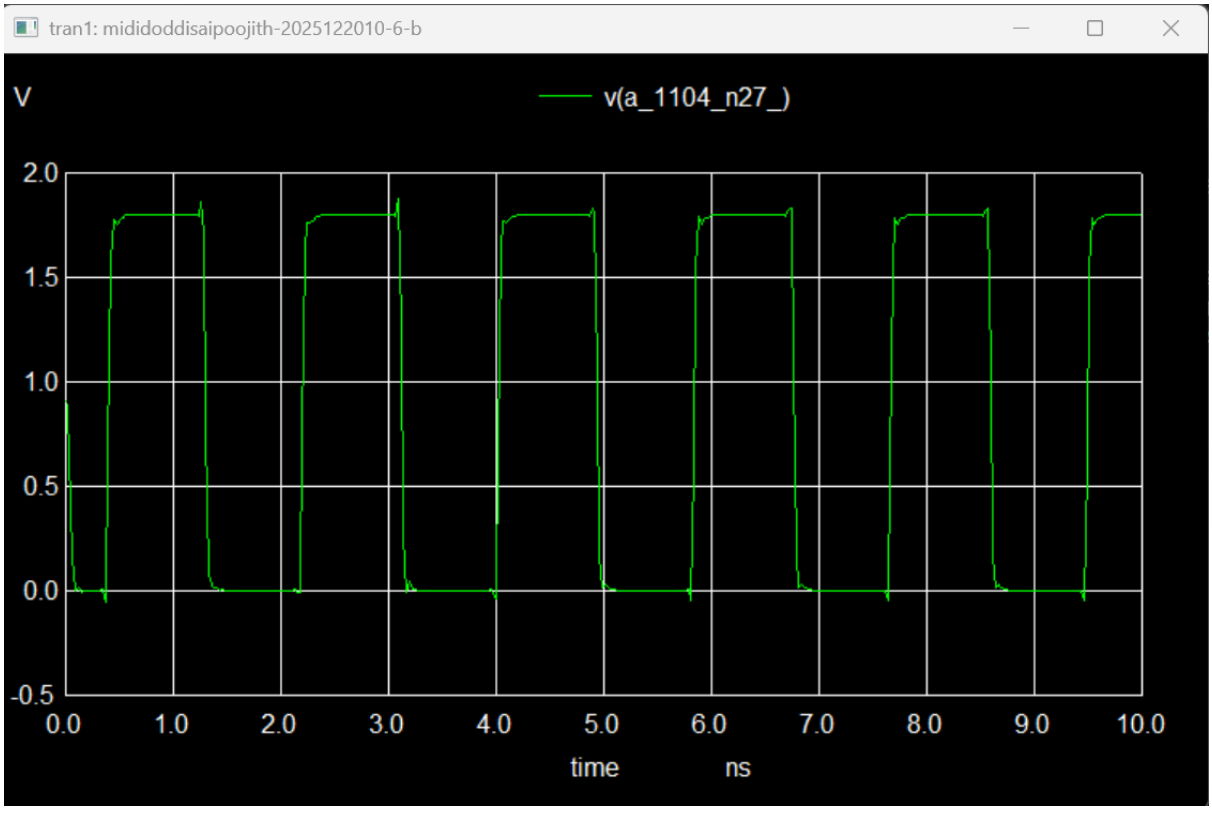
```
* SPICE3 file created from inv_final.ext - technology: scmos

.option scale=90n

M1000 a_458_n27# a_420_n27# vdd w_442_n10# pfet w=25 l=2
+  ad=0.2n pd=66u as=0.175n ps=64u
M1001 a_306_n27# a_268_n27# gnd Gnd nfet w=10 l=2
+  ad=80p pd=36u as=70p ps=34u
M1002 a_686_n27# a_648_n27# gnd Gnd nfet w=10 l=2
+  ad=80p pd=36u as=70p ps=34u
M1003 a_344_n27# a_306_n27# vdd w_328_n10# pfet w=25 l=2
+  ad=0.2n pd=66u as=0.175n ps=64u
M1004 a_838_n27# a_800_n27# gnd Gnd nfet w=10 l=2
+  ad=80p pd=36u as=70p ps=34u
M1005 a_230_n27# a_192_n27# vdd w_214_n10# pfet w=25 l=2
+  ad=0.2n pd=66u as=0.175n ps=64u
M1006 a_268_n27# a_230_n27# gnd Gnd nfet w=10 l=2
+  ad=80p pd=36u as=70p ps=34u
M1007 a_990_n27# a_952_n27# vdd w_974_n10# pfet w=25 l=2
+  ad=0.2n pd=66u as=0.175n ps=64u
M1008 a_420_n27# a_382_n27# gnd Gnd nfet w=10 l=2
+  ad=80p pd=36u as=70p ps=34u
M1009 a_40_n27# a_2_n27# vdd w_24_n10# pfet w=25 l=2
+  ad=0.2n pd=66u as=0.175n ps=64u
M1010 a_192_n27# a_154_n27# vdd w_176_n10# pfet w=25 l=2
+  ad=0.2n pd=66u as=0.175n ps=64u
M1011 a_116_n27# a_78_n27# vdd w_100_n10# pfet w=25 l=2
+  ad=0.2n pd=66u as=0.175n ps=64u
M1012 a_40_n27# a_2_n27# gnd Gnd nfet w=10 l=2
+  ad=80p pd=36u as=70p ps=34u
M1013 a_800_n27# a_762_n27# gnd Gnd nfet w=10 l=2
+  ad=80p pd=36u as=70p ps=34u
M1014 a_952_n27# a_914_n27# gnd Gnd nfet w=10 l=2
+  ad=80p pd=36u as=70p ps=34u
```

simulation data

```
fro = 6.202829e+06
delay = 2.600270e-09
ngspice 1 ->
```



6-D

pre-layout simulation results

```
fro = 9.732265e+06
delay = 1.657195e-09
ngspice 1 ->
```

post-layout simulation results

```
fro = 6.202829e+06
delay = 2.600270e-09
ngspice 1 ->
```

The post-layout simulation shows a difference compared to the pre-layout case. The delay of each inverter stage increases after layout due to the additional parasitic capacitances and resistances introduced by interconnects. As a result, the overall oscillation frequency of the ring oscillator decreases compared to the ideal schematic-based prediction.