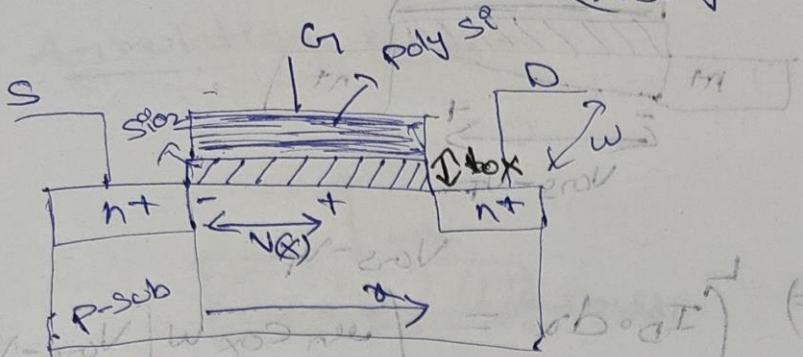


VLSI Design

(Assignment - 1)

②



The induced channel charge per unit area at point x is

$$Q_G = -C_{ox} [N_{DS} - N_G - N_T] \quad \left| C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \right.$$

$$(V - 2eV < 2eV) \quad I_D = -\mu_n \cdot Q_G \cdot W \quad \left| \begin{array}{l} \mu_n = -\frac{d\mu}{dV} \\ = \frac{d\mu}{dV} \end{array} \right.$$

$$\Rightarrow I_D = C_{ox} [N_{DS} - N_G - N_T] \cdot \frac{d\mu}{dV} \cdot W$$

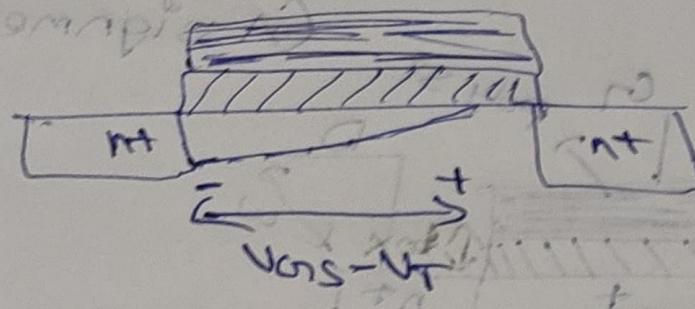
$$\left[\frac{dV}{dx} = \frac{1 + 2eV}{V - 2eV} \right] \frac{d\mu}{dV} = \frac{d\mu}{dx} \quad \left| \int I_D \cdot d\mu = \int \mu_n C_{ox} W [N_{DS} - N_G - N_T] d\mu \right.$$

$$I_{D,L} = \mu_n C_{ox} W \left[(N_{DS} - N_T) V_G - \frac{V_G^2}{2} \right] \Big|_0^L$$

$$\Rightarrow \boxed{I_D = \frac{\mu_n C_{ox} W}{L} \left[(N_{DS} - N_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right]}$$

(Intrinsic)
For $N_{DS} > N_T$
and $N_{DS} < N_{DS} - N_T$

For Saturation Region / 21 V



$$\Rightarrow \int_{0}^L I_D \cdot da = \int_0^L \sin \cos w [V_{05-N_1-N_2} - V_F]$$

$$I_{\text{sat}} = \frac{1}{2} \mu_0 n \cos \frac{\pi}{L} (N_{\text{tot}} - N_t)^2$$

For saturation mode = $(V_{DS} \geq V_{DS} - V_f)$

$$I_D = \frac{\mu_n C_{ox} W}{L} \left[(V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

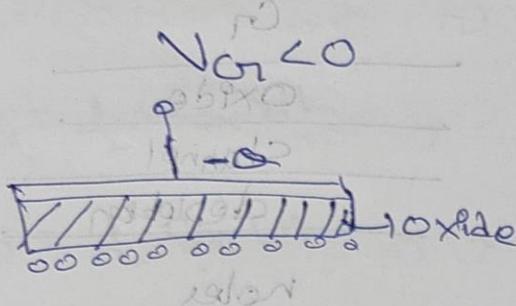
$$ID = \frac{1}{2} \mu n \cos \frac{\theta}{2} (N_{IS} - N_T)^2$$

$$V_{DS} \geq V_{DS} - V_T$$

Voszna

③ MOS capacitance

i) Accumulation mode



\rightarrow holes accumulate at the semiconductor oxide interface layer.

\Rightarrow Oxide and accumulated carriers form an electric double layer.

$$so \quad C \approx C_{ox}$$

$$\boxed{C_{ox}} \approx \frac{\text{Capacitance per unit area}}{\text{Area}}$$

ii) Depletion mode

$$0 < V_G < V_T$$

\rightarrow holes are repelled

\hookrightarrow depletion layers forming

$$C_{ox} = \frac{A}{d} \quad \text{and} \quad C_{dep} = \frac{A}{d} \cdot \epsilon_0 \cdot \frac{V - V_T}{d}$$

$$C = \frac{C_{ox} \cdot C_{dep}}{C_{ox} + C_{dep}}$$

\rightarrow It is less than accumulation

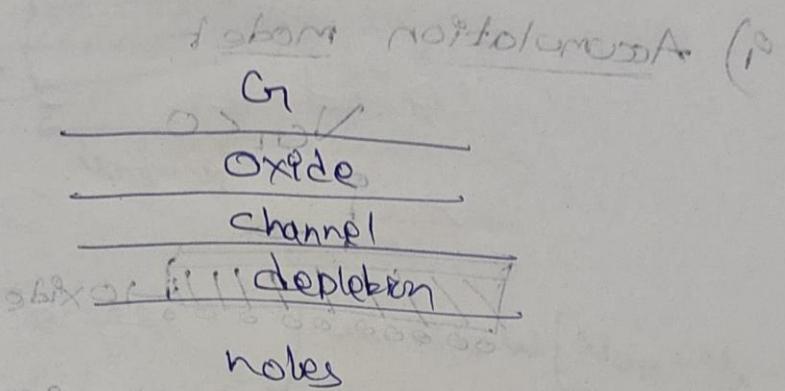
Capacitance

knows if enough

① Inversion Region

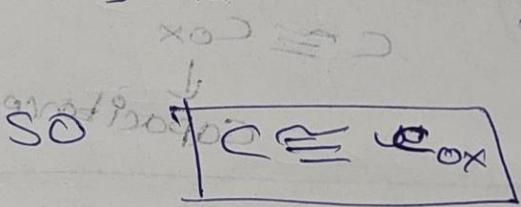
$$V_{GS} > V_{TH}$$

\Rightarrow



\rightarrow It is not series capacitor because

If we \uparrow V_{GS} \Rightarrow concentration of holes should inc. but concentration of holes are constant



① Cut-off ($V_{GS} < V_{TH}$)

\rightarrow No inversion channel is formed

$$C_{GS} \approx 0$$

$$C_{GD} \approx 0$$

C_{GB} = Smaller than C_{OX}

(C_{OX} Series with C_{dep})

$$C_{GB} \approx C_{OX}WL$$

$$\text{At } V_{GS} = V_{TH}$$

depletion layer width is max

So Capacitance is lowest.

② Linear $V_{DS} > V_{TH}$, $V_{DS} < V_{GS} - V_{TH}$ 4

↳ inversion channel exists from source to drain

$$C_{GS} = \frac{1}{2} C_{OX} WL$$

$$C_{GD} = \frac{1}{2} C_{OX} WL$$

$$C_{GB} = 0$$

③ Saturation r

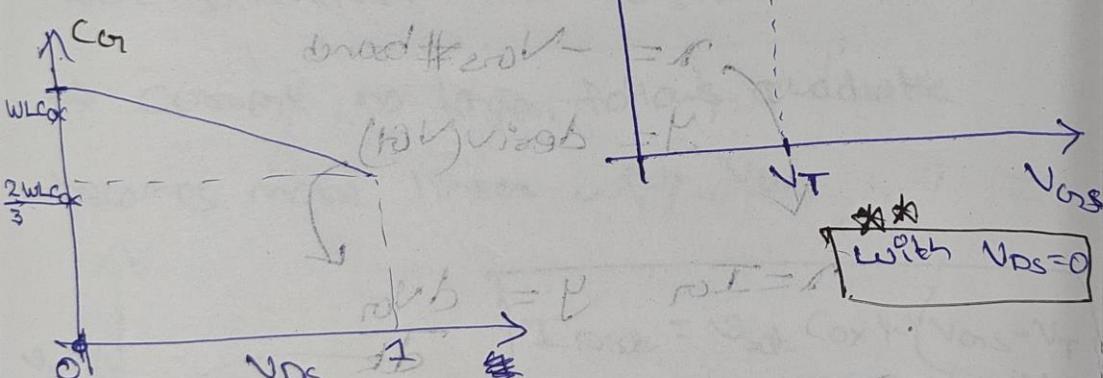
$V_{DS} > V_{TH} \therefore V_{DS} \geq V_{GS} - V_{TH}$

$$V_{DD} = 2.2V$$

$$C_{GS} \approx \frac{2}{3} C_{OX} WL$$

$$C_{GD} = 0$$

$$C_{GB} = 0$$



(C_{DS} as function degree of saturation)

(without overlap capacitance)

| | C_{GB} | C_{GS} | C_{GD} | C_{DS} |
|------------|------------|------------------------|------------------------|--------------------------|
| Cutoff | 0 | 0 | 0 | $COXWL + 2C_{OX}$ |
| Linear | $C_{OX}WL$ | $\frac{1}{2} C_{OX}WL$ | $\frac{1}{2} C_{OX}WL$ | $C_{OX}WL$ (with C_O) |
| Saturation | 0 | $\frac{2}{3} C_{OX}WL$ | 0 | $\frac{2}{3} C_{OX}WL$ |

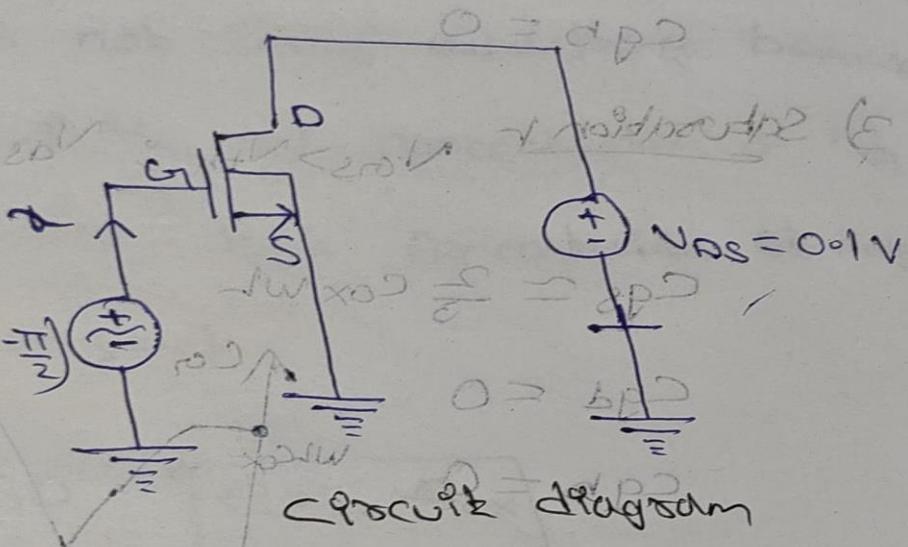
④

Circuit diagram from the net listing

$$\rightarrow V_{GS} \text{ or } \sin(0.108t) \text{ VDC } 0 \text{ - } 90^\circ$$

$$\rightarrow V_{DS} \text{ or } 0.108V = \text{exp}$$

$$\rightarrow M_1 \text{ or } \text{ground connection}$$



$$\alpha = I_{DS} \quad y = \frac{dN_{DS}}{dt}$$

$$C_{GS} = \left(\frac{I_{DS}}{\frac{dN_{DS}}{dt}} \right)$$

• branch 10 $400V \text{ to } 0V$

Plot C_{GS} vs V_{GS}

From this we will get gate capacitance C_{GS} with respect to V_{GS}

(3) (i) channel length modulation

→ In saturation I_D is not independent on V_{DS} .

$$XN_{DS} = \frac{\Delta L}{L}$$

→ effective channel length \downarrow

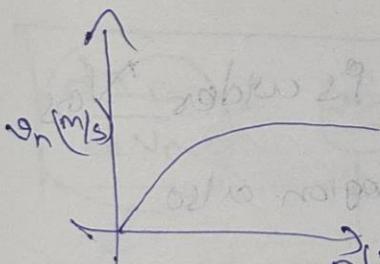
→ Drain current inc slightly with V_{DS} in saturation

$$I_D \approx \frac{1}{2} \mu_{eff} C_{ox} \frac{W}{L} (V_{DS} - V_T) (1 + \gamma V_{DS})$$

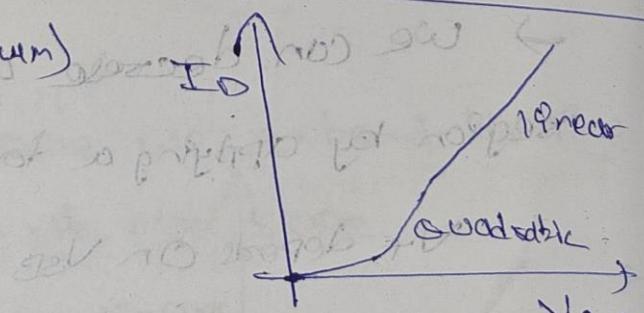
(ii) Velocity Saturation

→ For short channels carrier velocity no longer increases linearly with field but saturates at constant value

→ Current no longer follows quadratic becomes more linear with V_{DS}



$$I_{DSat} = V_{DSat} C_{ox} \frac{W}{L} (V_{DS} - V_T)$$



$$(V_{DS} - V_{DSat})^2 / L = T$$

(98) Mobility Degradation

- At high N_{DS} strong electric field rises closer to S_{DS} , surface toughness scatters by
- mobility increases with inc N_{DS}
- I_D is decreased

IV) drain induced barrier lowering

- In short channel MOSFETs high V_{DS} reduces V_T , making easier for carriers to enter channel
- inc leakage current in off state
- N_T decreases as V_{DS} increases

$$V_T' = V_T - b \cdot V_{DS}$$

V) Body Effect

- If depletion region is wider should fight with depletion region also.
- We can decrease width of depletion region by applying a forward bias b/w body and source
- V_T depends on V_{SB}

$$V_T = V_{To} + N \left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F} \right)$$

IV) Sub-threshold conduction \rightarrow ~~non-saturated~~

$V_{DS} < V_T \rightarrow$ carriers diffuse from source to drain

(a) $x_{DM-N} = x_{DM-N}$
 \rightarrow drain current decreases exponentially with V_{DS} . $I_{DS} = I_{DS0} \cdot e^{\frac{V_{DS}-V_T}{n \cdot V_{TH}}}$

points at threshold $\rightarrow 1.6V$

(b) I_D vs V_{DS} for $\frac{108\mu A}{0.48\mu A}$

$N_{DS} = 50mN \quad V_{DS} \rightarrow 0 - 1.08V$

\rightarrow This is in linear region.

$$I_D = \frac{4nCoxW}{L} \left[(V_{DS} - V_T) V_{DS} - \frac{1}{2} N_{DS}^2 \right]$$

For small V_{DS} $\Rightarrow N_{DS} \approx 0$

$$\Rightarrow N_{DS}^2 \approx 0$$

$$I_D = \frac{4nCoxW}{L} \left[(V_{DS} - V_T) V_{DS} - 0 \right]$$

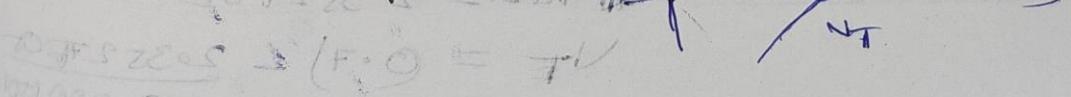
$$\frac{dI_D}{dV_{DS}} = \frac{4nCoxW V_{DS}}{L}$$

\rightarrow so at max slope we extend the line

* we draw tangent at max slope

\rightarrow where it touches x-axis

that is V_T



Calculation

$$m = \frac{dI_D}{dV_{DS}} \text{ at } V_{DS} = 0 \text{ V}$$

at the origin

$m_{\text{max}} = \text{maximum } (m)$

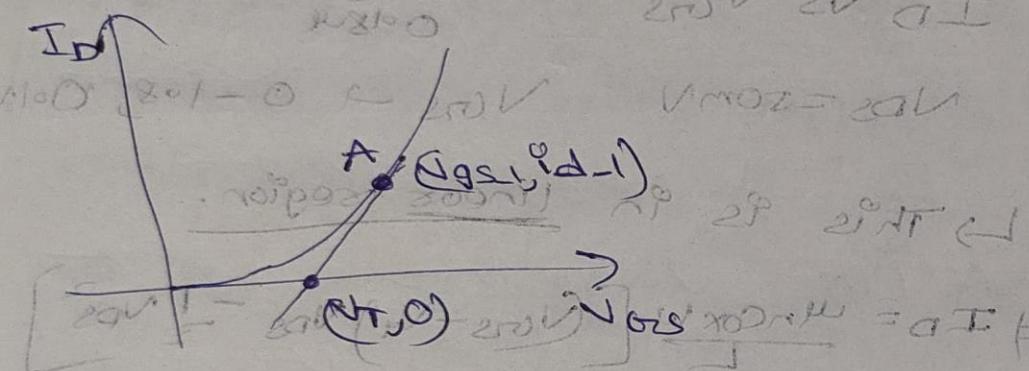
$$V_{GS-1} = \text{Voltage } V_G \text{ for } I_D = m_{\text{max}}$$

$V_{GS-1} = 0 \text{ V}$

$$I_D = 2.35278 \times 10^{-5} \text{ A} = m_{\text{max}}$$

$$I_{D-1} = \text{current } I_D \text{ when } m = m_{\text{max}}$$

$$\frac{m_{\text{max}}}{m_{\text{max}}} = 20 \text{ V} / 2 \text{ V} = 10$$



at point A we have

$$\text{slope} = m_{\text{max}}$$

and

$$A = (V_{GS-1}, I_{D-1})$$

From the eqn we get

$$\frac{I_{D-1} - 0}{V_{GS-1} - V_T} = m_{\text{max}}$$

$$\Rightarrow V_T = \left(V_{GS-1} \right) - \left(\frac{I_{D-1}}{m_{\text{max}}} \right)$$

From Simulations

$$\text{Slope} = m_{\text{max}} = 0.000150146$$

$$V_{GS-1} = 0.7 \text{ V}$$

$$I_{D-1} = 2.35278 \times 10^{-5} \text{ A}$$

$$V_T = 0.7 - \frac{2.35278 \times 10^{-5}}{0.000150146}$$

$$V_T = 0.5433V$$

b) $N_{DS} = 108$

V_{NDS} is swept from 0 to 108V

$$V_{ZD00} = V_{MOS} = 20V \quad \text{Step} - 0.1V$$

It is linear saturation mode

$$I_D = \frac{1}{2} \mu n C_{ox} \frac{W}{L} (N_{DS} - V_T)^2$$

$$\sqrt{I_D} = \sqrt{\frac{1}{2} \mu n C_{ox} \frac{W}{L} (N_{DS} - V_T)^2}$$

$$\sqrt{I_D} = k(N_{DS} - V_T)$$

With a straight line

→ with slope of this line extrapolate back to the x-axis

$$V_T = V_{DSI} - \frac{\sqrt{I_D}}{\text{slope}}$$

From simulation

2 points I took to find slope

$$(0.6, Y_1) \quad (0.8, Y_2) \quad (Y_1, Y_2 \text{ can be found})$$

$$\text{slope} = \frac{Y_2 - Y_1}{0.8 - 0.6}$$

$$V_{DSI} = \text{at } V_{DS} = 0 \text{ V}$$

$$V_{th} = 0.8 - \frac{Y_2}{\text{slope}}$$

$$V_{th} = 0.445V$$

③ There is difference in V_T in case A and case B.

$$80V = 20V$$

→ Case A

~~VS = 0.05V~~ and $V_{DS} = 29$ V

$$V_{DS} = 50mV = 0.05V$$

→ So because of small N_{DS} there

is no DIBL in case A

Case B ~~will fail~~

$$\hookrightarrow V_{DS} = 1.08V$$

→ Because of large V_{DS} DIBL will be there in case B

DIBL

With a large drain bias, the drain's electric field pulls down source-channel separation.

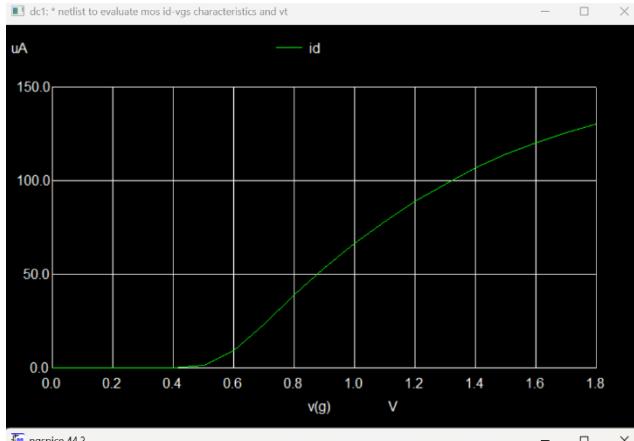
$$V_T = V_{TO} - k V_{DS}$$

(for $N_{DS} > 1$) (for $N_{DS} < 1$) $k = \frac{1}{N_{DS} + \text{DIBL coefficient}}$

$$V_T \text{ for } N_{DS} = 50mV$$

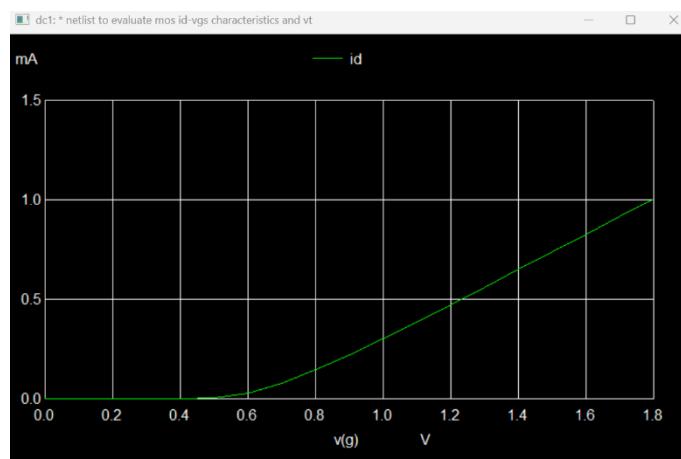
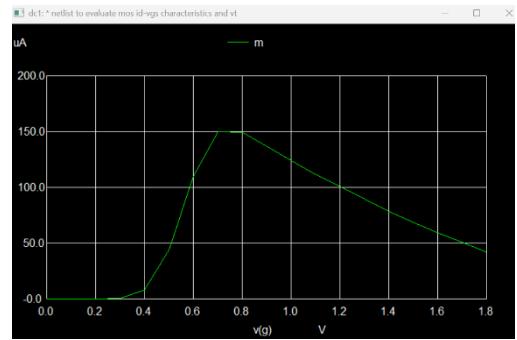
$$> V_T \text{ for } N_{DS} = 1.08V$$

$$V_T \text{ for } N_{DS} = 1.08V \rightarrow \text{because of DIBL}$$



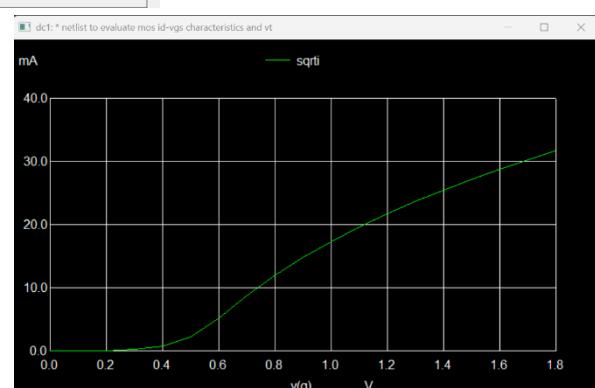
```
ngspice 44.2
Circuit: * netlist to evaluate mos id-vgs characteristics and vt
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
Using SPARSE 1.3 as Direct Linear Solver
No. of Data Rows : 19
n_max           = 1.501457e-04 at= 7.000000e-01
vgs_1            = 6.999999e-01
id_1             = 2.352776e-05
vt = 5.433004e-01
ngspice 1 ->
```

6-A



```
ngspice 44.2
Circuit: * netlist to evaluate mos id-vgs characteristics and vt
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
Using SPARSE 1.3 as Direct Linear Solver
No. of Data Rows : 19
y1               = 5.233036e-03
y2               = 1.202433e-02
vth = 4.458899e-01
ngspice 1 ->
```

6-B



7 Let $V_{DS} = V_{DS(LOOP)} = 20V$ $20V$ (g)

$$V_{DS} = 0.05V$$

For linear region $V_{DS} = (0, 1.08V, 0.1V)$ $1.08V$ $0.1V$

For saturation region $V_{DS} = 1.08V$ $1.08V$

(9) $V_{BS} = 0V$ $20V$ $0.05V$ $1.08V$ $0.1V$

$\rightarrow I_D$ took m_{DS} to be in linear region

For calculating m_{COX} and V_T .

$$\Rightarrow \tilde{V_{DS}} \approx 0$$

$$\Rightarrow I_D = m_{COX} \frac{W}{L} ((V_{DS} - V_T) V_{DS})$$

$$m = \frac{\partial I_D}{\partial V_{DS}} = m_{COX} \frac{W}{L} \cdot V_{DS}$$

max for least distribution

$$\Rightarrow m_{COX} = \frac{(m)_{\text{max}} \cdot L}{V_{DS}}$$

$$V_T = V_{DS} \left(\text{at } m_{\text{max}} \right) - \frac{I_D \left(\text{at } m_{\text{max}} \right)}{m_{\text{max}}}$$

From simulation

I got

$$V_T = 0.543V$$

$$m_{COX} = 3.00 \times 10^{-4}$$

Q9) $V_{BS} = 0.9V$ $V_{DSS} = 20V$ $I_D = 2A$

For this case to find N_T , μ_{COX}
I took mosfet to be in saturation

$$I_D = \frac{1}{2} \mu_{COX} \frac{W}{L} (V_{DS} - V_T)^2$$

$$I_D = \frac{1}{2} \mu_{COX} \frac{W}{L} \cdot (V_{DS} - V_T)$$

$$\sqrt{I_D} = k \cdot (V_{DS} - V_T)$$

With the slope of line k we can extrapolate back to x-axis to find V_T .

$$\text{and } k = \sqrt{\frac{1}{2} \mu_{COX} \frac{W}{L}}$$

$$\begin{aligned} N_T &= V_{DS} - \frac{\sqrt{I_D}}{\text{slope}} \\ \mu_{COX} &= \frac{2 \times (\text{slope})^2 \times L}{W} \end{aligned}$$

$$\text{I got } V_T = 0.367V$$

$$\mu_{COX} = \frac{1.55 \times 10^{-2}}{9.75 \times 10^{-5}}$$

(Q9) $V_{BS} = -0.9V$

Again for this case I took mosfet in linear region so

$$\mu_{COX} = \frac{(m)_{\max}}{V_{DS}} \cdot \frac{L}{W}$$

$$N_T = V_{DS} \text{ (at max m)} - \frac{I_D \text{ (at max m)}}{(m)_{\max}}$$

$$N_T = 0.740V$$

$$\mu_{COX} = 2.086 \times 10^{-4}$$

→ For $V_{BS} = 0.9V$ B to S $V_{DS} \approx 0.9V$ in forward bias
 so N_T decreased. and for $V_{BS} = -0.9V$
 N_T is in reverse bias so N_T inc.

Due to Body effect

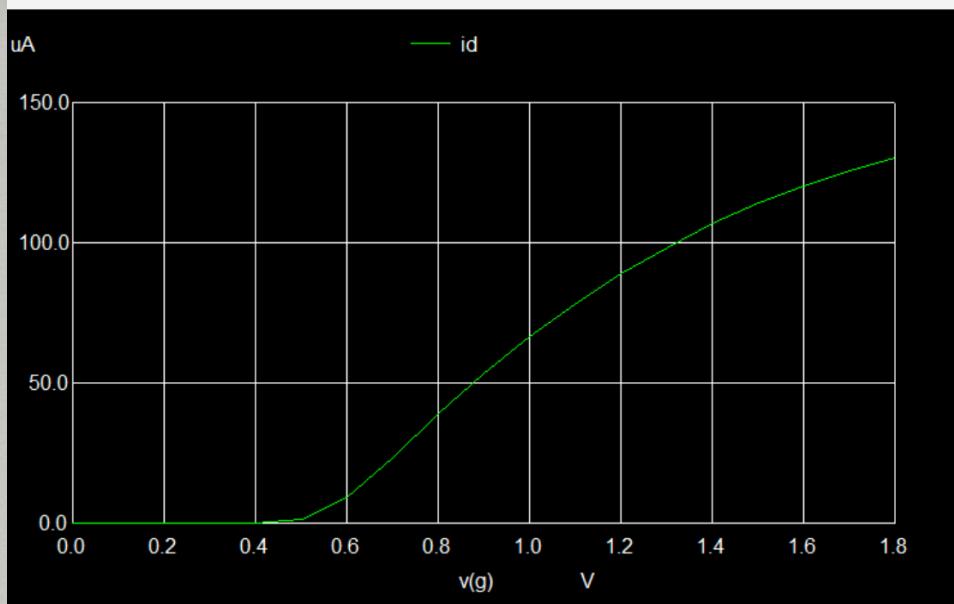
$$(N_T)_{V_{BS}=0.9V} < (N_T)_{V_{BS}=0}$$

$$< (N_T)_{V_{BS}=-0.9V}$$

$$(r_V - 2nV) \frac{w}{L} x_{COX} I = dI$$

7-A

dc1: * netlist to evaluate mos ucox and vt



ngspice 44.2

Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

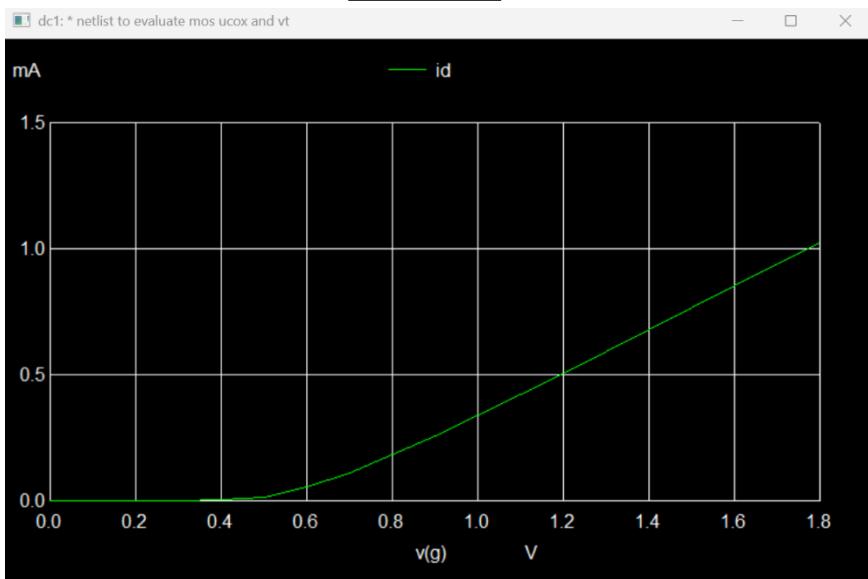
Using SPARSE 1.3 as Direct Linear Solver

```
No. of Data Rows : 19
u_max           = 1.501457e-04 at= 7.000000e-01
vgs_1           = 6.999999e-01
id_1            = 2.352776e-05
vt              = 5.433004e-01
ucox            = 3.002914e-04
ngspice 1 ->
```

$$V_{DS} + F_0 = r_V$$

$$F_0 \times 10^{-2} = x_{COX}$$

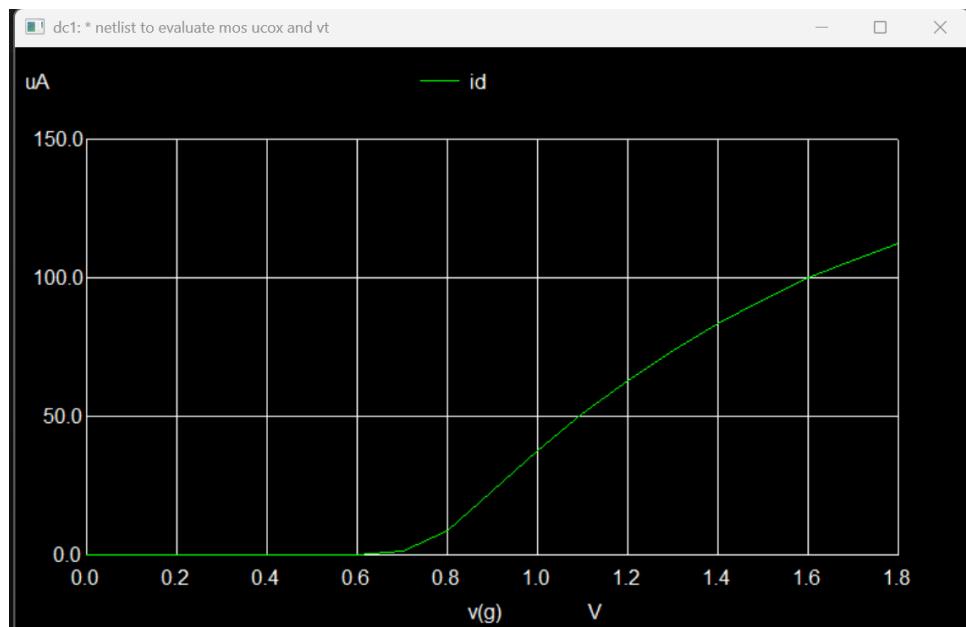
7-B



ngspice 44.2

```
Circuit: * netlist to evaluate mos ucox and vt
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
Using SPARSE 1.3 as Direct Linear Solver
No. of Data Rows : 19
y1 = 7.267378e-03
y2 = 1.351473e-02
vth = 3.673453e-01
ucox = 9.757352e-05
ngspice 1 ->
```

7-C



ngspice 44.2

```
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
Using SPARSE 1.3 as Direct Linear Solver
No. of Data Rows : 19
m_max = 1.431153e-04 at= 9.000000e-01
vgs_1 = 8.999999e-01
id_1 = 2.276835e-05
vt = 7.409089e-01
ucox = 2.862306e-04
ngspice 1 ->
```

⑧ Case (i) \rightarrow 2 $\frac{W}{L}$ transistors in series

Case (ii) \rightarrow single $\frac{Wb}{2L}$ transistor.

ideally,

case (i) \rightarrow 2 $\frac{W}{L}$ transistors in series
with respect to V_{DS}

(Effective channel length $\approx 2L$)

So should behave like single mosfet ($\frac{W}{2L}$)

But due to second order effects both has

I_{DSS} & V_{GS} different in two cases

(i) Channel-length modulation \downarrow

Each transistor in series experiences pinch-off individually, affecting the current differently from single longer transistor.

\rightarrow Each series transistor has full width w , so the series combination carries more current than a single $\frac{W}{2L}$ transistor.

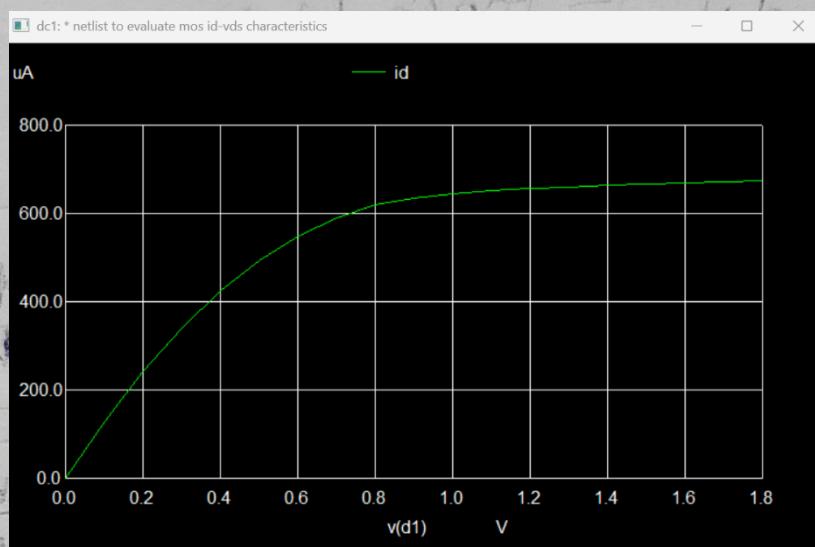
Also

⑨ DIBI \rightarrow shock channel devices show

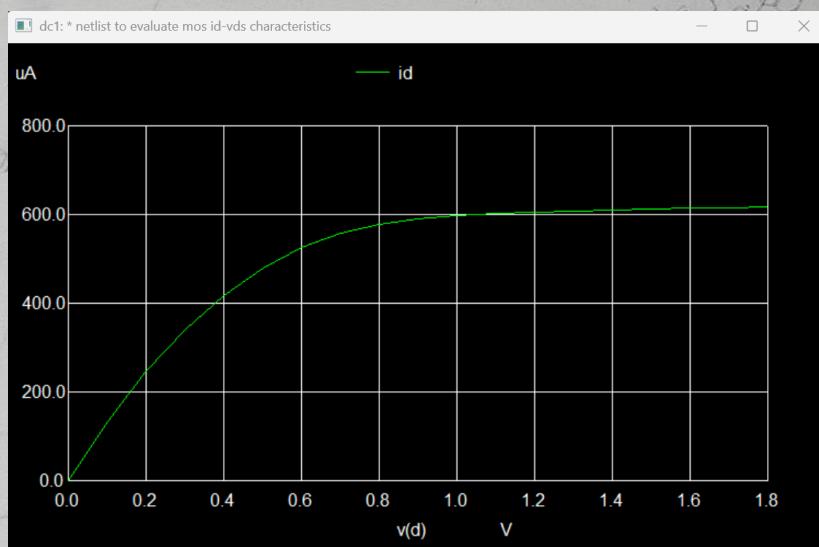
drain voltage influence, 2 series transistors distribute this differently.

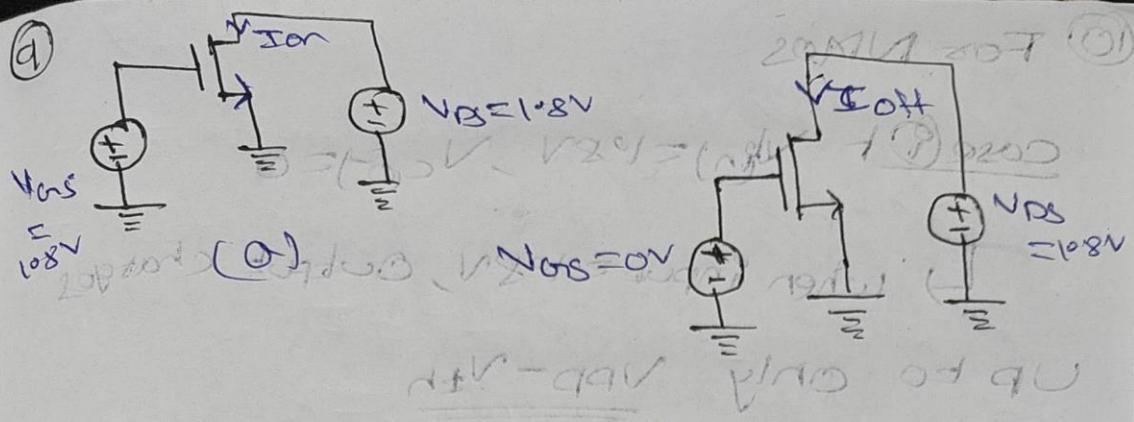
The series combination of two $\frac{w}{L}$ transistors shows different drain current than single $\frac{w}{2L}$ transistor for small values of V

8-A



8-B





→ For ideal case, $\frac{dI}{dt}$ or load current ID is directly proportional to $\frac{w}{L}$.

SO both Ion, Ioff Scale nearly
with w

↳ But practically due to second order effects

such as DIBL, mobility degradation, velocity saturation (no) and ηE does not vary linearly.

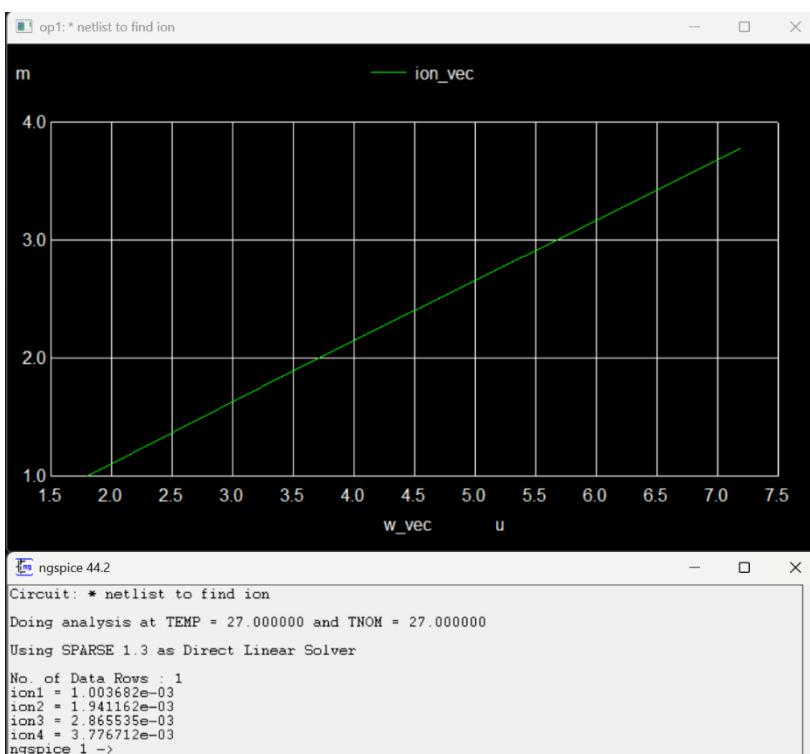
→ I_{ON}, I_{OFF} show approximate linear dependence on W_0 . 18/13/2020 → 10/2020

```
[nspice] nspice 44.2
Circuit: * netlist to find ion
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
Using SPARSE 1.3 as Direct Linear Solver
No. of Data Rows : 1
ion1 = 1.003682e-03
ion2 = 1.941162e-03
ion3 = 2.885535e-03
ion4 = 3.776712e-03
ion5 = 1.000000e+00
```

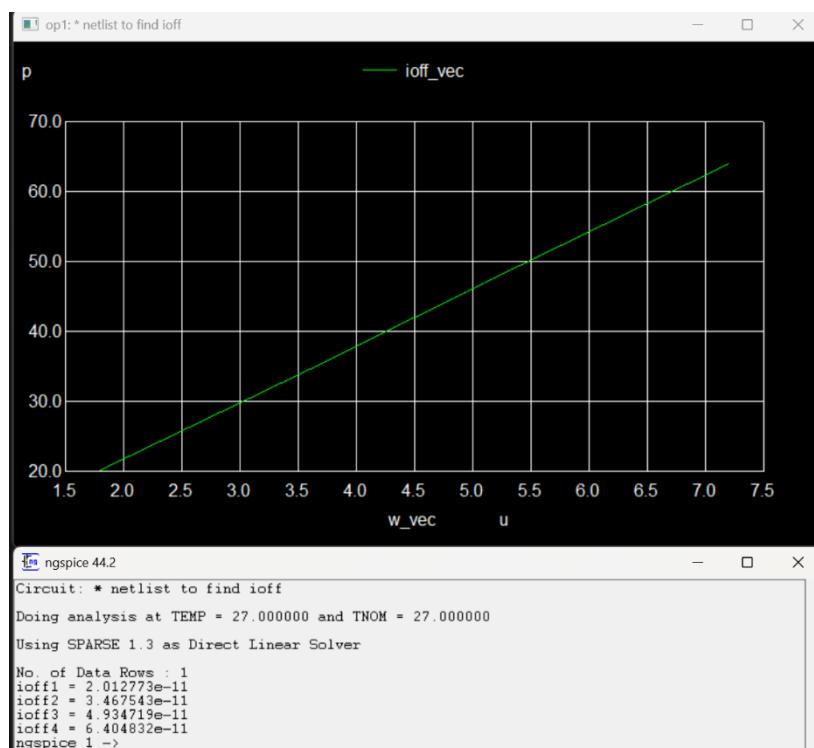
1975-01-14 1000
to most 1977

```
[ngspice] ngs spice 4.4.2
Circuit: * netlist to find ioff
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
Using SPARSE 1.3 as Direct Linear Solver
No. of Data Rows : 1
ioff1 = 2.012773e-11
ioff2 = 3.465543e-11
ioff3 = 4.934719e-11
ioff4 = 6.404832e-11
ngspice 1 ->
```

9-A



9-B



⑩ For NMOS

case (i) If $V_{in} = 1.8V$, $V_{c(0)} = 0$

↳ when input $= 1.8V$, output charged

up to only $V_{pp} - V_{th}$

↳ because $V_{out} \approx V_{in} - V_{th}$

$N_g's \approx N_{th}$ NMOS turn off

Case (ii) If $V_{in} = 0$, $V_{c(0)} = 1.8V$ (no further charging)

→ NMOS pulls the output capacitor node to ON

↳ Output matches Input (0V)

For PMOS

case (i) If $V_{in} = 1.8V$, $V_{c(0)} = 0$

↳ output charges fully to $1.8V$

case (ii) $V_{in} = 0$, $V_{c(0)} = 1.8V$

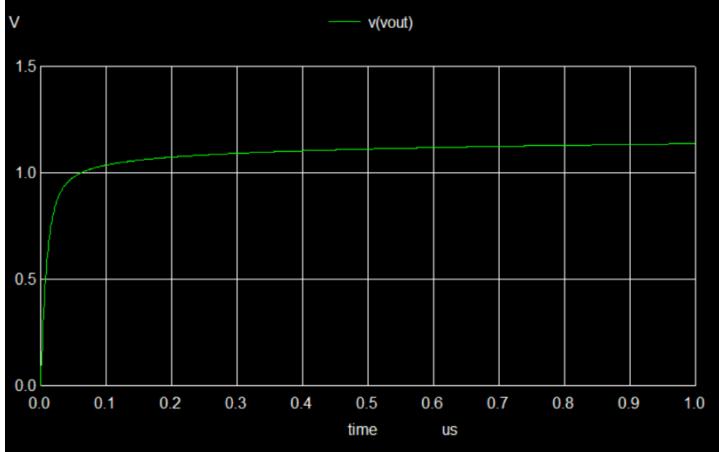
↳ It pulls the output only down to V_{th}

$V_{out} \approx V_{th}$, $N_g \approx N_{th}$

PMOS turns off

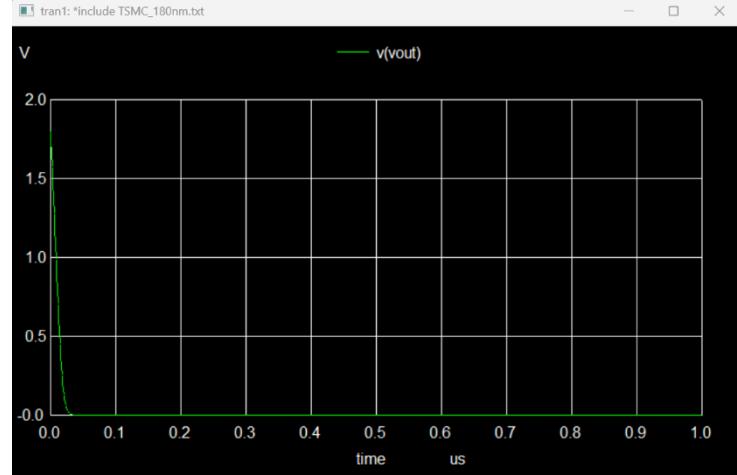
so output stops at V_{th}

tran1: *include TSMC_180nm.txt



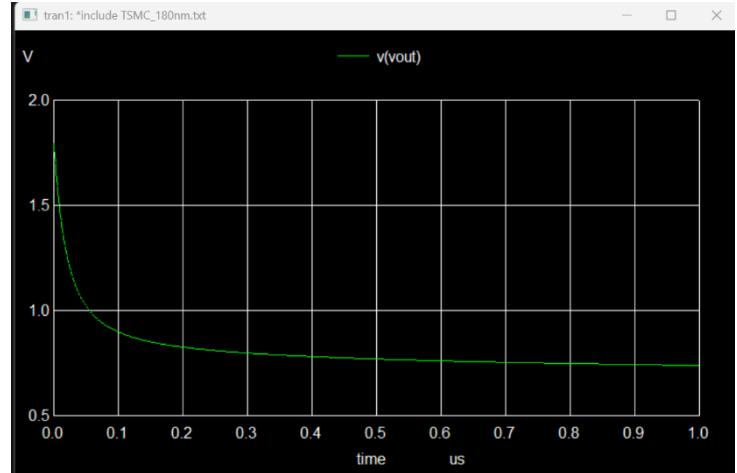
10-A

tran1: *include TSMC_180nm.txt



10-B

tran1: *include TSMC_180nm.txt



⑪ Effect of Transistor width on propagation delay

↳ Propagation delay (t_{pd}) mainly determined by how quickly the transistors can charge and discharge the load capacitors.

$$t_{pd} \approx \frac{C_L \cdot V_{DD}}{I_{drive}}$$

$$I_d \propto \frac{W}{L}$$

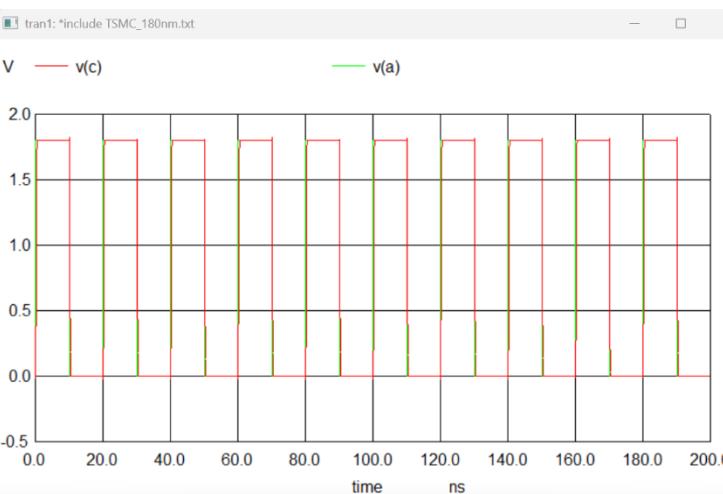
\Rightarrow Thus increasing the transistor widths inc the current \Rightarrow reduces the propagation delay for a given load capacitor.

\rightarrow For small transistor widths, the current drive is weaker, so takes longer to charge/discharge.

\rightarrow For large transistor widths current inc reducing rats, fall time \Rightarrow lowers t_{pd} .

* Scaling up W reduces delay significantly when capacitance is high.

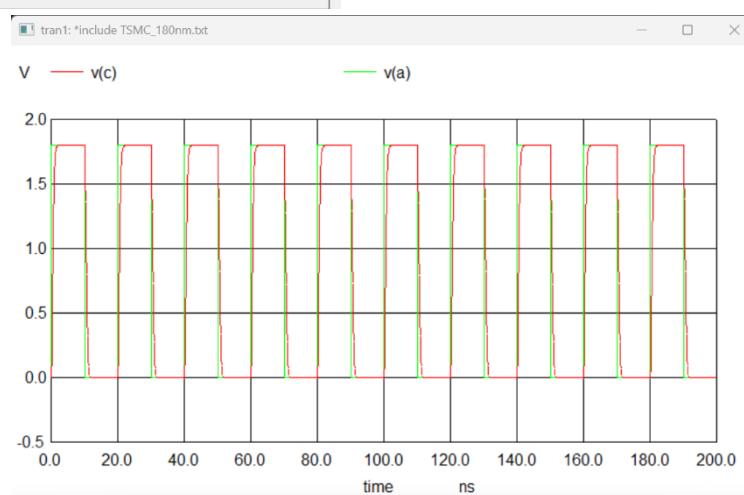
| Case | C_L (fF) | W_n (μm) | W_p (μm) | t_{pdR} (ps) | t_{pdf} (ps) | t_{pd} (ps) |
|------|------------|-------------------|-------------------|----------------|----------------|---------------|
| (a) | 100 | 1.8 | 4.5 | 163.94 | 176.4 | 170.17 |
| (b) | 500 | 1.8 | 4.5 | 486.73 | 544.65 | 515.62 |
| (c) | 500 | 9 | 22.5 | 174.1 | 186.05 | 180 |



11-A

ngspice 44.2

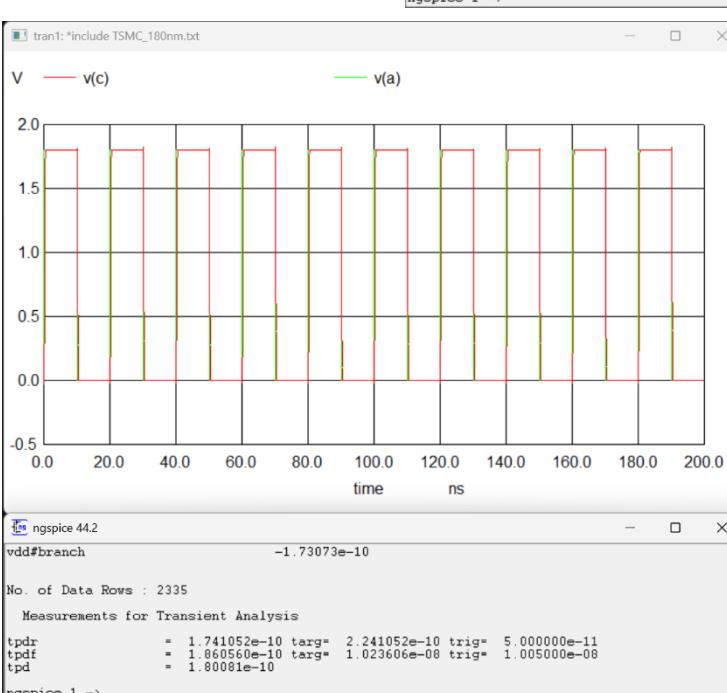
```
vdd#branch -4.16064e-11
No. of Data Rows : 2226
Measurements for Transient Analysis
tpdr = 1.639420e-10 targ= 2.139420e-10 trig= 5.000000e-11
tpdf = 1.764032e-10 targ= 1.022640e-08 trig= 1.005000e-08
tpd = 1.70173e-10
ngspice 1 ->
```



11-B

ngspice 44.2

```
vdd#branch -4.16064e-11
No. of Data Rows : 2213
Measurements for Transient Analysis
tpdr = 4.867300e-10 targ= 5.367300e-10 trig= 5.000000e-11
tpdf = 5.446545e-10 targ= 1.059465e-08 trig= 1.005000e-08
tpd = 5.15692e-10
ngspice 1 ->
```



11-C