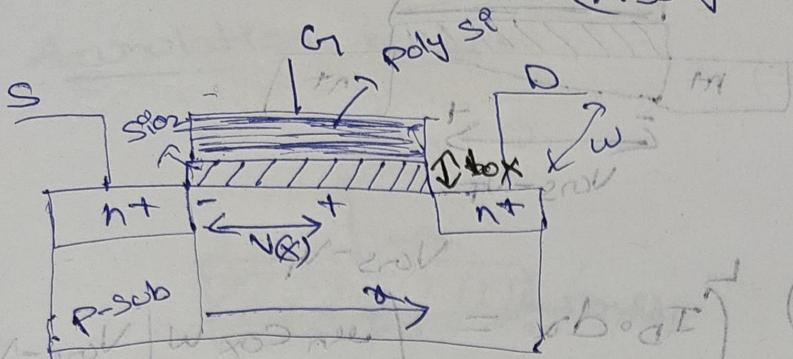


# VLSI Design

## (Assignment - 1)

②



The induced channel charge per unit area at point  $x$  is

$$Q_G = -C_{ox} [N_{DS} - N_G - N_T] \quad \left| C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \right.$$

$$I_D = -\mu_n C_{ox} W [N_{DS} - N_G - N_T] \quad \left| \begin{aligned} \mu_n &= \mu_n E_A \\ &= \frac{dI}{dV} \end{aligned} \right.$$

$$\Rightarrow I_D = C_{ox} [N_{DS} - N_G - N_T] \cdot \frac{dI}{dV} \cdot W$$

$$\int_{V_{DS}=0}^{V_{DS}=2AV} I_D \cdot dV = \mu_n C_{ox} W [N_{DS} - N_G - N_T] \cdot W \cdot \frac{dI}{dV} \cdot V_{DS} \quad \left| \begin{aligned} V_{DS} &\leq 2AV \\ V_{DS} &> 0 \end{aligned} \right.$$

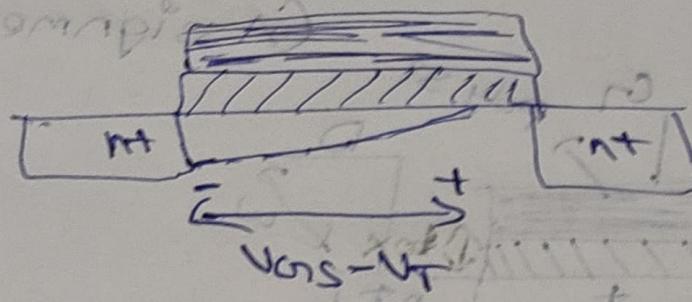
$$I_D = \mu_n C_{ox} W \left[ (N_{DS} - N_T) N_G - \frac{V_{DS}^2}{2} \right] \quad \left| \begin{aligned} V_{DS} &\leq 2AV \\ V_{DS} &> 0 \end{aligned} \right.$$

$$\Rightarrow I_D = \frac{\mu_n C_{ox} W}{L} \left[ (N_{DS} - N_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \quad \left| \begin{aligned} V_{DS} &\leq 2AV \\ V_{DS} &> 0 \end{aligned} \right.$$

(Intrinsic)  
For  $N_{DS} > N_T$   
and  $N_{DS} < N_{DS} - N_T$

For Saturation Region / 2 J V

(D - Thompson)



$$\Rightarrow \int_{0}^{VDS - VT} ID \cdot dx = \mu n C_{ox} W [VDS - VT - V_T]$$

$$[ \Rightarrow ] I_{DSat} = \frac{1}{2} \mu n C_{ox} \frac{W}{L} (VDS - VT)^2$$

For Saturation mode = ( $V_{DS} \geq V_{DS} - V_T$ )

$$v_{DS} =$$

$$I_D = \frac{\mu n C_{ox} W}{L} [(V_{DS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2]$$

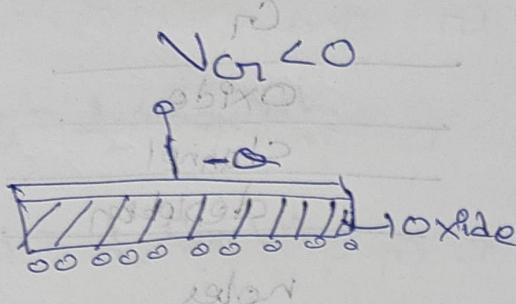
$$I_D = \frac{1}{2} \mu n C_{ox} \frac{W}{L} (V_{DS} - V_T)^2$$

For Saturation  
 $V_{DS} \geq V_{DS} - V_T$

$$V_{DS} \geq V_T$$

### ③ MOS capacitance

#### i) Accumulation mode



→ holes accumulate at the semiconductor oxide interface layer.

⇒ oxide and accumulated carriers

are in direct contact

$$so \quad C \approx C_{ox}$$

$$\boxed{C_{ox}} \approx \frac{\text{Capacitance per unit area}}{\text{Area}}$$

#### ii) Depletion mode

$$0 < V_{GS} < V_T$$

→ holes are repelled

↳ depletion layers form

$$C_{ox} = \frac{A}{d} \quad \text{and} \quad C_{dep} = \frac{A}{2d}$$

$$C = \frac{C_{ox} \cdot C_{dep}}{C_{ox} + C_{dep}}$$

→ It is less than accumulation

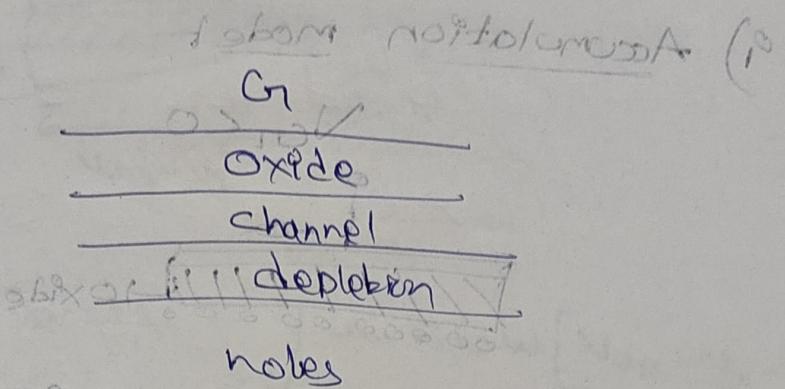
Capacitance

fewer electrons & same

## ① Inversion Region

$$V_{GS} > V_{TH}$$

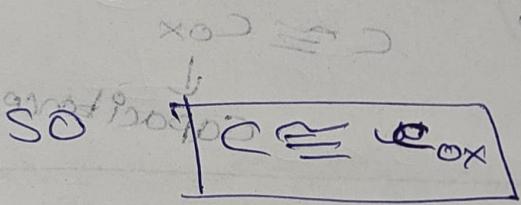
$\Rightarrow$



holes

$\rightarrow$  It is not series capacitor because

If we  $\uparrow V_{GS}$   $\Rightarrow$  concentration of holes should inc. but concentration of holes are constant



① Cut-off ( $V_{GS} < V_{TH}$ )

$\rightarrow$  No inversion channel is formed

$$C_{GS} \approx 0$$

$$C_{GD} \approx 0$$

$C_{GB}$  = Smaller than  $C_{ox}$

( $C_{ox}$  Series with  $C_{dep}$ )

$$C_{GS} \approx C_{ox}WL$$

$$\text{At } V_{GS} = V_{TH}$$

depletion layer width is max

So capacitance is lowest.

② Linear  $V_{GS} > V_{TH}$ ,  $V_{DS} < V_{GS} - V_{TH}$  (4)

↳ inversion channel exists from source to drain

$$C_{GS} = \frac{1}{2} C_{ox} WL$$

$$C_{GD} = \frac{1}{2} C_{ox} WL$$

$$C_{GB} = 0$$

③ Saturation r

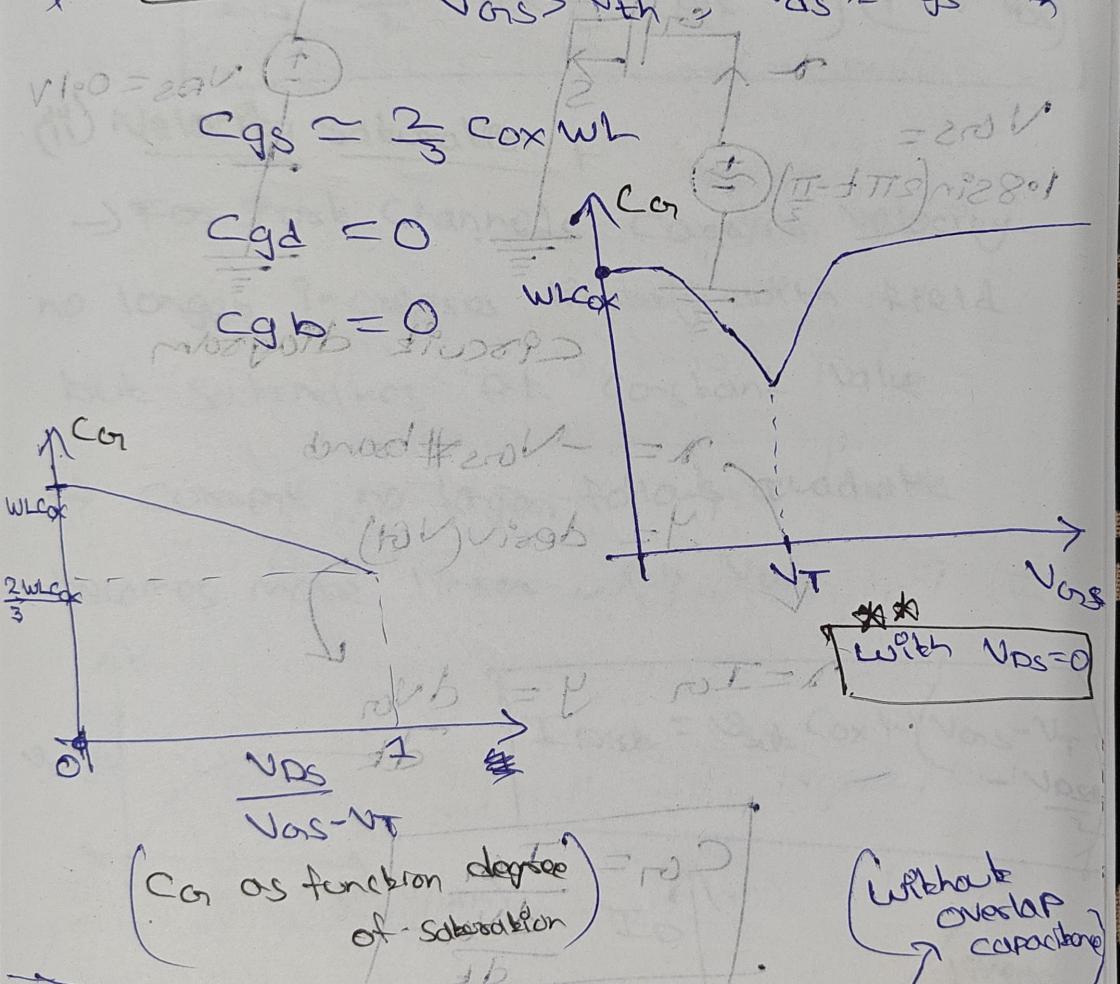
$$V_{GS} > V_{TH} \therefore V_{DS} \geq V_{GS} - V_{TH}$$

$$V_{DD} = 2.2V$$

$$C_{GS} \approx \frac{2}{3} C_{ox} WL$$

$$C_{GD} = 0$$

$$C_{GB} = 0$$



	$C_{GB}$	$C_{GS}$	$C_{GD}$	$C_{GE}$
Cutoff	$0$	$0$	$0$	$COXWL + 2CO$
Linear	$COXWL$	$\frac{1}{2} C_{ox} WL$	$\frac{COXWL}{2}$	$COXWL$ (with $C_G$ )
Saturation	$0$	$\frac{2}{3} COXWL$	$0$	$\frac{2}{3} COXWL$

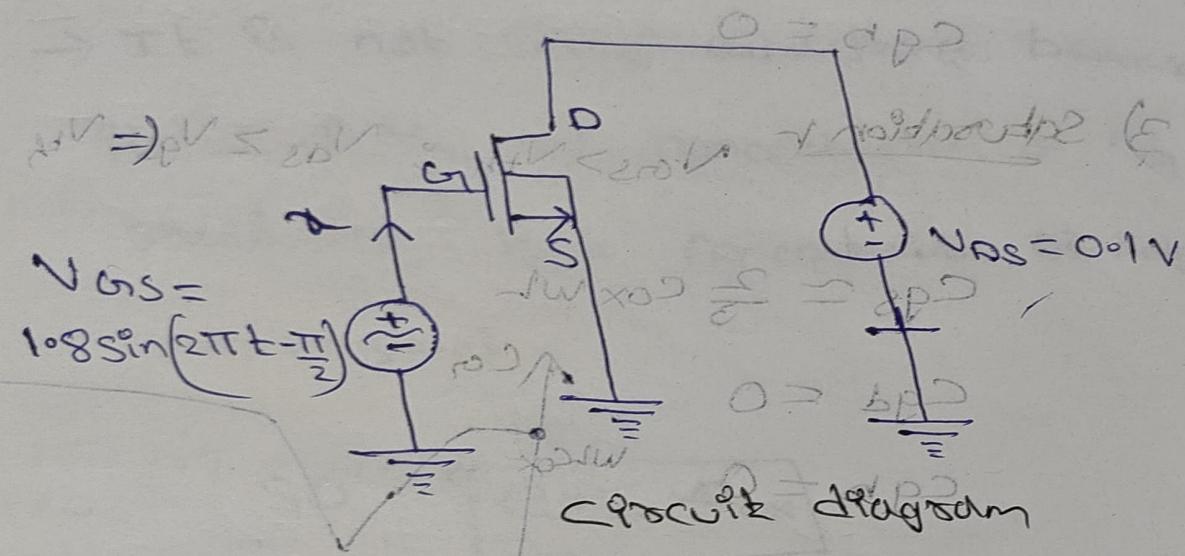
4

Circuit diagram from the netlist

$\rightarrow V_{GS}$  on gnd  $\sin(0,108,1k\text{MHz} 0^\circ)$

$\rightarrow V_{DS} \propto g_{ND} \cdot \frac{W}{D} = \frac{V_{DS}}{D}$

→ M, D Gr and grnd CMOS



$$V_{GS} = 1.08 \sin(2\pi)$$

$$1.08 \sin(2\pi)$$

$$z = -\lambda_{\text{orb}} \# \text{branch}$$

$\mathcal{Y} = \text{desinv}(N(\theta))$

$$a = I_G$$

$$CC = \frac{1}{\rho k}$$

$$C_{G1} = \left( \frac{I_{G1}}{D_{N1}} \right) \text{ (constant 20 mV)}$$

• ~~begin~~ 10 levels to

Plot  $\cos N$  vs  $N(G)$

→ From this we will get gate capacitance  $C_{GS}$  with respect to  $V_G$ .

### ③ (i) channel length modulation

→ In saturation  $I_D$  is not independent

on  $V_{DS}$ .



$$XV_{DS} = \frac{\Delta L}{L}$$

→ effective channel length  $\downarrow$

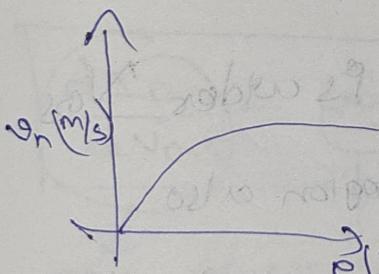
→ Drain current inc slightly with  $V_{DS}$  in saturation

$$I_D \approx \frac{1}{2} \mu_{eff} C_{ox} \frac{W}{L} (V_{GS} - V_T) (1 + \gamma V_{DS})$$

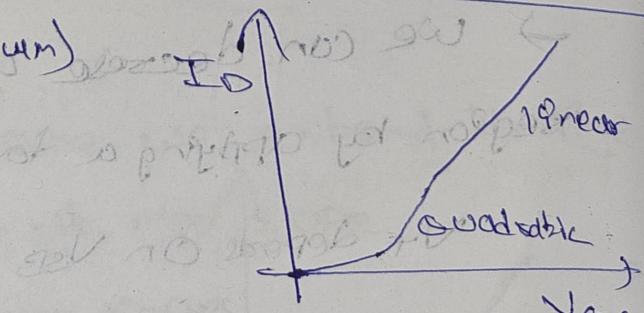
### (ii) Velocity Saturation

→ For short channels carrier velocity no longer increases linearly with field but saturates at constant value

→ Current no longer follows quadratic becomes more linear with  $V_{GS}$



$$I_{DSS} = V_{sat} C_{ox} W (V_{GS} - V_T)$$



$$(V_{GS} - V_{sat})^2 = rV$$

### (98) Mobility Degradation & ~~Impact of various factors~~ (92)

- At high  $N_{DS}$  strong electric field  $E_{DS}$  is close to  $SiO_2$ , surface toughness scatters  $b/w$   
→ mobility  $m$  decreases with inc  $N_{DS}$   
→  $I_D$  is decreased

### IV) drain induced barrier lowering ↴

- In short channel MOSFETs high  $V_{DS}$  reduces  $V_T$ , making easier for carriers to enter channel
- inc leakage current in off-state  
→  $N_T$  decreases as  $V_{DS}$  increases

$$V_T' = V_T - b \cdot V_{DS}$$

### V) Body Effect

- If depletion region is wider should fight with depletion region also.
- We can decrease width of depletion region by applying a forward bias b/w body and source  
 $N_T$  depends on  $V_{SB}$

$$V_T = V_T + V \left( \sqrt{2\phi_F} + V_{SB} - \sqrt{2\phi_F} \right)$$

IV) Sub-threshold conduction  $\rightarrow$  ~~no drain current~~

$I_D$  for  $V_{GS} < V_T \xrightarrow{AIB=0}$  carriers diffuse from source to drain.

(a)  $x_{DM} = x_{DS}$   
 $\rightarrow$  drain current decreases exponentially with  $V_{GS}$ . At position  $= 1.2Dl$

$$x_{DM} = I_{DS} \cdot e^{\frac{V_{GS}-V_T}{n \cdot V_{TH}}}$$

notes at threshold  $\rightarrow 1.2l$

⑥ ⑦  $I_D$  vs  $V_{GS}$  for  $\frac{108W}{0.48A}$

$$N_{DS} = 50mN \quad V_{GS} \rightarrow 0 - 1.08, 100mV$$

$\rightarrow$  This is in linear region.

$$\Rightarrow I_D = \frac{4nCoxW}{L} \left[ (V_{GS} - V_T) V_{DS} - \frac{1}{2} N_{DS}^2 \right]$$

For small  $V_{DS}$   $\rightarrow$   $N_{DS} \approx 0$

$$\Rightarrow I_D = \frac{4nCoxW}{L} [ (V_{GS} - V_T) V_{DS} - 0 ]$$

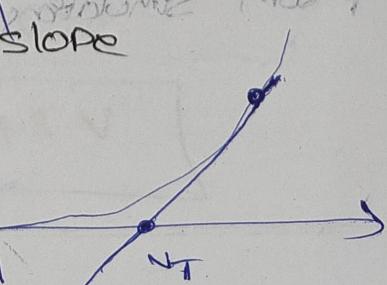
$$\frac{dI_D}{dV_{GS}} = \frac{4nCoxW V_{DS}}{L}$$

$\rightarrow$  So at max slope we extend the line

\* we draw tangent at max slope

$\rightarrow$  where it touches x-axis

$$\text{that is } V_{DS} = 1.2l$$



# Calculation

$$m = \frac{dI_D}{dV_{DS}} \text{ at } V_{DS} = 0 \text{ V}$$

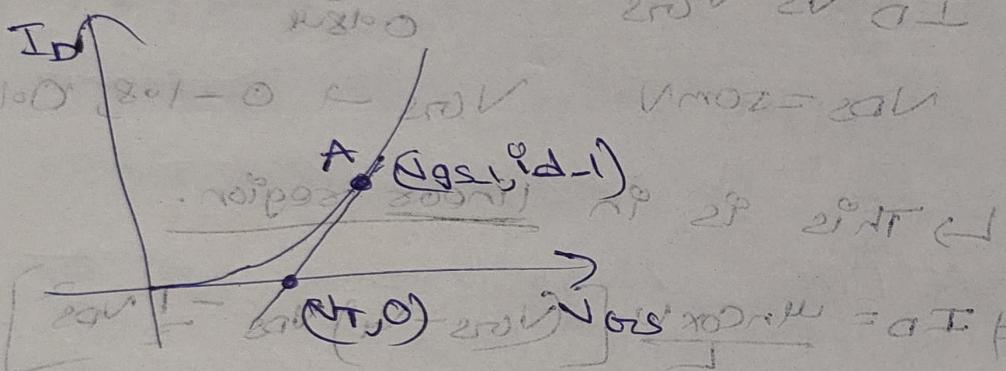
work on this

$m_{\text{max}} = \text{maximum } (m)$

$$V_{GS-1} = \text{Voltage } V_G \text{ for } I_D = m_{\text{max}}$$

$I_{D-1} = \text{current } I_D \text{ when}$

$$m = m_{\text{max}}$$



at point A we have

$$\text{slope} = m_{\text{max}}$$

and

$$A = (V_{GS-1}, I_{D-1})$$

From line (a) we get

$$\frac{I_{D-1}-0}{V_{GS-1}-V_T} = m_{\text{max}}$$

$$\Rightarrow V_T = (V_{GS-1}) - \left( \frac{I_{D-1}}{m_{\text{max}}} \right)$$

From simulations

$$\text{Slope} = m_{\text{max}} = 0.000150146$$

$$V_{GS-1} = 0.7$$

$$I_{D-1} = 2.35278E-05$$

$$V_T = 0.7 - \frac{2.35278E-05}{0.000150146}$$

$$\Rightarrow V_T = 0.5433V$$

b)  $N_{DS} = 108$

$V_{DS}$  is swept from 0 to  $108V$

$$V_{ZD00} = VM02 = 20V \quad \text{step } 101V$$

It is linearisation and  $\alpha^2$

$$I_D = \frac{1}{2} u_n \cos \frac{w}{L} (N_{DS} - V_T)^2$$

$$\sqrt{I_D} = \sqrt{\frac{1}{2} u_n \cos \frac{w}{L} (N_{DS} - V_T)^2}$$

$$\sqrt{I_D} = k(N_{DS} - V_T)$$

With  $181 \times 20V$  spot to source  
→ with slope of this line

extrapolate back to the x-axis

$$V_T = V_{DS,I} - \frac{\sqrt{I_D}}{\text{slope}}$$

From simulation

2 points I took to find slope

$$(0.6, Y_1) \quad (0.8, Y_2) \quad (Y_1, Y_2 \text{ can be found})$$

$$\text{slope} = \frac{Y_2 - Y_1}{0.8 - 0.6}$$

$$V_{DS,I} = \alpha V_{DS} \quad V_{th} = 0.8 - \frac{Y_2}{\text{slope}}$$

$$\Rightarrow V_{th} = 0.445V$$

⑥ There is difference in  $\eta$  in case (a) and case (b).

→ Case ④

$$\text{Case (a)} \quad V_{\text{DD}} = 2.9 \text{ V} \quad V_{\text{DS}} = 50 \text{ mV} = 0.05 \text{ V}$$

→ So because of small ~~these~~ ~~that's~~ these

Is no DIBL in case @

Case B:  $\text{www.} \neq \text{aTc}$

$$\hookrightarrow NDS = \log_2 N = 2^k$$

→ Because of large VDS DIBL will  
not sink to equilibrium &  
be there in case (b)  
Exo-X end of band aligning

DIBL

doings

With a large drain bias, the electric field pulls down source-channel potential.

$$\boxed{V_T = V_{T0} - h \frac{V_0}{2}}$$

o

$$V_T \text{ for } N_{DS} = 50\text{mV}$$

$$V_{DS} \geq V_T \text{ for } N_D = 108V$$

$V_2 + H_2O \rightarrow$  because of DIBL

7 Let  $V_P = 0 = V_{DSQOP} = 20V$   $20V$

$$V_{DS} = 0.05V$$

For linear region  $V_{DS} = (0, 1.08V, 0.1V) \text{ volt}$   $\rightarrow$   
because work of output voltage good with

(A) For saturation region  $V_{DS} = 1.08V$   $\rightarrow$  added load good process  
 $V_{DS} = (0, 1.08V, 0.1V)$   $\rightarrow$  good to save cost

(i)  $V_{BS} = 0V$   $\rightarrow$  I took  $MOS$  to be in linear region  
For calculating  $m_{Cox}$  and  $N_T$ .

$$\Rightarrow \tilde{V}_{DS} \approx 0$$

$$\Rightarrow I_D = m_{Cox} \frac{W}{L} ((V_{DS} - V_T) V_{GS})$$

$$m = \frac{\partial I_D}{\partial V_{DS}} = m_{Cox} \frac{W}{L} \cdot N_T$$

max for least distribution

$$\Rightarrow m_{Cox} = \frac{(m)_{\text{max}} \cdot L}{V_{DS}} = \frac{I_D(\text{at } m_{\text{max}})}{N_T \cdot m_{\text{max}}}$$

$$V_T = V_{DS} \text{ (at } m_{\text{max}})$$

From simulation

I got

$$V_T = 0.543V$$

$$m_{Cox} = 3.00 \times 10^4$$

$$Q9) V_{BS} = 0.9V \quad V_{P.D} = 20V \quad 20T < \\ \text{For this case to find } N_T, \mu_{COX}$$

↳ For this case to find  $N_T$ ,  $\mu_{COX}$   
 I took mosfet to be in saturation

$$I_D = \frac{1}{2} \mu_{COX} \frac{W}{L} (V_{DS} - V_T)^2$$

$$I_D = \frac{1}{2} \mu_{COX} \frac{W}{L} \cdot (V_{DS} - V_T)$$

$$J_{ID} = k \cdot (V_{DS} - V_T)$$

↳ with the slope of line  $\pm k$  we can extrapolate back to x-axis to find  $V_T$ .

$$\text{and } k = \sqrt{\frac{1}{2} \mu_{COX} \frac{W}{L}}$$

$$\begin{aligned} N_T &= V_{DS} - \frac{\sqrt{I_D}}{\text{slope}} \\ \mu_{COX} &= \frac{2 \times (\text{slope})^2 \times L}{W} \end{aligned}$$

$$\text{I got } V_T = 0.367V$$

$$\mu_{COX} = \frac{1.55 \times 10^{-2}}{9.75 \times 10^{-5}}$$

$$Q9) V_{BS} = -0.9V$$

↳ Again for this case I took mosfet in linear region so

$$\mu_{COX} = \frac{(m)_{\max}}{V_{DS}} \cdot \frac{L}{W}$$

$$N_T = V_{DS} \text{ (at max m)} - \frac{I_D \text{ (at max m)}}{(m)_{\max}}$$

$$\text{I got } V_T = 0.740V$$

$$\mu_{COX} = 2.086 \times 10^{-4}$$

→ For  $V_{BS} = 0.9V$  B to S  $V_{DS} = 0.9V$  forward bias  
 so  $V_T$  decreased and for  $V_{BS} = -0.9V$   
 $V_T$  is in reverse bias so  $V_T$  increased.

Due to Body effect

$$\frac{V}{(V-2mV)} \cdot \frac{w}{L} \cos \frac{1}{2} = aI$$

$$(V)_{V_{BS}=0.9V} < (V)_{V_{BS}=0} < (V)_{V_{BS}=-0.9V}$$

Now due to change in  $V_{BS}$   $\frac{w}{L} \cos \frac{1}{2}$  will change.

But  $w \propto V$  of  $\frac{w}{L} \cos \frac{1}{2}$   $\propto V$

$$\frac{w}{L} \cos \frac{1}{2} \propto V \text{ and}$$

$$\frac{aI}{(V-2mV)} = \frac{1}{w} \cos \frac{1}{2}$$

$$aI = \frac{(V-2mV)}{\cos \frac{1}{2}}$$

$$V_{FAC} = V$$

$$V_{FAC} = 28V \quad (99)$$

From root  $V = 28V$  out  $aI = 1A$

or  $w = 100 \mu m$

$$\frac{w}{L} \cos \frac{1}{2} = \frac{100 \mu m}{20 \mu m}$$

$$w \cos \frac{1}{2} = \frac{100 \mu m}{20 \mu m} \cdot 28V = V$$

$$V_{OHF} = V$$

$$20 \mu m \times 28V = 560 \mu m$$

⑧ Case (ii)  $\rightarrow$  2  $\frac{W}{L}$  transistors in series

Case (ii)  $\rightarrow$  single  $\frac{W}{2L}$  transistor.

ideally,

case (i)  $\rightarrow$  2  $\frac{W}{L}$  transistors in series

(Effective channel length  $\approx 2L$ )

So should behave like single mosfet ( $\frac{W}{2L}$ )

But due to second order effects both has

I<sub>DS</sub>s V<sub>DS</sub> different in two cases

(i) Channel-length modulation +

Each transistor in series experiences pinch-off individually, affecting the current differently from single longer transistor.

$\rightarrow$  Each series transistor has full width  $w$ , so the series combination carries more current than a single  $\frac{W}{2L}$  transistor.

Also

⑨ DIBI  $\rightarrow$  short channel devices show

drain voltage influence, 2 series transistors distribute this differently.

The series combination of two  $\frac{w}{L}$  transistors shows different drain current than single  $\frac{w}{2L}$  transistor

for small values of  $I_D$

$$(2AV \cdot (1 - \cos \theta)) \frac{w \cdot \cos \theta}{L} = \alpha I_D$$

$$2AV \cdot \frac{w}{L} \cos^2 \theta = \frac{\alpha I_D}{2AV b} = I_D$$

$$\left( \frac{1}{b} \times \frac{w \cdot \cos \theta}{2AV} \right) = \cos \theta = \theta$$

$$\left( \frac{1}{b} \times \frac{w \cdot \cos \theta}{2AV} \right) \cdot \frac{bI_D}{\cos \theta} = I_D$$

$$V_{DQ0} = V_{DQ0P} = 2AV \cdot \cos \theta$$

if  $\theta$  is bottom gate off we have

$\cos \theta = 0$

and now  $V_{DQ0} = 0$  at  $V_D = 0$

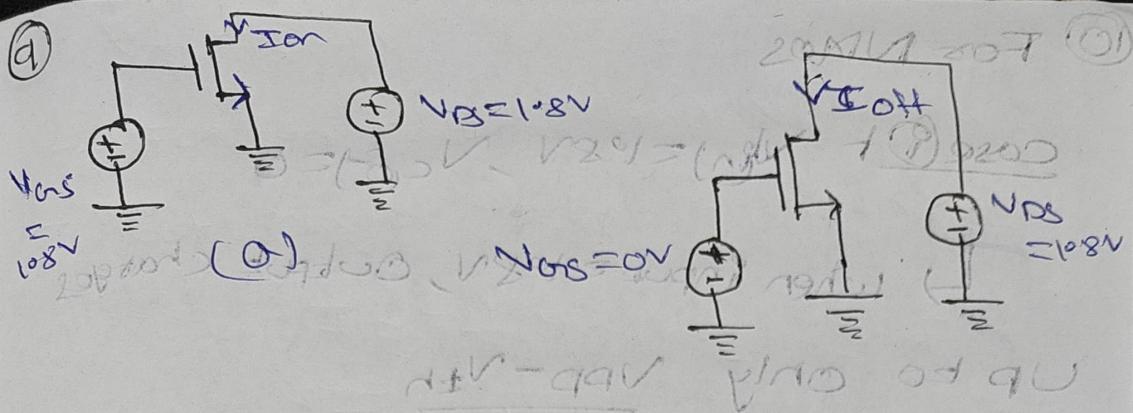
(Q)  $V_{DQ0} = 0$  at

[bottom gate to ground]

bottom gate to ground  $\theta = 0$

and now  $V_{DQ0} = 0$  at  $V_D = 0$

$V_D = 0$  at  $V_D = 0$



→ For ideal case, drain current  $I_D$  is directly proportional to  $\frac{W}{L}$ .

(approx so both)  $I_{ON}, I_{OFF}$  Scale linearly with  $W$

But practically due to second order effects

such as DIBL, mobility degradation, Velocity saturation →  $I_D$  does not vary linearly.

↳  $I_{ON}, I_{OFF}$  show approximate linear dependence on  $W$ .

$V_{DS} = 108V$

$V_{GS} = -1.8V$

$I_D \approx 10A$

$V_{DS} \approx 10V$

⑩ For NMOS

case (i) if  $V_{in} = 1.8V$ ,  $V_{CO} = 0$

↳ when input  $= 1.8V$ , output charged

up to only  $V_{DD} - V_{th}$

↳ because  $V_{out} \approx V_{in} - V_{th}$

$N_g's \approx N_{th}$  NMOS turn off

Case (ii) if  $V_{in} = 0$ ,  $V_{CO} \approx 1.8V$

→ NMOS pulls the output capacitor

node to ON

↳ Output matches Input (0V)

For PMOS

case (i) if  $V_{in} = 1.8V$ ,  $V_{CO} = 0$

↳ Output charges fully to  $1.8V$

case (ii) if  $V_{in} = 0$ ,  $V_{CO} = 1.8V$

↳ It pulls the output only down to  $V_{th}$

$V_{out} \approx V_{th}$ ,  $N_g \approx N_{th}$

PMOS turns off

so output stops at  $V_{th}$

## ⑪ Effect of Transistor width on propagation delay

↳ Propagation delay ( $t_{pd}$ ) mainly determined by how quickly the transistors can charge and discharge the load capacitors.

$$t_{pd} \approx \frac{C_L \cdot V_{DD}}{I_{drive}}$$

$$I_d \propto \frac{W}{L}$$

⇒ Thus increasing the transistor widths inc the current  $\Rightarrow$  reduces the propagation delay for a given load capacitor.

→ For small transistor widths, the current drive is weaker, so takes longer to charge/discharge.

→ For large transistor widths current inc reducing rise, fall time  $\Rightarrow$  lowers  $t_{pd}$ .

\* Scaling up W reduces delay significantly when capacitance is high.