Course Description

Academic Program: **B.Tech. in Electronics and Communication Engineering**

Course Code: **EC2.201** Title of the Course: **VLSI Design**
L-T-P: **3-1-0**. Credits: **4**
(L= Lecture hours, T=Tutorial hours, P=Practical hours)

1. Prerequisite Course / Knowledge:

Digital electronics, Network theory.

2. Course Outcomes (COs)

After completion of this course successfully, the students will be able to:

CO-1: Analyze delay and noise performances of CMOS inverter
CO-2: Apply the knowledge of delay and noise analysis of CMOS inverter for other logic styles
CO-3: Apply the knowledge of different logic styles for developing digital building blocks such as gates, multiplexors, latches and flip-flops
CO-4: Design delay optimized multistage logic circuits by using method of logical effort
CO-5: Design combinational circuits using CMOS and pass transistor logic for minimum delay and maximum noise margin performances
CO-6: Design a delay optimized sequential CMOS circuit such as 8-bit multiplier for the given load and speed requirements, while ensuring no setup time or hold time violations and verify its post lay-out performance using SPICE tools

3.Mapping of Course Outcomes (COs) with Program Outcomes (POs) and Program Specific Outcomes (PSOs) – Course Articulation Matrix

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3	PSO4
CO1	3	3	2	2	2	-	-	1	3	1	-	2	3	-	-	-
CO2	3	3	3	2	2	-	-	1	3	3	1	3	3	-	-	-
CO3	3	3	3	2	2	-	-	1	3	3	1	3	3	-	-	-
CO4	3	3	3	2	2	-	-	1	3	3	1	3	3	-	-	-
CO5	3	3	3	2	2	-	-	1	3	3	1	3	3	-	-	-
CO6	3	3	3	2	2	-	-	1	3	3	1	3	3	-	-	-

‘3’ in the box denotes ‘High-level’ mapping, 2 for ‘Medium-level’ mapping, 1 for ‘Low’-level’ mapping. Mappings with PO and PSO wherever applicable.

4. Detailed Syllabus:

Unit 1 (Introduction to VLSI design): 1) Introduction to VLSI design (top-bottom approach) - flow, applications, technologies, 2) MOSFET, FinFET transistors – Geometry and model, 3) Introduction to basic building blocks - SPICE, HDL, layout, 4) Moore's law, technology scaling, current trends (5-lectures/7.5-hours)

Unit 2 (CMOS Inverter): 1) Static characteristics- VTC, switching threshold, Noise margin, 2) Dynamic characteristics – rise time, fall time, delay, power, 3) Why CMOS Inverter, 4) CMOS inverter design flow- problem of achieving higher speeds (solution/technique discussed in the following unit), 5) From inverters to other logic - pull-up, pull-down networks, tristate inverter, Gates, Mux, Latches, Flip-flops, set-up hold time, clocked CMOS and true single phase clocked (TSPC) latches (7-lectures/10.5-hours)

Unit 3 (Multistage Logic Design and Optimization: 1) Parasitics in layout causing performance degradation – field transistor, active MOS, gate-drain overlap, latch-up, 2) Method of logical effort- fan-out, Stage effort, electrical effort, device sizing, design examples. (5-lectures/7.5-hours)

Unit 4 (Other Logic Styles): Pseudo nMOS, pass transistor logic, Cascode Voltage Switch Logic (CVSL), Dynamic logic. (3-lecturs/4.5-hours)

Unit 5 (Other topics Introduction to System Design using HDL): Finite state machines – Mealy, Moore, Intro to RTL, Data path, Control unit, combinational and sequential circuit design examples (6-lectures/9-hours)

REFERENCES:

1. Neil H. E. Weste, K. Eshraghian, "Principles of CMOS VLSI Design- A Systems Perspective", 2nd Edition, Pearson Education Pvt. Ltd.
2. J. M. Rabaey, A. Chandrakasan, B. Nikolic, "Digital Integrated Circuits - A Design Perspective", 2nd Edition, Prentice Hall of India.
3. Stephen Brown and Z. Vranesic, "Fundamentals of Digital Logic with Verilog Design", Tata McGraw-Hill Edition 2002.
4. Samir Palnitkar, "Verilog HDL – A Guide to Digital Design and Synthesis", Second edition, Pearson, 2003.
5. J. Bhaskar, "Verilog HDL Synthesis- A Practical Primer", Star Galaxy Pub; 1st edition, 2001

5.Teaching-Learning Strategies in brief:

Fundamentals of VLSI design will be discussed in the course with examples. SPICE tools will be introduced, and regular assignments will be given based on topics covered in lectures. Weekly tutorials will be conducted for problem solving and further discussions on any questions related to topics covered in lectures. A course project will be given that will involve analysis, design, layout and simulations (schematic and post-layout level) of an analog circuit for given specifications.

6. Assessment methods and weightages in brief:

Type of Evaluation	Weightage (in %)
HomeWorks	10%
Course project	20%
Quiz-1	10%
Quiz-2	10%
Mid semester exam	20%
End semester exam	30%