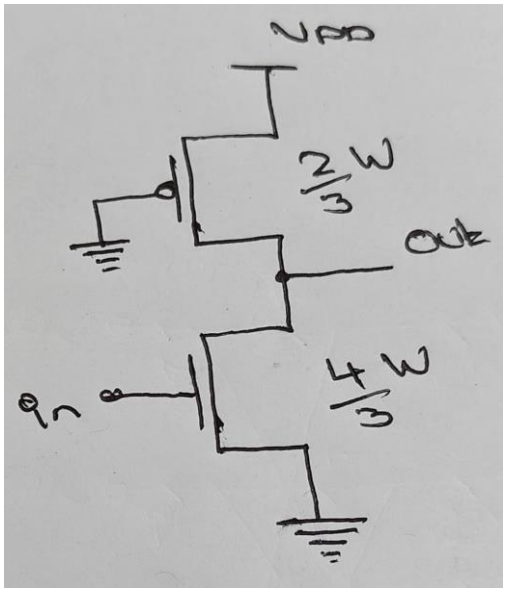
Name – SAI POOJITH (2025122010)

Assignment – 3

VLSI DESIGN

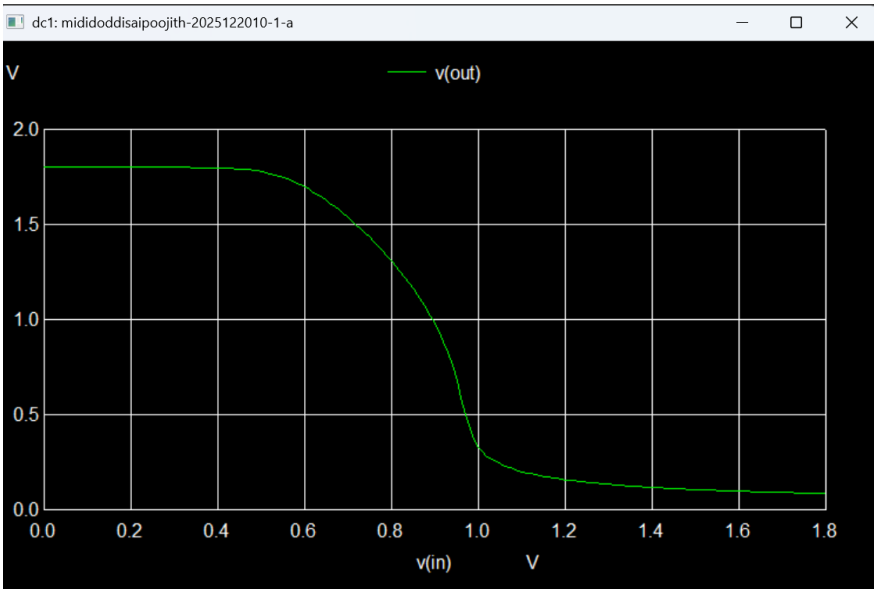
1-A



Netlist used

```
* Pseudo-NMOS Inverter VTC
.include TSMC_180nm.txt
.param Wn = 0.27u *(4/3)
.param Wp = Wn/2
.param L  = 0.18u
.param Cload = 10f
.param VDD = 1.8
.subckt pseudo_nmos in out vdd gnd Wn={Wn} Wp={Wp} L={L}
M1 out 0 vdd vdd CMOSP W={Wp} L={L}
M2 out in gnd gnd CMOSN W={Wn} L={L}
.ends pseudo_nmos
VDD vdd gnd {VDD}
Vin in gnd 0
Xinv in out vdd gnd pseudo_nmos Wn={Wn} Wp={Wp} L={L}
Cload out 0 {Cload}
.control
dc Vin 0 1.8 0.01
run
set curplottitle="mididoddisaipoojith-2025122010-1-A"
plot v(out) vs v(in)
.endc
.end
```

simulation data



Pseudo-NMOS inverter - VTC

In a Pseudo-NMOS inverter, the PMOS transistor is always ON because its gate is permanently tied to ground.

SO,

1. When the input $V_{in} = 0$:
   The NMOS is OFF, and the PMOS pulls the output to V_{DD}(logic HIGH).
   Only a small leakage current flows, resulting in negligible static power dissipation.

2. When the input $V_{in} = V_{DD}$:
   The NMOS is ON and the PMOS is also ON, so both transistors conduct simultaneously.
   A direct path from $V_{DD}$to ground exists, causing a continuous static current $I_{DD,static}$.
   This leads to static power dissipation.

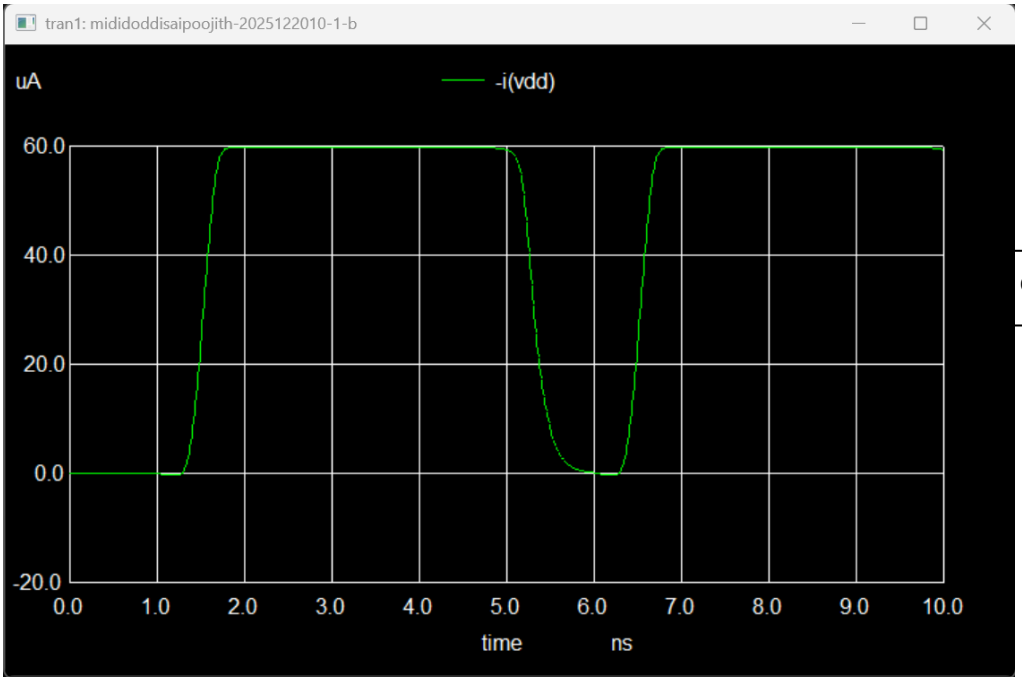
Because the PMOS never turns OFF completely, static current exists whenever the output is low, even when the circuit is not switching. As a result, the output never reaches exactly 0 V but settles slightly above ground.
This is the main disadvantage of pseudo-NMOS logic—it consumes static power even in steady state.

1-B

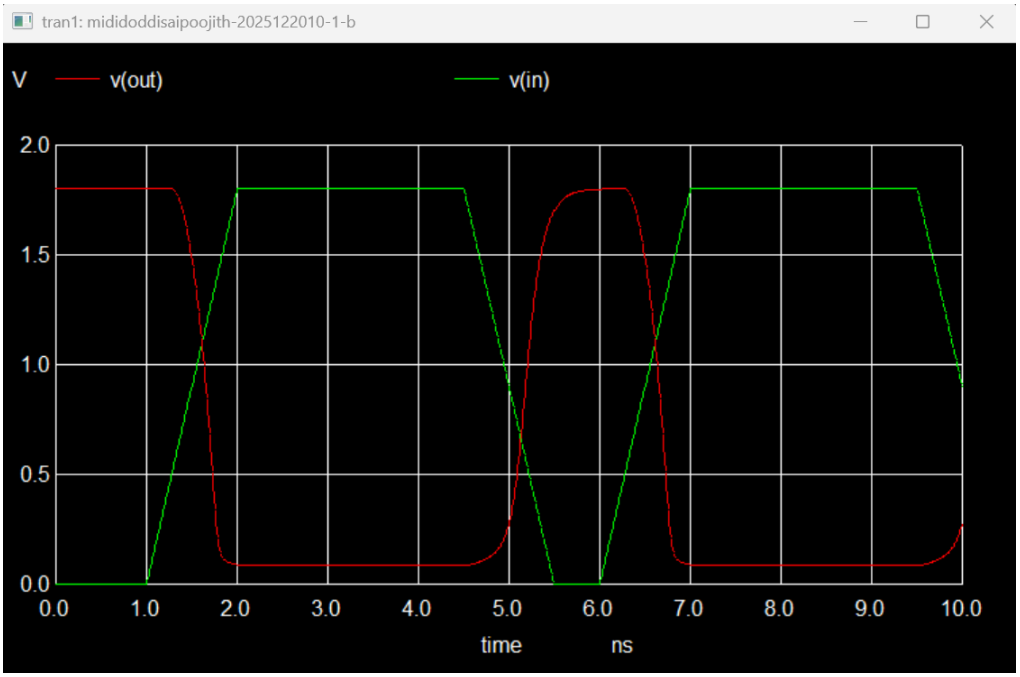
Netlist used

```
* Pseudo-NMOS Inverter Transient Simulation
.include TSMC_180nm.txt
.param Wn = 0.27u *(4/3)
.param Wp = Wn/2
.param L  = 0.18u
.param Cload = 10f
.param VDD = 1.8
.subckt pseudo_nmos in out vdd gnd Wn={Wn} Wp={Wp} L=
{L}
M1 out 0 vdd vdd CMOSP W={Wp} L={L}
M2 out in gnd gnd CMOSN W={Wn} L={L}
.ends pseudo_nmos
VDD vdd gnd {VDD}
Vin in gnd PULSE(0 {VDD} 1n 1n 1n 2.5n 5n)
Xinv in out vdd gnd pseudo_nmos Wn={Wn} Wp={Wp} L={L}
Cload out gnd {Cload}
.control
tran 0.01n 10n
set curplottitle="mididoddisaipoojith-2025122010-1-B"
plot v(in) v(out)
plot -i(VDD)
.endc
.end
```

simulation data



consumes static power

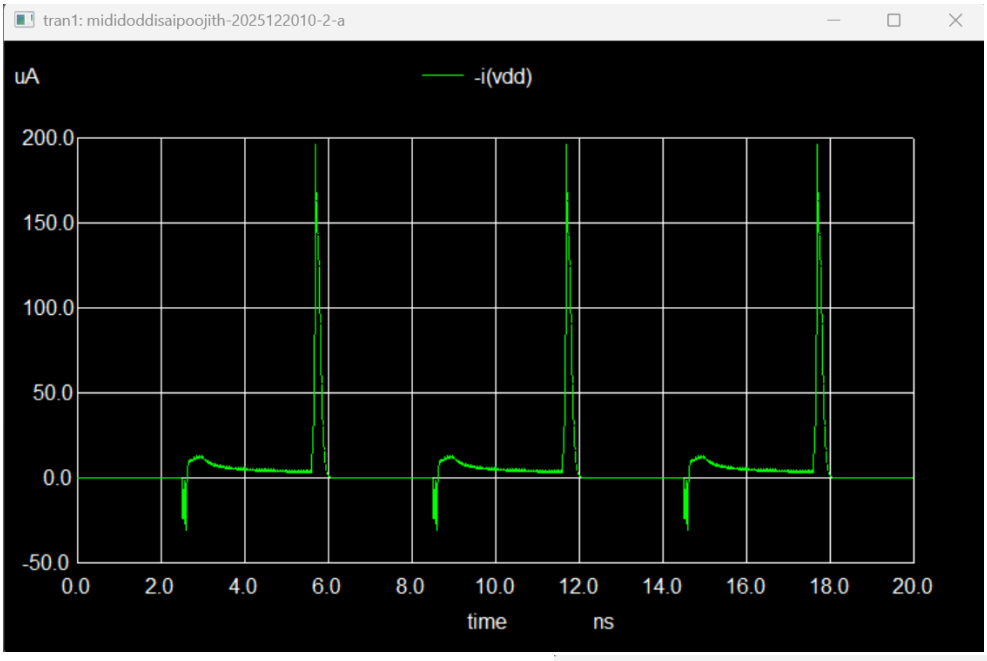


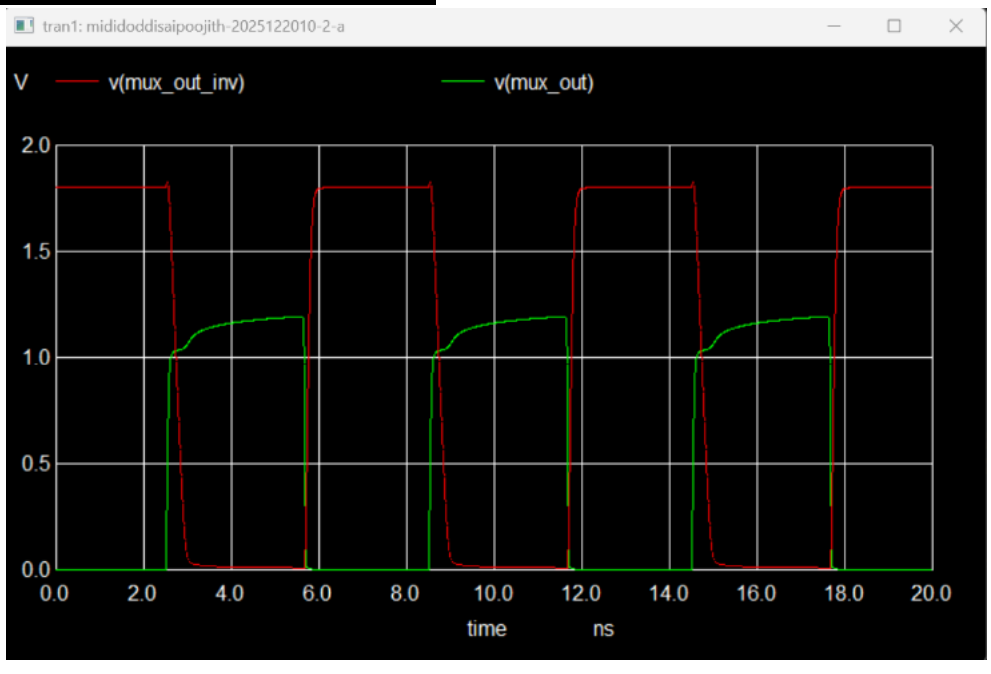
2-A

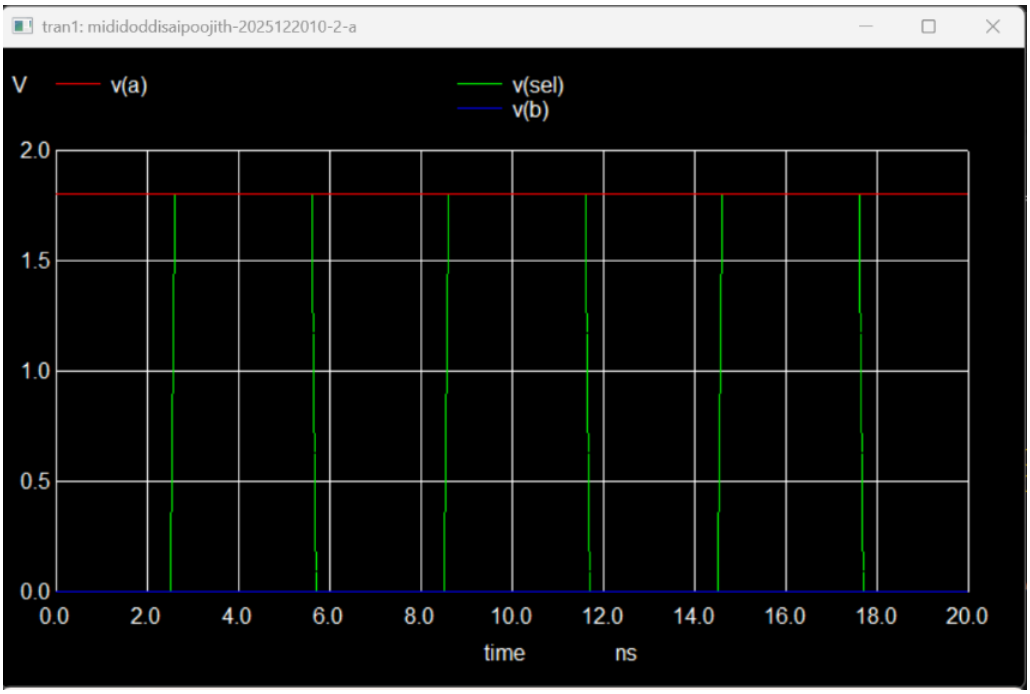
Netlist used

```
* NMOS Pass-Transistor 2:1 MUX (No Weak Keeper)
.include TSMC_180nm.txt
.param VDD   = 1.8
.param Wn    = 0.27u
.param Wp    = 0.54u
.param L     = 0.18u
.param Wpass = 0.27u
.param Cload = 10f
.subckt cmos_inv in out vdd gnd Wn={Wn} Wp={Wp} L={L}
Mp out in vdd vdd CMOSP W={Wp} L={L}
Mn out in gnd gnd CMOSN W={Wn} L={L}
.ends cmos_inv
.subckt mux2to1 a b sel out vdd gnd Wpass={Wpass} L={L}
Mp1 sel_bar sel vdd vdd CMOSP W={Wp} L={L}
Mn1 sel_bar sel gnd gnd CMOSN W={Wn} L={L}
Ma out sel a gnd CMOSN W={Wpass} L={L}
Mb out sel_bar b gnd CMOSN W={Wpass} L={L}
.ends mux2to1
VDD vdd gnd {VDD}
Va a gnd VDD
Vb b gnd 0
Vsel sel gnd PULSE(0 {VDD} 2.5n 0.1n 0.1n 3n 6n)
X1 a b sel mux_out vdd gnd mux2to1 Wpass={Wpass} L={L}
X2 mux_out mux_out_inv vdd gnd cmos_inv Wn={Wn} Wp={Wp} L={L}
Cload mux_out_inv gnd {Cload}
.control
tran 0.01n 20n
set curplottitle="mididoddisaipoojith-2025122010-2-A"
plot v(sel) v(a) v(b)
plot v(mux_out) v(mux_out_inv)
plot -i(VDD)
meas tran Trise TRIG v(mux_out_inv) VAL=0.18 RISE=1 TARG v(mux_out_inv) VAL=1.62 RISE=
meas tran Tfall TRIG v(mux_out_inv) VAL=1.62 FALL=1 TARG v(mux_out_inv) VAL=0.18 FALL=
1endc
.end
```

simulation data

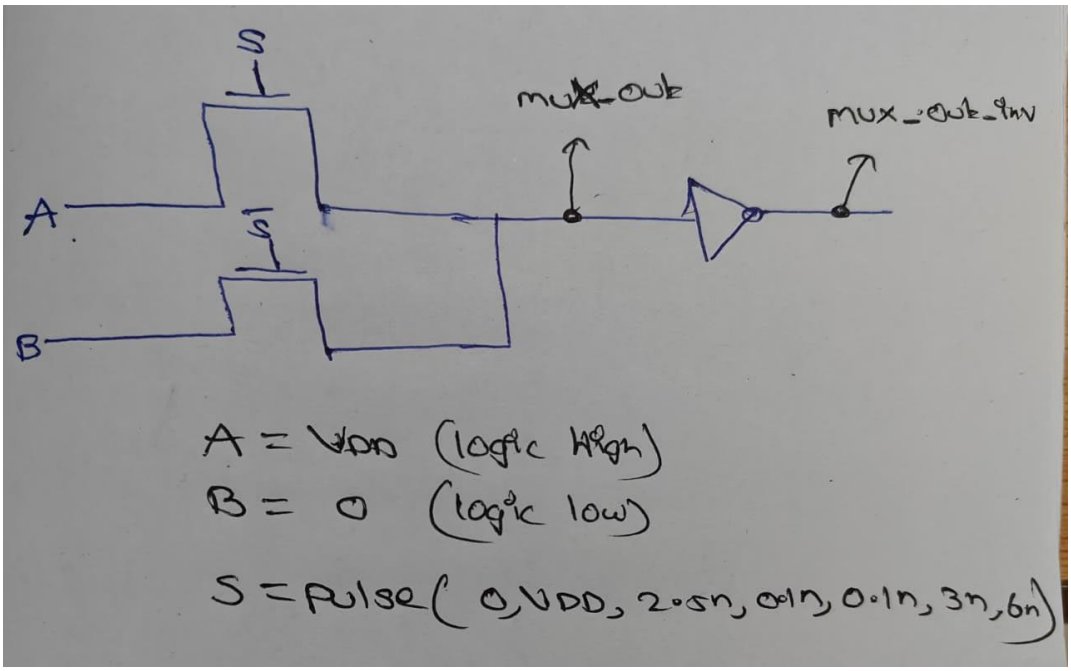







```
No. of Data Rows : 2044
trise                =   1.398714e-10
tfall                =   3.186693e-10
ngspice 1 ->
```

2 input multiplexor (without Weak-Keeper)



In an NMOS pass-transistor 2:1 MUX, the output node does not always achieve full logic levels because NMOS transistors can only pass a strong ‘0’ but degrade a ‘1’ by a threshold voltage drop (VDD − VTN). As a result, when a logic HIGH is passed, the MUX output may only reach VDD − VTN instead of the full VDD. By connecting a CMOS inverter at the MUX output, the degraded logic levels are restored, ensuring that the output swings fully between 0 V and VDD, providing proper logic levels for subsequent stages.

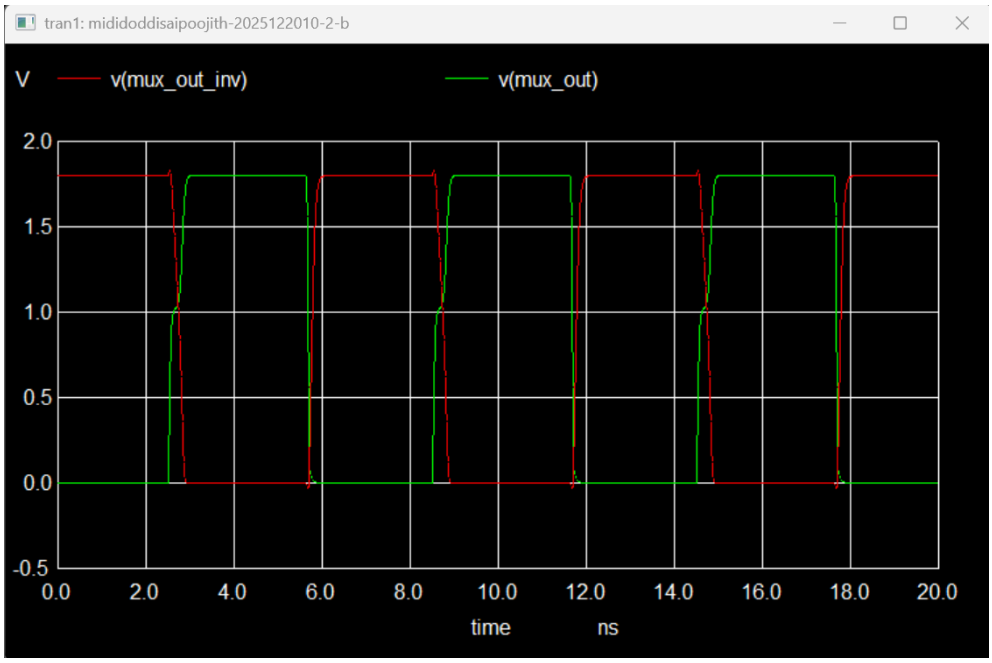
2-B

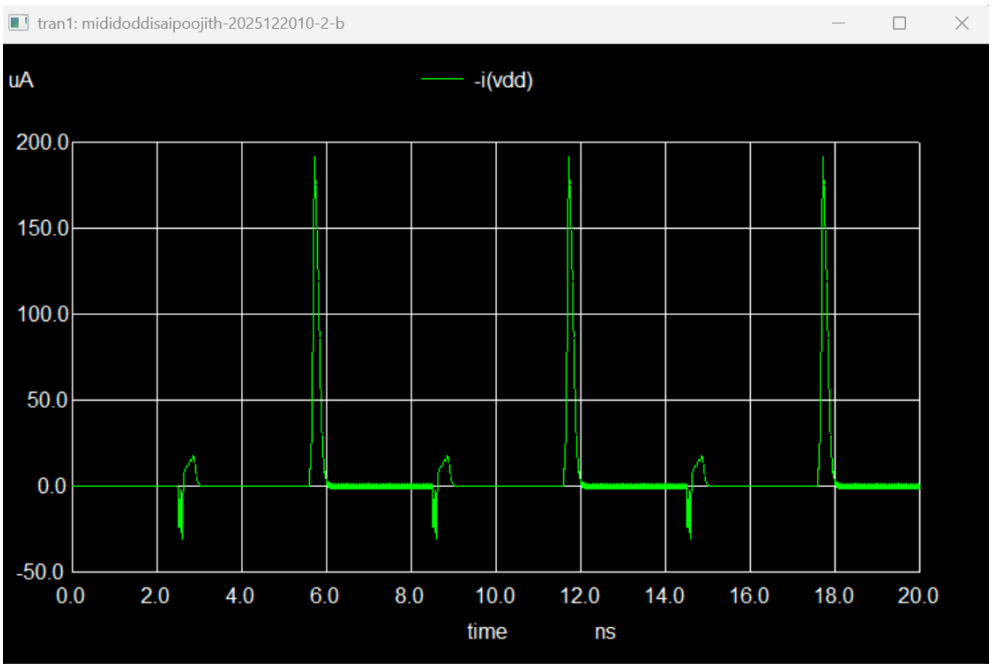
Netlist used

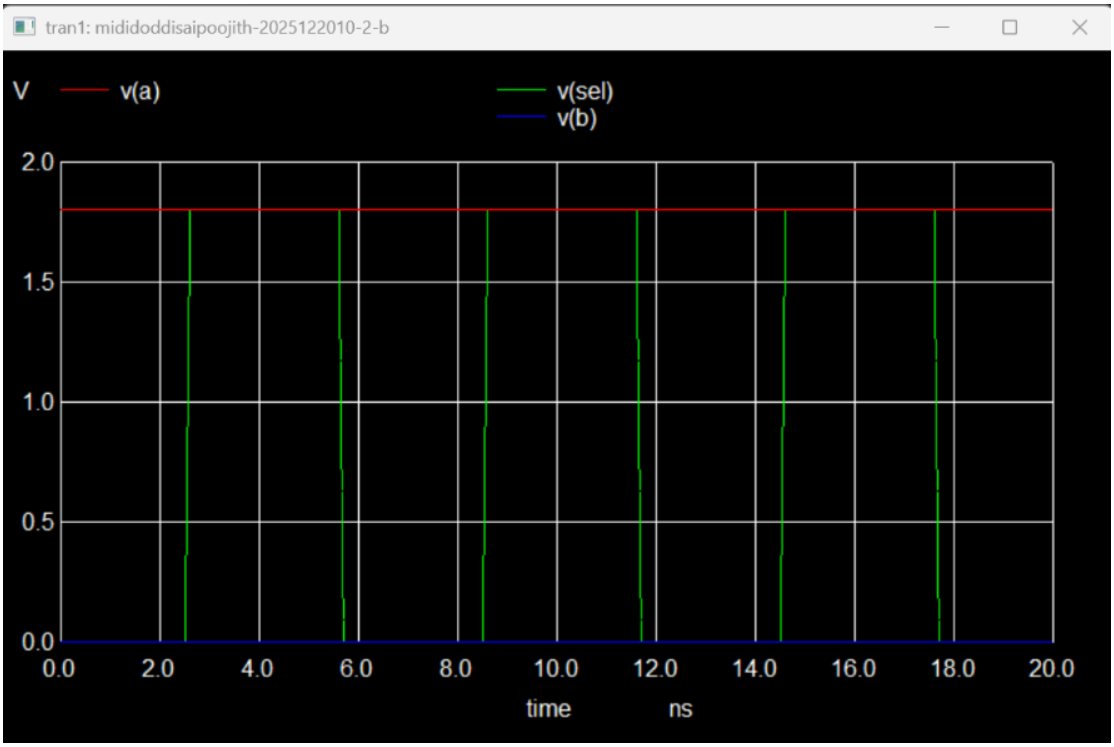
```
* NMOS Pass-Transistor 2:1 MUX (With Weak Keeper)
.include TSMC_180nm.txt
.param VDD      = 1.8
.param Wn       = 0.27u
.param Wp       = 0.54u
.param L        = 0.18u
.param Wpass    = 0.27u
.param Cload    = 10f
.param Wp_keep  = 0.14u
.subckt cmos_inv in out vdd gnd Wn={Wn} Wp={Wp} L={L}
Mp out in vdd vdd CMOSP W={Wp} L={L}
Mn out in gnd gnd CMOSN W={Wn} L={L}
.ends cmos_inv
.subckt mux2to1 a b sel out vdd gnd Wpass={Wpass} L={L}
Mp1 sel_bar sel vdd vdd CMOSP W={Wp} L={L}
Mn1 sel_bar sel gnd gnd CMOSN W={Wn} L={L}
Ma out sel a gnd CMOSN W={Wpass} L={L}
Mb out sel_bar b gnd CMOSN W={Wpass} L={L}
.ends mux2to1
VDD vdd gnd {VDD}
Va a gnd VDD
Vb b gnd 0
Vsel sel gnd PULSE(0 {VDD} 2.5n 0.1n 0.1n 3n 6n)
X1 a b sel mux_out vdd gnd mux2to1 Wpass={Wpass} L={L}
X2 mux_out mux_out_inv vdd gnd cmos_inv Wn={Wn} Wp={Wp} L={L}
Mkeeper mux_out mux_out_inv vdd vdd CMOSP W={Wp_keep} L={L}
Cload mux_out_inv gnd {Cload}
.control
tran 0.01n 20n
set curplottitle="mididoddisaipoojith-2025122010-2-B"
plot v(sel) v(a) v(b)
plot v(mux_out) v(mux_out_inv)
plot -i(VDD)
meas tran Trise TRIG v(mux_out_inv) VAL=0.18 RISE=1 TARG v(mux_out_inv) VAL=1.62 RISE=
meas tran Tfall TRIG v(mux_out_inv) VAL=1.62 FALL=1 TARG v(mux_out_inv) VAL=0.18 FALL=
1endc
.end

```

simulation data

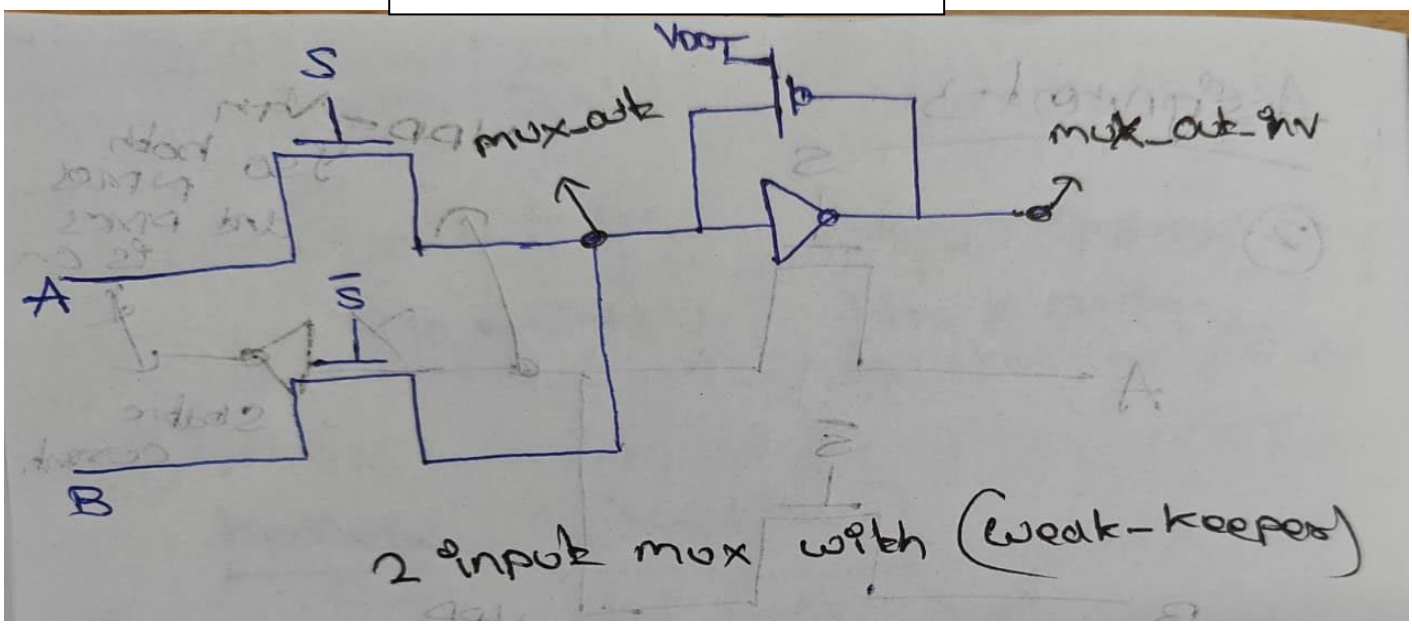







```
No. of Data Rows : 2044
trise                =   1.465586e-10
tfall                =   2.376982e-10
ngspice 1 ->
```

2 input multiplexor (with Weak-Keeper)

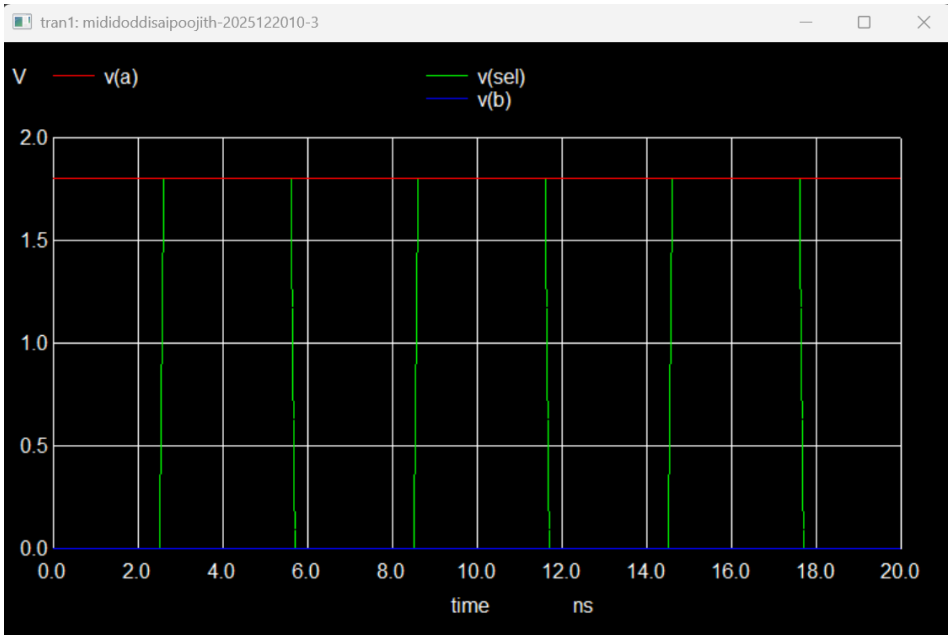


In the NMOS pass-transistor MUX without a keeper, the output node often reaches only VDD − VTN instead of a full logic HIGH. So, the NMOS transistor operates in the linear region while the PMOS remains partially ON in saturation, creating a direct path from VDD to GND and resulting in static current. By adding a weak keeper at the MUX output, the node is pulled up to full VDD. This ensures that the inverter input sees a proper logic HIGH, turning the PMOS completely OFF and the NMOS completely ON, thereby eliminating the DC path and reducing the static current to nearly zero.

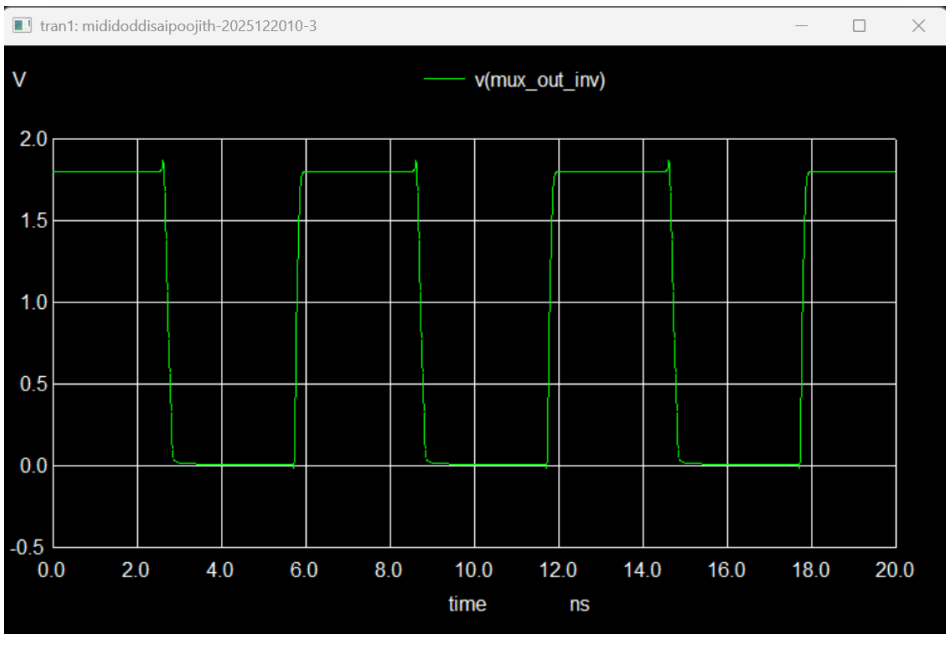
3

Netlist used

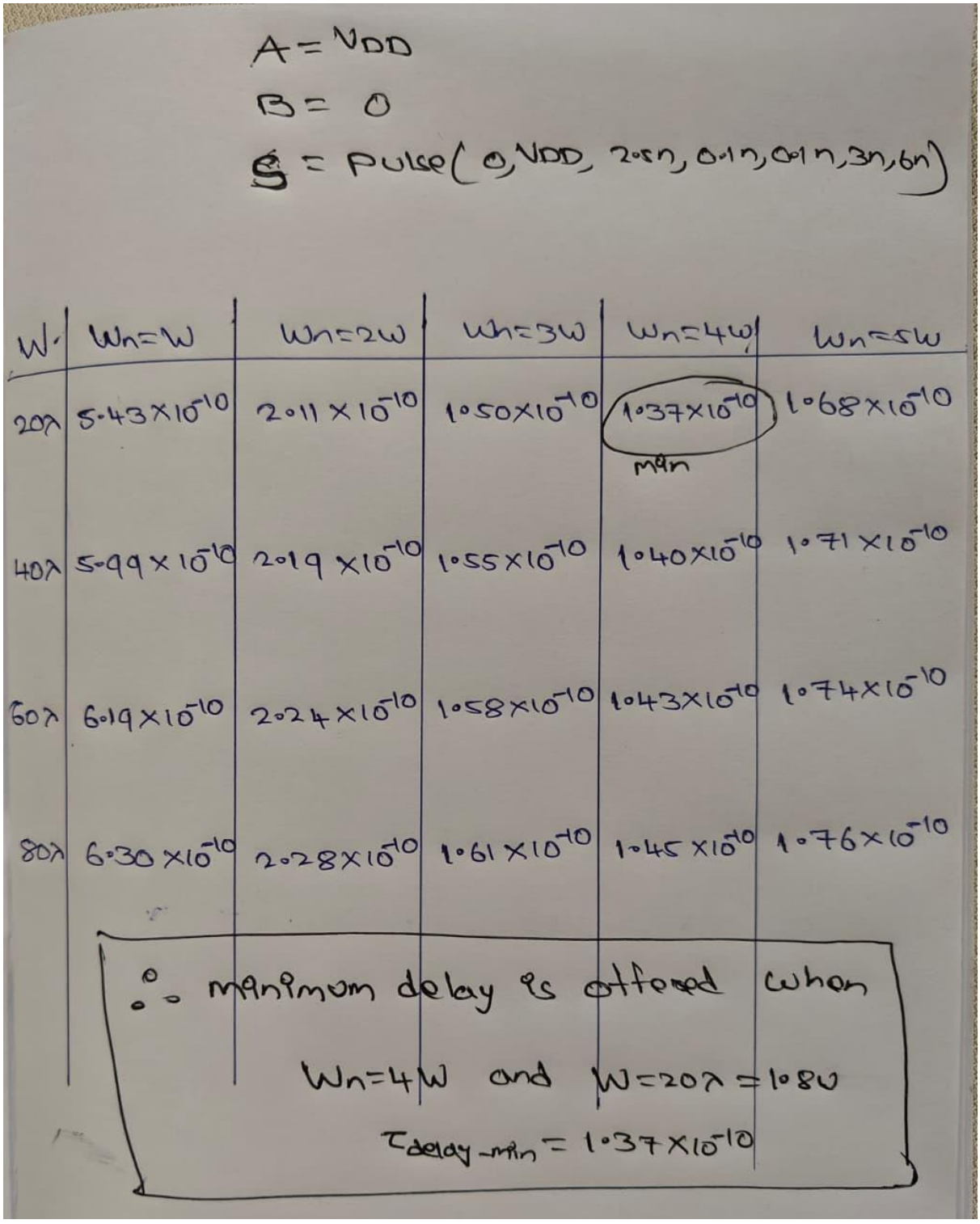
```
* NMOS Pass-Transistor 2:1 MUX
.include TSMC_180nm.txt
.param VDD   = 1.8
.param L     = 0.18u
.param W     = 1.8u
.param Wn_inv= 4*W
.param Wp_inv= (6*W-Wn_inv)
.param Wn    = W
.param Wp    = 2*W
.param Wpass = W
.subckt cmos_inv in out vdd gnd Wn_inv={Wn_inv} Wp_inv={Wp_inv} L={L}
Mp out in vdd vdd CMOSP W={Wp_inv} L={L} AS={Wp_inv*0.5u} AD={Wp_inv*0.5u} PS={2*(Wp_inv+L)} PD={2*(Wp_inv+
Mn out in gnd gnd CMOSN W={Wn_inv} L={L} AS={Wn_inv*0.5u} AD={Wn_inv*0.5u} PS={2*(Wn_inv+L)} PD={2*(Wn_inv+
.ends cmos_inv
.subckt mux2to1 a b sel out vdd gnd Wpass={Wpass} L={L} Wn={Wn} Wp={Wp}
Mp1 sel_bar sel vdd vdd CMOSP W={Wp} L={L} AS={Wp*0.5u} AD={Wp*0.5u} PS={2*(Wp+L)} PD={2*(Wp+L)}
Mn1 sel_bar sel gnd gnd CMOSN W={Wn} L={L} AS={Wn*0.5u} AD={Wn*0.5u} PS={2*(Wn+L)} PD={2*(Wn+L)}
Ma out sel a gnd CMOSN W={Wpass} L={L} AS={Wpass*0.5u} AD={Wpass*0.5u} PS={2*(Wpass+L)} PD={2*(Wpass+L)}
Mb out sel_bar b gnd CMOSN W={Wpass} L={L} AS={Wpass*0.5u} AD={Wpass*0.5u} PS={2*(Wpass+L)} PD={2*(Wpass+L)}
.ends mux2to1
VDD vdd gnd {VDD}
Va a gnd VDD
Vb b gnd 0
Vsel sel gnd PULSE(0 {VDD} 2.5n 0.1n 0.1n 3n 6n)
X1 a b sel mux_out vdd gnd mux2to1 Wpass={Wpass} L={L} Wn={Wn} Wp={Wp}
X2 mux_out mux_out_inv vdd gnd cmos_inv Wn_inv={Wn_inv} Wp_inv={Wp_inv} L={L}
X3 mux_out_inv  Z vdd gnd cmos_inv Wn_inv={Wn} Wp_inv={Wp} L={L}
X4 mux_out_inv  Y vdd gnd cmos_inv Wn_inv={Wn} Wp_inv={Wp} L={L}
.control
tran 0.01n 20n
set curplottitle="mididoddisaipoojith-2025122010-3"
plot v(sel) v(a) v(b)
plot v(mux_out_inv)
meas tran Trise TRIG v(mux_out_inv) VAL=0.18 RISE=1 TARG v(mux_out_inv) VAL=1.62 RISE=1
meas tran Tfall TRIG v(mux_out_inv) VAL=1.62 FALL=1 TARG v(mux_out_inv) VAL=0.18 FALL=1
let Tpd = (Trise+Tfall)/2
print Tpd
.endc
.end
```



simulation data



A pass-transistor logic (PTL) based 2:1 multiplexer selects one of the two input signals using NMOS pass transistors controlled by a select signal. The output inverter restores the logic level degraded by the NMOS threshold voltage drop. The overall delay of the circuit depends on the sizing of the pass transistors and the inverter, as larger widths reduce resistance but increase parasitic capacitance. Hence, transistor dimensions are optimized through NGSPICE simulations to achieve the minimum average propagation delay while ensuring correct functionality and full logic-level restoration



W	Wn=W	Wn=2W	Wn=3W	Wn=4W	Wn=5W
20λ	5.43×10^{-10}	2.011×10^{-10}	1.050×10^{-10}	1.037×10^{-10}	1.068×10^{-10}
40λ	5.99×10^{-10}	2.019×10^{-10}	1.055×10^{-10}	1.040×10^{-10}	1.071×10^{-10}
60λ	6.19×10^{-10}	2.024×10^{-10}	1.058×10^{-10}	1.043×10^{-10}	1.074×10^{-10}
80λ	6.30×10^{-10}	2.028×10^{-10}	1.061×10^{-10}	1.045×10^{-10}	1.076×10^{-10}

4-A

4-a) Given

$$f = a_1a_2 + a_1a_3 + a_1a_4 + a_2a_3 + a_2a_4 + a_3a_4$$

when $a_1 = 0$

$$f_1 = a_2a_3 + a_2a_4 + a_3a_4$$
$$= a_2a_3 + a_2a_4 + a_3a_4$$

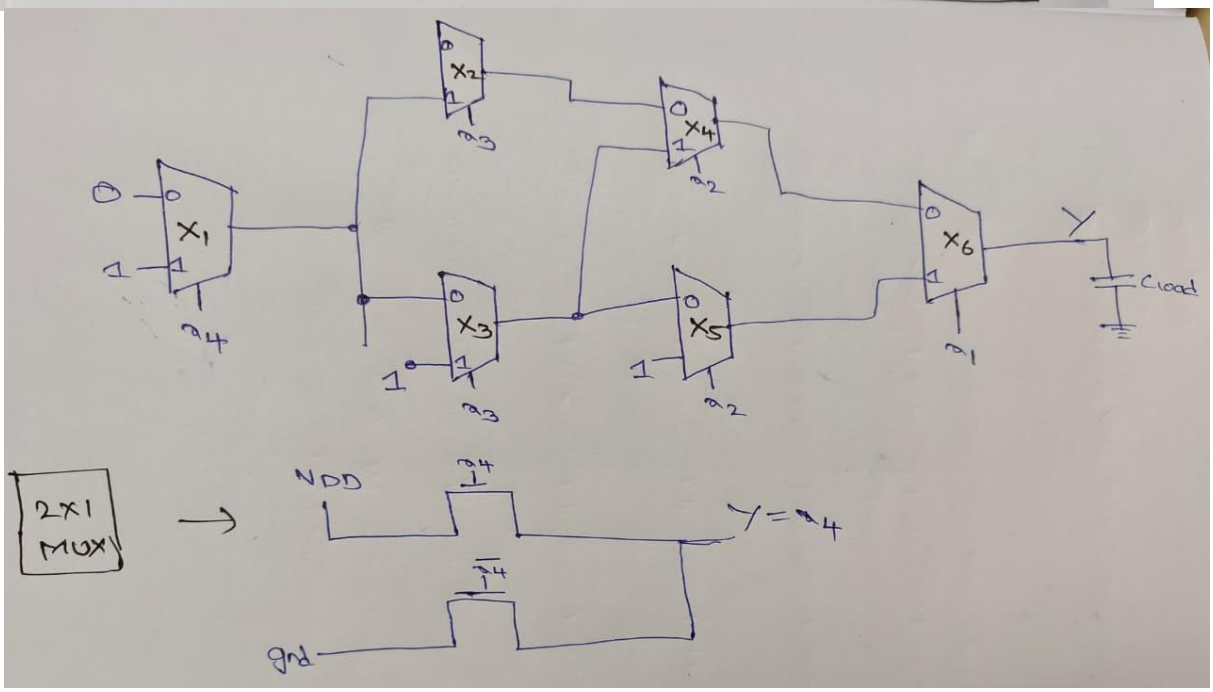
when $a_1 = 1$

$$f_2 = a_2 + a_3 + a_4 + a_2a_3 + a_2a_4 + a_3a_4$$
$$= a_2 + a_4 + a_3$$

$$\Rightarrow f = \bar{a}_1(a_2a_3 + a_2a_4 + a_3a_4) + a_1(a_2 + a_3 + a_4)$$

$$\Rightarrow f = \bar{a}_1(\bar{a}_2(a_3a_4) + a_2(a_3 + a_4)) + a_1(\bar{a}_2(a_3 + a_4) + a_2(1))$$

$$\Rightarrow f = \bar{a}_1(\bar{a}_2(a_3a_4) + a_2(\bar{a}_3a_4 + a_3)) + a_1(\bar{a}_2(\bar{a}_3a_4 + a_3) + a_2)$$



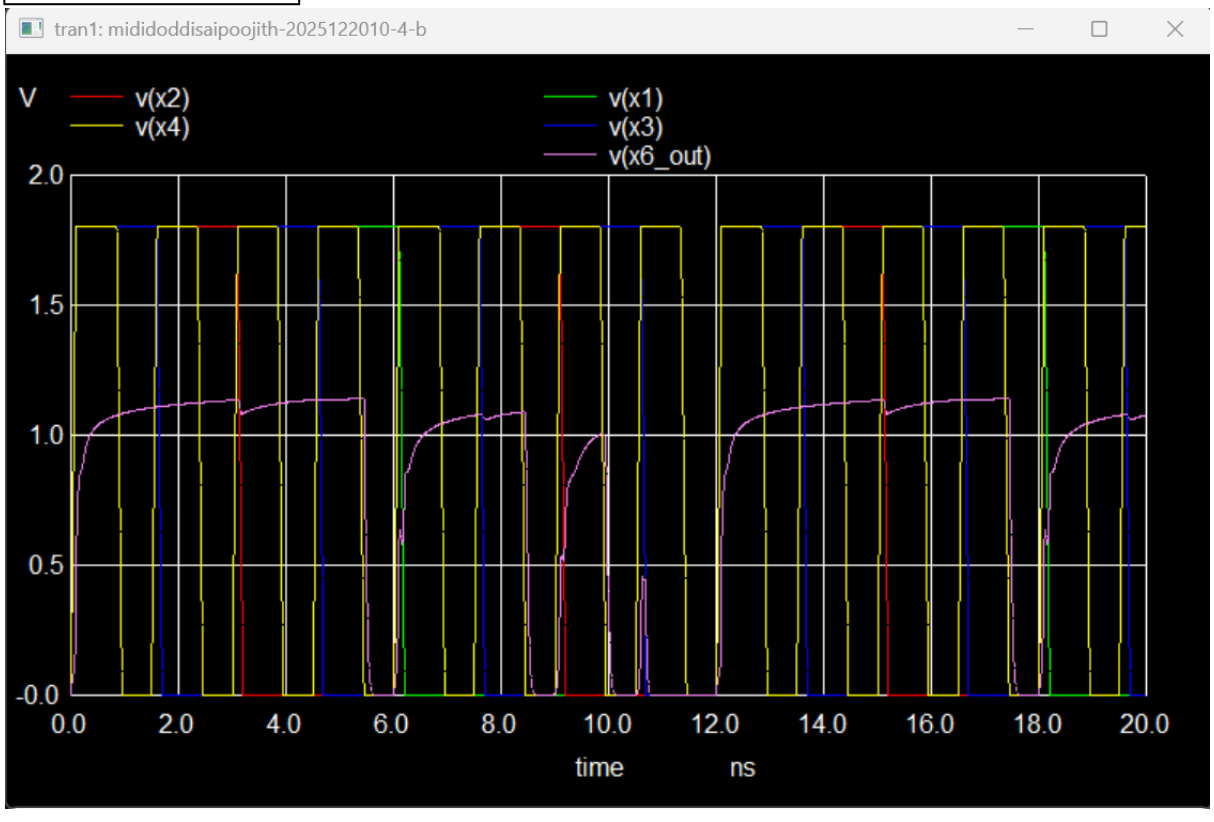
4-B

Netlist used

```
* NMOS Pass-Transistor 2:1 MUX netlist for f = x1x2 + x1x3 + x1x4 + x2x3 + x2x4 + x3x
4include TSMC_180nm.txt
.param VDD   = 1.8
.param Wn    = 1.8u
.param Wp    = 2*Wn
.param L     = 0.18u
.param Wpass = Wn
.subckt cmos_inv in out vdd gnd Wn_inv={Wn} Wp_inv={Wp} L={L}
Mp out in vdd vdd CMOSP W={Wp_inv} L={L}
Mn out in gnd gnd CMOSN W={Wn_inv} L={L}
.ends cmos_inv
.subckt mux2to1 a b sel out vdd gnd Wpass={Wpass} L={L}
Mp1 sel_bar sel vdd vdd CMOSP W={Wp} L={L}
Mn1 sel_bar sel gnd gnd CMOSN W={Wn} L={L}
Ma out sel a gnd CMOSN W={Wpass} L={L}
Mb out sel_bar b gnd CMOSN W={Wpass} L={L}
.ends mux2to1
VDD vdd gnd {VDD}
Vx1 x1 gnd PULSE(0 {VDD} 0n 0.1n 0.1n 6n 12n)
Vx2 x2 gnd PULSE(0 {VDD} 0n 0.1n 0.1n 3n 6n)
Vx3 x3 gnd PULSE(0 {VDD} 0n 0.1n 0.1n 1.5n 3n)
Vx4 x4 gnd PULSE(0 {VDD} 0n 0.1n 0.1n 0.75n 1.5n)
X1 VDD gnd x4 X1_out vdd gnd mux2to1 Wpass={Wpass} L={L}
X2 X1_out gnd x3 X2_out vdd gnd mux2to1 Wpass={Wpass} L={L}
X3 VDD X1_out x3 X3_out vdd gnd mux2to1 Wpass={Wpass} L={L}
X4 X3_out X2_out x2 X4_out vdd gnd mux2to1 Wpass={Wpass} L={L}
X5 VDD X3_out x2 X5_out vdd gnd mux2to1 Wpass={Wpass} L={L}
X6 X5_out X4_out x1 X6_out vdd gnd mux2to1 Wpass={Wpass} L={L}
X_load_1 X6_out  Z_1 vdd gnd cmos_inv Wn_inv={0.27u} Wp_inv={0.54u} L={L}
X_load_2 X6_out  Z_2 vdd gnd cmos_inv Wn_inv={0.27u} Wp_inv={0.54u} L={L}
X_load_3 X6_out  Z_3 vdd gnd cmos_inv Wn_inv={0.27u} Wp_inv={0.54u} L={L}
X_load_4 X6_out  Z_4 vdd gnd cmos_inv Wn_inv={0.27u} Wp_inv={0.54u} L={L}
.control
tran 0.01n 20n
set curplottitle="mididoddisaipoojith-2025122010-4-B"
meas tran VMAX MAX V(X6_out)
meas tran VMIN MIN V(X6_out)
plot v(x1) v(x2) v(x3) v(x4) v(X6_out)
meas tran Trise TRIG v(X6_out) VAL=0.1*VMIN RISE=1 TARG v(X6_out) VAL=0.9*VMAX RISE=1
meas tran Tfall TRIG v(X6_out) VAL=0.9*VMAX FALL=1 TARG v(X6_out) VAL=0.1*VMIN FALL=1
.endc
.end

```

simulation data

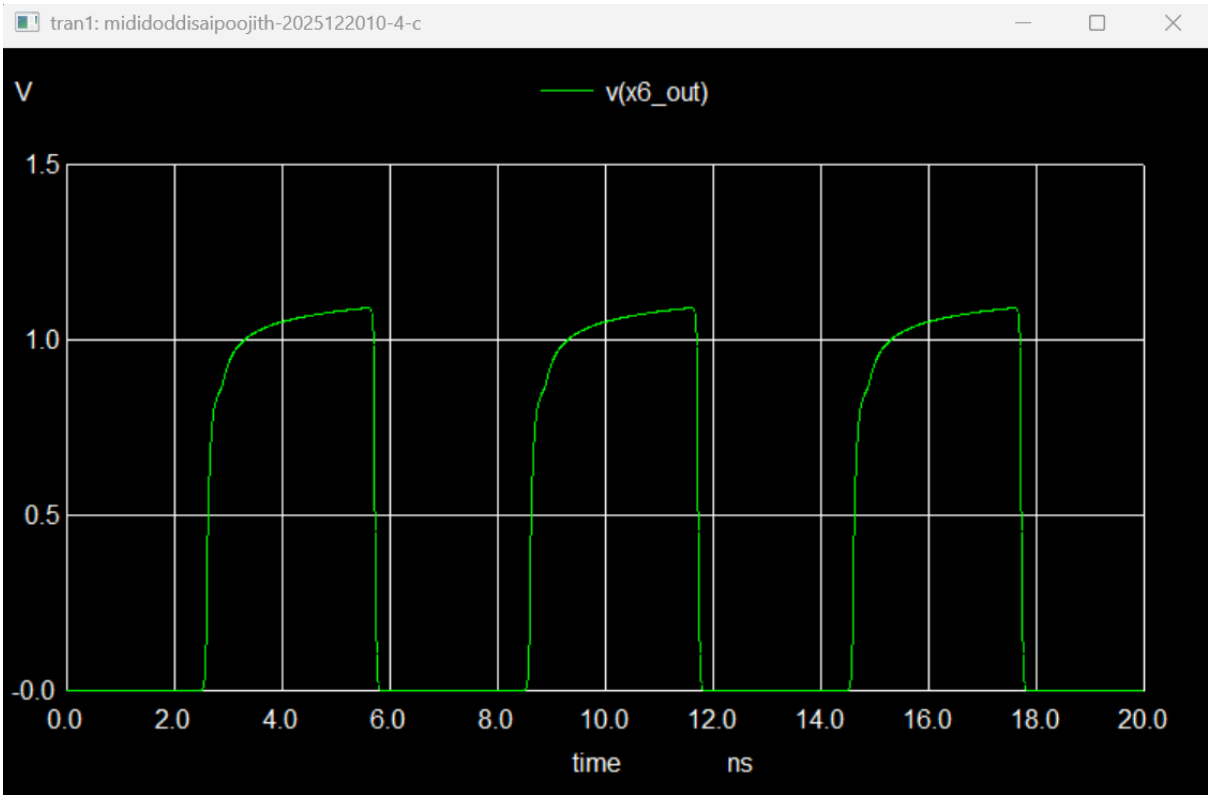


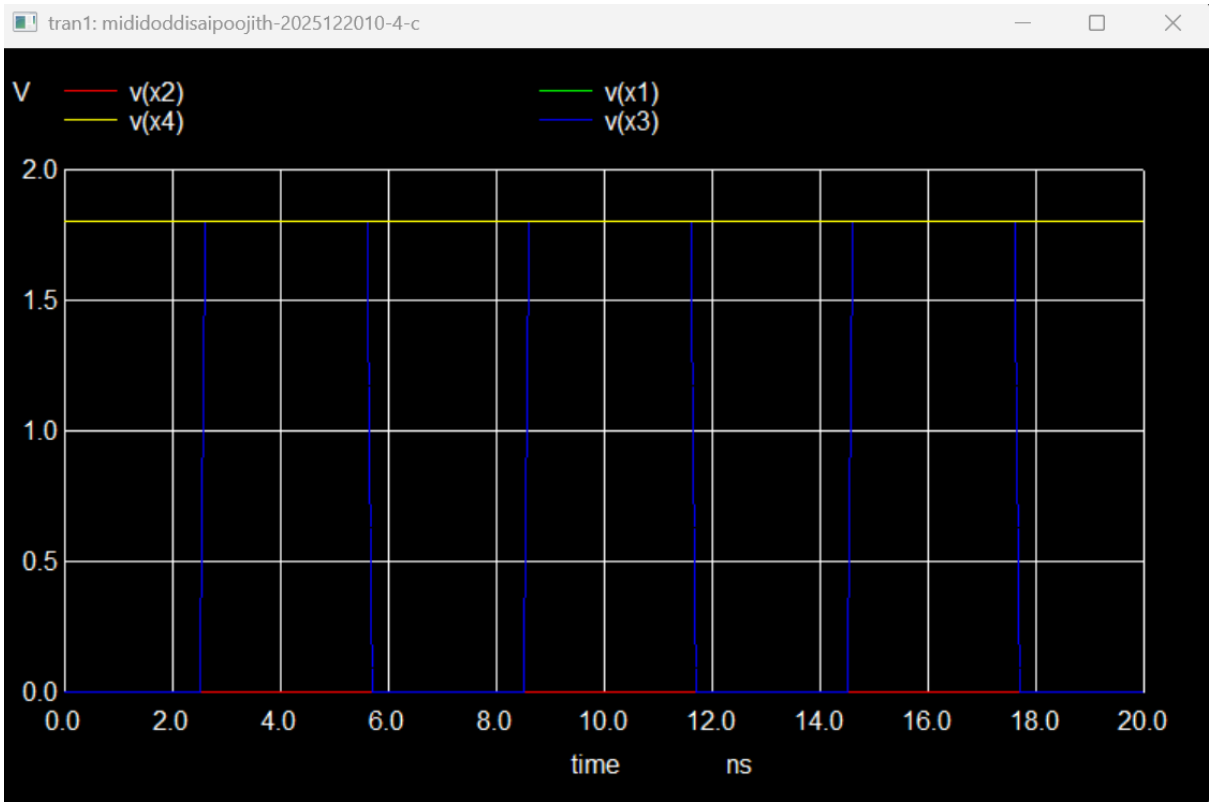
4-C

Netlist used

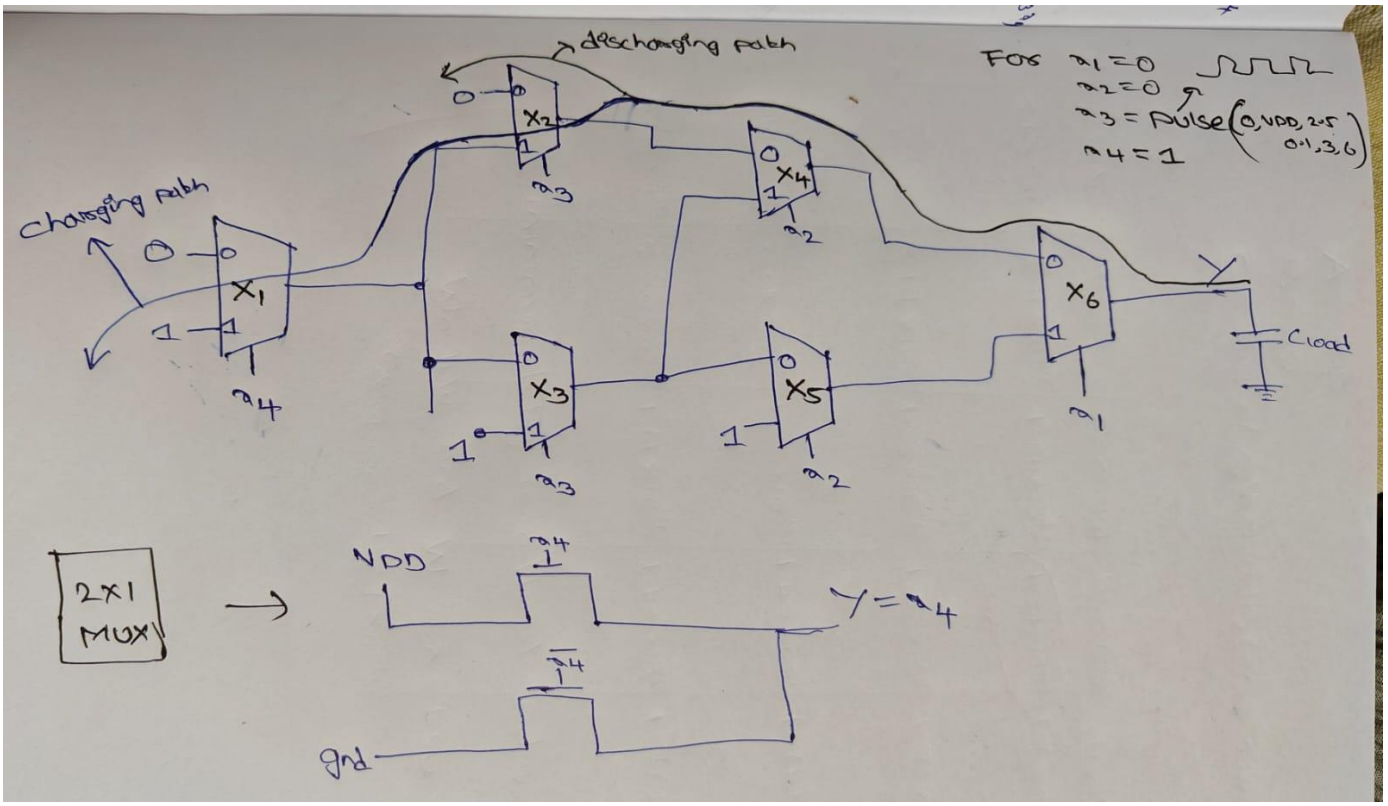
```
* NMOS Pass-Transistor 2:1 MUX netlist for f = x1x2 + x1x3 + x1x4 + x2x3 + x2x4 + x3x
4include TSMC_180nm.txt
.param VDD   = 1.8
.param Wn    = 1.8u
.param Wp    = 2*Wn
.param L     = 0.18u
.param Wpass = Wn
.subckt cmos_inv in out vdd gnd Wn_inv={Wn} Wp_inv={Wp} L={L}
Mp out in vdd vdd CMOSP W={Wp_inv} L={L}
Mn out in gnd gnd CMOSN W={Wn_inv} L={L}
.ends cmos_inv
.subckt mux2to1 a b sel out vdd gnd Wpass={Wpass} L={L}
Mp1 sel_bar sel vdd vdd CMOSP W={Wp} L={L}
Mn1 sel_bar sel gnd gnd CMOSN W={Wn} L={L}
Ma out sel a gnd CMOSN W={Wpass} L={L}
Mb out sel_bar b gnd CMOSN W={Wpass} L={L}
.ends mux2to1
VDD vdd gnd {VDD}
Vx1 x1 gnd 0
Vx2 x2 gnd 0
Vx3 x3 gnd PULSE(0 {VDD} 2.5n 0.1n 0.1n 3n 6n)
Vx4 x4 gnd VDD
X1 VDD gnd x4 X1_out vdd gnd mux2to1 Wpass={Wpass} L={L}
X2 X1_out gnd x3 X2_out vdd gnd mux2to1 Wpass={Wpass} L={L}
X3 VDD X1_out x3 X3_out vdd gnd mux2to1 Wpass={Wpass} L={L}
X4 X3_out X2_out x2 X4_out vdd gnd mux2to1 Wpass={Wpass} L={L}
X5 VDD X3_out x2 X5_out vdd gnd mux2to1 Wpass={Wpass} L={L}
X6 X5_out X4_out x1 X6_out vdd gnd mux2to1 Wpass={Wpass} L={L}
X_load_1 X6_out  Z_1 vdd gnd cmos_inv Wn_inv={0.27u} Wp_inv={0.54u} L={L}
X_load_2 X6_out  Z_2 vdd gnd cmos_inv Wn_inv={0.27u} Wp_inv={0.54u} L={L}
X_load_3 X6_out  Z_3 vdd gnd cmos_inv Wn_inv={0.27u} Wp_inv={0.54u} L={L}
X_load_4 X6_out  Z_4 vdd gnd cmos_inv Wn_inv={0.27u} Wp_inv={0.54u} L={L}
.control
tran 0.01n 20n
set curplottitle="mididoddisaipoojith-2025122010-4-C"
meas tran VMAX MAX V(X6_out)
meas tran VMIN MIN V(X6_out)
plot v(x1) v(x2) v(x3) v(x4)
plot v(X6_out)
meas tran Trise TRIG v(X6_out) VAL=0.1*VMIN RISE=1 TARG v(X6_out) VAL=0.9*VMAX RISE=1
meas tran Tfall TRIG v(X6_out) VAL=0.9*VMAX FALL=1 TARG v(X6_out) VAL=0.1*VMIN FALL=1
print Trise-Tfall
.endc
.end
```

simulation data






```
trise                  =   3.543807e-10
tfall                  =   5.713439e-11
trise-tfall = 2.972463e-10
ngspice 1 ->
```



4-D

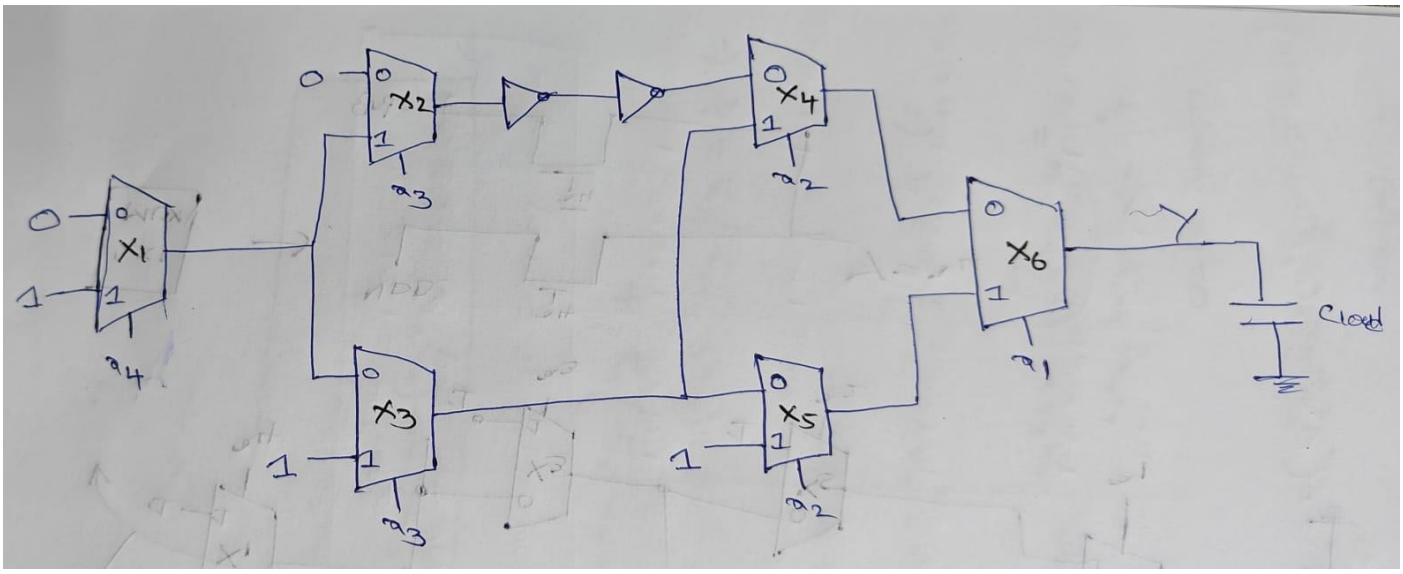
Netlist used

```
* NMOS Pass-Transistor 2:1 MUX netlist for f = x1x2 + x1x3 + x1x4 + x2x3 + x2x4 + x3x4 with Repeater
sinclude TSMC_180nm.txt
.param VDD   = 1.8
.param Wn    = 1.8u
.param Wp    = 2*Wn
.param L     = 0.18u
.param Wpass = Wn
.subckt cmos_inv in out vdd gnd Wn_inv={Wn} Wp_inv={Wp} L={L}
Mp out in vdd vdd CMOSP W={Wp_inv} L={L}
Mn out in gnd gnd CMOSN W={Wn_inv} L={L}
.ends cmos_inv
.subckt mux2to1 a b sel out vdd gnd Wpass={Wpass} L={L}
Mp1 sel_bar sel vdd vdd CMOSP W={Wp} L={L}
Mn1 sel_bar sel gnd gnd CMOSN W={Wn} L={L}
Ma out sel a gnd CMOSN W={Wpass} L={L}
Mb out sel_bar b gnd CMOSN W={Wpass} L={L}
.ends mux2to1
VDD vdd gnd {VDD}
Vx1 x1 gnd 0
Vx2 x2 gnd 0
Vx3 x3 gnd PULSE(0 {VDD} 2.5n 0.1n 0.1n 3n 6n)
Vx4 x4 gnd VDD
X1 VDD gnd x4 X1_out vdd gnd mux2to1 Wpass={Wpass} L={L}
X2 X1_out gnd x3 X2_out vdd gnd mux2to1 Wpass={Wpass} L={L}

X_rep1 X2_out K_1 vdd gnd cmos_inv Wn_inv={Wn} Wp_inv={Wp} L={L}
X_rep2 K_1 K_2 vdd gnd cmos_inv Wn_inv={Wn} Wp_inv={Wp} L={L}

X3 VDD X1_out x3 X3_out vdd gnd mux2to1 Wpass={Wpass} L={L}
X4 X3_out K_2 x2 X4_out vdd gnd mux2to1 Wpass={Wpass} L={L}
X5 VDD X3_out x2 X5_out vdd gnd mux2to1 Wpass={Wpass} L={L}
X6 X5_out X4_out x1 X6_out vdd gnd mux2to1 Wpass={Wpass} L={L}
X_load_1 X6_out  Z_1 vdd gnd cmos_inv Wn_inv={0.27u} Wp_inv={0.54u} L={L}
X_load_2 X6_out  Z_2 vdd gnd cmos_inv Wn_inv={0.27u} Wp_inv={0.54u} L={L}
X_load_3 X6_out  Z_3 vdd gnd cmos_inv Wn_inv={0.27u} Wp_inv={0.54u} L={L}
X_load_4 X6_out  Z_4 vdd gnd cmos_inv Wn_inv={0.27u} Wp_inv={0.54u} L={L}
.control
tran 0.01n 20n
set curplottitle="mididoddisaipoojith-2025122010-4-D"
meas tran VMAX MAX V(X6_out)
meas tran VMIN MIN V(X6_out)
plot v(x1) v(x2) v(x3) v(x4)
plot v(X6_out)
meas tran Trise TRIG v(X6_out) VAL=0.1*VMIN RISE=1 TARG v(X6_out) VAL=0.9*VMAX RISE=1
meas tran Tfall TRIG v(X6_out) VAL=0.9*VMAX FALL=1 TARG v(X6_out) VAL=0.1*VMIN FALL=1
print Trise-Tfall
.endc
.end
```

To equalize tPLH and tPHL, the charging path (VDD to out) and the discharging path (out to gnd) should have an equal number of transistors of the same size. Therefore, we inserted two inverters at the output of X2 (the intermediate MUX node). This ensures that the charging and discharging paths have comparable drive strength and effectively the same number of transistors in series, resulting in nearly equal rise and fall times.



simulation data

```
trise                  =   1.898644e-10
tfall                  =   5.666284e-11
trise-tfall  =  1.332016e-10
ngspice 1 ->
```

After inserting two inverters at the output of X2, the difference between rise and fall times reduced significantly to $tPLH - tPHL = 1.33 \times 10^{-10}$ s, becoming nearly equal, compared to the previous value of 2.97×10^{-10} s. This demonstrates that the inverter insertion effectively balanced the charging and discharging paths.