

# System Verilog Basics

1. Different ways to generate a Clock Signal - <https://www.edaplayground.com/x/eLGe>
2. Array basics
  - a. Fixed Size Array - <https://www.edaplayground.com/x/hdL8> , <https://www.edaplayground.com/x/9qTn>
  - b. Dynamic Array - <https://www.edaplayground.com/x/tTFv>
  - c. Queue Array - <https://www.edaplayground.com/x/uh4>
3. Initialize Array with different loops - <https://www.edaplayground.com/x/Sdbq>
4. Use Case of pass by value and pass by reference - <https://www.edaplayground.com/x/TDCu>