1. Description

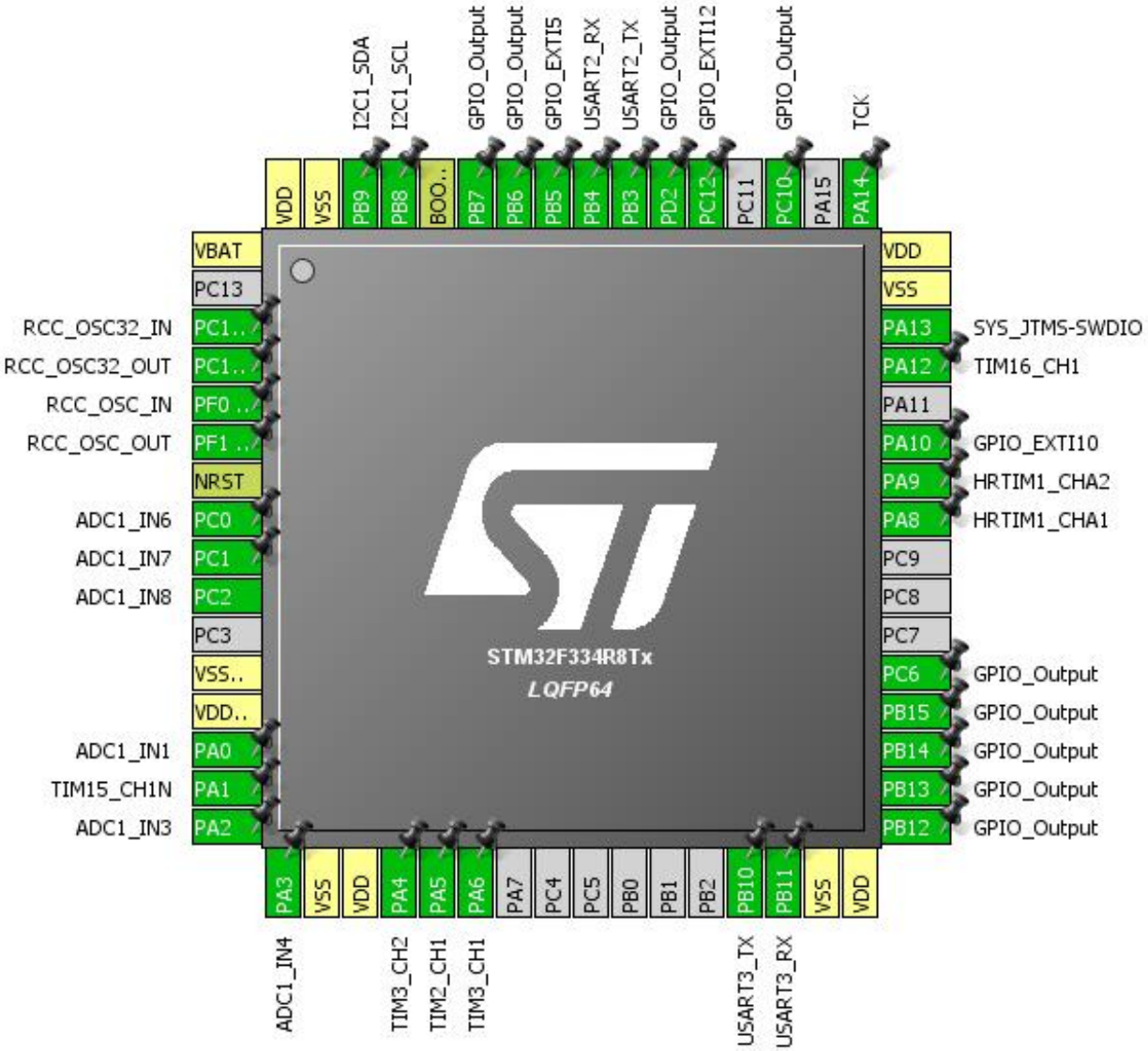
1.1. Project

Project Name	HRTIM_test_master
Board Name	NUCLEO-F334R8
Generated with:	STM32CubeMX 4.23.0
Date	10/25/2017

1.2. MCU

MCU Series	STM32F3
MCU Line	STM32F334
MCU name	STM32F334R8Tx
MCU Package	LQFP64
MCU Pin number	64

2. Pinout Configuration



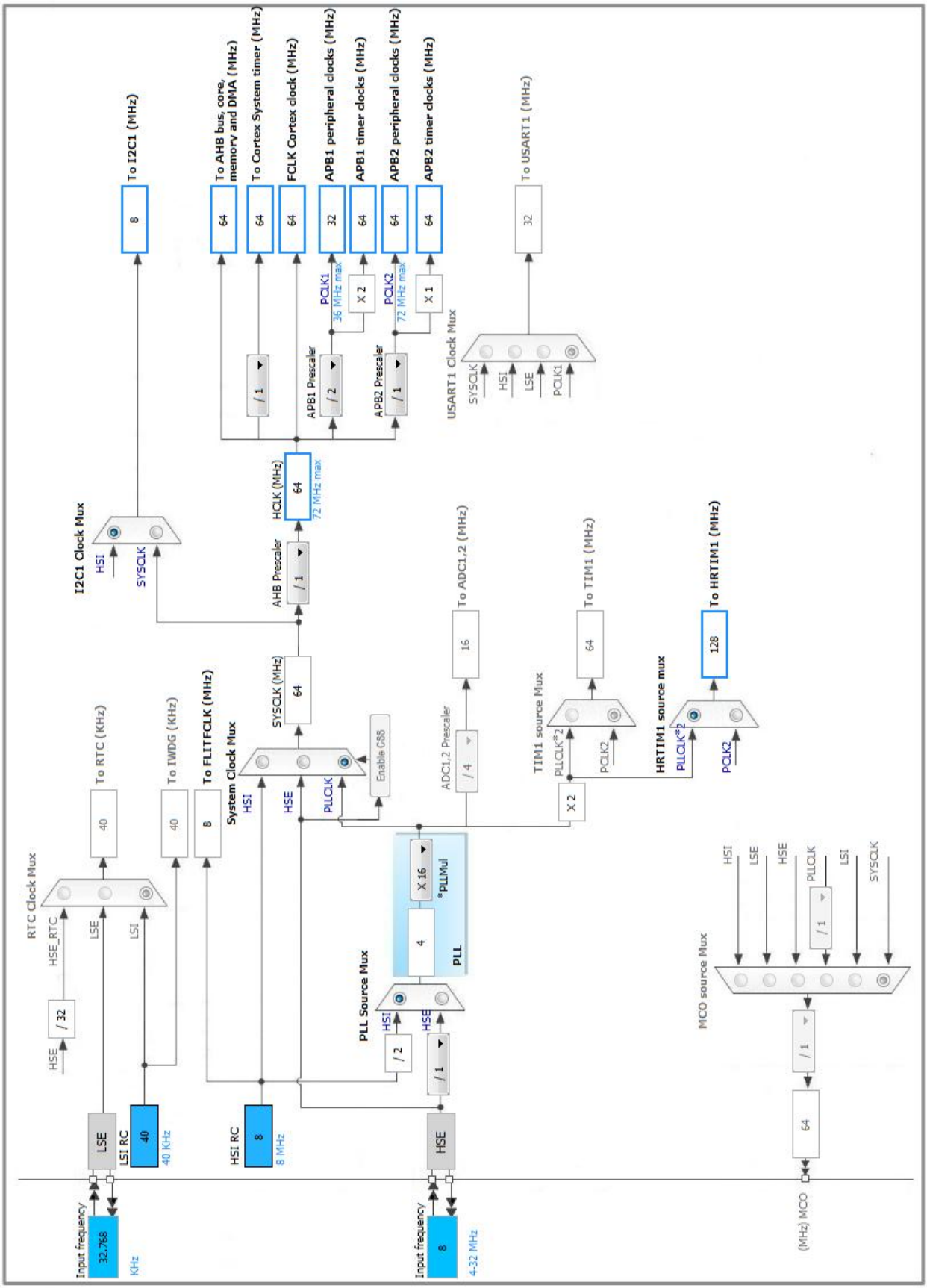
3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
3	PC14 / OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15 / OSC32_OUT	I/O	RCC_OSC32_OUT	
5	PF0 / OSC_IN	I/O	RCC_OSC_IN	
6	PF1 / OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	PC0	I/O	ADC1_IN6	
9	PC1	I/O	ADC1_IN7	
10	PC2	I/O	ADC1_IN8	
12	VSSA/VREF-	Power		
13	VDDA/VREF+	Power		
14	PA0	I/O	ADC1_IN1	
15	PA1	I/O	TIM15_CH1N	
16	PA2	I/O	ADC1_IN3	
17	PA3	I/O	ADC1_IN4	
18	VSS	Power		
19	VDD	Power		
20	PA4	I/O	TIM3_CH2	
21	PA5	I/O	TIM2_CH1	
22	PA6	I/O	TIM3_CH1	
29	PB10	I/O	USART3_TX	
30	PB11	I/O	USART3_RX	
31	VSS	Power		
32	VDD	Power		
33	PB12 *	I/O	GPIO_Output	
34	PB13 *	I/O	GPIO_Output	
35	PB14 *	I/O	GPIO_Output	
36	PB15 *	I/O	GPIO_Output	
37	PC6 *	I/O	GPIO_Output	
41	PA8	I/O	HRTIM1_CHA1	
42	PA9	I/O	HRTIM1_CHA2	
43	PA10	I/O	GPIO_EXTI10	
45	PA12	I/O	TIM16_CH1	
46	PA13	I/O	SYS_JTMS-SWDIO	
47	VSS	Power		
48	VDD	Power		

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
49	PA14	I/O	SYS_JTCK-SWCLK	TCK
51	PC10 *	I/O	GPIO_Output	
53	PC12	I/O	GPIO_EXTI12	
54	PD2 *	I/O	GPIO_Output	
55	PB3	I/O	USART2_TX	
56	PB4	I/O	USART2_RX	
57	PB5	I/O	GPIO_EXTI5	
58	PB6 *	I/O	GPIO_Output	
59	PB7 *	I/O	GPIO_Output	
60	BOOT0	Boot		
61	PB8	I/O	I2C1_SCL	
62	PB9	I/O	I2C1_SDA	
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

IN1: IN1 Single-ended
IN3: IN3 Single-ended
mode: IN4
IN6: IN6 Single-ended
IN7: IN7 Single-ended
IN8: IN8 Single-ended
mode: Temperature Sensor Channel

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**Synchronous clock mode divided by 4 ***
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	**End of sequence of conversion ***
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	**6 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 1
Sampling Time	**7.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**2 ***

Channel	**Channel 3 ***
Sampling Time	**7.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**3 ***
Channel	**Channel 4 ***
Sampling Time	**7.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**4 ***
Channel	**Channel 6 ***
Sampling Time	**7.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**5 ***
Channel	**Channel 7 ***
Sampling Time	**7.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**6 ***
Channel	**Channel Temperature Sensor ***
Sampling Time	**61.5 Cycles ***
Offset Number	No offset
Offset	0

ADC_Injected_ConversionMode:

Enable Injected Conversions	Enable
Number Of Conversions	**1 ***
External Trigger Source	**HRTimer Trigger Out 2 event ***
External Trigger Conversion Edge	Trigger detection on the rising edge
Injected Conversion Mode	None
Queue Injected Context Mode	Injected Queue enabled with Mode 0 (2 contexts, last active)
Rank	1
Channel	**Channel 8 ***
Sampling Time	**4.5 Cycles ***
Offset Number	No offset
Injected Offset	0

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

5.2. HRTIM1

mode: Master Timer Enable

Timer A: TA1 and TA2 outputs active

Timer B: No external Output

5.2.1. HRTIM Interrupt Configuration:

Sources:

1st Source of interrupt	No interrupt enabled
2nd Source of interrupt	No interrupt enabled
3rd Source of interrupt	No interrupt enabled
4th Source of interrupt	No interrupt enabled
5th Source of interrupt	No interrupt enabled
6th Source of interrupt	No interrupt enabled
7th Source of interrupt	No interrupt enabled
8th Source of interrupt	No interrupt enabled

5.2.2. Synchro Configuration:

Master Timer Synchronization:

Sync Options	HRTIM instance doesn't handle external synchronization signals (SYNCIN, SYNCOUT)

5.2.3. High Resolution:

High Resolution Setting:

High Resolution to reach steps down to 217 ps (4.6GHz Equivalent Frequency)	Enabled with Simple DLL Calibration

Calibration Settings:

Calibration Rate	Periodic DLL calibration: T : 2048 mult tHRTIM (0.014 ms)

Polling:

Timeout (in ms)	10

5.2.4. External Event Configuration:

External Event 1:

Event Configuration	Disable

External Event 2:

Event Configuration	Disable

External Event 3:

Event Configuration	Disable

External Event 4:

Event Configuration	Disable

External Event 5:

Event Configuration	Disable

External Event 6:

Event Configuration	Disable

External Event 7:

Event Configuration	Disable

External Event 8:

Event Configuration	Disable

External Event 9:

Event Configuration	Disable

External Event 10:

Event Configuration	Disable

5.2.5. Fault Lines Configuration:

Fault Line 1:

Line Configuration	No Configuration of Fault Line

Fault Line 2:

Line Configuration	No Configuration of Fault Line

Fault Line 3:

Line Configuration	No Configuration of Fault Line

Fault Line 4:

Line Configuration	No Configuration of Fault Line

Fault Line 5:

Line Configuration	No Configuration of Fault Line

5.2.6. ADC Triggers Configuration:

ADC Trigger 1:

ADC Trigger Configuration	Disable

ADC Trigger 2:

ADC Trigger Configuration	**Enable ADC Trigger 2 ***
Update Trigger Source	Master timer
Trigger Sources Selection : Please enter the number of Active Trigger Sources	**1 ***
1st Trigger Source	**ADC Trigger on master compare 2 ***

ADC Trigger 3:

ADC Trigger Configuration	Disable

ADC Trigger 4:

ADC Trigger Configuration	Disable

5.2.7. Burst Mode Configuration:

Burst Mode Enabling:

Burst Mode	Burst mode disabled

5.2.8. Master Timer:

General:

Timer Idx	Master Timer

Time Base Setting:

Prescaler Ratio	**Multiply by 8 - fHRCK: 1.152 GHz for fHRTIM=144MHz ***
Period	**4000 ***
Resulting PWM Period	256000
Repetition Counter	**0 ***
Mode	The timer operates in continuous (free-running) mode

Timing Unit:

Half Mode Enable - The Compare Value of CP Unit 1 is set automatically to half the Timer Period -	**Half mode is enabled - Period has to be set at least twice its Min Value ***
Start On Sync	Synchronization input event has no effect on the timer
Reset On Sync	Synchronization input event has no effect on the timer
Dac Synchro	No DAC synchronization event generated
Preload Enable	**Preload enabled: the write access is done into the preload register ***
Update Gating	Update done independently from the DMA burst transfer completion
Repetition Update	Update on repetition disabled

Burst Mode	Timer counter clock is maintained and the timer operates normally
Interrupt Requests Sources Selection : Please enter the number of Active Interrupt Requests	0
Number of Master Timer Internal DMA Request Sources - you first have to enable the Master Timer DMA Request in the DMA Settings Tab	0

Compare Unit 1:

Compare Unit 1 Configuration	**Enable ***

Compare Unit 2:

Compare Unit 2 Configuration	**Enable ***
Compare Value	**5760 ***

Compare Unit 3:

Compare Unit 3 Configuration	Disable

Compare Unit 4:

Compare Unit 4 Configuration	Disable

Burst DMA Controller:

Burst DMA Configuration	Disable

5.2.9. Timer A:

General:

Timer Idx	Timer A
Basic/Advanced Configuration	Advanced (using HAL_Waveform methods)

Time Base Setting:

Prescaler Ratio	**Multiply by 8 - fHRCK: 1.152 GHz for fHRTIM=144MHz ***
Period	**20000 ***
Resulting PWM Period	51200
Repetition Counter	**0x00 ***
Mode	The timer operates in continuous (free-running) mode

Timing Unit:

Half Mode Enable - The Compare Value of CP Unit 1 is set automatically to half the Timer Period -	Half mode is disabled
Start On Sync	Synchronization input event has no effect on the timer
Reset On Sync	Synchronization input event has no effect on the timer
Dac Synchro	No DAC synchronization event generated
Preload Enable	**Preload enabled: the write access is done into the preload register ***
Update Gating	Update done independently from the DMA burst transfer completion
Repetition Update	Update on repetition disabled
Burst Mode	Timer counter clock is maintained and the timer operates normally

Push Pull	Push-Pull mode disabled
Number of Faults to enable	0
Fault Lock	Timer fault enabling bits are read/write
Dead Time Insertion	Output 1 and output 2 signals are independent
Delayed Protection Mode	No action
Update Trigger Sources Selection : Please enter the number of Triggers to select	0
Reset Update	**Update by Timer reset / roll-over enabled ***
Reset Trigger Sources Selection : Please enter the number of Triggers to select	**1 ***
1st Reset Trigger Source	**The timer counter is reset upon master timer period event ***
Interrupt Requests Sources Selection : Please enter the number of Active Interrupt Requests	0
Number of Timer A Internal DMA Request Sources - you first have to enable the Timer A DMA Request in the DMA Settings Tab	0

Compare Unit 1:

Compare Unit 1 Configuration	**Enable ***
Compare Value	**11520 ***

Compare Unit 2:

Compare Unit 2 Configuration	Disable

Compare Unit 3:

Compare Unit 3 Configuration	Disable

Compare Unit 4:

Compare Unit 4 Configuration	Disable

Burst DMA Controller:

Burst DMA Configuration	Disable

Capture Unit 1:

Capture Unit 1 Configuration	Disable

Capture Unit 2:

Capture Unit 2 Configuration	Disable

External Event 1 Filtering:

Filtering Configuration	Disable

External Event 2 Filtering:

Filtering Configuration	Disable

External Event 3 Filtering:

Filtering Configuration	Disable

External Event 4 Filtering:

Filtering Configuration	Disable

External Event 5 Filtering:

Filtering Configuration	Disable

External Event 6 Filtering:

Filtering Configuration	Disable

External Event 7 Filtering:

Filtering Configuration	Disable

External Event 8 Filtering:

Filtering Configuration	Disable

External Event 9 Filtering:

Filtering Configuration	Disable

External Event 10 Filtering:

Filtering Configuration	Disable

Dead Time:

Dead Time Configuration	Disable

Output 1 Configuration:

Output1 Configuration	TA1
Polarity	Output is active HIGH
Set Source Selection : Please enter the number of Active Set Sources	**1 ***
1st Set Source	**The master timer period event forces the output to its active state ***
Reset Source Selection : Please enter the number of Active Reset Sources	**1 ***
1st Reset Source	**Timer compare 1 event forces the output to its inactive state ***
Idle Mode	The output is not affected by the burst mode operation
Idle Level	Output at inactive level when in IDLE state
Fault Level	The output is not affected by the fault input
Chopper Mode Enable	Output signal is not altered
Burst Mode Entry Delayed	The programmed Idle state is applied immediately to the Output

Output 2 Configuration:

Output2 Configuration	TA2
Polarity	Output is active HIGH
Set Source Selection : Please enter the number of Active Set Sources	**1 ***
1st Set Source	**Master Timer compare 1 event forces the output to its active state ***
Reset Source Selection : Please enter the number of Active Reset Sources	**1 ***
1st Reset Source	**Timer event 1 (Timer B CMP1) forces the output to its inactive state ***
Idle Mode	The output is not affected by the burst mode operation
Idle Level	Output at inactive level when in IDLE state

Fault Level	The output is not affected by the fault input
Chopper Mode Enable	Output signal is not altered
Burst Mode Entry Delayed	The programmed Idle state is applied immediately to the Output

Chopper Mode:

Chopper Mode Configuration	Disable

5.2.10. Timer B:

General:

Timer Idx	Timer B
Basic/Advanced Configuration	Advanced (using HAL_Waveform methods)

Time Base Setting:

Prescaler Ratio	**Multiply by 8 - fHRCK: 1.152 GHz for fHRTIM=144MHz ***
Period	**20000 ***
Resulting PWM Period	51200
Repetition Counter	**0x00 ***
Mode	The timer operates in continuous (free-running) mode

Timing Unit:

Half Mode Enable - The Compare Value of CP Unit 1 is set automatically to half the Timer Period -	Half mode is disabled
Start On Sync	Synchronization input event has no effect on the timer
Reset On Sync	Synchronization input event has no effect on the timer
Dac Synchro	No DAC synchronization event generated
Preload Enable	**Preload enabled: the write access is done into the preload register ***
Update Gating	Update done independently from the DMA burst transfer completion
Repetition Update	Update on repetition disabled
Burst Mode	Timer counter clock is maintained and the timer operates normally
Push Pull	Push-Pull mode disabled
Number of Faults to enable	0
Fault Lock	Timer fault enabling bits are read/write
Dead Time Insertion	Output 1 and output 2 signals are independent
Delayed Protection Mode	No action
Update Trigger Sources Selection : Please enter the number of Triggers to select	0
Reset Update	**Update by Timer reset / roll-over enabled ***
Reset Trigger Sources Selection : Please enter the number of Triggers to select	**1 ***
1st Reset Trigger Source	**The timer counter is reset upon master timer Compare 1 event ***
Interrupt Requests Sources Selection : Please enter	0

the number of Active Interrupt Requests	
Number of Timer B Internal DMA Request Sources - you first have to enable the Timer B DMA Request in the DMA Settings Tab	0

Compare Unit 1:

Compare Unit 1 Configuration	**Enable ***
Compare Value	**11520 ***

Compare Unit 2:

Compare Unit 2 Configuration	Disable

Compare Unit 3:

Compare Unit 3 Configuration	Disable

Compare Unit 4:

Compare Unit 4 Configuration	Disable

Burst DMA Controller:

Burst DMA Configuration	Disable

Capture Unit 1:

Capture Unit 1 Configuration	Disable

Capture Unit 2:

Capture Unit 2 Configuration	Disable

External Event 1 Filtering:

Filtering Configuration	Disable

External Event 2 Filtering:

Filtering Configuration	Disable

External Event 3 Filtering:

Filtering Configuration	Disable

External Event 4 Filtering:

Filtering Configuration	Disable

External Event 5 Filtering:

Filtering Configuration	Disable

External Event 6 Filtering:

Filtering Configuration	Disable

External Event 7 Filtering:

Filtering Configuration	Disable

External Event 8 Filtering:

Filtering Configuration	Disable

External Event 9 Filtering:

Filtering Configuration	Disable

External Event 10 Filtering:

Filtering Configuration	Disable

5.3. I2C1

I2C: I2C

5.3.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x2000090E

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

5.4. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

5.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

5.5. SYS

Debug: Serial Wire

Timebase Source: SysTick

5.6. TIM2

Channel1: PWM Generation CH1

5.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**2559 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (32 bits value)	**255 ***
Fast Mode	Disable
CH Polarity	High

5.7. TIM3

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

5.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

5.8. TIM6

mode: Activated

5.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**2559 ***
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.9. TIM15

mode: Clock Source
Channel1: PWM Generation CH1N

5.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1N:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CHN Polarity	High
CHN Idle State	Reset

5.10. TIM16

mode: Activated
Channel1: PWM Generation CH1

5.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

5.11. TIM17

mode: Activated

5.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**2559 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

5.12. USART2

Mode: Asynchronous

5.12.1. Parameter Settings:

Basic Parameters:

Baud Rate	38400
Word Length	7 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

5.13. USART3

Mode: Asynchronous

5.13.1. Parameter Settings:

Basic Parameters:

Baud Rate	38400
Word Length	7 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

TX Pin Active Level Inversion	Disable

RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_IN6	Analog mode	No pull up pull down	n/a	
	PC1	ADC1_IN7	Analog mode	No pull up pull down	n/a	
	PC2	ADC1_IN8	Analog mode	No pull up pull down	n/a	
	PA0	ADC1_IN1	Analog mode	No pull up pull down	n/a	
	PA2	ADC1_IN3	Analog mode	No pull up pull down	n/a	
	PA3	ADC1_IN4	Analog mode	No pull up pull down	n/a	
HRTIM1	PA8	HRTIM1_CHA1	Alternate Function Push Pull	No pull up pull down	High	
	PA9	HRTIM1_CHA2	Alternate Function Push Pull	No pull up pull down	High	
I2C1	PB8	I2C1_SCL	Alternate Function Open Drain	Pull up	**High ***	
	PB9	I2C1_SDA	Alternate Function Open Drain	Pull up	**High ***	
RCC	PC14 / OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15 / OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PF0 / OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PF1 / OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	TCK
TIM2	PA5	TIM2_CH1	Alternate Function Push Pull	No pull up pull down	Low	
TIM3	PA4	TIM3_CH2	Alternate Function Push Pull	No pull up pull down	Low	
	PA6	TIM3_CH1	Alternate Function Push Pull	No pull up pull down	Low	
TIM15	PA1	TIM15_CH1N	Alternate Function Push Pull	No pull up pull down	Low	
TIM16	PA12	TIM16_CH1	Alternate Function Push Pull	No pull up pull down	Low	
USART2	PB3	USART2_TX	Alternate Function Push Pull	Pull up	**High ***	
	PB4	USART2_RX	Alternate Function Push Pull	Pull up	**High ***	
USART3	PB10	USART3_TX	Alternate Function Push Pull	Pull up	**High ***	
	PB11	USART3_RX	Alternate Function Push Pull	Pull up	**High ***	
GPIO	PB12	GPIO_Output	Output Push Pull	No pull up pull down	Low	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PB13	GPIO_Output	Output Push Pull	No pull up pull down	Low	
	PB14	GPIO_Output	Output Push Pull	No pull up pull down	Low	
	PB15	GPIO_Output	Output Push Pull	No pull up pull down	Low	
	PC6	GPIO_Output	Output Push Pull	No pull up pull down	Low	
	PA10	GPIO_EXTI10	External Interrupt Mode with Rising edge trigger detection	No pull up pull down	n/a	
	PC10	GPIO_Output	Output Push Pull	No pull up pull down	Low	
	PC12	GPIO_EXTI12	External Interrupt Mode with Rising edge trigger detection	No pull up pull down	n/a	
	PD2	GPIO_Output	Output Push Pull	No pull up pull down	Low	
	PB5	GPIO_EXTI5	External Interrupt Mode with Rising edge trigger detection	No pull up pull down	n/a	
	PB6	GPIO_Output	Output Push Pull	No pull up pull down	Low	
	PB7	GPIO_Output	Output Push Pull	No pull up pull down	Low	

6.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Channel1	Peripheral To Memory	Low

ADC1: DMA1_Channel1 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Word ***
Memory Data Width:	**Word ***

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel1 global interrupt	true	0	1
ADC1 and ADC2 interrupts	true	0	0
TIM1 trigger and commutation and TIM17 interrupts	true	0	1
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
EXTI line[9:5] interrupts	unused		
TIM1 break and TIM15 interrupts	unused		
TIM1 update and TIM16 interrupts	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
I2C1 event global interrupt / I2C1 wake-up interrupt through EXT line 23	unused		
I2C1 error interrupt	unused		
USART2 global interrupt / USART2 wake-up interrupt through EXT line 26	unused		
USART3 global interrupt / USART3 wake-up interrupt through EXT line 28	unused		
EXTI line[15:10] interrupts	unused		
TIM6 global and DAC1 underrun error interrupts	unused		
HRTIM master timer global interrupt	unused		
HRTIM timer A global interrupt	unused		
HRTIM timer B global interrupt	unused		
HRTIM fault global interrupt	unused		
Floating point unit interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F3
Line	STM32F334
MCU	STM32F334R8Tx
Datasheet	025409_Rev6

7.2. Parameter Selection

Temperature	25
Vdd	3.6

8. Software Project

8.1. Project Settings

Name	Value
Project Name	HRTIM_test_master
Project Folder	D:\Project\3SL_NODE_ORIGINAL\LT.LED0038.16_FW
Toolchain / IDE	EWARM
Firmware Package Name and Version	STM32Cube FW_F3 V1.9.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No