CECS 460 Lab 5 (Matrix Determinant)

Objectives

- Setup and introduction to XilinxVivado
- Review Verilog
- Review synthesis and creating a bit file to load onto an FPGA
- Introduce Design and IP

Introduction

In this lab, we will synthesize and run Verilog code that calculates the determinant of a preloaded 3x3 matrix on an FPGA.

$$A = \begin{bmatrix} a & b & c \\ d & e & f \\ g & h & i \end{bmatrix} \quad |A| = a(ei - fh) - b(di - fg) + c(dh - eg)$$

Determinant of 3x3 matrix

$$A = \begin{pmatrix} 3 & 2 & 4 \\ 2 & 0 & 2 \\ 4 & 2 & 3 \end{pmatrix}$$

$$3\big((0*3)-(2*2)\big)-2\big((2*3)-(4*2)\big)+4\big((2*2)-(4*0)\big)=8$$

$$3(0-4)-2(6-8)+4(4-0)=8$$

$$3(-4)-2(-2)+4(4)=8$$

$$-12+4+16=8$$

$$Det(A)=8$$

Lab Description:

In this lab, you will be able to calculate the determinant of four predefined matrices. The matrix is selected by toggling the board's switches(SW).

0	0	0		1	0	0		16	21	23	
0	0	0		0	1	0		20	0	20	
0	0	0		0	0	1		12	29	18	
								16	21	23	
								20	0	20	
								12	1	18	

$$DET(A)=0: SW=0$$

$$DET(B)=1: SW=1$$

$$DET(C)=1540: SW=2$$

$$DET(D)=-2380: SW=3$$

The determinant of each matrix will be outputted onto the Nexys4DDR's 16 led display in binary. Since determinants are integers, the range of our led display is calculated by

$$-(2^{n-1}) \rightarrow (2^{n-1}-1)$$

$$n=16, number\ of\ bits$$

$$-32768 \rightarrow 32767$$

Figure 1: Det(A) = 8 from introduction example one b'0000000000001000

Figure 2: -145 displayed in binary

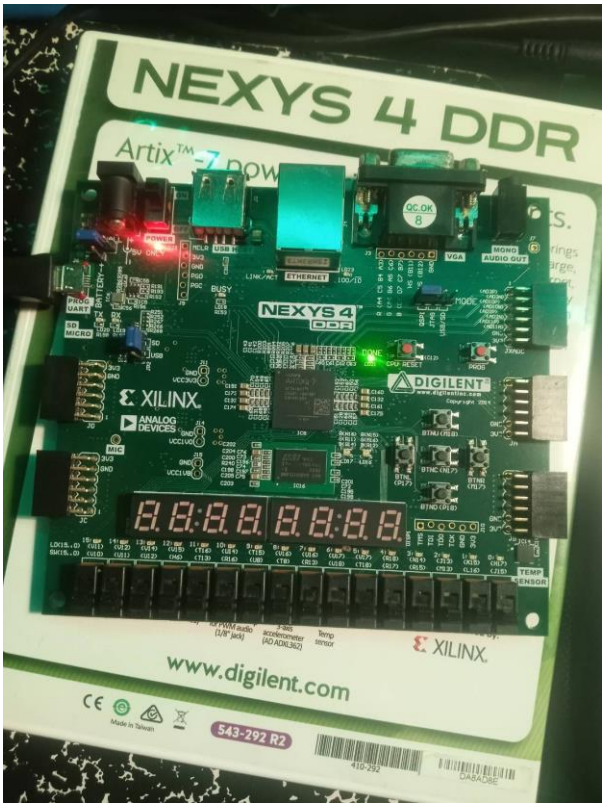


Figure 3: DET(A) = 0 =16'b0. SW = 3'b00

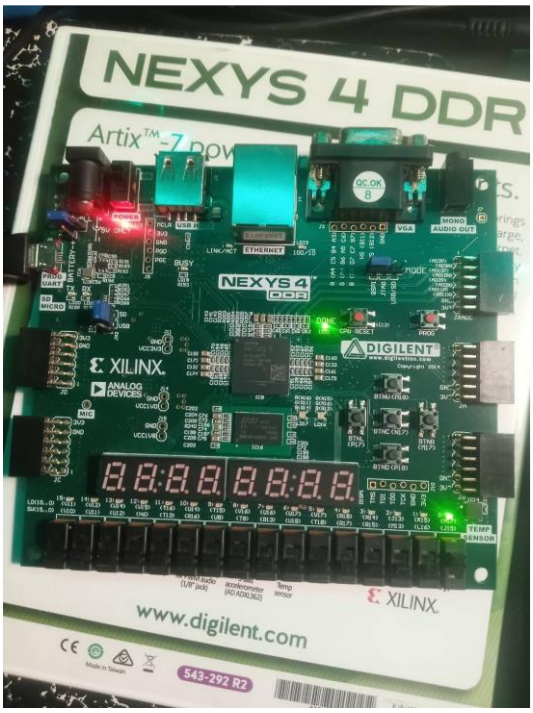


Figure 4: DET(B) = 1 = 16'b1. SW = 3'b01

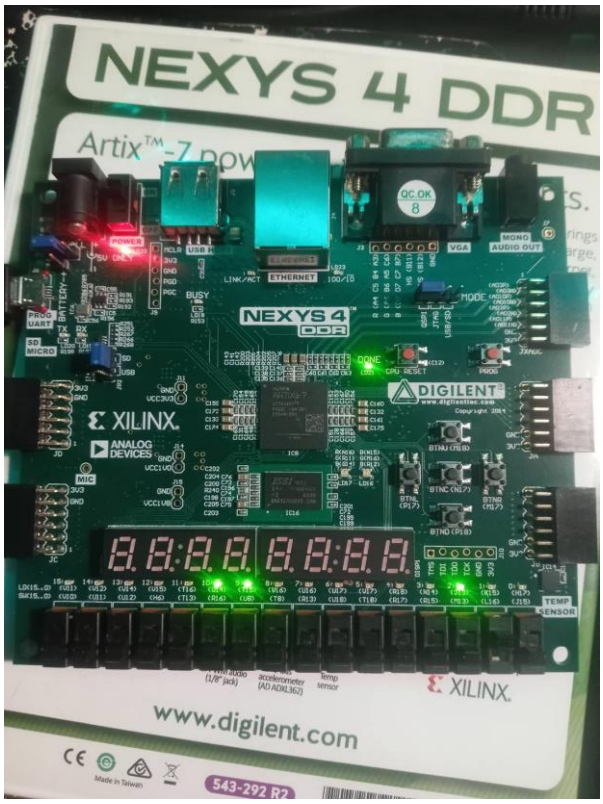


Figure 5: DET(C) = 1540 = 12'b11000000100. SW = 3'b10

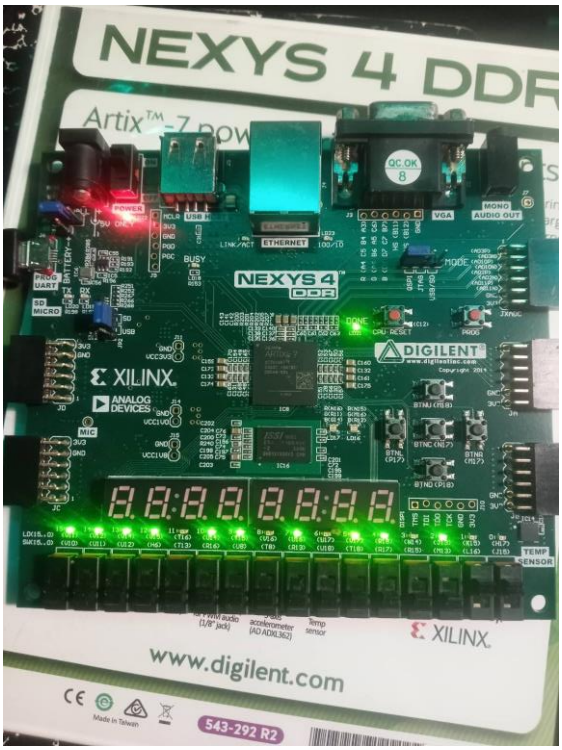


Figure 6: DET(D) = -2380 = 16'b11110110101101. SW = 3'b11

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

When displaying signed integers in binary, the MSB (most significant bit) Is reserved for the integer's sign. The remaining bits are for the integer's magnitude. To get the binary output of a negative integer take the 2's complement of the magnitude.

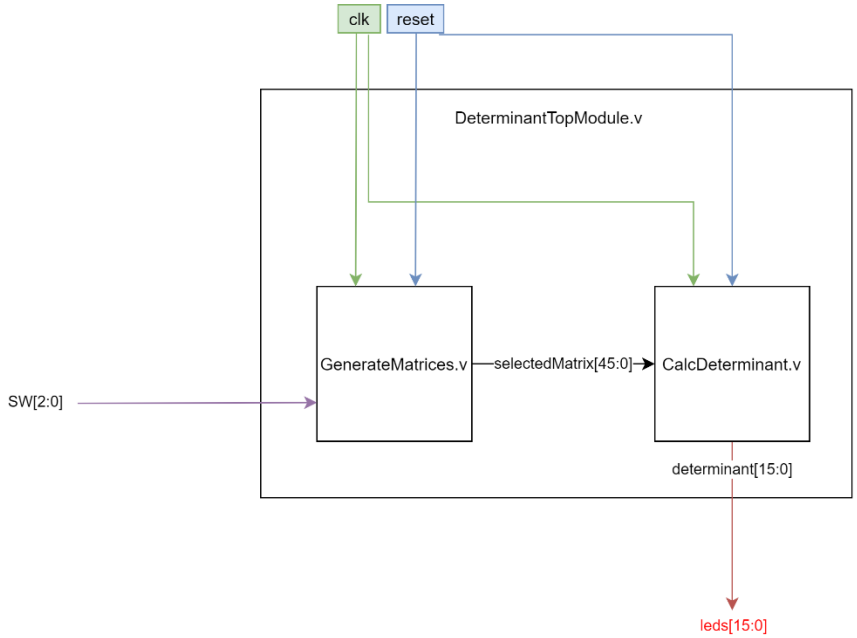


Figure 7:Block Diagram

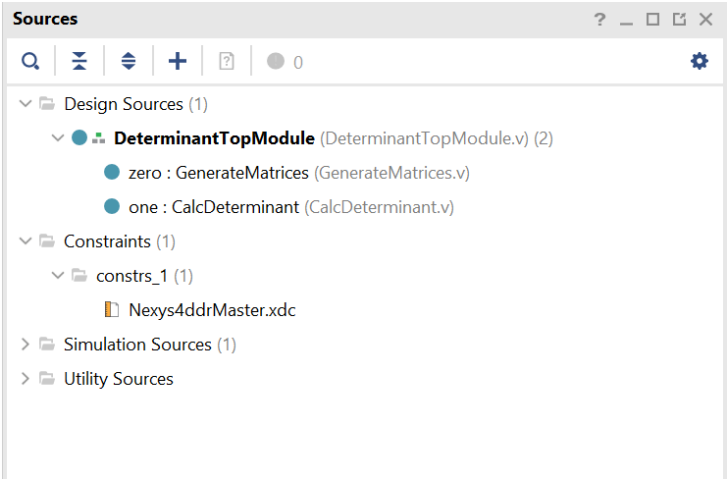


Figure 8: Project sources view in vivado with constraint file

Setup

- Start a project
  - Open Vivado
  - Create a new project with your board
  - Click the plus sign on the sources project view

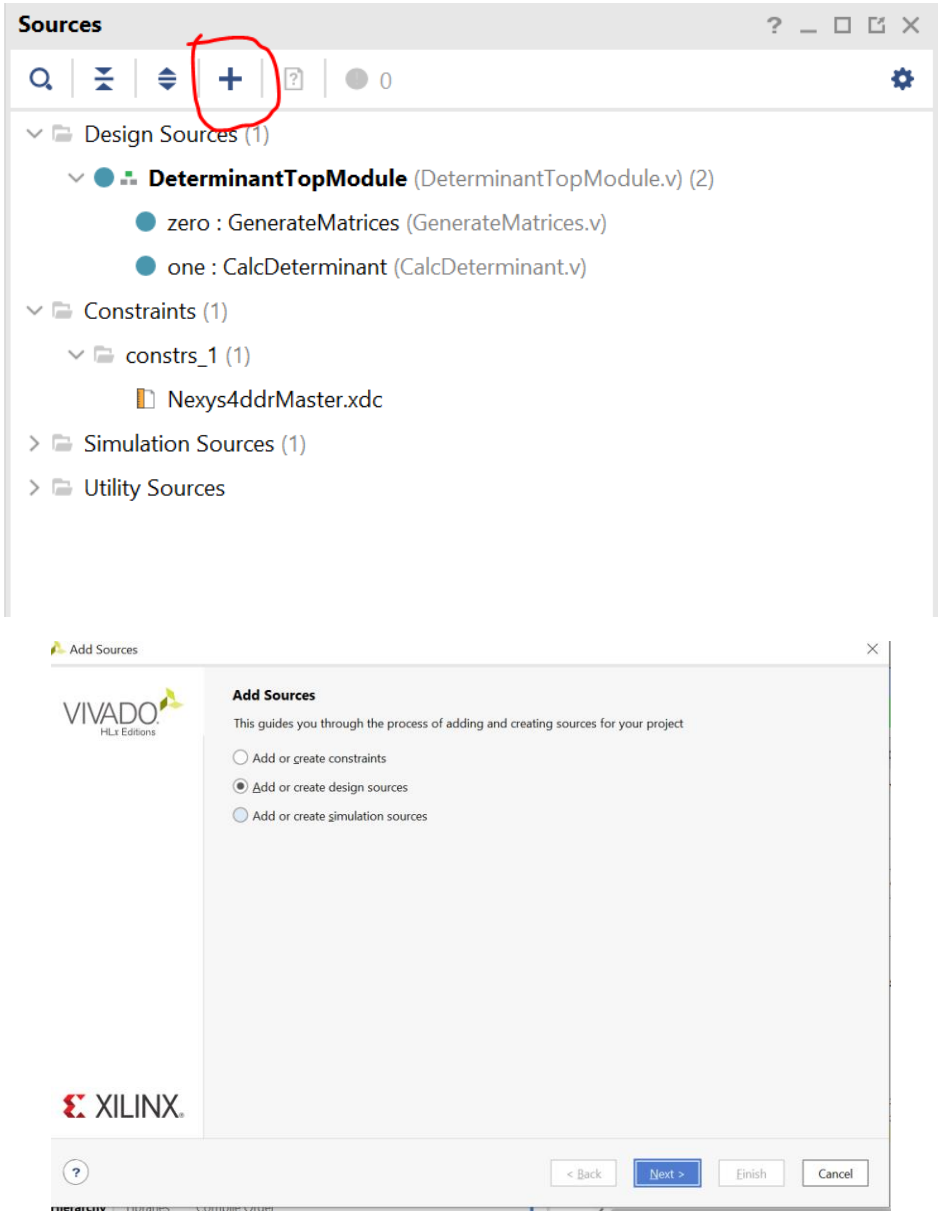
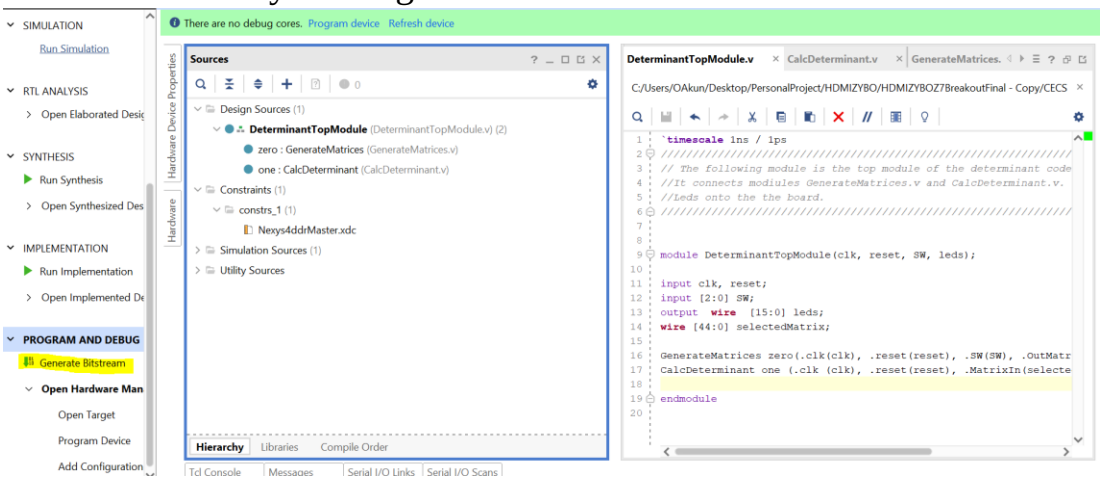
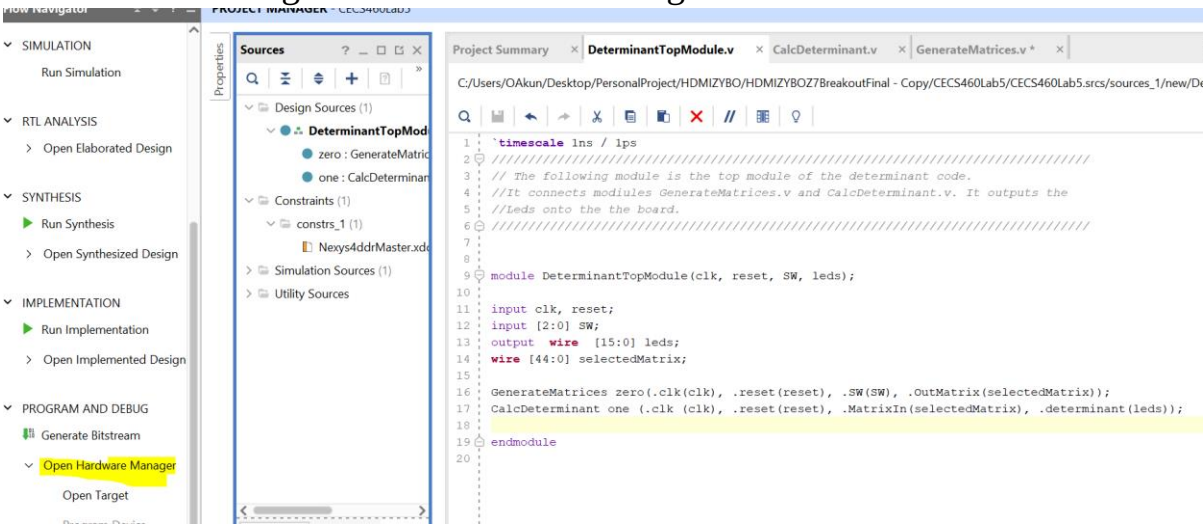
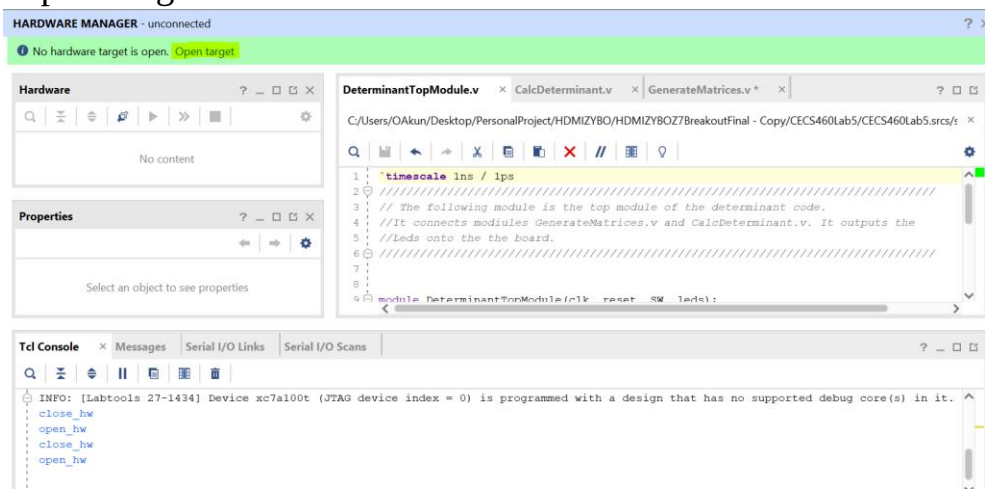


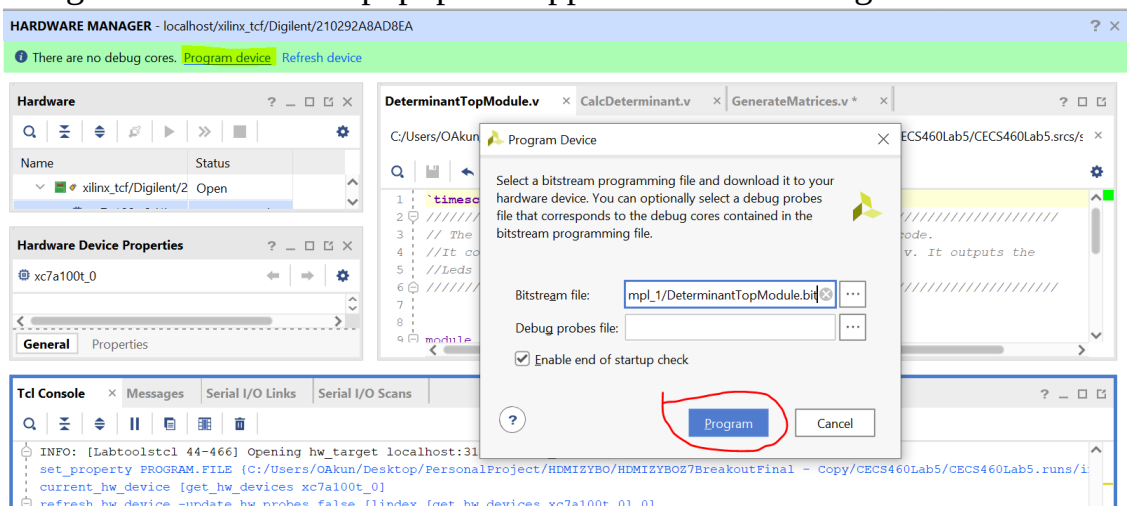
Figure 9: click "Add or create design sources" to add Verilog files." Add or create constraints" to add (.xdc) file

- Once all files are added you can generate the bitstream.
  - 

- Open the hardware manager when the bitstream is generated
  - 

- Click “Open Target”
  - 

  - Click “Recent Targets” or “autoconnect” (Make sure your board is connected)

- Click “Program Device” after popup will appear and click “Program”
  - 

What you can do?

1. Setup and successfully run the program.
2. Add 4 other matrices.
3. Add more switch inputs.
4. Attempt to go over the range 16-bit signed range. (Overflow)
5. Change the default matrices.
6. Perform another operation on the matrices Addition, Subtraction, etc. via switches.
7. What are the benefits of using a behavioral block to do multiple operations in one clock cycle?
8. Create a testbench to see at what point is the determinant calculated theoretically. How many clock cycles does it take?
9. Send the matrix differently. Is there a better way?
10. Add determinant support for a 2X2 matrix.
11. Study the code.