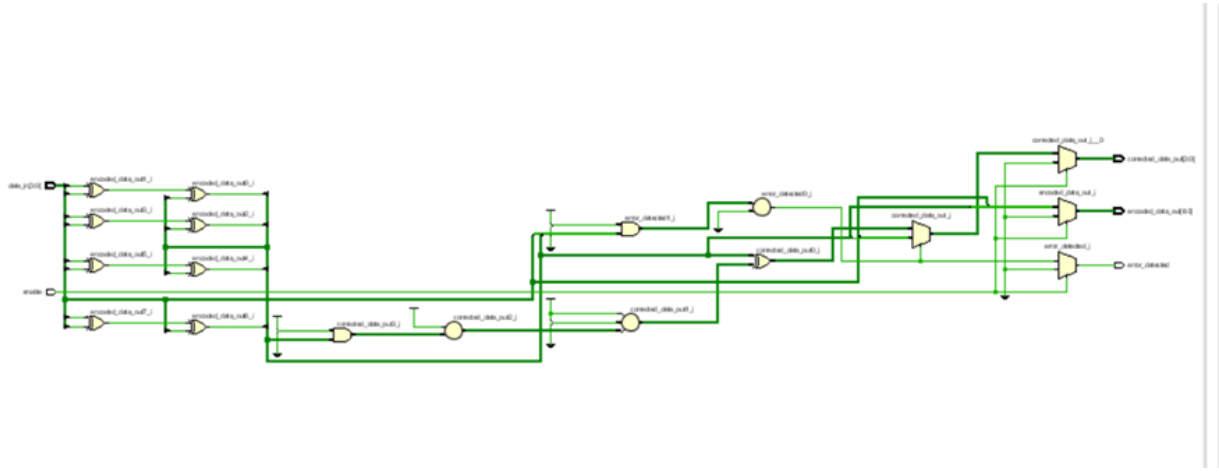

Fig.1 Schematic Simulation System Structure of VHDL

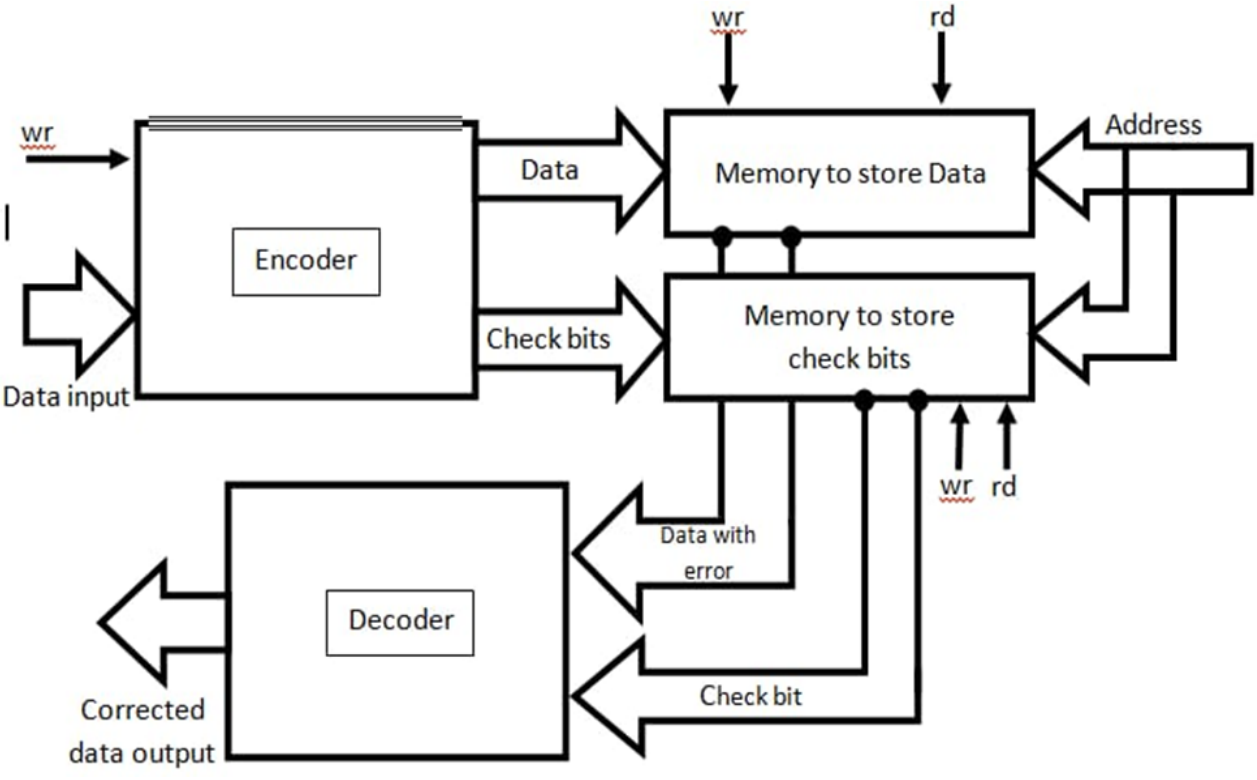

Fig.2 Block diagram of ECC code.

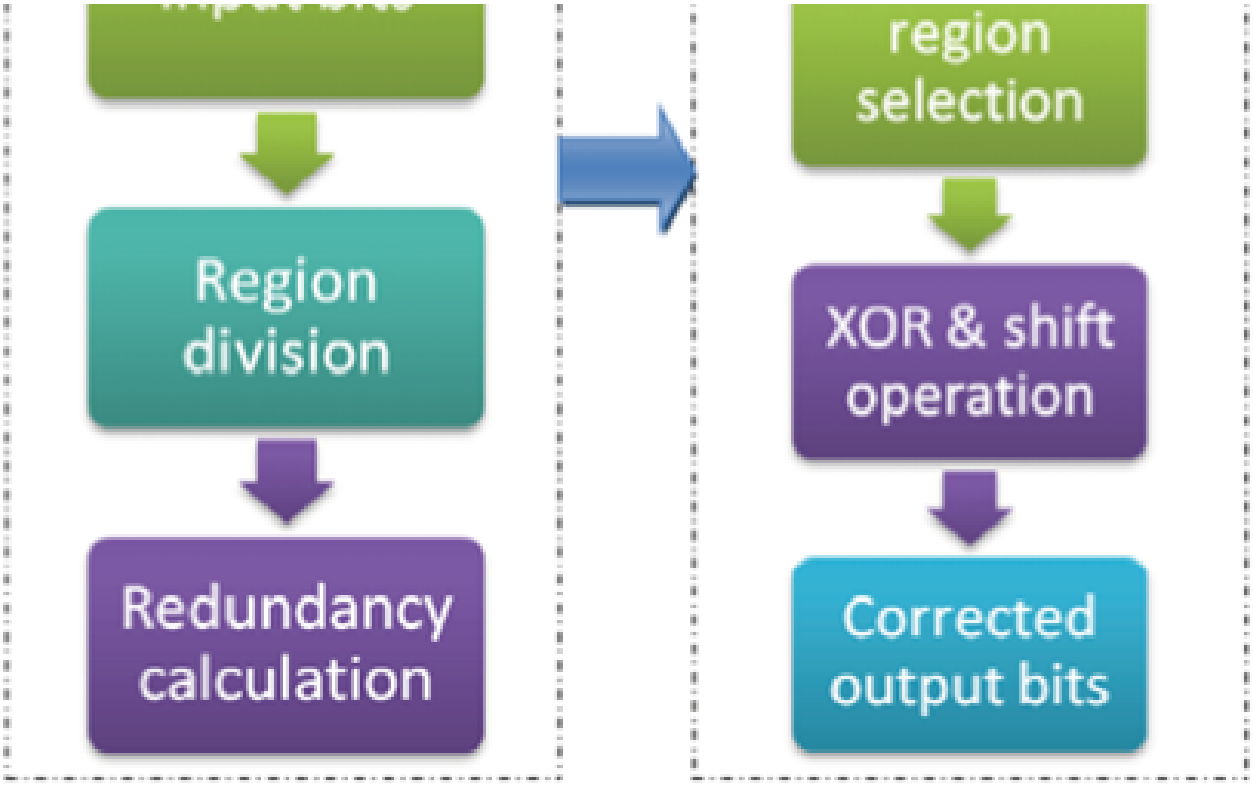

Fig. 3 ECC methodology.