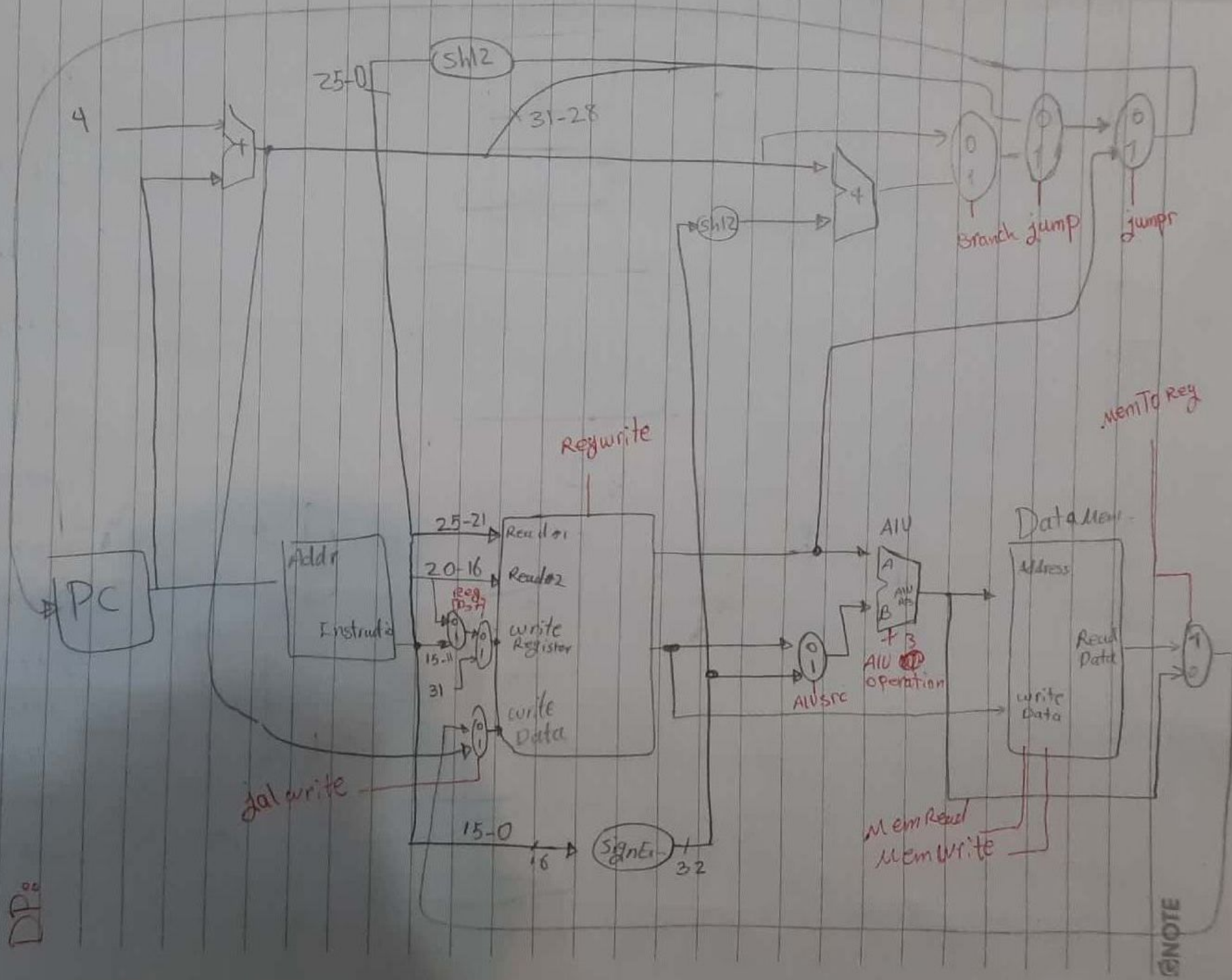


DP



	OpC	RegDst	RegWrite	ALUSrc	MemRead	MemWrite	MemToReg	ALUOp	Branch	Jump	Jump & Branch Write	Jal Write
add	000000	01	1	0	0	0	0	00	0	0	0	0
Sub	000000	01	1	0	0	0	0	01	0	0	0	0
and	000000	01	1	0	0	0	0	11	0	0	0	0
or	000000	01	1	0	0	0	0	11	0	0	0	0
Slt	000000	01	1	0	0	0	0	10	0	0	0	0
addi	000001	01	1	1	0	0	0	00	0	0	0	0
Slti	000010	01	1	1	0	0	0	10	0	0	0	0
lw	000011	00	1	1	1	0	1	00	0	0	0	0
Sw	000100	00(X)	0	1	0	1	0	00	0	0	0	0
beq	000101	00(X)	0	0	0	0	0	01	1	0	0	0
J	000110	00(X)	0	0	0	0	0	X	0	1	0	0
Jr	000111	00(X)	0	0	0	0	0	X	0	0	1	0
Jal	0001000	10	1	0	0	0	0	X	0	1	0	1