



Saeed Safari
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	RegDst	RegWrite	AluSrc	MemRead	MemWrite	MemToReg	Branch	ALUOp	Jmp
RT	1	1	0	0	0	0	0	10	0
lw	0	1	1	1	0	1	0	00	0
sw	X	0	1	0	1	X	0	00	0
beq	X	0	0	0	0	X	1	01	0
addi	00	1	1	0	0	0	0	00	0
j	00	0	0	0	0	0	0	00	1
jal	10	1	0	0	0	0	0	00	1
jr (jr = 1)	00	0	0	0	0	0	0	00	1
slt	01	1	0	0	0	0	0	10	0
slti	00	1	1	0	0	0	0	11	0

For jal and (slt & slti), new signal data_to_write is added and is set at 1 and 2 respectively.