

ZCU106 IP Integrator Application

June 2018



XTP493

Revision History

Date	Version	Description
06/18/18	3.0	Updated for 2018.2. AR71127 fixed.
05/22/18	2.1	Added AR71127. Update Board Flow files as detailed in this Answer Record.
05/07/18	2.0	Updated for 2018.1.
12/20/17	1.0	Initial version.

© Copyright 2018 Xilinx, Inc. Xilinx, the Xilinx logo, Artix, ISE, Kintex, Spartan, Virtex, Vivado, Zynq, and other designated brands included herein are trademarks of Xilinx in the United States and other countries. All other trademarks are the property of their respective owners.

NOTICE OF DISCLAIMER: The information disclosed to you hereunder (the “Information”) is provided “AS-IS” with no warranty of any kind, express or implied. Xilinx does not assume anyliabilityarising from your use of the Information. You are responsible for obtaining anyrights you may require for your use of this Information. Xilinx reserves the right to make changes, at any time, to the Information without notice and at its sole discretion. Xilinx assumes no obligation to correct any errors contained in the Information or to advise you of any corrections or updates. Xilinx expressly disclaims anyliabilityin connection with technical support or assistance that may be provided to you in connection with the Information. XILINX MAKES NO OTHER WARRANTIES, WHETHER EXPRESS, IMPLIED, OR STATUTORY, REGARDING THE INFORMATION, INCLUDING ANY WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NONINFRINGEMENT OF THIRD-PARTY RIGHTS.

Overview

- > **ZCU106 Board Self Test Demo**
- > **Xilinx ZCU106 Board**
- > **Software Requirements**
- > **ZCU106 Setup**
- > **ZCU106 IPI Design**
- > **Compile ZCU106 IPI Design**
- > **Program ZCU106**
 - » Programming the ZCU106 with Dual QSPI
 - » Programming the ZCU106 from Vivado
- > **Run the LwIP Ethernet Design**
- > **References**

ZCU106 IPI Design Description

> Description

- » The IP Integrator (IPI) application uses an MicroBlaze system to verify board functionality. A UART based terminal program interface offers users a menu of tests to run.

> Block Design Source

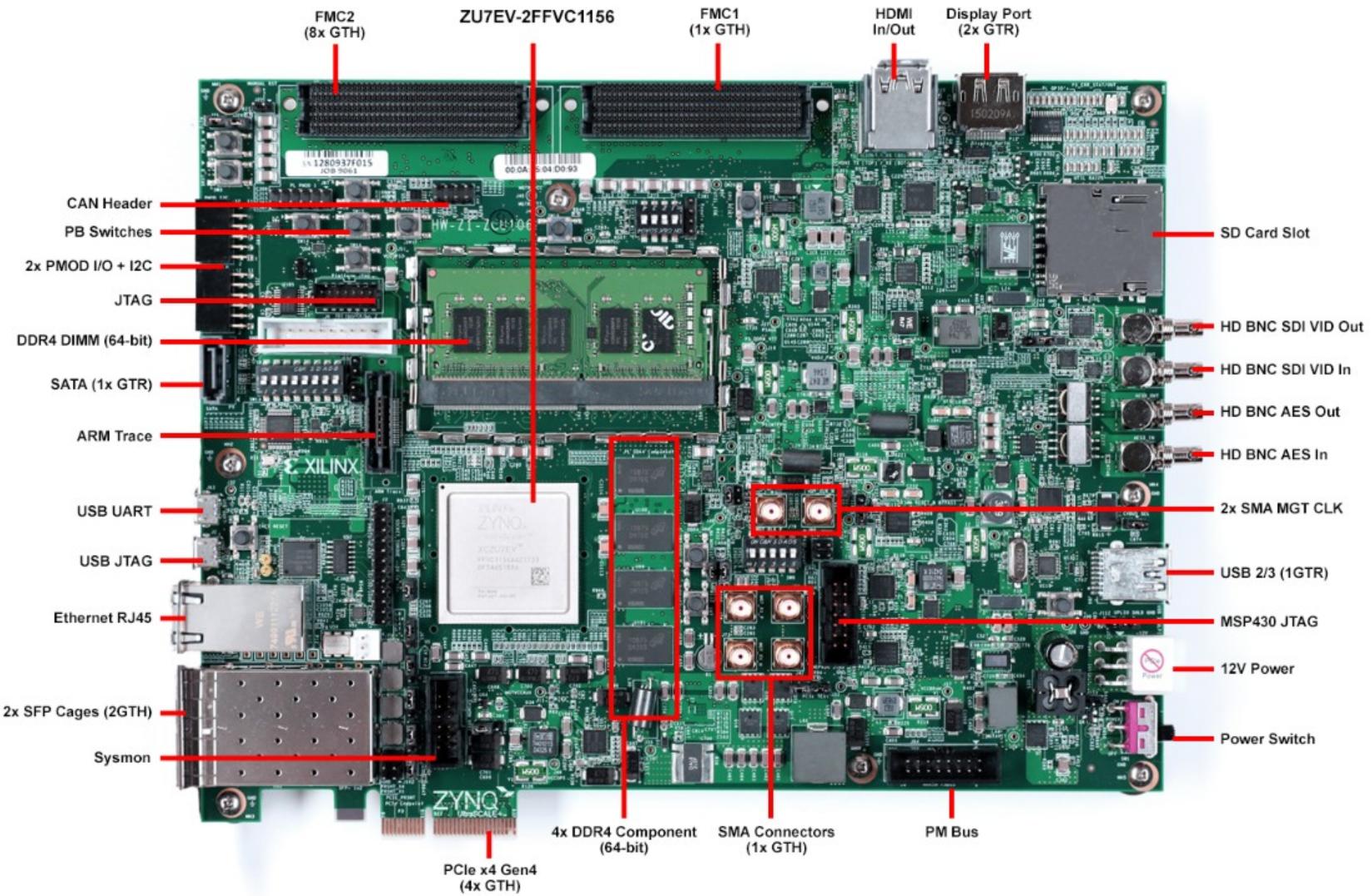
- » RDF0448 – ZCU106 IPI Design Files (2018.2 C) ZIP file

ZCU106 IPI Design Description

> Block Design IP

- » Processor and Subsystems: Zynq UltraScale+ MPSoC, Processor System Reset, Concat
- » AXI Bus: AXI Interconnect
- » Memory: DDR4 SDRAM (MIG), AXI BRAM Controller, Block Memory Generator
- » Peripherals: AXI IIC, AXI GPIO, AXI UART16550, System Management Wizard
- » Other IP: diff_freq_counter, gt_freq_counter, Clocking Wizard, ILA
 - [Vivado Design Suite Tcl Command Reference Guide](#) (UG835)
 - [Designing IP Subsystems Using IP Integrator](#) (UG994)

Xilinx ZCU106 Board



ZCU106 Software Install and Board Setup

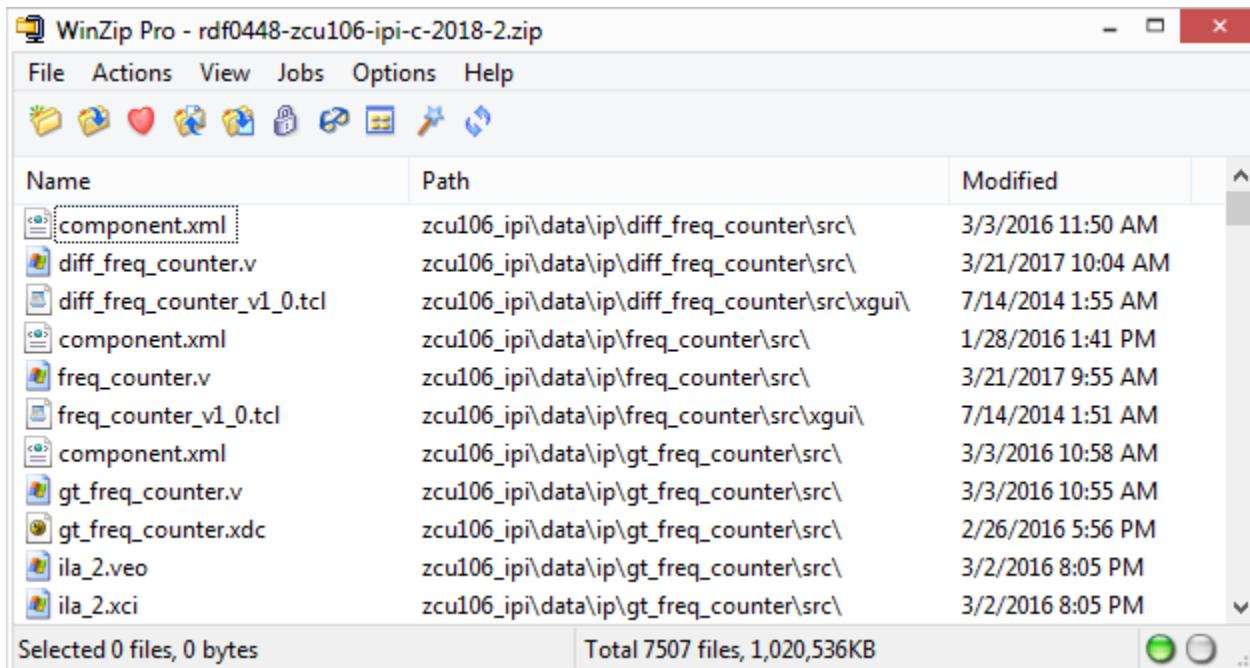
> Refer to XTP497 – ZCU106 Software Install and Board Setup for details on:

- » Software Requirements
- » ZCU106 Board Setup
- » UART Driver Install
- » Optional Hardware Setup



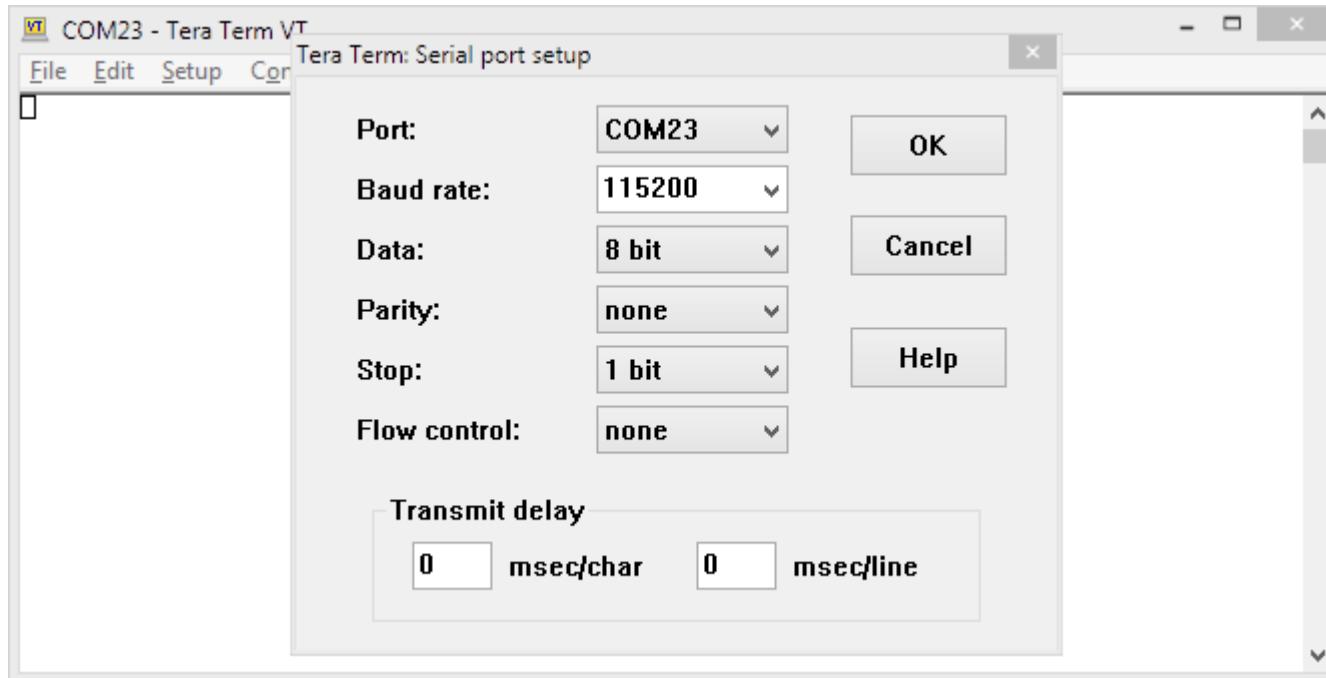
ZCU106 Setup

- > Unzip the RDF0448 - ZCU106 IPI Design Files (2018.2 C) ZIP file, and extract to your C:\ drive:



ZCU106 Setup

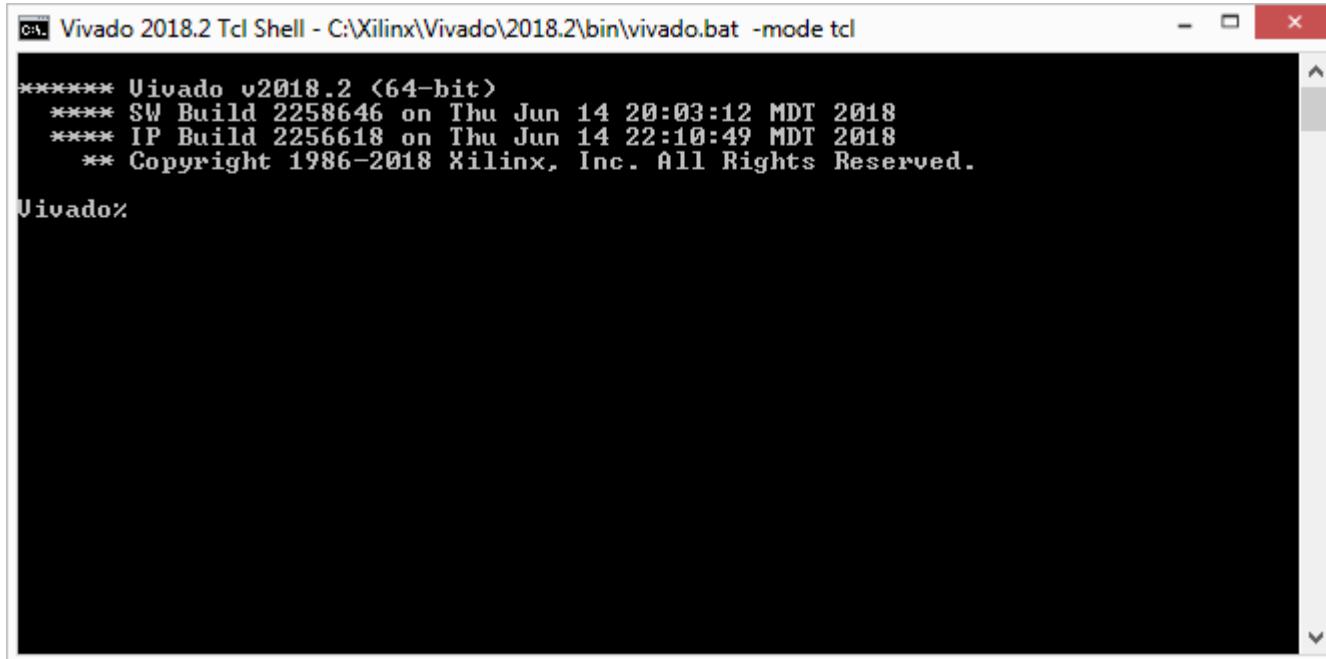
- > Open a Tera Term window for the Interface 0 COM Port
- > Set the baud to 115200



ZCU106 IPI Design

> Open a Vivado Tcl Shell:

Start → All Programs → Xilinx Design Tools → Vivado 2018.2 →
Vivado 2018.2 Tcl Shell



Vivado 2018.2 Tcl Shell - C:\Xilinx\Vivado\2018.2\bin\vivado.bat -mode tcl

```
***** Vivado v2018.2 (64-bit)
***** SW Build 2258646 on Thu Jun 14 20:03:12 MDT 2018
***** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018
** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.
```

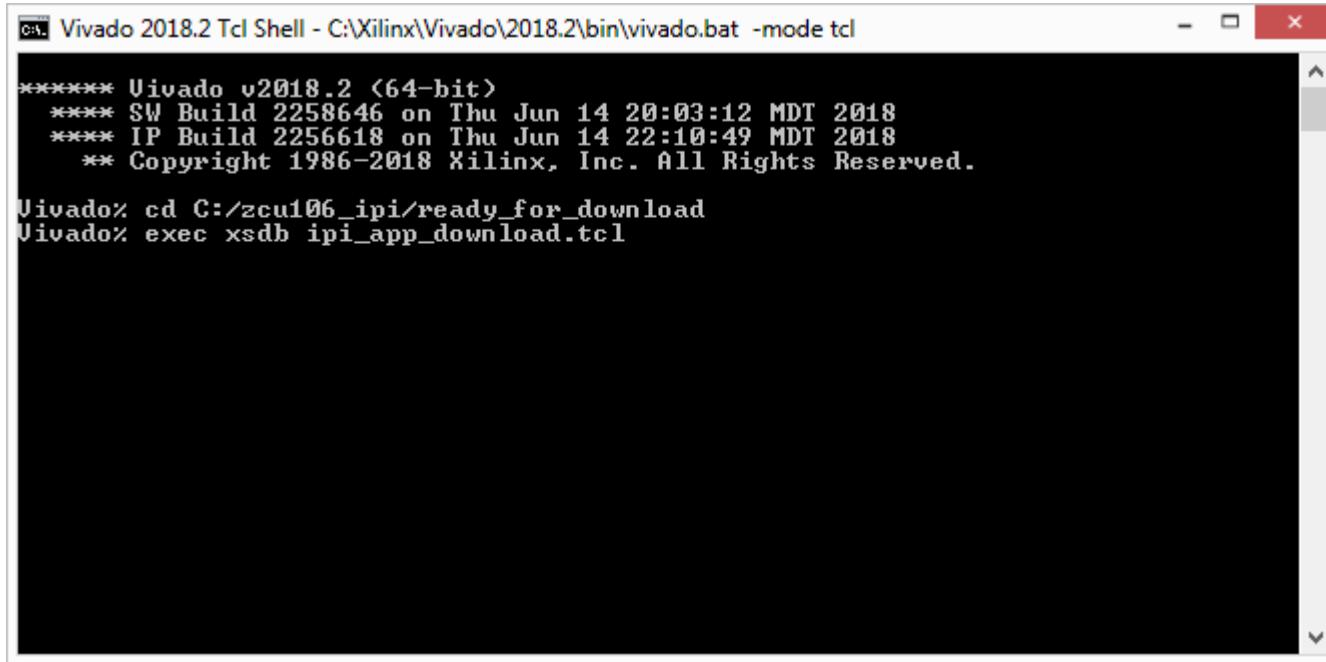
Vivado>

ZCU106 IPI Design

> Download the blink bitstream

> In the Vivado Tcl Shell type:

```
cd C:/zcu106_ipi/ready_for_download  
exec xsdb ipi_app_download.tcl
```

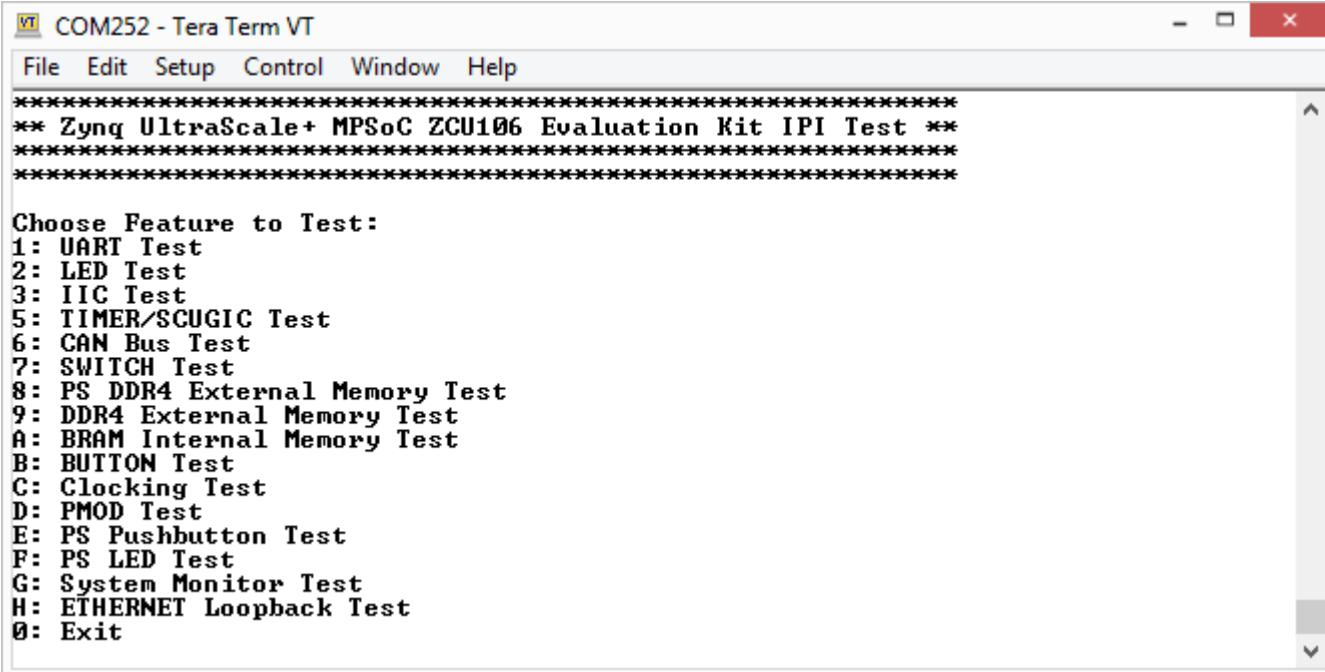


The screenshot shows a Windows command-line interface window titled "Vivado 2018.2 Tcl Shell - C:\Xilinx\Vivado\2018.2\bin\vivado.bat -mode tcl". The window displays the following text:

```
***** Vivado v2018.2 (64-bit)  
***** SW Build 2258646 on Thu Jun 14 20:03:12 MDT 2018  
***** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018  
** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.  
  
Vivado> cd C:/zcu106_ipi/ready_for_download  
Vivado> exec xsdb ipi_app_download.tcl
```

ZCU106 IPI Design

> View the initial IPI Test screen



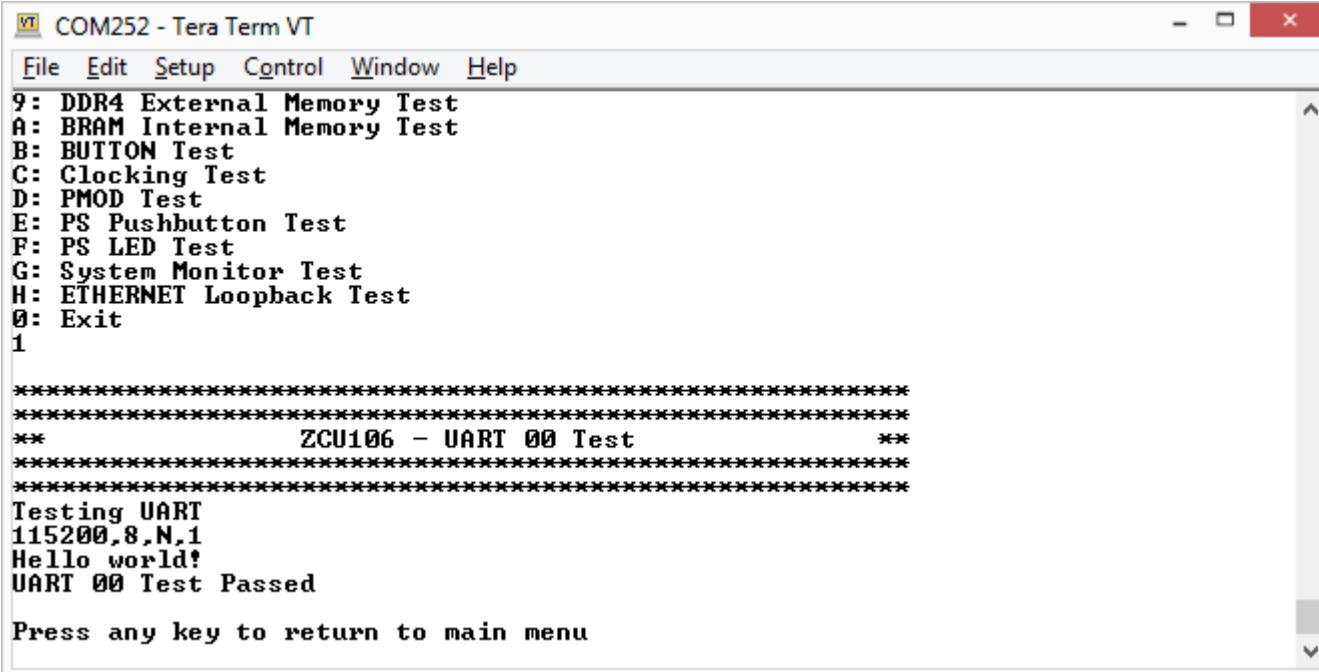
The screenshot shows a terminal window titled "COM252 - Tera Term VT". The window has a standard Windows-style title bar with icons for minimize, maximize, and close. Below the title bar is a menu bar with options: File, Edit, Setup, Control, Window, Help. The main content area displays the following text:

```
*****
** Zynq UltraScale+ MPSoC ZCU106 Evaluation Kit IPI Test **
*****
Choose Feature to Test:
1: UART Test
2: LED Test
3: IIC Test
5: TIMER/SCUGIC Test
6: CAN Bus Test
7: SWITCH Test
8: PS DDR4 External Memory Test
9: DDR4 External Memory Test
A: BRAM Internal Memory Test
B: BUTTON Test
C: Clocking Test
D: PMOD Test
E: PS Pushbutton Test
F: PS LED Test
G: System Monitor Test
H: ETHERNET Loopback Test
0: Exit
```

ZCU106 IPI Design

> UART Test

- » Type “1” to start the UART Test
- » After each test, press any key to return to the main menu



The screenshot shows a terminal window titled "COM252 - Tera Term VT". The window has a menu bar with "File", "Edit", "Setup", "Control", "Window", and "Help". Below the menu is a list of test options:

```
9: DDR4 External Memory Test
A: BRAM Internal Memory Test
B: BUTTON Test
C: Clocking Test
D: PMOD Test
E: PS Pushbutton Test
F: PS LED Test
G: System Monitor Test
H: ETHERNET Loopback Test
0: Exit
```

The user has typed "1" to start the UART test. The terminal then displays the following output:

```
*****
**      ZCU106 - UART 00 Test      **
*****
Testing UART
115200,8,N,1
Hello world!
UART 00 Test Passed

Press any key to return to main menu
```

ZCU106 IPI Design

- > LED Test
 - » Type 2 to begin LED Test
- > View Walking 1's pattern on GPIO LEDs

The screenshot shows a terminal window titled "COM252 - Tera Term VT". The window has a menu bar with "File", "Edit", "Setup", "Control", "Window", and "Help". Below the menu is a list of test options:

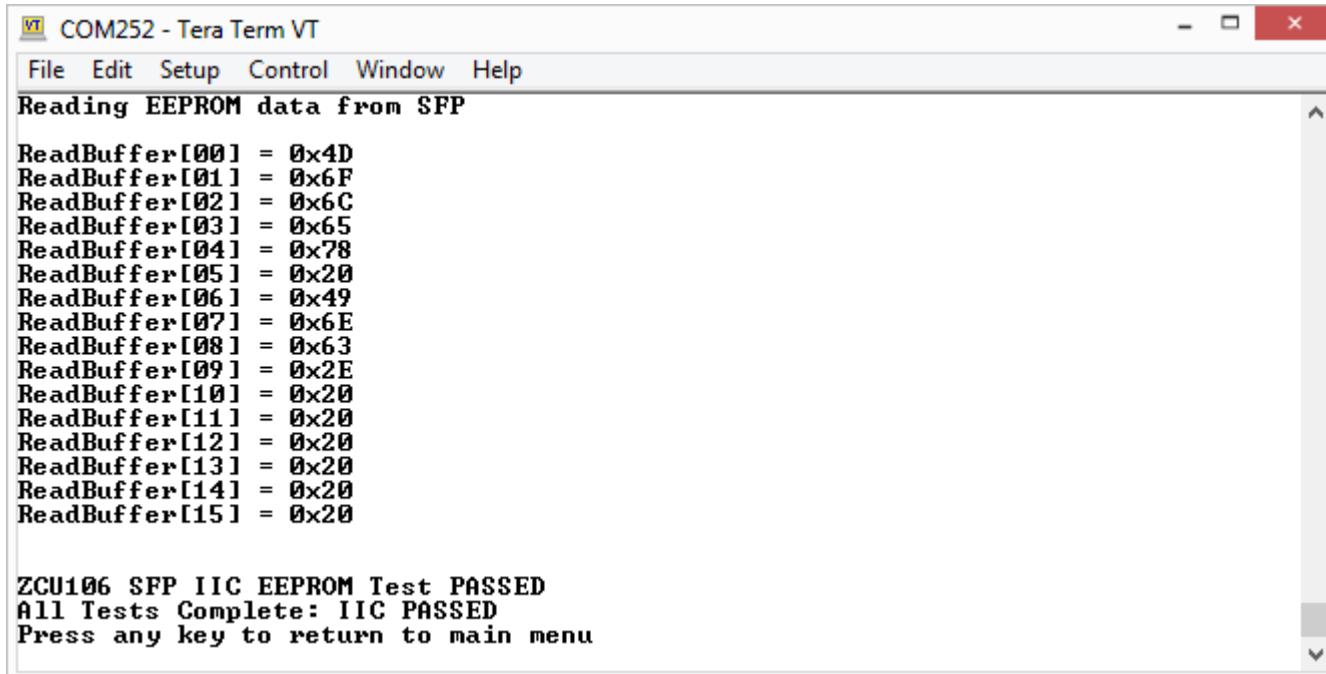
- 5: TIMER/SCUGIC Test
- 6: CAN Bus Test
- 7: SWITCH Test
- 8: PS DDR4 External Memory Test
- 9: DDR4 External Memory Test
- A: BRAM Internal Memory Test
- B: BUTTON Test
- C: Clocking Test
- D: PMOD Test
- E: PS Pushbutton Test
- F: PS LED Test
- G: System Monitor Test
- H: ETHERNET Loopback Test
- 0: Exit

After the menu, the number "2" is typed. This is followed by a series of asterisks: *****. Then, the text "ZCU106 - GPIO LED Test" is displayed between two sets of asterisks. Finally, the instructions "Watch the LEDs" and "Press any key to return to main menu" are shown at the bottom.

ZCU106 IPI Design

> IIC Test

» Type 3 to begin IIC Test



The screenshot shows a terminal window titled "COM252 - Tera Term VT". The window has a menu bar with File, Edit, Setup, Control, Window, and Help. The main text area displays the output of an IIC test. It starts with "Reading EEPROM data from SFP" followed by a series of hex values for ReadBuffer[00] through ReadBuffer[15]. Below this, it shows the test results: "ZCU106 SFP IIC EEPROM Test PASSED", "All Tests Complete: IIC PASSED", and "Press any key to return to main menu".

```
Reading EEPROM data from SFP
ReadBuffer[00] = 0x4D
ReadBuffer[01] = 0x6F
ReadBuffer[02] = 0x6C
ReadBuffer[03] = 0x65
ReadBuffer[04] = 0x78
ReadBuffer[05] = 0x20
ReadBuffer[06] = 0x49
ReadBuffer[07] = 0x6E
ReadBuffer[08] = 0x63
ReadBuffer[09] = 0x2E
ReadBuffer[10] = 0x20
ReadBuffer[11] = 0x20
ReadBuffer[12] = 0x20
ReadBuffer[13] = 0x20
ReadBuffer[14] = 0x20
ReadBuffer[15] = 0x20

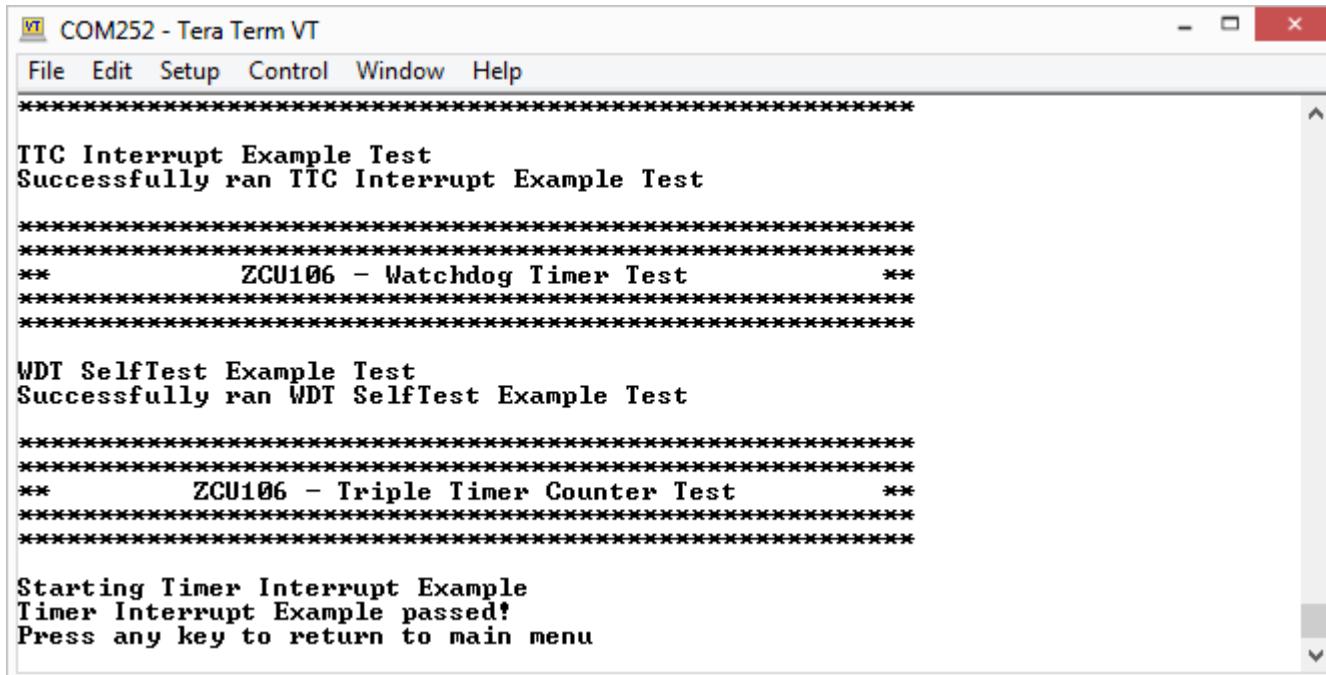
ZCU106 SFP IIC EEPROM Test PASSED
All Tests Complete: IIC PASSED
Press any key to return to main menu
```

Note: IIC test requires optional XM107 boards
and SFP Loopback modules

ZCU106 IPI Design

> Timer/SCUGIC Test

» Type 5 to begin Timer Test



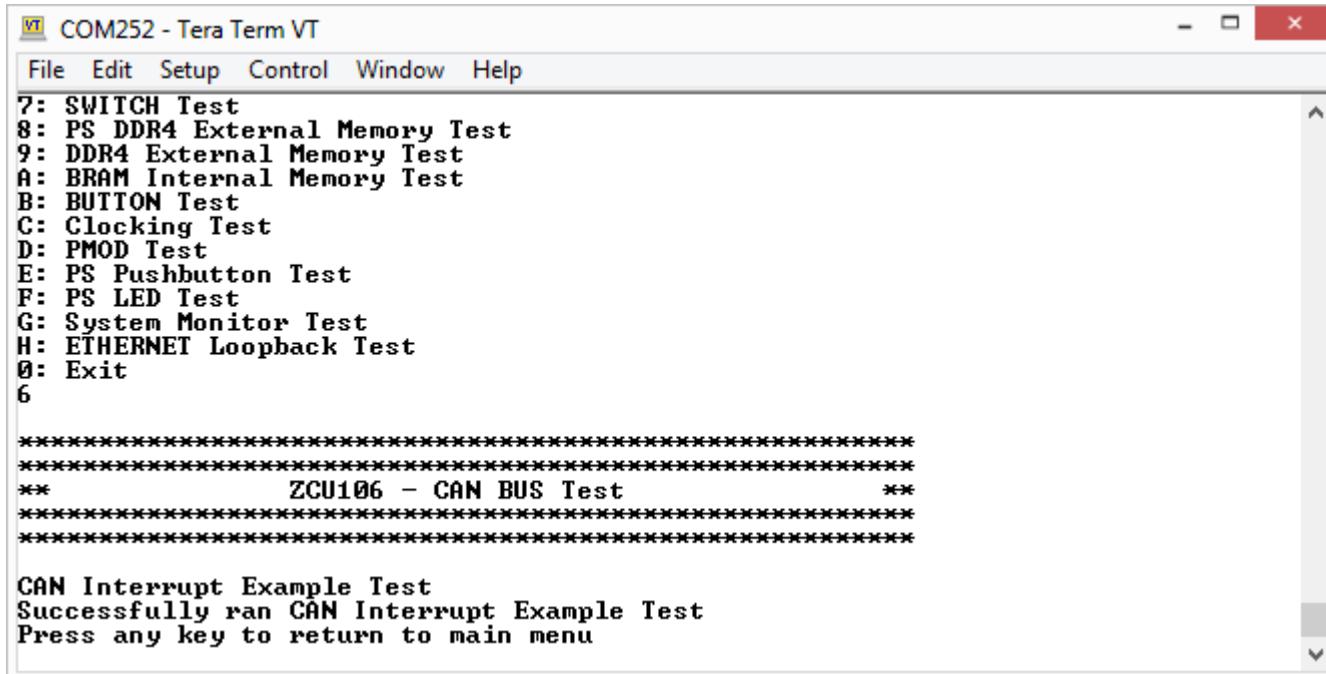
The screenshot shows a terminal window titled "COM252 - Tera Term VT". The window has a menu bar with File, Edit, Setup, Control, Window, and Help. The main pane displays the following text:

```
*****
TTC Interrupt Example Test
Successfully ran TTC Interrupt Example Test
*****
**          ZCU106 - Watchdog Timer Test      **
*****
WDT SelfTest Example Test
Successfully ran WDT SelfTest Example Test
*****
**          ZCU106 - Triple Timer Counter Test  **
*****
Starting Timer Interrupt Example
Timer Interrupt Example passed!
Press any key to return to main menu
```

ZCU106 IPI Design

> CAN Bus Test

» Type 6 to begin CAN Bus Test



COM252 - Tera Term VT

File Edit Setup Control Window Help

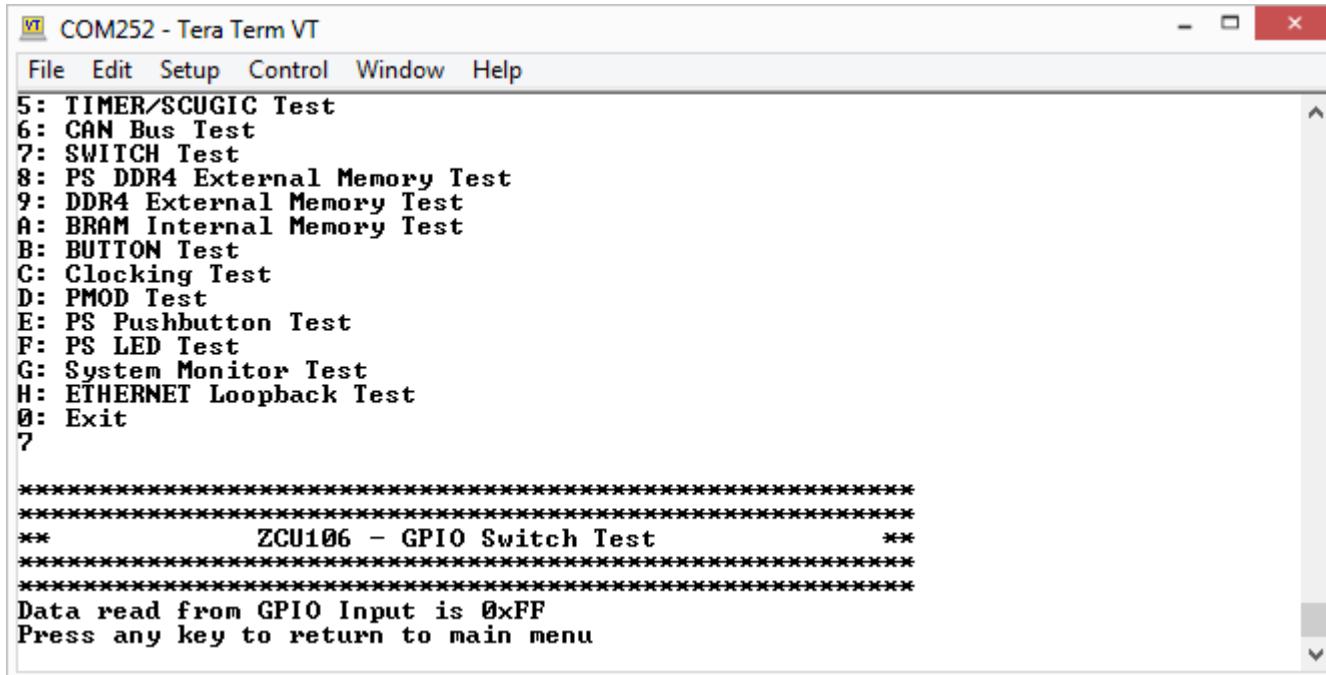
```
7: SWITCH Test
8: PS DDR4 External Memory Test
9: DDR4 External Memory Test
A: BRAM Internal Memory Test
B: BUTTON Test
C: Clocking Test
D: PMOD Test
E: PS Pushbutton Test
F: PS LED Test
G: System Monitor Test
H: ETHERNET Loopback Test
0: Exit
6

*****
**          ZCU106 – CAN BUS Test      **
*****
CAN Interrupt Example Test
Successfully ran CAN Interrupt Example Test
Press any key to return to main menu
```

ZCU106 IPI Design

> GPIO Switch Test

- » Set 8-position PL DIP Switch (SW13)
- » Type 7 to begin GPIO Switch Test



COM252 - Tera Term VT

File Edit Setup Control Window Help

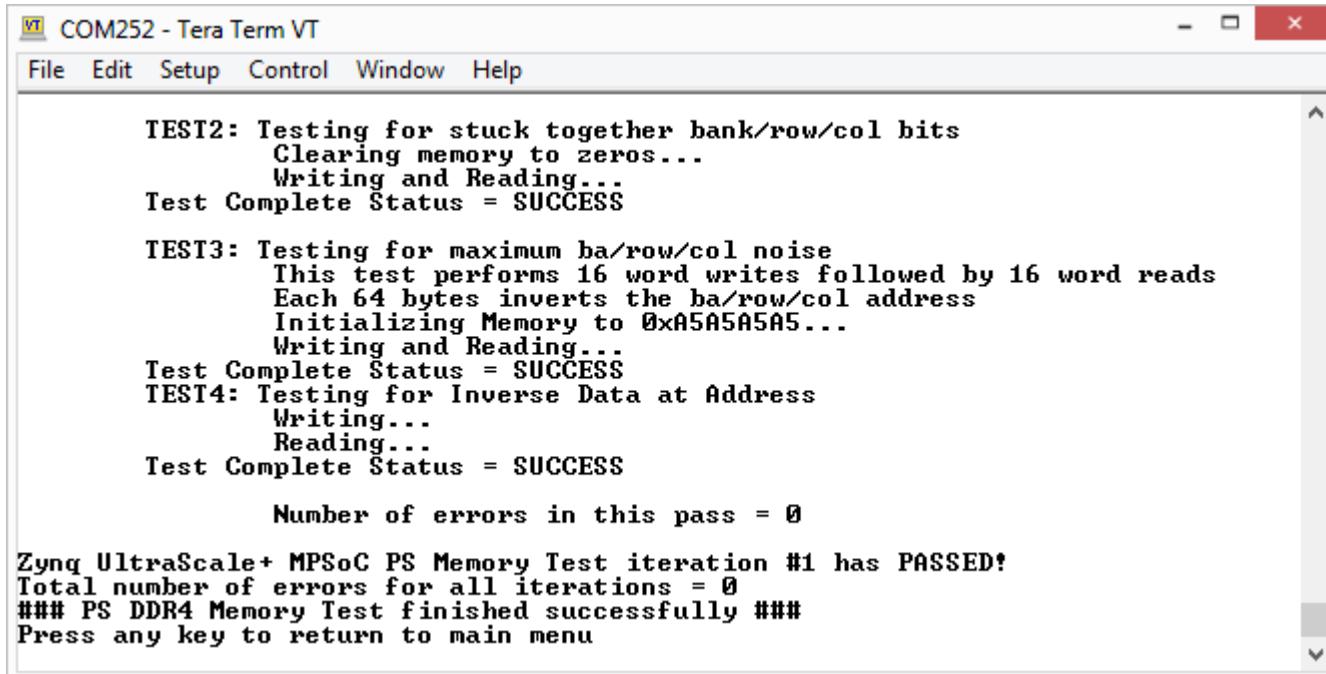
```
5: TIMER/SCUGIC Test
6: CAN Bus Test
7: SWITCH Test
8: PS DDR4 External Memory Test
9: DDR4 External Memory Test
A: BRAM Internal Memory Test
B: BUTTON Test
C: Clocking Test
D: PMOD Test
E: PS Pushbutton Test
F: PS LED Test
G: System Monitor Test
H: ETHERNET Loopback Test
0: Exit
7

*****
**          ZCU106 - GPIO Switch Test          **
*****
Data read from GPIO Input is 0xFF
Press any key to return to main menu
```

ZCU106 IPI Design

> DDR4 External Memory Test

» Type 8 to begin PS DDR4 Memory Test



VT COM252 - Tera Term VT

File Edit Setup Control Window Help

```
TEST2: Testing for stuck together bank/row/col bits
Clearing memory to zeros...
Writing and Reading...
Test Complete Status = SUCCESS

TEST3: Testing for maximum ba/row/col noise
This test performs 16 word writes followed by 16 word reads
Each 64 bytes inverts the ba/row/col address
Initializing Memory to 0xA5A5A5A5...
Writing and Reading...
Test Complete Status = SUCCESS
TEST4: Testing for Inverse Data at Address
Writing...
Reading...
Test Complete Status = SUCCESS

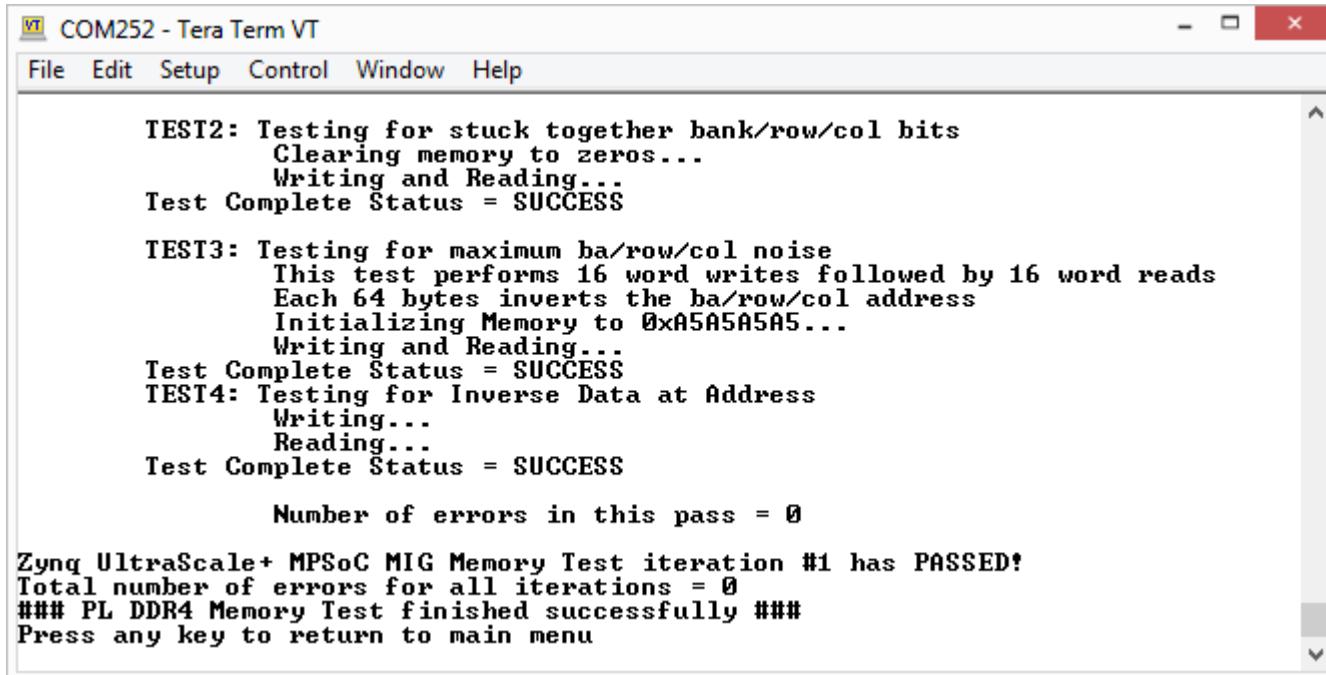
Number of errors in this pass = 0

Zynq UltraScale+ MPSoC PS Memory Test iteration #1 has PASSED!
Total number of errors for all iterations = 0
### PS DDR4 Memory Test finished successfully ####
Press any key to return to main menu
```

ZCU106 IPI Design

> DDR4 External Memory Test

» Type 9 to begin PL DDR4 Memory Test



COM252 - Tera Term VT

File Edit Setup Control Window Help

```
TEST2: Testing for stuck together bank/row/col bits
Clearing memory to zeros...
Writing and Reading...
Test Complete Status = SUCCESS

TEST3: Testing for maximum ba/row/col noise
This test performs 16 word writes followed by 16 word reads
Each 64 bytes inverts the ba/row/col address
Initializing Memory to 0xA5A5A5A5...
Writing and Reading...
Test Complete Status = SUCCESS
TEST4: Testing for Inverse Data at Address
Writing...
Reading...
Test Complete Status = SUCCESS

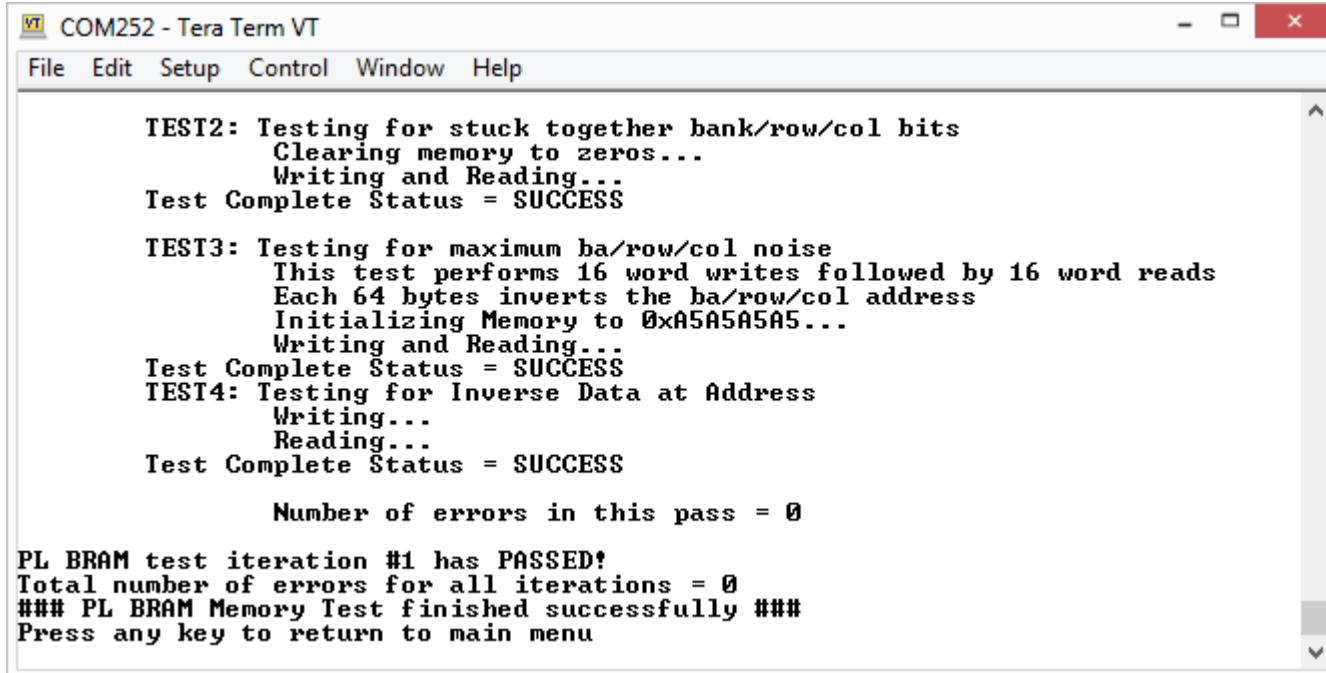
Number of errors in this pass = 0

Zynq UltraScale+ MPSoC MIG Memory Test iteration #1 has PASSED!
Total number of errors for all iterations = 0
### PL DDR4 Memory Test finished successfully ####
Press any key to return to main menu
```

ZCU106 IPI Design

> BRAM Internal Memory Test

» Type A to begin PL BRAM Memory Test



The screenshot shows a terminal window titled "COM252 - Tera Term VT". The window contains the following text output from a PL BRAM memory test:

```
TEST2: Testing for stuck together bank/row/col bits
Clearing memory to zeros...
Writing and Reading...
Test Complete Status = SUCCESS

TEST3: Testing for maximum ba/row/col noise
This test performs 16 word writes followed by 16 word reads
Each 64 bytes inverts the ba/row/col address
Initializing Memory to 0xA5A5A5A5...
Writing and Reading...
Test Complete Status = SUCCESS
TEST4: Testing for Inverse Data at Address
Writing...
Reading...
Test Complete Status = SUCCESS

Number of errors in this pass = 0

PL BRAM test iteration #1 has PASSED!
Total number of errors for all iterations = 0
### PL BRAM Memory Test finished successfully ####
Press any key to return to main menu
```

ZCU106 IPI Design

> Button Test

» Type B to begin Button Test

```
VT COM252 - Tera Term VT
File Edit Setup Control Window Help
H: ETHERNET Loopback Test
0: Exit
B

*****
**      ZCU106 - PL GPIO Pushbutton Test**
*****
Press west button
Press south button
Press east button
Press north button
Press center button
Press any button

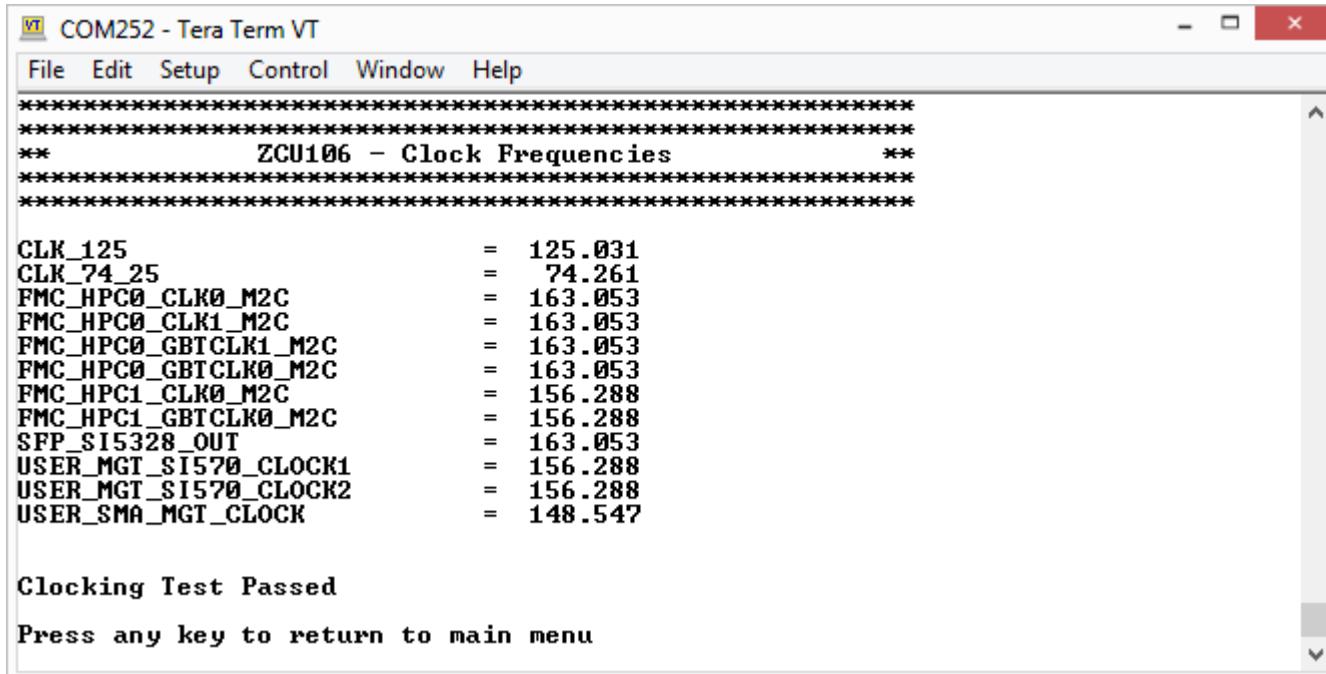
Successfully ran PL GPIO Pushbutton Test
Press any key to return to main menu
```



ZCU106 IPI Design

> Clock Test

- » This test requires the optional SMA cables, 148.5 MHz clock source and XM107 boards
- » The clocks must be set up as detailed in XTP497
- » Type C to begin Clock Test



COM252 - Tera Term VT

File Edit Setup Control Window Help

```
*****
**          ZCU106 - Clock Frequencies      **
*****
```

CLK_125	= 125.031
CLK_74_25	= 74.261
FMC_HPC0_CLK0_M2C	= 163.053
FMC_HPC0_CLK1_M2C	= 163.053
FMC_HPC0_GBTCLK1_M2C	= 163.053
FMC_HPC0_GBTCLK0_M2C	= 163.053
FMC_HPC1_CLK0_M2C	= 156.288
FMC_HPC1_GBTCLK0_M2C	= 156.288
SFP_SI5328_OUT	= 163.053
USER_MGT_SI570_CLOCK1	= 156.288
USER_MGT_SI570_CLOCK2	= 156.288
USER_SMA_MGT_CLOCK	= 148.547

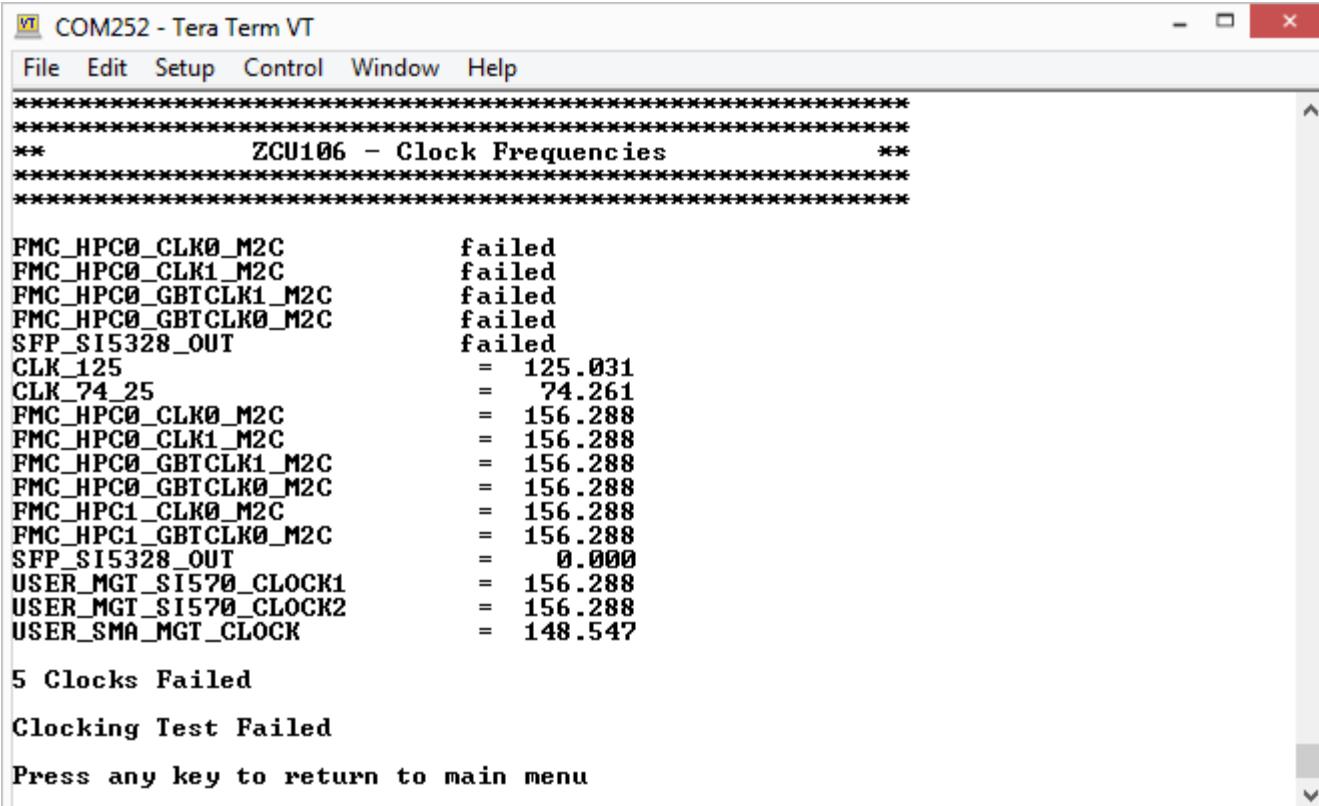
Clocking Test Passed

Press any key to return to main menu

ZCU106 IPI Design

> Clock Test

- » Without the proper set up, optional SMA cables, clock source, and XM107 boards, several clocks will not show a correct frequency
- » The FMC HPC0 Si570 must be set to 163 MHz after a power cycle
- » The SFP Si5328 must be set to 163 MHz after a power cycle
- » The User SMA MGT clock must be connected to a 148.5 MHz clock source



The screenshot shows a terminal window titled "COM252 - Tera Term VT". The window displays a list of clock frequencies and their status. The output is as follows:

```
*****
**          ZCU106 - Clock Frequencies      **
*****
FMC_HPC0_CLK0_M2C      failed
FMC_HPC0_CLK1_M2C      failed
FMC_HPC0_GBTCLK1_M2C   failed
FMC_HPC0_GBTCLK0_M2C   failed
SFP_SI5328_OUT          failed
CLK_125                 = 125.031
CLK_74_25                = 74.261
FMC_HPC0_CLK0_M2C      = 156.288
FMC_HPC0_CLK1_M2C      = 156.288
FMC_HPC0_GBTCLK1_M2C   = 156.288
FMC_HPC0_GBTCLK0_M2C   = 156.288
FMC_HPC1_CLK0_M2C      = 156.288
FMC_HPC1_GBTCLK0_M2C   = 156.288
SFP_SI5328_OUT          = 0.000
USER_MGT_SI570_CLOCK1   = 156.288
USER_MGT_SI570_CLOCK2   = 156.288
USER_SMA_MGT_CLOCK     = 148.547

5 Clocks Failed

Clocking Test Failed

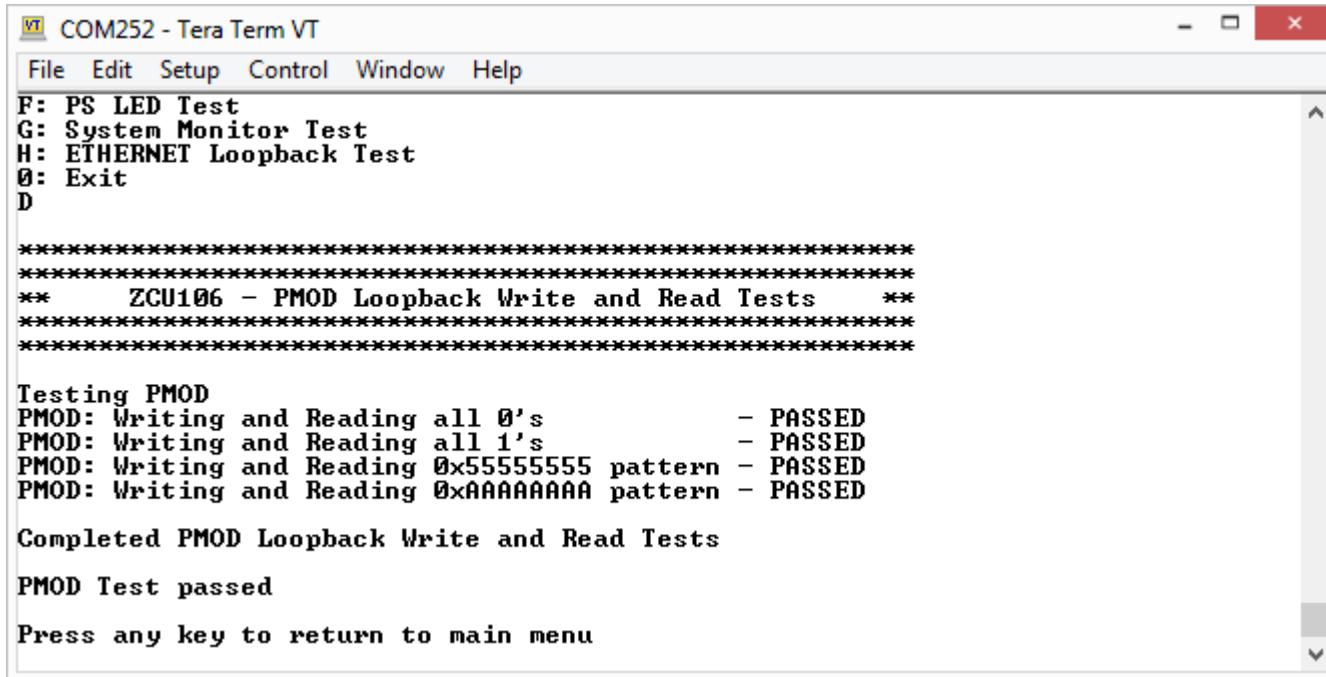
Press any key to return to main menu
```

The XILINX logo is visible in the bottom right corner of the terminal window.

ZCU106 IPI Design

> PMOD Loopback Test

- » This test requires the optional PMOD jumpers
- » Type D to begin PMOD Loopback Test



The screenshot shows a terminal window titled "COM252 - Tera Term VT". The menu bar includes File, Edit, Setup, Control, Window, and Help. Below the menu is a command-line interface with the following text:

```
F: PS LED Test
G: System Monitor Test
H: ETHERNET Loopback Test
Q: Exit
D

*****
**      ZCU106 - PMOD Loopback Write and Read Tests      **
*****
Testing PMOD
PMOD: Writing and Reading all 0's          - PASSED
PMOD: Writing and Reading all 1's          - PASSED
PMOD: Writing and Reading 0x55555555 pattern - PASSED
PMOD: Writing and Reading 0xAAAAAAA pattern - PASSED

Completed PMOD Loopback Write and Read Tests

PMOD Test passed

Press any key to return to main menu
```

ZCU106 IPI Design

> PS Push Button Test (SW19)

» Type E to begin PS Push Button Test

```
VT COM252 - Tera Term VT
File Edit Setup Control Window Help
8: PS DDR4 External Memory Test
9: DDR4 External Memory Test
A: BRAM Internal Memory Test
B: BUTTON Test
C: Clocking Test
D: PMOD Test
E: PS Pushbutton Test
F: PS LED Test
G: System Monitor Test
H: ETHERNET Loopback Test
Q: Exit
E

*****
**      ZCU106 - PS GPIO Pushbutton Test      **
*****


Press PS push button

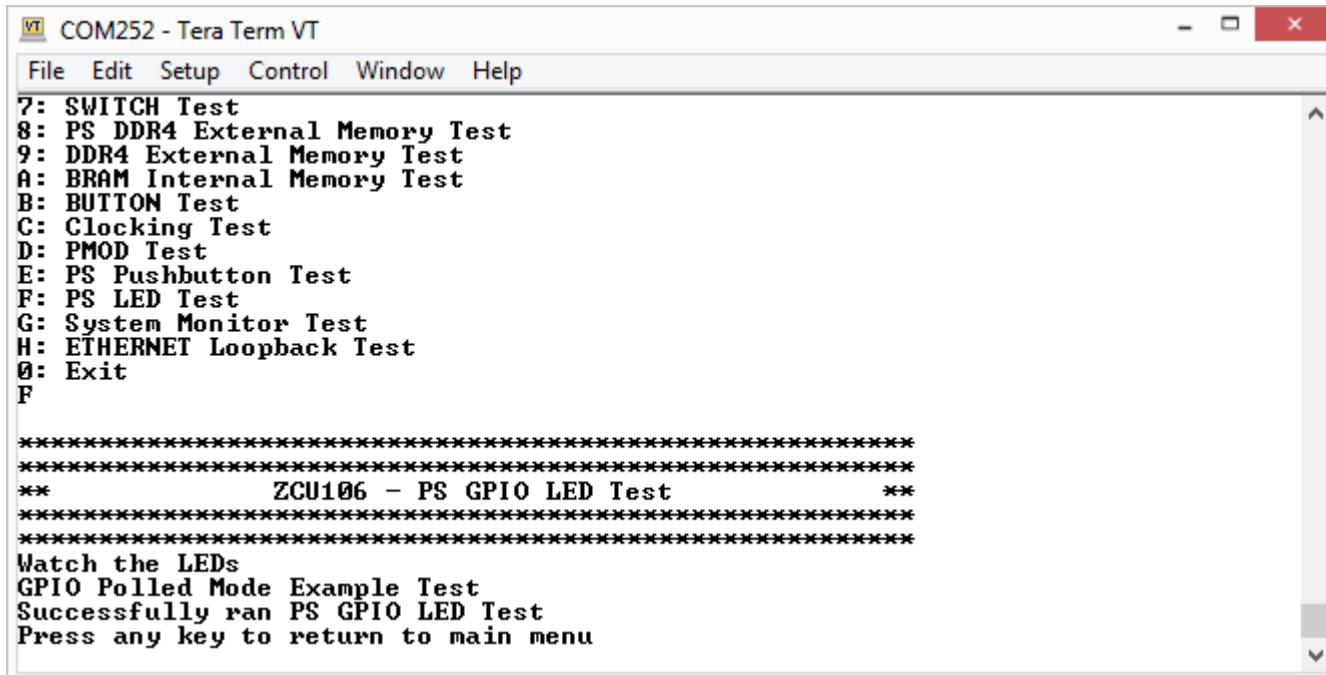
Successfully ran PS GPIO Pushbutton Test
Press any key to return to main menu
```



ZCU106 IPI Design

> PS LED Test

» Type F to begin PS LED Test



COM252 - Tera Term VT

File Edit Setup Control Window Help

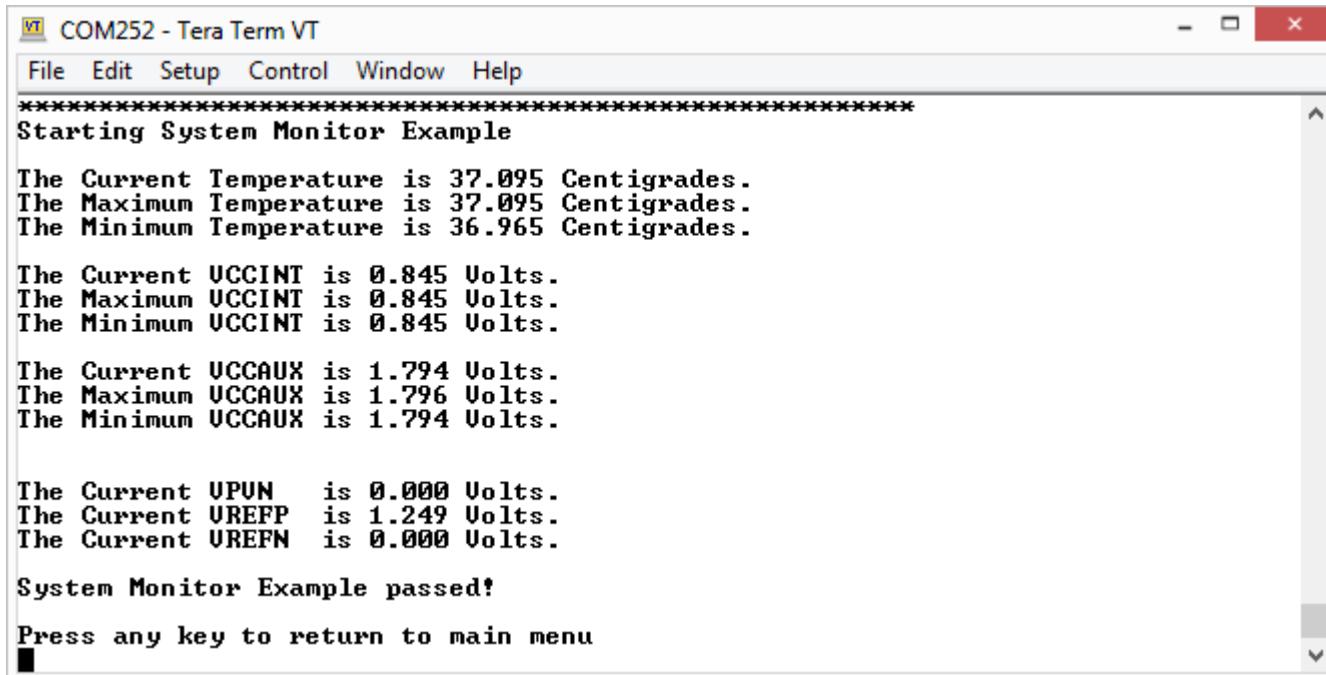
```
7: SWITCH Test
8: PS DDR4 External Memory Test
9: DDR4 External Memory Test
A: BRAM Internal Memory Test
B: BUTTON Test
C: Clocking Test
D: PMOD Test
E: PS Pushbutton Test
F: PS LED Test
G: System Monitor Test
H: ETHERNET Loopback Test
Q: Exit
F

*****
**          ZCU106 - PS GPIO LED Test      **
*****
Watch the LEDs
GPIO Polled Mode Example Test
Successfully ran PS GPIO LED Test
Press any key to return to main menu
```

ZCU106 IPI Design

> System Monitor Test

» Type G to begin System Monitor Test



COM252 - Tera Term VT

```
*****
Starting System Monitor Example

The Current Temperature is 37.095 Centigrades.
The Maximum Temperature is 37.095 Centigrades.
The Minimum Temperature is 36.965 Centigrades.

The Current UCCINT is 0.845 Volts.
The Maximum UCCINT is 0.845 Volts.
The Minimum UCCINT is 0.845 Volts.

The Current UCCAUX is 1.794 Volts.
The Maximum UCCAUX is 1.796 Volts.
The Minimum UCCAUX is 1.794 Volts.

The Current UPUN is 0.000 Volts.
The Current UREFP is 1.249 Volts.
The Current UREFN is 0.000 Volts.

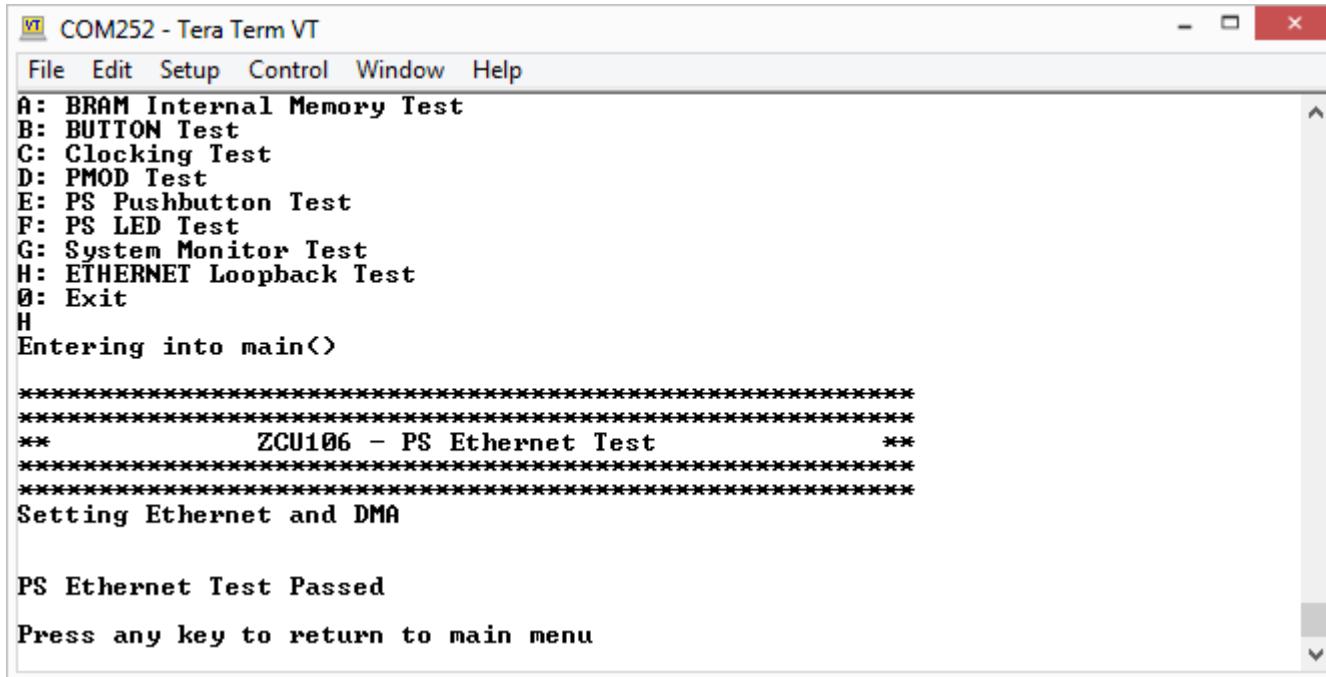
System Monitor Example passed!

Press any key to return to main menu
```

ZCU106 IPI Design

> PS Ethernet Test

» Type H to begin PS Ethernet Loopback Test



The screenshot shows a terminal window titled "COM252 - Tera Term VT". The menu bar includes File, Edit, Setup, Control, Window, and Help. Below the menu is a list of test options:

- A: BRAM Internal Memory Test
- B: BUTTON Test
- C: Clocking Test
- D: PMOD Test
- E: PS Pushbutton Test
- F: PS LED Test
- G: System Monitor Test
- H: ETHERNET Loopback Test
- Q: Exit

The window then displays the following text:

```
H  
Entering into main()  
*****  
**      ZCU106 - PS Ethernet Test      **  
*****  
Setting Ethernet and DMA  
  
PS Ethernet Test Passed  
Press any key to return to main menu
```

Compile ZCU106 IPI Design

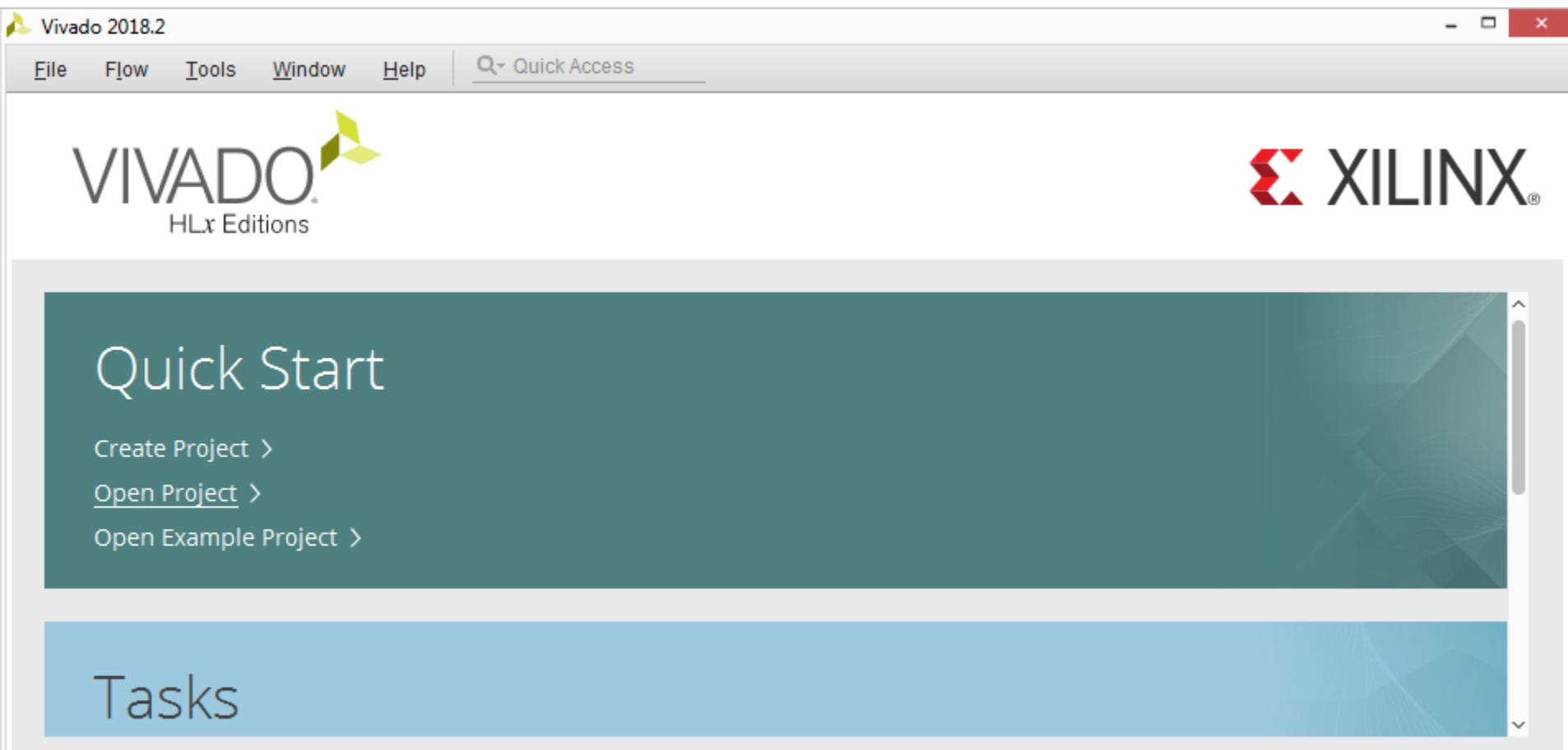


Compile ZCU106 IPI Design

> Open Vivado

Start → All Programs → Xilinx Design Tools → Vivado 2018.2 → Vivado 2018.2

> Select Open Project



Open Project

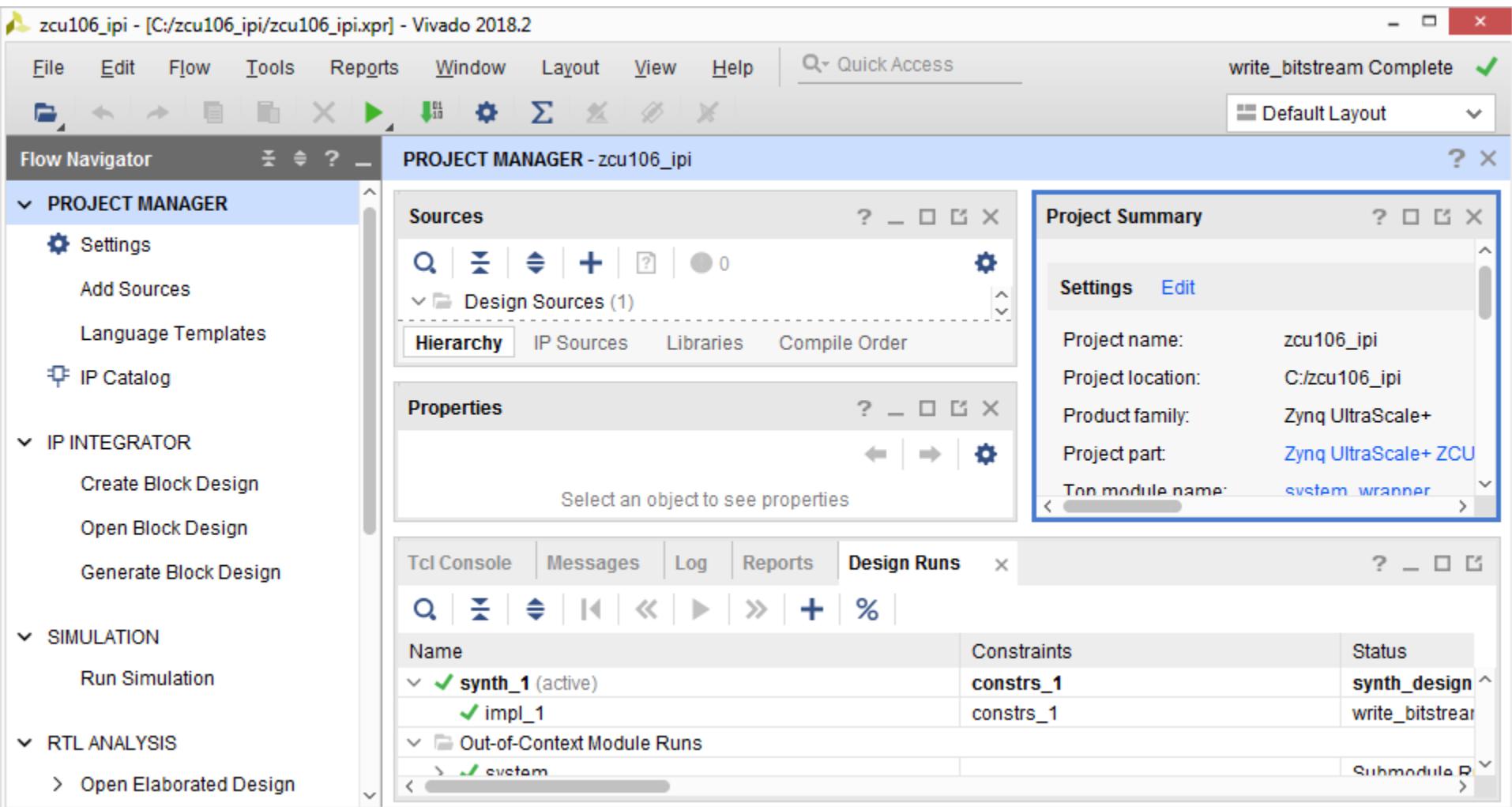
Note: Presentation applies to the ZCU106

XILINX

Compile ZCU106 IPI Design

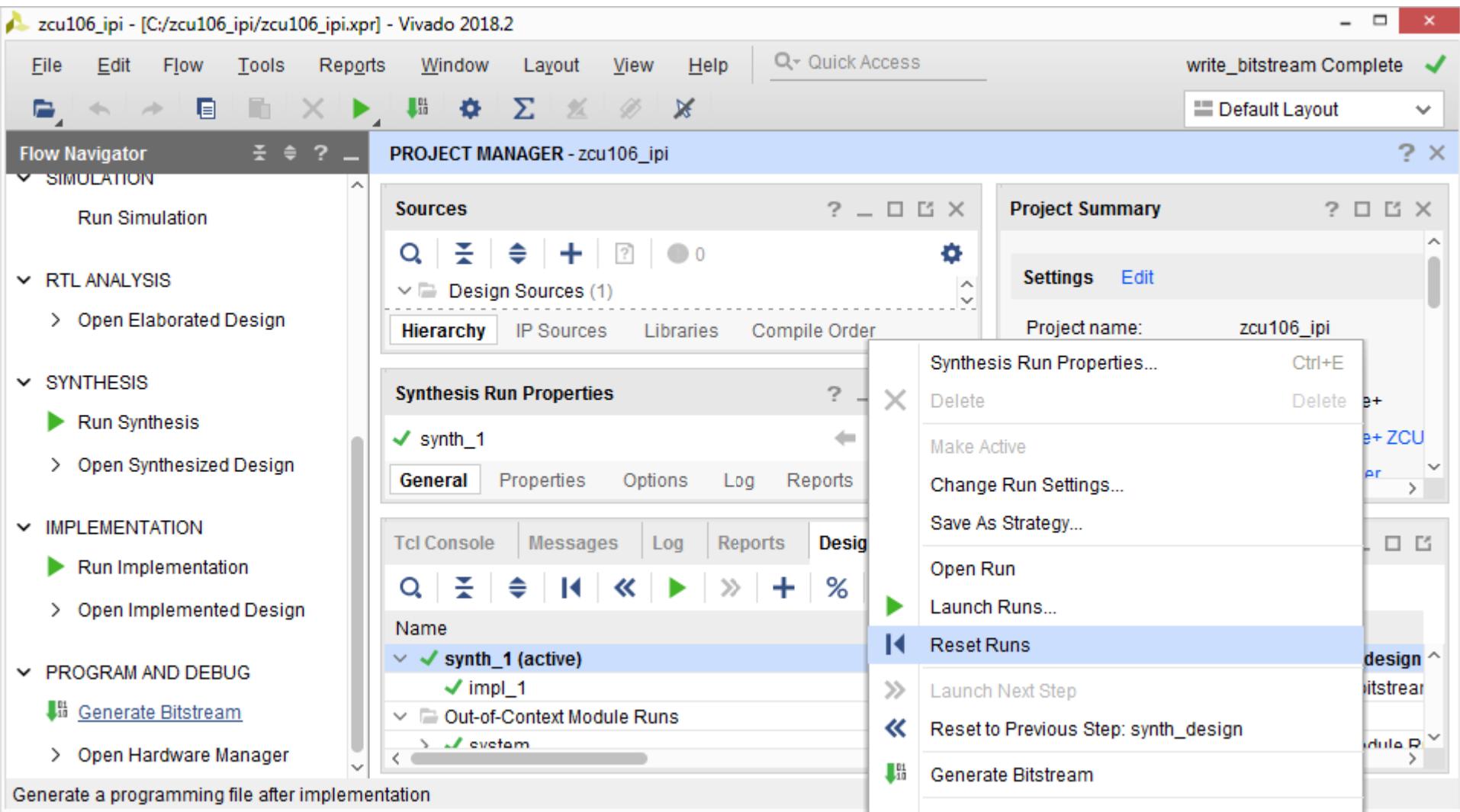
> Open the ZCU106 Design:

» C:\zcu106_ipi\zcu106_ipi.xpr



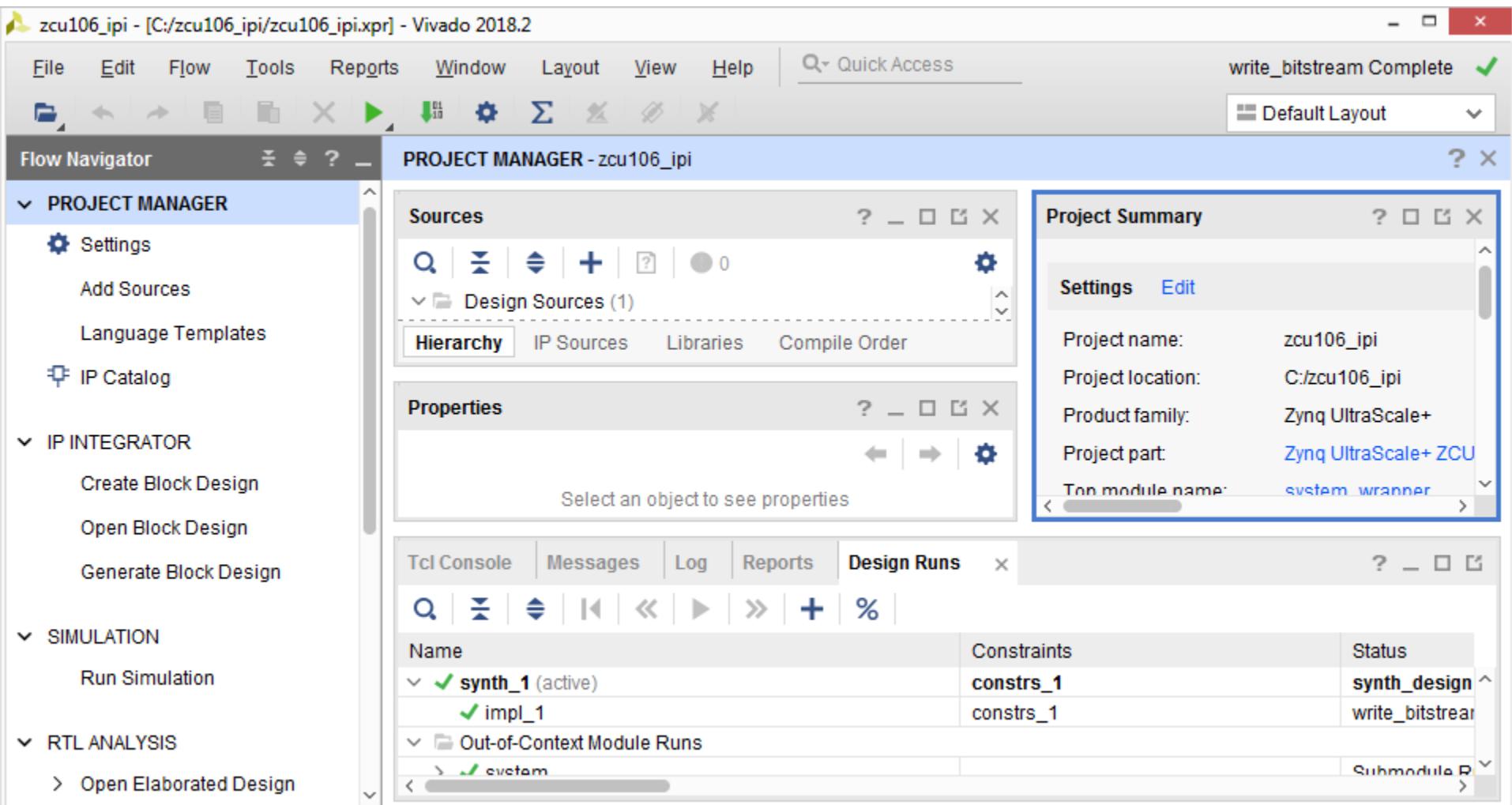
Compile ZCU106 IPI Design

- > The design is fully implemented; you can recompile, or export to SDK
 - » To recompile, right-click synth_1, select Reset Runs then Generate Bitstream



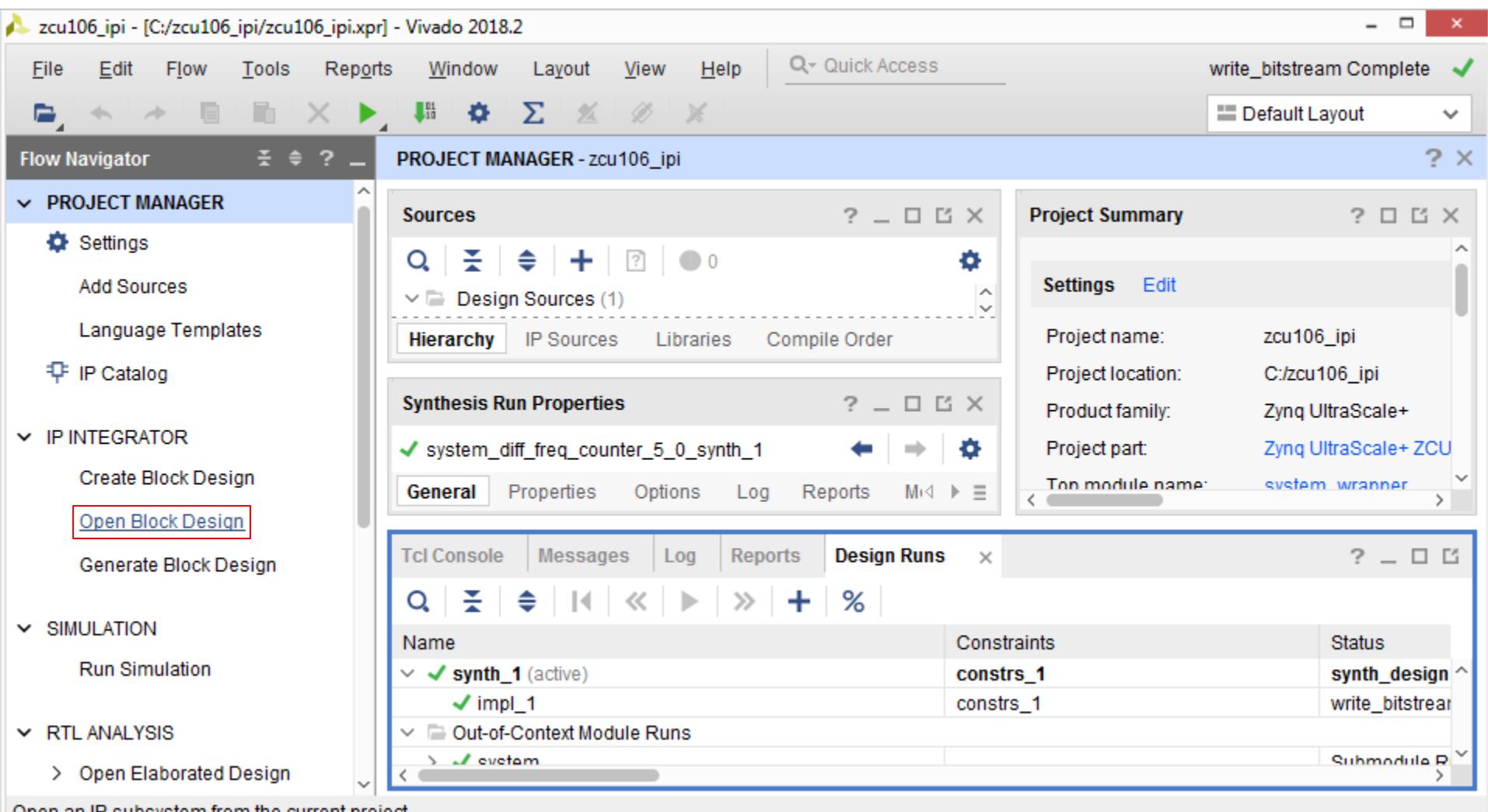
Compile ZCU106 IPI Design

- Once done, both the Synthesis and Implementation will have green check marks



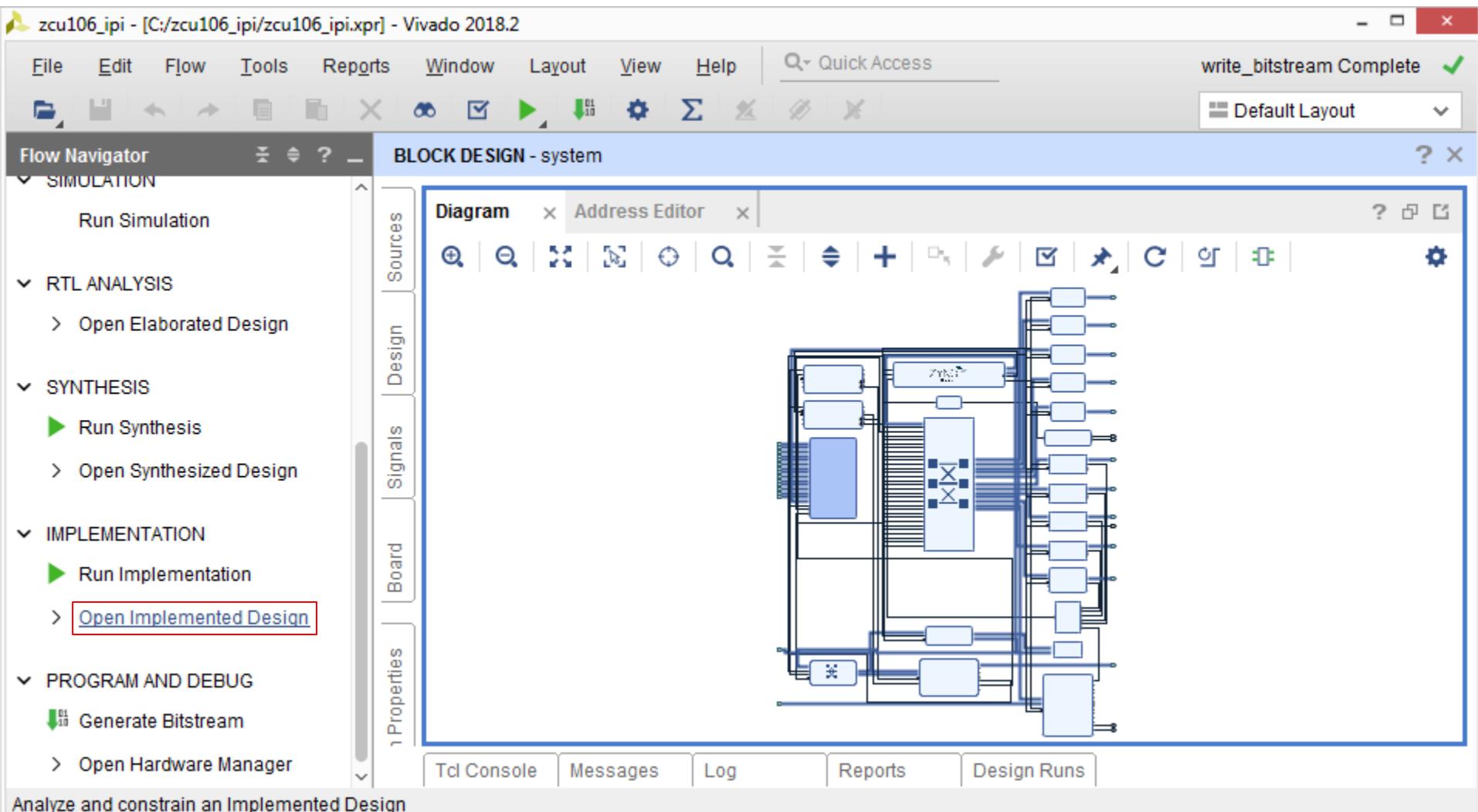
Compile ZCU106 IPI Design

- > The IPI Design has been implemented with IP Integrator (IPI)
- > Click Open Block Design



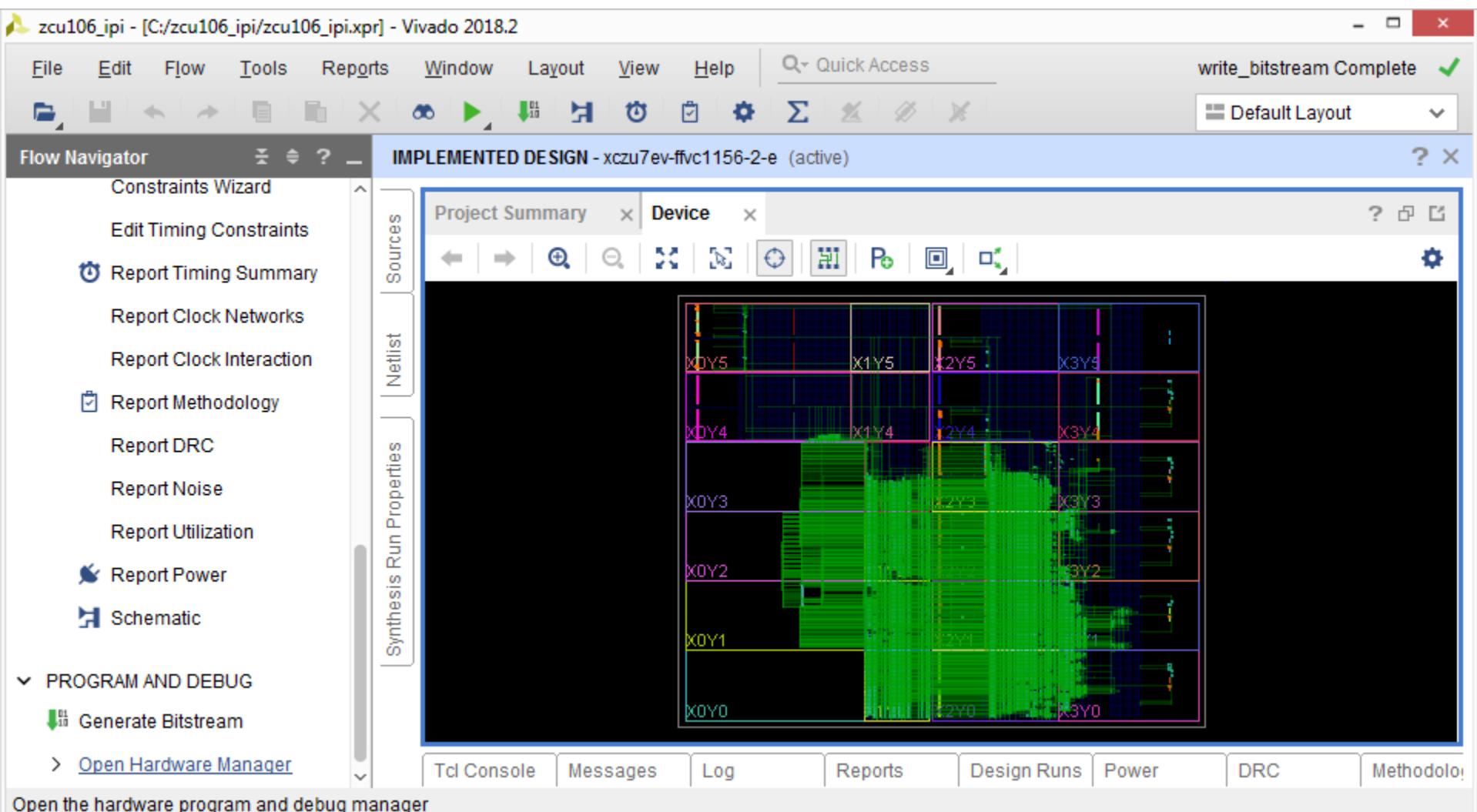
Compile ZCU106 IPI Design

- > All the IP Blocks used in the design can be seen in this view
- > Click Open Implemented Design



Compile ZCU106 IPI Design

> View Implemented Design

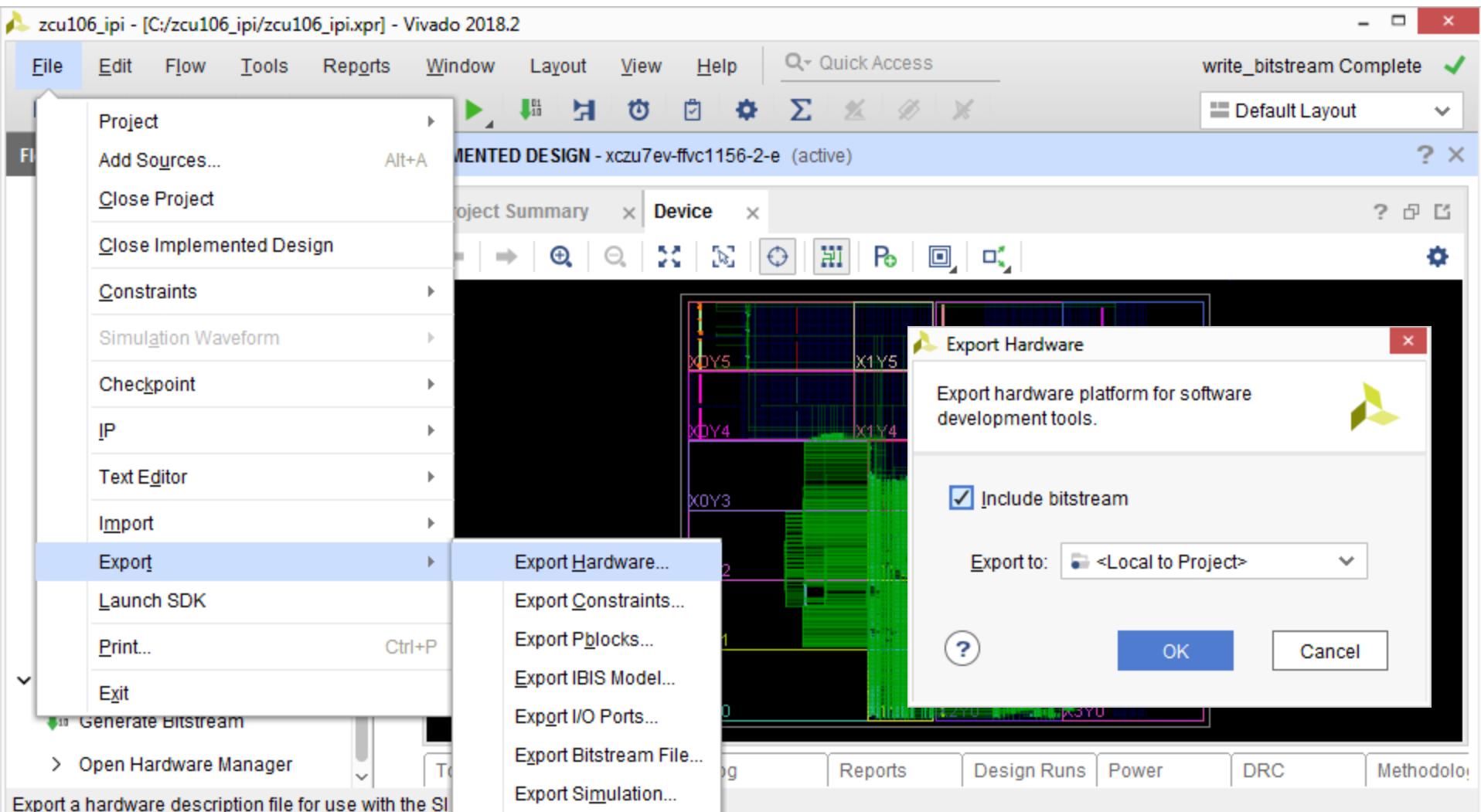


Note: Presentation applies to the ZCU106

 XILINX

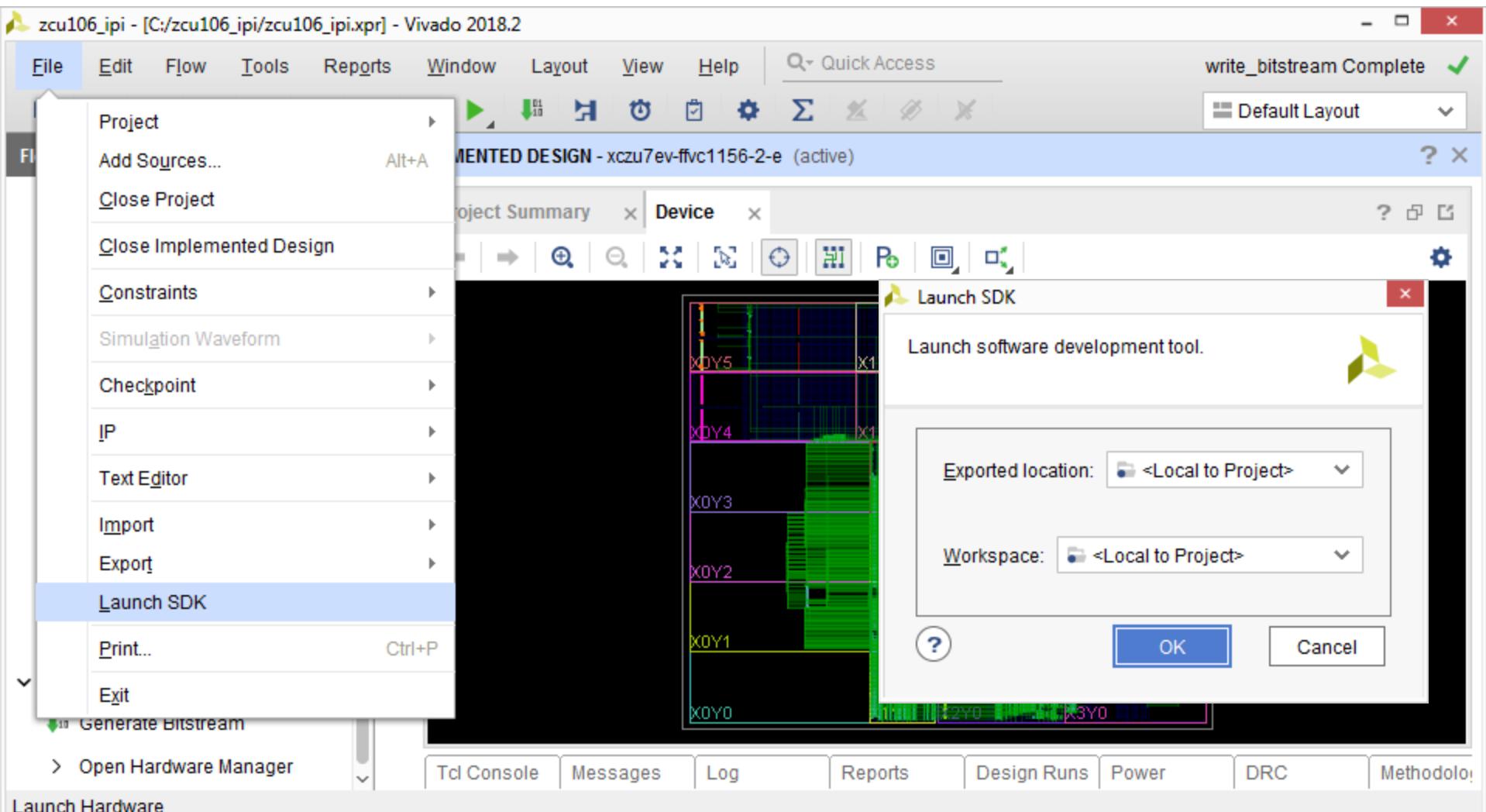
Compile ZCU106 IPI Design

- > Select File → Export → Export Hardware
- > Click OK



Compile ZCU106 IPI Design

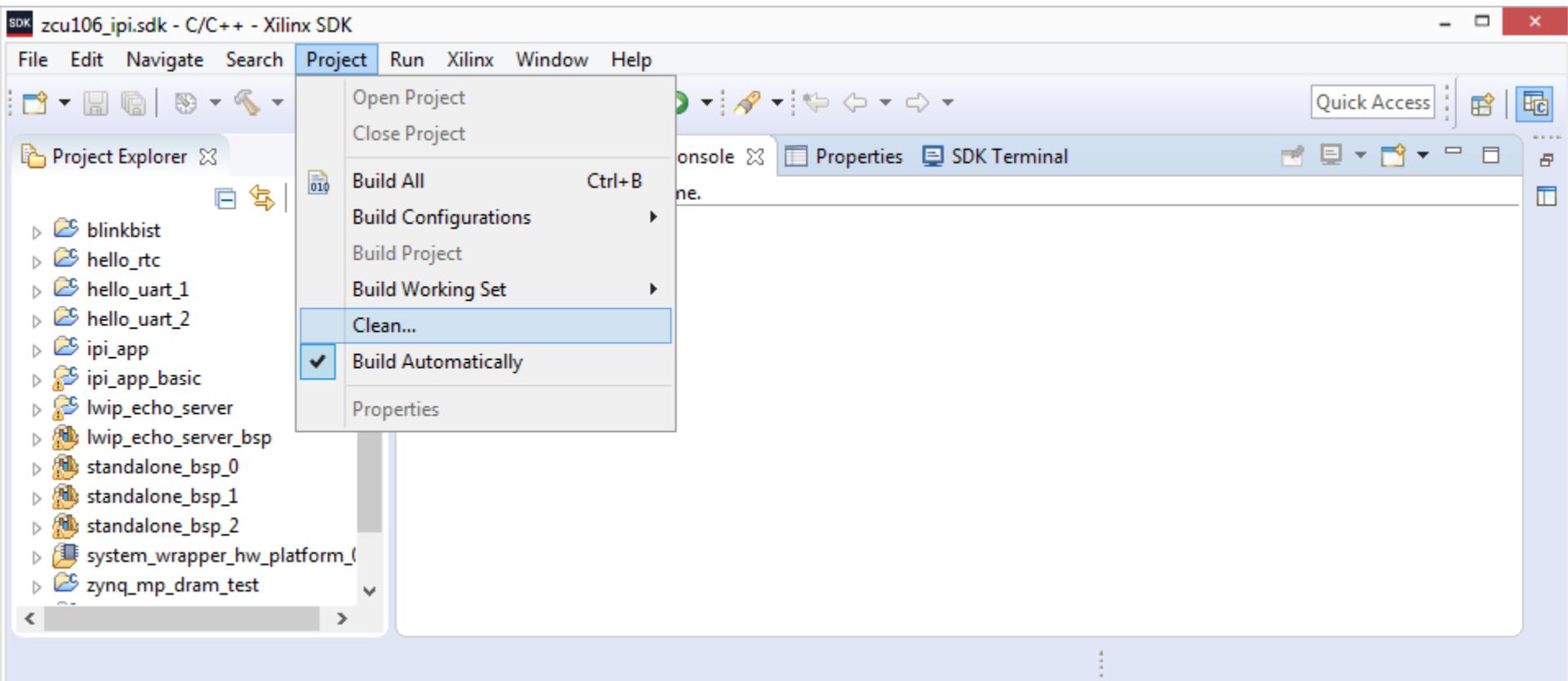
- > Select File → Launch SDK
- > Click OK



Compile ZCU106 Software in SDK

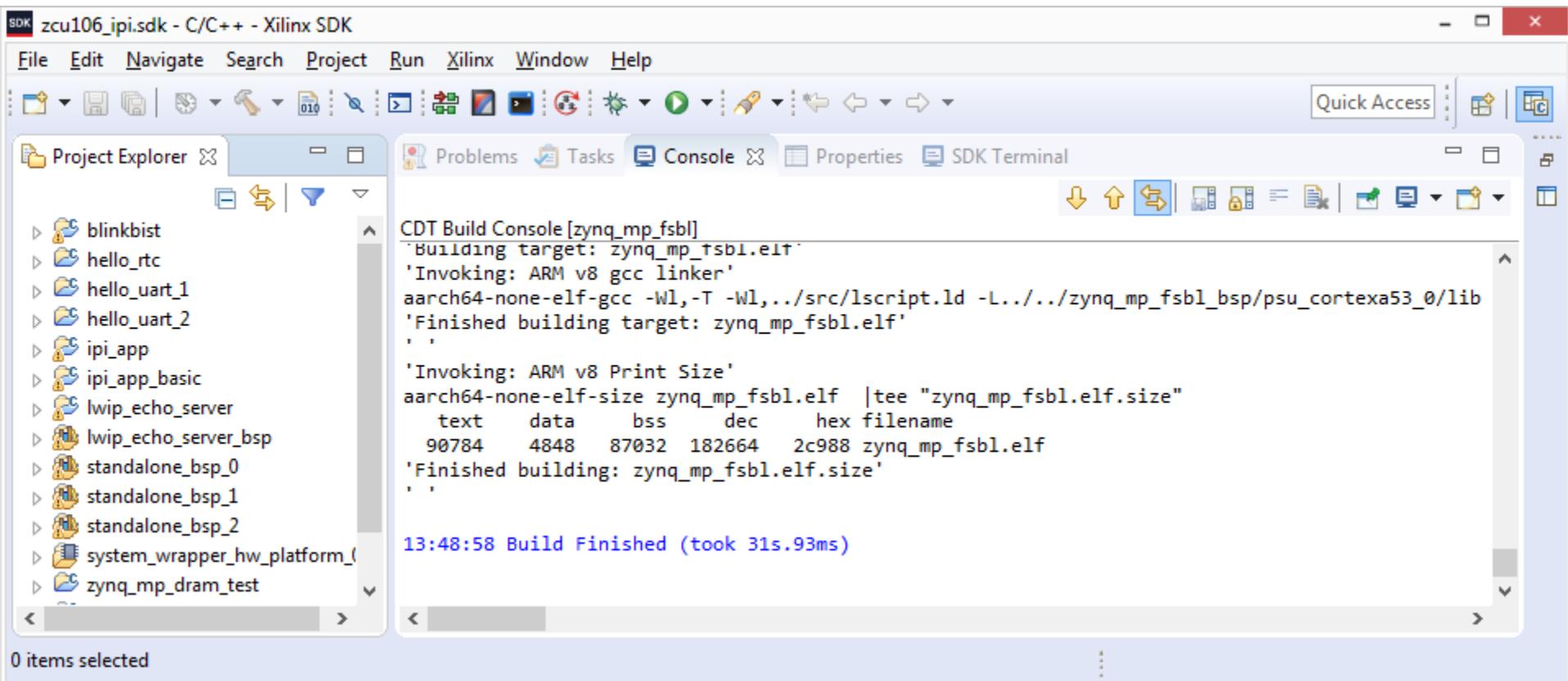
> SDK Software Compile - Build ELF files in SDK

» Select Project → Clean...



Compile ZCU106 Software in SDK

- > All files compiled



The screenshot shows the Xilinx SDK interface for the ZCU106 board. The title bar reads "SDK zcu106_ipi.sdk - C/C++ - Xilinx SDK". The menu bar includes File, Edit, Navigate, Search, Project, Run, Xilinx, Window, and Help. The toolbar contains various icons for file operations like Open, Save, and Build. The left sidebar is the "Project Explorer" showing a list of projects: blinkbist, hello_RTC, hello_uart_1, hello_uart_2, ipi_app, ipi_app_basic, lwip_echo_server, lwip_echo_server_bsp, standalone_bsp_0, standalone_bsp_1, standalone_bsp_2, system_wrapper_hw_platform_, and zynq_mp_dram_test. The main area is the "Console" tab, which displays the build log for the "zynq_mp_fsbl" target:

```
CDT Build Console [zynq_mp_fsbl]
'Building target: zynq_mp_fsbl.elf'
'Invoking: ARM v8 gcc linker'
aarch64-none-elf-gcc -Wl,-T -Wl,../src/lscript.ld -L../../zynq_mp_fsbl_bsp/psu_cortexa53_0/lib
'Finished building target: zynq_mp_fsbl.elf'
'

'Invoking: ARM v8 Print Size'
aarch64-none-elf-size zynq_mp_fsbl.elf | tee "zynq_mp_fsbl.elf.size"
    text      data      bss      dec      hex filename
  90784     4848    87032   182664   2c988 zynq_mp_fsbl.elf
'Finished building: zynq_mp_fsbl.elf.size'
'

13:48:58 Build Finished (took 31s.93ms)
```

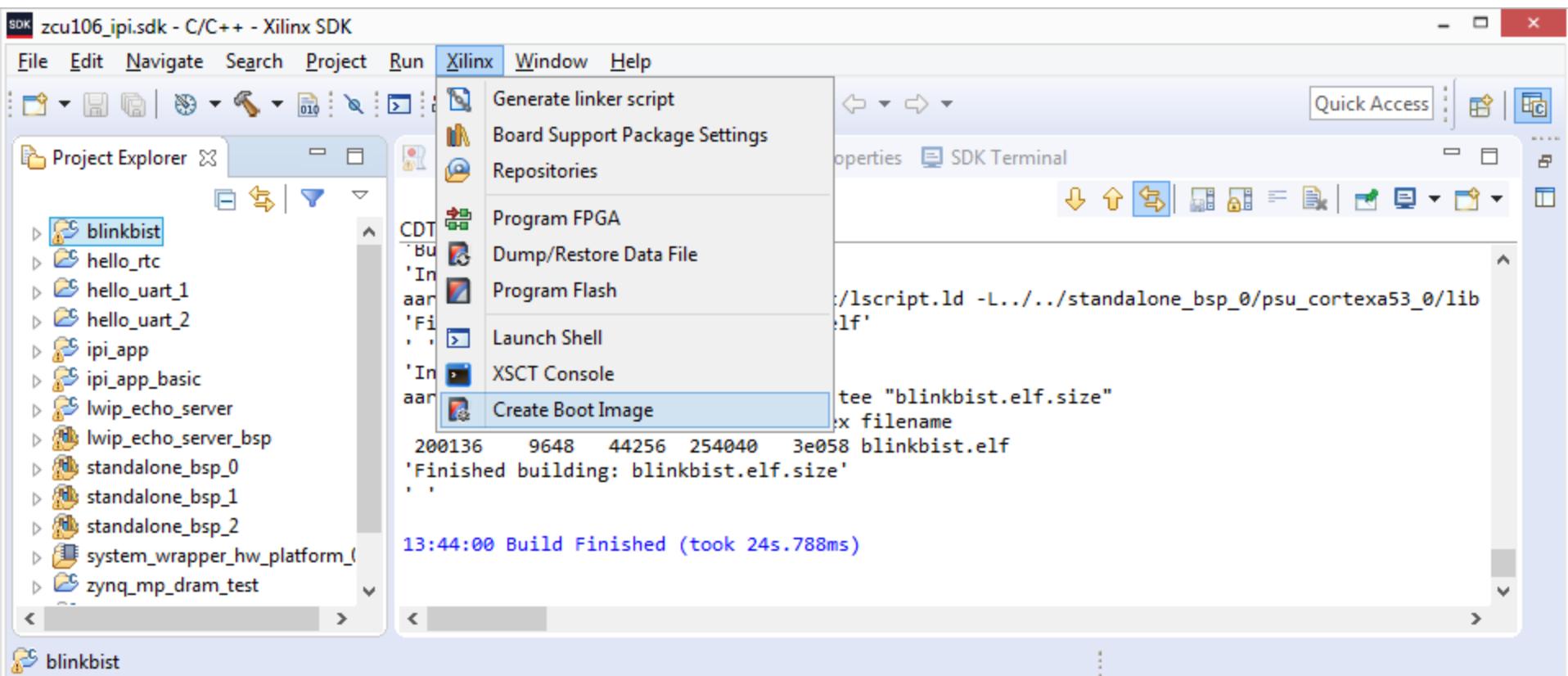
At the bottom left, it says "0 items selected".

Creating a BOOT Image



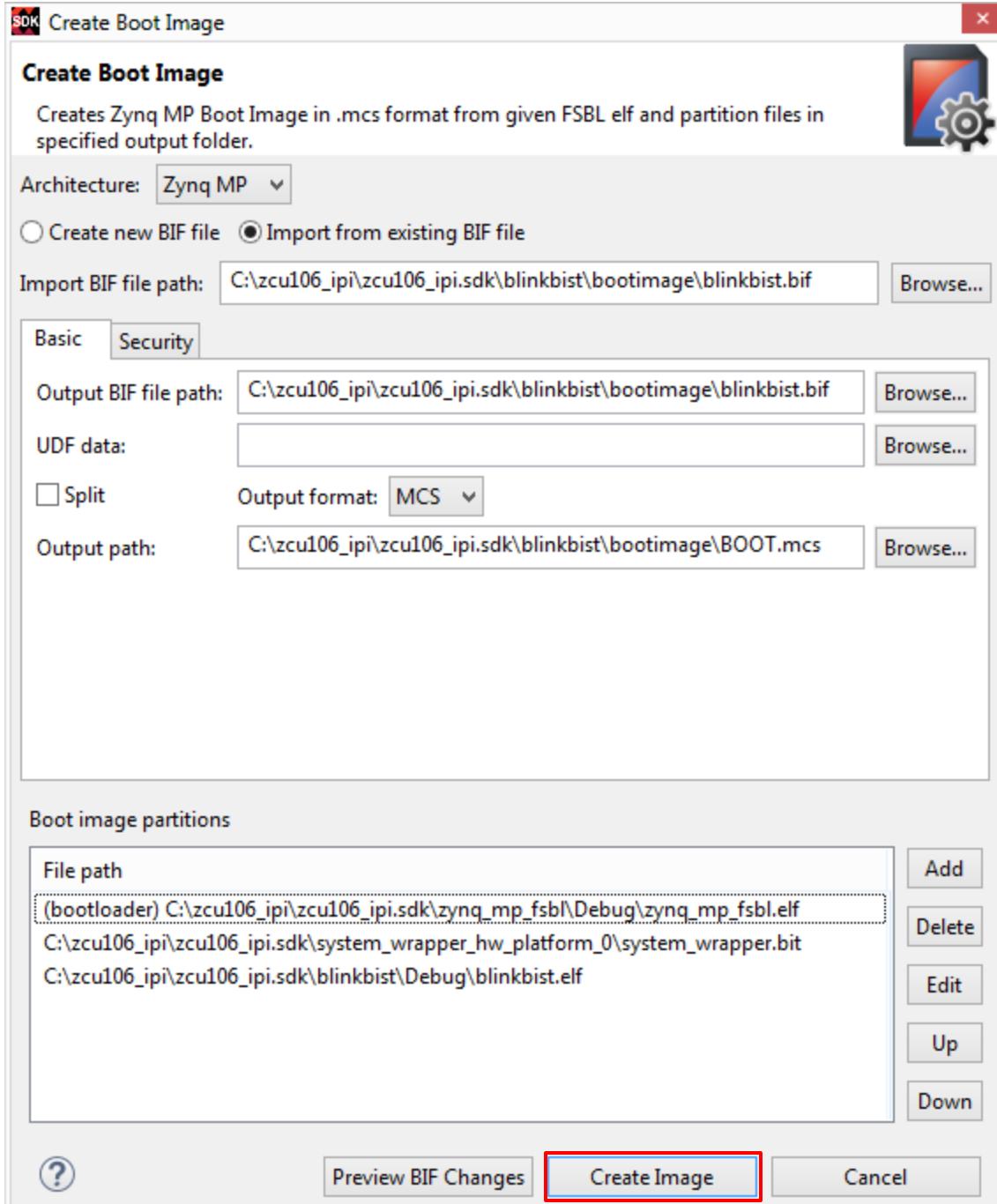
Creating a BOOT Image

- > Select blinkbist
- > Select Xilinx → Create Boot Image



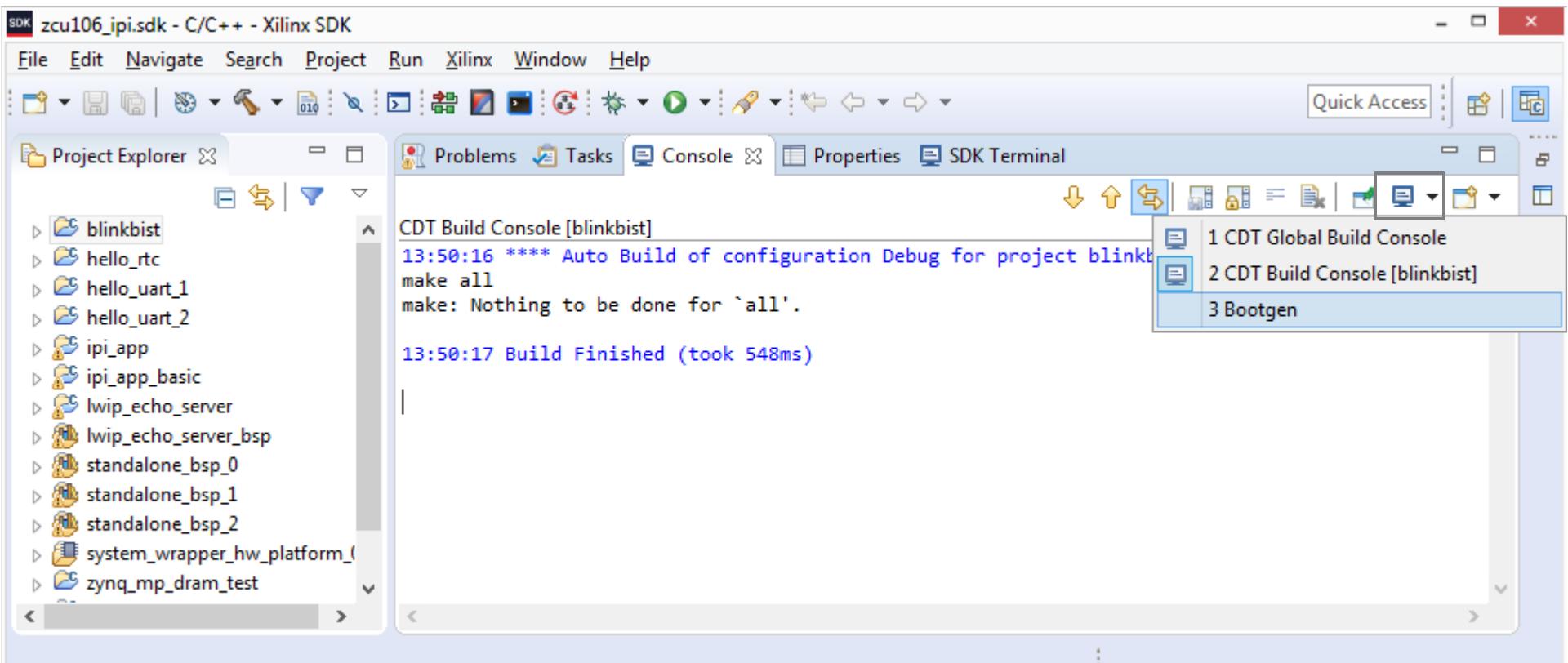
Creating a BOOT Image

- Create the BlinkBIST MCS
- Uses the default BIF file
- The file paths should be in this order:
 - » zynq_mp_fsbl.elf
 - » system_wrapper.bit
 - » blinkbist.elf
 - » If any of these files are missing, add them
- Click Create Image



Creating a BOOT Image

- > If necessary, select the Bootgen console



Creating a BOOT Image

- > The BOOT.mcs is created

The screenshot shows the Xilinx SDK interface for the ZCU106_IPI SDK. The Project Explorer on the left lists various projects including blinkbist, hello_RTC, hello_uart_1, hello_uart_2, ipi_app, ipi_app_basic, lwip_echo_server, lwip_echo_server_bsp, standalone_bsp_0, standalone_bsp_1, standalone_bsp_2, system_wrapper_hw_platform_, and zynq_mp_dram_test. The Console tab in the center displays the command used to run Bootgen and its output. The output shows the command: cmd /C bootgen -image blinkbist.bif -arch zynqmp -o \C:\zcu106_ipi\zcu106_ipi.sdk\blinkbist\bootimage\BOOT.mcs -w on. It also includes the Xilinx Bootgen version information: Xilinx Bootgen v2018.2, Build date: Jun 14 2018-20:41:20, Copyright 1986-2018 Xilinx, Inc. All Rights Reserved, and a warning about deprecated fsbl_config options.

```
cmd /C bootgen -image blinkbist.bif -arch zynqmp -o \
C:\zcu106_ipi\zcu106_ipi.sdk\blinkbist\bootimage\BOOT.mcs -w on

***** Xilinx Bootgen v2018.2
**** Build date : Jun 14 2018-20:41:20
** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.

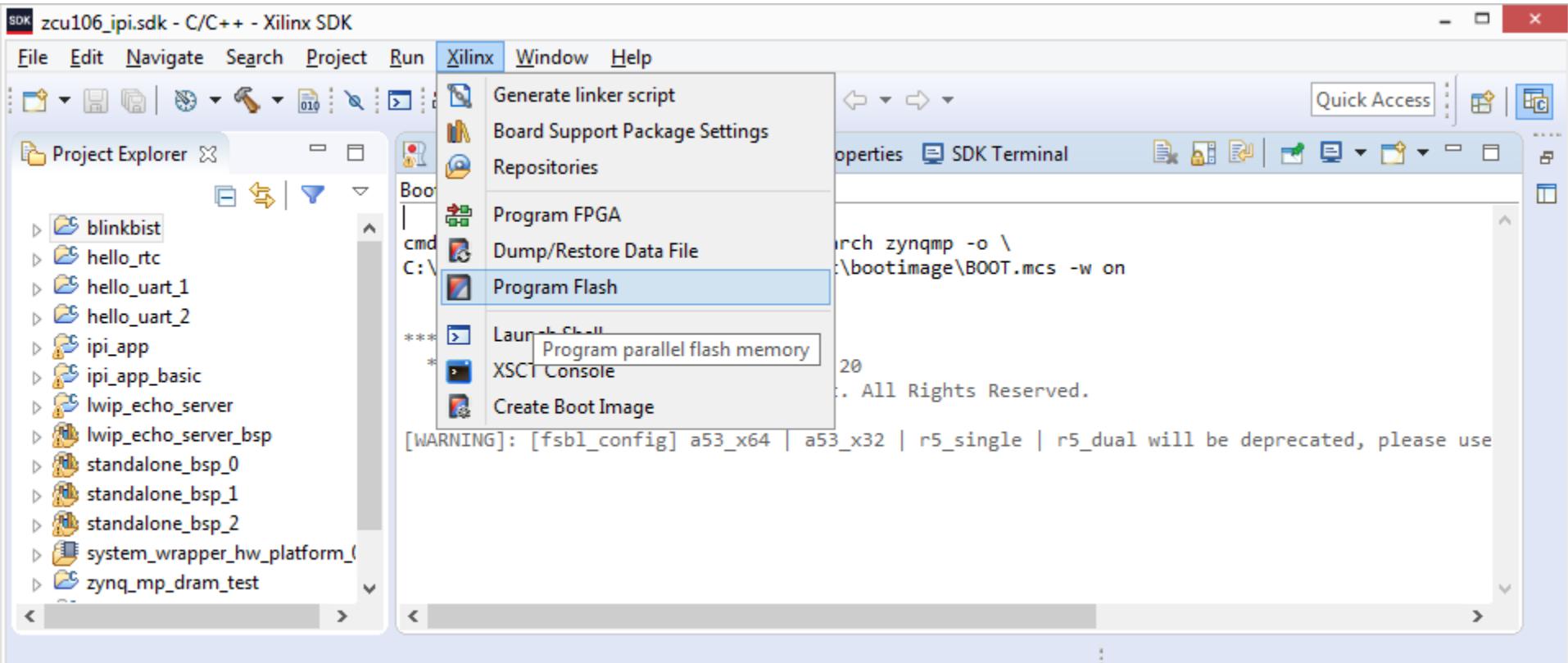
[WARNING]: [fsbl_config] a53_x64 | a53_x32 | r5_single | r5_dual will be deprecated, please use
```

Program ZCU106



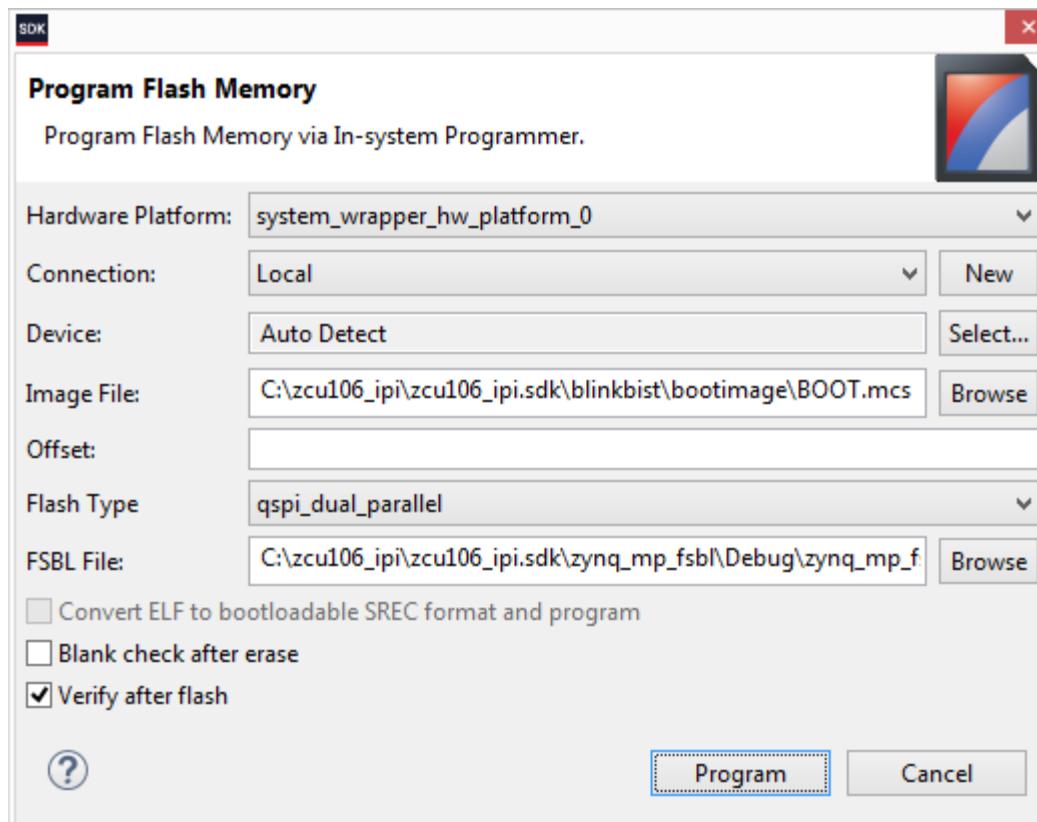
Programming the ZCU106 with Dual QSPI

- > Cycle ZCU106 power
- > Select Xilinx → Program Flash



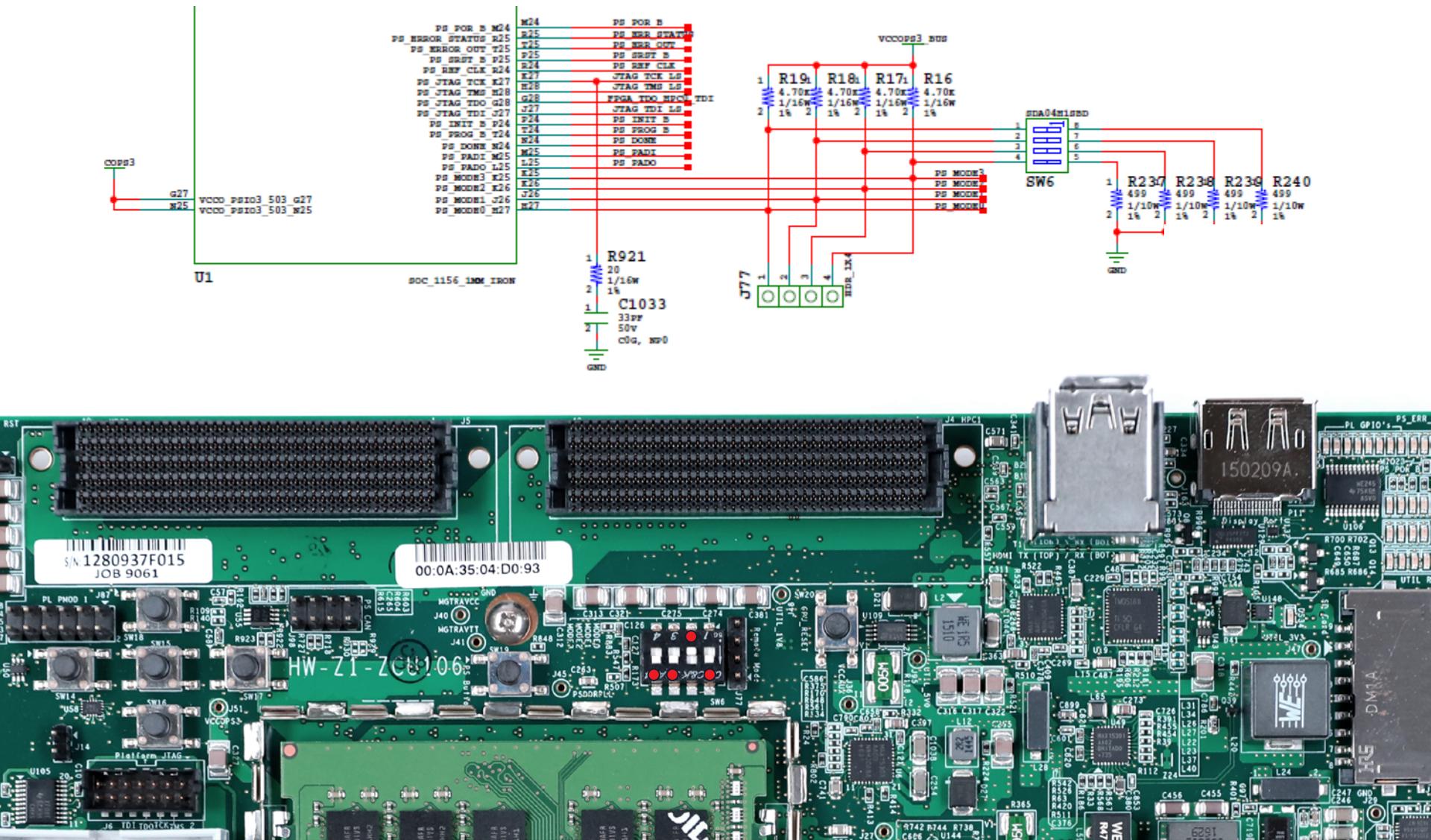
Programming the ZCU106 with Dual QSPI

- > Select the BOOT.mcs as the Image File
- > Select qspi_dual_parallel
- > Select the zynq_mp_fsbl.elf as the FSBL File
- > Select Verify after Flash
- > Click Program



Programming the ZCU106 with Dual QSPI

- Set SW6 to 0100 (0 = GND, Position 1 → Position 4) (Up, Down, Up, Up) to boot from QSPI



Programming the ZCU106 with Dual QSPI

- > Cycle power, and the Blink BIST program begins running
- > Follow the steps in the UG426, ZCU106 Quick Start Guide

STEP 4: Run the Built-In Self-Test

The BIST consists of a set of pass/fail tests that run sequentially. As each test passes, its corresponding LED glows green. If a test fails, its corresponding PL GPIO LED is off. The flashing LEDs are at the top right edge of the board. For SW13, up is ON or 1.

Note: To pass the PL DIP test, all the switches in SW13 must be up before any of them are moved down. The LEDs flash faster after you begin the DIP or pushbutton (PB) test.

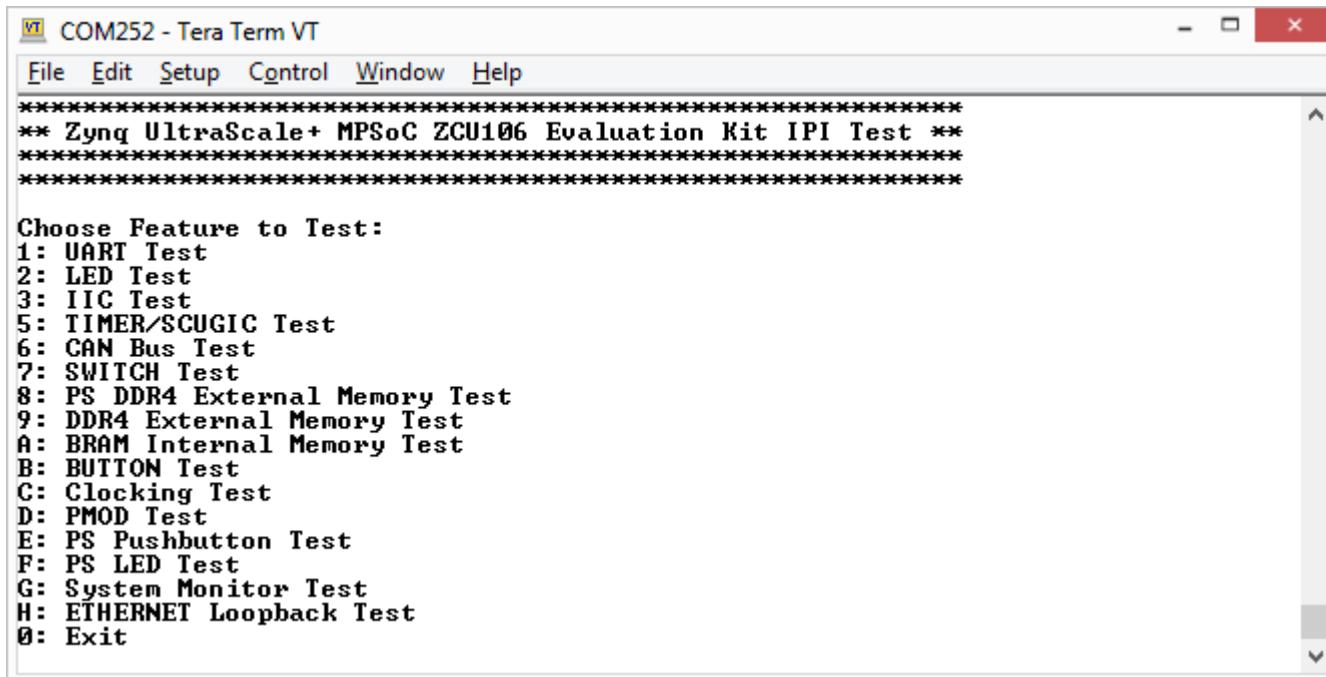
- The Clock, BRAM, PL-DDR4, PS-DDR4, Flash, and I2C tests run without user input.
- The DIP switch test (SW13) waits for you to move all the DIP switches toward the label ON, and then back.
- The PB test waits for you to push all the pushbuttons. The N, W, S, and E pushbuttons can be pushed in any order, but push the center button (SW15) last.
- The LED for the test that is waiting for your input slowly flashes on and off.

Self-Test Assignments for PL LEDs

MSB→LSB							
7	6	5	4	3	2	1	0
Clock	BRAM	PL-DDR4	PS-DDR4	Flash	I2C	DIP	PB

Program ZCU106 with IPI Design

- Once the Quick Start Guide steps are complete, you can view the IPI App in UART0 window



COM252 - Tera Term VT

File Edit Setup Control Window Help

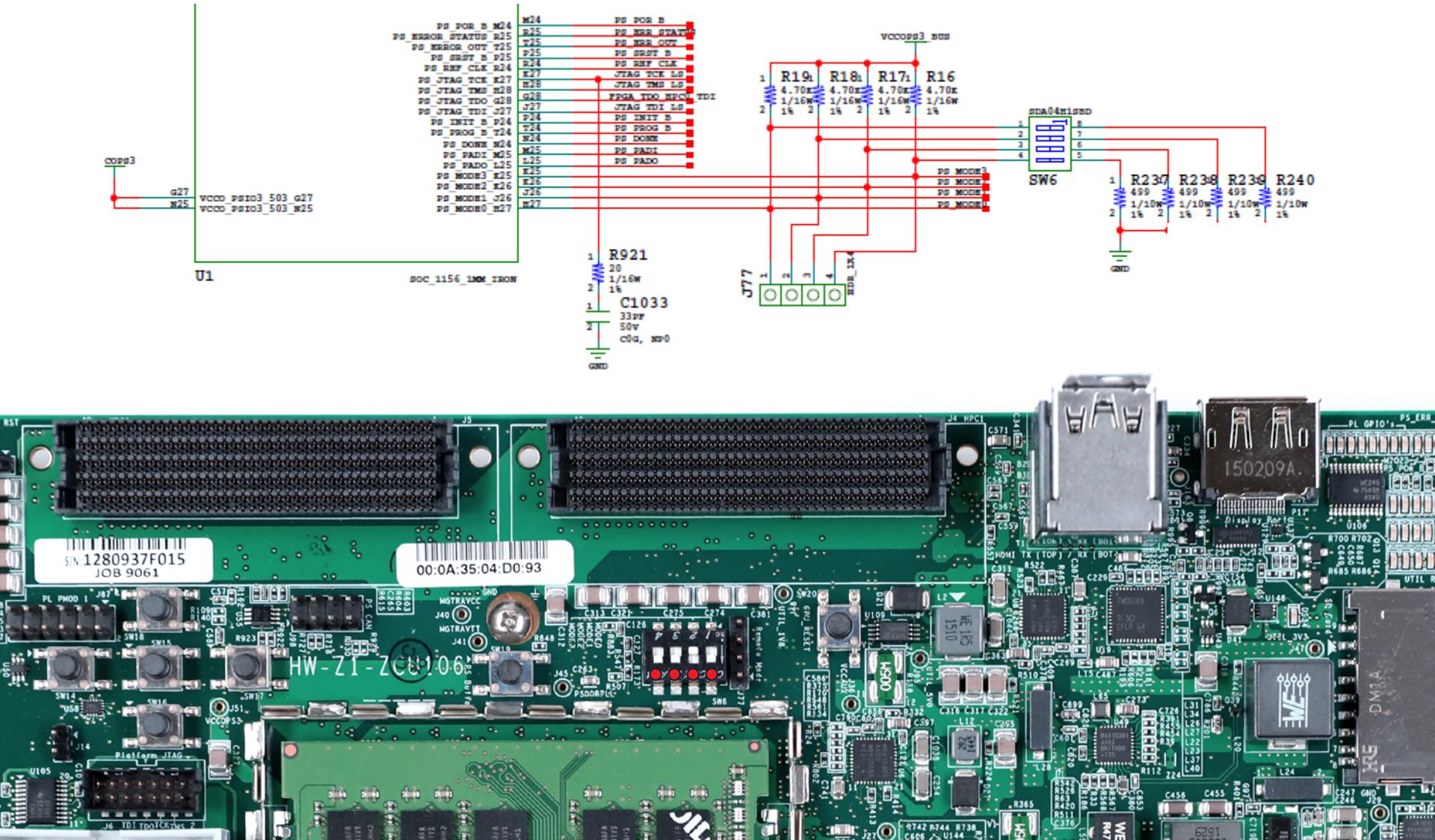
```
*****
** Zynq UltraScale+ MPSoC ZCU106 Evaluation Kit IPI Test **
*****
```

Choose Feature to Test:

- 1: UART Test
- 2: LED Test
- 3: IIC Test
- 5: TIMER/SCUGIC Test
- 6: CAN Bus Test
- 7: SWITCH Test
- 8: PS DDR4 External Memory Test
- 9: DDR4 External Memory Test
- A: BRAM Internal Memory Test
- B: BUTTON Test
- C: Clocking Test
- D: PMOD Test
- E: PS Pushbutton Test
- F: PS LED Test
- G: System Monitor Test
- H: ETHERNET Loopback Test
- 0: Exit

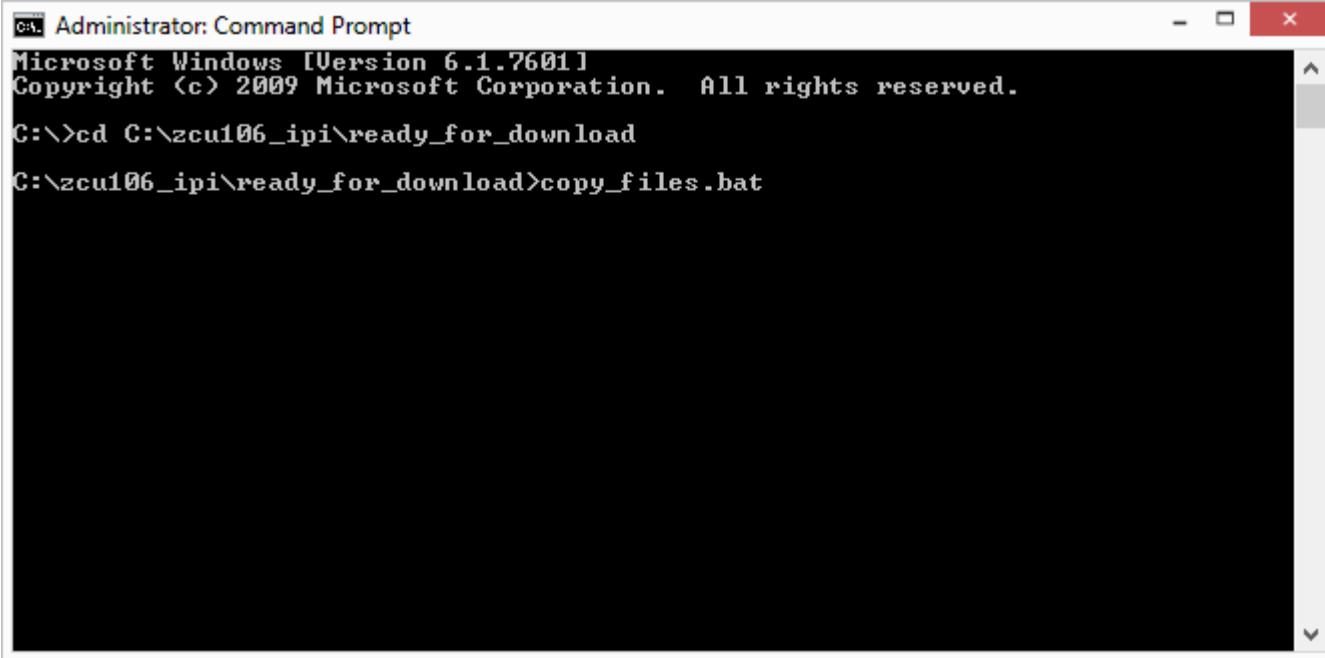
Programming the ZCU106 from Vivado

- > Set SW6 to 0000 (0 = GND, Position 1 → Position 4) (All Up)



Programming the ZCU106 from Vivado

- > Copy the files to the ready_for_download directory
- > Open a Windows CMD prompt and type:
cd C:\zcu106_ipi\ready_for_download
copy_files.bat



The screenshot shows a Windows Command Prompt window titled "Administrator: Command Prompt". The window displays the following text:

```
Administrator: Command Prompt
Microsoft Windows [Version 6.1.7601]
Copyright (c) 2009 Microsoft Corporation. All rights reserved.

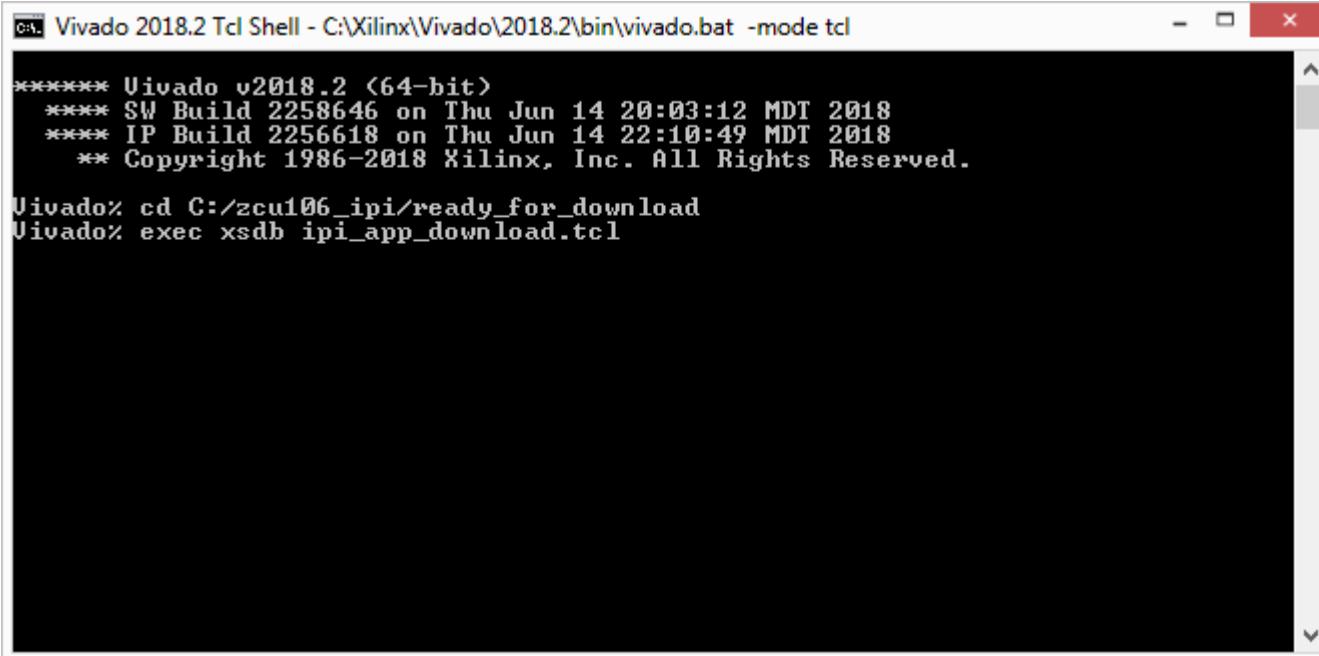
C:\>cd C:\zcu106_ipi\ready_for_download
C:\zcu106_ipi\ready_for_download>copy_files.bat
```

Programming the ZCU106 from Vivado

> Download the IPI bitstream

> In the Vivado Tcl Shell type:

```
cd C:/zcu106_ipi/ready_for_download  
exec xsdb ipi_app_download.tcl
```

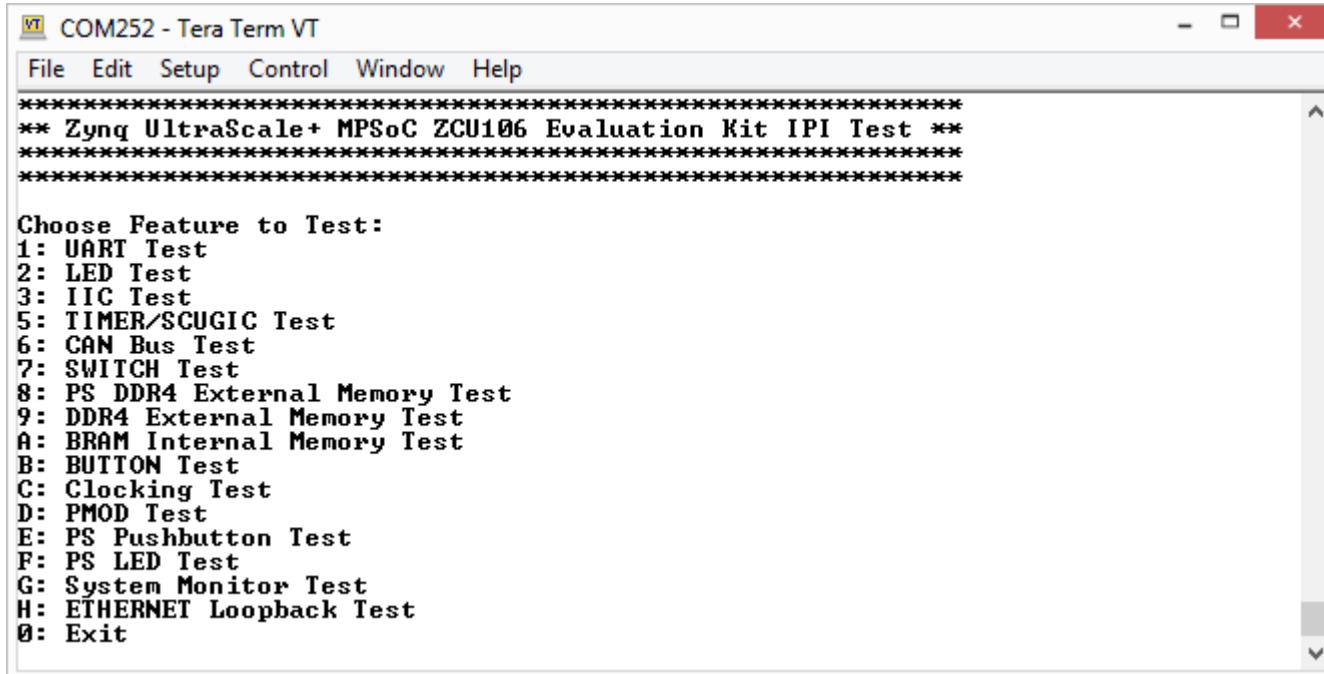


The screenshot shows a terminal window titled "Vivado 2018.2 Tcl Shell - C:\Xilinx\Vivado\2018.2\bin\vivado.bat -mode tcl". The window displays the following text:

```
***** Vivado v2018.2 (64-bit)  
**** SW Build 2258646 on Thu Jun 14 20:03:12 MDT 2018  
**** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018  
** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.  
  
Vivado> cd C:/zcu106_ipi/ready_for_download  
Vivado> exec xsdb ipi_app_download.tcl
```

Programming the ZCU106 from Vivado

- > The IPI Application runs in the terminal window

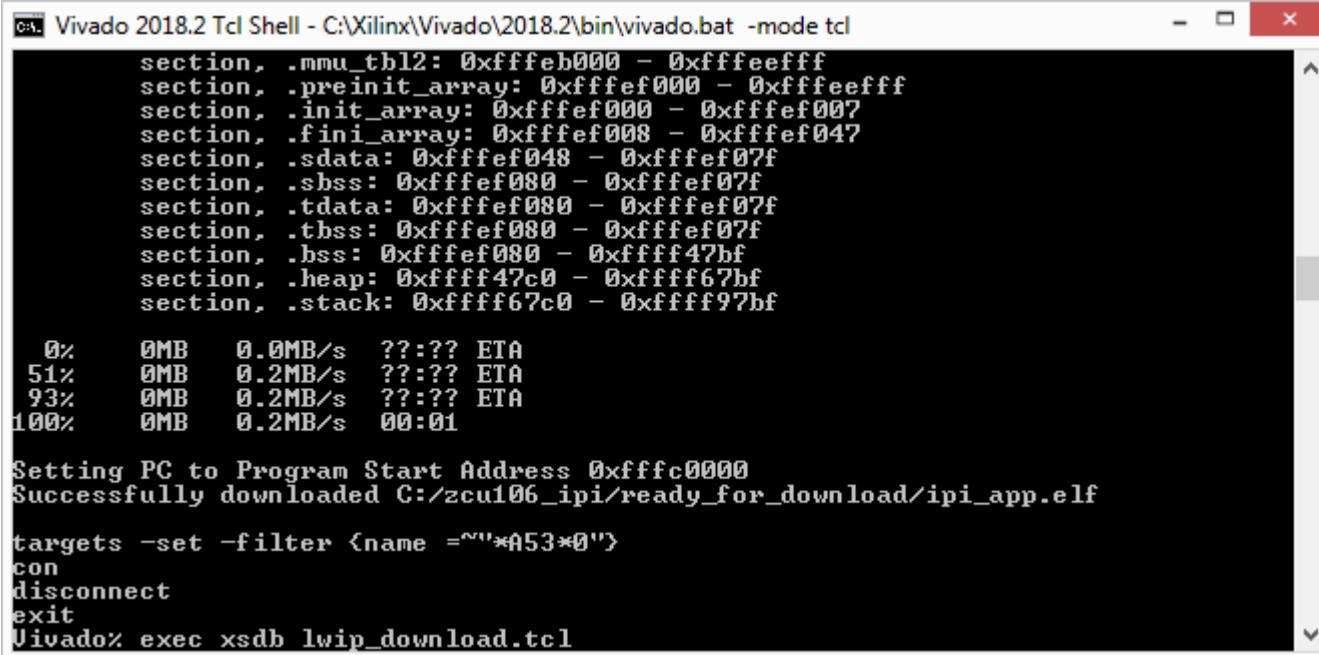


Run the LwIP Ethernet Design



Run the LwIP Ethernet Design

- > Download the LwIP bitstream
- > In the Vivado Tcl Shell type:
`exec xsdb lwip_download.tcl`



```
Vivado 2018.2 Tcl Shell - C:\Xilinx\Vivado\2018.2\bin\vivado.bat -mode tcl
section, .mmu_tbl2: 0xffffeb000 - 0xffffeefff
section, .preinit_array: 0xffffef000 - 0xffffeefff
section, .init_array: 0xffffef000 - 0xffffef007
section, .fini_array: 0xffffef008 - 0xffffef047
section, .sdata: 0xffffef048 - 0xffffef07f
section, .sbss: 0xffffef080 - 0xffffef07f
section, .tdata: 0xffffef080 - 0xffffef07f
section, .tbss: 0xffffef080 - 0xffffef07f
section, .bss: 0xffffef080 - 0xfffff47bf
section, .heap: 0xfffff47c0 - 0xfffff67bf
section, .stack: 0xfffff67c0 - 0xfffff97bf

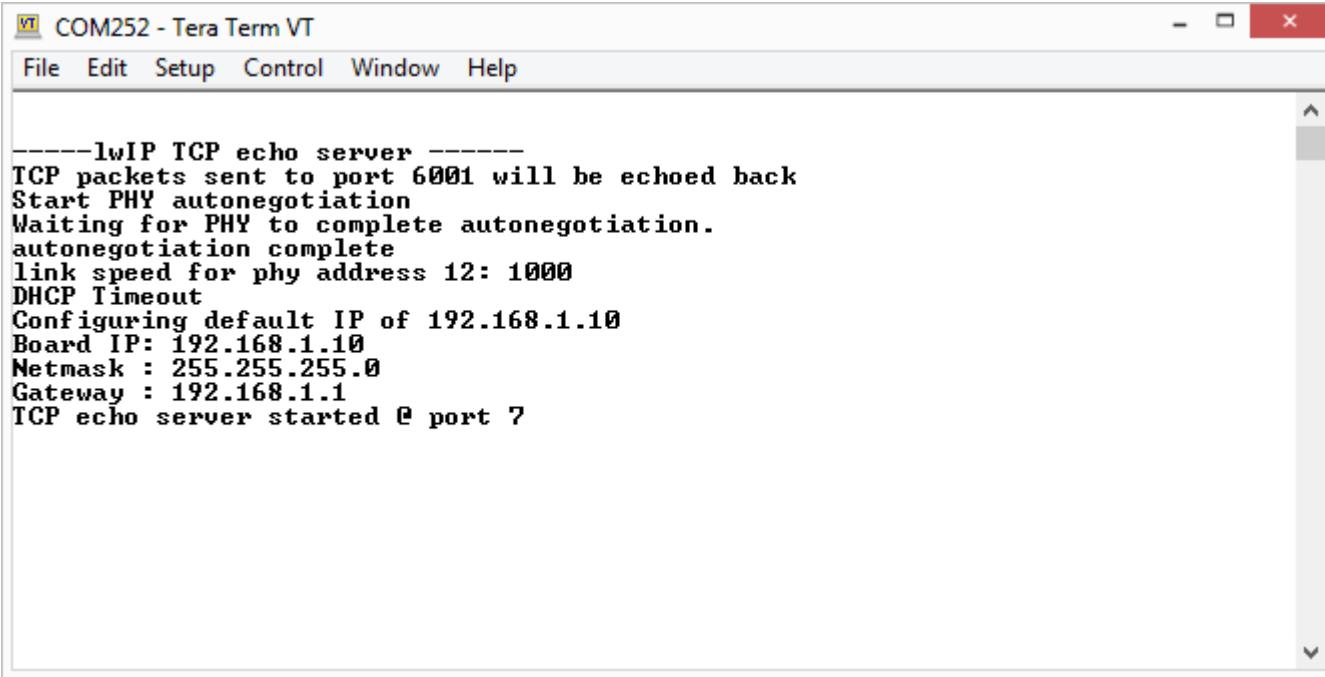
0%    0MB    0.0MB/s  ??:?? ETA
51%   0MB    0.2MB/s  ??:?? ETA
93%   0MB    0.2MB/s  ??:?? ETA
100%  0MB    0.2MB/s  00:01

Setting PC to Program Start Address 0xfffffc0000
Successfully downloaded C:/zcu106_ipi/ready_for_download/ipi_app.elf

targets -set -filter {name =~ "A53*0"}
con
disconnect
exit
Vivado% exec xsdb lwip_download.tcl
```

Run the LwIP Ethernet Design

- > View LwIP echo server screen



The screenshot shows a terminal window titled "COM252 - Tera Term VT". The window has a menu bar with "File", "Edit", "Setup", "Control", "Window", and "Help". The main pane displays the following text:

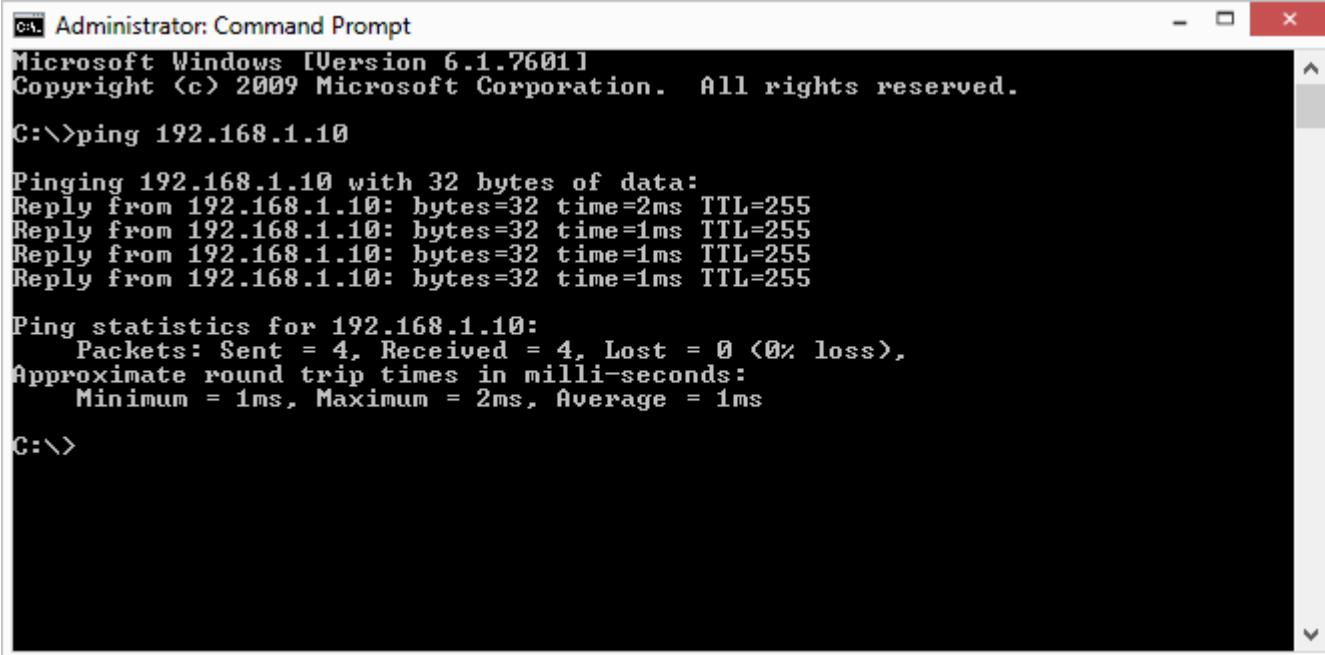
```
-----lwIP TCP echo server -----
TCP packets sent to port 6001 will be echoed back
Start PHY autonegotiation
Waiting for PHY to complete autonegotiation.
autonegotiation complete
link speed for phy address 12: 1000
DHCP Timeout
Configuring default IP of 192.168.1.10
Board IP: 192.168.1.10
Netmask : 255.255.255.0
Gateway : 192.168.1.1
TCP echo server started @ port 7
```

Run the LwIP Ethernet Design

- > From a DOS window on the PC Host, enter the command:

ping 192.168.1.10

» Ping from PC host 192.168.1.2 to ZCU106 target 192.168.1.10



```
C:\>Administrator: Command Prompt
Microsoft Windows [Version 6.1.7601]
Copyright <c> 2009 Microsoft Corporation. All rights reserved.

C:>ping 192.168.1.10

Pinging 192.168.1.10 with 32 bytes of data:
Reply from 192.168.1.10: bytes=32 time=2ms TTL=255
Reply from 192.168.1.10: bytes=32 time=1ms TTL=255
Reply from 192.168.1.10: bytes=32 time=1ms TTL=255
Reply from 192.168.1.10: bytes=32 time=1ms TTL=255

Ping statistics for 192.168.1.10:
    Packets: Sent = 4, Received = 4, Lost = 0 (0% loss),
    Approximate round trip times in milli-seconds:
        Minimum = 1ms, Maximum = 2ms, Average = 1ms

C:>
```

Note: Don't ping LwIP while it is initializing

References



References

> IP Integrator Documentation

- » Vivado Design Suite Tcl Command Reference Guide – UG835
 - https://www.xilinx.com/support/documentation/sw_manuals/xilinx2018_2/ug835-vivado-tcl-commands.pdf
- » Designing IP Subsystems Using IP Integrator – UG994
 - https://www.xilinx.com/support/documentation/sw_manuals/xilinx2018_2/ug994-vivado-ip-subsystems.pdf

> Vivado Release Notes

- » Vivado Design Suite User Guide - Release Notes – UG973
 - https://www.xilinx.com/support/documentation/sw_manuals/xilinx2018_2/ug973-vivado-release-notes-install-license.pdf
- » Vivado Design Suite 2018 - Vivado Known Issues
 - <https://www.xilinx.com/support/answers/70860.html>

Documentation



Documentation

> Zynq UltraScale+

- » Zynq UltraScale+ MPSoC
 - <http://www.xilinx.com/products/silicon-devices/soc/zynq-ultrascale-mpsoc.html>

> ZCU106 Documentation

- » Xilinx Zynq UltraScale+ MPSoC ZCU106 Evaluation Kit
 - <https://www.xilinx.com/products/boards-and-kits/zcu106.html>
- » ZCU106 Board User Guide – UG1244
 - https://www.xilinx.com/support/documentation/boards_and_kits/zcu106/ug1244-zcu106-eval-bd.pdf
- » ZCU106 Evaluation Kit Quick Start Guide User Guide – XTP472
 - https://www.xilinx.com/support/documentation/boards_and_kits/zcu106/xtp472-zcu106-quickstart.pdf