

Vector Display Processor Project

Project Group: Group 19

Project Member:

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Top Level Design

Synthesis VDP RTL

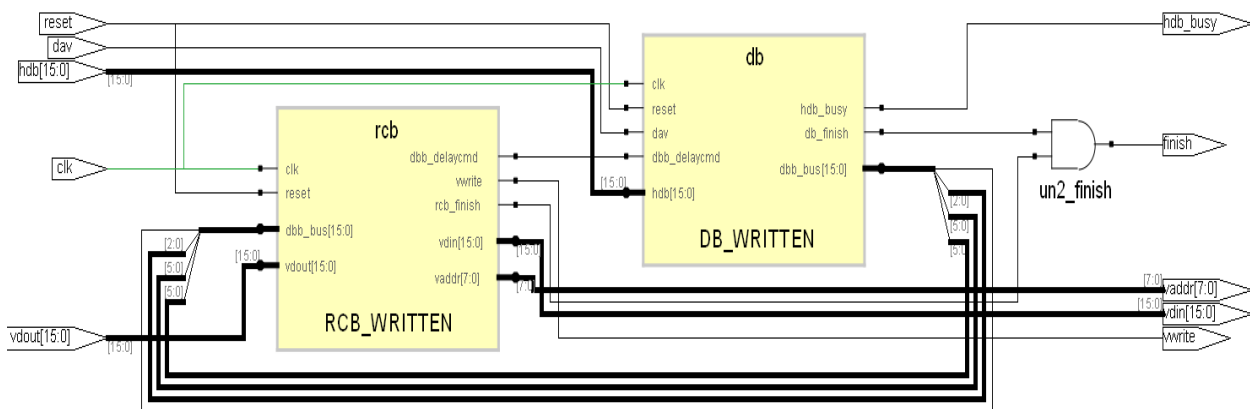


Figure 1 VDP Synthesis RTL

Clock frequency required for VDP

```
1 # Synopsys Constraint Checker(syntax only), version maprc, Build 1911R, built Nov 26 2013
2 # Copyright (C) 1994-2013, Synopsys, Inc. This software and the associated documentation are prop:
3
4 # Written on Mon Mar 21 16:38:02 2016
5
6
7 ##### DESIGN INFO #####
8
9 Top View: "vdp"
10 Constraint File(s): (none)
11
12 #Run constraint checker to find more issues with constraints.
13 #####
14
15
16
17 No issues found in constraint syntax.
18
19
20
21 Clock Summary
22 *****
23
24 Start Requested Requested Clock Clock
25 Clock Frequency Period Type Group
26 -----
27 vdp|clk 120.6 MHz 8.290 inferred Autoconstr_clkgroup_0
28 -----
```

Post-synthesis Modelsim Results

[illegible]

Pre-synthesis Modelsim Results

Instance	Design unit	Design unit type	Visibility	Cover Options	Total coverage	Assertion hits	Assertion misses
vdp_testbench	vdp_testbe...	Architecture	+acc=	+cover=bcefst	89.7%	2	
RAM1	vram(behav)	Architecture	+acc=<... +cover=bcefst		92.5%	1	
DUT	vdp(rtl)	Architecture	+acc=	+cover=bcefst	89.0%		
DB_WRITE	db(rtl)	Architecture	+acc=<... +cover=bcefst		91.1%		
RCB_WRITE	rcb(rtl)	Architecture	+acc=<... +cover=bcefst		91.8%		
line__79	vdp(rtl)	Process	+acc=				
P_RST_CLK	vdp_testbe...	Process	+acc=				
MAIN	vdp_testbe...	Process	+acc=				
standard	standard	Package	+acc=<... +cover=<none>				
textio	textio	Package	+acc=<... +cover=<none>				
std_logic_1164	std_logic_1...	Package	+acc=<... +cover=<none>				
numeric_std	numeric_std	Package	+acc=<... +cover=<none>				
utility_pack	utility_pack	Package	+acc=<... +cover=bcefst		12.7%		
deallocate	[work.utility...	Subprogram	+acc=<... +cover=bcefst		12.7%		
"/="	[work.utility...	Subprogram	+acc=<... +cover=bcefst		12.7%		
"="	[work.utility...	Subprogram	+acc=<... +cover=bcefst		12.7%		
maximum	[INTEGER, I...	Subprogram	+acc=<... +cover=bcefst		100.0%		
minimum	[INTEGER, I...	Subprogram	+acc=<... +cover=bcefst		100.0%		
random	[INTEGER, I...	Subprogram	+acc=<... +cover=bcefst		0.0%		
ones_mask	[INTEGER, I...	Subprogram	+acc=<... +cover=bcefst		0.0%		

```

*****
***+*****+*****+*****+*****+*****+*****+*****+*****+*****+
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***+*****+*****+*****+*****+*****+*****+*****+*****+*****+
** Note: Bad character (I) should be [DMC] in col 1, line 82
Time: 21715 ns Iteration: 1 Instance: /vdp_testbench
** Note: Bad character (B) should be [DMC] in col 1, line 108
Time: 21715 ns Iteration: 1 Instance: /vdp_testbench
** Note: Bad character (B) should be [DMC] in col 1, line 123
Time: 21715 ns Iteration: 1 Instance: /vdp_testbench
** Note: Bad character (I) should be [DMC] in col 1, line 129
Time: 21715 ns Iteration: 1 Instance: /vdp_testbench
** Note: Bad character (I) should be [DMC] in col 1, line 133
Time: 21715 ns Iteration: 1 Instance: /vdp_testbench
** Note: Bad character (I) should be [DMC] in col 1, line 143
Time: 21715 ns Iteration: 1 Instance: /vdp_testbench
** Note: Bad character (I) should be [DMC] in col 1, line 160
Time: 21715 ns Iteration: 1 Instance: /vdp_testbench
** Note: Bad character (I) should be [DMC] in col 1, line 167
Time: 21715 ns Iteration: 1 Instance: /vdp_testbench
** Note: Commands from: sample_host_commands.txt, VDP PASSED.
Time: 21715 ns Iteration: 1 Instance: /vdp_testbench
** Failure: Test finished normally.
Time: 21715 ns Iteration: 1 Process: /vdp_testbench/MAIN File: H:/vhdl_coursework/vdp_prj2beha/vdp_1
Break in Process MAIN at H:/vhdl_coursework/vdp_prj2beha/vdp_testbench.vhd line 212
  
```