Vector Display Processor Project

Project Group: Group 19

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Top Level Design

Synthesis VDP RTL

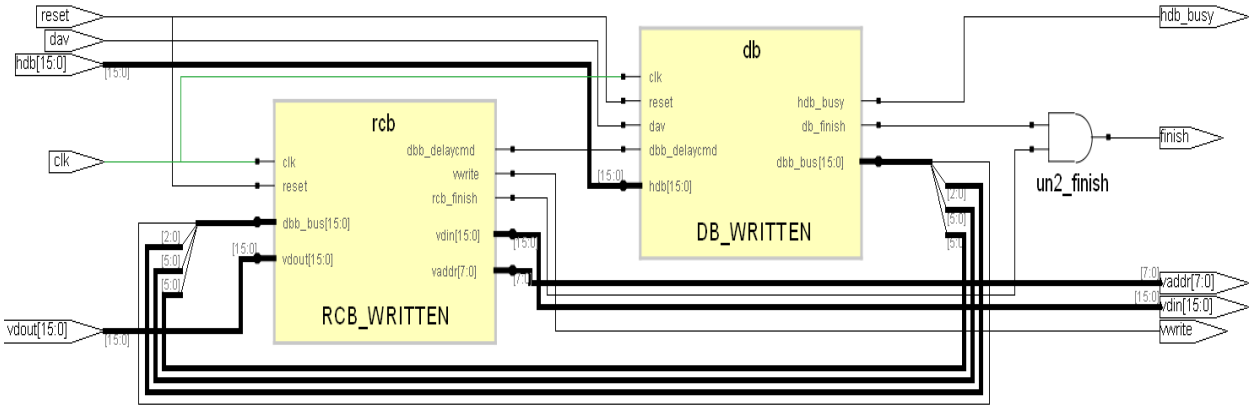

Figure 1 VDP Synthesis RTL

Clock frequency required for VDP

```
# Synopsys Constraint Checker(syntax only), version maprc, Build 1911R, built Nov 26 2013
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# Written on Mon Mar 21 16:38:02 2016


##### DESIGN INFO ############################################################

Top View:                "vdp"
Constraint File(s):      (none)

#Run constraint checker to find more issues with constraints.
##############################################################################



No issues found in constraint syntax.



Clock Summary
**************

Start       Requested     Requested     Clock        Clock
Clock       Frequency     Period        Type         Group
------------------------------------------------------------------------------
vdp|clk     120.6 MHz     8.290         inferred     Autoconstr_clkgroup_0
==============================================================================
```
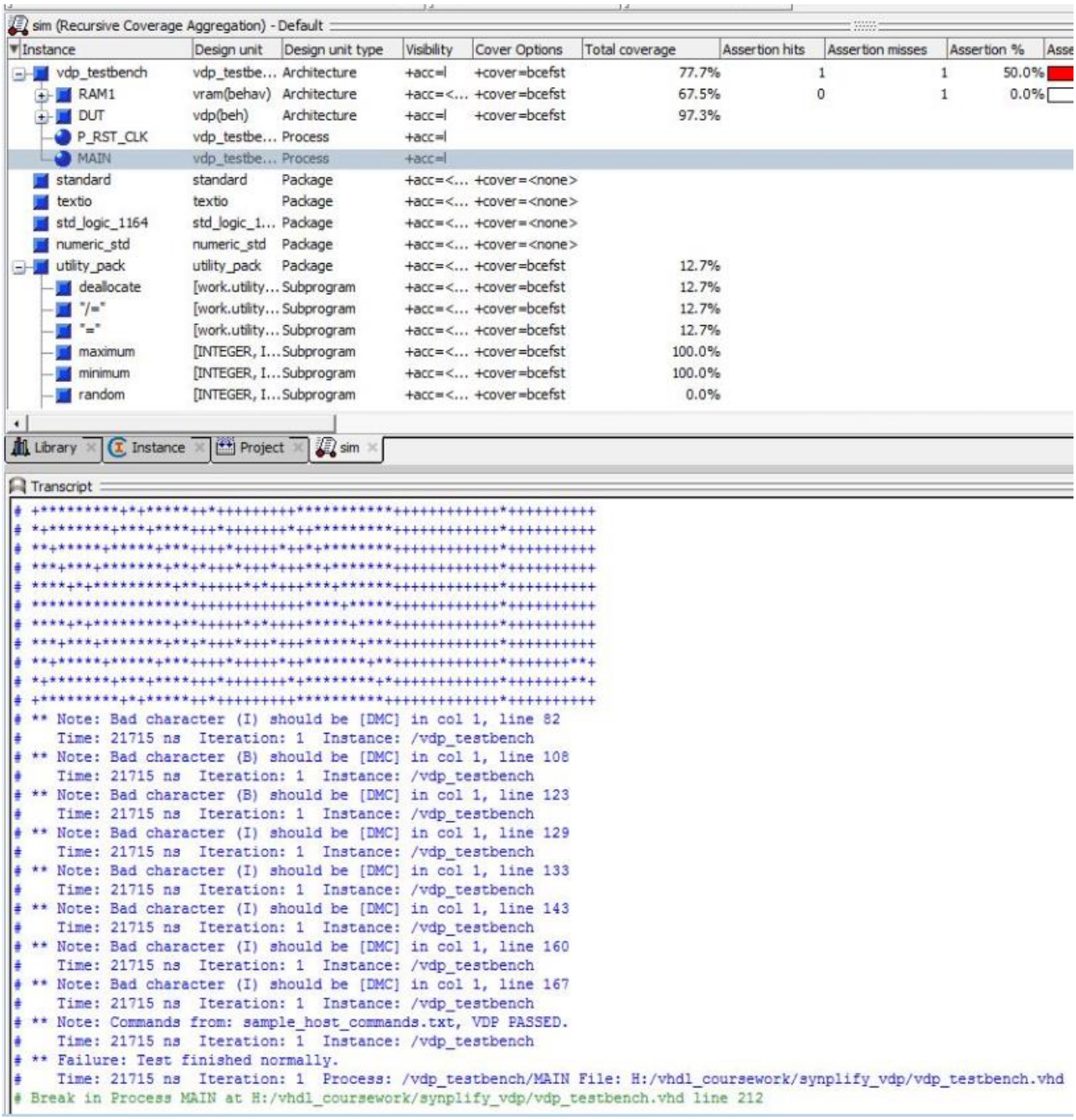

Post-synthesis Modelsim Results



Pre-synthesis Modelsim Results