



## 1. Description

### 1.1. Project

Project Name	I4_BCC
Board Name	NUCLEO-F411RE
Generated with:	STM32CubeMX 6.8.1
Date	05/14/2023

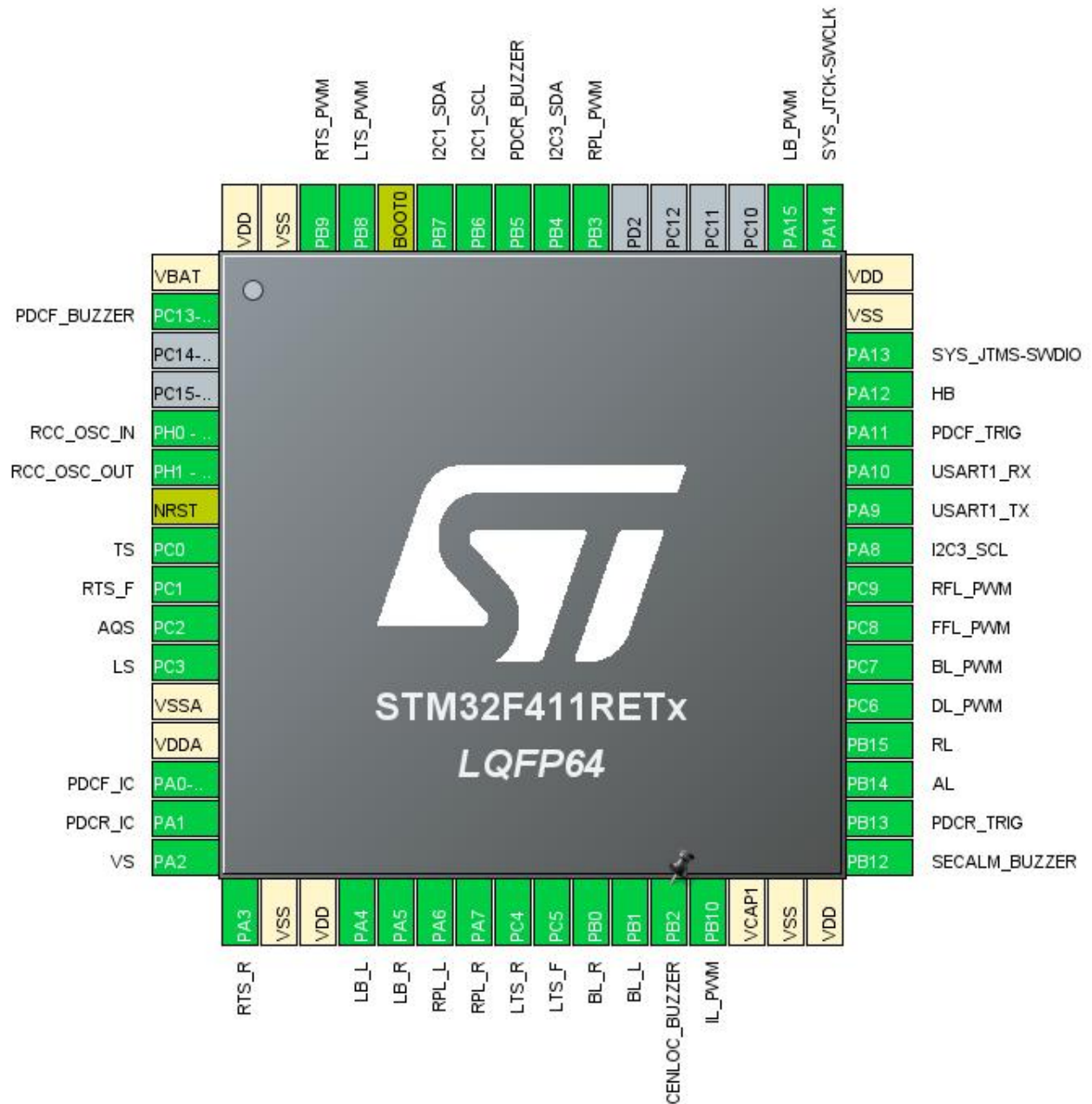
### 1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F411
MCU name	STM32F411RETx
MCU Package	LQFP64
MCU Pin number	64

### 1.3. Core(s) information

Core(s)	Arm Cortex-M4
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## 2. Pinout Configuration



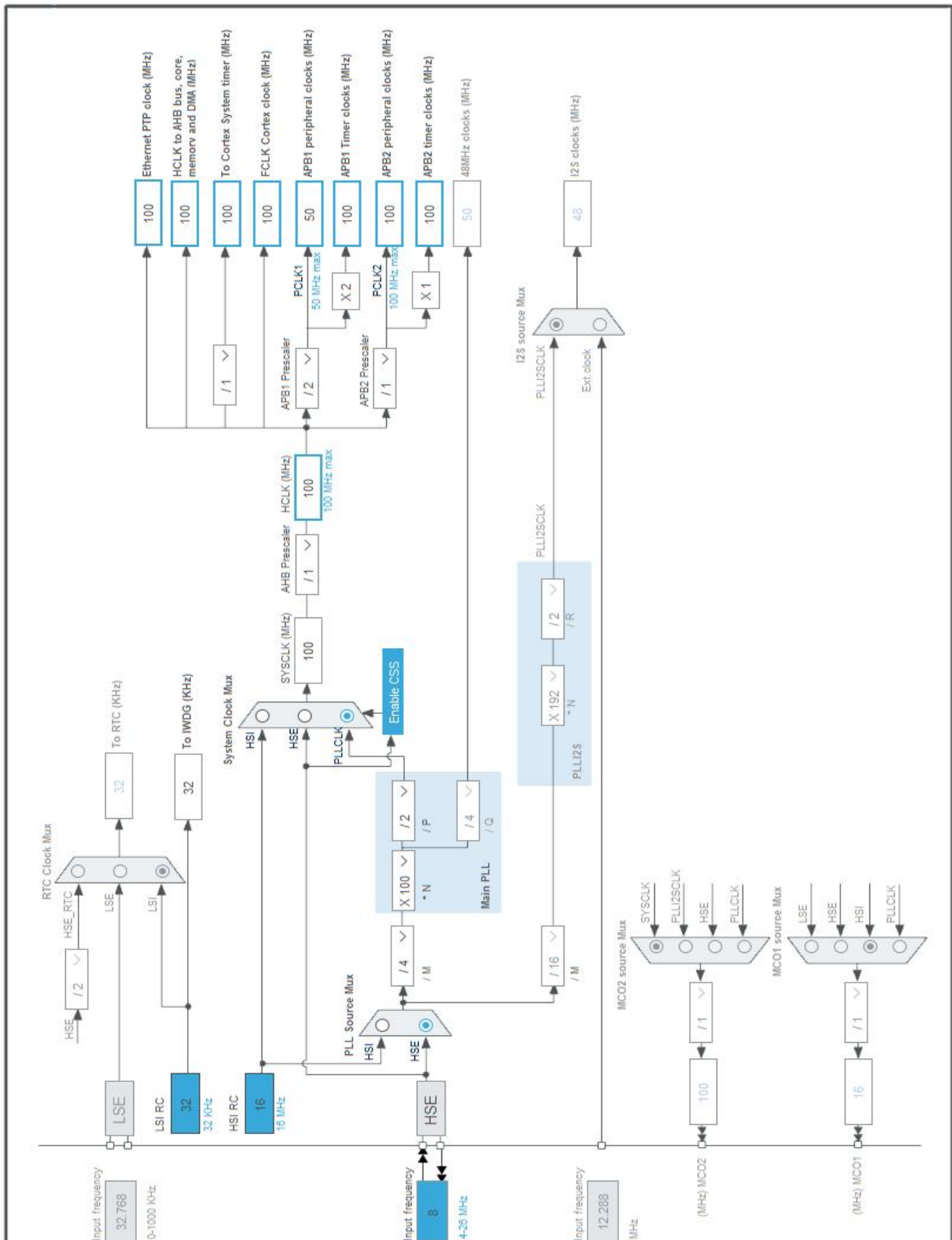
### 3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13-ANTI_TAMP *	I/O	GPIO_Output	PDCF_BUZZER
5	PH0 - OSC_IN	I/O	RCC_OSC_IN	
6	PH1 - OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	PC0	I/O	ADC1_IN10	TS
9	PC1	I/O	ADC1_IN11	RTS_F
10	PC2	I/O	ADC1_IN12	AQS
11	PC3	I/O	ADC1_IN13	LS
12	VSSA	Power		
13	VDDA	Power		
14	PA0-WKUP	I/O	TIM5_CH1	PDCF_IC
15	PA1	I/O	TIM5_CH2	PDCR_IC
16	PA2	I/O	ADC1_IN2	VS
17	PA3	I/O	ADC1_IN3	RTS_R
18	VSS	Power		
19	VDD	Power		
20	PA4	I/O	ADC1_IN4	LB_L
21	PA5	I/O	ADC1_IN5	LB_R
22	PA6	I/O	ADC1_IN6	RPL_L
23	PA7	I/O	ADC1_IN7	RPL_R
24	PC4	I/O	ADC1_IN14	LTS_R
25	PC5	I/O	ADC1_IN15	LTS_F
26	PB0	I/O	ADC1_IN8	BL_R
27	PB1	I/O	ADC1_IN9	BL_L
28	PB2 *	I/O	GPIO_Output	CENLOC_BUZZER
29	PB10	I/O	TIM2_CH3	IL_PWM
30	VCAP1	Power		
31	VSS	Power		
32	VDD	Power		
33	PB12 *	I/O	GPIO_Output	SECALM_BUZZER
34	PB13 *	I/O	GPIO_Output	PDCR_TRIG
35	PB14 *	I/O	GPIO_Output	AL
36	PB15 *	I/O	GPIO_Output	RL
37	PC6	I/O	TIM3_CH1	DL_PWM
38	PC7	I/O	TIM3_CH2	BL_PWM

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
39	PC8	I/O	TIM3_CH3	FFL_PWM
40	PC9	I/O	TIM3_CH4	RFL_PWM
41	PA8	I/O	I2C3_SCL	
42	PA9	I/O	USART1_TX	
43	PA10	I/O	USART1_RX	
44	PA11 *	I/O	GPIO_Output	PDCF_TRIG
45	PA12 *	I/O	GPIO_Output	HB
46	PA13	I/O	SYS_JTMS-SWDIO	
47	VSS	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	
50	PA15	I/O	TIM2_CH1	LB_PWM
55	PB3	I/O	TIM2_CH2	RPL_PWM
56	PB4	I/O	I2C3_SDA	
57	PB5 *	I/O	GPIO_Output	PDCR_BUZZER
58	PB6	I/O	I2C1_SCL	
59	PB7	I/O	I2C1_SDA	
60	BOOT0	Boot		
61	PB8	I/O	TIM4_CH3	LTS_PWM
62	PB9	I/O	TIM4_CH4	RTS_PWM
63	VSS	Power		
64	VDD	Power		

\* The pin is affected with an I/O function

## 4. Clock Tree Configuration



## 5. Software Project

### 5.1. Project Settings

Name	Value
Project Name	I4_BCC
Project Folder	C:\Users\Daniel\Documents\BMW\I4\I4_BCC_WORKSPACE\I4_BCC
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.27.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

### 5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Add necessary library files as reference in the toolchain project configuration file
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	Yes
Enable Full Assert	No

### 5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_TIM2_Init	TIM2
5	MX_TIM3_Init	TIM3
6	MX_TIM4_Init	TIM4
7	MX_ADC1_Init	ADC1
8	MX_CRC_Init	CRC
9	MX_USART1_UART_Init	USART1
10	MX_TIM5_Init	TIM5
11	MX_I2C1_Init	I2C1

Rank	Function Name	Peripheral Instance Name
12	MX_I2C3_Init	I2C3
13	MX_IWDG_Init	IWDG



## 6. Power Consumption Calculator report

### 6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F411
MCU	STM32F411RETx
Datasheet	DS10314_Rev6

### 6.2. Parameter Selection

Temperature	25
Vdd	1.7

### 6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

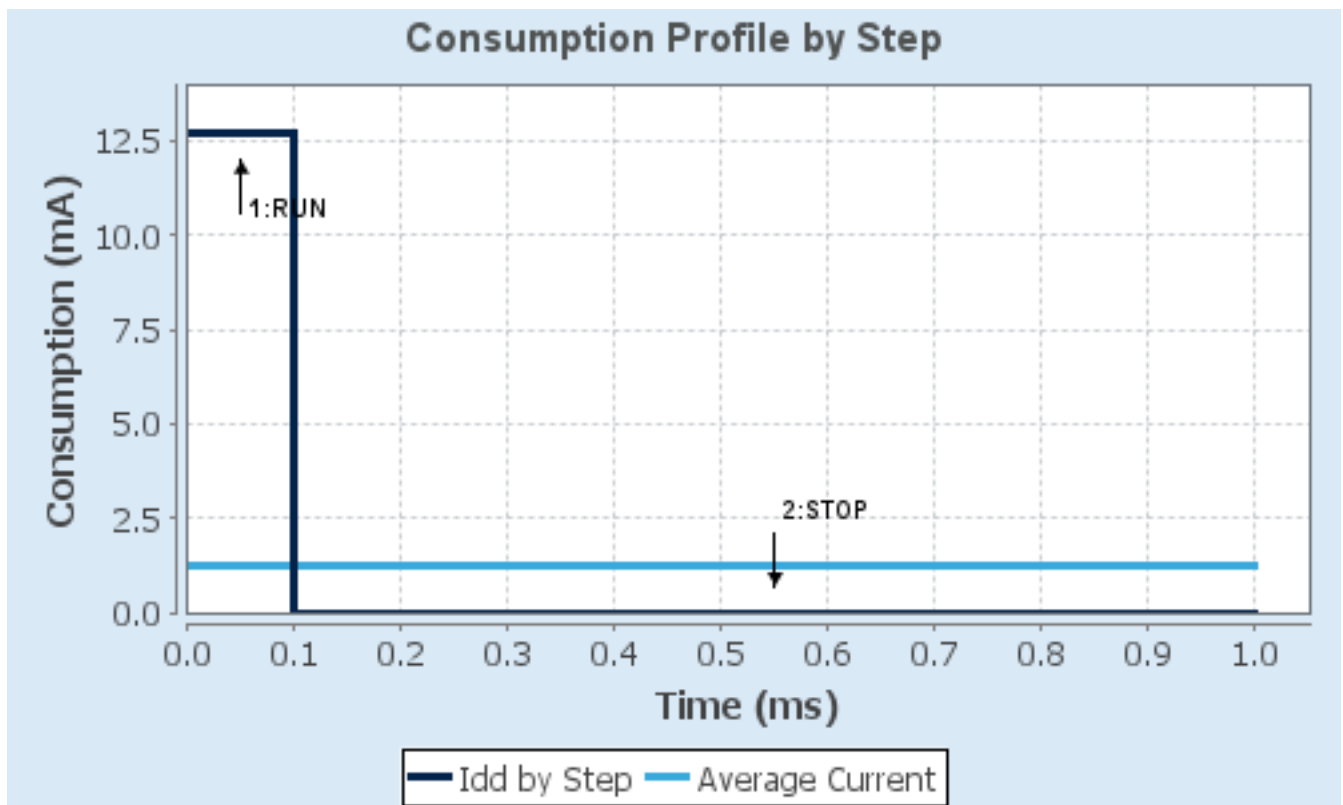
#### 6.4. Sequence

<b>Step</b>	Step1	Step2
<b>Mode</b>	RUN	STOP
<b>Vdd</b>	1.7	1.7
<b>Voltage Source</b>	Battery	Battery
<b>Range</b>	Scale1-High	No Scale
<b>Fetch Type</b>	SRAM	n/a
<b>CPU Frequency</b>	100 MHz	0 Hz
<b>Clock Configuration</b>	HSE PLL	Regulator_LPLV Flash-PwrDwn
<b>Clock Source Frequency</b>	4 MHz	0 Hz
<b>Peripherals</b>		
<b>Additional Cons.</b>	0 mA	0 mA
<b>Average Current</b>	12.7 mA	9 $\mu$ A
<b>Duration</b>	0.1 ms	0.9 ms
<b>DMIPS</b>	125.0	0.0
<b>Ta Max</b>	103.99	105
<b>Category</b>	In DS Table	In DS Table

#### 6.5. Results

Sequence Time	1 ms	Average Current	1.28 mA
Battery Life	3 months, 19 days, 6 hours	Average DMIPS	125.0 DMIPS

#### 6.6. Chart



## 7. Peripherals and Middlewares Configuration

### 7.1. ADC1

mode: IN2

mode: IN3

mode: IN4

mode: IN5

mode: IN6

mode: IN7

mode: IN8

mode: IN9

mode: IN10

mode: IN11

mode: IN12

mode: IN13

mode: IN14

mode: IN15

#### 7.1.1. Parameter Settings:

##### ADCs\_Common\_Settings:

Mode Independent mode

##### ADC\_Settings:

Clock Prescaler **PCLK2 divided by 8 \***

Resolution 12 bits (15 ADC Clock cycles)

Data Alignment Right alignment

Scan Conversion Mode Enabled

Continuous Conversion Mode **Enabled \***

Discontinuous Conversion Mode Disabled

DMA Continuous Requests **Enabled \***

End Of Conversion Selection EOC flag at the end of single channel conversion

##### ADC\_Regular\_ConversionMode:

Number Of Conversion **14 \***

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None

Rank 1

Channel **Channel 13 \***

Sampling Time **480 Cycles \***

Rank **2 \***

Channel	Channel 2
Sampling Time	<b>480 Cycles *</b>
<u>Rank</u>	<b>3 *</b>
Channel	<b>Channel 12 *</b>
Sampling Time	<b>480 Cycles *</b>
<u>Rank</u>	<b>4 *</b>
Channel	<b>Channel 10 *</b>
Sampling Time	<b>480 Cycles *</b>
<u>Rank</u>	<b>5 *</b>
Channel	<b>Channel 4 *</b>
Sampling Time	<b>480 Cycles *</b>
<u>Rank</u>	<b>6 *</b>
Channel	<b>Channel 5 *</b>
Sampling Time	<b>480 Cycles *</b>
<u>Rank</u>	<b>7 *</b>
Channel	<b>Channel 6 *</b>
Sampling Time	<b>480 Cycles *</b>
<u>Rank</u>	<b>8 *</b>
Channel	<b>Channel 7 *</b>
Sampling Time	<b>480 Cycles *</b>
<u>Rank</u>	<b>9 *</b>
Channel	<b>Channel 8 *</b>
Sampling Time	<b>480 Cycles *</b>
<u>Rank</u>	<b>10 *</b>
Channel	<b>Channel 9 *</b>
Sampling Time	<b>480 Cycles *</b>
<u>Rank</u>	<b>11 *</b>
Channel	<b>Channel 15 *</b>
Sampling Time	<b>480 Cycles *</b>
<u>Rank</u>	<b>12 *</b>
Channel	<b>Channel 14 *</b>
Sampling Time	<b>480 Cycles *</b>
<u>Rank</u>	<b>13 *</b>
Channel	<b>Channel 3 *</b>
Sampling Time	<b>480 Cycles *</b>
<u>Rank</u>	<b>14 *</b>

Channel	<b>Channel 11 *</b>
Sampling Time	<b>480 Cycles *</b>
<b>ADC_Injected_ConversionMode:</b>	
Number Of Conversions	0
<b>WatchDog:</b>	
Enable Analog WatchDog Mode	false

## 7.2. CRC

**mode: Activated**

## 7.3. I2C1

### I2C: I2C

#### 7.3.1. Parameter Settings:

**Master Features:**

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

**Slave Features:**

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

## 7.4. I2C3

### I2C: I2C

#### 7.4.1. Parameter Settings:

**Master Features:**

I2C Speed Mode	<b>Fast Mode *</b>
I2C Clock Speed (Hz)	400000
Fast Mode Duty Cycle	Duty cycle Tlow/Thigh = 2

**Slave Features:**

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled

Primary slave address	0
General Call address detection	Disabled

## 7.5. IWDG

**mode: Activated**

### 7.5.1. Parameter Settings:

#### **Clocking:**

IWDG counter clock prescaler	<b>128 *</b>
IWDG down-counter reload value	<b>63 *</b>

## 7.6. RCC

**High Speed Clock (HSE): Crystal/Ceramic Resonator**

### 7.6.1. Parameter Settings:

#### **System Parameters:**

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	3 WS (4 CPU cycle)

#### **RCC Parameters:**

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

#### **Power Parameters:**

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
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## 7.7. SYS

**Debug: Serial Wire**

**Timebase Source: TIM1**

## 7.8. TIM2

**Clock Source : Internal Clock**

**Channel1: PWM Generation CH1**

**Channel2: PWM Generation CH2**

**Channel3: PWM Generation CH3**

### 7.8.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value)	<b>10000-1 *</b>
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value )	<b>200-1 *</b>
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

#### **Trigger Output (TRGO) Parameters:**

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

#### **PWM Generation Channel 1:**

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	<b>Enable *</b>
CH Polarity	High

#### **PWM Generation Channel 2:**

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	<b>Enable *</b>
CH Polarity	High

#### **PWM Generation Channel 3:**

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	<b>Enable *</b>
CH Polarity	High

## **7.9. TIM3**

**Clock Source : Internal Clock**

**Channel1: PWM Generation CH1**



## Channel2: PWM Generation CH2

## Channel3: PWM Generation CH3

## Channel4: PWM Generation CH4

### 7.9.1. Parameter Settings:

#### Counter Settings:

Prescaler (PSC - 16 bits value)	<b>10000-1 *</b>
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	<b>200-1 *</b>
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

#### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

#### PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	<b>Enable *</b>
CH Polarity	High

#### PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	<b>Enable *</b>
CH Polarity	High

#### PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	<b>Enable *</b>
CH Polarity	High

#### PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	<b>Enable *</b>
CH Polarity	High

## 7.10. TIM4

**mode: Clock Source**

**Channel3: PWM Generation CH3**

**Channel4: PWM Generation CH4**

### 7.10.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value)	<b>10000-1 *</b>
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	<b>1000-1 *</b>
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

#### **Trigger Output (TRGO) Parameters:**

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

#### **PWM Generation Channel 3:**

Mode	PWM mode 1
Pulse (16 bits value)	<b>999 *</b>
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

#### **PWM Generation Channel 4:**

Mode	PWM mode 1
Pulse (16 bits value)	<b>999 *</b>
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

## 7.11. TIM5

**mode: Clock Source**

**Channel1: Input Capture direct mode**

**Channel2: Input Capture direct mode**

### 7.11.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value)	<b>100-1 *</b>
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value )	0xffffffff
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

#### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

#### Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

#### Input Capture Channel 2:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

## 7.12. USART1

### Mode: Asynchronous

#### 7.12.1. Parameter Settings:

##### Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

##### Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

## 7.13. FREERTOS

### Interface: CMSIS\_V2

#### 7.13.1. Config parameters:

##### API:

FreeRTOS API	CMSIS v2
<b>Versions:</b>	
FreeRTOS version	10.3.1
CMSIS-RTOS version	2.00
<b>MPU/FPU:</b>	
ENABLE_MPU	Disabled
ENABLE_FPU	Disabled
<b>Kernel settings:</b>	
USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	56
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	<b>255 *</b>
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	<b>Disabled *</b>
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Enabled
USE_COUNTING_SEMAPHORES	Enabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	<b>Enabled *</b>
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Disabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	<b>Enabled *</b>
<b>Memory management settings:</b>	
Memory Allocation	Dynamic / Static
TOTAL_HEAP_SIZE	<b>21448 *</b>
Memory Management scheme	<b>heap_1 *</b>
<b>Hook function related definitions:</b>	
USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	<b>Enabled *</b>
USE_MALLOC_FAILED_HOOK	<b>Enabled *</b>
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	<b>Option2 *</b>
<b>Run time and task stats gathering related definitions:</b>	
GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Enabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

#### Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

#### Software timer definitions:

USE_TIMERS	Enabled
TIMER_TASK_PRIORITY	<b>55 *</b>
TIMER_QUEUE_LENGTH	<b>255 *</b>
TIMER_TASK_STACK_DEPTH	<b>2048 *</b>

#### Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	<b>10 *</b>

#### Added with 10.2.1 support:

MESSAGE_BUFFER_LENGTH_TYPE	size_t
USE_POSIX_ERRNO	<b>Enabled *</b>

#### CMSIS-RTOS V2 flags:

USE_OS2_THREAD_SUSPEND_RESUME	Enabled
USE_OS2_THREAD_ENUMERATE	Enabled
USE_OS2_EVENTFLAGS_FROM_ISR	Enabled
USE_OS2_THREAD_FLAGS	Enabled
USE_OS2_TIMER	Enabled
USE_OS2_MUTEX	Enabled

### 7.13.2. Include parameters:

#### Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	<b>Enabled *</b>
vTaskSuspend	Enabled
vTaskDelayUntil	Enabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Enabled
xSemaphoreGetMutexHolder	<b>Enabled *</b>
pcTaskGetTaskName	<b>Enabled *</b>
uxTaskGetStackHighWaterMark	Enabled
xTaskGetCurrentTaskHandle	Enabled
eTaskGetState	Enabled

xEventGroupSetBitFromISR	<b>Enabled *</b>
xTimerPendFunctionCall	Enabled
xTaskAbortDelay	<b>Enabled *</b>
xTaskGetHandle	<b>Enabled *</b>
uxTaskGetStackHighWaterMark2	<b>Enabled *</b>

### 7.13.3. Advanced settings:

#### **Newlib settings (see parameter description first):**

USE_NEWLIB_REENTRANT	<b>Enabled *</b>
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#### **Project settings (see parameter description first):**

Use FW pack heap file	Enabled
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**\* User modified value**

## 8. System Configuration

### 8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_IN10	Analog mode	No pull-up and no pull-down	n/a	TS
	PC1	ADC1_IN11	Analog mode	No pull-up and no pull-down	n/a	RTS_F
	PC2	ADC1_IN12	Analog mode	No pull-up and no pull-down	n/a	AQS
	PC3	ADC1_IN13	Analog mode	No pull-up and no pull-down	n/a	LS
	PA2	ADC1_IN2	Analog mode	No pull-up and no pull-down	n/a	VS
	PA3	ADC1_IN3	Analog mode	No pull-up and no pull-down	n/a	RTS_R
	PA4	ADC1_IN4	Analog mode	No pull-up and no pull-down	n/a	LB_L
	PA5	ADC1_IN5	Analog mode	No pull-up and no pull-down	n/a	LB_R
	PA6	ADC1_IN6	Analog mode	No pull-up and no pull-down	n/a	RPL_L
	PA7	ADC1_IN7	Analog mode	No pull-up and no pull-down	n/a	RPL_R
	PC4	ADC1_IN14	Analog mode	No pull-up and no pull-down	n/a	LTS_R
	PC5	ADC1_IN15	Analog mode	No pull-up and no pull-down	n/a	LTS_F
	PB0	ADC1_IN8	Analog mode	No pull-up and no pull-down	n/a	BL_R
	PB1	ADC1_IN9	Analog mode	No pull-up and no pull-down	n/a	BL_L
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Very High *	
	PB7	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Very High *	
I2C3	PA8	I2C3_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Very High *	
	PB4	I2C3_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Very High *	
RCC	PH0 - OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1 - OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM2	PB10	TIM2_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	IL_PWM
	PA15	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	LB_PWM
	PB3	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	RPL_PWM
TIM3	PC6	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	DL_PWM
	PC7	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	BL_PWM
	PC8	TIM3_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	FFL_PWM

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC9	TIM3_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	RFL_PWM
TIM4	PB8	TIM4_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	LTS_PWM
	PB9	TIM4_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	RTS_PWM
TIM5	PA0-WKUP	TIM5_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	PDCF_IC
	PA1	TIM5_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	PDCR_IC
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
GPIO	PC13- ANTI_TAMP	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PDCF_BUZZER
	PB2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CENLOC_BUZZER
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SECALM_BUZZER
	PB13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PDCR_TRIG
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	AL
	PB15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	RL
	PA11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PDCF_TRIG
	PA12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	HB
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PDCR_BUZZER



## 8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA2_Stream0	Peripheral To Memory	<b>Very High *</b>
I2C3_RX	DMA1_Stream2	Peripheral To Memory	<b>Very High *</b>
I2C3_TX	DMA1_Stream4	Memory To Peripheral	<b>Very High *</b>

### ADC1: DMA2\_Stream0 DMA request Settings:

Mode: **Circular \***  
 Use fifo: **Enable \***  
 FIFO Threshold: Full  
 Peripheral Increment: Disable  
 Memory Increment: **Enable \***  
 Peripheral Data Width: **Word \***  
 Memory Data Width: **Word \***  
 Peripheral Burst Size: Single  
 Memory Burst Size: Single

### I2C3\_RX: DMA1\_Stream2 DMA request Settings:

Mode: Normal  
 Use fifo: Disable  
 Peripheral Increment: Disable  
 Memory Increment: **Enable \***  
 Peripheral Data Width: **Word \***  
 Memory Data Width: **Word \***

### I2C3\_TX: DMA1\_Stream4 DMA request Settings:

Mode: **Circular \***  
 Use fifo: Disable  
 Peripheral Increment: Disable  
 Memory Increment: **Enable \***  
 Peripheral Data Width: **Word \***  
 Memory Data Width: **Word \***



### 8.3. NVIC configuration

#### 8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	15	0
Pre-fetch fault, memory access fault	true	15	0
Undefined instruction or illegal state	true	15	0
System service call via SWI instruction	true	15	0
Debug monitor	true	15	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
PVD interrupt through EXTI line 16	true	15	0
Flash global interrupt	true	15	0
RCC global interrupt	true	15	0
DMA1 stream2 global interrupt	true	10	0
DMA1 stream4 global interrupt	true	10	0
ADC1 global interrupt	true	15	0
TIM1 update interrupt and TIM10 global interrupt	true	15	0
TIM2 global interrupt	true	15	0
TIM3 global interrupt	true	15	0
TIM4 global interrupt	true	15	0
I2C1 event interrupt	true	10	0
I2C1 error interrupt	true	10	0
USART1 global interrupt	true	15	0
TIM5 global interrupt	true	10	0
DMA2 stream0 global interrupt	true	10	0
I2C3 event interrupt	true	15	0
I2C3 error interrupt	true	15	0
FPU global interrupt	true	15	0

#### 8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	false	true
PVD interrupt through EXTI line 16	true	true	true
Flash global interrupt	true	true	true
RCC global interrupt	true	true	false
DMA1 stream2 global interrupt	true	true	true
DMA1 stream4 global interrupt	true	true	true
ADC1 global interrupt	true	true	true
TIM1 update interrupt and TIM10 global interrupt	false	true	true
TIM2 global interrupt	true	true	true
TIM3 global interrupt	true	true	true
TIM4 global interrupt	true	true	true
I2C1 event interrupt	true	true	true
I2C1 error interrupt	true	true	true
USART1 global interrupt	true	true	true
TIM5 global interrupt	true	true	true
DMA2 stream0 global interrupt	true	true	true
I2C3 event interrupt	true	true	true
I2C3 error interrupt	true	true	true
FPU global interrupt	true	true	false

\* User modified value

## 9. System Views

### 9.1. Category view

#### 9.1.1. Current

## 10. Software Pack Report

### 10.1. Software Pack selected

Vendor	Name	Version	Component
SEGGER	I-CUBE-embOS	1.3.1	Class : RTOS Group : embOS kernel configuration Variant : Debug and Trace Version : 1.1.0 Class : RTOS Group : embOS API configuration Variant : CMSIS- RTOS2 Version : 1.1.0 Class : RTOS Group : embOS sample applications Variant : OS_Start2Tasks_ CMSIS2.c Version : 1.1.0

## 11. Docs & Resources

Type	Link
BSDL files	<a href="https://www.st.com/resource/en/bsdl_model/stm32f411_bsd1.zip">https://www.st.com/resource/en/bsdl_model/stm32f411_bsd1.zip</a>
IBIS models	<a href="https://www.st.com/resource/en/ibis_model/stm32f411_ibis.zip">https://www.st.com/resource/en/ibis_model/stm32f411_ibis.zip</a>
System View Description	<a href="https://www.st.com/resource/en/svd/stm32f4_svd.zip">https://www.st.com/resource/en/svd/stm32f4_svd.zip</a>
BSDL files	<a href="https://www.st.com/resource/en/bsdl_model/stm32f411_bsd1.zip">https://www.st.com/resource/en/bsdl_model/stm32f411_bsd1.zip</a>
IBIS models	<a href="https://www.st.com/resource/en/ibis_model/stm32f411_ibis.zip">https://www.st.com/resource/en/ibis_model/stm32f411_ibis.zip</a>
System View Description	<a href="https://www.st.com/resource/en/svd/stm32f4_svd.zip">https://www.st.com/resource/en/svd/stm32f4_svd.zip</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf">https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf">https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf">https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf">https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf</a>
Training Material	<a href="https://www.st.com/resource/en/sales_guide/sg_sc2154.pdf">https://www.st.com/resource/en/sales_guide/sg_sc2154.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flstm32f4x1.pdf">https://www.st.com/resource/en/flyer/flstm32f4x1.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flstm32nucleo.pdf">https://www.st.com/resource/en/flyer/flstm32nucleo.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flstmcsuite.pdf">https://www.st.com/resource/en/flyer/flstmcsuite.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flstm32trust.pdf">https://www.st.com/resource/en/flyer/flstm32trust.pdf</a>
Product Certifications	<a href="https://www.st.com/resource/en/certification_document/stm32_authentication_can.pdf">https://www.st.com/resource/en/certification_document/stm32_authentication_can.pdf</a>
Application Notes	<a href="https://www.st.com/resource/en/application_note/an1181-electrostatic-discharge-sensitivity-measurement-stmicroelectronics.pdf">https://www.st.com/resource/en/application_note/an1181-electrostatic-discharge-sensitivity-measurement-stmicroelectronics.pdf</a>
Application Notes	<a href="https://www.st.com/resource/en/application_note/an1709-emc-design-guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf">https://www.st.com/resource/en/application_note/an1709-emc-design-guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf</a>
Application Notes	<a href="https://www.st.com/resource/en/application_note/an2606-stm32-">https://www.st.com/resource/en/application_note/an2606-stm32-</a>

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