Product Specifications

Customer	**Standard**
Description	**2.9” E-PAPER DISPLAY**
Model Name	**2.9inch e-Paper (B)**
Date	**2020/02/10**
Revision	**3.1**

Table of Contents

Version	Content	Date	Producer
3.1	New release	2020/1/16	

1. General Description

1.1 Overview

This display is an Active Matrix Electrophoretic Display (AMEPD), with interface and a reference system design. The 2.9" active area contains 128×296 pixels, and has 1-bit B/W/R full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC. SRAM.LUT, VCOM and border are supplied with each panel.

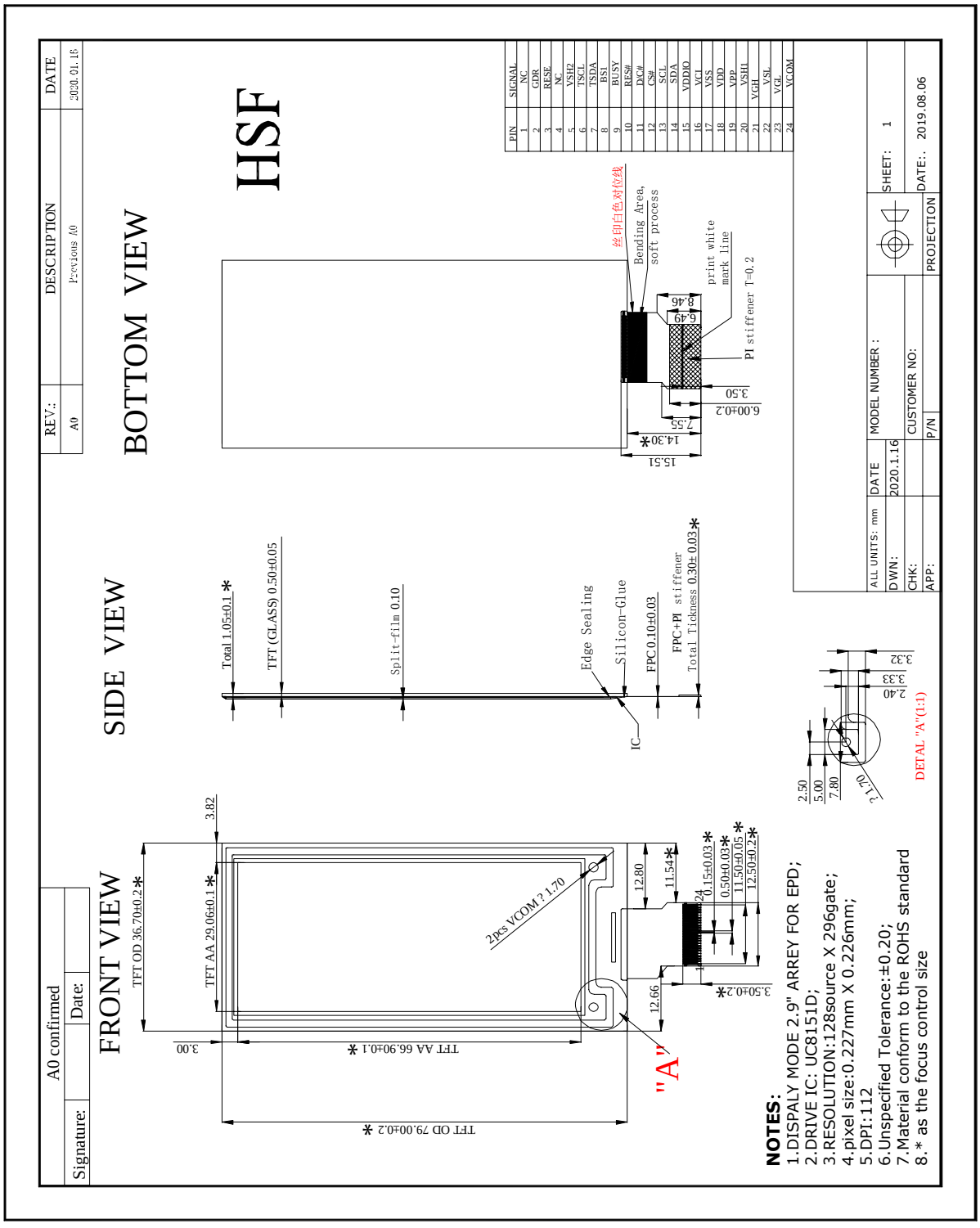
1.2 Features

- 128×296 pixels display
- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Commercial temperature range
- Landscape, portrait modes
- Hard-coat antiglare display surface
- Ultra Low current deep sleep mode
- On chip display RAM
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I2C signal master interface to read external temperature sensor/built-in temperature sensor

1.3 Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	2.9	Inch	
Display Resolution	128(H)×296(V)	Pixel	Dpi:112
Active Area	29.06(H)×66.90(V)	mm	
Pixel Pitch	0.227×0.226	mm	
Pixel Configuration	Rectangle		
Outline Dimension	36.7(H)×79.0(V) ×1.15(D)	mm	
Weight	3.0±0.2	g	

1.4 Mechanical Drawing of EPD module



1.5 Input/Output Terminals

Pin #	Single	Description	Remark
	B P	BONDING PIN	
1	NC	No connection and do not connect with other NC pins	Keep Open
2	GDR	N-Channel MOSFET Gate Drive Control	
3	RESE	Current Sense Input for the Control Loop	
4	NC	No connection and do not connect with other NC pins	Keep Open
5	VDHR	Positive Source driving voltage	
6	TSCL	I2C Interface to digital temperature sensor Clock pin	
7	TSDA	I2C Interface to digital temperature sensor Date pin	
8	BS	Bus selection pin	Note 1.5-5
9	BUSY_N	Busy state output pin	Note 1.5-4
10	RST_N	Reset	Note 1.5-3
11	DC	Data /Command control pin	Note 1.5-2
12	CSB	Chip Select input pin	Note 1.5-1
13	SCL	serial clock pin (SPI)	
14	SDA	serial data pin (SPI)	
15	VDDIO	Power for interface logic pins	
16	VCI	Power Supply pin for the chip	
17	GND	Ground	
18	VDD	Core logic power pin	
19	VPP	Power Supply for OTP Programming	
20	VDH(VSH)	Positive source driver Voltage	
21	VGH	Positive Gate driving voltage	
22	VDL(VSL)	Negative Source driving voltage	
23	VGL	Negative Gate voltage.	
24	VCOM	VCOM driving voltage	
	B P	BONDING PIN	

Note 1.5-1: This pin (CSB) is the chip select input connecting to the MCU. The chip is enabled for MCU communication: only when CSB is pulled LOW.

Note 1.5-2: This pin (DC) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled LOW, the data will be interpreted as command.

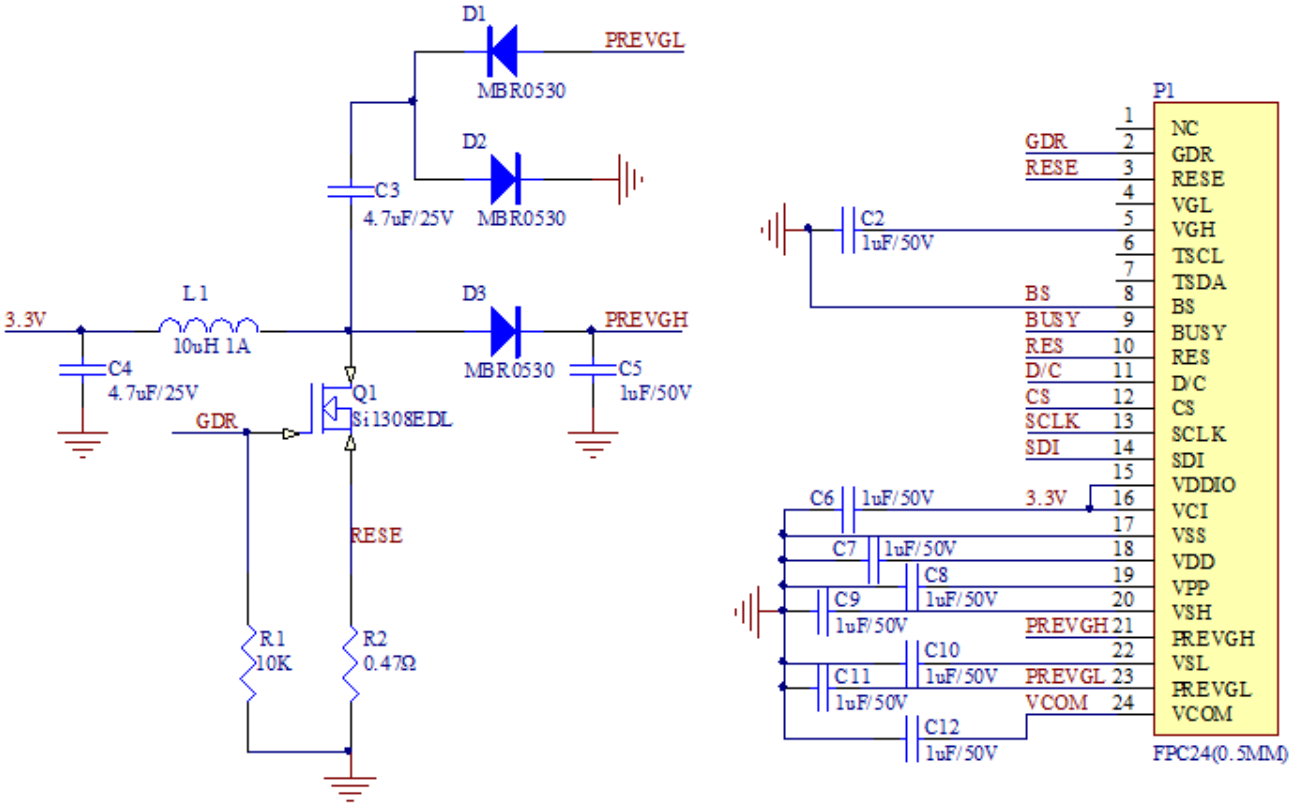
Note 1.5-3: This pin (RST_N) is reset signal input. The Reset is active low.

Note 1.5-4: This pin (BUSY_N) is Busy state output pin. When Busy_N is low operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put Busy_N pin low en the driver IC is working such as:

- Outputting display waveform; or
- Communicating with digital temperature sensor

Note 1.5-5: This pin (BS) is for 3-line SPI or 4-line SPI selection. When it is “Low”, 4-line SPI is selected. When it is “High”, 3-line SPI (9 bits SPI) is selected.

1.6 Reference Circuit



2. Environmental

2.1 HANDLING, SAFETY AND ENVIROMENTAL REQUIREMENTS

WARNING
The display module should be kept flat or fixed to a rigid, curved support with limited bending along the long axis. It should not be used for continual flexing and bending. Handle with care. Should the display break do not touch any material that leaks out. In case of contact with the leaked material then wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.
Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Mounting Precautions
(1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.
(2) It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.
(3) You should adopt radiation structure to satisfy the temperature specification.
(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.

Data sheet status	
Product specification	The data sheet contains final product specifications.

Limiting values
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.
Application information
Where application information is given, it is advisory and dose not form part of the specification.

Product Environmental certification
ROHS
REMARK
All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.

2.2 Reliability test

	TEST	CONDITION	METHOD	REMARK
1	High-Temperature Operation	T=40℃，RH=35%RH，For 240Hr	IEC 60 068-2-2Bb	
2	Low-Temperature Operation	T = 0℃ for 240 hrs	IEC 60 068-2-2Ab	
3	High-Temperature Storage	T=60℃ RH=35%RH For 240Hr Test in white pattern	IEC 60 068-2-2Bb	
4	Low-Temperature Storage	T = -25℃ for 240 hrs Test in white pattern	IEC 60 068-2-2Ab	
5	High Temperature, High-Humidity Operation	T=40℃，RH=80%RH，For 168Hr	IEC 60 068-2-3CA	
6	High Temperature, High-Humidity Storage	T=50℃，RH=80%RH，For 240Hr Test in white pattern	IEC 60 068-2-3CA	
7	Temperature Cycle	-25℃(30min) ~60℃(30min) 50 Cycle Test in white pattern	IEC 60 068-2-14NB	
8	Package Vibration	1.04G,Frequency : 10~500Hz Direction : X,Y,Z Duration:1hours in each direction	Full packed for shipment	
9	Package Drop Impact	Drop from height of 122 cm on Concrete surface Drop sequence:1 corner, 3edges, 6face One drop for each.	Full packed for shipment	
10	UV exposure Resistance	765 W/㎡ for 168hrs,40℃	IEC 60068-2-5 Sa	
11	Electrostatic discharge	Machine model: +/-250V,0Ω,200pF	IEC61000-4-2	

Actual EMC level to be measured on customer application.

Note1: The protective film must be removed before temperature test.

Note2：Stay white pattern for storage and non-operation test.

Note3：Operation is black/white/red pattern , hold time is 150S.

Note4：The function,appearence,opticals should meet the requirements of the test before and after the test. Note5：Keep testing after 2 hours placing at 20℃-25℃.

3. Electrical Characteristics

3.1 ABSOLUTE MAXIMUM RATING

Table 3.11: Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CI}	Logic supply voltage	-0.3 to +6.0	V
T_{OPR}	Operation temperature range	0 to 40	°C
T_{STG}	Storage temperature range	-25 to 60	°C
-	Humidity range	40~70	%RH

3.2 DC CHARACTERISTICS

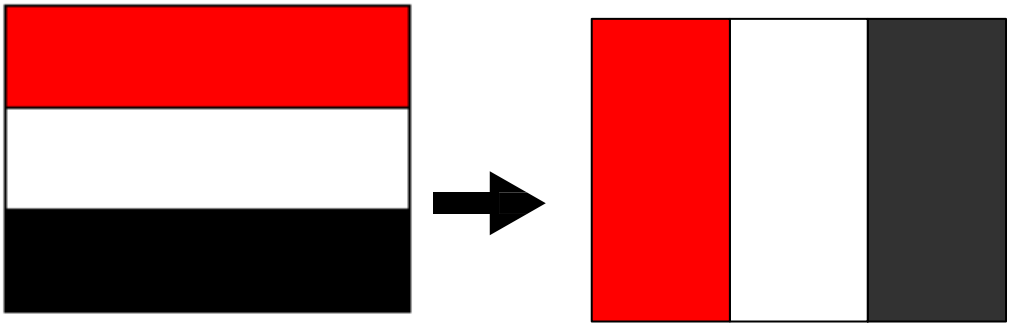
The following specifications apply for: VSS=0V, VCI=3.3V, TOPR=25℃.

Table 3.2-1: DC Characteristics

DIGITAL DC CHARACTERISTICS						
Symbol	**Parameter**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
VCI	VCI operation voltage	-	2.3	3.3	3.6	V
VIH	High level input voltage	Digital input pins	0.7xV DDIO	-	V DDIO	V
VIL	Low level input voltage	Digital input pins	0	-	0.3xVDD	V
VOH	High level output voltage	Digital input pins, IOH=400 uA	VDDIO-0.4	-		V
VOL	Low level output voltage	Digital input pins, IOL=-400 uA	0	-	0.4	V
Iupdate	Module operating current	-	-	10	-	mA
Isleep	Deep sleep mode	VCI=3.3V	-		2	uA

- The Typical power consumption is measured using associated 25℃ waveform with following pattern transition: from horizontal scan pattern to vertical scan pattern. (Note 3.2-1)
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Waveshare.
- Vcom value will be OTP before in factory or present on the label sticker.

Note 3.2-1
The Typical power consumption



3.3 Serial Peripheral Interface Timing

The following specifications apply for: VSS=0V, VCI=2.3V to 3.6V, T_{OPR}=25℃

Write mode

Symbol	Parameter	Min	Typ	Max	Unit
fSCL	SCL frequency (Write Mode)			20	MHz
tCSSU	Time CSB has to be low before the first rising edge of SCLK	20			ns
tCSHLD	Time CSB has to remain low after the last falling edge of SCLK	20			ns
tCSHIGH	Time CSB has to remain high between two transfers	100			ns
tSCLHIGH	Part of the clock period where SCL has to remain high	25			ns
tSCLLOW	Part of the clock period where SCL has to remain low	25			ns
tSISU	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	10			ns
tSIHLD	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	40			ns

Read mode

Symbol	Parameter	Min	Typ	Max	Unit
fSCL	SCL frequency (Read Mode)			2.5	MHz
tCSSU	Time CSB has to be low before the first rising edge of SCLK	100			ns
tCSHLD	Time CSB has to remain low after the last falling edge of SCLK	50			ns
tCSHIGH	Time CSB has to remain high between two transfers	250			ns
tSCLHIGH	Part of the clock period where SCL has to remain high	180			ns
tSCLLOW	Part of the clock period where SCL has to remain low	180			ns
tSOSU	Time SO(SDA Read Mode) will be stable before the next rising edge of SCL		50		ns
tSOHLD	Time SO (SDA Read Mode) will remain stable after the falling edge of SCL		0		ns

Note: All timings are based on 20% to 80% of VDDIO-VSS

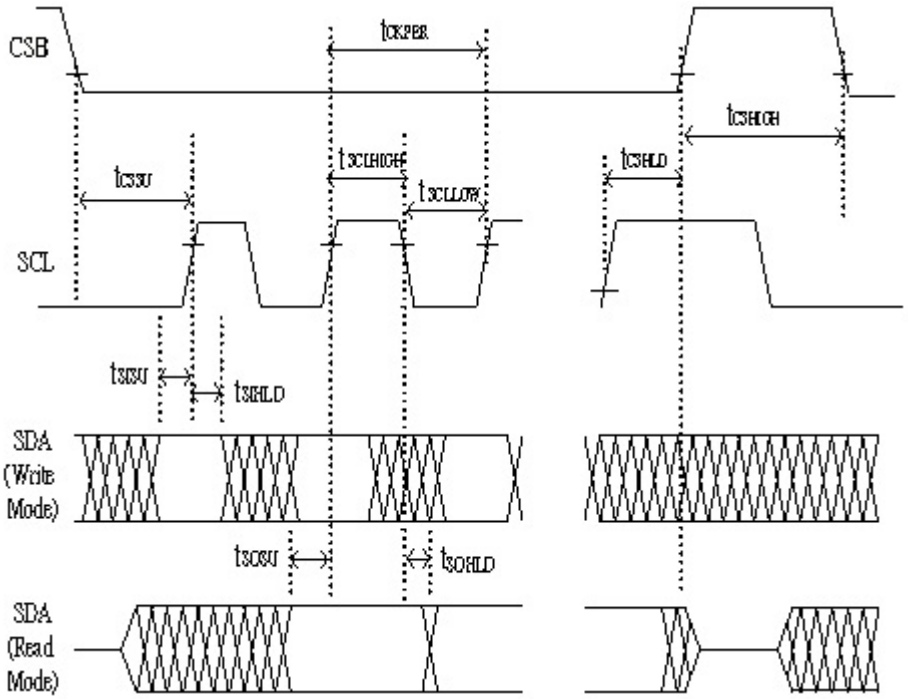
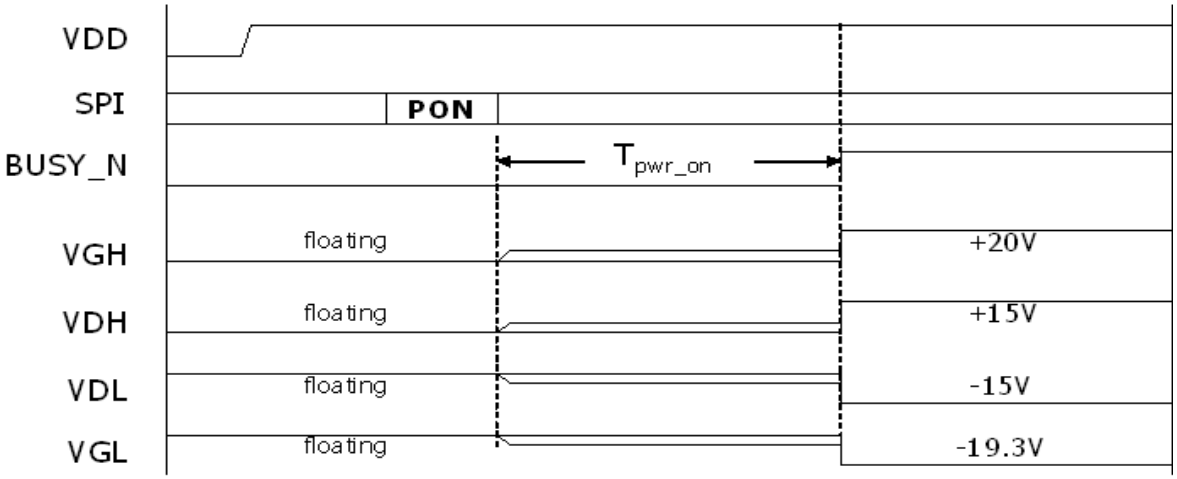


Figure 3.3-1: Serial peripheral interface characteristics

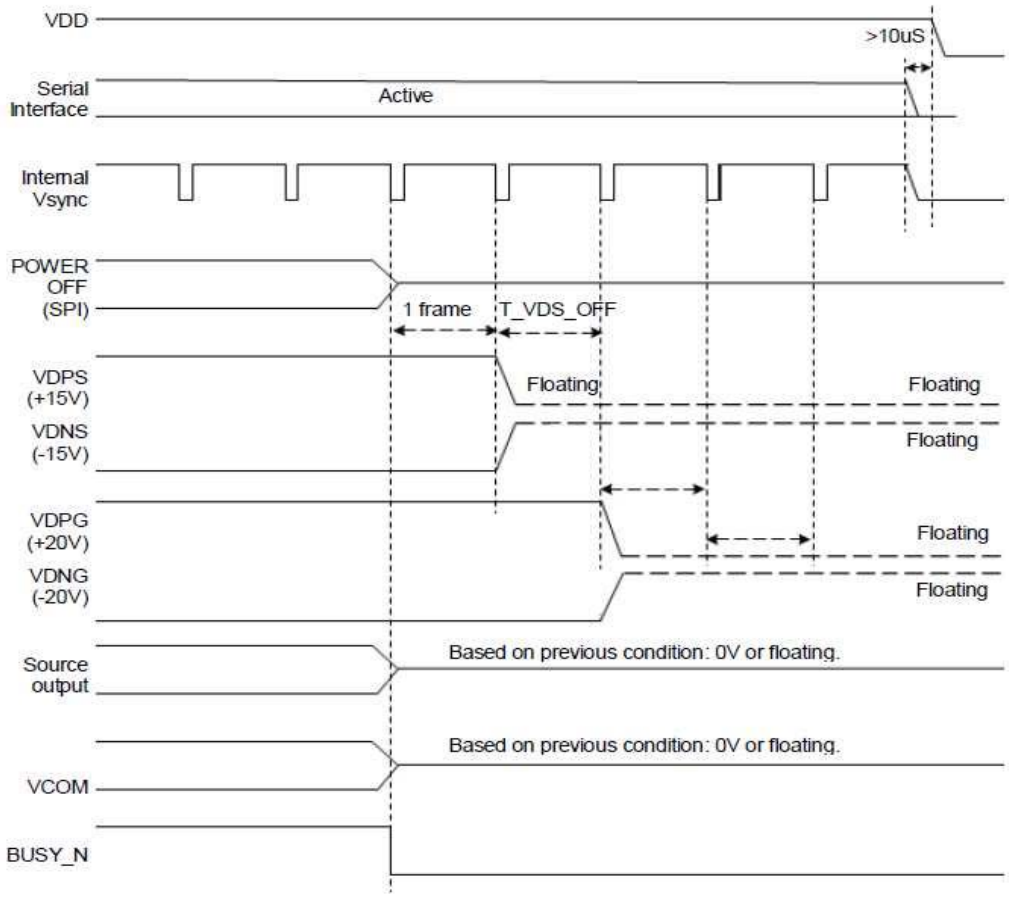
3. 3 Power ON /OFF Sequence

Power ON Sequence



T_{pwr_on} = ~80ms (default)

Power OFF Sequence



3.4 Power Consumption

Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Panel power consumption during update	-	25℃	-	70	mAs	-
Deep sleep mode	-	25℃	-	2	uA	-

MAs=update average current×update time

3.5 MCU Interface

3.5.1 MCU interface selection

The Display can support 3-wire/4-wire serial peripheral interface. In the Module, the MCU interface is pin selectable by BS pins shown in.

Table 3.5.1-1: MCU interface selection

BS	MPU Interface
L	4-lines serial peripheral interface (SPI)
H	3-lines serial peripheral interface (SPI) - 9 bits SPI

3.5.2 MCU Serial Peripheral Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCL, serial data SDA, DC and CSB,The control pins status in 4-wire SPI in writing command/data is shown in Table 3.5 and the write procedure 4-wire SPI is shown in Figue 3.5.2-2.

Table 3.5.2-2 : Control pins status of 4-wire SPI

Function	SCL pin	SDA pin	DC pin	CSB pin
Write command	↑	Command bit	L	L
Write data	↑	Data bit	H	L

Note:

(1) L is connected to GND and H is connected to VDDIO

(2) ↑ stands for rising edge of signal

In the write mode, SDA is shifted into an 8-bit shift register on each rising edge of SCL in the order of D7, D6, ... D0. The level of DC should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or command Byte register according to DC pin.

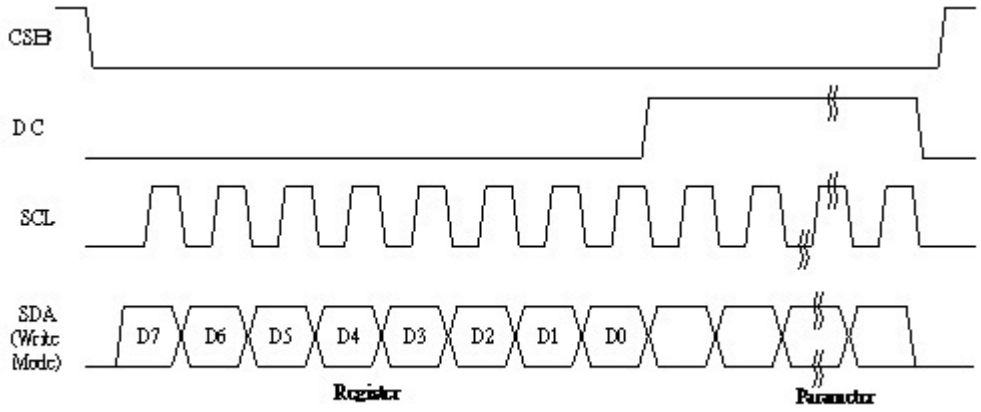


Figure 3.5.2-2: Write procedure in 4-wire SPI mode

In the Read mode:

1. After driving CSB to low, MCU need to define the register to be read.
2. SDA is shifted into an 8-bit shift register on each rising edge of SCL in the order of D7, D6, ... D0 with DC# keep low.
3. After SCL change to low for the last bit of register, DC need to drive to high.
4. SDA is shifted out an 8-bit data on each falling edge of SCL in the order of D7, D6, … D0.
5. Depending on register type, more than 1 byte can be read out. After all byte are read, CSB need to drive to high to stop the read operation.

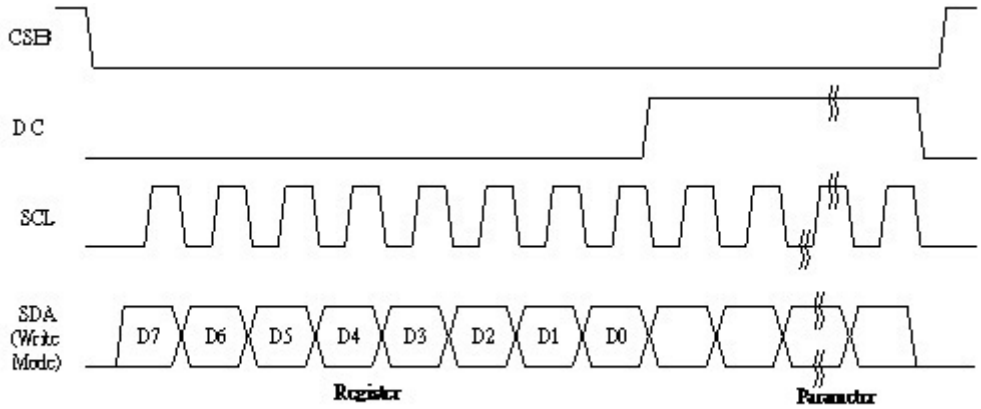


Figure 3.5.2-2: Read procedure in 4-wire SPI mode

3.5.3 MCU Serial Peripheral Interface (3-wire SPI)

The 3-wire SPI consists of serial clock SCL, serial data SDA and CSB. The operation is similar to 4-wire SPI while DC pin is not used and it must be tied to LOW. The control pins status in 3-wire SPI is shown in Table 3.5.3-3.

Table 3.5.3-3 : Control pins status of 3-wire SPI

Function	SCL pin	SDA pin	DC pin	CSB pin
Write command	↑	Command bit	Tie LOW	L
Write data	↑	Data bit	Tie LOW	L

Note:

(1)L is connected to GND and H is connected to VDDIO

(2)↑ stands for rising edge of signal

In the write operation, a 9-bit data will be shifted into the shift register on each clock rising edge. The bit shifting sequence is DC bit, D7 bit, D6 bit to D0 bit. The first bit is DC bit which determines the following byte is command or data. When DC bit is 0, the following byte is command. When DC bit is 1, the following byte is data. shows the write procedure in 3-wire SPI

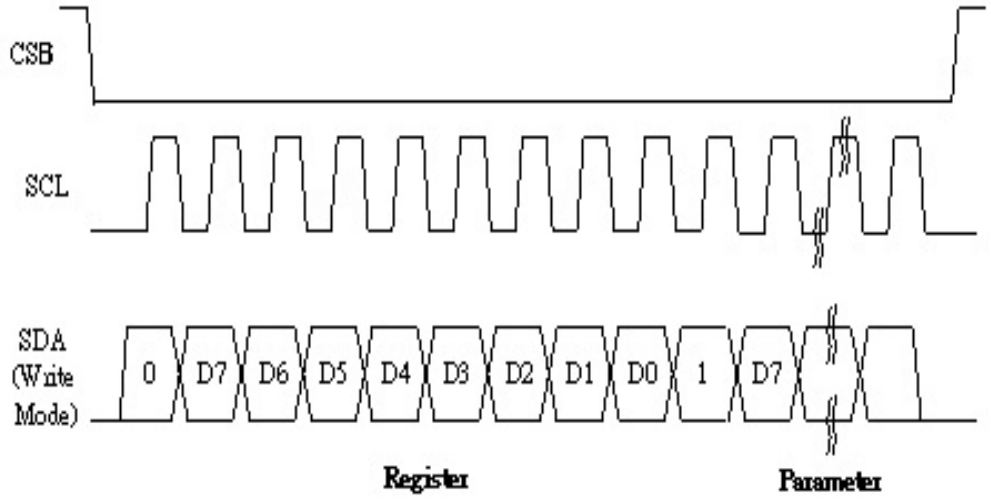


Figure 3.5.3-3: Write procedure in 3-wire SPI mode

In the Read mode:

1. After driving CSB to low, MCU need to define the register to be read.
2. DC=0 is shifted thru SDA with one rising edge of SCL
3. SDA is shifted into an 8-bit shift register on each rising edge of SCL in the order of D7, D6, ... D0.
4. DC=1 is shifted thru SDA with one rising edge of SCL
5. SDA is shifted out an 8-bit data on each falling edge of SCL in the order of D7, D6, … D0.
6. Depending on register type, more than 1 byte can be read out. After all byte are read, CSB need to drive to high to stop the read operation.

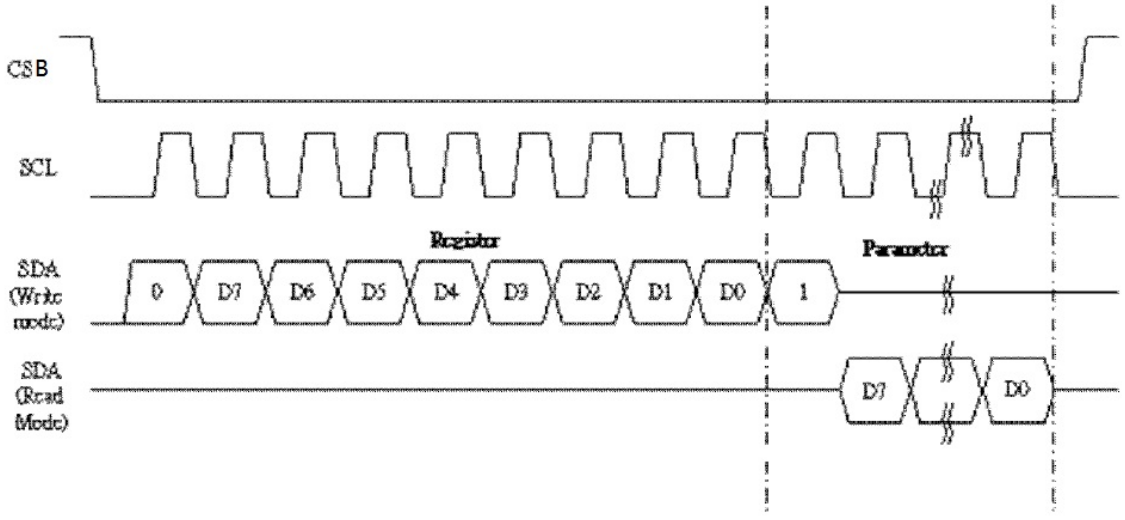


Figure 3.5.3-3: Read procedure in 3-wire SPI mode

4. Typical Operating Sequence

4.1 Normal Operation Flow

Sequence	Action by	Command	Action Description	Remark
1	User	-	Power on(VCI supply)	-
2	User	-	HW reset	-
	IC	-	After HW reset ,the driver IC will have registers load with POR value. Ready for command input. Vcom register loaded with OTP value.	-
3	-	-	Send initial code to driver including setting of.	-
	User	C00	Panel configuration:Resolution setting,LUT selection,BW/BWR mode.	-
	User	C50	Setting Vcom and Data interval.	-
4	-	-	Data operations.	-
	User	C61	Display resolution start and end active gate/source.	-
	User	C10 and C13	Write display data to RAM.	-
5	User	C04	Output gate/source voltage.	-
	User	C12	Boosters and regulators turn on. Load temperture register with sensor reading. Load LUT(register or OTP)	-
	User	C02	Turn off gate/source voltage.	-
6	User	-	Power off.	-

5. COMMAND TABLE

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
1	Panel Setting (PSR)	0	0	0	0	0	0	0	0	0	0		00H
		0	1	#	#	#	#	#	#	#	#	RES[1:0],REG,KW/R,UD,SHL, SHD_N,RST_N	0FH
2	Power Setting (PWR)	0	0	0	0	0	0	0	0	0	1		01H
		0	1	-	-	-	-	-	-	#	#	VDS_EN, VDG_EN	03H
		0	1	-	-	-	-	-	#	#	#	VCOM_HV,VGHL_LV[1:0]	00H
		0	1	-	-	#	#	#	#	#	#	VDH[5:0]	26H
		0	1	-	-	#	#	#	#	#	#	VDL[5:0]	26H
		0	1	-	-	#	#	#	#	#	#	VDHR[5:0]	03H
3	Power OFF (POF)	0	0	0	0	0	0	0	0	1	0		02H
4	Power OFF Sequence Setting (PFS)	0	0	0	0	0	0	0	0	1	1		03H
		0	1	-	-	#	#	-	-	-	-	T_VDS_OF[1:0]	00H
5	Power ON (PON)	0	0	0	0	0	0	0	1	0	0		04H
6	Power ON Measure (PMES)	0	0	0	0	0	0	0	1	0	1		05H
7	Booster Soft Start (BTST)	0	0	0	0	0	0	0	1	1	0		06H
		0	1	#	#	#	#	#	#	#	#	BT_PHA[7:0]	17H
		0	1	#	#	#	#	#	#	#	#	BT_PHB[7:0]	17H
		0	1	-	-	#	#	#	#	#	#	BT_PHC[5:0]	17H
8	Deep sleep (DSLP)	0	0	0	0	0	0	0	1	1	1		07H
		0	1	1	0	1	0	0	1	0	1	Check code	A5H
9	Display Start Transmission 1 (DTM1, White/Black Data) (x-byte command)	0	0	0	0	0	1	0	0	0	0	B/W or OLD Pixel Data (160x296):	10H
		0	1	#	#	#	#	#	#	#	#	KPXL[1:8]	00H
		0	1	:	:	:	:	:	:	:	:	:	:
		0	1	#	#	#	#	#	#	#	#	KPXL[n-1:n]	00H
10	Data Stop (DSP)	0	0	0	0	0	1	0	0	0	1		11H
		1	1	#	-	-	-	-	-	-	-		00H
11	Display Refresh (DRF)	0	0	0	0	0	1	0	0	1	0		12H
12	Display Start transmission 2 (DTM2, Red Data) (x-byte command)	0	0	0	0	0	1	0	0	1	1	Red or NEW Pixel Data (160X296):	13H
		0	1	#	#	#	#	#	#	#	#	RPXL[1:8]	00H
		0	1	:	:	:	:	:	:	:	:	:	:
		0	1	#	#	#	#	#	#	#	#	RPXL[n-1:n]	00H
13	Auto Sequence (AUTO)	0	0	0	0	0	1	0	1	1	1		17H
		1	1	1	0	1	0	0	1	0	1	Check code	A5H
14	VCOM LUT (LUTC) (61-byte command, structure of bytes 2~7 repeated 10 times)	0	0	0	0	1	0	0	0	0	0		20H
		0	1	#	#	#	#	#	#	#	#	Level select-0~3[1:0]	00H
		0	1	:	:	:	:	:	:	:	:	Number of frames-0[7:0]	00H
		0	1	:	:	:	:	:	:	:	:	Number of frames-1[7:0]	00H
		0	1	:	:	:	:	:	:	:	:	Number of frames-2[7:0]	00H
		0	1	:	:	:	:	:	:	:	:	Number of frames-3[7:0]	00H
		0	1	#	#	#	#	#	#	#	#	Times to repeat[7:0]	00H
15	W2W LUT (LUTBW / LUTR) (37-byte command, structure of bytes 2~7 repeated 10 times)	0	0	0	0	1	0	0	0	0	1		21H
		0	1	#	#	#	#	#	#	#	#	Level select-0~3[1:0]	00H
		0	1	:	:	:	:	:	:	:	:	Number of frames-0[7:0]	00H
		0	1	:	:	:	:	:	:	:	:	Number of frames-1[7:0]	00H

		0	1	:	:	:	:	:	:	:	:	Number of frames-2[7:0]	00H
		0	1	:	:	:	:	:	:	:	:	Number of frames-3[7:0]	00H
		0	1	#	#	#	#	#	#	#	#	Times to repeat[7:0]	00H
16	B2W LUT (LUTBW / LUTR) (61-byte command, structure of bytes 2~7 repeated 10 times)	0	0	0	0	1	0	0	0	1	0		22H
		0	1	#	#	#	#	#	#	#	#	Level select-0~3[1:0]	00H
		0	1	:	:	:	:	:	:	:	:	Number of frames-0[7:0]	00H
		0	1	:	:	:	:	:	:	:	:	Number of frames-1[7:0]	00H
		0	1	:	:	:	:	:	:	:	:	Number of frames-2[7:0]	00H
		0	1	:	:	:	:	:	:	:	:	Number of frames-3[7:0]	00H
		0	1	#	#	#	#	#	#	#	#	Times to repeat[7:0]	00H
17	W2B LUT (LUTWB / LUTW) (37-byte command, structure of bytes 2~7 repeated 6 times)	0	0	0	0	1	0	0	0	1	1		23H
		0	1	#	#	#	#	#	#	#	#	Level select-0~3[1:0]	00H
		0	1	:	:	:	:	:	:	:	:	Number of frames-0[7:0]	00H
		0	1	:	:	:	:	:	:	:	:	Number of frames-1[7:0]	00H
		0	1	:	:	:	:	:	:	:	:	Number of frames-2[7:0]	00H
		0	1	:	:	:	:	:	:	:	:	Number of frames-3[7:0]	00H
		0	1	#	#	#	#	#	#	#	#	Times to repeat[7:0]	00H
18	B2B LUT (LUTBB / LUTB) (37-byte command, structure of bytes 2~7 repeated 6 times)	0	0	0	0	1	0	0	1	0	0		24H
		0	1	#	#	#	#	#	#	#	#	Level select-0~3[1:0]	00H
		0	1	:	:	:	:	:	:	:	:	Number of frames-0[7:0]	00H
		0	1	:	:	:	:	:	:	:	:	Number of frames-1[7:0]	00H
		0	1	:	:	:	:	:	:	:	:	Number of frames-2[7:0]	00H
		0	1	:	:	:	:	:	:	:	:	Number of frames-3[7:0]	00H
		0	1	#	#	#	#	#	#	#	#	Times to repeat[7:0]	00H
19	LUT option (LUTOPT)	0	0	0	0	1	0	1	0	1	0		2AH
		0	1	-	-	#	#	#	#	#	#	STATE_XON[5:0]	00H
		0	1	-	-	#	#	-	#	#	#	EXS[1:0], DMS[2:0]	00H
20	PLL control (PLL)	0	0	0	0	1	1	0	0	0	0		30H
		0	1	-	-	#	#	#	#	#	#	M[2:0], N[2:0]	3CH
21	Temperature Sensor Calibration(TSC)	0	0	0	1	0	0	0	0	0	0		40H
		1	1	#	#	#	#	#	#	#	#	D[10:3] / TS[7:0]	00H
		1	1	#	#	#	-	-	-	-	-	D[2:0] / -	00H
22	Temperature Sensor Selection(TSE)	0	0	0	1	0	0	0	0	0	1		41H
		0	1	#	-	-	-	#	#	#	#	TSE, TO[3:0]	00H
23	Temperature Sensor Write (TSW)	0	0	0	1	0	0	0	0	0	0		42H
		0	1	#	#	#	#	#	#	#	#	WATTR[7:0]	00H
		0	1	#	#	#	#	#	#	#	#	WMSB[7:0]	00H
		0	1	#	#	#	#	#	#	#	#	WLSB[7:0]	00H
24	Temperature Sensor Read (TSR)	0	0	0	1	0	0	0	0	1	1		43H
		1	1	#	#	#	#	#	#	#	#	RMSB[7:0]	00H
		1	1	#	#	#	#	#	#	#	#	RLSB[7:0]	00H
25	Panel Break Check (PBC)	0	0	0	1	0	0	0	1	0	0		44H
		1	1	-	-	-	-	-	-	-	#	PSTA	00H
26	VCOM and data interval setting(CDI)	0	0	0	1	0	1	0	0	0	0		50H
		0	1	#	#	#	#	#	#	#	#	VBD[1:0], DDX[1:0], CDI[3:0]	D7H
27	Lower Power Detection (LPD)	0	0	0	1	0	1	0	0	0	1		51H
		1	1	-	-	-	-	-	-	-	#	LPD	01H
28	TCON setting (TCON)	0	0	0	1	1	0	0	0	0	0		60H

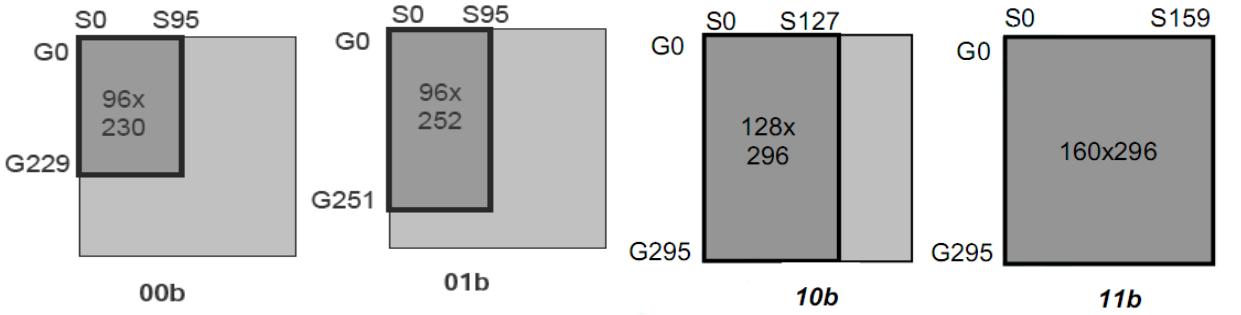
		0	1	#	#	#	#	#	#	#	#	S2G[3:0], G2S[3:0]	22H
29	Resolution setting (TRES)	0	0	0	1	1	0	0	0	0	1		61H
		0	1	#	#	#	#	#	0	0	0	HRES[7:3]	00H
		0	1	-	-	-	-	-	-	-	#	VRES[8:0]	00H
		0	1	#	#	#	#	#	#	#	#		00H
30	Gate/Source Start setting (GSST)	0	0	0	1	1	0	0	1	0	1		65H
		0	1	#	#	#	#	#	0	0	0	HST[7:3]	00H
		0	1	-	-	-	-	-	-	-	#	VST[8:0]	00H
		0	1	#	#	#	#	#	#	#	#		00H
31	Revision (REV)	0	0	0	1	1	1	0	0	0	0		70H
		1	1	#	#	#	#	#	#	#	#	LUT_REV[7:0]	FFH
		1	1	-	-	-	-	#	#	#	#	CHIP_REV[3:0]	0DH
32	Get Status (FLG)	0	0	0	1	1	1	0	0	0	1		71H
		1	1	-	#	#	#	#	#	#	#	PTL_FLAG ,I2C_ERR, I2C_BUSYN, DATA_FLAG, PON, POF, BUSY_N	13H
33	Auto Measurement VCOM (AMV)	0	0	1	0	0	0	0	0	0	0		80H
		0	1	-	-	#	#	#	#	#	#	AMVT[1:0], XON,AMVS, AMV, AMVE	10H
34	Read VCOM Value (VV)	0	0	1	0	0	0	0	0	0	1		81H
		1	1	-	-	#	#	#	#	#	#	VV[5:0]	00H
35	VCOM_DC Setting (VDCS)	0	0	1	0	0	0	0	0	1	0		82H
		0	1	-	-	#	#	#	#	#	#	VDCS[5:0]	00H
36	Partial Window (PTL)	0	0	1	0	0	1	0	0	0	0		90H
		0	1	#	#	#	#	#	0	0	0	HRST[7:3]	00H
		0	1	#	#	#	#	#	1	1	1	HRED[7:3]	07H
		0	1	-	-	-	-	-	-	-	#	VRST[8:0]	00H
		0	1	#	#	#	#	#	#	#	#		00H
		0	1	-	-	-	-	-	-	-	#	VRED[8:0]	00H
		0	1	#	#	#	#	#	#	#	#		00H
		0	1	-	-	-	-	-	-	-	#	PT_SCAN	01H
37	Partial In (PTIN)	0	0	1	0	0	1	0	0	0	1		91H
38	Partial Out (PTOUT)	0	0	1	0	0	1	0	0	1	0		92H
39	Program Mode (PGM)	0	0	1	0	1	0	0	0	0	0		A0H
40	Active Programming (APG)	0	0	1	0	1	0	0	0	0	1		A1H
41	Read OTP (ROTP)	0	0	1	0	1	0	0	0	1	0		A2H
		1	1	-	-	-	-	-	-	-	-	Read Dummy	N/A
		1	1	#	#	#	#	#	#	#	#	Data of Address = 000h	N/A
		1	1	:	:	:	:	:	:	:	:	:	N/A
		1	1	#	#	#	#	#	#	#	#	Data of Address = n	N/A
42	Cascade Setting (CCSET)	0	0	1	1	1	0	0	0	0	0		E0H
		0	1	-	-	#	#	#	#	#	#	TSFIX, CCEN	00H
43	Power Saving (PWS)	0	0	1	1	1	0	0	0	1	1		E3H
		0	1	#	#	#	#	#	#	#	#	VCOM_W[3:0], SD_W[3:0]	00H
44	LVD Voltage Select (LVSEL)	0	0	1	1	1	0	0	1	0	0		E4H
		0	1	-	-	-	-	-	-	#	#	LVD_SEL[1:0]	03H
45	Force Temperature (TSSET)	0	0	1	1	1	0	0	1	0	1		E5H
		0	1	#	#	#	#	#	#	#	#	TS_SET[7:0]	00H

5-1) Register Definition

5-1-1) PANEL SETTING (PSR) (REGISTER : R00 H

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Setting the panel	0	0	0	0	0	0	0	0	0	0	00 H
	0	1	RES1	RES0	REG	KW/R	UD	SHL	SHD_N	RST_N	0F H

RES[1:0]: Display Resolution setting (source x gate)
00b: 96x230 (Default) Active source channels: S0 ~ S95. Active gate channels: G0 ~ G229.
01b: 96x252 Active source channels: S0 ~ S95. Active gate channels: G0 ~ G251.
10b: 128x296 Active source channels: S0 ~ S127. Active gate channels: G0 ~ G295.
11b: 160x296 Active source channels: S0 ~ S159. Active gate channels: G0 ~ G295.



(1) Minimum active GD is always G0 regardless of <UD>(R00H).
(2) Minimum active SD is always S0 regardless of <SHL>(R00H).

maximum resolution
active resolution

REG: LUT selection
0: LUT from OTP. (Default)
1: LUT from register.
KW/R: Black / White / Red
0: Pixel with Black/White/Red, KWR mode. (Default)
1: Pixel with Black/White, KW mode.
UD: Gate Scan Direction
0: Scan down. First line to Last line: Gn-1 → Gn-2 → Gn-3 → …→ G0
1: Scan up. (Default) First line to Last line: G0→G1→G2→ … … . → Gn-1
SHL: Source Shift Direction
0: Shift left. First data to Last data: Sn-1 ? Sn-2 ? Sn-3 ? … ? S0
1: Shift right. (Default) First data to Last data: S0 →S1 → S2 → … … . → Sn-1
SHD_N: Booster Switch
0: Booster OFF
1: Booster ON (Default)
When SHD_N becomes LOW, charge pump will be turned OFF, register and SRAM data will keep until VDD OFF. And Source/Gate/Border/VCOM will be released to floating.
RST_N: Soft Reset
0: Reset. Booster OFF, Register data are set to their default values, all drivers will be reset, and all functions will
Be disabled. Source/Gate/Border/VCOM will be released to floating.
1: No effect (Default).

5-1-2) POWER SETTING (PWR) (R01 H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Selecting Internal/External Power	0	0	0	0	0	0	0	0	0	1	01H
	0	1	-	-	-	-	-	-	VDS_EN	VDG_EN	03 H
	0	1	-	-	-	-	-	VCOM_HV	VGHL_LV[1:0]		00H
	0	1	-	-	VDH[5:0]						26H
	0	1	-	-	VDL[5:0]						26H
	0	1	-	-	VDHR[5:0]						03H

VDS_EN: Source power selection

0 : External source power from VDH/VDL/VDHR pins

1 : Internal DC/DC function for generating VDH/VDL/VDHR. (Default)

VDG_EN: Gate power selection

0 : External gate power from VGH/VGL pins

1 : Internal DC/DC function for generating VGH/VGL. (Default)

VCOM_HV: VCOM Voltage Level

0 : VCOMH=VDH+VCOM_DC, VCOML=VDL+VCOM_DC. (Default)

1 : VCOMH=VGH, VCOML=VGL

VGHL_LV[1:0]: VGH / VGL Voltage Level selection.

VGHL_LV	VGHL Voltage Level
00 (Default)	VGH=20V, VGL= -20V
1	VGH=19V, VGL= -19V
10	VGH=18V, VGL= -18V
11	VGH=17V, VGL= -17V

VDH[5:0]: Internal VDH power selection for B/W pixel.**(Default value: 100110b)**

VDH	Voltage	VDH	Voltage	VDH	Voltage	VDH	Voltage
000000	6.4 V	001100	8.8 V	011000	11.2 V	100100	13.6 V
000001	6.6 V	001101	9.0 V	011001	11.4 V	100101	13.8 V
000010	6.8 V	001110	9.2 V	011010	11.6 V	**100110**	**14.0 V**
000011	7.0 V	001111	9.4 V	011011	11.8 V	100111	14.2 V
000100	7.2 V	010000	9.6 V	011100	12.0 V	101000	14.4 V
000101	7.4 V	010001	9.8 V	011101	12.2 V	101001	14.6 V
000110	7.6 V	010010	10.0 V	011110	12.4 V	101010	14.8 V
000111	7.8 V	010011	10.2 V	011111	12.6 V	101011	15.0 V
001000	8.0 V	010100	10.4 V	100000	12.8 V	(others)	15.0 V
001001	8.2 V	010101	10.6 V	100001	13.0 V		
001010	8.4 V	010110	10.8 V	100010	13.2 V		
001011	8.6 V	010111	11.0 V	100011	13.4 V		

VDL[5:0]: Internal VDL power selection for B/W pixel. **(Default value: 100110b)**

VDH	Voltage	VDH	Voltage	VDH	Voltage	VDH	Voltage
000000	-6.4 V	001100	-8.8 V	011000	-11.2 V	100100	-13.6 V
000001	-6.6 V	001101	-9.0 V	011001	-11.4 V	100101	-13.8 V
000010	-6.8 V	001110	-9.2 V	011010	-11.6 V	**100110**	**-14.0 V**
000011	-7.0 V	001111	-9.4 V	011011	-11.8 V	100111	-14.2 V
000100	-7.2 V	010000	-9.6 V	011100	-12.0 V	101000	-14.4 V
000101	-7.4 V	010001	-9.8 V	011101	-12.2 V	101001	-14.6 V
000110	-7.6 V	010010	-10.0 V	011110	-12.4 V	101010	-14.8 V

000111	-7.8 V	010011	-10.2 V	011111	-12.6 V	101011	-15.0 V
001000	-8.0 V	010100	-10.4 V	100000	-12.8 V	(others)	-15.0 V
001001	-8.2 V	010101	-10.6 V	100001	-13.0 V		
001010	-8.4 V	010110	-10.8 V	100010	-13.2 V		
001011	-8.6 V	010111	-11.0 V	100011	-13.4 V		

VDHR[5:0]: Internal VDHR power selection for Red pixel. **(Default value: 000011b)**

VDH	Voltage	VDH	Voltage	VDH	Voltage	VDH	Voltage
000000	2.4 V	001100	4.8 V	011000	7.2 V	100100	9.6 V
000001	2.6 V	001101	5.0 V	011001	7.4 V	100101	9.8 V
000010	2.8 V	001110	5.2 V	011010	7.6 V	100110	10.0 V
000011	**3.0 V**	001111	5.4 V	011011	7.8 V	100111	10.2 V
000100	3.2 V	010000	5.6 V	011100	8.0 V	101000	10.4 V
000101	3.4 V	010001	5.8 V	011101	8.2 V	101001	10.6 V
000110	3.6 V	010010	6.0 V	011110	8.4 V	101010	10.8 V
000111	3.8 V	010011	6.2 V	011111	8.6 V	101011	11.0 V
001000	4.0 V	010100	6.4 V	100000	8.8 V	(others)	11.0 V
001001	4.2 V	010101	6.6 V	100001	9.0 V		
001010	4.4 V	010110	6.8 V	100010	9.2 V		
001011	4.6 V	010111	7.0 V	100011	9.4 V		

5-1-3) POWER OFF (POF) (R02 H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Turning OFF the power	0	0	0	0	0	0	0	0	1	0	02 H

After the Power OFF command, the driver will be powered OFF. Refer to the POWER MANAGEMENT section for the sequence. This command will turn off booster, controller, source driver, gate driver, VCOM, and temperature sensor, but register data will be kept until VDD turned OFF or Deep Sleep Mode. Source/Gate/Border/VCOM will be released to floating.

5-1-4) POWER OFF SEQUENCE SETTING (PFS) (R03 H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Setting Power OFF sequence	0	0	0	0	0	0	0	0	1	1	03 H
	0	1	-	-	T_VDS_OFF[1:0]		-	-	-	-	00 H

T_VDS_OFF[1:0]: Source to gate power off interval time.
00b: 1 frame (Default) 01b: 2 frames 10b: 3 frames 11b: 4 frame

5-1-5) POWER ON (PON) (REGISTER : R04 H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Turning ON the power	0	0	0	0	0	0	0	1	0	0	04H

After the Power ON command, the driver will be powered ON. Refer to the POWER MANAGEMENT section for the sequence.
This command will turn on booster, controller, regulators, and temperature sensor will be activated for one-time sensing before enabling booster.
When all voltages are ready, the BUSY_N signal will return to high.

5-1-6) POWER ON MEASURE (PMES) (R05 H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
	0	0	0	0	0	0	0	1	0	1	05H

This command enables the internal bandgap, which will be cleared by the next POF.

5-1-7) BOOSTER SOFT START (BTST) (R06 H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	0	0	0	0	0	1	1	0	06H
	0	1	BT_PHA7	BT_PHA6	BT_PHA5	BT_PHA4	BT_PHA3	BT_PHA2	BT_PHA1	BT_PHA0	17H
	0	1	BT_PHB7	BT_PHB6	BT_PHB5	BT_PHB4	BT_PHB3	BT_PHB2	BT_PHB1	BT_PHB0	17H
	0	1	-	-	BT_PHC5	BT_PHC4	BT_PHC3	BT_PHC2	BT_PHC1	BT_PHC0	17H

BTPHA[7:6]: Soft start period of phase A.
00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BTPHA[5:3]: Driving strength of phase A

000b: strength 1 001b: strength 2 010b: strength 3 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHA[2:0]: Minimum OFF time setting of GDR in phase B

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS 111b: 6.58uS

BTPHB[7:6]: Soft start period of phase B.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BTPHB[5:3]: Driving strength of phase B

000b: strength 1 001b: strength 2 010b: strength 3 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHB[2:0]: Minimum OFF time setting of GDR in phase B

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS 111b: 6.58uS

BTPHC[5:3]: Driving strength of phase C

000b: strength 1 001b: strength 2 010b: strength 3 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHC[2:0]: Minimum OFF time setting of GDR in phase C

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS 111b: 6.58uS

5-1-8) DEEP SLEEP (DSLP) (R07 H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Deep Sleep	0	0	0	0	0	0	0	1	1	1	07H
	0	1	1	0	1	0	0	1	0	1	A5 H

After this command is transmitted, the chip will enter Deep Sleep Mode to save power. Deep Sleep Mode will return to Standby Mode by hardware reset. The only one parameter is a check code, the command will be executed if check code = 0xA5.

5-1-9) DATA START TRANSMISSION 1 (DTM1) (R10 H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	0	0	0	1	0	0	0	0	10 H
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8	00H
	0	1	:	:	:	:	:	:	:	:	00H
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)	00H

This command starts transmitting data and write them into SRAM.
In KW mode, this command writes "OLD" data to SRAM.
In KWR mode, this command writes "B/W" data to SRAM.
In Program mode, this command writes "OTP" data to SRAM for programming.

5-1-10) DATA STOP (DSP) (R11 H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Stopping data transmission	0	0	0	0	0	1	0	0	0	1	11H
	1	1	data_flag	-	-	-	-	-	-	-	00 H

Check the completeness of data. If data is complete, start to refresh display.
Data_flag: Data flag of receiving user data.
0: Driver didn't receive all the data.
1: Driver has already received all the one-frame data (DTM1 and DTM2).
After "Data Start" (R10h) or "Data Stop" (R11h) commands and when data_flag=1, the refreshing of panel starts and BUSY_N signal will become "0".

5-1-11) DISPLAY REFRESH (DRF) (R12 H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Refreshing the display	0	0	0	0	0	1	0	0	1	0	12H

While user sent this command, driver will refresh display (data/VCOM) according to SRAM data and LUT. After Display Refresh command, BUSY_N signal will become "0" and the refreshing of panel starts.
The waiting interval form BUSY_N falling to the first FLG command must be larger than 200uS.

5-1-12) DATA START TRANSMISSION 2 (DTM2) (R13 H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	0	0	0	1	0	0	1	1	13H
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8	00H
	0	1	:	:	:	:	:	:	:	:	00H
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)	00H

This command starts transmitting data and write them into SRAM. In KW mode, this command writes "NEW" data to SRAM.
In KWR mode, this command writes "RED" data to SRAM.

5-1-13) AUTO SEQUENCE (AUTO) (R17 H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Auto Sequence	0	0	0	0	0	1	0	1	1	1	17 H
	0	1	1	0	1	0	0	1	0	1	A5 H

The command can enable the internal sequence to execute several commands continuously. The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of host's control procedure. The sequence contains several operations, including PON, DRF, POF, DSLP.
AUTO (0x17) + Code(0xA5) = (PON→DRF→ POF)
AUTO (0x17) + Code(0xA7) = (PON →DRF → POF →DSLP)

5-1-14) VCOM LUT (LUTC) (R20 H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Build Look-up Table for VCOM (61-byte command, structure of bytes 2~7 repeated 10 times)	0	0	0	0	1	0	0	0	0	0	20 H
	0	1	LEVEL SELECT-0		LEVEL SELECT-1		LEVEL SELECT-2		LEVEL SELECT-3		00 H
	0	1	NUMBER OF FRAMES-0								00 H
	0	1	NUMBER OF FRAMES-1								00 H
	0	1	NUMBER OF FRAMES-2								00 H

	0	1	NUMBER OF FRAMES-3	00 H
	0	1	TIMES TO REPEAT	00 H

This command stores VCOM Look-Up Table with 10 groups of data. Each group contains information for one state and is stored with 6 bytes (byte 2~7, 8~13, 14~19, 20~25, …), while the sixth byte indicates how many times that phase will repeat.

Bytes 2, 8, 14, 20, 26, 32, 38, 44, 50, 56:

D[7:6], D[5:4], D[3:2], D[1:0]: Level Selection
00b: VCOM_DC
01b: VDH+VCOM_DC (VCOMH)
10b: VDL+VCOM_DC (VCOML)
11b: Floating

Bytes 3~6, 9~12, 15~18, 21~24, 27~30, 33~36, 39~42, 45~48, 51~54, 57~60:

Number of Frames
0000 0000b: 0 frame
: :
: :
1111 1111b: 255 frames

Bytes 7, 13, 19, 25, 31, 37, 43, 49, 55, 61:

Times to Repeat
0000 0000b: 0 time
: :
: :
1111 1111b: 255 times

If KW/R=0 (KWR mode), all 10 groups are used.
If KW/R=1 (KW mode), only 6 groups are used.

5-1-15) W2W LUT (LUTWW) (R21 H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Build White Look-up Table for W2W (37-byte command, structure of bytes 2~7 repeated 6 times)	0	0	0	0	1	0	0	0	0	1	21 H
	0	1	LEVEL SELECT-0		LEVEL SELECT-1		LEVEL SELECT-2		LEVEL SELECT-3		00 H
	0	1	NUMBER OF FRAMES-0								00 H
	0	1	NUMBER OF FRAMES-1								00 H
	0	1	NUMBER OF FRAMES-2								00 H
	0	1	NUMBER OF FRAMES-3								00 H
	0	1	TIMES TO REPEAT								00 H

This command stores White-to-White Look-Up Table with 6 groups of data. Each group contains information for one state and is stored with 6 bytes (byte 2~7, 8~13, 14~19, 20~25, …), while the sixth byte indicates how many times that phase will repeat.

Bytes 2, 8, 14, 20, 26, 32:

Level Selection.
00b: GND
01b: VDH
10b: VDL
11b: VDHR

Bytes 3~6, 9~12, 15~18, 21~24, 27~30, 33~36:

Number of Frames
0000 0000b: 0 frame
: :
: :
1111 1111b: 255 frames

Bytes 7, 13, 19, 25, 31, 37:
Times to Repeat
0000 0000b: 0 time
: :
: :
1111 1111b: 255 times
If KW/R=0 (KWR mode), LUTWW is not used.
If KW/R=1 (KW mode), LUTWW is used.

5-1-16) B2W LUT (LUTBW / LUTR) (R22 H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Build Look-up Table for B2W or Red (61-byte command, structure of bytes 2~7 repeated 10 times)	0	0	0	0	1	0	0	0	0	1	21 H
	0	1	LEVEL SELECT-0		LEVEL SELECT-1		LEVEL SELECT-2		LEVEL SELECT-3		00 H
	0	1	NUMBER OF FRAMES-0								00 H
	0	1	NUMBER OF FRAMES-1								00 H
	0	1	NUMBER OF FRAMES-2								00 H
	0	1	NUMBER OF FRAMES-3								00 H
	0	1	TIMES TO REPEAT								00 H

This command stores White-to-White Look-Up Table with 10 groups of data. Each group contains information for one state and is stored with 6 bytes (byte 2~7, 8~13, 14~19, 20~25, …), while the sixth byte indicates how many times that phase will repeat.
Bytes 2, 8, 14, 20, 26, 32, 38, 44, 50, 56:
Level Selection.
00b: GND
01b: VDH 10b: VDL 11b: VDHR
Bytes 3~6, 9~12, 15~18, 21~24, 27~30, 33~36, 39~42, 45~48, 51~54, 57~60:
Number of Frames
0000 0000b: 0 frame
: :
: :
1111 1111b: 255 frames
Bytes 7, 13, 19, 25, 31, 37, 43, 49, 55, 61:
Times to Repeat
0000 0000b: 0 time
: :
: :
1111 1111b: 255 times
If KW/R=0 (KWR mode), all 10 groups are used.
If KW/R=1 (KW mode), only 6 groups are used.

5-1-17) W2B LUT (LUTWB / LUTW) (R23 H)

This command builds Look-up Table for White-to-Black. Please refer to W2W LUT (LUTWW) for similar definition details. Regardless of KW/R=0 or KW/R=1, LUTWB/LUTW is used.

5-1-18) B2B LUT (LUTBB / LUTB) (R24 H)

This command builds Look-up Table for Black-to-Black. Please refer to W2W LUT (LUTWW) for similar definition details. Regardless of KW/R=0 or KW/R=1, LUTBB/LUTB is used.

5-1-19) LUT OPTION (LUTOPT) (R2A H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
LUT Option	0	0	0	0	1	0	1	0	1	0	2A H
	0	1	-	-	STATE_XON[5:0]						00H
	0	1	-	-	EXS[2:0]		-	DMS[2:0]			00H

This command sets XON and the 2 options of KWR mode's LUT.

STATE_XON[5:0]:

All Gate ON (Each bit controls one state, STATE_XON [0] for state-1, STATE_XON [1] for state-2 …..)

00 0000b: no All-Gate-ON

00 0001b: State-1 All-Gate-ON

00 0011b: State-1 and State2 All-Gate-ON

: :

DMS[2:0]: Dummy state position. The option is only available when KW/R=0.

EXS[1:0]: Extra state number. The option is only available when KW/R=0.

5-1-20) PLL CONTROL (PLL) (R30 H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Controlling PLL	0	0	0	0	1	1	0	0	0	0	30 H
	0	1	-	-	M[2:0]			N[2:0]			3C H

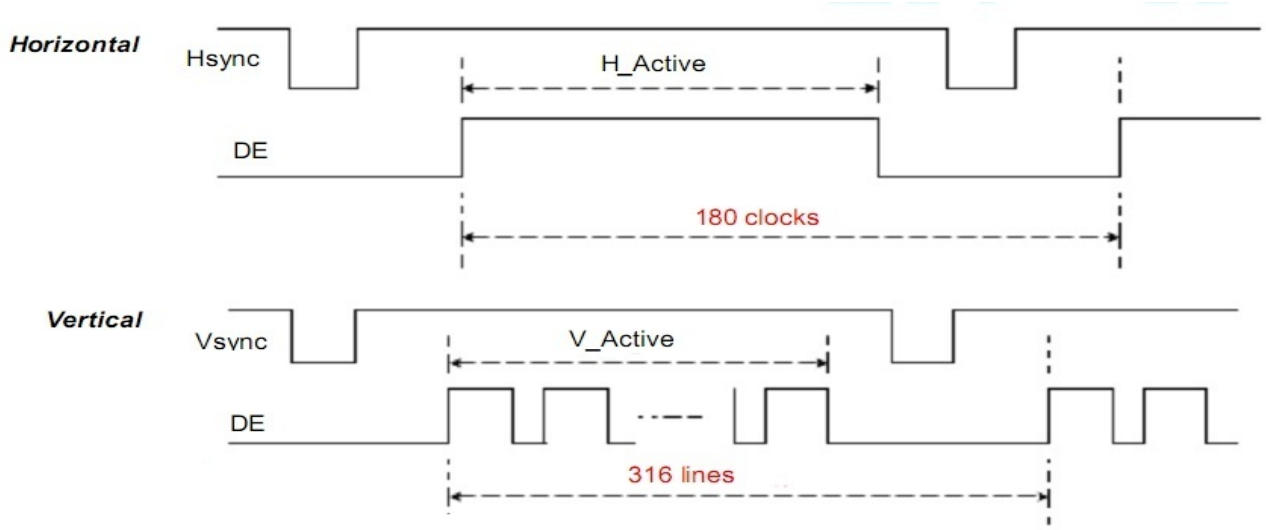
The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

M	N	Frame rate
1	1	29 Hz
	2	14 Hz
	3	10 Hz
	4	7 Hz
	5	6 Hz
	6	5 Hz
	7	4 Hz
2	1	57 Hz
	2	29 Hz
	3	19 Hz
	4	14 Hz
	5	11 Hz
	6	10 Hz
	7	8 Hz

M	N	Frame rate
3	1	86 Hz
	2	43 Hz
	3	29 Hz
	4	21 Hz
	5	17 Hz
	6	14 Hz
	7	12 Hz
4	1	114 Hz
	2	57 Hz
	3	38 Hz
	4	29 Hz
	5	23 Hz
	6	19 Hz
	7	16 Hz

M	N	Frame rate
5	1	150 Hz
	2	72 Hz
	3	48Hz
	4	36 Hz
	5	29 Hz
	6	24 Hz
	7	20 Hz
6	1	171 Hz
	2	86 Hz
	3	57 Hz
	4	43 Hz
	5	34 Hz
	6	29 Hz
	7	24 Hz

M	N	Frame rate
7	1	200 Hz
	2	100 Hz
	3	67 Hz
	4	50 Hz (default)
	5	40 Hz
	6	33 Hz
	7	29 Hz



5-1-21) TEMPERATURE SENSOR CALIBRATION (TSC) (R40H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Sensing Temperature	0	0	0	1	0	0	0	0	0	0	40 H
	1	1	D10/TS7	D9/TS6	D8/TS5	D7/TS4	D6 / TS3	D5 / TS2	D4 / TS1	D3 / TS0	00 H
	1	1	D2	D1	D0	-	-	-	-	-	00 H

This command enables internal or external temperature sensor, and reads the result.

TS[7:0]: When TSE (R41h) is set to 0, this command reads internal temperature sensor value.

D[10:0]: When TSE (R41h) is set to 1, this command reads external LM75 temperature sensor value.

TS[7:0]/D[10:3]	Temperature (℃)
1110_0111	-25
1110_1000	-24
1110_1001	-23
1110_1010	-22
1110_1011	-21
1110_1100	-20
1110_1101	-19
1110_1110	-18
1110_1111	-17
1111_0000	-16
1111_0001	-15
1111_0010	-14
1111_0011	-13
1111_0100	-12
1111_0101	-11
1111_0110	-10
1111_0111	-9
1111_1000	-8
1111_1001	-7
1111_1010	-6

TS[7:0]/D[10:3]	Temperature(℃)
0000_0000	0
0000_0001	1
0000_0010	2
0000_0011	3
0000_0100	4
0000_0101	5
0000_0110	6
0000_0111	7
0000_1000	8
0000_1001	9
0000_1010	10
0000_1011	11
0000_1100	12
0000_1101	13
0000_1110	14
0000_1111	15
0001_0000	16
0001_0001	17
0001_0010	18
0001_0011	19

TS[7:0]/D[10:3]	Temperature(℃)
0001_1001	25
0001_1010	26
0001_1011	27
0001_1100	28
0001_1101	29
0001_1110	30
0001_1111	31
0010_0000	32
0010_0001	33
0010_0010	34
0010_0011	35
0010_0100	36
0010_0101	37
0010_0110	38
0010_0111	39
0010_1000	40
0010_1001	41
0010_1010	42
0010_1011	43
0010_1100	44

1111_1011	-5	0001_0100	20	0010_1101	45
1111_1100	-4	0001_0101	21	0010_1110	46
1111_1101	-3	0001_0110	22	0010_1111	47
1111_1110	-2	0001_0111	23	0011_0000	48
1111_1111	-1	0001_1000	24	0011_0001	49

5-1-22) TEMPERATURE SENSOR ENABLE (TSE) (R41 H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Enable Temperature Sensor /Offset	0	0	0	1	0	0	0	0	0	1	41 H
	0	1	TSE	-	-	-	TO[3:0]				00 H

This command selects Internal or External temperature sensor.
TSE: Internal temperature sensor switch
0: Enable (default) 1: Disable; using external sensor.
TO[3:0]: Temperature offset.

TO[3:0]	Calculation
0000 b	+0 (Default)
0001	+1
0010	+2
0011	+3
0100	+4
0101	+5
0110	+6
0111	+7

TO[3:0]	Calculation
1000	-8
1001	-7
1010	-6
1011	-5
1100	-4
1101	-3
1110	-2
1111	-1

5-1-23) TEMPERATURE SENSOR WRITE (TSW) (R42 H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Write External Temperature Sensor	0	0	0	1	0	0	0	0	1	0	42 H
	0	1	WATTR[7:0]								00 H
	0	1	WMSB[7:0]								00 H
	0	1	WLSB[7:0]								00 H

This command writes the temperature sensed by the temperature sensor.
WATTR[7:6]: I 2 C Write Byte Number
00b : 1 byte (head byte only)
01b : 2 bytes (head byte + pointer)
10b : 3 bytes (head byte + pointer + 1st parameter)
11b : 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)
WATTR[5:3]: User-defined address bits (A2, A1, A0)
WATTR[2:0]: Pointer setting
WMSB[7:0]: MSByte of write-data to external temperature sensor
WLSB[7:0]: LSByte of write-data to external temperature sensor

5-1-24) TEMPERATURE SENSOR READ (TSR) (R43 H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read External Temperature Sensor	0	0	0	1	0	0	0	0	1	1	43 H
	1	1	RMSB[7:0]								00 H
	1	1	RLSB[7:0]								00 H

This command reads the temperature sensed by the temperature sensor.
RMSB[7:0]: MSByte read data from external temperature sensor
RLSB[7:0]: LSByte read data from external temperature sensor

5-1-25) PANEL GLASS CHECK (PBC)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Check Panel Glass	W	0	0	1	0	0	0	1	0	0	44H
	R	1	-	-	-	-	-	-	-	PSTA	00 H

This command is used to enable panel check, and to disable after reading result.
PSTA: 0: Panel check fail (panel broken) 1: Panel check pass

5-1-26) VCOM AND DATA INTERVAL SETTING (CDI) (R50 H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Interval between VCOM and Data	0	0	0	1	0	1	0	0	0	0	50H
	0	1	VBD[1:0]		DDX[1:0]		CDI[3:0]				D7h

This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be kept (20 Hsync).
VBD[1:0]: Border data selection
KWR mode (KW/R=0)

DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTR
	10	LUTW
	11	LUTB
1 (Default)	00	LUTB
	01	LUTW
	10	LUTR
	11	Floating

KW mode (KW/R=1)

DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTBW (1→ 0)
	10	LUTWB (0→1)
	11	Floating
1 (Default)	00	Floating
	01	LUTWB (1→ 0)
	10	LUTBW (0 →1)
	11	Floating

DDX[1:0]: Data polality.
Under KWR mode (KW/R=0):
DDX[1] is for RED data.
DDX[0] is for B/W data,

DDX[1:0]	Data {Red, B/W}	LUT
0	00	LUTW
	01	LUTB
	10	LUTR
	11	LUTR
1 (Default)	00	LUTB
	01	LUTW
	10	LUTR
	11	LUTR

DDX[1:0]	Data {Red, B/W}	LUT
10	00	LUTR
	01	LUTR
	10	LUTW
	11	LUTB
11	00	LUTR
	01	LUTR
	10	LUTB
	11	LUTW

Under KW mode (KW/R=1):
DDX[1]=0 is for KW mode with NEW/OLD,
DDX[1]=1 is for KW mode without NEW/OLD.

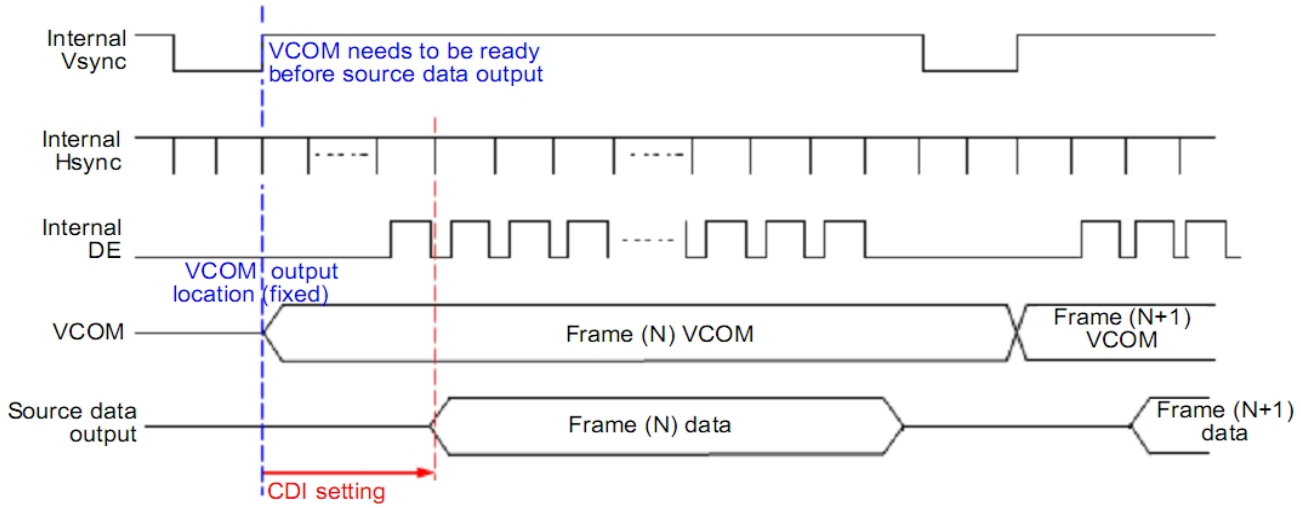
DDX[0]	Data {Red, B/W}	LUT
0	00	LUTWW (0→0)
	01	LUTBW (1→0)
	10	LUTWB (0→1)
	11	LUTBB (1→1)
1 (Default)	00	LUTBB (0→0)
	01	LUTWB (1→0)
	10	LUTBW (0→1)
	11	LUTWW (1→1)

DDX[0]	Data {NEW}	LUT
10	0	LUTBW (1→0)
	1	LUTWB (0→1)
11	0	LUTWB (1→0)
	1	LUTBW (0→1)

CDI[3:0]: VCOM and data interval

CDI[3:0]	VCOM and Data Interval
0000 b	17 hsync
0001	16
0010	15
0011	14
0100	13
0101	12
0110	11
0111	10(Default)

CDI[3:0]	VCOM and Data Interval
1000	9
1001	8
1010	7
1011	6
1100	5
1101	4
1110	3
1111	2



5-1-27)LOW POWER DETECTION (LPD) (R51 H)

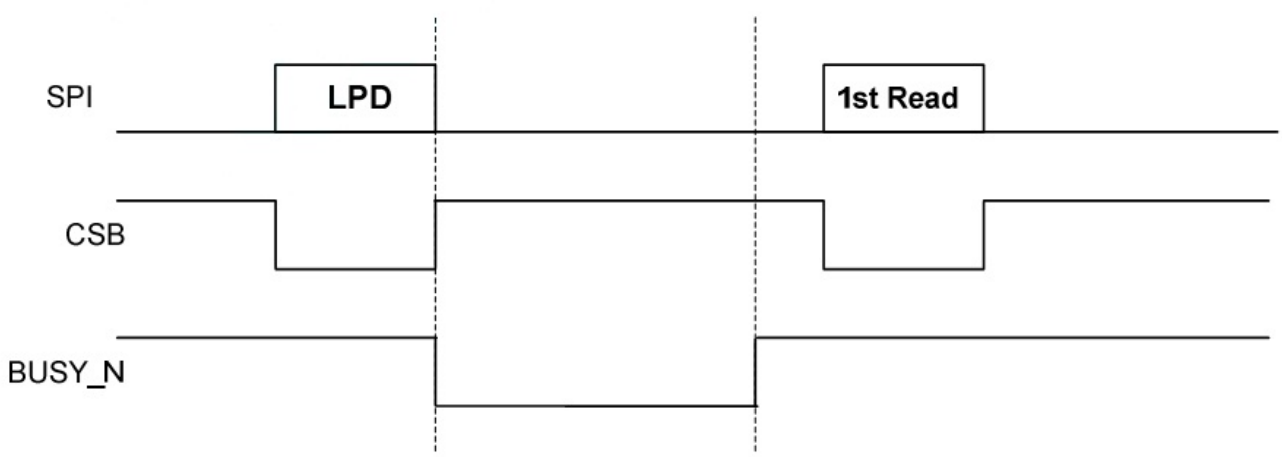
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Detect Low Power	0	0	0	1	0	1	0	0	0	1	51H
	1	1	-	-	-	-	-	-	-	LPD	01h

This command indicates the input power condition. Host can read this flag to learn the battery condition.

LPD: Internal Low Power Detection Flag

0: Low power input (V DD <2.5V, selected by LVD_SEL[1:0] in command LVSEL)

1: Normal status (default)



5-1-28) TCON SETTING (TCON) (R60 H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Gate/Source Non-overlap Period	0	0	0	1	1	0	0	0	0	0	60H
	0	1	S2G[3:0]				G2S[3:0]				22h

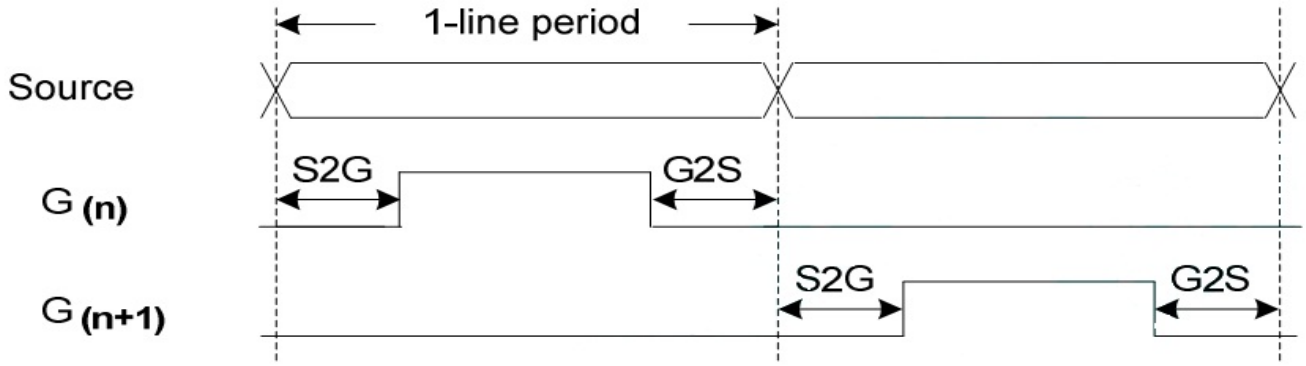
This command defines non-overlap period of Gate and Source.

S2G[3:0] or G2S[3:0]: Source to Gate / Gate to Source Non-overlap period

S2G[3:0] or G2S[3:0]	Period
0000 b	4
0001	8
0010	12 (Default)
0011	16
0100	20
0101	24
0110	28
0111	32

S2G[3:0] or G2S[3:0]	Period
1000 b	36
1001	40
1010	44
1011	48
1100	52
1101	56
1110	60
1111	64

Period Unit = 660 nS.



5-1-29) RESOLUTION SETTING (TRES) (R61 H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Display Resolution	0	0	0	1	1	0	0	0	0	1	61H
	0	1	HRES[7:3]					0	0	0	00h
	0	1	-	-	-	-	-	-	-	VRES[8]	00h
	0	1	VRES[7:0]								00h

This command defines alternative resolution and this setting is of higher priority than the RES[1:0] in R00H (PSR).
HRES[7:3]: Horizontal Display Resolution
VRES[8:0]: Vertical Display Resolution
Active channel calculation:
Gate: First active gate = G0 (defined by GSST setting, default start gate is G0);
Last active gate = VRES[8:0] – 1
Source: First active source = S0 (defined by GSST setting, default start source is S0);
Last active source = HRES[7:3]*8 - 1
Example: 128 (source) x 272 (gate)
Gate: First active gate = G0 (default start gate),
Last active gate = 272 - 1= 271; (VRES[8:0] = 272, G271)
Source: First active source = S0 (default start source),
Last active source = 16*8 – 1 = 127; (HRES[7:3]=16, S127)

5-1-30) GATE /SOURCE START SETTING (GSST) (R65 H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Gate/Source Start	0	0	0	1	1	0	0	1	0	1	61H
	0	1	HST[7:3]					0	0	0	00h
	0	1	-	-	-	-	-	-	-	VST[8]	00h
	0	1	VST[7:0]								00h

This command defines resolution start gate/source position.
HST[7:3]: Horizontal Display Start Position (Source)
VST[8:0]: Vertical Display Start Position (Gate)
Example : 128(Source) x 240(Gate)
HST[7:3] = 4 (HST = 4*8 = 32),
VST[8:0] = 32

Gate: First active gate = G32 (Because HST[7:3] = 4),
Last active gate = G271
Source: First active source = S32 (Because VST[8:0] = 32),
Last active source = S159

5-1-31) REVISION (REV) (R70 H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Chip Revision	0	0	0	1	1	1	0	0	0	0	70H
	1	1	LUT_REV								FFh
	1	1	-	-	-	-	CHIP_REV[3:0]				0Dh

The LUT_REV is read from OTP address = 0x001 / 0x801.
CHIP_REV[3:0]: Chip Revision, fixed at 1101b.

5-1-32) GET STATUS (FLG) (R71 H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read Flags	0	0	0	1	1	1	0	0	0	1	71H
	1	1	-	PTL_flag	I²C_ERR	I²C_BUSYN	Data_flag	PON	POF	BUSY_N	13h

This command reads the IC status.
PTL_FLAG Partial display status (high: partial mode)
I²C_ERR: I²C master error status
I²C_BUSYN: I²C master busy status (low active)
data_flag: Driver has already received all the one frame data
PON: Power ON status
POF: Power OFF status yi
BUSY_N: Driver busy status (low active)

5-1-33) AUTO MEASURE VCOM (AMV) (R80 H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Automatically measure VCOM	0	0	0	1	0	0	0	0	0	0	80H
	0	1	-	-	AMVT[1:0]		XON	AMVS	AMV	AMVE	10h

This command reads the IC status.
AMVT[1:0]: Auto Measure VCOM Time
00b: 3s 01b: 5s (default)
10b: 8s 11b: 10s
XON: All Gate ON of AMV
0: Gate normally scan during Auto Measure VCOM period. (default)
1: All Gate ON during Auto Measure VCOM period.
AMVS: Source output of AMV
0: Source output 0V during Auto Measure VCOM period. (default)
1: Source output VDHR during Auto Measure VCOM period.
AMV: Analog signal
0: Get VCOM value with the VV command (R81h) (default
1: Get VCOM value in analog signal. (External analog to digital converter)
AMVE: Auto Measure VCOM Enable (/Disable)
0: No effect (default)
1: Trigger auto VCOM sensing.

5-1-34) VCOM VALUE (VV) (R81 H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Automatically measure VCOM	0	0	1	0	0	0	0	0	0	1	81H
	1	1	-	-	VV[5:0]						00h

This command gets the VCOM value.
VV[5:0]: VCOM Value Output

VV [5:0]	VCOM Voltage (V)	VV [5:0]	VCOM Voltage (V)	VV [5:0]	VCOM Voltage (V)
00 0000b	-0.10	01 0100b	-1.10	10 1000b	-2.10
00 0001b	-0.15	01 0101b	-1.15	10 1001b	-2.15
00 0010b	-0.20	01 0110b	-1.20	10 1010b	-2.20
00 0011b	-0.25	01 0111b	-1.25	10 1011b	-2.25
00 0100b	-0.30	01 1000b	-1.30	10 1100b	-2.30
00 0101b	-0.35	01 1001b	-1.35	10 1101b	-2.35
00 0110b	-0.40	01 1010b	-1.40	10 1110b	-2.40
00 0111b	-0.45	01 1011b	-1.45	10 1111b	-2.45
00 1000b	-0.50	01 1100b	-1.50	11 0000b	-2.50
00 1001b	-0.55	01 1101b	-1.55	11 0001b	-2.55
00 1010b	-0.60	01 1110b	-1.60	11 0010b	-2.60
00 1011b	-0.65	01 1111b	-1.65	11 0011b	-2.65
00 1100b	-0.70	10 0000b	-1.70	11 0100b	-2.70
00 1101b	-0.75	10 0001b	-1.75	11 0101b	-2.75
00 1110b	-0.80	10 0010b	-1.80	11 0110b	-2.80
00 1111b	-0.85	10 0011b	-1.85	11 0111b	-2.85
01 0000b	-0.90	10 0100b	-1.90	11 1000b	-2.90
01 0001b	-0.95	10 0101b	-1.95	11 1001b	-2.95
01 0010b	-1.00	10 0110b	-2.00	11 1010b	-3.00
01 0011b	-1.05	10 0111b	-2.05	11 1011b	-3.05

5-1-35) VCOM_DC SETTING (VDCS) (R82 H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set VCOM_DC	0	0	1	0	0	0	0	0	1	0	82H
	0	1	-	-	VDCS[5:0]						00h

This command sets VCOM_DC value
VDCS[5:0]: VCOM_DC Setting

VDCS [5:0]	VCOM Voltage (V)	VDCS [5:0]	VCOM Voltage (V)	VDCS [5:0]	VCOM Voltage (V)
00 0000b	-0.10	01 0100b	-1.10	10 1000b	-2.10
00 0001b	-0.15	01 0101b	-1.15	10 1001b	-2.15
00 0010b	-0.20	01 0110b	-1.20	10 1010b	-2.20
00 0011b	-0.25	01 0111b	-1.25	10 1011b	-2.25
00 0100b	-0.30	01 1000b	-1.30	10 1100b	-2.30
00 0101b	-0.35	01 1001b	-1.35	10 1101b	-2.35
00 0110b	-0.40	01 1010b	-1.40	10 1110b	-2.40
00 0111b	-0.45	01 1011b	-1.45	10 1111b	-2.45
00 1000b	-0.50	01 1100b	-1.50	11 0000b	-2.50

00 1001b	-0.55	01 1101b	-1.55	11 0001b	-2.55
00 1010b	-0.60	01 1110b	-1.60	11 0010b	-2.60
00 1011b	-0.65	01 1111b	-1.65	11 0011b	-2.65
00 1100b	-0.70	10 0000b	-1.70	11 0100b	-2.70
00 1101b	-0.75	10 0001b	-1.75	11 0101b	-2.75
00 1110b	-0.80	10 0010b	-1.80	11 0110b	-2.80
00 1111b	-0.85	10 0011b	-1.85	11 0111b	-2.85
01 0000b	-0.90	10 0100b	-1.90	11 1000b	-2.90
01 0001b	-0.95	10 0101b	-1.95	11 1001b	-2.95
01 0010b	-1.00	10 0110b	-2.00	11 1010b	-3.00
01 0011b	-1.05	10 0111b	-2.05	11 1011b	-3.05

5-1-36) PARTIAL WINDOW (PTL) (R90 H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Partial Window	0	0	1	0	0	0	0	0	1	0	90h
	0	1	HRST[7:3]					0	0	0	00h
	0	1	HRED[7:3]					1	1	1	07h
	0	1	-	-	-	-	-	-	-	VRST[8]	00h
	0	1	VRST[7:0]								00h
	0	1	-	-	-	-	-	-	-	VRED[8]	00h
	0	1	VRED[7:0]								00h
	0	1	-	-	-	-	-	-	-	VRED[8]	01h

This command sets partial window.
HRST[7:3]: Horizontal start channel bank. (value 00h~13h)
HRED[7:3]: Horizontal end channel bank. (value 00h~13h). HRED must be greater than HRST.
VRST[8:0]: Vertical start line. (value 000h~127h)
VRED[8:0]: **Vertical end line. (value 000h~127h). VRED must be greater than VRST.**
PT_SCAN: 0: Gates scan only inside of the partial window.
1: Gates scan both inside and outside of the partial window. (default)

5-1-37) PARTIAL IN (PTIN) (R91 H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Partial In	0	0	1	0	0	1	0	0	0	1	91h

This command makes the display enter partial mode.

5-1-38) PARTIAL OUT (PTOUT) (R92 H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Partial Out	0	0	1	0	0	1	0	0	1	0	92h

This command makes the display exit partial mode and enter normal mode.

5-1-39) PROGRAM MODE (PGM) (RA0 H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Enter Program Mode	0	0	1	0	1	0	0	0	0	0	A0h

After this command is issued, the chip would enter the program mode.
After the programming procedure completed, a hardware reset is necessary for leaving program mode.

5-1-40) ACTIVE PROGRAM (APG) (RA1 H)

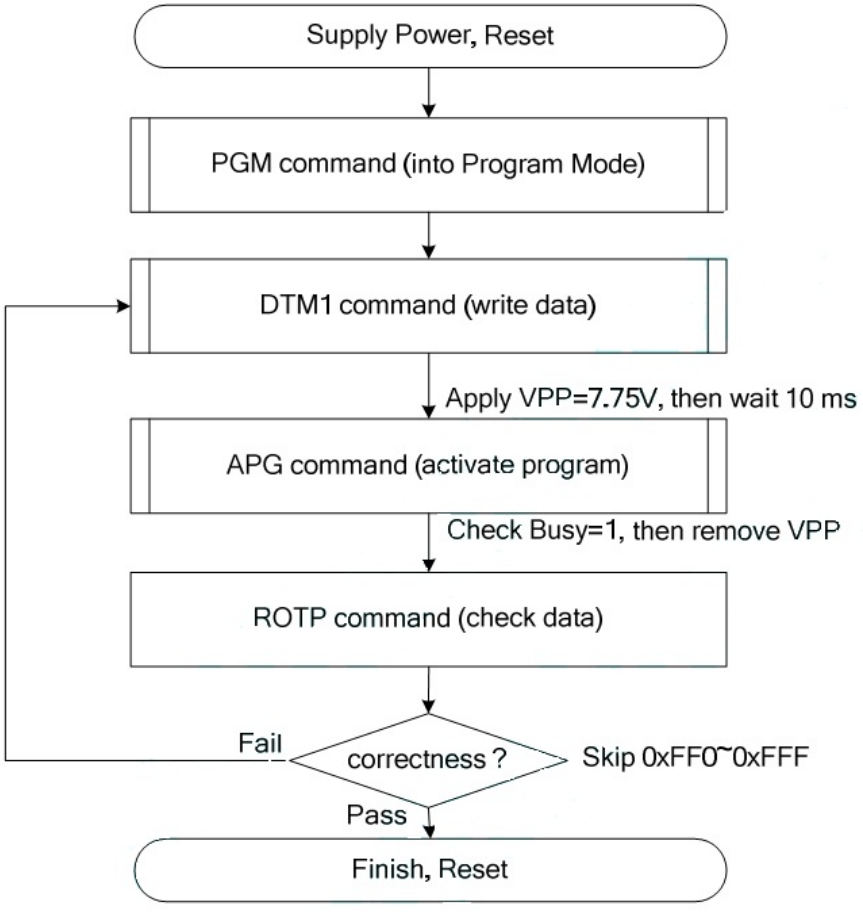
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Active Program OTP	0	0	1	0	1	0	0	0	0	1	A1h

After this command is transmitted, the programming state machine would be activated.
The BUSY_N flag would fall to 0 until the programming is completed.

5-1-41) READ OTP DATA (ROTP) (RA2 H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read OTP data for check	0	0	1	0	1	0	0	0	1	0	A2h
	1	1	Dummy								--
	1	1	The data of address 0x000 in the OTP								--
	1	1	The data of address 0x001 in the OTP								--
	1	1	:								--
	1	1	The data of address (n-1) in the OTP								--
	1	1	The data of address (n) in the OTP								--

The command is used for reading the content of OTP for checking the data of programming.
The value of (n) is depending on the amount of programmed data, the max address = 0xFFF.



The sequence of programming OTP.

5-1-42) CASCADE SETTING (CCSET) (RE0 H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Cascade Option	0	0	1	1	1	0	0	0	0	0	E0h
	0	1	-	-	-	-	-	-	TSFIX	CCEN	00h

This command is used for cascade.

CCEN: Output clock enable/disable.

0: Output 0V at CL pin. (default)

1: Output clock at CL pin for slave chip.

TSFIX: Let the value of slave's temperature is same as the master's.

0: Temperature value is defined by internal temperature sensor / external LM75. (default)

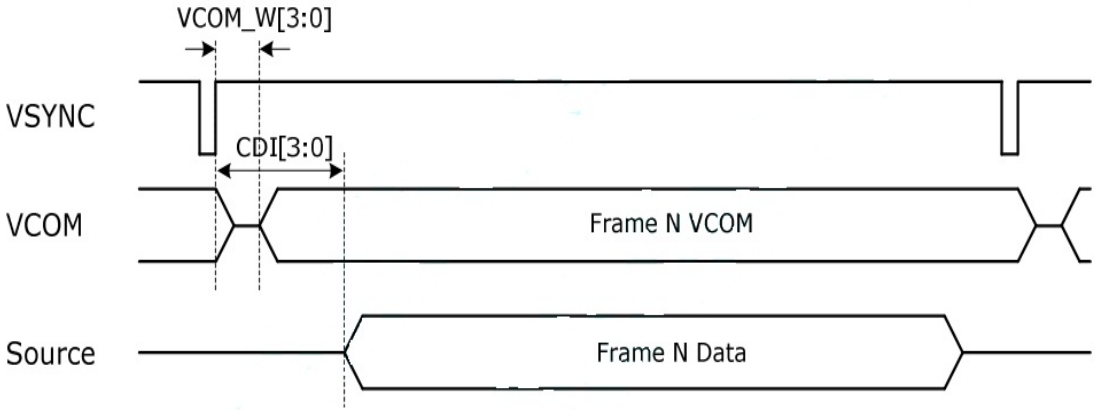
1: Temperature value is defined by TS_SET[7:0] registers.

5-1-43) POWER SAVING (PWS) (RE3 H)

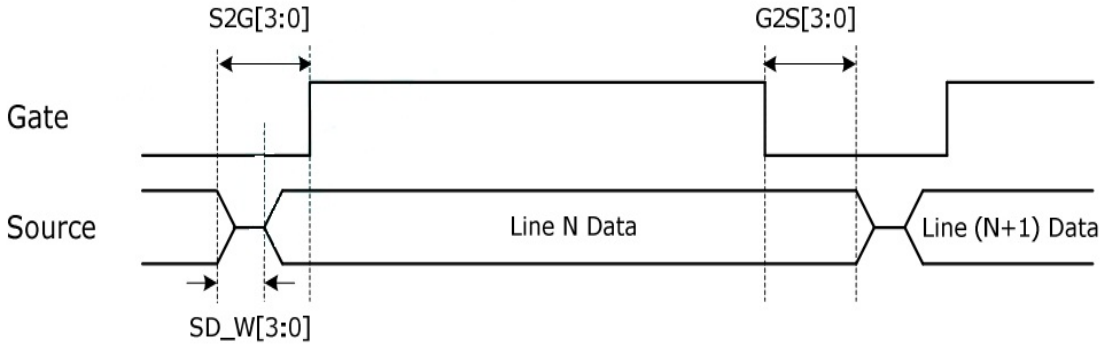
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Power Saving for VCOM & Source	0	0	1	1	1	0	0	0	1	1	E3h
	0	1	VCOM_W[3:0]				SD_W[3:0]				00h

This command is set for saving power during refreshing period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.

VCOM_W[3:0]: VCOM power saving width (unit = line period)



SD_W[3:0]: Source power saving width (unit = 660nS)



5-1-44) LVD VOLTAGE SELECT (LVSEL) (RE4 H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Select LVD Voltage	0	0	1	1	1	0	0	1	0	0	E4h
	0	1	-	-	-	-	-	-	LVD_SEL[1:0]		03h

LVD_SEL[1:0]: Low Power Voltage selection

LVD_SEL[1:0]	LVD value
00	< 2.2 V
01	< 2.3 V
10	< 2.4 V
11	< 2.5 V (default)

5-1-45)FORCE TEMPERATURE (TSSET) (RE5 H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Force Temperature Value for Cascade	0	0	1	1	1	0	0	1	0	1	E5h
	0	1	TS_SET[7:0]								00h

This command is used for cascade to fix the temperature value of master and slave chip.

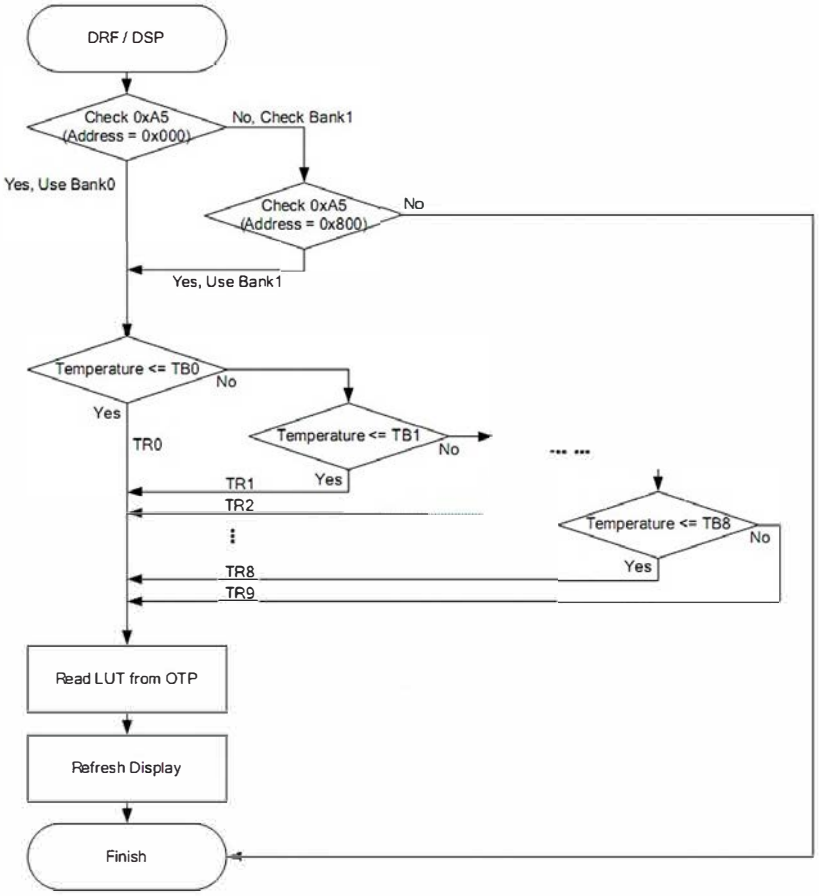
6. TEMPERATURE RANGE

The temperature selection mechanism consists of a less-than-or-equal-to operator and 9 temperature boundary settings (TBx) to determine 10 temperature ranges. The sequence of mechanism is from TB0 to TB8, as shown below. If less than 10 tempeature ranges are used, the last TBx must be set to 0x7F to end the mechanism.

Procedure Order	Comparison Condition	Action & Segment Selection
1-0. Read 0x000	Content = 0xA5 ?	Yes: Jump to Procedure 2 (Bank0), No: Jump to Procedure 1-1
1-1, Read 0x800	Content = 0xA5 ?	Yes: Jump to Procedure 2 (Bank1), No: Stop Refresh
2. Read 0x002 / 0x802	Real Temperature ≦ TB0	Use TR0's table & setting, exit
3. Read 0x003 / 0x803	Real Temperature ≦ TB1	Use TR1's table & setting, exit
4. Read 0x004 / 0x804	Real Temperature ≦ TB2	Use TR2's table & setting, exit
5. Read 0x005 / 0x805	Real Temperature ≦ TB3	Use TR3's table & setting, exit
6. Read 0x006 / 0x806	Real Temperature ≦ TB4	Use TR4's table & setting, exit
7. Read 0x007 / 0x807	Real Temperature ≦ TB5	Use TR5's table & setting, exit
8. Read 0x008 / 0x808	Real Temperature ≦ TB6	Use TR6's table & setting, exit
9. Read 0x009 / 0x809	Real Temperature ≦ TB7	Use TR7's table & setting, exit
10. Read 0x00A / 0x80A	Real Temperature ≦ TB8	Use TR8's table & setting, exit
11. Other	Real Temperature ＞ TB8	Use TR9's table & setting, finish

*Note:
(1) TRx's content is defined in “LUT F ORMAT IN OTP” section.
Example:
If temperature = -20 o C, TR0 is selected.
If temperature = -10 o C, TR1 is selected.
If temperature = 0 o C, TR2 is selected.
If temperature = 20 o C, TR4 is selected.
If temperature = 40 o C, TR5 is selected.
If temperature > 40 o C, TR5 is selected.

OTP Address	Content	
002h	0xF1	(-15℃)
003h	0xFB	(-5℃)
004h	0x00	(0℃)
005h	0x0A	(10℃)
006h	0x1E	(30℃)
007h	0x7F	



Temperature Selection Mechanism

7. PANEL BREAK CHECK

The panel break check (PBC) function is accomplished by testing the connection of the ITO along panel edge. If the panel is broken, the loop ITO may be cut off. The connection check is judged by signal transmission from CHKGO to CHKGI.

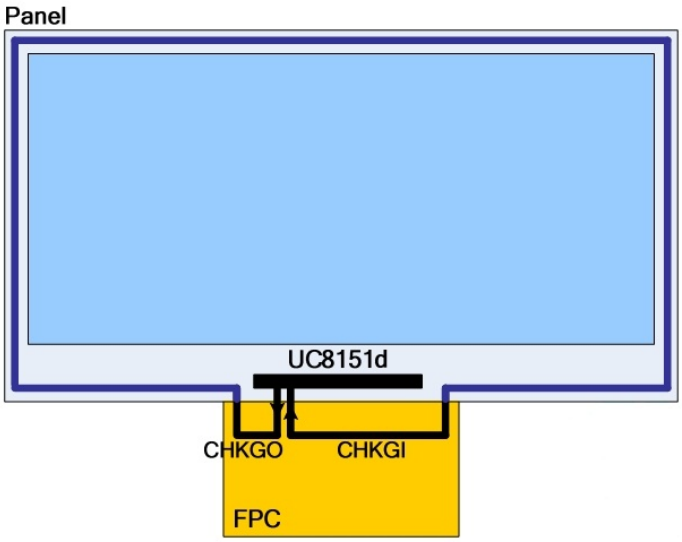


Figure: Panel break check layout example

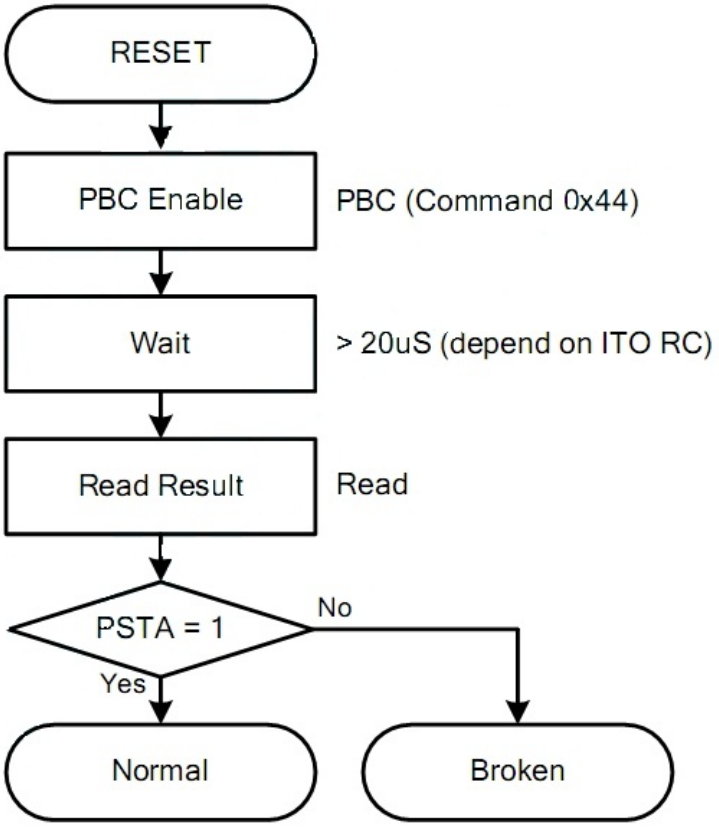


Figure: Panel Break Check (PBC) Sequence

8. Optical characteristics

8.1 Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25℃

SYMBOL	PARAMETER	CONDITIONS	MIN	TYPE	MAX	UNIT	Note
R	Reflectance	White	30	35	-	%	Note 8.1-1
Gn	2Grey Level	-	-	DS+(WS-DS)×n(m-1)	-	L*	-
RS_a*	Red State a* value	Red	35	45	48	-	Note 8.1-1
CR	Contrast Ratio	indoor	-	15	-	-	-
Panel's life	-	0℃～40℃		5years or 1000000 times	-	-	-
Panel	Image Update	Storage and transportation	-	Update the white screen	-	-	-
	Update Time	Operation	-	at least update 1 time per day	-	-	-

WS: White state, DS : Dark state

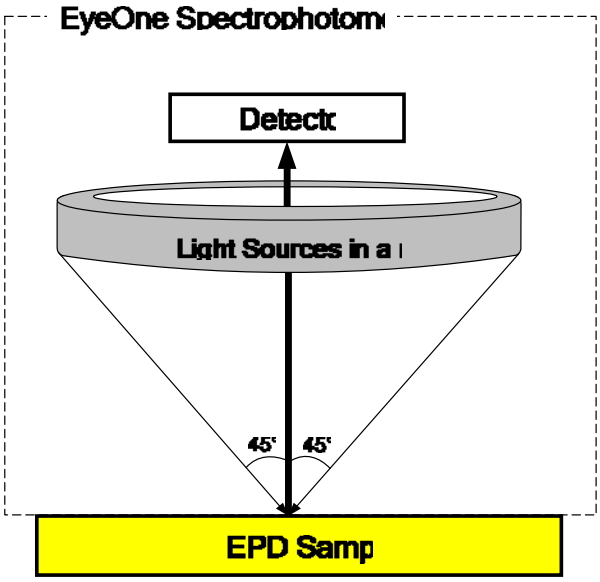
m: 2

Note 8.1-1: Luminance meter : Eye - One Pro Spectrophotometer

8.2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectance in a dark area (Rd):

CR = Rl/Rd

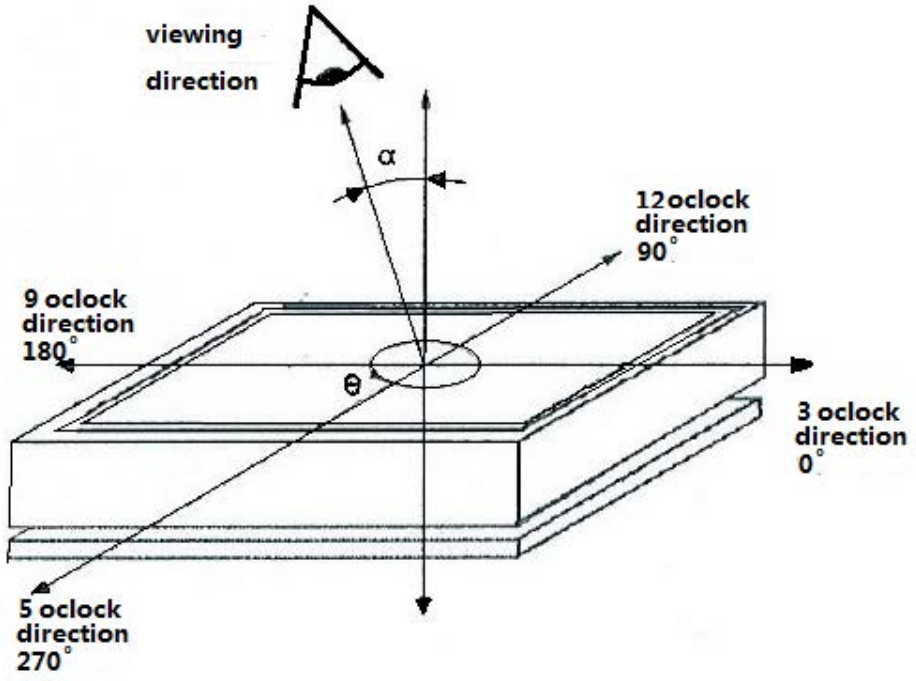


8.3 Reflection Ratio

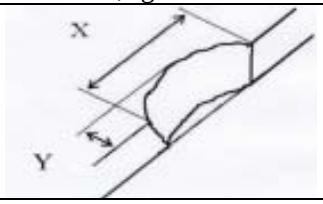
The reflection ratio is expressed as:

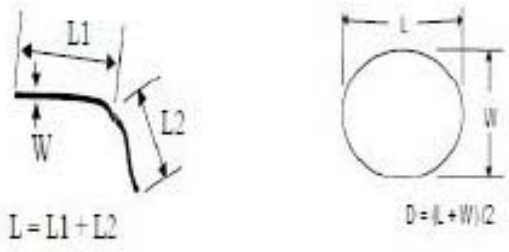
R = Reflectance Factor $_{\text{white board}}$ x (L_{center} / $L_{\text{white board}}$)

L_{center} is the luminance measured at center in a white area (R=G =B=1). $L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.



9. Point and line standard

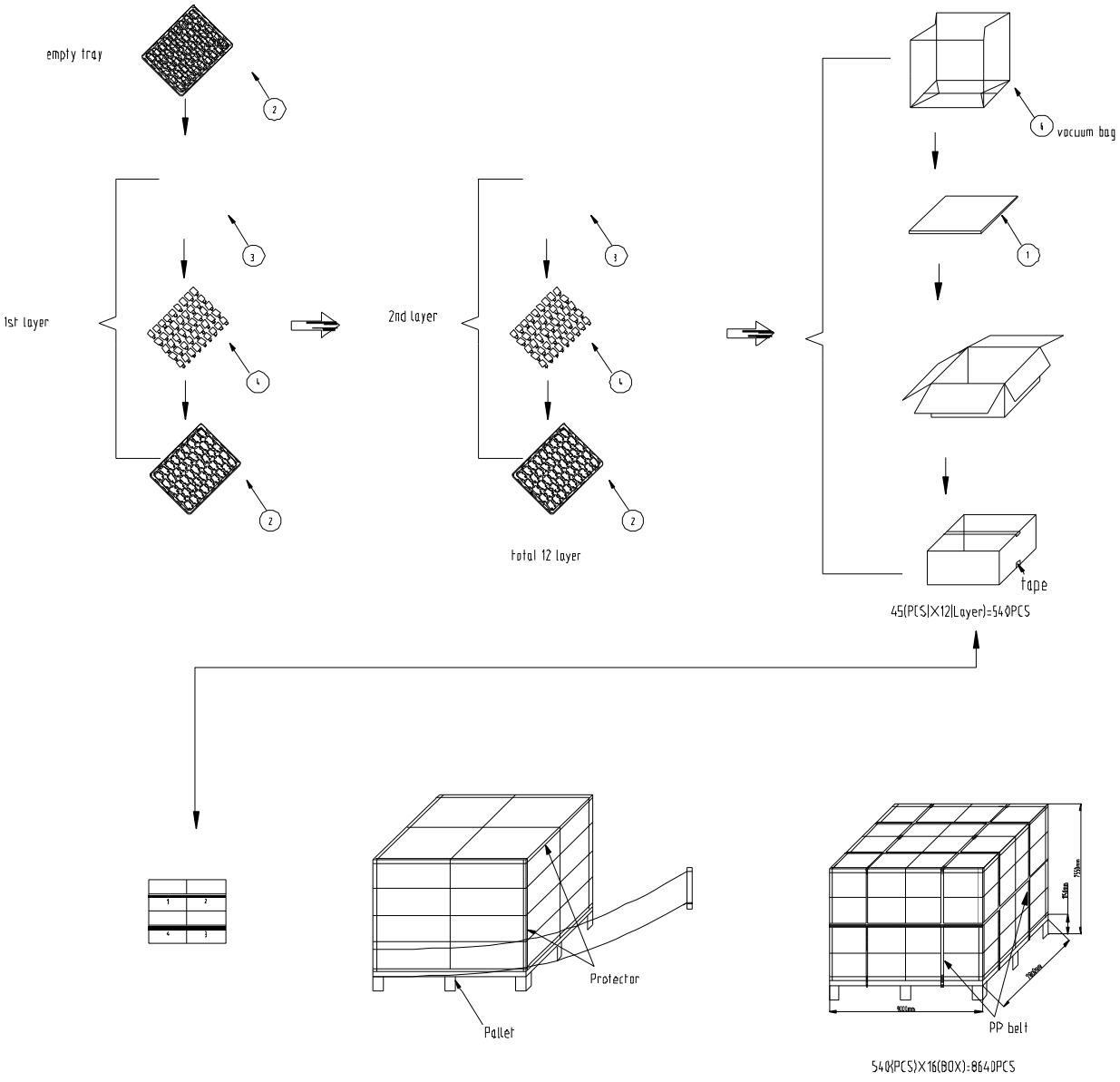
<table>
<tr><th colspan="7">Shipment Inspection Standard</th></tr>
<tr><td colspan="7">Equipment：Electrical test fixture, Point gauge</td></tr>
<tr><td>Outline dimension</td><td>36.7(H)×79.0(V) ×1.15(D)</td><td>Unit：㎜</td><td>Part-A</td><td>Active area</td><td>Part-B</td><td>Border area</td></tr>
<tr><td rowspan="2">Environment</td><td>Temperature</td><td>Humidity</td><td>Illuminance</td><td>Distance</td><td>Time</td><td>Angle</td></tr>
<tr><td>19℃～25℃</td><td>55%±5%RH</td><td>800～1300Lux</td><td>300 ㎜</td><td>35Sec</td><td></td></tr>
<tr><td>Defet type</td><td>Inspection method</td><td colspan="2">Standard</td><td colspan="2">Part-A</td><td>Part-B</td></tr>
<tr><td rowspan="3">Spot</td><td rowspan="3">Electric Display</td><td colspan="2">D≤0.25 ㎜</td><td colspan="2">Ignore</td><td>Ignore</td></tr>
<tr><td colspan="2">0.25 ㎜＜D≤0.4 ㎜</td><td colspan="2">N≤4</td><td>Ignore</td></tr>
<tr><td colspan="2">D＞0.4 ㎜</td><td colspan="2">Not Allow</td><td>Ignore</td></tr>
<tr><td>Display unwork</td><td>Electric Display</td><td colspan="2">Not Allow</td><td colspan="2">Not Allow</td><td>Ignore</td></tr>
<tr><td>Display error</td><td>Electric Display</td><td colspan="2">Not Allow</td><td colspan="2">Not Allow</td><td>Ignore</td></tr>
<tr><td rowspan="3">Scratch or line defect(include dirt)</td><td rowspan="3">Visual/Film card</td><td colspan="2">L≤2 ㎜，W≤0.2 ㎜</td><td colspan="2">Ignore</td><td>Ignore</td></tr>
<tr><td colspan="2">2.0mm＜L≤5.0mm，0.2＜W≤0.3mm,</td><td colspan="2">N≤2</td><td>Ignore</td></tr>
<tr><td colspan="2">L＞5 ㎜，W＞0.3 ㎜</td><td colspan="2">Not Allow</td><td>Ignore</td></tr>
<tr><td rowspan="3">PS Bubble</td><td rowspan="3">Visual/Film card</td><td colspan="2">D≤0.2mm</td><td colspan="2">Ignore</td><td>Ignore</td></tr>
<tr><td colspan="2">0.2mm≤D≤0.35mm & N≤4</td><td colspan="2">N≤4</td><td>Ignore</td></tr>
<tr><td colspan="2">D＞0.35 mm</td><td colspan="2">Not Allow</td><td>Ignore</td></tr>
<tr><td rowspan="2">Side Fragment</td><td rowspan="2">Visual/Film card</td><td colspan="5">X≤5mm，Y≤0.5mm, Do not affect the electrode circuit , Ignore</td></tr>
<tr><td colspan="5"> 
</td></tr>
<tr><td rowspan="3">Remark</td><td colspan="6">1.Cannot be defect & failure cause by appearance defect；</td></tr>
<tr><td colspan="6">2.Cannot be larger size cause by appearance defect；</td></tr>
<tr><td colspan="6">L=long W=wide D=point size N=Defects NO</td></tr>
</table>



Line Defect　　Spot Defect

L=long　　W=wide　D=point size

10. Packing


empty tray
2
1st layer
3
4
2
2nd layer
3
4
2
total 12 layer
4
vacuum bag
1
tape
45(PCS)X12(Layer)=540PCS
Protector
Pallet
PP belt
540(PCS)X16(BOX)=8640PCS

11. Precautions

(1) Do not apply pressure to the EPD panel in order to prevent damaging it.

(2) Do not connect or disconnect the interface connector while the EPD panel is in operation.

(3) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.

(4) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.

(5) If the EPD Panel / Module is not refreshed every 24 hours, a phenomena known as “Ghosting” or “Image Sticking” may occur. It is recommended to refreshed the ESL /EPD Tag every 24 hours in use case. It is recommended that customer ships or stores the ESL / EPD Tag with a completely white image to avoid this issue

(6) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel’s performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.