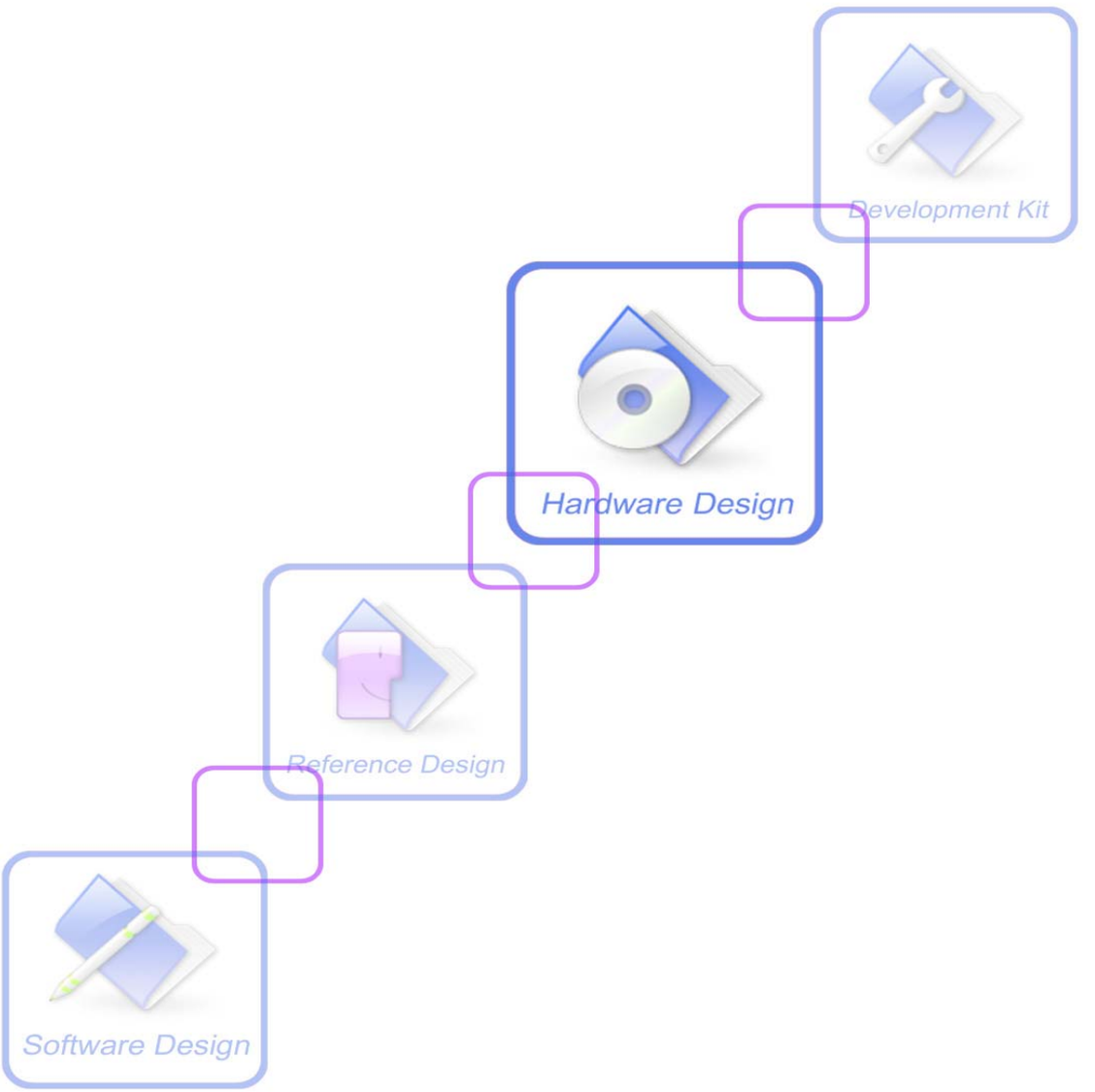
SIM18_Hardware Design_V1.00



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Version history

Date	Version	Description of change	Author
2010-10-07	V1.00	Origin	Huangqiuju

1 Introduction

This document describes the hardware interface of the SIMCom SIM18 module that can be used as a stand alone or Aided GPS receiver. As SIM18 can be integrated with a wide range of applications, all functional components of SIM18 are described in great detail.

1.1 Related Documents

Table 1: Related Documents

SN	Document name	Remark
[I]	CS-130679-DS-3	GSD4E datasheet
[II]	CS-129291-DC-2	One Socket Protocol Interface Control Document
[III]	CS-129435-MA	NMEA Reference Manual

1.2 Terms and Abbreviations

Table 1: Terms and Abbreviations

Abbreviation	Description
CGEE	Client Generated Extended Ephemeris
CMOS	Complementary Metal Oxide Semiconductor
EEPROM	Electrically Erasable Programmable Read Only Memory
FSM	Finite State Machine
GPS	Global Positioning System
I/O	Input/Output
IC	Integrated Circuit
Inorm	Normal Current
Imax	Maximum Load Current
kbps	Kilo bits per second
KA	Keep alive
NEMA	National Marine Electronics Association
OSP	One Socket Protocol
POR	Power on reset

ROM	Read Only Memory
RTC	Real Time Clock
RX	Receive Direction
SGEE	Server Generated Extended Ephemeris
TBD	To be defined
TTFF	Time To First Fix
TX	Transmit Direction
VIHmax	Maximum Input High Level Voltage Value
VIHmin	Minimum Input High Level Voltage Value
VILmax	Maximum Input Low Level Voltage Value
VILmin	Minimum Input Low Level Voltage Value
VImax	Absolute Maximum Input Voltage Value
VImin	Absolute Minimum Input Voltage Value
Vmax	Maximum Voltage Value
Vmin	Minimum Voltage Value
Vnorm	Normal Voltage Value
VOHmax	Maximum Output High Level Voltage Value
VOHmin	Minimum Output High Level Voltage Value
VOLmax	Maximum Output Low Level Voltage Value
VOLmin	Minimum Output Low Level Voltage Value

2 Overview

The SIM18 module is a ROM-based stand-alone or Aided GPS receiver. Designed with the new generation of SiRFstarIV^{TM} navigation processor, The SIM18 can acquire as low as -161dBm even without network assistance and can cost as low as 36uW @1.8V power consumption in sleep mode. Because of its ROM-based structure, SIM18 requires no host integration and is easy to use and can enable a shorter time to market.

With a tiny configuration of 11mm x 11mm x 2.2mm, SIM18 can meet almost all the space requirements in your applications.

The module provides complete signal processing from antenna input to host port in either NMEA messages or in SiRF OSP binary protocol. The module requires 1.8V power supply. The host port is configurable to UART, SPI or I^2C during power up. Host data and I/O signal levels are 1.8V CMOS compatible, inputs are 3.6V tolerable.

The SiRFstar IV provides a new feature called SiRFAware (also referenced as Micro Power Management mode), which enables fast TTFF for Snap start mode while consuming only 500 uA average current (typical) in autonomous sleep mode. The receiver does wakeup autonomously to calibrate internal GPS time and to collect ephemeris data while maintaining 1 sec Snap fix capability.

The receiver is optionally self-assisted since the Client Generated Extended Ephemeris (CGEE) calculation is embedded in the software without any resources required from the host. The CGEE data is stored on external serial EEPROM memory on the master mode DR I^2C bus (which can be also optionally transferred to/from host).

The module supports also connectivity to optional external sensors for Dead Reckoning on the DR I^2C bus.

2.1 SIM18 Functional Diagram

The following figure shows a functional diagram of the SIM18 and illustrates the mainly functional parts:

- The GPS chip
- LNA
- SAW filter
- The antenna interface
- The communication interface
- The control signals

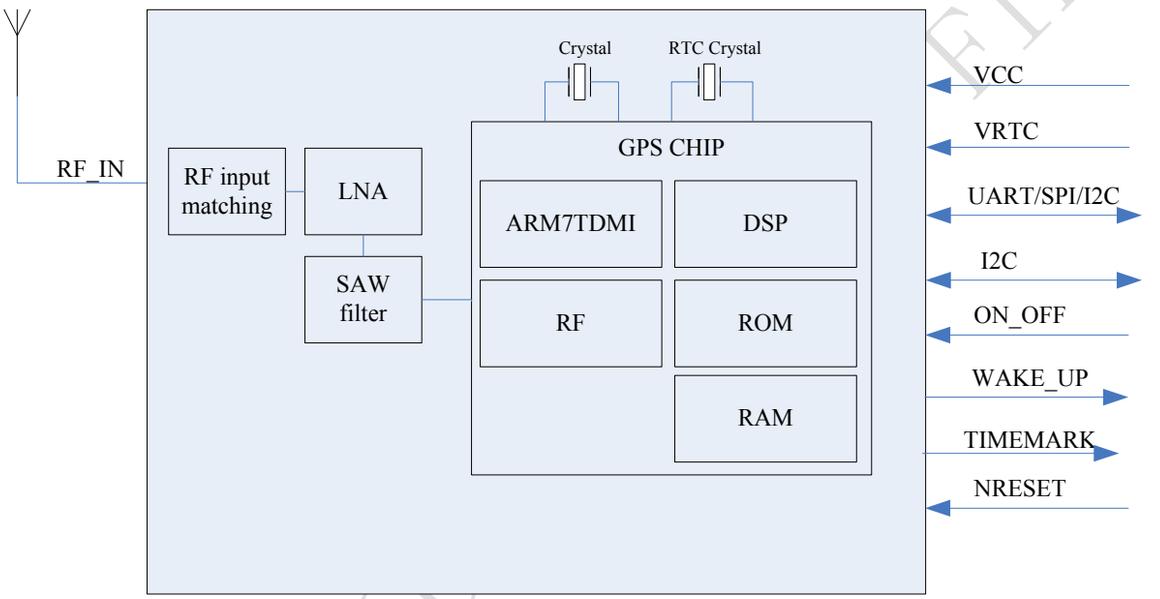

Figure 1: SIM18 functional diagram

2.2 GPS Performance

SIM18 is a ROM-based GPS module, the firmware that is associated with SIM18 is executed for internal ROM memory. The firmware inside SIM18 internal ROM memory is called as the default firmware, current SIM18 default firmware version is V01, as showing in SIM18-Z01 Label.
The characteristics in the following table are tested on SIM18-Z01 without ROM firmware patch.

Table 2: GPS Performance

Parameter	Description	Performance			
		Min	Typ	Max	Unit
Horizontal Position Accuracy[(a)]	Autonomous		<2.5		m
Velocity Accuracy[(b)]	Speed		<0.01		m/s
	Heading		<0.01		°
Time To First Fix[(c)]	Hot start		<1		s
	Warm start		<33		s
	Cold start		33	40	s
Sensitivity	Autonomous acquisition		-147		dBm
	Tracking		-161		dBm
Receiver	Channels		48		
	Update rate		1		Hz
	Altitude			<18288	km
	Velocity			<1850	km/h
	Tracking L1, CA Code				
	Protocol support NMEA,OSP				
Power consumption[(d)]	Continuous tracking		40		mA
	Sleep current		20		uA

(a) 50% 24hr static, -130dBm
(b) 50% at 30m/s
(c) GPS sigal level: -130 dBm
(d) single Power supply 1.8V

2.3 SIM18 Evaluation Board

In order to help user on the application of SIM18, SIMCom can supply an Evaluation Board (EVB) that interfaces SIM18 directly with appropriate power supply, USB interface, antenna and all control signals of the SIM18.

Figure 2: Top view of SIM18 EVB

For details please refer to the *SIM18-EVB_UGD* document.

3 Application Interface

SIM18 is equipped with a 24-pin SMT pad that connects to the GPS application platform. Sub-interfaces included in these SMT pads are described in detail in the following chapters:

- Power management *(please refer to Chapter 3.2.1)*
- Host interfaces *(please refer to Chapter 3.3)*

Electrical and mechanical characteristics of the SMT pad are specified in *Chapter 5*.

3.1 SIM18 Pin Description

Table 3: Pin description

Power Supply				
PIN NAME	I/O	DESCRIPTION	DC CHARACTERISTICS	COMMENT
VCC	I	Main power input, which will be used to power the baseband and RF section internal.	Vmax= 1.89V Vmin=1.71V Vnorm=1.8V	Provide clean and stable power source to this pin. Add a 4.7uF capacitor to this pin for decouple.
VRTC	I/O	1.8V backup battery input	Vmax= 1.89V Vmin=1.71V Vnorm=1.8V	If KA mode is not used, connect this pin to VCC directly; if KA mode is used, VRTC should be powered by a 1.8V power supply all the time.
VCC_RF	O	1.8V output power supply for active antenna	Vmax= 1.89V Vmin=1.71V Vnorm=1.8V	If it is used, connect to VCC_ANT directly. If unused, keep open.
VCC_ANT	I	Power input for active antenna	Vmax= 5.5V Vmin=-5.5V	It depends on your active antenna's power requirement, if it is unused, keep

				open
GND		Ground		
Power control				
PIN NAME	I/O	DESCRIPTION	DC CHARACTERISTICS	
ON_OFF	I	Control the module to go into or wakeup from sleep mode	VIHmin=0.7*VCC VIHmax=3.6V VILmax=0.45V VILmin= -0.4V	
WAKEUP	O	Indicate the module's state, when run, to be high; when in sleep or off state, to be low	VOHmin=0.75*VCC VOmax=VCC VOLmax=0.4V VOLmin= 0V	If unused, keep open
nRESET	I	External reset input, active low	VIHmin=0.7*VCC VIHmax=3.6V VILmax=0.45V VILmin= -0.4V	If unused, keep open
Host port interface				
PIN NAME	I/O	DESCRIPTION	DC CHARACTERISTICS	COMMENT
TXD/MISO/SCL2	O	Function overlay: slave SPI data output(MISO) UART data transmit(TXD) I² C bus clock (SCL2)	VOHmin=0.75*VCC VOmax=VCC VOLmax=0.4V VOLmin= 0V	The default interface is SPI, user can configure the CTS/CLK and RTS/CS signal to select host port interface type. for details, please refer to chapter3.3.
RXD/MOSI/SDA2	I	Function overlay: slave SPI data input(MOSI) UART data receive(RXD) I² C bus data (SDA2)	VIHmin=0.7*VCC VIHmax=3.6V VILmax=0.45V VILmin= -0.4V	
CTS/CLK	IO	slave SPI clock input(CLK) UART clear to send(CTS) active low	VOHmin=0.75*VCC VOmax=VCC VOLmax=0.4V VOLmin= 0V	
RTS/CS	IO	slave SPI chip select (CS) active low UART ready to send (RTS) active low	VOHmin=0.75*VCC VOmax=VCC VOLmax=0.4V VOLmin= 0V	
GPIO				

SCL1	IO	dead reckoning I²C bus data (SCL)	VOHmin=0.75*VCC VOmax=VCC VOLmax=0.4V VOLmin= 0V	
SDA1	IO	dead reckoning I²C bus data (SDA)	VOHmin=0.75*VCC VOmax=VCC VOLmax=0.4V VOLmin= 0V	
EINT0	I	Provides an interrupt on either high or low logic level or edge-sensitive interrupt	VIHmin=0.7*VCC VIHmax=3.6V VILmax=0.45V VILmin= -0.4V	
TIMEMARK	O	Time Mark output timing pulse related to receiver time, GPS time or UTC time	VOHmin=0.75*VCC VOmax=VCC VOLmax=0.4V VOLmin= 0V	
RF Input				
RF_IN	I	GPS Signal input		

3.2 Power management

3.2.1 Power Input

SIM18 has two power input pins: VCC and VRTC. VCC is the main power input pin, VRTC is the backup battery input, and both of these two pins are in 1.8V voltage domain. VRTC should be powered all the time when the module is running, while VCC can be removed when the module is in KA mode.

For fastest possible TTFF, the two power supply should be kept active all the time in order to keep the non-volatile RTC & RAM active. First power up may take 300ms typical due to internal RTC startup time (which may increase up to 5 seconds at cold temperature) after which the module will enter to sleep mode. The host may try to wakeup the module via successive ON_OFF interrupts sent every second until the host port messages are outputted and/or WAKEUP output is at high state.

When power supplies are intended to be removed, it is suggested that prior power removal a serial message in binary (MID 205 *ref II*) or NMEA format ($PSRF117,16*0B<CR><LF>) is sent to the module to shut down firmware operations orderly. Otherwise e.g. external EEPROM may get corrupted if power down happens in the middle of EEPROM writing, which may increase in TTFF. If external EEPROM is also used for ROM patch code, the abrupt power removal may cause patch code corruption that may end to system failure.

Second option for orderly shutdown is to send ON_OFF interrupt prior power supply removal. Operations shutdown may take anything between 10 to 900 ms depending upon operation in progress and messages pending

and hence is dependent upon serial interface speed and host port type.

If it is likely that all of the two power supplies will be removed abruptly, suggestion is to add external voltage monitor to detect under voltage condition below 5% nominal supply voltage and to drive RESET_N signal to reset condition (low state). This is important especially when external EEPROM or data storage at host is used. Power supply off-time is suggested to be over 10 seconds to next power up in order to clear all internal backup RAM content and to minimize risk for wrong backup data.

By-pass the VCC and VRTC supply input by a low ESR ceramic de-coupling capacitor (e.g. 2.2 uF) placed nearby VCC and VRTC pin to ensure low ripple voltage . Ensure that all of the two supplies input ripple voltage is low enough: 54 mV(RMS) max @ f = 0… 3MHz and 15 mV(RMS) max @ f > 3 MHz.

3.2.2 Power management system modes

The SIM18 module supports also SiRF operating modes for reduced average power consumption (*ref II*) like Adaptive TricklePower™, Advanced Power Management, Push-to-Fix™ and SiRFAware™ modes:

1. *Adaptive TricklePower (ATP):* In this mode the receiver stays at Full on power state for 200… 900ms and provides a valid fix. Between fixes with 1… 10 sec interval the receiver stays in sleep mode. ATP mode is configurable with SiRF binary protocol message ID151 (*ref II*). The receiver stays once in while in Full on power mode automatically (typical every 1800 sec) to receive new ephemeris data from rising satellites or if the received signal levels drop below certain level.

2. *Advanced Power Management (APM)*: APM allows power savings while ensuring that the quality of the solution is maintained when signal levels drop. APM does not engage until all necessary information is received. Host can configure e.g. number of APM cycles (continuous or up to 255), time between fixes (10… 180 sec), Power duty cycle (5…100%) and max position error. Rest of the time the receiver stays in Sleep mode. This mode is configurable with SiRF binary protocol message ID53 (*ref II*).

3. *Push-to-Fix (PTF)*: In this mode the receiver is configured to wake up periodically, typically every 1800 sec (configurable range 10… 7200 sec), for position update and to collect new ephemeris data from rising satellites. Rest of the time the receiver stays in Sleep mode. When position update is needed, the host can wake up the receiver by ON_OFF control input interrupt (pulse low-high-low >90us after which the receiver performs either Snap or Hot start and a valid fix is available within 1… 8 seconds typically. This mode is configurable with SiRF binary protocol message ID151 & 167 (*ref II*).

4. *SiRFAware (Micro Power Management* mode*, MPM)*: In this mode the receiver is configured to wake up periodically for 18 seconds, typically every 1800 seconds, to collect new ephemeris data from rising satellites, and also every 60 seconds for 250 ms to calibrate internal navigation state and GPS time estimate. Rest of the time the receiver stays in Sleep mode and module achieves 0.5 mA typical. average current drain. The host wakes up the receiver by ON_OFF control input interrupt (pulse low-high-low >90us) to *Full on* power mode after which the receiver performs Snap start and a valid fix is available within 1 second typically. After valid fix, operation can return back to *Micro Power Management* mode by re-sending the configuration binary message from the host. This mode is configurable with SiRF OSP (One Socket Protocol) binary protocol message MID218 (*ref II*).
These power management modes are also configurable with SiRF OSP binary protocol message MID 218, Power

Mode Request (*ref II*).
Note that position accuracy is somewhat degraded in power management modes when compared to full power operation.

3.2.3 Operating mode

Table 4: Power supply and clock state according to operation mode:

MODE	VRTC	VCC	Main clock	RTC clock
Full on	on	on	on	on
Sleep	on	on	off	on
KA	on	off	off	on

3.2.3.1 Full on mode

The module will enter sleep mode after first power up with factory configuration settings. The Navigation mode will start after waking up from sleep mode in cold start mode by sending ON_OFF signal interrupt pulse from host. Power consumption will vary depending on the amount of satellite acquisitions and number of satellites in track. This mode is also referenced as Full on, Full Power or Navigation mode.
Navigation is available and any configuration settings are valid as long as the VCC and VRTC power supplies are both active. When the power supply is off, settings are reset to factory configuration and receiver performs a cold start on next power up.
The power supply is intended to be kept active all the time and navigation activity is suggested to be controlled to low quiescent sleep mode via ON_OFF control input

3.2.3.2 Sleep mode

Sleep mode means a low quiescent (20uA typ.) power state where only the internal I/O Keep Alive, non-volatile RTC, patch RAM and backup RAM block is powered on. Other internal blocks like digital baseband and RF are internally powered off. The power supply input VCC and VRTC shall be kept active all the time, even during sleep mode. Waking up from and entering into sleep mode is controlled by host interrupt at ON_OFF control input (rising edge toggle low-high-low>90us).
During sleep mode the I/O Keep Alive is still active, thus I/O signals keep respective states except TX and RX signals, which are configured to high input impedance state.

3.2.3.3 KA mode

KA mode means keep alive only mode. In this mode, VCC is removed, only VRTC is alive, RTC and FSM is on, some IO's state is uncertain, the power consumption may rise to 600uA.

3.2.4 ON_OFF

An interrupt on the ON_OFF input line can control the SIM18 module going into or waking up from sleep mode. When the module is powered, it will going into sleep mode, then an ON_OFF interrupt will lead the module into full-on mode; or when the module is in full-on mode, a same interrupt will make the module go into sleep mode. The ON_OFF interrupt is generated by rising edge of a low-high-low pulse, which should be longer than 90us and less than 1s (suggestion is abt. 100ms pulse length). Do not generate ON_OFF interrupts less than 1 sec intervals. Especially take care that any multiple switch bounce pulses are filtered out.

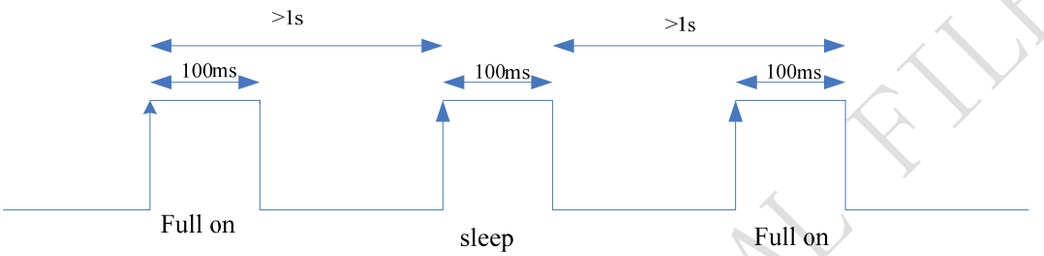

Figure 3: ON_OFF timing

3.2.5 WAKEUP

Wakeup is an output pin which can indicate the SIM18 module's state. When in full-on mode, the SIM18 module will pull up the WAKEUP pin, while in sleep or KA mode, the WAKEUP pin will be pulled low. So the host can verify the module's mode by reading this pin's state.

3.2.6 nRESET

The nRESET pin is an optional, external, emergency reset. It is only for use in the event of a malfunction. The internal POR that occurs when VRTC is applied is the preferred system reset method. When power supply may be abruptly removed, suggestion is to use externally generated reset by means of external voltage monitor or connect this pin to a GPIO of host to control the module.
When nRESET signal is used, it will force volatile RAM data loss (e.g. ROM patch code). Non-Volatile Backup RAM content is not cleared and thus fast TTFF is possible after reset. The input has internal pull up resistor and leave it not connected (floating) if not used.

3.2.7 VCC_ANT, VCC_RF

VCC_RF is a 1.8V output for external active antenna, if the external active antenna works at 1.8V voltage supply domain, the user can tie the VCC_RF and VCC_ANT directly. If the antenna's power is not 1.8V, the pin VCC_ANT should be provided a proper voltage depending on the active antenna, and the pin VCC_RF should be kept open. For passive antennas, both the pin VCC_RF and the pin VCC_ANT should be open.

3.3 Host Interface

User can select the host port configuration between UART, SPI (slave) and I2C (master/slave) during power up boot.
Table 5 shows these 3 alternative ports are multiplexed on a shared set of pins.

Table 5: Host Port Multiplexed Function Pins

PIN name	Pin number	Host interface		
		UART	Slave SPI	I^2C
TXD/MISO/SCL2	21	data transmit	slave SPI data output (MISO)	I^2C bus clock (SCL)
RXD/MOSI/SDA2	20	data receive	slave SPI data output (MOSI)	I²C bus data (SDA)
CTS/CLK	24	clear to send active low	slave SPI clock input (CLK)	
RTS/CS	23	ready to send active low	slave SPI chip select (CS#) active low	

At system reset, the host port pins are disabled so no port conflict occurs. The user can configure the multiplexed ports by pulling up or pulling down the CTS/CLK and RTS/CS. Table 6 shows the pin strapping information for selecting the host port interface type.

Table 6:Host Port Type Selection

Port type	CTS/CLK	RTS/CS
SPI(default)	0	1
UART	1 (Add a pull-up 10kΩ resistor.)	1
I²C	0	0 (Add a pull-down)

The port selection is not intended to be changed dynamically but only set once at power up.

3.3.1 UART

This UART is used for GPS data reports and receiver control. At boot up, the software uses different default baud rates depending on the protocol selected, in OSP mode it is 115200 baud and in NMEA mode it is 4800 baud. The protocol (OSP or NMEA) and/or the communication parameters (Baud rate, data bits, stop bits, and parity) can be configured by NMEA $PSRF100 message, while operation at speeds below 38400 carries risk of dropped messages when using SGEE (Server Generated Extended Ephemeris).

3.3.2 Slave SPI

The host interface SPI is a slave mode SPI:

- Supports both SPI and Microwire formats
- An interrupt is provided when the transmit FIFO and output serial register (SR) are both empty
- The transmitter and receiver each have independent 1024B FIFO buffers
  The transmitter and receiver have individual software-defined 2-byte idle patterns of 0xa7 0xb4
- SPI detects synchronization errors and is reset by software
- Supports a maximum clock of 6.8MHz

As a 4-wire slave mode SPI port, the I/O pins are located in the KA domain so byte sync is maintained while the main core is off and the slave SPI module is not powered and / or clocked.
The maximum clock rate permitted on the CLK pin from the external master is determined by the source clock of the slave SPI module. The source clock must be 8x the rate on the CLK pin from the master. The highest possible rate on the CLK pin is 6.840320MHz.

3.3.3 I²C Interface

The I²C host port interface supports:

- Operation up to 400kbps
- Individual transmit and receive FIFO lengths of 64B
- The default I^2C address values are:
- Rx: 0x60
- Tx: 0x62
- Multi-master I²C mode is supported by default.

Notes: When host port is configured to I²C bus, require external pull-up resistors at both signals.

3.4 Master mode dead reckoning (DR) I²C Bus

The SCL1 and SDA1 are the DR I²C bus pins, can be optionally connected to a 1 Mbit EEPROM for Client Generated Extended Ephemeris (CGEE) data storage (see Chapter 3.4.1 and 3.4.2) or be optionally connected to dead reckoning sensors such as gyros, accelerometers, compasses or other sensors that can operate with an I²C bus.
DR I²C interface supports:

- Common sensor formats (TBD devices)
- Typical data lengths (command + in/data out) of several bytes
- Standard I²C bus maximum data rate 400kbps
- Minimum data rate 100kbps

NOTE: the SCL1 and SDA1 pins are both pseudo open-drain and require pull-up resistors on the external bus, when be connected to DR sensor, the EINT0 can be used as the sensor's interrupt input to SIM18.

3.4.1 Self-Assistance - Client Generated EE usage

The SIM18 module supports Client Generated Extended Ephemeris (CGEE), which allows fast TTFF 10 sec typically for 3 days. The CGEE data is generated internally from satellite ephemeris as a background task and thus host should allow the SIM18 to navigate and to collect ephemeris from as many satellites as possible before entering Sleep mode. The CGEE feature requires that power supply is kept active all the time and that an external 1Mbit EEPROM connected to DR I^2C bus for CGEE data storage. A command is also required from host to enable EE storage to EEPROM ($PSRF120,F,R*30<CR><LF> or OSP binary message ID 232, Sub ID 253 (*ref II*)). The CGEE data can be also stored optionally to host (contact SIMCom support for availability and details).

3.4.2 Patching ROM Firmware

The firmware that is associated with SIM18 is executed for internal ROM memory. It is a normal practice that firmware patches may be provided from time to time in order to address ROM firmware issues as a method of implementing bug fixes. Patch can be stored on external EEPROM at DR I^2C bus or at host.

Patch firmware (max. size 24 kB) and downloading tools are available Contact SIMCom support for suggested procedure.

Note: power down will clear internal patch RAM and thus after power up the patch must be up either re-loaded from host or re-issued from external EEPROM by two binary OSP messages sent from host.

3.5 Timemark output

The Timemark pin outputs pulse-per-second (1PPS) pulse signal for precise timing purposes. Pulse high level is 200ms about 1us accuracy synchronized at rising edge to full UTC second.

3.6 GPS Antenna

3.6.1 Antenna Interface

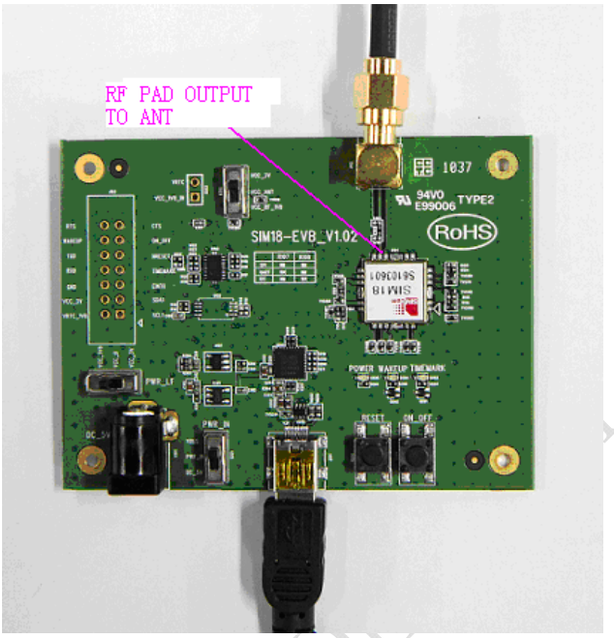

Figure 4: Antenna Interface

The RF interface has an impedance of 50Ω. The trace from RF PAD to antenna should also be 50Ω. To suit the physical design of individual applications the RF interface pad can lead to three alternatives:

- Recommended approach: solderable RF coaxial cable assembly antenna connector, such as HRS' U.FL-R-SMT(10) connector or I-PEX's 20279-001E-01 RF connector.
- SMA connector, such as the example shown in the photo above.
- PCB Antenna

3.6.2 GPS Antenna Choice Consideration

To obtain excellent GPS reception performance, a good antenna will always be required. The antenna is the most critical item for successful GPS reception in a weak signal environment. Proper choice and placement of the antenna will ensure that satellites at all elevations can be seen, and therefore, accurate fix measurements are obtained.

Most customers contract with antenna design houses to properly measure the radiation pattern of the final mounted configuration in a plastic housing with associated components near the antenna. Linear antennas are becoming more popular, and the gain is reasonable, since a smaller ground plane can be used.

We can consider these factors as following:

- Choose a linear antenna with a reasonably uniform hemispherical gain pattern of >-4dBi..
- Use of an antenna with lower gain than this will give less than desirable results. Please note that a RHCP antenna with a gain of 3dBi, equates to a linear polarized antenna of 0dBi.
- Proper ground plane sizing is a critical consideration for small GPS antennas.
- Proper placement of the GPS antenna should always be the FIRST consideration in integrating the SIM18 GPS Module.

If the customer's design will allow for a ceramic RHCP patch antenna with an appropriately sized ground plane, and the patch is normally oriented towards the sky, then that particular solution usually works the best. Please note that if the patch antenna ground plane is less than 60x60mm, then compromises to the beam width and gain pattern could result. Usually the gain becomes very directional, and looses several dB of performance. Since results can vary, measuring the antenna radiation pattern in the final housing in an appropriate anechoic chamber will be required.

Some customers do not have the size availability to implement a patch antenna approach. In that instance, use of a Linear Polarized (LP) antenna is the next best alternative. There are new ceramic LP antennas on the market that exhibit reasonable gain characteristics once properly mounted in the housing, and when matched to an appropriate sized ground. Generally the ground plane requirements are smaller for a LP antenna when compared to a patch, but once again, proper testing in an anechoic chamber is a mandatory requirement. These ceramic elements will need to be located near the end of the ground plane, and will require several mm of clearance between the closest component. It is important to note that use of a LP antenna will result in a minimum of 3dB of gain loss when compared to a RHCP antenna at a defined elevation. This is due to the right hand gain rule of antenna propagation.

Use of PIFA antenna is another LP possibility, but the PIFA usually exhibits a considerable amount of gain nulls, or "holes" in the radiation pattern. This will be undesirable for obtaining a low circular error probability (CEP), since the antenna may not allow the receiver to capture the desired satellite at the ideal orientation due to these noted gain nulls. Once again, careful testing in an appropriate anechoic chamber is required.

If the customer's design is for automotive applications, then an active antenna can be used and located on top of the car in order for guarantee the best signal quality. GPS antenna choice should base on the designing product and other conditions.

For detailed Antenna designing consideration, please refer to related antenna vendor's design recommendation. The antenna vendor will offer further technical support and tune their antenna characteristic to achieve successful GPS reception performance depending on the customer's design.

4 Electrical, Reliability and Radio Characteristics

4.1 Absolute Maximum Ratings

The absolute maximum ratings stated in Table 7 are stress ratings under non-operating conditions. Stresses beyond any of these limits will cause permanent damage to SIM18.

Table 7: Absolute maximum ratings

Parameter	Min	Max	Unit
VCC	-	2.2	V
VRTC	-	2.2	V
RF pin voltage	-	2.2	V
I/O pin voltage	-	3.6	V
Storage temperature	-	150	℃

4.2 Recommended Operating Conditions

Table 8: SIM18 operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating temperature range		-40	+25	+85	℃
Main supply voltage	VCC	1.71	1.8	1.89	V
Backup battery voltage	VRTC	1.71	1.8	1.89	V
Active antenna supply voltage	VCC_RF	1.71	1.8	1.89	V

4.3 Electro-Static Discharge

The GPS engine is not protected against Electrostatic Discharge (ESD) in general. Therefore, it is subject to ESD handing precautions that typically apply to ESD sensitive components. Proper ESD handing and packaging procedures must be applied throughout the processing, handing and operation of any application using a SIM18 module.

5 Mechanics

This chapter describes the mechanical dimensions of SIM18 and provides pad layout.

5.1 Mechanical Dimensions of SIM18

Following shows the Mechanical dimensions of SIM18 (top view, side view and bottom view).

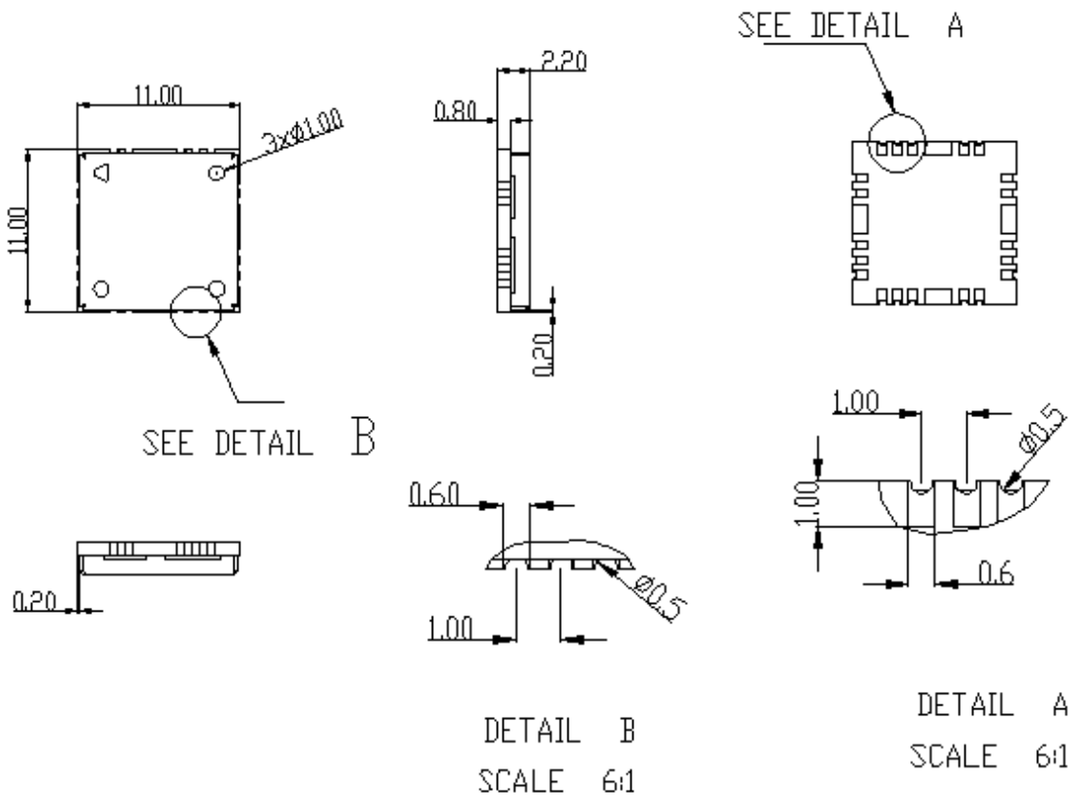

Figure 5: Mechanical dimensions of module （Unit: mm）

5.2 SIM18 recommended PCB decal

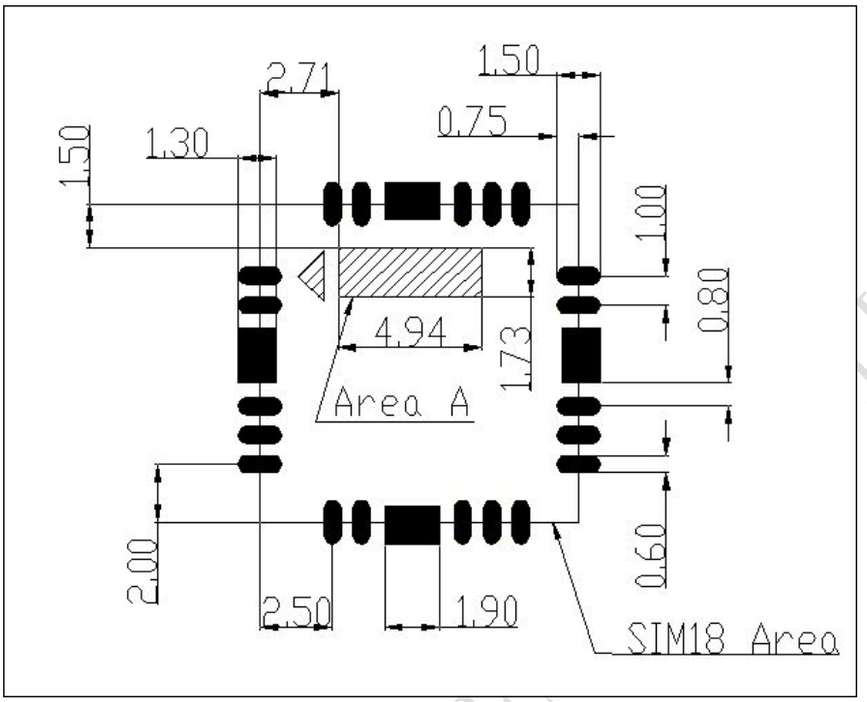

Figure 6：Recommended PCB decal（Unit: mm）

In the figure, "Area A" is the copper ground on the bottom side of SIM18

5.3 SIM18 recommended PCB paste

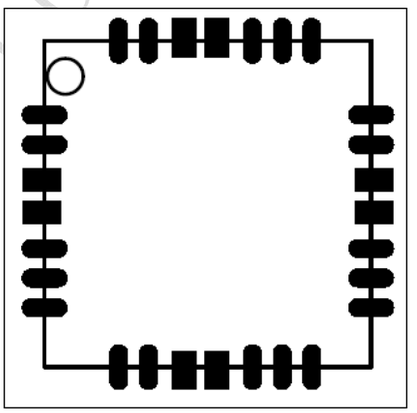

Figure 7：Recommended PCB paste

Note:

1) ***The area under SIM18 should be dedicated to keep-out to both traces and ground plane (copper plane), except for via holes, which can be placed close to the pad under the module. If possible, the amount of VIA holes underneath the module should be minimized.***
2) ***Because the large pad area of four GNDs, their pastes are divided into 2 parts.***

5. 4 Top and Bottom View of the SIM18

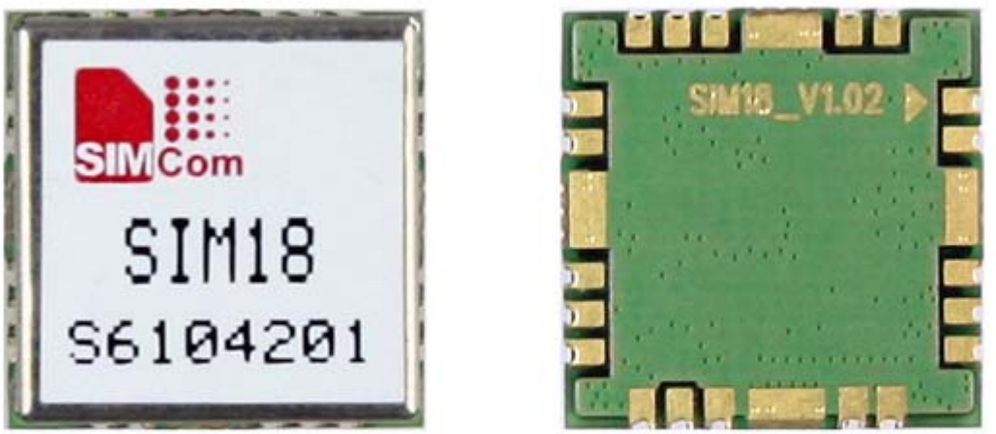

Figure 8: Top and Bottom view of the SIM18

6 Manufacturing

6.1 Assembly and soldering

The SIM18 module is intended for SMT assembly and soldering in a Pb-free reflow process on the top side of the PCB. Suggested solder paste stencil height is 150um minimum to ensure sufficient solder volume. If required paste mask pad openings can be increased to ensure proper soldering and solder wetting over pads.
The following figure is the Ramp-Soak-Spike Reflow Profile of SIM18:

Figure 9: the Ramp-Soak-Spike Reflow Profile of SIM18

SIM18 modules are Moisture Sensitive Devices (MSD), appropriate MSD handling instruction and precautions are summarized in Chapter 6.2.
SIM18 modules are also Electrostatic Sensitive Devices (ESD), handling SIM18 modules without proper ESD protection may destroy or damage them permanently, see Chapter 6.3
Avoid also ultrasonic exposure due to internal crystal and SAW components.

6.2 Moisture sensitivity

SIM18 module is moisture sensitive at MSL level 3, dry packed according to IPC/JEDEC specification J-STD-020C. The calculated shelf life for dry packed SMD packages is a minimum of 12 months from the bag seal date, when stored in a non condensing atmospheric environment of <40°C/90% RH.

Table 9 lists floor life for different MSL levels in the IPC/JDEC specification:

Table 9: Moisture Classification Level and Floor Life

Level	Floor Life(out of bag)at factory ambient≦30℃/60%RH or as stated
1	Unlimited at ≦30℃/85% RH
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.

Factory floor life is 1 week for MSL 3, SIM18 must be processed and soldered within the time. If this time is exceeded, or the humidity indicator card in the sealed package indicates that they have been exposed to moisture, the devices need to be pre-baked before the reflow solder process.

Both encapsulate and substrate materials absorb moisture. IPC/JEDEC specification J-STD-020 must be observed to prevent cracking and delamination associated with the "popcorn" effect during reflow soldering. The popcorn effect can be described as miniature explosions of evaporating moisture. Baking before processing is required in the following cases:

- Humidity indicator card: At least one circular indicator is no longer blue
- Floor life or environmental requirements after opening the seal have been exceeded, e.g. exposure to excessive seasonal humidity.

Refer to Section 4 of IPC/JEDEC J-STD-033 for recommended baking procedures.

Notes:

Oxidation Risk: Baking SMD packages may cause oxidation and/or inter metallic growth of the terminations, which if excessive can result in solder ability problems during board assembly. The temperature and time for baking SMD packages are therefore limited by solder ability considerations. The cumulative bake time at a temperature greater than 90°C and up to 125°C shall not exceed 96 hours. If the bake temperature is not

6.3 ESD handling precautions

SIM18 modules are Electrostatic Sensitive Devices (ESD). Observe precautions for handling!
Failure to observe these precautions can result in severe damage to the GPS receiver!

GPS receivers are Electrostatic Sensitive Devices (ESD) and require special precautions when handling. Particular care must be exercised when handling patch antennas, due to the risk of electrostatic charges. In addition to standard ESD safety practices, the following measures should be taken into account whenever handling the receiver:

- Unless there is a galvanic coupling between the local GND (i.e. the work Table) and the PCB GND, then the first point of contact when handling the PCB shall always be between the local GND and PCB GND.
- Before mounting an antenna patch, connect ground of the device

- When handling the RF pin, do not come into contact with any charged capacitors and be careful when contacting materials that can develop charges (e.g. patch antenna ~10pF, coax cable ~50-80pF/m, soldering iron, …)
- To prevent electrostatic discharge through the RF input, do not touch the mounted patch antenna.
- When soldering RF connectors and patch antennas to the receiver's RF pin, make sure to use an ESD safe soldering iron (tip).

6.4 Shipment

SIM18 is designed and packaged to be processed in an automatic assembly line, now packaged in SIM18 tray.

6.5 PIN Assignment of SIM18

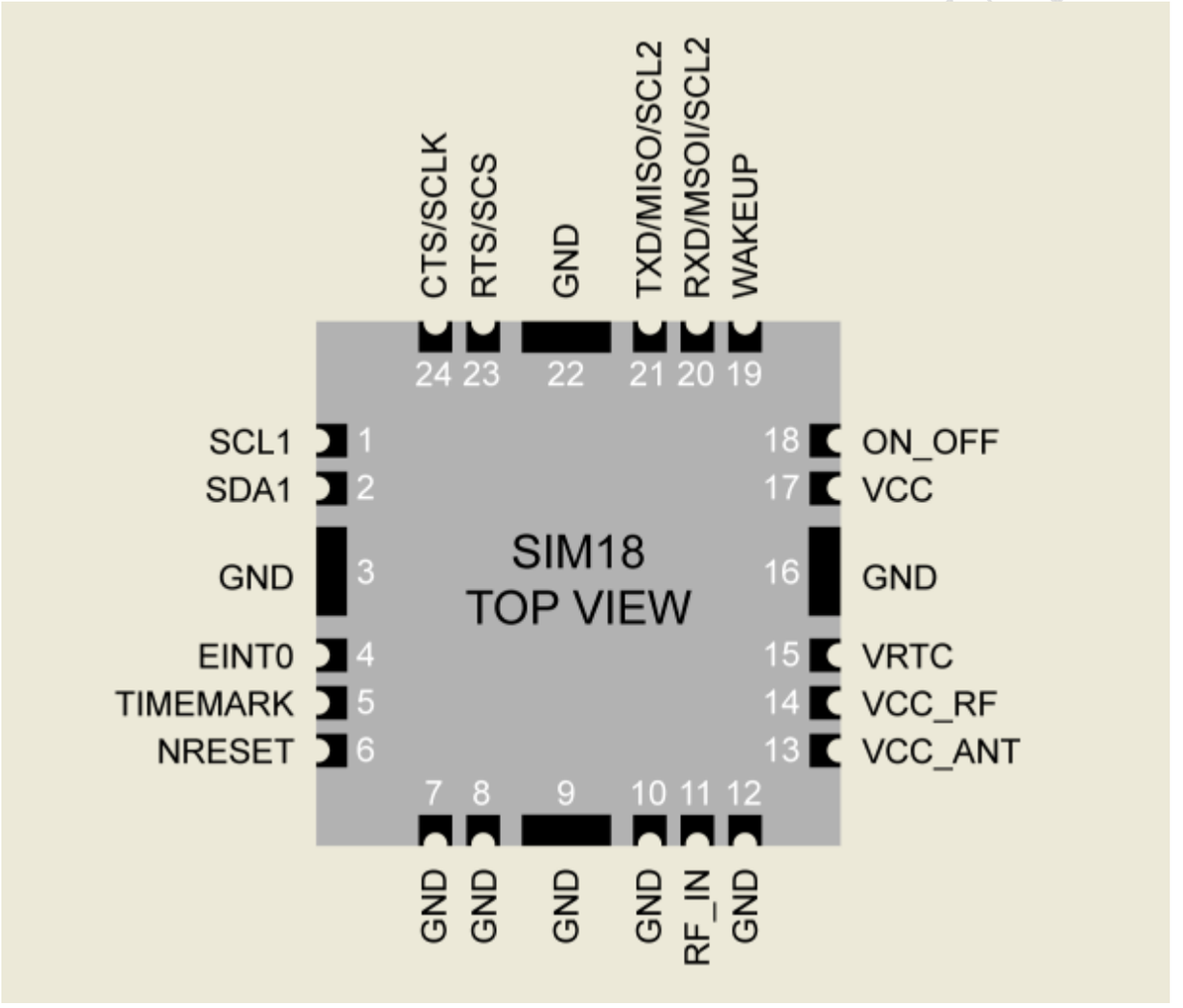

Figure 10: PIN assignment

6.6 Example Application Schematic

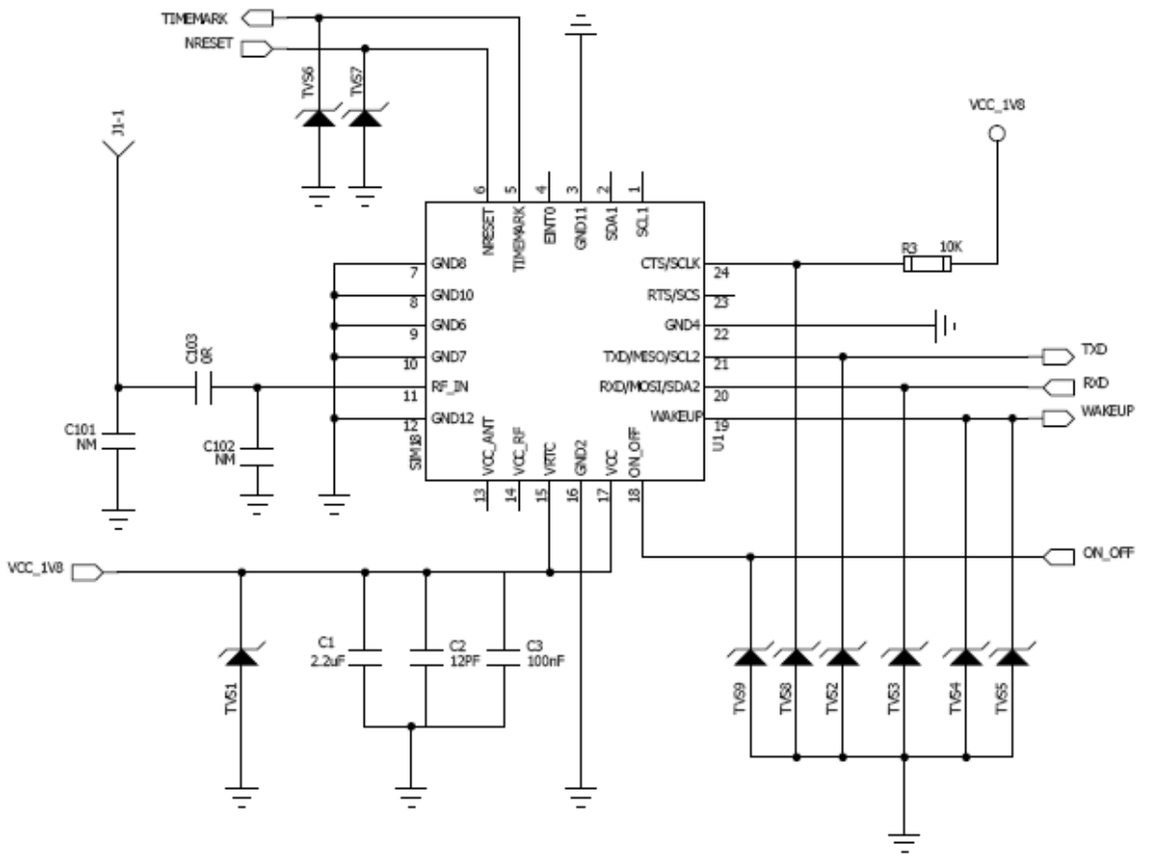

Figure 11: Example Application Schematic with UART and single power supply

Notes:

1) ***The pin VCC_RF provides a 1.8V output level for external active antenna.***
   For active antenna, if antenna's power domain is 1.8V, the pin VCC_RF could connect to the pin VCC_ANT directly. If the antenna's power is not 1.8v, keep the pin VCC_RF open and supply the pin VCC_ANT proper voltage depending on the active antenna.
   For passive antenna, the pin VCC_RF and the pin VCC_ANT should be kept open.
2) ***All I/O signal levels are CMOS 1.8V compatible and inputs are 3.6V tolerable. For when SIM18 working in 3V domain, level shift components are needed for output pins.***
3) ***The maximum input ripple of VCC and VRTC are as follows:***

Table 10: Maximum allowable ripple

Rail	*Frequency range*	*Allowable ripple*
VCC,VRTC	*0~3MHZ*	*54mV*
	>3MHZ	*15mV*

6.7 Special Notes

If customers using SIM18-Z01without patching ROM firmware, the nRESET, ON_OFF and TIMEMARK on SIM18-Z01 perform differently, described as follows:

- nRESET is defined to control SIM18 going into sleep mode.
- ON_OFF is defined to wake up the SIM18 module from sleep mode only. Besides patching ROM firmware, nRESET can be used to control SIM18 going to sleep mode.
- TIMEMARK does not support 1PPS (1 pulse-per-second), it outputs high level after SIM18 firstly going to full on mode. If 1PPS is needed, patching ROM firmware is needed.

SIM18-Z01 has been verified carefully, its GPS performance has been described in chapter 2.2.

The default firmware 2.0 will correct above definitions, and released in 2Q 2011. For the customers using SIM18-Z01, the only thing that they need to do is to re-define these pins in software, no change in hardware is needed.

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