Lab 02 - First Verilog

In this lab, you've learned how to do an initial and simple design in Verilog to learn the Vivado tooling and process involved in RTL/FPGA design.

Rubric

Item	Description	Value
Summary Answers	Your writings about what you learned in this lab.	25%
Question 1	Your answers to the question	25%
Question 2	Your answers to the question	25%
Question 3	Your answers to the question	25%

Lab Summary

- In this lab we were required to learn the basic processes, setup procedures, and navigation of the Vivado Software, and then used a prebuilt set of code to practice exporting to an external board for testing.

Lab Questions

1 - Describe the stages of building a Verilog project in Vivado.

- First: We were instructed to download the Vivado Software to either a Windows Pc, Windows or Linux VM, or to use the software exclusively on one of the Lab Computers.
- Second: We then downloaded the required files for this Lab 02, and then import them into Vivado during the introduction stage of the Lab. During this stage it guided us through how to set up a new project in Vivado, how to select and access the desired files, and then how to change and view components of each file.
- Third: We were instructed to play around with and write down what we expected/wanted to happen, when on the digital board when simulated.
- Fourth: Following our testing through the simulations, we were instructed to connect our physical boards to the computer we were using and then to "Generate Bitstream", which sent out code to the Physical Board (Baysys3). We were then able to Validate whether or not the code was functioning correctly, and then conclude the Lab 02.

2 - What is the value in looking at the elaborated design schematic?

- It is valuable to look into the elaborated design of a schematic, because it can help to give an idea about how the board will behave when given any specific simulation. This includes behaviors such as which LEDs have inputs and outputs, and whether the inputs are the ones which were specified, and whether the outputs are actually functioning as intended.

3 - Why should we simulate our designs frequently? What does the simulation do?

- It is important to simulate our code frequently because this allows us to view how our code functions after each and every change we make to the code. This ensures that we are able to know which change resulted in our code giving any error codes, and where to potentially fix it. When each change is made, we can also get a reading of the values of any specific variables we would like to pay attention to, rather than try and figure out which modification to the code resulted in an unexpected change to the value of these variables.

Code Submission

Upload a .zip of all your code or a public repository on GitHub.