CPE301 – SPRING 2019

Design Assignment 1B

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Primary Github address: https://github.com/portig1/submissions_E
Directory: submissions_E/DA/LAB1B/

Submit the following for all Labs:

1. In the document, for each task submit the modified or included code (only) with highlights and justifications of the modifications. Also, include the comments.
2. Use the previously create a Github repository with a random name (no CPE/301, Lastname, Firstname). Place all labs under the root folder ESD301/DA, sub-folder named LABXX, with one document and one video link file for each lab, place modified asm/c files named as LabXX-TYY.asm/c.
3. If multiple asm/c files or other libraries are used, create a folder LabXX-TYY and place these files inside the folder.
4. The folder should have a) Word document (see template), b) source code file(s) and other include files, c) text file with youtube video links (see template).

1. COMPONENTS LIST AND CONNECTION BLOCK DIAGRAM w/ PINS

Atmel Studio 7

2. INITIAL/MODIFIED/DEVELOPED CODE OF TASK 1/A

```
;
; LAB1B.asm
;
; Created: 2/16/2019 1:06:49 PM
; Author : gausp
;


.include<m328pdef.inc>

.cseg
.org 0x00

.DEF ZERO = R10             ;Will be to add cary for the upper 8-bits of the sums
.DEF COUNTER = R25          ;R25 will be used as the counter
.DEF COPYVALUE = R20
.DEF NUM = R21              ;Defined variable for the division segment of code
.DEF DENOMINATOR = R22
.DEF QUOTIENT = R23

        CLR ZERO
        CLR R16             ;Clearing Registers R16:R19 since they will be used for the
sum results
        CLR R17
        CLR R18
        CLR R19
        LDI  COUNTER ,0x63        ;COUNTER = 99
        LDI  COPYVALUE,0x0A       ;R20 = 10(initial value to be copied), will be
incremented in till it is 109 but the last stored value will be 108

        LDI  XL,LOW(0x200)        ;load the low byte of X with value STARTADS = 0x0200
        LDI  XH,HIGH(0x200)       ;load the high byte of X with value STARTADS = 0x0200
        LDI  YL,LOW(0x400)        ;load the low byte of Y with 0x0400
        LDI  YH,HIGH(0x400)       ;load the high byte of Y with 0x0400
        LDI  ZL,LOW(0x600)        ;load the low byte of Z with  0x0600
        LDI  ZH,HIGH(0x600)       ;load the high byte of Z with 0x0600

L1:
      ST X+, COPYVALUE     ;Store R20 to memory location X
      MOV NUM, COPYVALUE   ;Copy R20 to NUM
      LDI DENOMINATOR, 3
      DIVLOOP1:
            INC QUOTIENT
            SUB NUM, DENOMINATOR
            BRCC DIVLOOP1
            DEC QUOTIENT
            ADD NUM, DENOMINATOR
      DIVCHECK:
```

```
            CPI NUM, 0
            BRNE NOTDIV3        ;If NUM = 0, R20 is divisible by 3 and will be stored
in Y
            ST Y+,COPYVALUE
            ADD R16, COPYVALUE  ;Adds value that's divisible by 3 to the appropriate
sum
            ADC R17, ZERO
            RJMP NEXT
      NOTDIV3:            ;Stores value of R20 at Z since it is not divisible by 3
            ST Z+, COPYVALUE
            ADD R18, COPYVALUE  ;Adds value that's not divisible by 3 to the
appropriate sum
            ADC R19, ZERO
      NEXT:
      INC COPYVALUE       ;Increment value to store
      DEC COUNTER         ;decrement the counter
      BRNE L1             ;loop until counter = zero

END: RJMP END
```

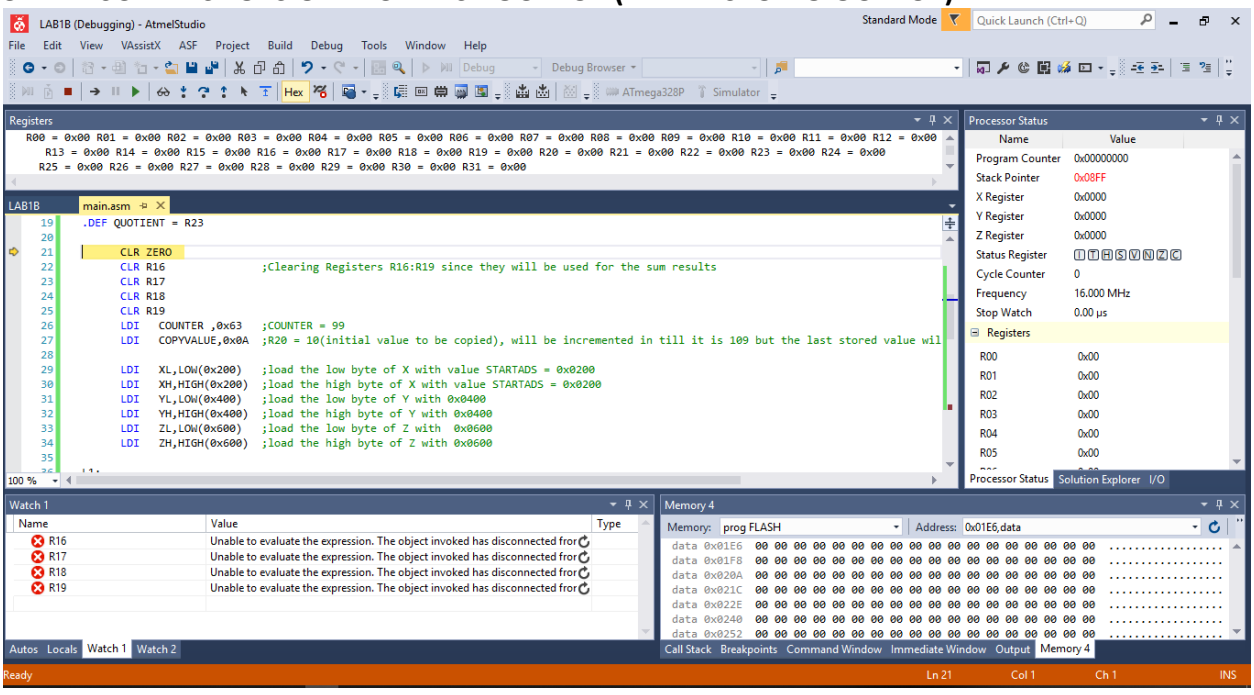
3. DEVELOPED MODIFIED CODE OF TASK 2/A from TASK 1/A

Verified results using google sheets @
https://docs.google.com/spreadsheets/d/131Yni3C4D0n44uFcH8fwElzPeHHAXc-zYhx5vDc3qxU/edit?usp=sharing

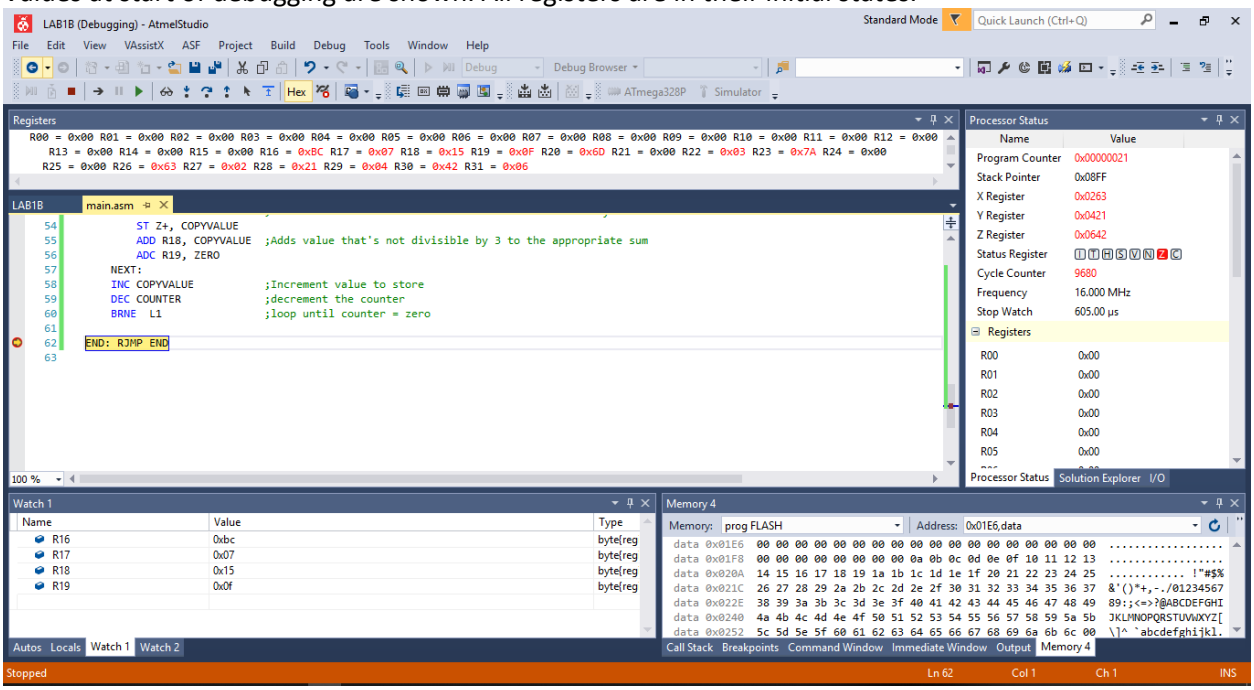
4. SCHEMATICS

No schematics

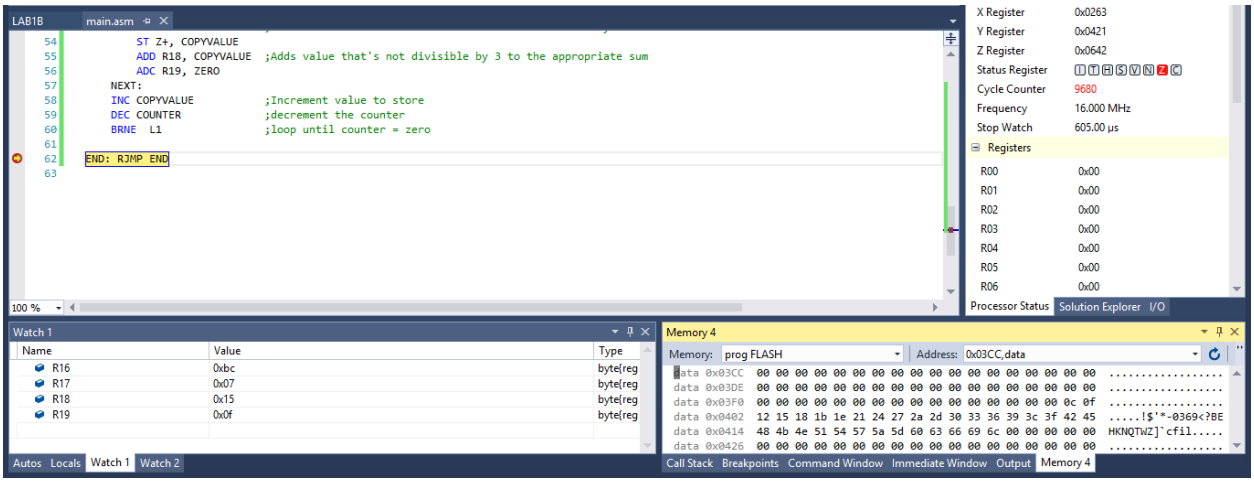
5. SCREENSHOTS OF EACH TASK OUTPUT (ATMEL STUDIO OUTPUT)



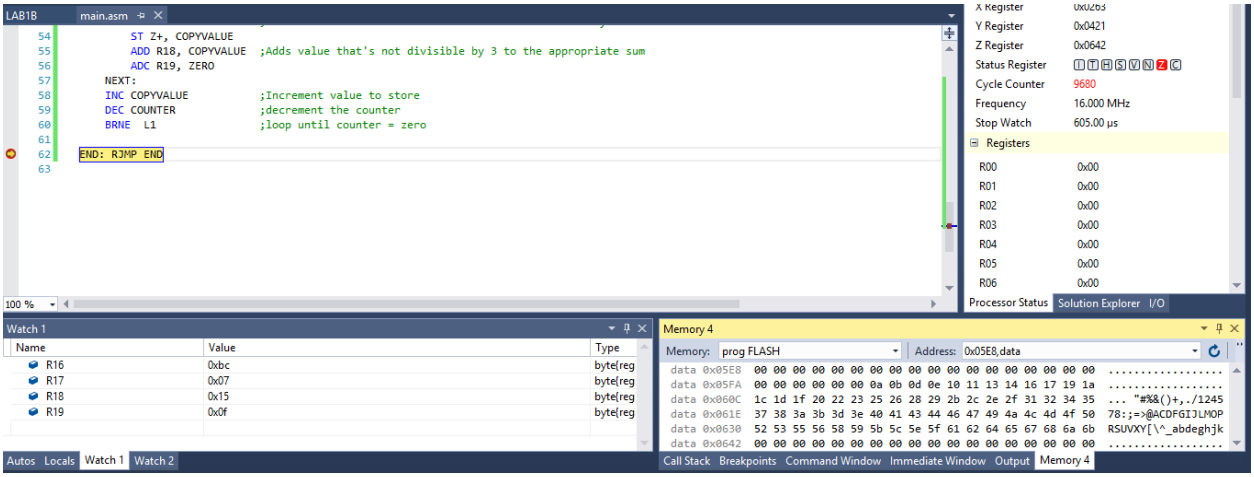
Values at start of debugging are shown. All registers are in their initial states.



The values stored for X are shown as well as the total clock cycles of 9680 @ 16MHz with a time of 605us.



Values stored for Y are shown in the lower right-hand corner.



Values stored for Y are shown in the lower-right hand corner.

6. SCREENSHOT OF EACH DEMO (BOARD SETUP)

7. VIDEO LINKS OF EACH DEMO

8. GITHUB LINK OF THIS DA

https://github.com/portig1/submissions_E/tree/master/DA/LAB1B

Student Academic Misconduct Policy

http://studentconduct.unlv.edu/misconduct/policy.html

"*This assignment submission is my own, original work*".

NAME OF THE STUDENT