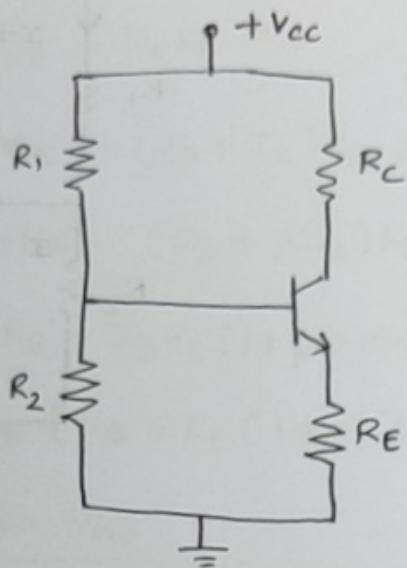
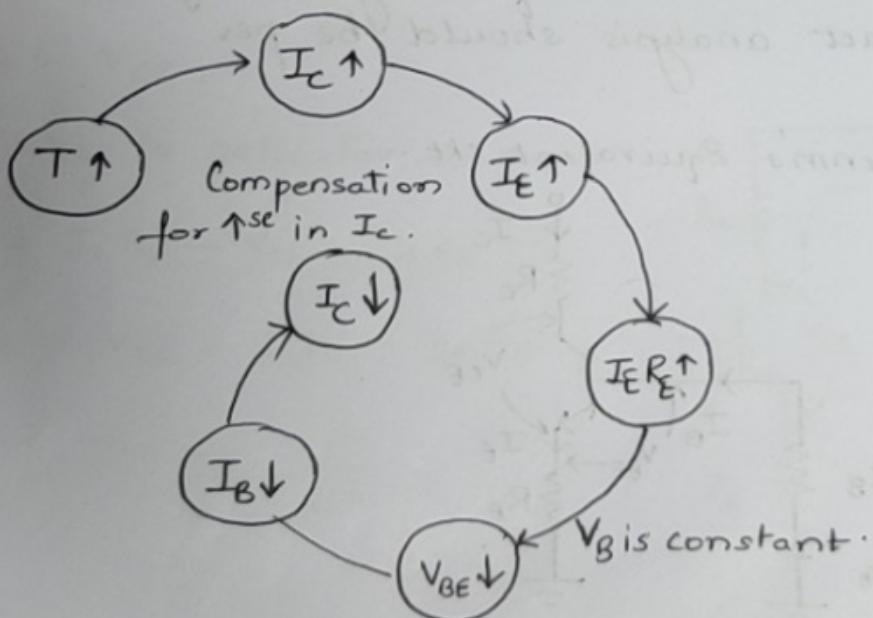


VOLTAGE DIVIDER BIAS :-



- ① This is the 3rd bias stabilizing ckt.
- ② R_1 & R_2 forms a potential divider to apply a fixed voltage V_B to the base.
- ③ R_E is connected at the emitter.



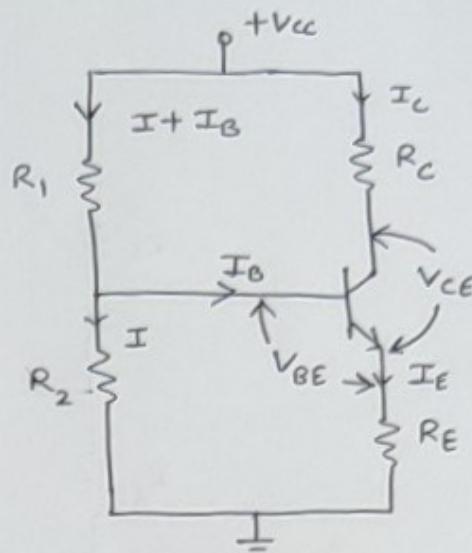
Approximate Analysis of Voltage Divider Bias :-

If $(I > I_B)$.

Step

Base Circuit :-

$$V_B = V_{R_2} = \frac{R_2}{R_1 + R_2} V_{cc}$$



Collector Circuit :-

$$V_E = I_E R_E = V_B - V_{BE}$$

$$I_E = \frac{V_E - V_{BE}}{R_E}$$

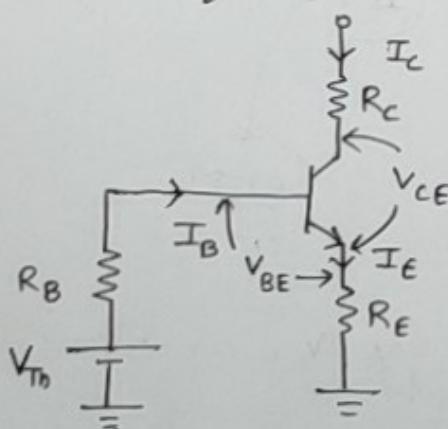
Apply KVL to the collector circuit.

$$V_{cc} = I_c R_c + V_{ce} + I_E R_E$$

$$V_{ce} = V_{cc} - I_c R_c - I_E R_E.$$

Exact Analysis of using Thvenin's Equivalent Circuit.
If $(I_B \ll I)$ is not satisfied by the self bias circuit
then the exact analysis should be per

Step 1:- Thvenin's equivalent ckt.



$$R_B = R_1 \parallel R_2 = \frac{R_1 \times R_2}{R_1 + R_2} = \frac{R_1 R_2}{R_1 + R_2}.$$

$$V_{th} = \frac{R_2}{R_1 + R_2} V_{cc}.$$

Step 2:- Obtain I_B :-

Apply KVL to base loop.

$$V_{Th} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$V_{Th} - I_B R_B - V_{BE} - (I_B + I_c) R_E = 0$$

$$V_{Th} - V_{BE} - I_B R_B - (I_B + \beta I_B) R_E = 0$$

$$V_{Th} - V_{BE} - I_B R_B - I_B R_E (1 + \beta) = 0$$

$$V_{Th} - V_{BE} - I_B [R_B + R_E (1 + \beta)] = 0$$

$$I_B = \frac{V_{Th} - V_{BE}}{R_B + R_E (1 + \beta)}$$

Step 3 :- I_c .

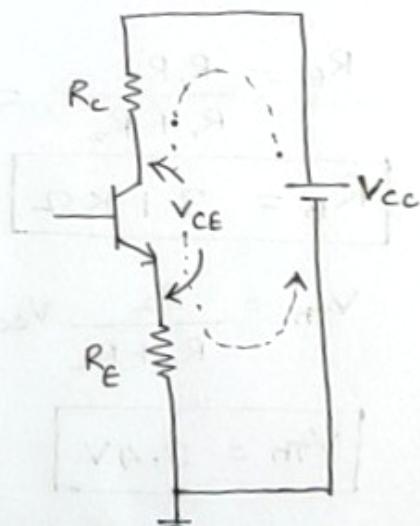
$$I_c = \beta I_B = \beta \left[\frac{V_{Th} - V_{BE}}{R_B + R_E (1 + \beta)} \right]$$

Step 4 :- V_{CE} .

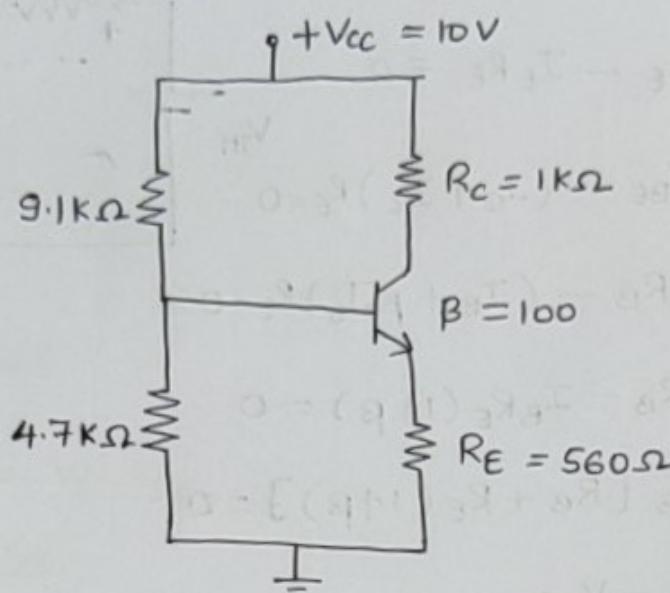
Apply KVL to collector loop.

$$V_{CC} - I_c R_C - V_{CE} - I_E R_E = 0$$

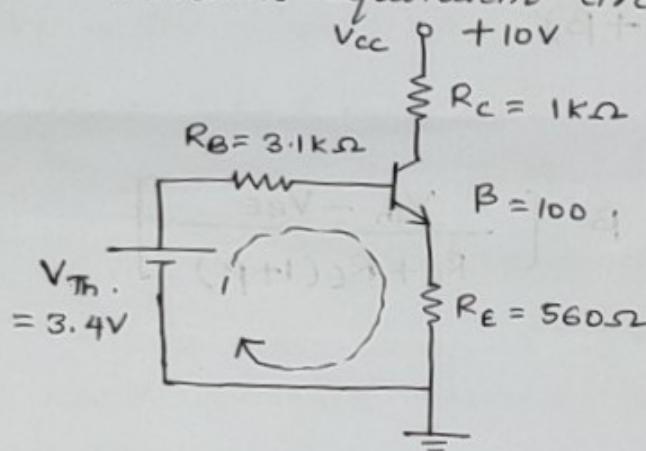
$$V_{CE} = V_{CC} - I_c R_C - I_E R_E$$



Q: Calculate the Q point values of I_C and V_{CE} for the voltage divider bias circuit shown. Assume that the transistor is a Si transistor with $\beta_{dc} = 100$.



Soln:- Step 1:- Thevenin's Equivalent Circuit.



$$R_B = \frac{R_1 R_2}{R_1 + R_2} = \frac{9.1 \times 10^3 \times 4.7 \times 10^3}{(9.1 \times 10^3) + (4.7 \times 10^3)} = 3.099 \times 10^3 \Omega$$

$$\boxed{R_B = 3.1 \text{ k}\Omega}$$

$$V_{Th} = \frac{R_2}{R_1 + R_2} V_{cc} = \frac{4.7 \times 10^3}{9.1 \times 10^3 + 4.7 \times 10^3} \times 10 = 3.4 \text{ V}$$

$$\boxed{V_{Th} = 3.4 \text{ V}}$$

Step 2:- I_B .

Apply KVL to base loop,

$$V_{Th} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$3.4 - I_B (3.1 \times 10^3) - 0.7 - (1 + \beta) I_B R_E = 0$$

$$I_B = \frac{3.4 - 0.7}{(3.1 \times 10^3) - (1 + 100)(560)} = 0.04525 \text{ mA}$$

$$I_B = 45.25 \mu A$$

Step 3 :- I_C

$$I_C = \beta I_B$$

$$I_C = 100 \times 45.25 \times 10^{-6}$$

$$I_C = 4.525 \times 10^{-3}$$

$$I_C = 4.525 \text{ mA}$$

Step 4 :- V_{CE}

Apply KVL to collector

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

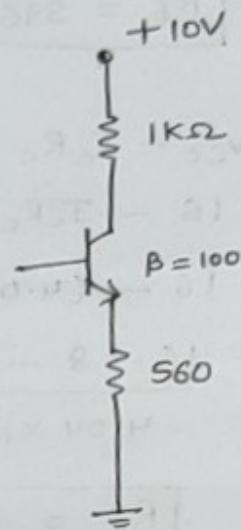
$$= V_{CC} - I_C R_C - (1 + \beta) I_B R_E$$

$$= 10 - (4.525 \times 10^3) \times 1 \times 10^3$$

$$- (1 + 100) \times 45.25 \times 10^6 \times 560$$

$$= 10 - 4.525 - 2.56$$

$$V_{CE} = 2.91 \text{ V}$$



Q) Design voltage divider bias circuit for the following specification.

$$V_{CC} = 16 \text{ V}$$

$$V_{CEQ} = 8 \text{ V}$$

$$I_{CQ} = 4 \text{ mA}$$

$$\beta = 100$$

Soln. $I_B = \frac{I_C}{\beta} = \frac{4 \times 10^{-3}}{100} = 40 \mu \text{A}$

$$I_B = 40 \mu \text{A}$$

$$V_E = 0.1 V_{CC}$$

$$= 0.1 \times 16$$

$$V_E = 1.6 \text{ V}$$

$$I_E = (1 + \beta) I_B$$

$$= (1 + 100) \times 40 \times 10^{-6}$$

$$= 101 \times 40 \times 10^{-6}$$

$$I_E = 4.04 \text{ mA}$$

$$V_E = I_E R_E$$

$$1.6 = 4.04 \times 10^{-3} \times R_E$$

$$R_E = \frac{1.6}{4.04 \times 10^{-3}} = 396 \Omega$$

$$R_E = 396 \Omega$$

$$V_{CC} - I_c R_c - V_{CE} - I_E R_E = 0$$

$$16 - I_c R_c - V_{CE} - V_E = 0$$

$$16 - (4.04 \times 10^{-3}) R_c - 8 - 1.6 = 0$$

$$\frac{16 - 8 - 1.6}{4.04 \times 10^{-3}} = R_c$$

$$R_c = 1.6 \text{ k}\Omega$$

$$V_B = V_E + V_{BE}$$

$$(\because V_{BE} = V_B - V_E)$$

$$V_B = 1.6 + 0.7$$

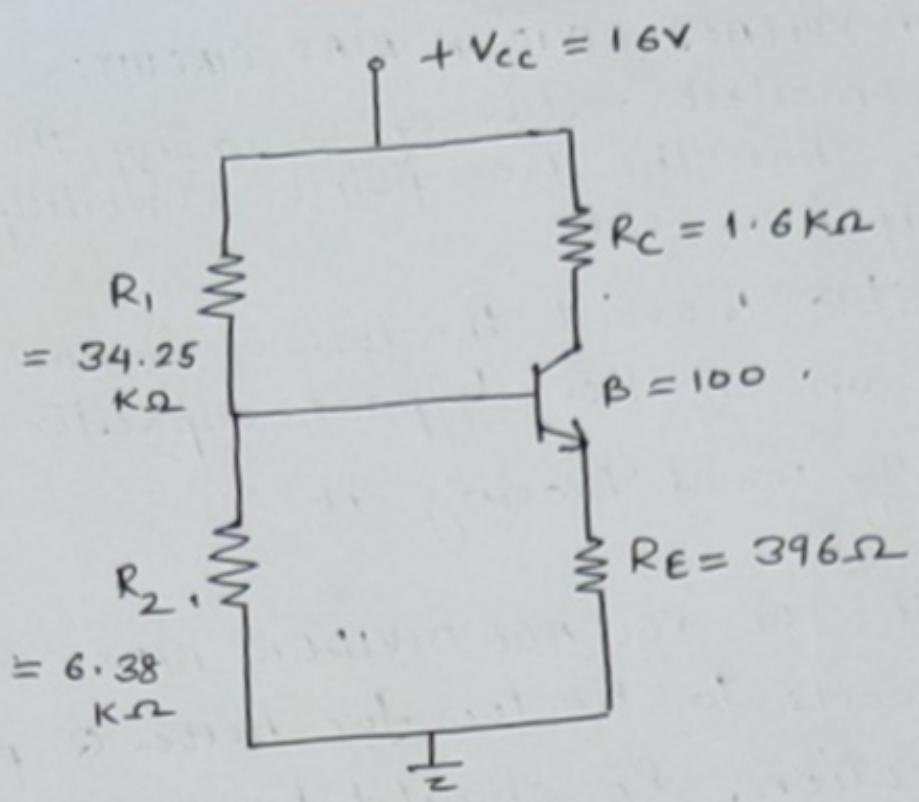
$$V_B = 2.3 \text{ V}$$

$$I_1 = 10 I_B = 10 \times 40 \times 10^{-6} = 400 \times 10^{-6} = 400 \mu\text{A}$$

$$I_2 = I_1 - I_B = 400 \times 10^{-6} - 40 \times 10^{-6} = 360 \mu\text{A}$$

$$R_2 = \frac{V_B}{I_2} = \frac{2.3}{360 \times 10^{-6}} = 6.38 \text{ k}\Omega //$$

$$R_1 = \frac{V_{CC} - V_B}{I_1} = \frac{16 - 2.3}{400 \times 10^{-6}} = 34.25 \text{ k}\Omega //$$



ADVANTAGES OF VOLTAGE DIVIDER BIAS CIRCUIT:-

- ① It has the smallest value of β among the β biasing ckt. This shows that the bias point stability is higher for the self bias ckt.

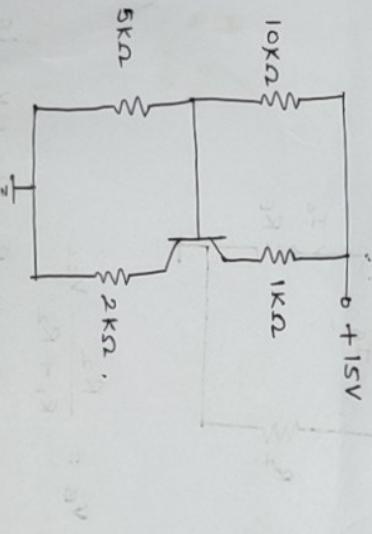
- ② It is possible to avoid the loss of signal gain by connecting an emitter bypass capacitor across R_E .
- ③ Most widely used biasing ckt.

DISADVANTAGES OF VOLTAGE DIVIDER BIAS CIRCUIT:-

- ① R_B / R_E needs to be low for better Q-point stabilization. R_E should be small and R_E should be high.
- ② Reduction in gain due to -ve feedback.

Numericals:-

- ① Fig shows the voltage divider bias method. Draw the dc load line and determine the operating point. Assume the transistor to be of Si.



Soln:-

$$V_{CE} =$$