

FET Biasing

CHAPTER OBJECTIVES

- Be able to perform a dc analysis of JFET, MOSFET, and MESFET networks.
- Become proficient in the use of load-line analysis to examine FET networks.
- Develop confidence in the dc analysis of networks with both FETs and BJTs.
- Understand how to use the Universal JFET Bias Curve to analyze the various FET configurations.

7.1 INTRODUCTION

In Chapter 4 we found that the biasing levels for a silicon transistor configuration can be obtained using the approximate characteristic equations $V_{BE} = 0.7$ V, $I_C = \beta I_B$, and $I_C \approx I_E$. The link between input and output variables is provided by β , which is assumed to be fixed in magnitude for the analysis to be performed. The fact that beta is a constant establishes a *linear* relationship between I_C and I_B . Doubling the value of I_B will double the level of I_C , and so on.

For the field-effect transistor, the relationship between input and output quantities is *nonlinear* due to the squared term in Shockley's equation. Linear relationships result in straight lines when plotted on a graph of one variable versus the other, whereas nonlinear functions result in curves as obtained for the transfer characteristics of a JFET. The nonlinear relationship between I_D and V_{GS} can complicate the mathematical approach to the dc analysis of FET configurations. A graphical approach may limit solutions to tenths-place accuracy, but it is a quicker method for most FET amplifiers. Since the graphical approach is in general the most popular, the analysis of this chapter will have graphical solutions rather than mathematical solutions.

Another distinct difference between the analysis of BJT and FET transistors is that:

The controlling variable for a BJT transistor is a current level, whereas for the FET a voltage is the controlling variable.

In both cases, however, the controlled variable on the output side is a current level that also defines the important voltage levels of the output circuit.

The general relationships that can be applied to the dc analysis of all FET amplifiers are

$$I_G \approx 0 \text{ A} \quad (7.1)$$

and

$$I_D = I_S \quad (7.2)$$

For JFETs and depletion-type MOSFETs and MESFETs, Shockley's equation is applied to relate the input and output quantities:

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2 \quad (7.3)$$

For enhancement-type MOSFETs and MESFETs, the following equation is applicable:

$$I_D = k(V_{GS} - V_T)^2 \quad (7.4)$$

It is particularly important to realize that all of the equations above are for the *field-effect transistor only!* They do not change with each network configuration so long as the device is in the active region. The network simply defines the level of current and voltage associated with the operating point through its own set of equations. In reality, the dc solution of BJT and FET networks is the solution of simultaneous equations established by the device and the network. The solution can be determined using a mathematical or graphical approach—a fact to be demonstrated by the first few networks to be analyzed. However, as noted earlier, the graphical approach is the most popular for FET networks and is employed in this book.

The first few sections of this chapter are limited to JFETs and the graphical approach to analysis. The depletion-type MOSFET will then be examined with its increased range of operating points, followed by the enhancement-type MOSFET. Finally, problems of a design nature are investigated to fully test the concepts and procedures introduced in the chapter.

7.2 FIXED-BIAS CONFIGURATION

The simplest of biasing arrangements for the *n*-channel JFET appears in Fig. 7.1. Referred to as the fixed-bias configuration, it is one of the few FET configurations that can be solved just as directly using either a mathematical or a graphical approach. Both methods are included in this section to demonstrate the difference between the two methods and also to establish the fact that the same solution can be obtained using either approach.

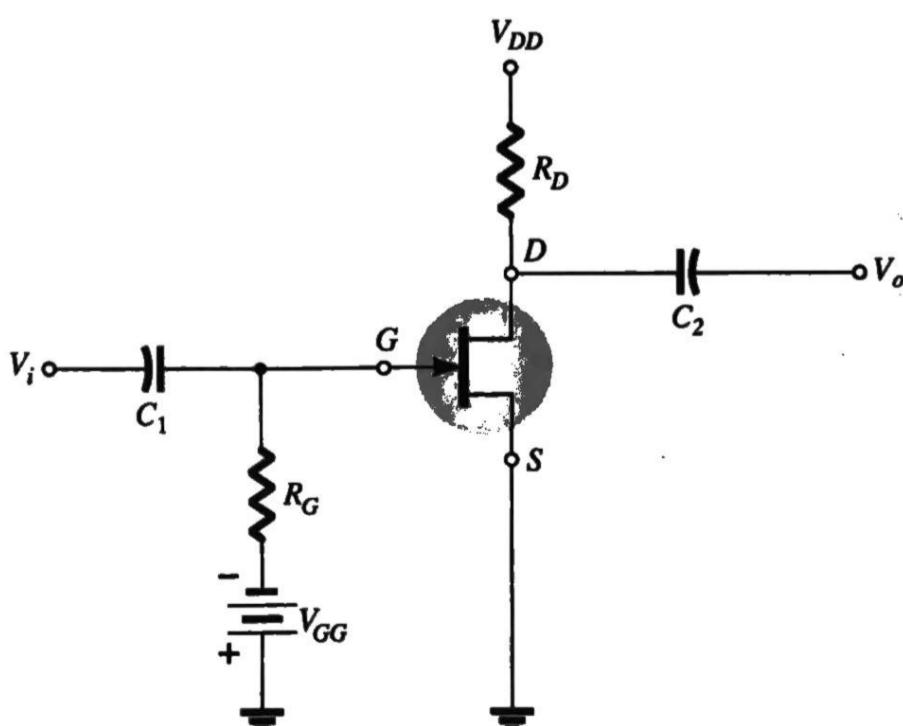


FIG. 7.1
Fixed-bias configuration.

The configuration of Fig. 7.1 includes the ac levels V_i and V_o and the coupling capacitors (C_1 and C_2). Recall that the coupling capacitors are “open circuits” for the dc analysis and low impedances (essentially short circuits) for the ac analysis. The resistor R_G is present to ensure that V_i appears at the input to the FET amplifier for the ac analysis (Chapter 8). For the dc analysis,

$$I_G \approx 0 \text{ A}$$

and

$$V_{R_G} = I_G R_G = (0 \text{ A}) R_G = 0 \text{ V}$$

The zero-volt drop across R_G permits replacing R_G by a short-circuit equivalent, as appearing in the network of Fig. 7.2, specifically redrawn for the dc analysis.

The fact that the negative terminal of the battery is connected directly to the defined positive potential of V_{GS} clearly reveals that the polarity of V_{GS} is directly opposite to that of V_{GG} . Applying Kirchhoff's voltage law in the clockwise direction of the indicated loop of Fig. 7.2 results in

$$-V_{GG} - V_{GS} = 0$$

and

$$V_{GS} = -V_{GG}$$

Since V_{GG} is a fixed dc supply, the voltage V_{GS} is fixed in magnitude, resulting in the designation “fixed-bias configuration.”

The resulting level of drain current I_D is now controlled by Shockley’s equation:

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$

Since V_{GS} is a fixed quantity for this configuration, its magnitude and sign can simply be substituted into Shockley’s equation and the resulting level of I_D calculated. This is one of the few instances in which a mathematical solution to a FET configuration is quite direct.

A graphical analysis would require a plot of Shockley’s equation as shown in Fig. 7.3. Recall that choosing $V_{GS} = V_P/2$ will result in a drain current of $I_{DSS}/4$ when plotting the equation. For the analysis of this chapter, the three points defined by I_{DSS} , V_P , and the intersection just described will be sufficient for plotting the curve.

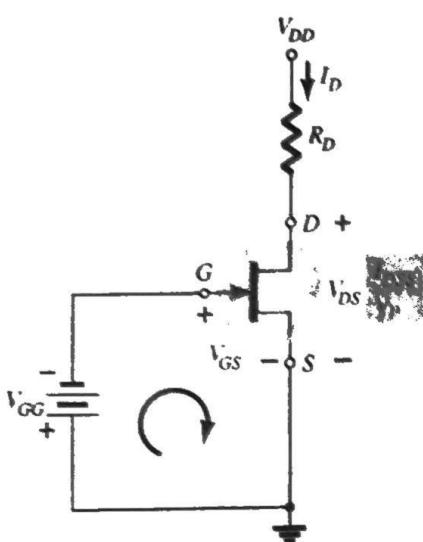


FIG. 7.2

Network for dc analysis.

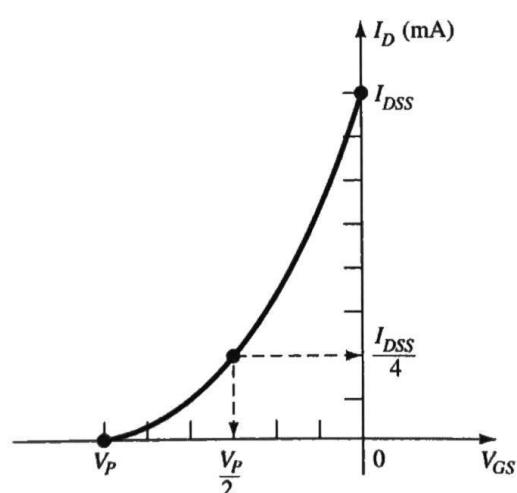


FIG. 7.3
Plotting Shockley's equation.

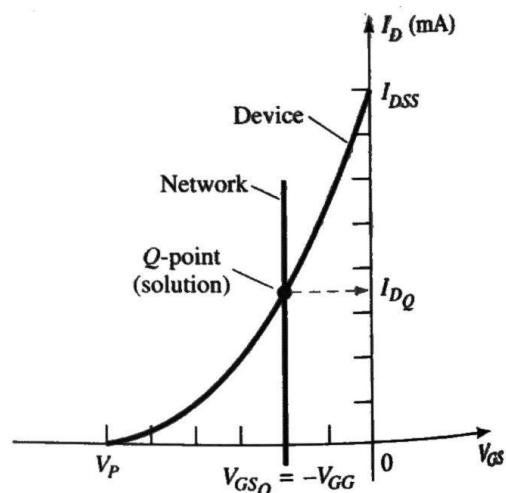


FIG. 7.4
Finding the solution for the fixed-bias configuration.

In Fig. 7.4, the fixed level of V_{GS} has been superimposed as a vertical line at $V_{GS} = -V_{GG}$. At any point on the vertical line, the level of V_{GS} is $-V_{GG}$ —the level of I_D must simply be determined on this vertical line. The point where the two curves intersect is the common solution to the configuration—commonly referred to as the *quiescent* or *operating point*. The subscript Q will be applied to the drain current and gate-to-source voltage to identify their levels at the Q -point. Note in Fig. 7.4 that the quiescent level of I_D is determined by drawing a horizontal line from the Q -point to the vertical I_D axis. It is important to realize

that once the network of Fig. 7.1 is constructed and operating, the dc levels of I_D and V_{GS} that will be measured by the meters of Fig. 7.5 are the quiescent values defined by Fig. 7.4.

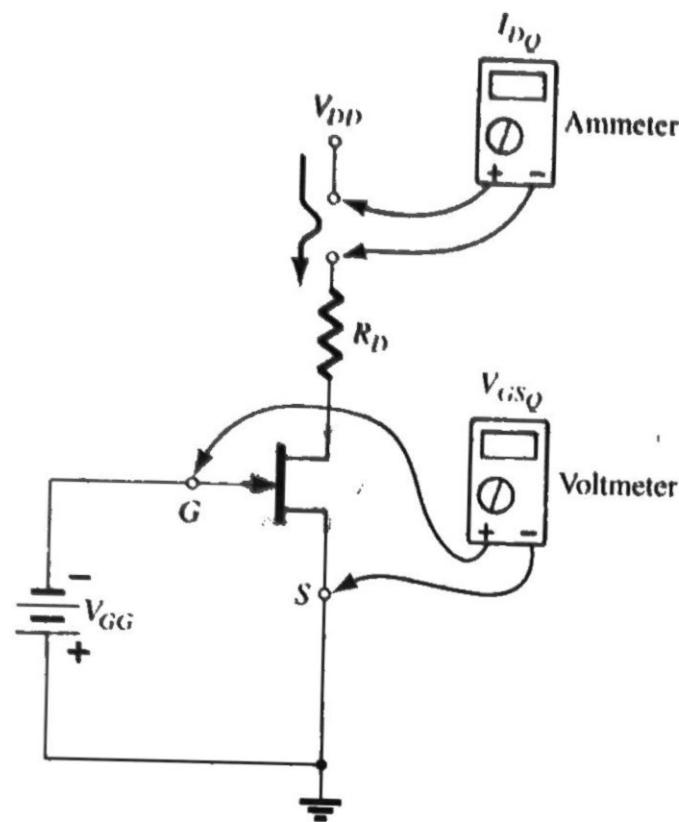


FIG. 7.5
Measuring the quiescent values of I_D and V_{GS} .

The drain-to-source voltage of the output section can be determined by applying Kirchhoff's voltage law as follows:

$$+V_{DS} + I_D R_D - V_{DD} = 0$$

and

$$\boxed{V_{DS} = V_{DD} - I_D R_D} \quad (7.6)$$

Recall that single-subscript voltages refer to the voltage at a point with respect to ground. For the configuration of Fig. 7.2,

$$\boxed{V_S = 0 \text{ V}} \quad (7.7)$$

Using double-subscript notation, we have

$$V_{DS} = V_D - V_S$$

or

$$V_D = V_{DS} + V_S = V_{DS} + 0 \text{ V}$$

and

$$\boxed{V_D = V_{DS}} \quad (7.8)$$

In addition,

$$V_{GS} = V_G - V_S$$

or

$$V_G = V_{GS} + V_S = V_{GS} + 0 \text{ V}$$

and

$$\boxed{V_G = V_{GS}} \quad (7.9)$$

The fact that $V_D = V_{DS}$ and $V_G = V_{GS}$ is fairly obvious from the fact that $V_S = 0 \text{ V}$, but the derivations above were included to emphasize the relationship that exists between double-subscript and single-subscript notation. Since the configuration requires two dc supplies, its use is limited and will not be included in the forthcoming list of the most common FET configurations.

EXAMPLE 7.1 Determine the following for the network of Fig. 7.6:

- V_{GSQ}
- I_{DQ}
- V_{DS}
- V_D
- V_G
- V_S

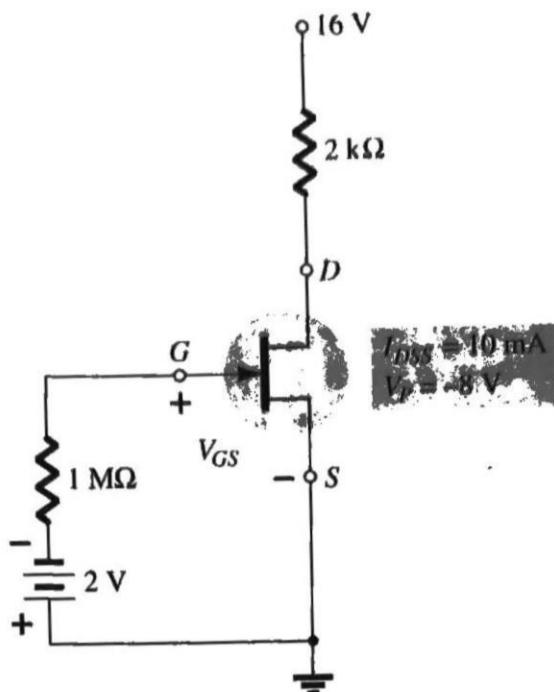


FIG. 7.6
Example 7.1.

Solution:

Mathematical Approach

a. $V_{GSQ} = -V_{GG} = -2 \text{ V}$

b. $I_{DQ} = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2 = 10 \text{ mA} \left(1 - \frac{-2 \text{ V}}{-8 \text{ V}} \right)^2$
 $= 10 \text{ mA} (1 - 0.25)^2 = 10 \text{ mA} (0.75)^2 = 10 \text{ mA} (0.5625)$
 $= 5.625 \text{ mA}$

c. $V_{DS} = V_{DD} - I_D R_D = 16 \text{ V} - (5.625 \text{ mA})(2 \text{ k}\Omega)$
 $= 16 \text{ V} - 11.25 \text{ V} = 4.75 \text{ V}$

d. $V_D = V_{DS} = 4.75 \text{ V}$

e. $V_G = V_{GS} = -2 \text{ V}$

f. $V_S = 0 \text{ V}$

Graphical Approach The resulting Shockley curve and the vertical line at $V_{GS} = -2 \text{ V}$ are provided in Fig. 7.7. It is certainly difficult to read beyond the second place without

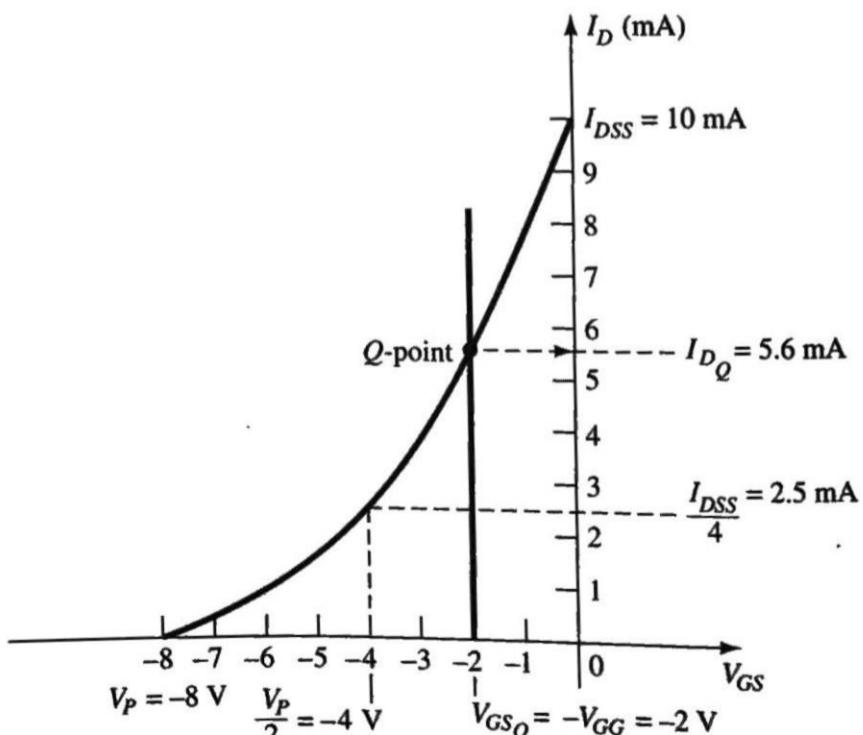


FIG. 7.7
Graphical solution for the network of Fig. 7.6.

- d. Eq. (7.12): $V_S = I_D R_S$
 $= (2.6 \text{ mA})(1 \text{ k}\Omega)$
 $= 2.6 \text{ V}$
- e. Eq. (7.13): $V_G = 0 \text{ V}$
- f. Eq. (7.14): $V_D = V_{DS} + V_S = 8.82 \text{ V} + 2.6 \text{ V} = 11.42 \text{ V}$
or $V_D = V_{DD} - I_D R_D = 20 \text{ V} - (2.6 \text{ mA})(3.3 \text{ k}\Omega) = 11.42 \text{ V}$

EXAMPLE 7.3 Find the quiescent point for the network of Fig. 7.12 if:

- a. $R_S = 100 \Omega$.
b. $R_S = 10 \text{ k}\Omega$.

Solution: Both $R_S = 100 \Omega$ and $R_S = 10 \text{ k}\Omega$ are plotted on Fig. 7.16.

- a. For $R_S = 100 \Omega$:

$$I_{DQ} \approx 6.4 \text{ mA}$$

and from Eq. (7.10),

$$V_{GSQ} \approx -0.64 \text{ V}$$

- b. For $R_S = 10 \text{ k}\Omega$

$$V_{GSQ} \approx -4.6 \text{ V}$$

and from Eq. (7.10),

$$I_{DQ} \approx 0.46 \text{ mA}$$

In particular, note how lower levels of R_S bring the load line of the network closer to the I_D axis, whereas increasing levels of R_S bring the load line closer to the V_{GS} axis.

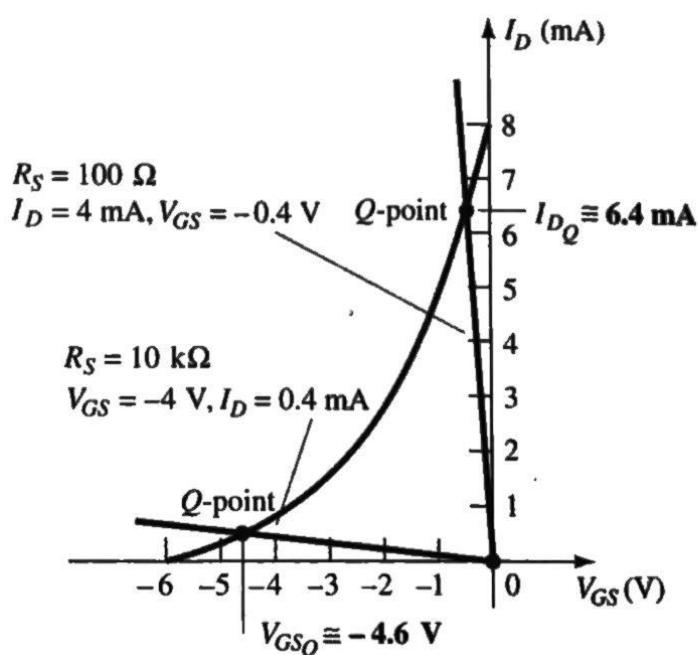


FIG. 7.16
Example 7.3.

7.4 VOLTAGE-DIVIDER BIASING

The voltage-divider bias arrangement applied to BJT transistor amplifiers is also applied to FET amplifiers as demonstrated by Fig. 7.17. The basic construction is exactly the same, but the dc analysis of each is quite different. $I_G = 0 \text{ A}$ for FET amplifiers, but the magnitude of I_B for common-emitter BJT amplifiers can affect the dc levels of current and voltage in both the input and output circuits. Recall that I_B provides the link between input and output circuits for the BJT voltage-divider configuration, whereas V_{GS} does the same for the FET configuration.

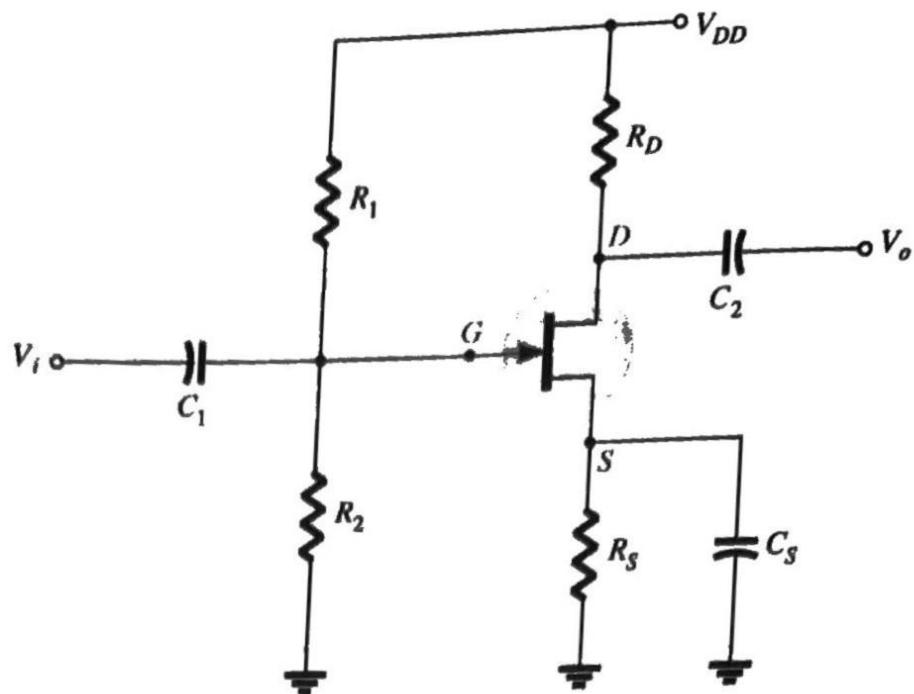


FIG. 7.17
Voltage-divider bias arrangement.

The network of Fig. 7.17 is redrawn as shown in Fig. 7.18 for the dc analysis. Note that all the capacitors, including the bypass capacitor C_S , have been replaced by an “open-circuit” equivalent in Fig. 7.18b. In addition, the source V_{DD} was separated into two equivalent sources to permit a further separation of the input and output regions of the network. Since $I_G = 0 \text{ A}$, Kirchhoff’s current law requires that $I_{R_1} = I_{R_2}$, and the series equivalent circuit appearing to the left of the figure can be used to find the level of V_G . The voltage V_G , equal to the voltage across R_2 , can be found using the voltage-divider rule and Fig. 7.18a as follows:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} \quad (7.15)$$

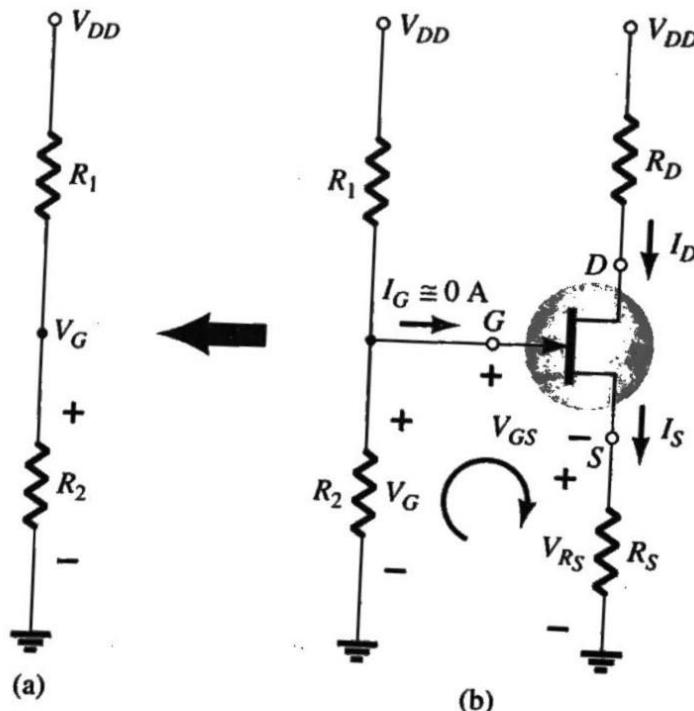


FIG. 7.18
Redrawn network of Fig. 7.17 for dc analysis.

Applying Kirchhoff’s voltage law in the clockwise direction to the indicated loop of Fig. 7.18 results in

$$\begin{aligned} V_G - V_{GS} - V_{RS} &= 0 \\ V_{GS} &= V_G - V_{RS} \end{aligned}$$

and

Substituting $V_{RS} = I_S R_S = I_D R_S$, we have

$$V_{GS} = V_G - I_D R_S \quad (7.16)$$

The result is an equation that continues to include the same two variables appearing in Shockley's equation: V_{GS} and I_D . The quantities V_G and R_S are fixed by the network construction. Equation (7.16) is still the equation for a straight line, but the origin is no longer a point in the plotting of the line. The procedure for plotting Eq. (7.16) is not a difficult one and will proceed as follows. Since any straight line requires two points to be defined, let us first use the fact that anywhere on the horizontal axis of Fig. 7.19 the current $I_D = 0$ mA. If we therefore select I_D to be 0 mA, we are in essence stating that we are somewhere on the horizontal axis. The exact location can be determined simply by substituting $I_D = 0$ mA into Eq. (7.16) and finding the resulting value of V_{GS} as follows:

$$\begin{aligned} V_{GS} &= V_G - I_D R_S \\ &= V_G - (0 \text{ mA}) R_S \end{aligned}$$

and

$$V_{GS} = V_G \Big|_{I_D=0 \text{ mA}} \quad (7.17)$$

The result specifies that whenever we plot Eq. (7.16), if we choose $I_D = 0$ mA, the value of V_{GS} for the plot will be V_G volts. The point just determined appears in Fig. 7.19.

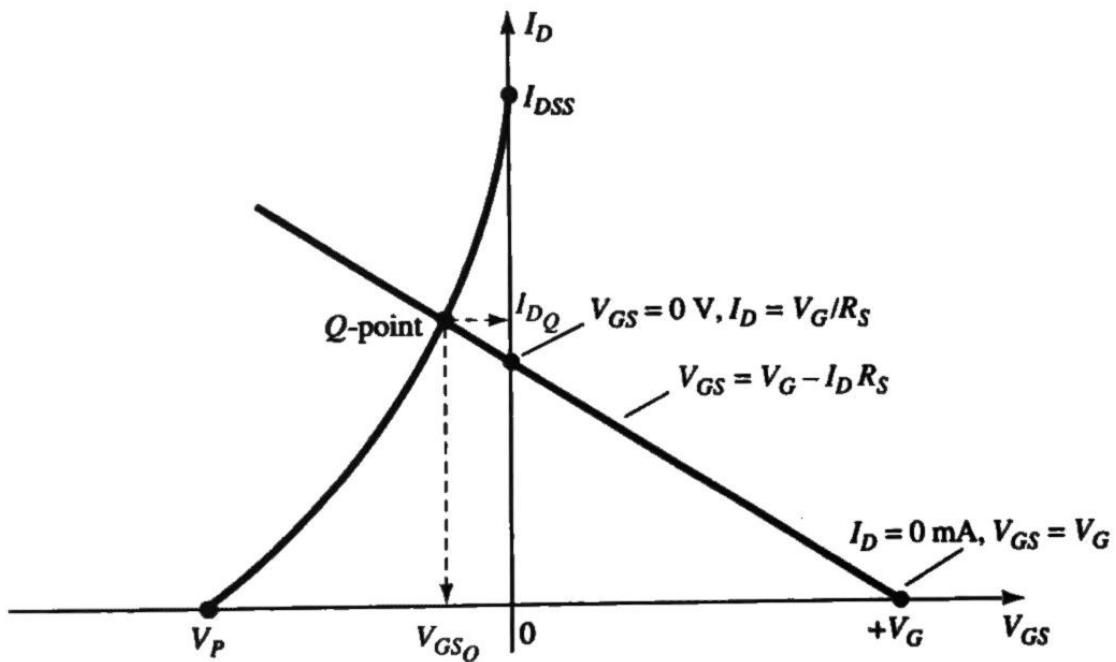


FIG. 7.19
Sketching the network equation for the voltage-divider configuration.

For the other point, let us now employ the fact that at any point on the vertical axis $V_{GS} = 0$ V and solve for the resulting value of I_D :

$$\begin{aligned} V_{GS} &= V_G - I_D R_S \\ 0 \text{ V} &= V_G - I_D R_S \end{aligned}$$

and

$$I_D = \frac{V_G}{R_S} \Big|_{V_{GS}=0 \text{ V}} \quad (7.18)$$

The result specifies that whenever we plot Eq. (7.16), if $V_{GS} = 0$ V, the level of I_D is determined by Eq. (7.18). This intersection also appears on Fig. 7.19.

The two points defined above permit the drawing of a straight line to represent Eq. (7.16). The intersection of the straight line with the transfer curve in the region to the left of the vertical axis will define the operating point and the corresponding levels of I_D and V_{GS} .

Since the intersection on the vertical axis is determined by $I_D = V_G/R_S$ and V_G is fixed by the input network, increasing values of R_S will reduce the level of the I_D intersection as

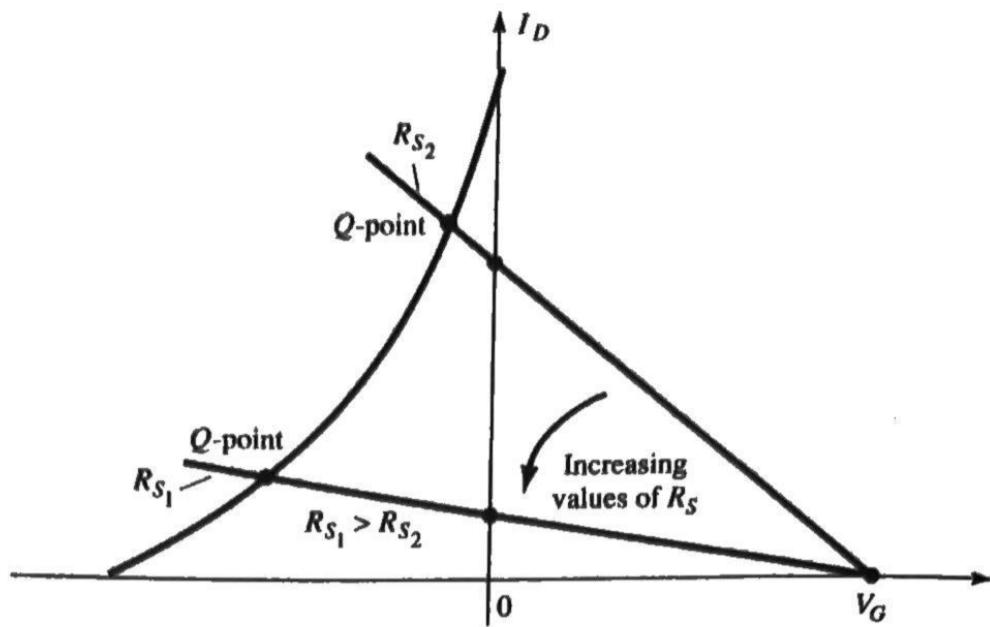


FIG. 7.20
Effect of R_S on the resulting Q -point.

shown in Fig. 7.20. It is fairly obvious from Fig. 7.20 that:

Increasing values of R_S result in lower quiescent values of I_D and declining values of V_{GS} .

Once the quiescent values of I_{DQ} and V_{GSQ} are determined, the remaining network analysis can be performed in the usual manner. That is,

$$V_{DS} = V_{DD} - I_D(R_D + R_S) \quad (7.19)$$

$$V_D = V_{DD} - I_D R_D \quad (7.20)$$

$$V_S = I_D R_S \quad (7.21)$$

$$I_{R_1} = I_{R_2} = \frac{V_{DD}}{R_1 + R_2} \quad (7.22)$$

EXAMPLE 7.4 Determine the following for the network of Fig. 7.21:

- I_{DQ} and V_{GSQ} .
- V_D .
- V_S .
- V_{DS} .
- V_{DG} .

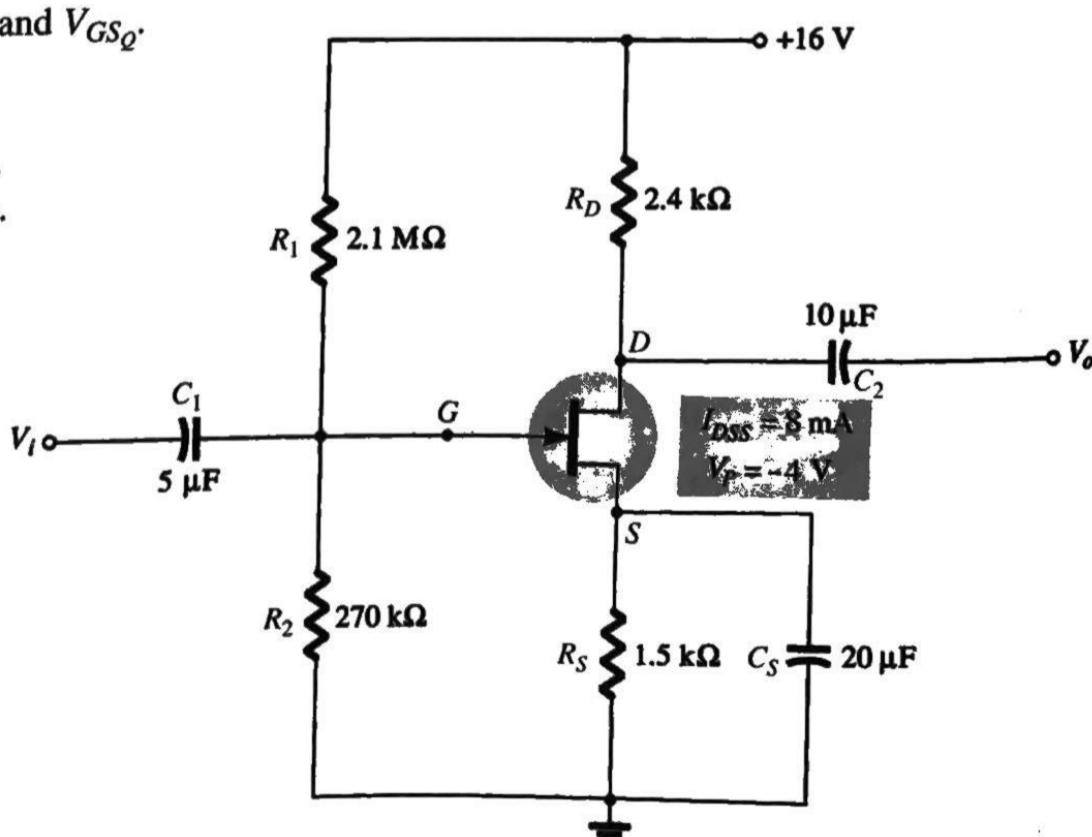


FIG. 7.21
Example 7.4.

Solution:

- a. For the transfer characteristics, if $I_D = I_{DSS}/4 = 8 \text{ mA}/4 = 2 \text{ mA}$, then $V_{GS} = V_P/2 = -4 \text{ V}/2 = -2 \text{ V}$. The resulting curve representing Shockley's equation appears in Fig. 7.22. The network equation is defined by

$$\begin{aligned}V_G &= \frac{R_2 V_{DD}}{R_1 + R_2} \\&= \frac{(270 \text{ k}\Omega)(16 \text{ V})}{2.1 \text{ M}\Omega + 0.27 \text{ M}\Omega} \\&= 1.82 \text{ V}\end{aligned}$$

and

$$\begin{aligned}V_{GS} &= V_G - I_D R_S \\&= 1.82 \text{ V} - I_D (1.5 \text{ k}\Omega)\end{aligned}$$

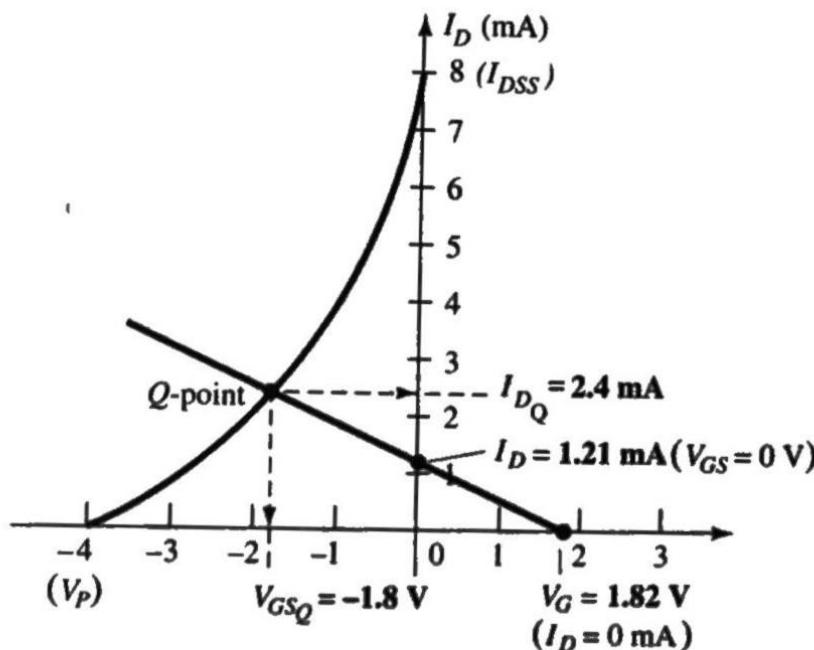


FIG. 7.22
Determining the *Q*-point for the network of Fig. 7.21.

When $I_D = 0 \text{ mA}$,

$$V_{GS} = +1.82 \text{ V}$$

When $V_{GS} = 0 \text{ V}$,

$$I_D = \frac{1.82 \text{ V}}{1.5 \text{ k}\Omega} = 1.21 \text{ mA}$$

The resulting bias line appears on Fig. 7.22 with quiescent values of

$$I_{DQ} = 2.4 \text{ mA}$$

and $V_{GSQ} = -1.8 \text{ V}$

b. $V_D = V_{DD} - I_D R_D$

$$\begin{aligned}&= 16 \text{ V} - (2.4 \text{ mA})(2.4 \text{ k}\Omega) \\&= 10.24 \text{ V}\end{aligned}$$

c. $V_S = I_D R_S = (2.4 \text{ mA})(1.5 \text{ k}\Omega)$

$$= 3.6 \text{ V}$$

d. $V_{DS} = V_{DD} - I_D(R_D + R_S)$

$$\begin{aligned}&= 16 \text{ V} - (2.4 \text{ mA})(2.4 \text{ k}\Omega + 1.5 \text{ k}\Omega) \\&= 6.64 \text{ V}\end{aligned}$$

or $V_{DS} = V_D - V_S = 10.24 \text{ V} - 3.6 \text{ V}$

$$= 6.64 \text{ V}$$