

FIELD-EFFECT TRANSISTOR

Notes By:-

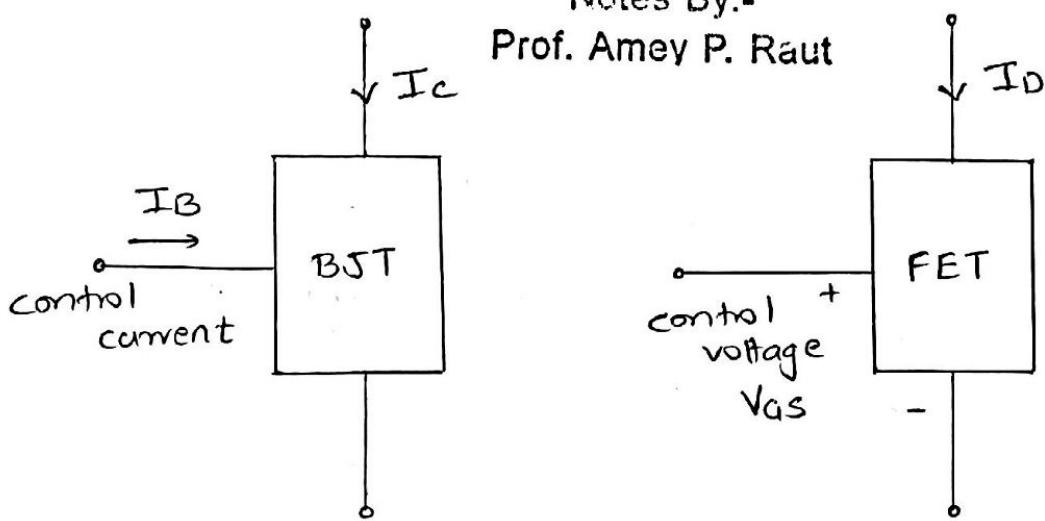
Prof. Amey P. Raut

The field-effect transistor (FET) is a three-terminal device like BJT, although there are important differences between the two type of devices as follows:-

- 1) The BJT transistor is a current-controlled device whereas the JFET transistor is a voltage controlled device.
- 2) One of the most important characteristics of the FET is its high input impedance.
- 3) AC voltage gains for BJT amplifiers are great deal more than for FET's.
- 4) FET's are more temperature stable than BJT's.
- 5) FET's are usually smaller than BJT's making them particularly useful in integrated-circuits (IC).

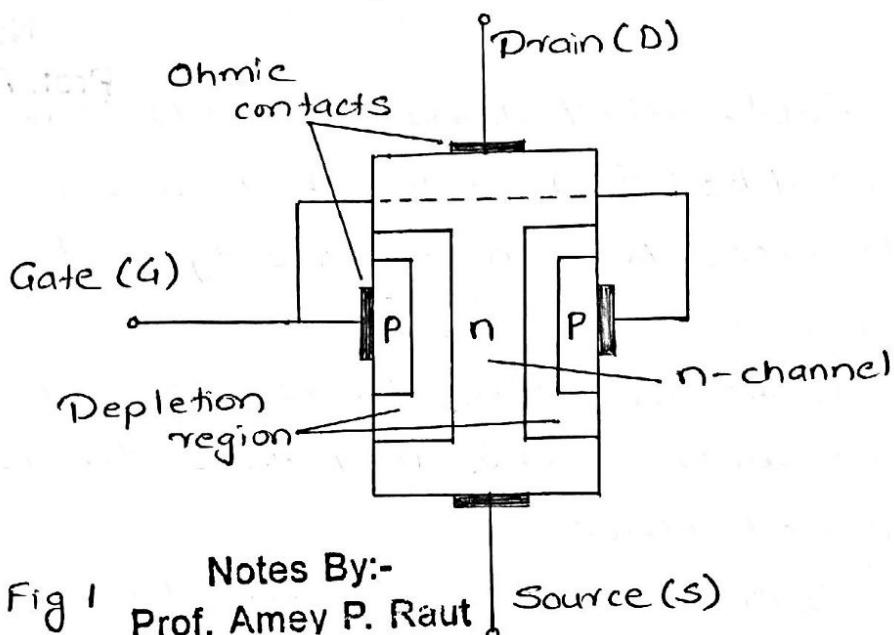
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* CONSTRUCTION AND CHARACTERISTICS

The JFET is a three-terminal device with one terminal capable of controlling the currents between the other two.



The basic construction of the n-channel JFET is shown in fig 1. The major part of the structure is the n-type material, which forms the channel between the embedded layers of p-type material.

The top of the n-type channel is connected through an ohmic contact to a terminal referred to as the drain (D).

The lower end of the same material is connected through an ohmic contact to a terminal referred to as the source (S). Notes By:- Prof. Amey P. Raut

The two p-type materials are connected together and to the gate (G) terminal.

In the absence of any applied potentials the JFET has two p-n junctions under no-bias conditions. The result is a depletion region at each junction.

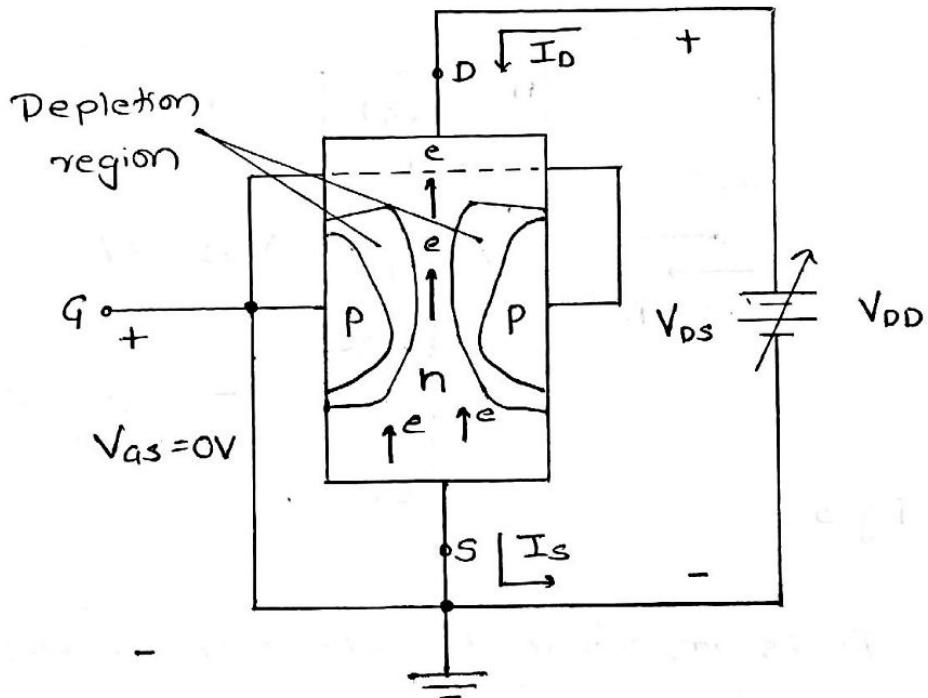
Depletion region is void of free electrons and is therefore unable to support conduction.

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* $V_{GS} = 0V$, V_{DS} some Positive Value

Fig 2



In Fig 2, a positive voltage V_{DS} is applied across the channel and the gate is connected directly to the source to establish the condition $V_{GS} = 0V$.

The result is a gate and a source terminal at the same potential and a depletion region in the low end of each p-material similar to the no-bias conditions.

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The instant the voltage V_{DD} ($= V_{DS}$) is applied, the electrons are drawn to the drain terminal, establishing the conventional current I_D with the defined direction of fig 2.

The path of charge flow clearly reveals that the drain and source currents are equivalent ($I_D = I_S$). Under the conditions in fig 2, the flow of charge is relatively uninhibited and is limited solely by the resistance of the n-channel between drain and source.

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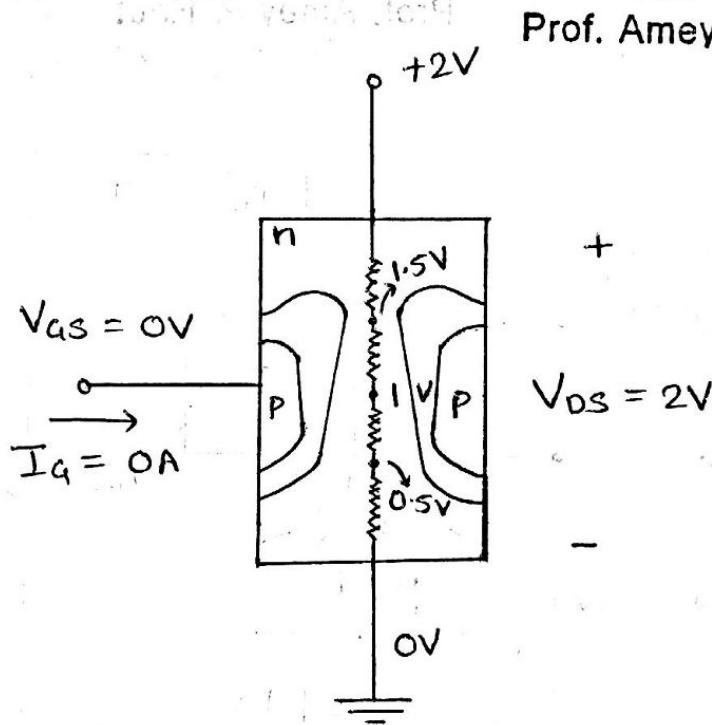


Fig 3

It is important to note that the depletion region is wider near the top of both p-type materials. The reason for the change in width of the region is described with help of fig 3.

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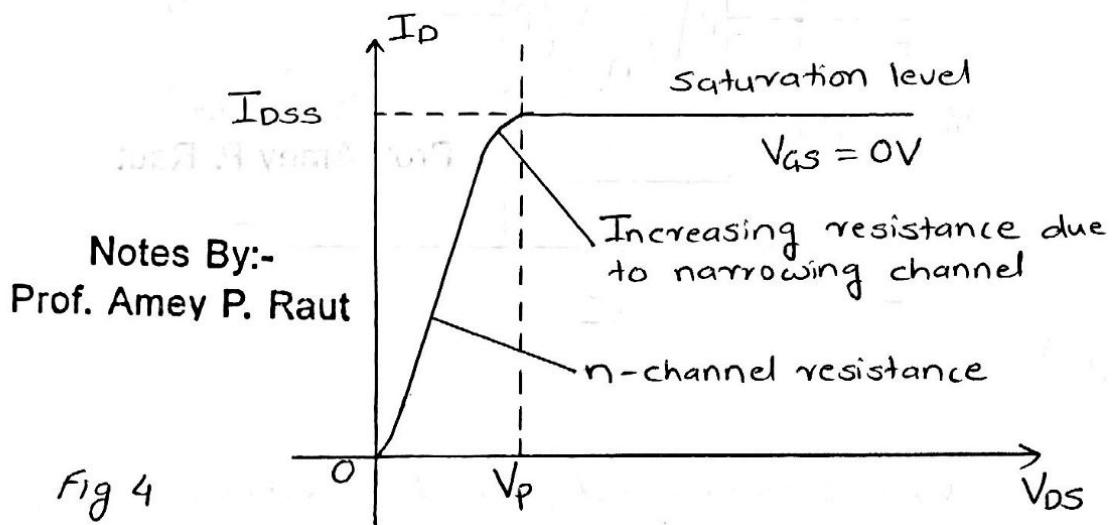
Assuming a uniform resistance in the n-channel the resistance of the channel can be breakdown into the divisions as shown in fig 3.

The current I_D will establish the voltage levels through the channel as indicated in fig.

The result is that the upper region of the p-type material will be reverse-biased by about 1.5V, with the lower region only reverse-biased by 0.5V.

As in the reverse biased condition the greater the applied reverse bias, the wider is the depletion region - hence the distribution of the depletion region as shown in Fig 3.

As the p-n junction is reverse-biased for the length of the channel results in a gate current of zero amperes i.e. $I_g = 0A$, which is an important characteristic of the JFET.



As the voltage V_{DS} is increased from 0V to a few volts, the current will increase as determined by Ohm's law and the plot of I_D v/s V_{DS} will appear as shown in fig 4.

The relative straightness of the plot reveals that for the region of low values of V_{DS} , the resistance is essentially constant.

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As V_{DS} increases and approaches a level referred to as V_p , the depletion regions will widen, causing a noticeable reduction in the channel width. The reduced path of conduction causes the resistance to increase and the curve in the graph of fig 4 to occur.

The more horizontal the curve, the higher the resistance, suggesting that the resistance is approaching infinite ohms in the horizontal region.

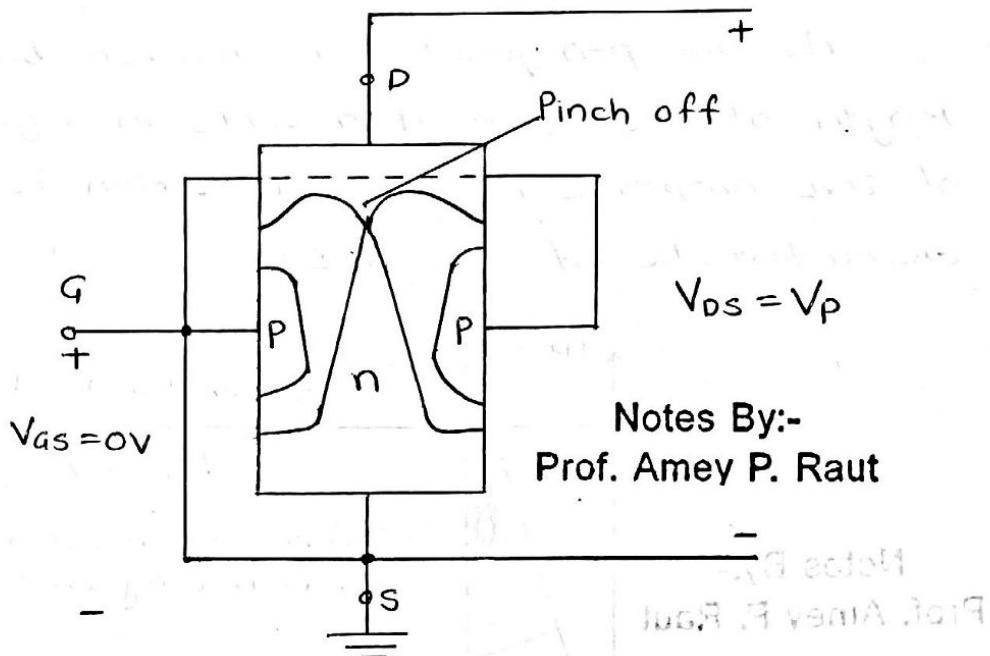


Fig 5.

If V_{DS} is increased to a level where it appears that the two depletion regions would "touch" as shown in Fig 5. a condition referred to as pinch off occurs.

The level of V_{DS} that establishes this condition is referred to as the pinch-off voltage and is denoted by V_p as shown in fig 4. it suggests the current I_D is pinched off and drops to 0A.

However, I_D maintains a saturation level defined as I_{DSS} . In reality a very small channel still exists with a current of very high density.

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The absence of a drain current would remove the possibility of different potential levels through the n-channel to establish the varying levels of reverse bias along the junction. The result would be a loss of depletion region distribution that caused pinch-off in the first place.

As V_{DS} is increased beyond V_p , the region of close encounter between the two depletion regions increases in length along the channel, but the level of I_D remains the same. Therefore once $V_{DS} > V_p$ the JFET has the characteristics of a current source. The current is fixed at $I_D = I_{DSS}$, but the voltage V_{DS} is determined by the applied load.

I_{DSS} is the maximum drain current for a JFET and is defined by the conditions $V_{GS}=0V$, $V_{DS} > |V_p|$

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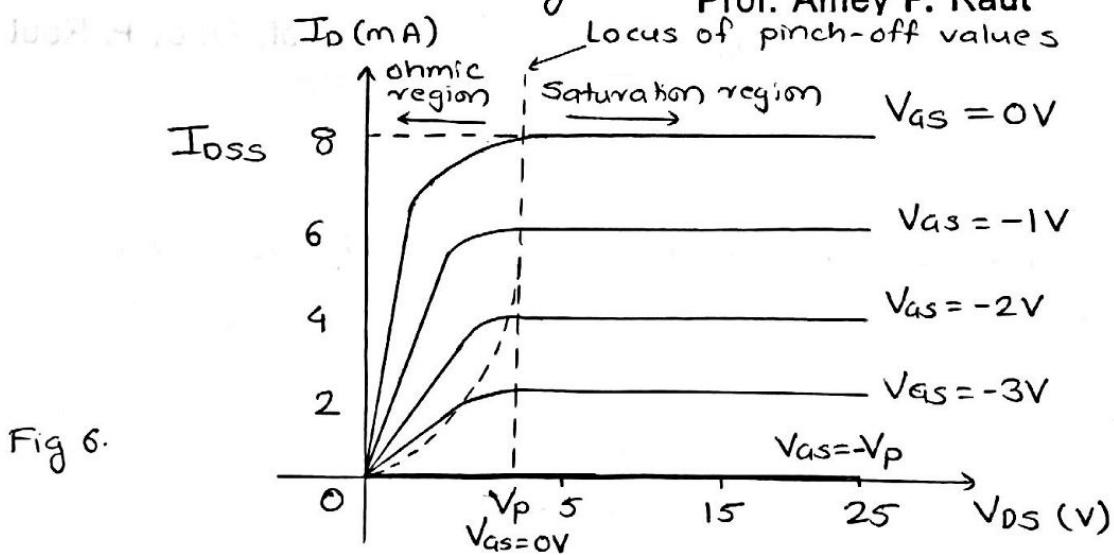
* $V_{GS} < 0V$

The voltage from gate to source V_{GS} is the controlling voltage of the JFET. For the n-channel device the controlling voltage V_{GS} is made more and more negative from its $V_{GS}=0V$ level.

If a negative voltage of $-1V$ is applied betn the gate and source terminals for a low level of V_{DS} . The effect of the applied negative-bias V_{GS} will establish depletion regions similar to those obtained with $V_{GS}=0V$, but a lower levels of V_{DS} . Thus the JFET reaches the saturation level at a lower level

of V_{DS} as shown in fig 6.

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The resulting saturation level for I_D has been reduced and will continue to decrease as V_{AS} is made more and more negative.

The pinch-off voltage continues to drop in a parabolic manner as V_{AS} becomes more and more negative.

When $V_{AS} = -V_P$, V_{AS} will be sufficiently negative to establish a saturation level that is 0mA. and for all practical purposes the device has been turned off.

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The level of V_{AS} that results in $I_D = 0mA$ is defined by $V_{AS} = V_P$, with V_P being a negative voltage for n-channel devices and a positive voltage for p-channel JFETs.

* Voltage controlled Resistor

The region to the left of the pinch-off locus of Fig 6 is referred to as the ohmic or voltage controlled resistance region. In the region the JFET can actually be employed as a variable resistor whose resistance is controlled by the V_{AS} .

The resistance level in terms of applied V_{AS} is given by

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$$R_d = \frac{R_0}{(1 - V_{AS}/V_P)^2}$$

Where $R_0 \rightarrow$ resistance with $V_{AS} = 0V$

$R_d \rightarrow$ resistance at particular level of V_{AS} .

* P-CHANNEL DEVICES

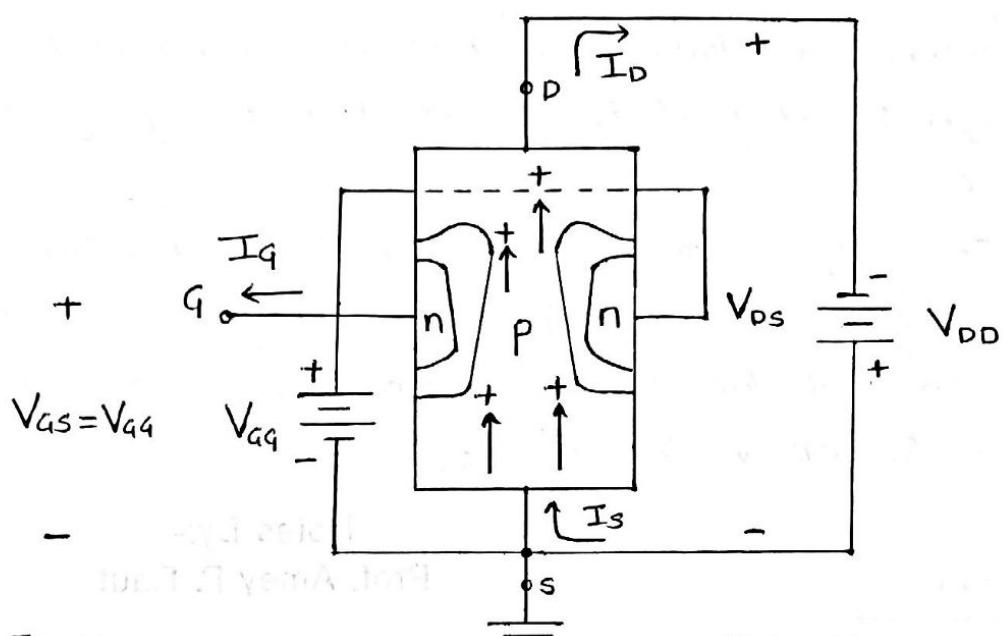


Fig 7.

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The p-channel JFET is constructed in exactly the same manner as the n-channel device, but with a reversal of the p- and n-type materials as shown.

The defined current directions are reversed, as are the actual polarities for the voltages V_{GS} and V_{DS} .

For the p-channel device, the channel will be constricted by increasing positive voltages from gate to source, and the source V_{DD} will result in negative voltages for V_{DS} on the characteristics of fig 8. The minus sign indicates that source is at higher potential than drain.

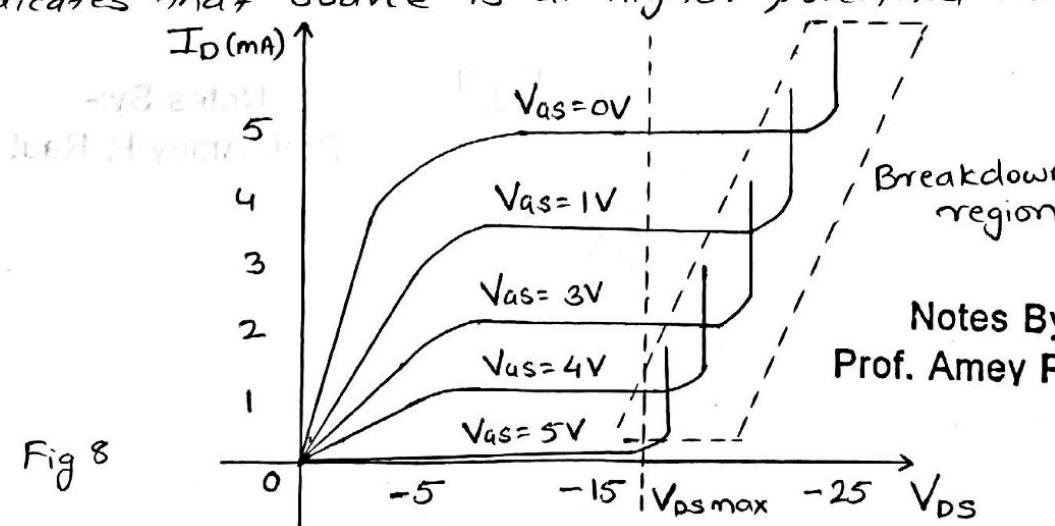


Fig 8

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At high levels of V_{GS} the curves suddenly rise to levels that seem unbounded. The vertical rise is an indication that breakdown has occurred and the current through the channel is now limited solely by the external circuit.

This region can be avoided if the level of V_{GSmax} is noted on the specification sheet and the design is such that the actual level of V_{GS} is less than this value for all values of V_{DS} .

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* Symbols

The graphic symbols for the n-channel and p-channel JFET's are provided in fig 9. The arrow represents the direction in which I_D would flow if the p-n junction were forward biased.

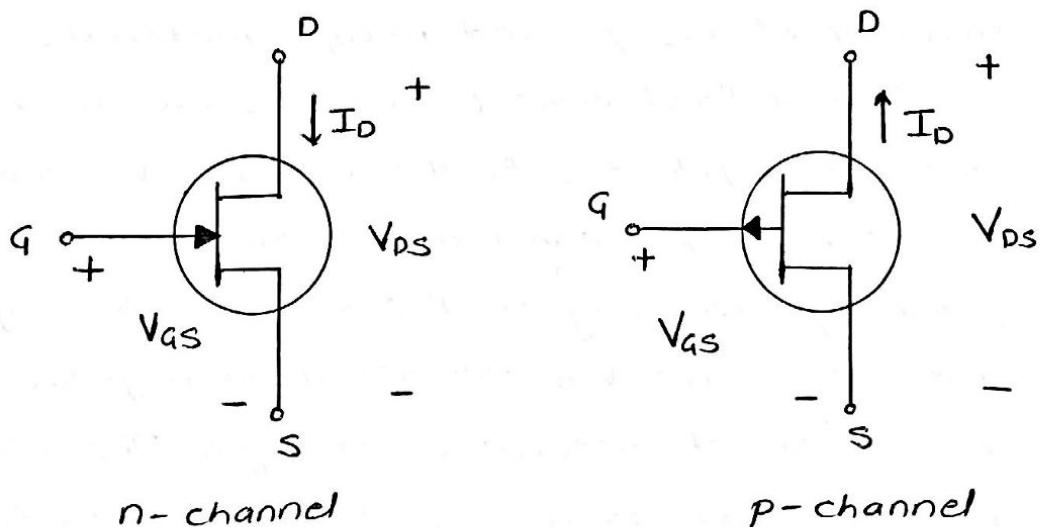


Fig 9

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* TRANSFER CHARACTERISTICS

Linear relationship does not exist between the output and input quantities of a JFET. The relationship between I_D and V_{GS} is defined by Shockley's equation.

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$

where, I_{DSS} & $V_P \rightarrow$ constants

$V_{GS} \rightarrow$ control variables

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The squared term in the equation results in a non-linear relationship between I_D and V_{GS} , producing a curve that grows exponentially with decreasing magnitude of V_{GS} .

The transfer curve can be obtained using Shockley's equation or from the output characteristics.

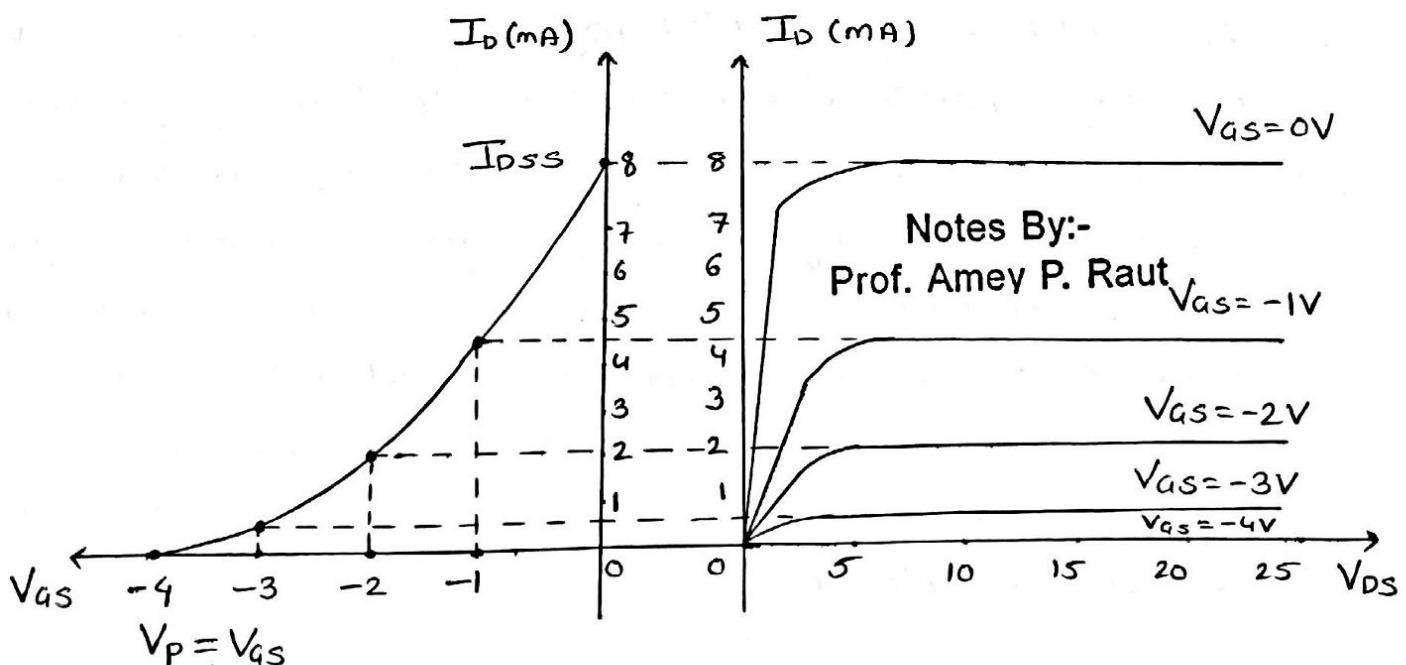


Fig 10

In fig 10 two graphs are provided, with the vertical scaling in milliamperes for each graph. One is plot of I_D versus V_{DS} , whereas the other is I_D versus V_{AS} .

Using the drain characteristics on the right of the y axis we can draw a horizontal line from the saturation region of the curve denoted $V_{AS} = 0V$. to the I_D axis. The resulting current level for both graphs is I_{DSS} .

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The point of intersection on the I_D versus V_{AS} curve will be as shown since the vertical axis is defined as $V_{AS} = 0V$.

when, $V_{AS} = 0V$, $I_D = I_{DSS}$

$V_{AS} = V_p$, $I_D = 0mA$

The transfer characteristics are a plot of an output current versus an input control quantity. There is therefore a direct transfer from input to output variables when employing the curve.

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If the relationship were linear, the plot of I_D v/s V_{AS} would result in a straight line between I_{DSS} & V_p . However, a parabolic curve will result because the vertical spacing between steps of V_{AS} on the drain characteristics decreases noticeably as V_{AS} becomes more & more negative.

If a horizontal line is drawn from the $V_{AS} = -1V$ curve to the I_D axis and then extended to the other axis, another point on the transfer curve can be located. Continuing with $V_{AS} = -2V$ and $-3V$, the transfer curve is completed.

* Parameters of JFET:-

→ Dynamic Drain Resistance (r_d)

Drain resistance is an AC resistance of a JFET. It is defined as the ratio of change in the drain to source voltage (V_{DS}) to the corresponding change in the drain current, at a constant value of gate to source voltage (V_{GS}).

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$$r_d = \left. \frac{\Delta V_{DS}}{\Delta I_D} \right|_{\text{constant } V_{GS}}$$

Drain resistance is calculated in the saturation region of the FET output characteristics.

→ Transconductance (g_m)

The transconductance (g_m) is defined as the ratio of change in drain current to the corresponding change in gate to source voltage, at a constant value of drain to source voltage.

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$$g_m = \left. \frac{\Delta I_D}{\Delta V_{GS}} \right|_{\text{constant } V_{DS}}$$

→ Amplification Factor (μ)

Amplification factor ' μ ' is defined as the ratio of change in the drain to source voltage to change in the gate to source voltage, at a constant value of drain current.

$$\therefore M = \left| \frac{\Delta V_{DS}}{\Delta V_{GS}} \right| \quad | I_D \text{ constant}$$

Relationship between M , r_d & g_m

$$M = \frac{\Delta V_{DS}}{\Delta V_{GS}} = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}}$$

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$$\therefore M = r_d \times g_m$$

→ Input Resistance (R_{in})

The JFET operates with reverse biased gate to source junction. Therefore its input resistance at the gate is very high.

It can be determined as the ratio of gate to source voltage to the gate reverse current at a certain gate to source voltage.

$$R_{in} = \left| \frac{V_{GS}}{I_{GSS}} \right|$$

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with increase in temperature I_{GSS} will also increase. Hence R_{in} decreases with increase in temperature.

→ Input Capacitance (C_{iss})

The reverse biased p-n junction offers a capacitance called junction capacitance or transition capacitance.

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Input capacitance is the capacitance of the reverse biased gate to source p-n junction. It depends on the reverse voltage applied across the junction.

* MOSFET

The name MOSFET stands for metal-oxide-semiconductor field-effect transistor. MOSFETs are further broken down into depletion type and enhancement type.

* Depletion - Type MOSFET

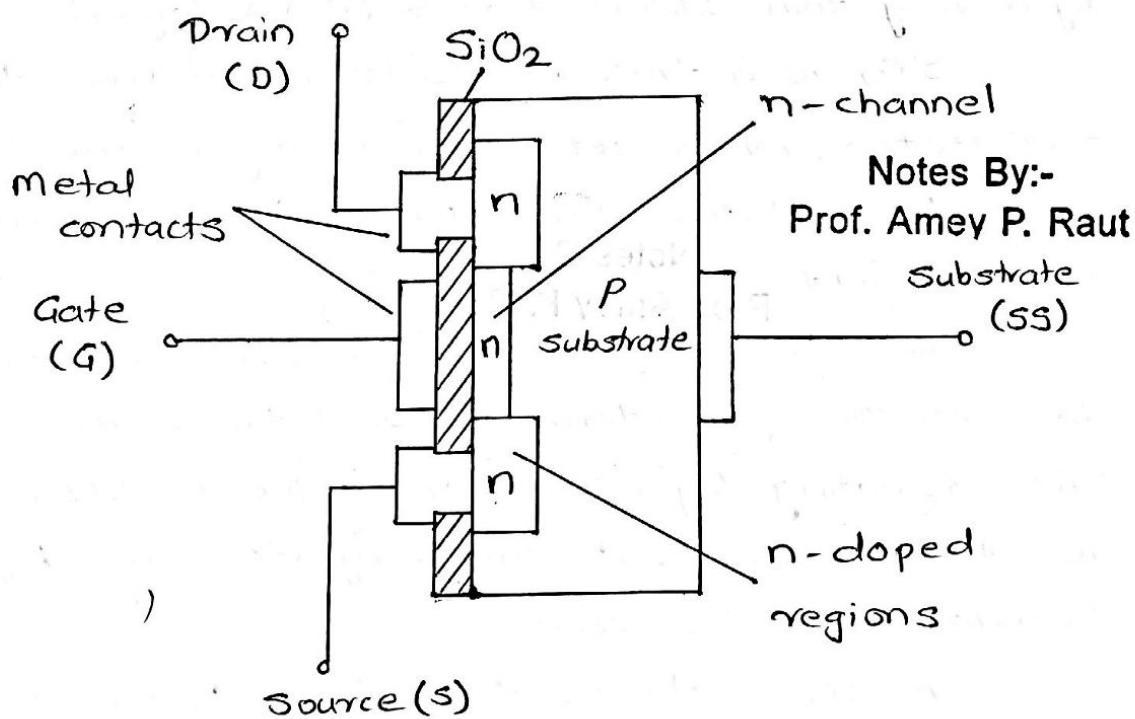


Fig 11

→ Construction

The basic construction of the n-channel depletion-type MOSFET is shown in fig 11.

A slab of p-type material is formed from a silicon base and is referred to as the substrate. It is the foundation on which the device is constructed. In some cases the substrate is internally connected to the source terminal. However, many discrete devices provide an additional terminal labeled SS, resulting in a four-terminal device.

The source and drain terminals are connected through metallic contacts to n-doped regions linked by an n-channel as shown in fig 11.

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The gate is also connected to a metal contact surface but remains insulated from the n-channel by a very thin silicon dioxide (SiO_2) layer.

SiO_2 is a type of insulator referred to as a dielectric, which sets up opposing electric fields within the dielectric when exposed to an externally applied field.

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Thus there is no direct electrical connection between the gate terminal and the channel of MOSFET. The insulating layer of SiO_2 in the MOSFET construction that accounts for the very desirable high input impedance of the device.

MOSFET stands for, metal for the drain, source and gate connections; oxide for the silicon dioxide insulating layer and semiconductor for the basic structure on which the n-and p-type regions are diffused.

→ Basic operation and Characteristics

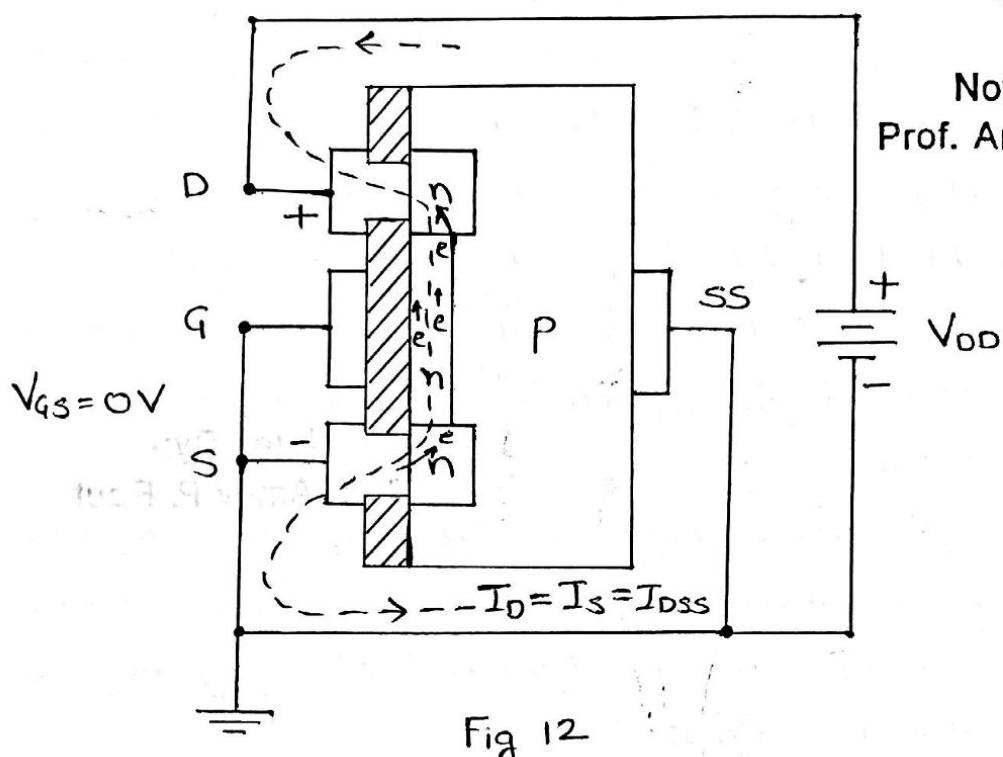


Fig 12

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In fig 12 the gate-to-source voltage is set to 0V by the direct connection from one terminal to the other, and a voltage V_{DD} is applied across the drain-to-source terminals.

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The result is an attraction of the free electrons of the n-channel for the positive voltage at the drain.

The result is a current similar to the flowing in the channel of the JFET, the resulting current with $V_{GS} = 0$ is labeled as I_{DSS} .

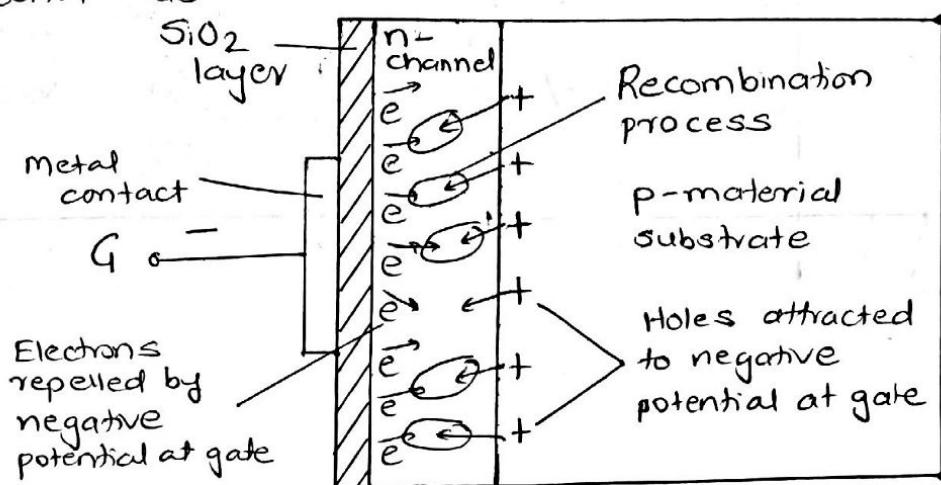


Fig 11

In fig 11 V_{AS} is set at a negative voltage such as $-1V$. The negative potential at the gate will tend to pressure electrons towards the p-type substrate and attract holes from the p-type substrate as shown.

Depending on the magnitude of the negative bias established by V_{AS} , a level of recombination between electrons and holes will occur that will reduce the number of free electrons in the n-channel available for conduction.

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The more negative the bias, the higher is the rate of recombination. The resulting level of drain current is therefore reduced with increasing negative bias of V_{AS} as shown in fig 12.

For $V_{AS} = -1V, -2V$ and so on to the pinch-off level of $-6V$, the resulting levels of drain current and transfer curve are shown in fig 12.

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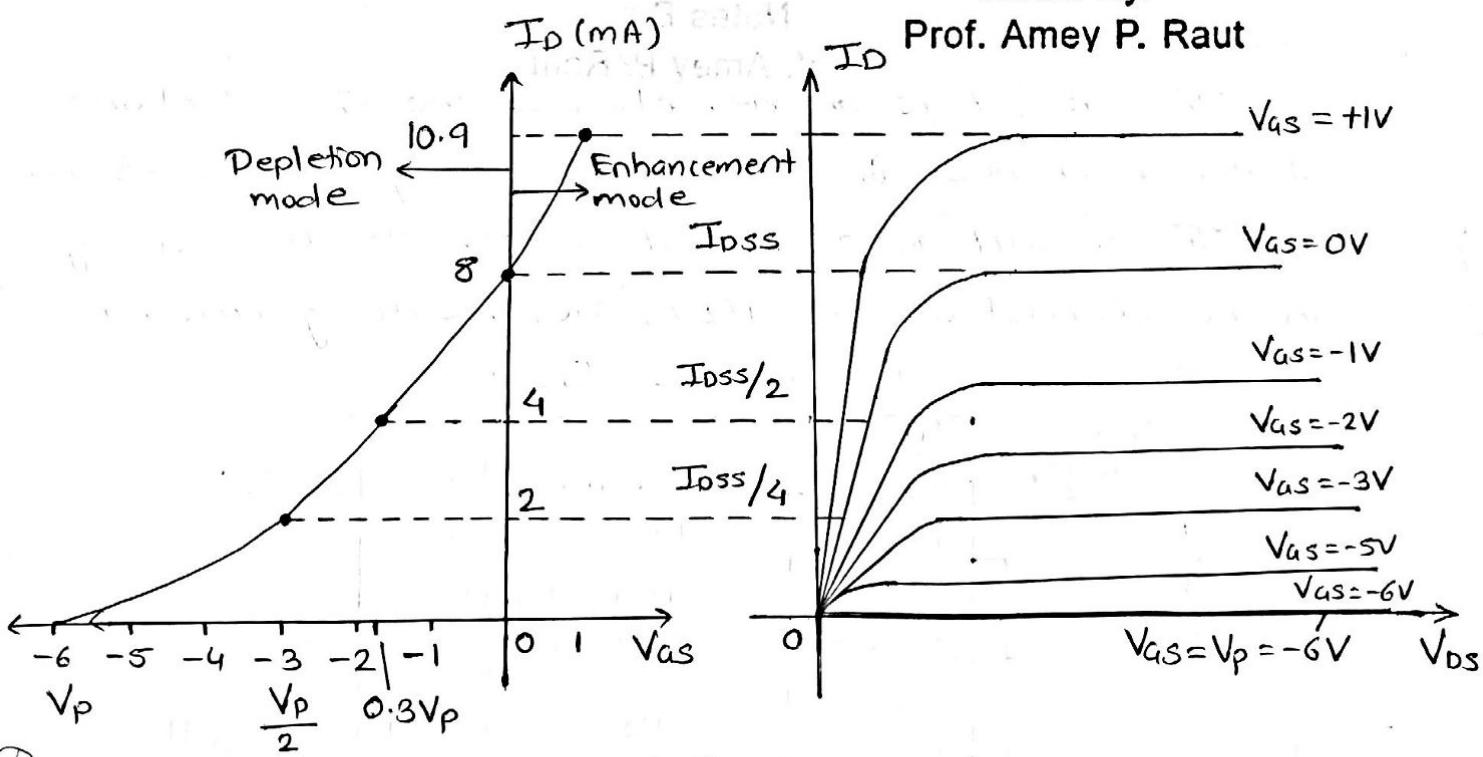


Fig 12

For positive values of V_{GS} , the positive gate will draw additional electrons from the p-type substrate due to the reverse-leakage current and establish new carriers through the collisions resulting between accelerating particles.

As the gate-to-source voltage will increase in the positive direction, the drain current will increase at a rapid rate for the reasons described above.

The application of a positive gate-to-source voltage has "enhanced" the level of free carriers in the channel compared to with $V_{GS} = 0V$. For this reason the region of positive gate voltages on the drain or transfer characteristics is often referred to as the enhancement region.

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The region between cut-off and the saturation level of I_{DS} referred to as the depletion region.

* p-channel Depletion-Type MOSFET

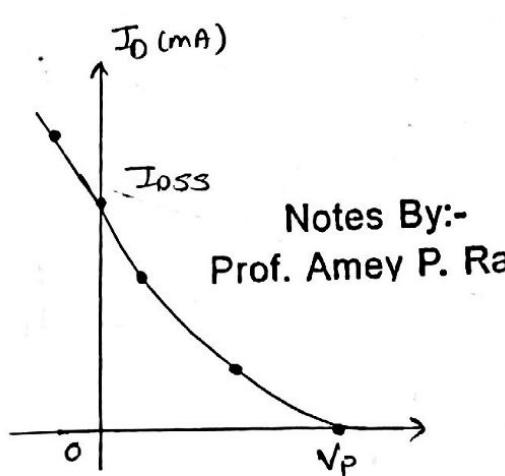
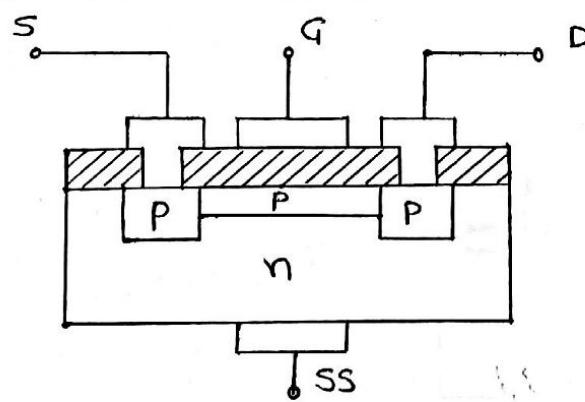
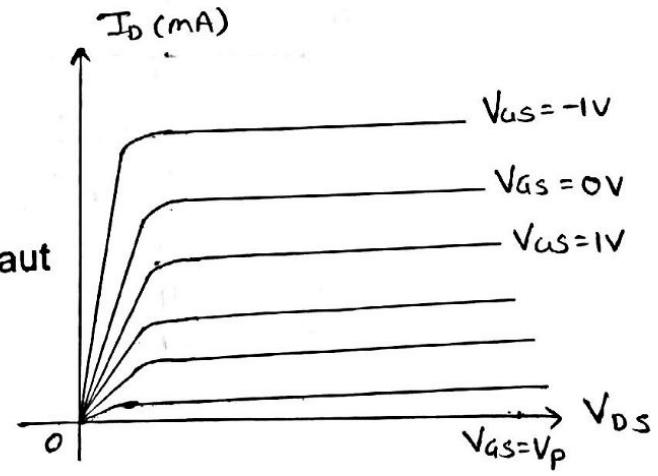


Fig 13



The construction of a p-channel depletion-type MOSFET is exactly the reverse of that of n-channel MOSFET, there is an n-type substrate and a p-type channel as shown in fig 13.

The terminals remain as identified, but all the voltage polarities and the current directions are reversed.

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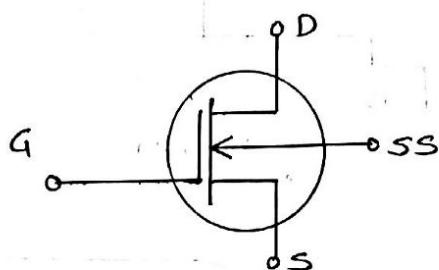
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The drain characteristics would appear exactly as n-channel device, but with V_{DS} having negative values, I_D having positive values, and V_{GS} having the opposite polarities as shown in fig 13.

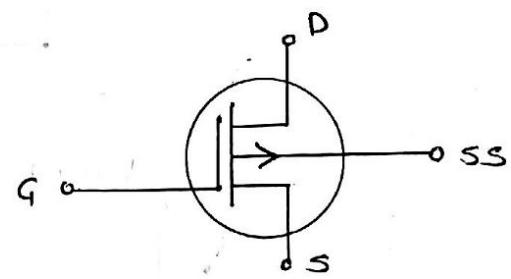
The reversal in V_{GS} will result in a mirror image for the transfer characteristics as shown. In other words the drain current will increase from cut-off at $V_{GS} = V_p$ in the positive V_{GS} region to I_{DSS} and then continue to increase for increasingly negative values of V_{GS} .

* SYMBOLS

n-channel



p-channel



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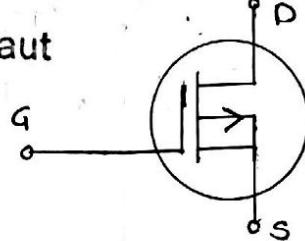
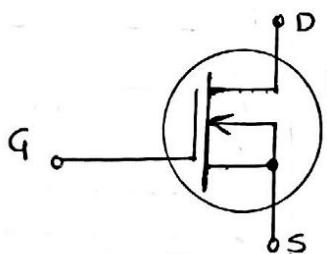


Fig 14

* ENHANCEMENT-TYPE MOSFET:

(21)

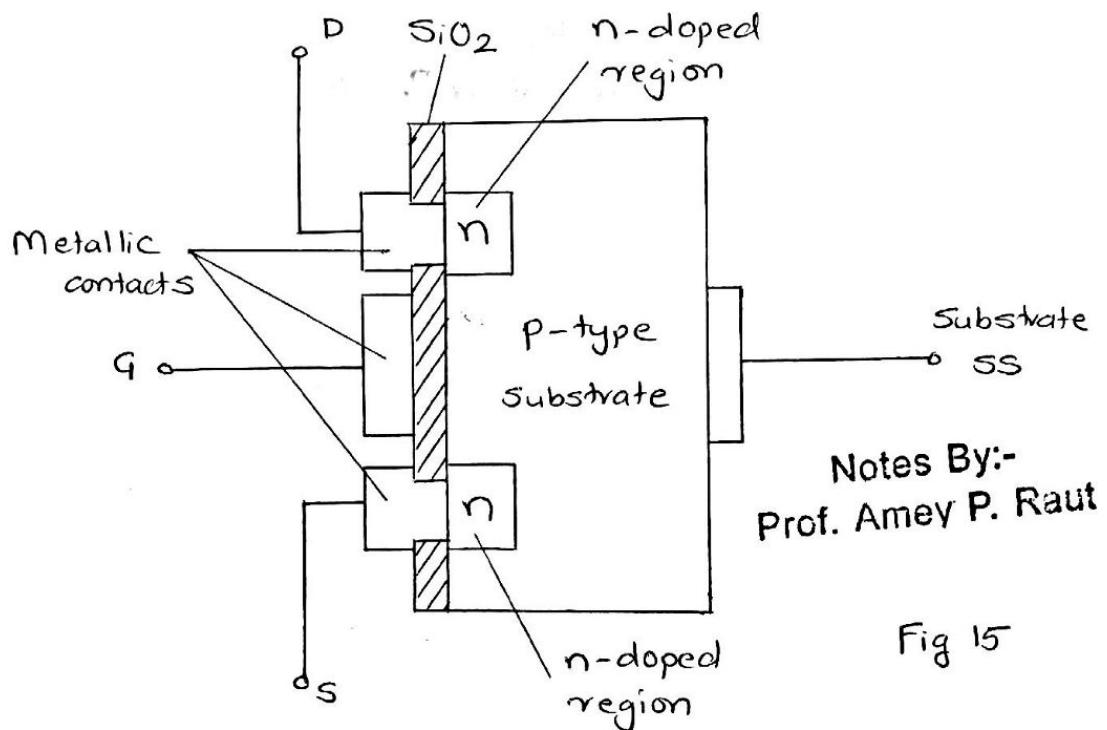


Fig 15

→ Construction

The basic construction of the n-channel enhancement-type MOSFET is provided in fig 15. A slab of p-type material is formed from a silicon base and is referred to as Substrate.

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The substrate is sometimes internally connected to the source terminal or fourth lead is made available for external control of its potential level.

The source and drain terminals are connected through metallic contacts to n-doped regions.

The primary difference between the construction of depletion type and enhancement-type MOSFET is the absence of a channel as a constructed component of the device.

The SiO_2 layer isolates the gate metallic platform from the region between the drain and source, but now it is simply separated from a section of the p-type material.

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→ Basic Operation and Characteristics

If V_{GS} is set at 0V and a voltage applied between the drain and the source of the device, the absence of an n-channel will result in a current of effectively 0A.

With V_{GS} some positive voltage, V_{DS} at 0V, and terminal SS directly connected to the source, there are two reverse-biased p-n junctions between the n-doped regions and the p-substrate to oppose any significant flow between drain and source.

Insulating layer Notes By:-

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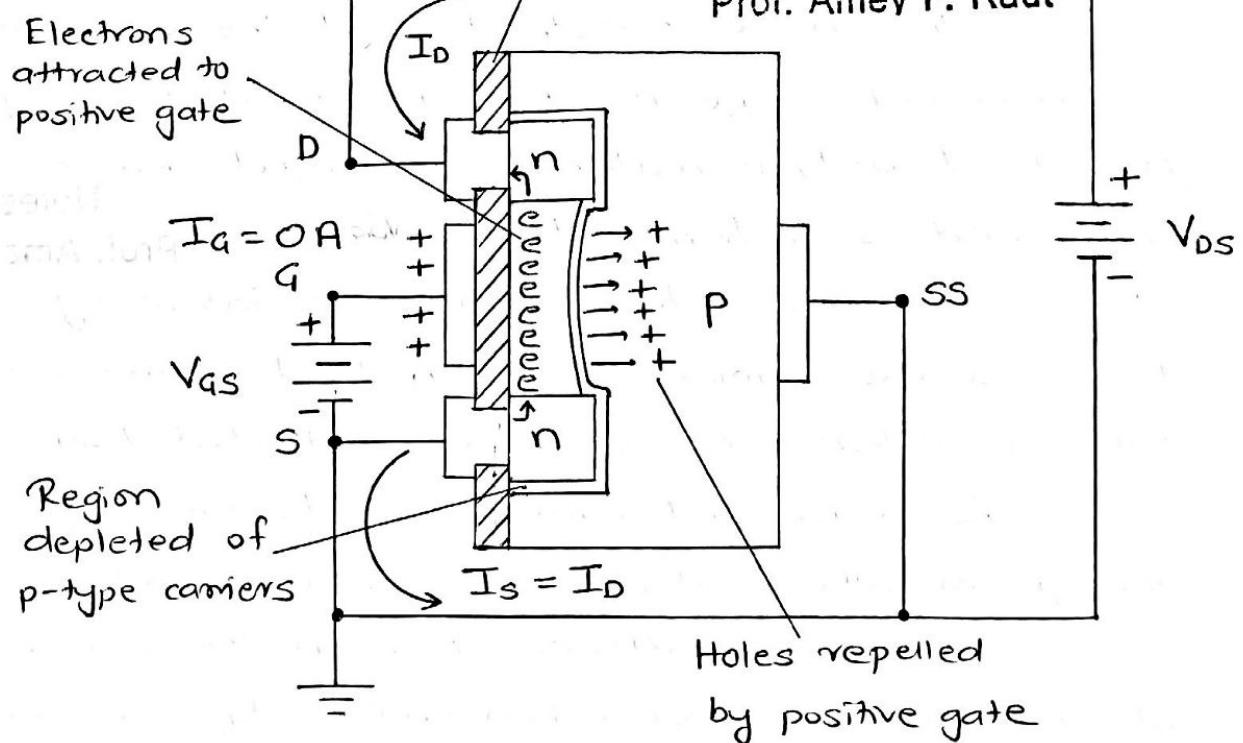


Fig 16

In fig 16 both V_{DS} and V_{GS} have been set at some positive voltage greater than 0V, establishing the drain and the gate at a positive potential with respect to the source.

The positive potential at the gate will pressure the holes in the p-substrate along the edge of the SiO_2 layer to leave the area and enter deeper regions of the p-substrate.

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The result is a depletion region near the SiO_2 insulating layer void of holes.

The electrons in the p-substrate (minority carriers) will be attracted to the positive gate and accumulate in the region near the surface of the SiO_2 layer.

The SiO_2 layer and its insulating qualities will prevent the negative carriers from being absorbed at the gate terminal.

As V_{GS} increases in magnitude, the concentration of electrons near the SiO_2 surface increases until eventually the induced n-type region can support a measurable flow between drain and source.

The level of V_{GS} that results in the significant increase in drain current is called the threshold voltage.

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and is given the symbol V_T .

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Since the channel is non-existent with $V_{GS} = 0V$ and enhanced by the application of a positive gate to source voltage, this type of MOSFET is called an enhancement-type MOSFET.

As V_{GS} is increased beyond the threshold level, the density of free carriers in the induced channel will increase, resulting in an increased level of drain current.

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current.

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However, if we hold V_{GS} constant and increase the level of V_{DS} , the drain current will eventually reach a saturation level.

The levelling off of I_D is due to a pinching-off process depicted by the narrower channel at the drain end of the induced channel as shown in fig 17.

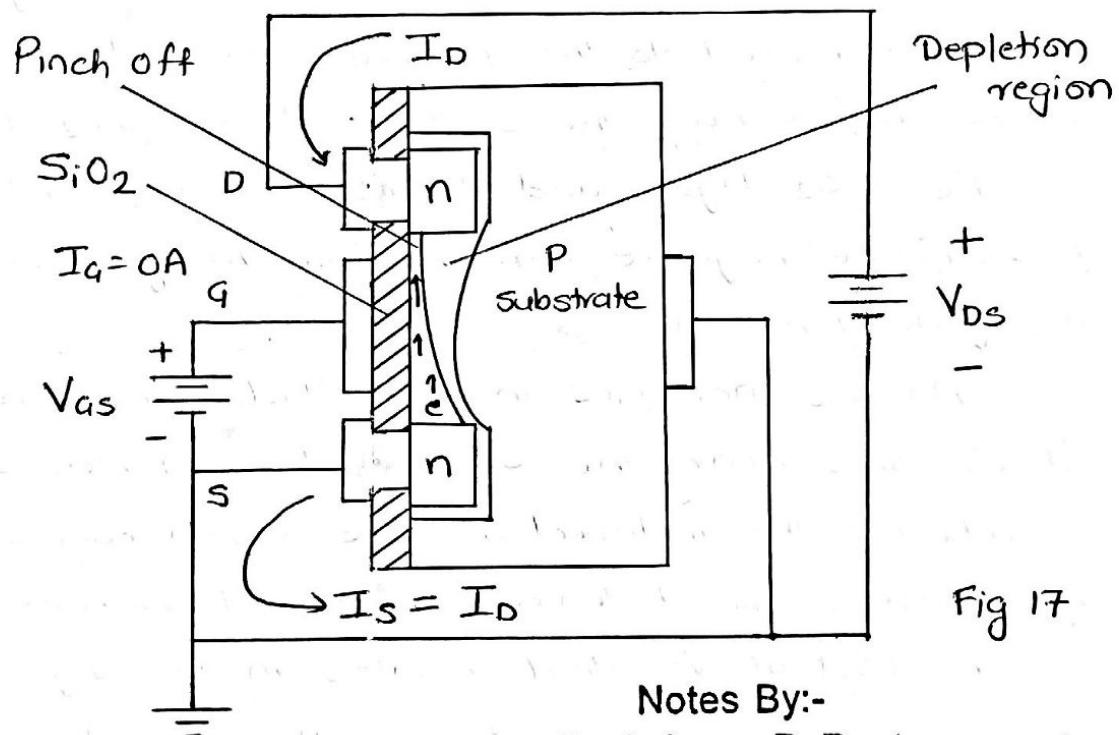


Fig 17

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Applying Kirchhoff's voltage law to the terminal voltages of the MOSFET of fig 17 we get

$$V_{DG} = V_{DS} - V_{GS}$$

If V_{GS} is held fixed at some value and V_{DS} is increased the voltage V_{DG} will increase and the gate will become less and less positive with respect to the drain.

This reduction in gate-to-drain voltage will in turn reduce the attractive forces for free carriers in this region of the induced channel, causing a reduction in the effective channel width.

Eventually, the channel will be reduced to the point of pinch-off and a saturation condition will be established.

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Any further increase in V_{DS} at the fixed value of V_{GS} will not affect the saturation level of I_D until breakdown conditions are encountered.

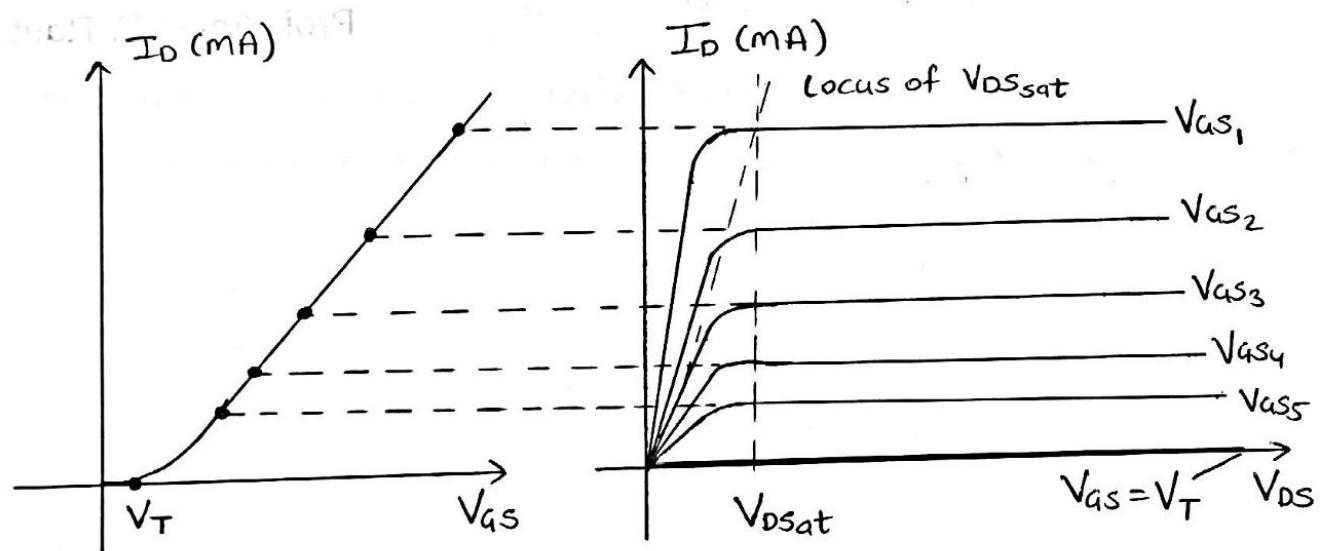


Fig 18

The drain characteristics of fig 18 reveal the saturation level for V_{DS} is related to the level of applied V_{GS} by

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$$V_{DS,sat} = V_{GS} - V_T$$

Therefore, for a fixed value of V_T , the higher the level of V_{GS} , the greater is the saturation level for V_{DS} .

For values of V_{GS} less than the threshold level, the drain current of an enhancement type MOSFET is 0mA.

(26)

For levels of $V_{GS} > V_T$, the drain current is related to the applied gate-to-source voltage by the following non-linear relationship.

$$I_D = K(V_{GS} - V_T)^2$$

The squared term results in the nonlinear relationship between I_D and V_{GS} .

The K term is a constant that is a function of the construction of the device. The value of K can be determined from the following equation

$$K = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_T)^2}$$

Notes By:-
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where $I_{D(\text{on})}$ and $V_{GS(\text{on})}$ are the values for each at a particular point on the characteristics of the device.