1. Description

1.1. Project

Project Name	STM32G431KB_TEST
Board Name	NUCLEO-G431KB
Generated with:	STM32CubeMX 6.3.0
Date	03/14/2023

1.2. MCU

MCU Series	STM32G4
MCU Line	STM32G4x1
MCU name	STM32G431KBTx
MCU Package	LQFP32
MCU Pin number	32

1.3. Core(s) information

Core(s)	ARM Cortex-M4

2. Pinout Configuration
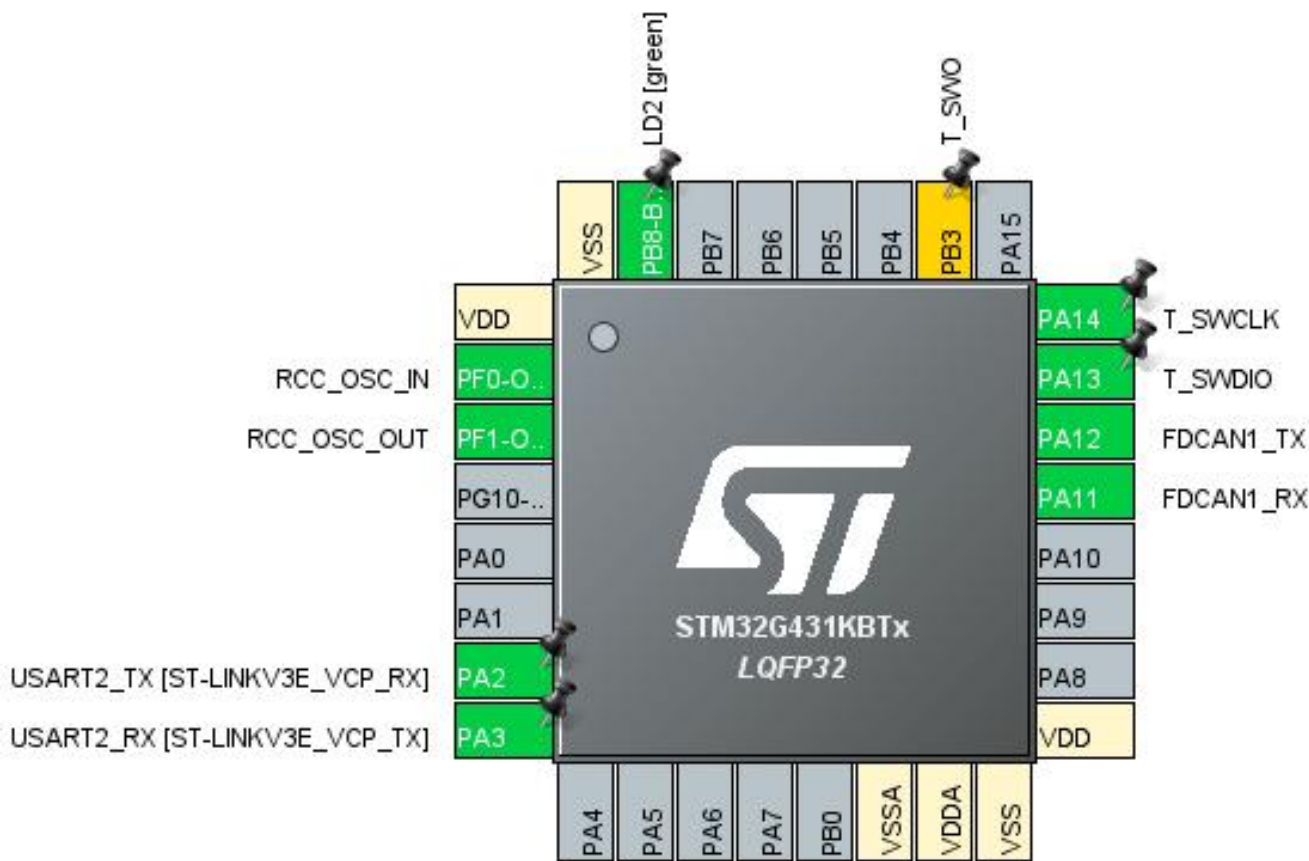
3. Pins Configuration

Pin Number LQFP32	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VDD	Power		
2	PF0-OSC_IN	I/O	RCC_OSC_IN	
3	PF1-OSC_OUT	I/O	RCC_OSC_OUT	
7	PA2	I/O	USART2_TX	USART2_TX [ST-LINKV3E_VCP_RX]
8	PA3	I/O	USART2_RX	USART2_RX [ST-LINKV3E_VCP_TX]
14	VSSA	Power		
15	VDDA	Power		
16	VSS	Power		
17	VDD	Power		
21	PA11	I/O	FDCAN1_RX	
22	PA12	I/O	FDCAN1_TX	
23	PA13	I/O	SYS_JTMS-SWDIO	T_SWDIO
24	PA14	I/O	SYS_JTCK-SWCLK	T_SWCLK
26	PB3 *	I/O	SYS_JTDO-SWO	T_SWO
31	PB8-BOOT0 **	I/O	GPIO_Output	LD2 [green]
32	VSS	Power		

** The pin is affected with an I/O function

 * The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration
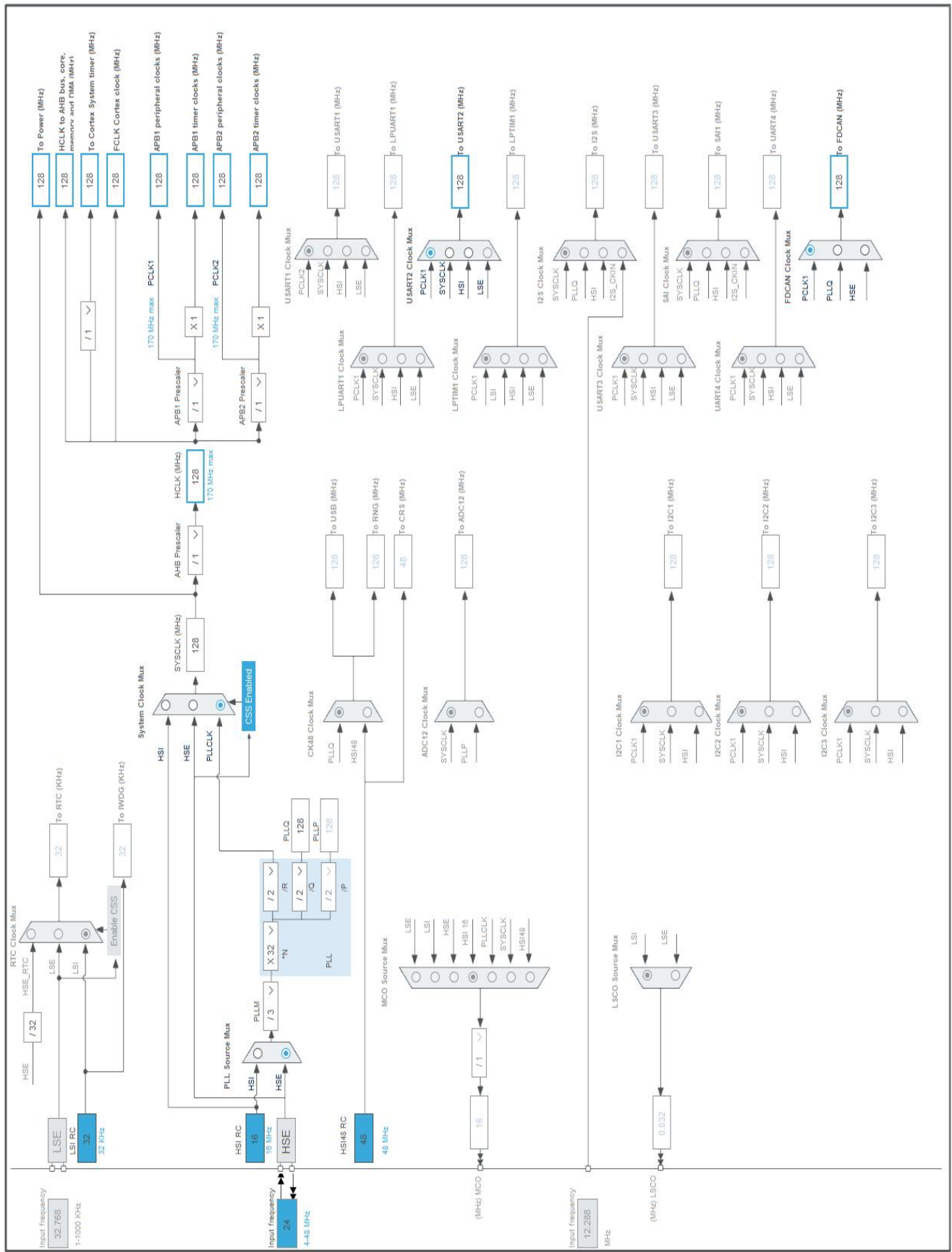
5. Software Project

5.1. Project Settings

Name	Value
Project Name	STM32G431KB_TEST
Project Folder	D:\STM32CubeMX_ws\STM32G431KB_TEST
Toolchain / IDE	EWARM V8.32
Firmware Package Name and Version	STM32Cube FW_G4 V1.4.0
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_DMA_Init	DMA
3	MX_GPIO_Init	GPIO
4	MX_FDCAN1_Init	FDCAN1
5	MX_USART2_UART_Init	USART2

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32G4
Line	STM32G4x1
MCU	STM32G431KBTx
Datasheet	DS12589_Rev0

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP1
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-Boost	NoRange
Fetch Type	FLASH/ART	NA
CPU Frequency	170 MHz	0 Hz
Clock Configuration	HSE BYP PLL	ALL CLOCKS OFF
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	25.5 mA	59 µA
Duration	0.1 ms	0.9 ms
DMIPS	213.0	0.0
Ta Max	124.19	129.99
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	2.6 mA
Battery Life	1 month, 23 days, 22 hours	Average DMIPS	212.5 DMIPS

6.6. Chart

Consumption Profile by Step
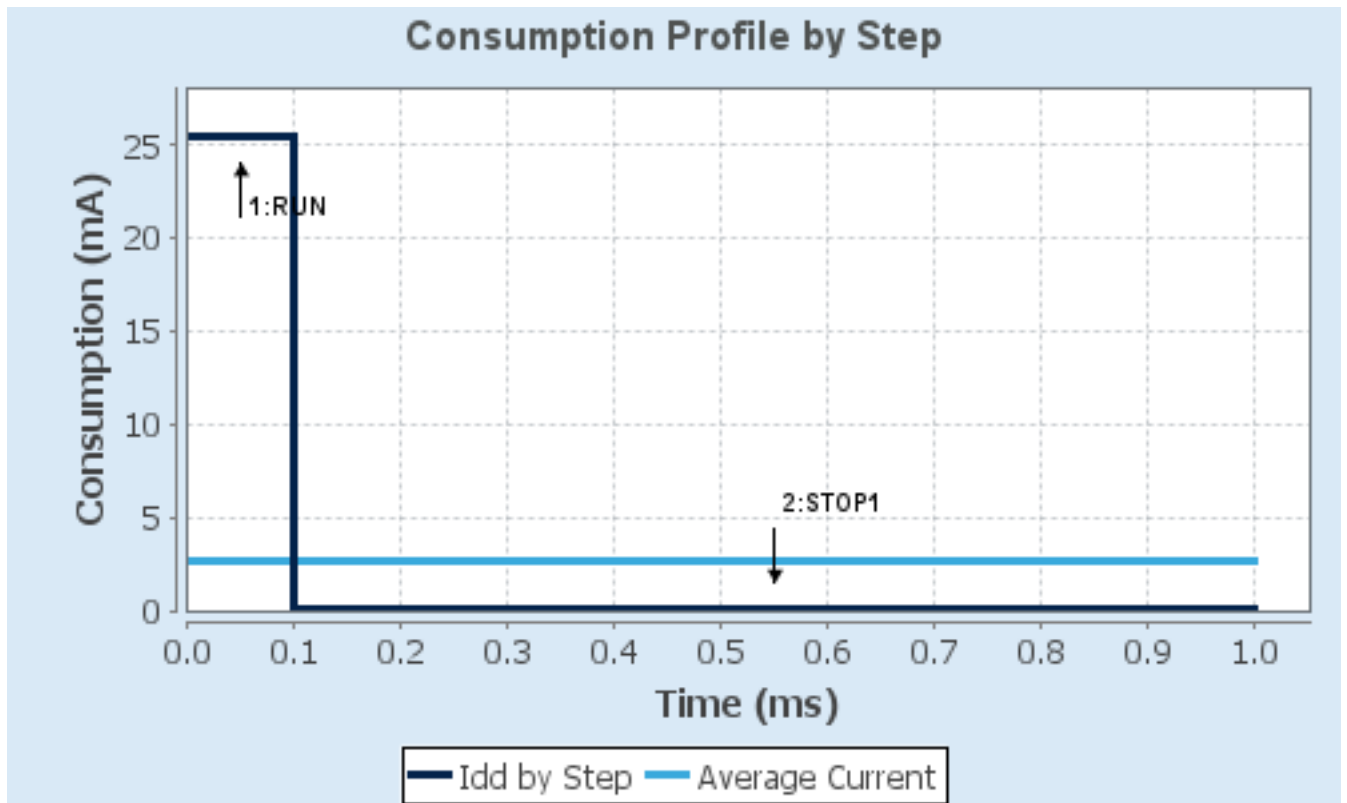
7. Peripherals and Middlewares Configuration

7.1. FDCAN1

mode: Activated

7.1.1. Parameter Settings:

Basic Parameters:

Clock Divider	Divide kernel clock by 1
Frame Format	Classic mode
Mode	Normal mode
Auto Retransmission	Disable
Transmit Pause	Disable
Protocol Exception	Disable
Nominal Prescaler	**8 ***
Nominal Sync Jump Width	1
Nominal Time Seg1	**13 ***
Nominal Time Seg2	2
Data Prescaler	1
Data Sync Jump Width	1
Data Time Seg1	1
Data Time Seg2	1
Std Filters Nbr	**28 ***
Ext Filters Nbr	0
Tx Fifo Queue Mode	FIFO mode

7.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.2.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Disabled
Data Cache	Enabled
Flash Latency(WS)	3 WS (4 CPU cycle)

RCC Parameters:

HSI Calibration Value	64
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale   Power Regulator Voltage Scale 1

Peripherals Clock Configuration:

Generate the peripherals clock configuration   TRUE

7.3. SYS
Debug: Serial Wire
Timebase Source: SysTick
mode: save power of non-active UCPD - deactive Dead Battery pull-up

7.4. USART2
Mode: Asynchronous
7.4.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

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* User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
FDCAN1	PA11	FDCAN1_RX	Alternate Function Push Pull	**Pull-up ***	**Very High ***	
	PA12	FDCAN1_TX	Alternate Function Push Pull	**Pull-up ***	**Very High ***	
RCC	PF0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PF1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	T_SWDIO
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	T_SWCLK
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	USART2_TX [ST-LINKV3E_VCP_RX]
	PA3	USART2_RX	Alternate Function Push Pull	**Pull-up ***	Low	USART2_RX [ST-LINKV3E_VCP_TX]
Single Mapped Signals	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	T_SWO
GPIO	PB8-BOOT0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [green]

8.2. DMA configuration

DMA request	Stream	Direction	Priority
USART2_RX	DMA1_Channel1	Peripheral To Memory	Low
USART2_TX	DMA1_Channel2	Memory To Peripheral	Low

USART2_RX: DMA1_Channel1 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART2_TX: DMA1_Channel2 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel1 global interrupt	true	0	0
DMA1 channel2 global interrupt	true	0	0
FDCAN1 interrupt 0	true	0	0
USART2 global interrupt / USART2 wake-up interrupt through EXTI line 26	true	0	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/38/39/40/41	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
FDCAN1 interrupt 1	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	true
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 channel1 global interrupt	false	true	true
DMA1 channel2 global interrupt	false	true	true
FDCAN1 interrupt 0	false	true	true
USART2 global interrupt / USART2 wake-up interrupt through EXTI line 26	false	true	true

* User modified value

9. System Views

9.1. Category view

9.1.1. Current

Middleware

System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing	Utilities
DMA ✓			FDCAN1 ✓				
GPIO ⚠			USART2 ✓				
NVIC ✓							
RCC ✓							
SYS ✓							

10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00507199.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00355726.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00502298.pdf
Application note	http://www.st.com/resource/en/application_note/CD00160362.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00074240.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00083249.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00151811.pdf
Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note	http://www.st.com/resource/en/application_note/DM00311483.pdf
Application note	http://www.st.com/resource/en/application_note/DM00355687.pdf
Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note	http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note	http://www.st.com/resource/en/application_note/DM00442716.pdf
Application note	http://www.st.com/resource/en/application_note/DM00442720.pdf

Application note   http://www.st.com/resource/en/application_note/DM00493651.pdf
Application note   http://www.st.com/resource/en/application_note/DM00535045.pdf
Application note   http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note   http://www.st.com/resource/en/application_note/DM00605707.pdf
Application note   http://www.st.com/resource/en/application_note/DM00607955.pdf
Application note   http://www.st.com/resource/en/application_note/DM00610467.pdf
Application note   http://www.st.com/resource/en/application_note/DM00625282.pdf
Application note   http://www.st.com/resource/en/application_note/DM00625700.pdf
Application note   http://www.st.com/resource/en/application_note/DM00725181.pdf