Sound Analysis, Synthesis and Processing

Fourth Homework

Report

Wave Digital Filters

Students

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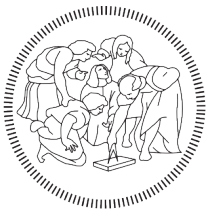

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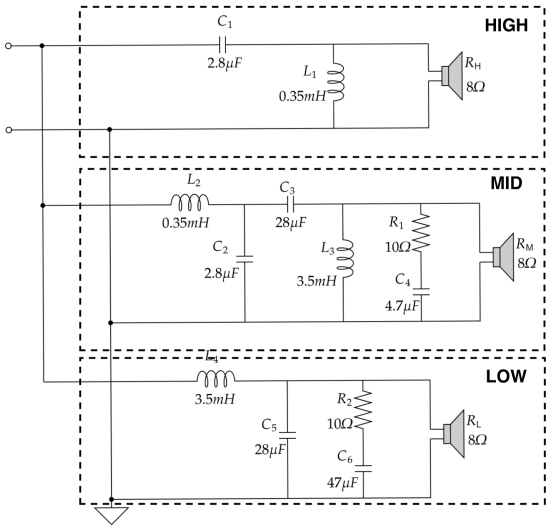

Figure 1: Circuit scheme

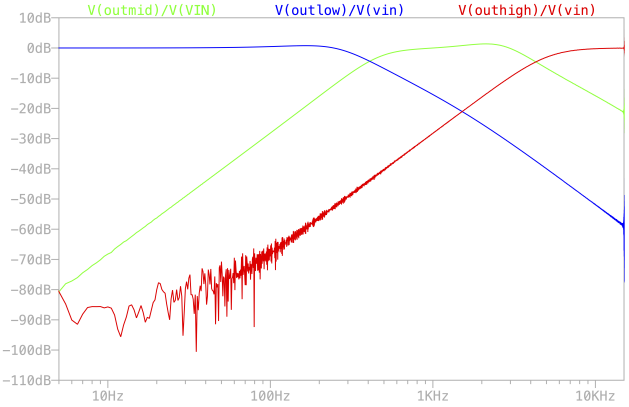

Figure 2: Frequency Response of the system

Introduction

Given a 3-way passive analog crossover filter, represented in figure 1, its circuit is modelled in the *Wave Digital Filter Domain* and then its properties are tested. The frequency response of the system with respect to the input provided are simulated using `LTspice` and represented in figure 2. The time responses of the three subcircuits generated through the `LTspice` simulation are saved into audio files and used as references to compute the error for the *WDF* implementation presented in the next section.

WDF implementation

In the *wave digital filter* derivation (figure 3) of the analog circuit (figure 1), Kirchhoff variables in the discrete-time domain at one port of an element are expressed in terms of wave variables as:

$$i[k] = \frac{a[k] - b[k]}{2Z[k]} \tag{1}$$

$$v[k] = \frac{a[k] + b[k]}{2} \tag{2}$$

Where $a[k]$ is the incident wave and $b[k]$ is the reflected wave to the element considered. $Z[k]$ is the reference port resistance.
One port elements are mapped and adapted from their constitutive equation as in table 1, using the *Trapezoidal Rule* for time derivative approximations.

Constitutive Equations	**Wave Mapping**	**Adaptation Conditions**
$v(t) = V_g(t) + R_g i(t)$	$b[k] = V_g[k]$	$Z[k] = R_g$
$v(t) = Ri(t)$	$b[k] = 0$	$Z[k] = R$
$i(t) = C\frac{dv(t)}{dt}$	$b[k] = a[k-1]$	$Z[k] = \frac{T_s}{2C}$
$v(t) = L\frac{di(t)}{dt}$	$b[k] = -a[k-1]$	$Z[k] = \frac{2L}{T_s}$

Table 1: Mapping of linear one-port elements

Instead, the ideal voltage source is mapped into the WD model as:

$$b[k] = 2V_{in}[k] - a[k] \tag{3}$$

where V_{in} is an exponential sine sweep that is defined as [1]:

$$V_{in}(t) = sin\left(\frac{2\pi f_1 T_{end}}{ln\frac{f_2}{f_1}}\left(exp\left(\frac{t}{T_{end}}ln\frac{f_2}{f_1}\right) - 1\right)\right)$$

The initialization parameters for V_{in} are $f_1 = 5\ Hz$, $f_1 = 15\ kHz$, $T_{end} = 1.99\ s$.
The scattering relation of the generator cannot be adapted. This means that it must be placed as root of the *WD topological tree* and it must be computed at every cycle at the end of the *Forward Scan* after the combination all the other waves in the circuit. In order to build the *WD topological tree* it is necessary to define junctions that connect together all the elements in parallel and in series. Incident and reflected waves at each junction are related through a Scattering matrix **S**, that can be derived from the application of *Kirchoff Voltage Law* and *Kirchoff Current Law* respectively at series and parallel.
For the purpose of this homework it is assumed the point of view of the junction to define incident and reflected wave. Therefore the waves defined as b_n are the waves reflected from the n-th junction, while a_n are the waves incident from the n-th junction. This choice allows a simpler and unambiguous formulation of the wave in the circuit. This requires to swap $a[k]$ and $b[k]$ in equations (1) (2) (3) and in table 1.
In this case only a 3-port junction was used, so the

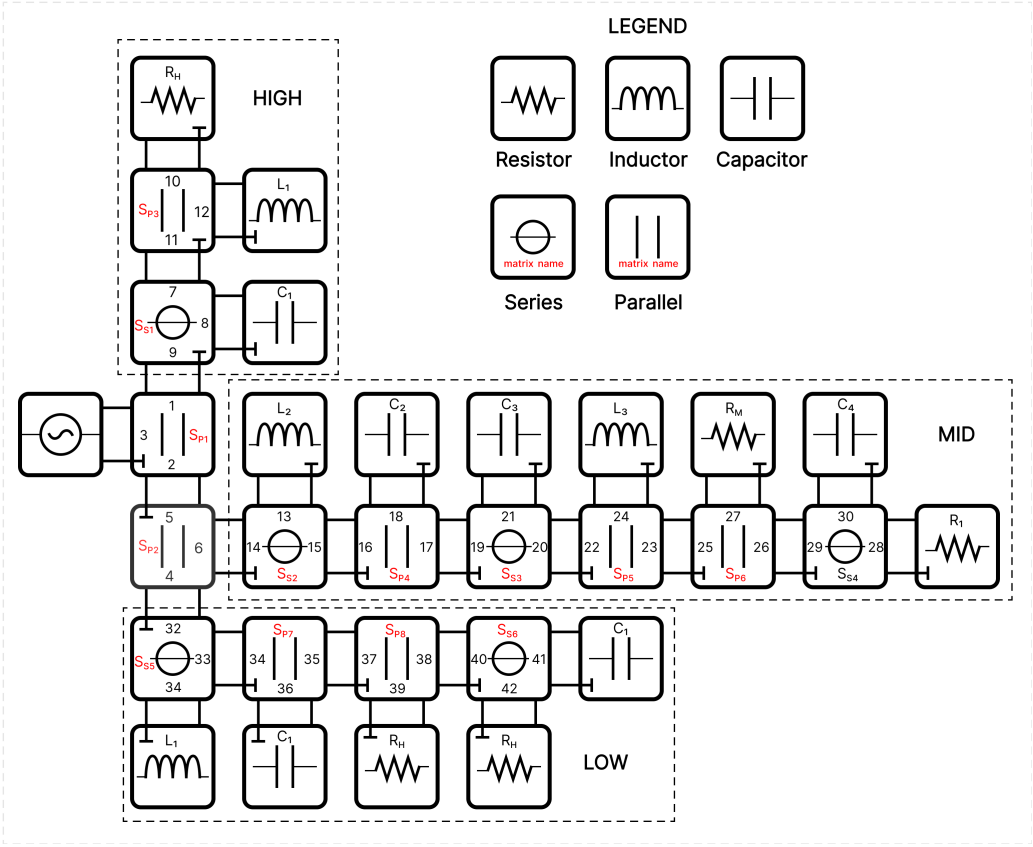

Figure 3: Circuit WD Domain

scattering relation is:

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \end{bmatrix} = \mathbf{S} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \end{bmatrix} \tag{4}$$

where the matrix $\mathbf{S}$ for the series is:

$$\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} - \frac{2}{\sum_{n=1}^{3} Z_n} \begin{bmatrix} Z_1 \\ Z_2 \\ Z_3 \end{bmatrix} \begin{bmatrix} 1 & 1 & 1 \end{bmatrix} \tag{5}$$

and for the parallel:

$$\frac{2}{\sum_{n=1}^{3} G_n} \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \begin{bmatrix} G_1 & G_2 & G_3 \end{bmatrix} - \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{6}$$

Ports can be made reflection-free by setting the following relations:

Series:

$$Z_q = \sum_{n=1, n\neq q}^{3} Z_n \tag{7}$$

Parallel:

$$G_q = \sum_{n=1, n\neq q}^{3} G_n \tag{8}$$

Following the scheme in figure 3 all the impedances values are assigned as:

Resistance adaptation:

$$Z_{28} = R_1 \quad Z_{42} = R_2$$
$$Z_{10} = RspkHigh \quad Z_{27} = RspkMid$$
$$Z_{39} = RspkLow$$

Condenser adaptation:

$$Z_9 = \frac{T_s}{2C_1} \quad Z_{18} = \frac{T_s}{2C_2}$$
$$Z_{21} = \frac{T_s}{2C_3} \quad Z_{30} = \frac{T_s}{2C_4}$$
$$Z_{36} = \frac{T_s}{2C_5} \quad Z_{41} = \frac{T_s}{2C_6}$$

Inductors adaptation:

$$Z_{12} = \frac{2L_1}{T_s} \quad Z_{13} = \frac{2L_2}{T_s}$$
$$Z_{24} = \frac{2L_3}{T_s} \quad Z_{31} = \frac{2L_4}{T_s}$$

Series and Parallels nodes

HIGH:

$$Z_{11} = \frac{Z_{10} \cdot Z_{12}}{Z_{10} + Z_{12}} \quad Z_7 = Z_{11}$$

$$Z_8 = Z_7 + Z_9$$

MID:

$$\begin{aligned} Z_{29} &= Z_{28} + Z_{30} \quad & Z_{26} &= Z_{29} \\ Z_{25} &= \frac{Z_{26} \cdot Z_{27}}{Z_{26} + Z_{27}} \quad & Z_{23} &= Z_{25} \\ Z_{22} &= \frac{Z_{23} \cdot Z_{24}}{Z_{23} + Z_{24}} \quad & Z_{20} &= Z_{22} \\ Z_{19} &= Z_{20} + Z_{21} \quad & Z_{17} &= Z_{19} \\ Z_{16} &= \frac{Z_{17} \cdot Z_{18}}{Z_{17} + Z_{18}} \quad & Z_{15} &= Z_{16} \\ Z_{14} &= Z_{13} + Z_{15} \end{aligned}$$

LOW:

$$\begin{aligned} Z_{40} &= Z_{41} + Z_{42} \quad & Z_{38} &= Z_{40} \\ Z_{37} &= \frac{Z_{38} \cdot Z_{39}}{Z_{38} + Z_{39}} \quad & Z_{35} &= Z_{37} \\ Z_{34} &= \frac{Z_{36} \cdot Z_{37}}{Z_{36} + Z_{37}} \quad & Z_{33} &= Z_{34} \\ Z_{32} &= Z_{31} + Z_{33} \end{aligned}$$

Main circuit impedances:

$$\begin{aligned} Z_1 &= Z_8 \quad & Z_4 &= Z_{32} \\ Z_6 &= Z_{14} \quad & Z_5 &= \frac{Z_4 \cdot Z_6}{Z_4 + Z_6} \\ Z_2 &= Z_5 \quad & Z_3 &= \frac{Z_1 \cdot Z_2}{Z_1 + Z_2} \end{aligned}$$

Once these values were computed it was possible to begin the *forward scan*, starting from the leaves towards the root. The waves from the adapted elements were first computed, then the waves from the near junction could be computed and so on through the graph. Once arrived at the ideal voltage source, its wave is computed as stated by the equation (3).
At this point the tree is walked again in the *backward scan* process until the leaves are reached. Doing so it's possible to digitally model the analog circuit and then obtain the output signals $V_{outHigh}, V_{outMid}, V_{outLow}$ as the voltage across R_H, R_M, R_L resistors.

Q1) Simulation accuracy

Considering the output values and the different errors for the three subcircuits, represented in figure 4, we can notice how the main difference between the three in terms of errors is caused by the frequency range in which the single circuit operates. As a matter of fact the *low-frequencies subcircuit* operates in a range below 400 Hz, the *mid-frequencies subcircuit* operates in a range approximately from 400 Hz to 5000 Hz, and the *high-frequencies subcircuit* works above 5000 Hz. The two cut-off frequencies for the subcircuits are acquired evaluating the frequency response from the `LTspice` simulation in figure 2, where the results are computed at the same sampling frequency of the ones used for the `LTspice` simulation. Therefore the overall error amplitude results to be the lowest for the *low-frequencies subcircuit*, and the highest for the *high-frequencies subcircuit*. This behaviour is caused by the frequency warping which happens due to the discretization method used to map the *Laplace domain* into the *Z-domain*. In the specific the method used, as discussed in the previous section, is the *Trapezoidal Rule*

$$s \leftarrow \frac{2}{T_s} \frac{1 - z^{-1}}{1 + z^{-1}} \tag{9}$$

where the *Laplace* variable as a combination of the Z variable. Considering now the frequency domain the mapping results to be:

$$j\omega \leftarrow \frac{2}{T_s} \frac{e^{j\tilde{\omega}T_s} - 1}{e^{j\tilde{\omega}T_s} + 1} \tag{10}$$

with $j\omega = s$ and $e^{j\tilde{\omega}T_s} = z$, the previous formulation can be simplified as

$$j\omega \leftarrow \frac{2}{T_s} \tan\left(\tilde{\omega}\frac{T_s}{2}\right) \tag{11}$$

from this formulation we derive that ω is very close to $\tilde{\omega}$ at low frequencies, while the difference is enhanced at high frequencies.

Q2) Sampling Frequency variation

Recalling the relation between $j\omega$ continuous frequency and $j\tilde{\omega}$ discrete frequency stated in equation (11) of the previous section, we can understand how increasing the sampling frequency for the discretized frequency allows make the difference between ω and $\tilde{\omega}$ negligible in the whole frequency range of interest. The results of the different sampling frequency are visible in figure 5, 6, 7.

Q3) Circuit variation

Now a slight variation on the circuit presented in figure 1 is considered and shown in figure 8, specifically a diode D_1 is added in parallel to the tweeter resistor R_H.

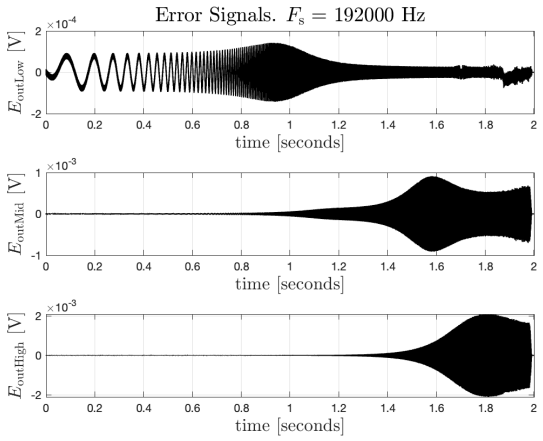

Figure 4: Error between ground truth signal and output signal

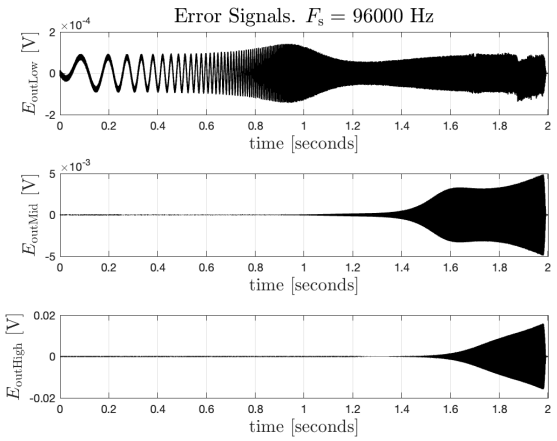

Figure 5: Error between ground truth signal and output signal $F_s = 96kHz$

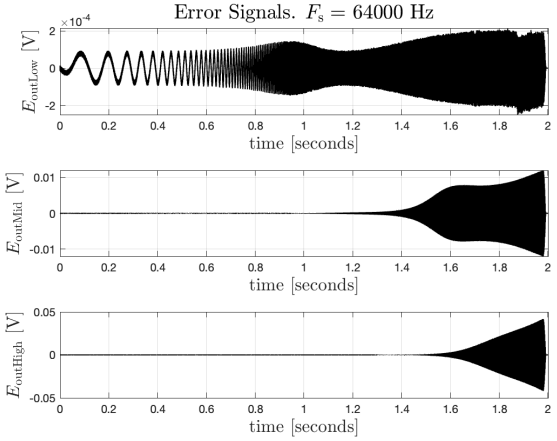

Figure 6: Error between ground truth signal and output signal $F_s = 64kHz$

Being the diode a non-linear electronic component, its constitutive equation can be modelled and solved in a

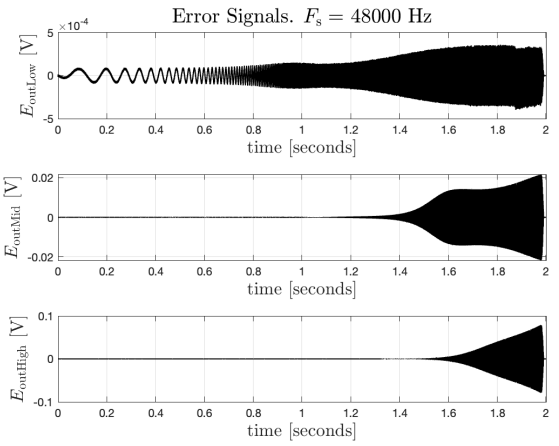

Figure 7: Error between ground truth signal and output signal $F_s = 48kHz$

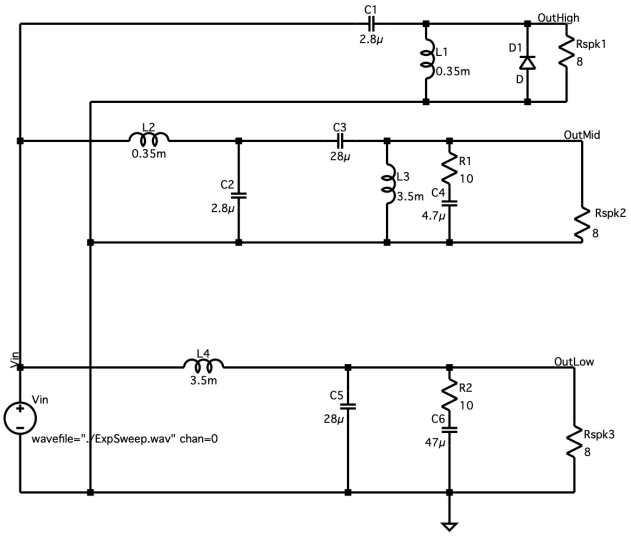

Figure 8: Circuit scheme with added diode

closed form rewriting its constitutive equation by means of *incident* and *reflected* wave as

$$b[k] = a[k] + Z[k] I_s = 2\eta V_{th} W\left(\frac{Z[k] I_s}{\eta V_{th}} e^{\frac{Z[k] I_S + a[k]}{\eta V_{th}}}\right)$$

This form presents a direct relations between the two waves at the same instant k. The addition of this component introduces two *non-linear* components in the circuit. Hence, the solution must be computed using iterative solvers. In this case, the simpler method that has been used up until this point cannot be implemented.

Diode and real voltage source implementation

The ideal voltage source considered in the previous sections is now replaced with a resistive voltage source, modeled as the series between an ideal voltage source and a resistor. The circuit modelling is present in figure

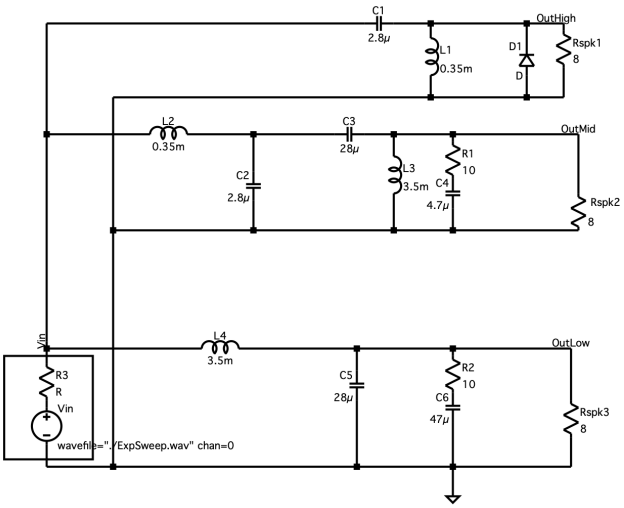

Figure 9: Circuit scheme with added diode and real voltage source

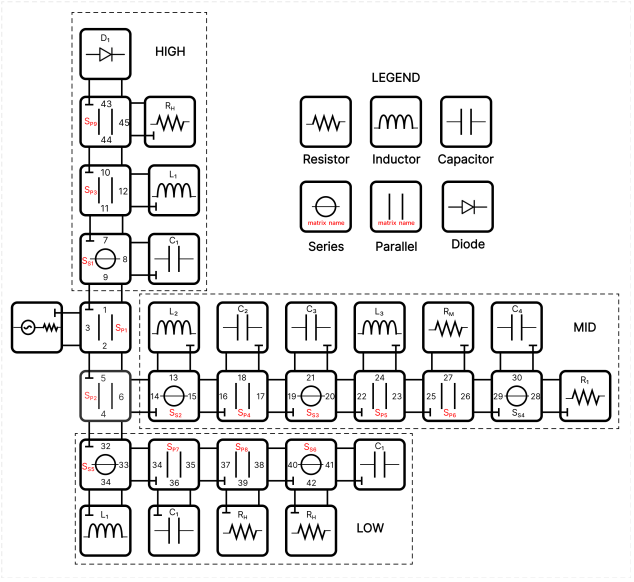

Figure 10: Circuit Diode WD Domain

9. The resistive voltage source component can be modelled in *Wave Digital Filters* domain as a single linear *Wave Digital One-Port* component whose parameters are listed in the first row of Table 1. Considering the *Wave Mapping* equation below

$$b\,[k] = V_g\,[k] \tag{12}$$

We can notice how there is no direct dependence between the reflected and incident wave of the component thanks to the linearity of the component obtained with the application of the resistance to the circuit. Therefore the only non-linear component in the circuit is the diode and the generated *WDF* tree can be represented positioning the diode as the root of the tree and the linear components as leaves, so that it is directly solvable using the techniques considered in the previous sections. In figure 10 a possible *WD topological tree* solution is presented, considering the non-linear element as the root.

Q4) Different discretization technique

The constitutive equation of an inductor in the continuos time domain is:

$$v(t) = L\frac{di(t)}{dt} \tag{13}$$

Which can be written in the Laplace domain:

$$V(s) = sLI(s) \tag{14}$$

From this formulation, applying the Backward Euler Method to approximate derivatives, with this mapping:

$$s \leftarrow \frac{1 - z^{-1}}{T_s} \tag{15}$$

the discrete-time version is obtained:
substituting (15) into (14), the equation

$$V(z) = \frac{1 - z^{-1}}{T_s} LI(z) \tag{16}$$

is then transformed into discrete domain where z^{-1} is seen as a delay of $[k-1]$ with respect to the k-th sample.

$$v[k] = \frac{L}{T_s} i[k] - \frac{L}{T_s} i[k-1] \tag{17}$$

From the general formula of a constitutive equation:

$$v[k] = R_e[k]i[k] + V_e[k] \tag{18}$$

the resistance parameter $R_e[k]$ and the voltage bias parameter $V_e[k]$ take on these values:

$$R_e[k] = \frac{L}{T_s} \tag{19}$$

$$V_e[k] = -\frac{L}{T_s} i[k-1] \tag{20}$$

Combining equations (1) and (2) into (18) it results in the non-adapted scattering relation in the WD domain:

$$b[k] = -\frac{L}{ZT_s + L}(a[k-1] - b[k-1]) - a[k]\left(\frac{ZT_s - L}{ZT_s + L}\right)$$

The adaptation eliminates the instantaneous dependency of $b[k]$ from $a[k]$ and it's value is :

$$b[k] = -\frac{1}{2}(a[k-1] - b[k-1]) \tag{21}$$

that is obtained, setting:

$$b[k] = V_e[k] \quad with \quad Z[k] = R_e = \frac{L}{T_s}$$

In table 2 there's a summary of the obtained results.

Constitutive Equations	**Wave Mapping in Case of Adaptation**	**Adaptation Conditions**
$v(t) = L\frac{di(t)}{dt}$	$b[k] = -\frac{1}{2}(a[k-1] - b[k-1])$	$Z[k] = \frac{L}{T_s}$

Table 2: WD Inductor Model based on Backward Euler Method

References

[1] A. Farina, *Advancements in impulse response measurements by sine sweeps*, Journal of The Audio Engineering Society, (2007).