



# Lessons Learned from Automated Analysis of Industrial SW for 15 Year

Moonzoo Kim

Software Testing and Verification Group  
KAIST, South Korea



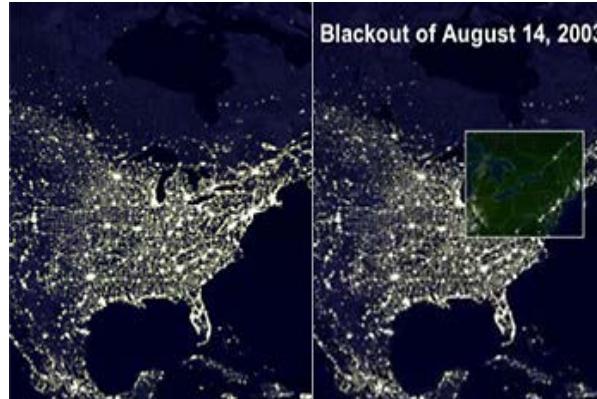
<http://swtv.kaist.ac.kr>

*Thanks to Hotae Kim, Youil Kim, Sacheon Park, Yoonkyu Jang, Dongju Lee, Yunseok Choi,  
Joohyun Lee, Junki Baek and more @ IT industry in South Korea*

# Part I: Motivation of Applying Formal Techniques to Industries

## Social and Economic Loss due to High Complexity of SW

Although most areas of modern society depend on SW,  
**reliability of SW** is not improved much due to its **high complexity**



### (1980s) Medical accident: Therac 25

- For 1985-1987, excessive radio reactive beam enforced.
- **6 persons died due to the problem**
- Data race bug was the cause of the problem

### (2003) US & Canada Blackout

- 7 states in US and 1 state in Canada suffered 3 days electricity blackout
- Caused by the failures of MISO monitoring SW
- **50 million people** suffered and economic loss of **6 billion USD**

### (2010s) Toyoda SUA (sudden unintended acceleration)

- **Dozens of people died** since 2002
- SW bugs detected in 2012
- Fined **1.2 billion USD** in 2014



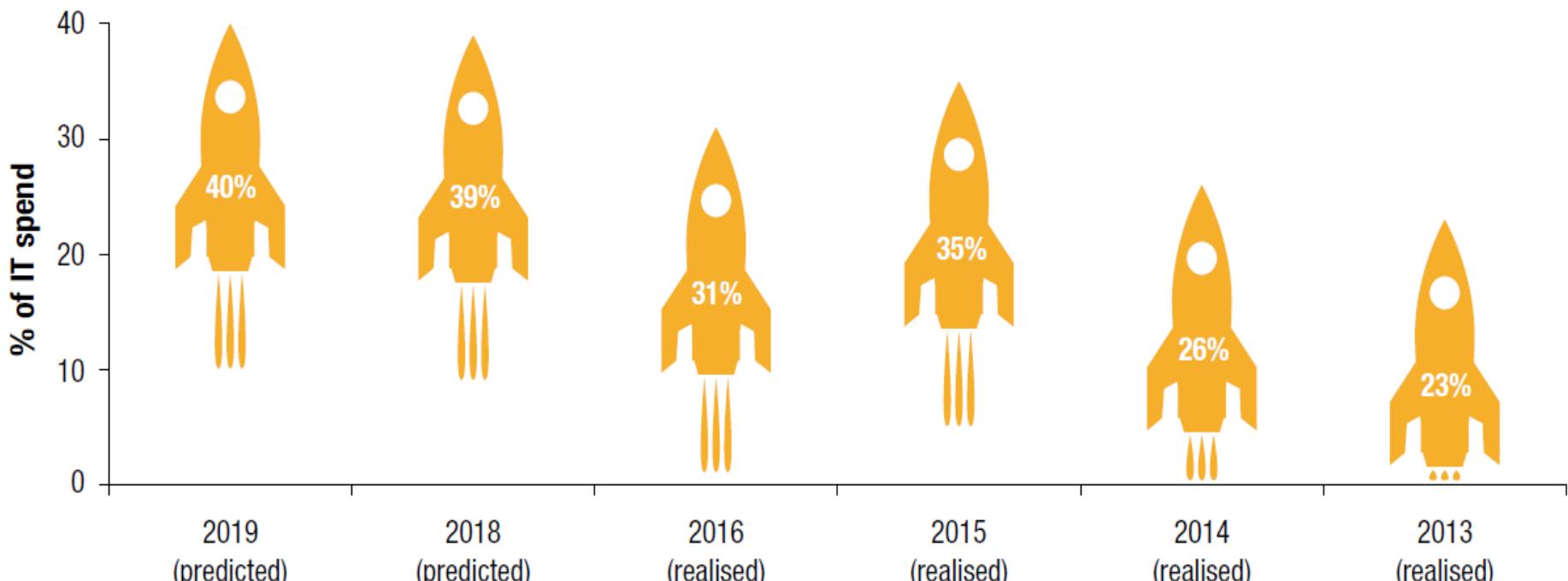
# SW Testing is a Complex and Challenging task!!!

Object-Oriented Programming, Systems Languages, and Applications, Seattle, Washington, November 8, 2002

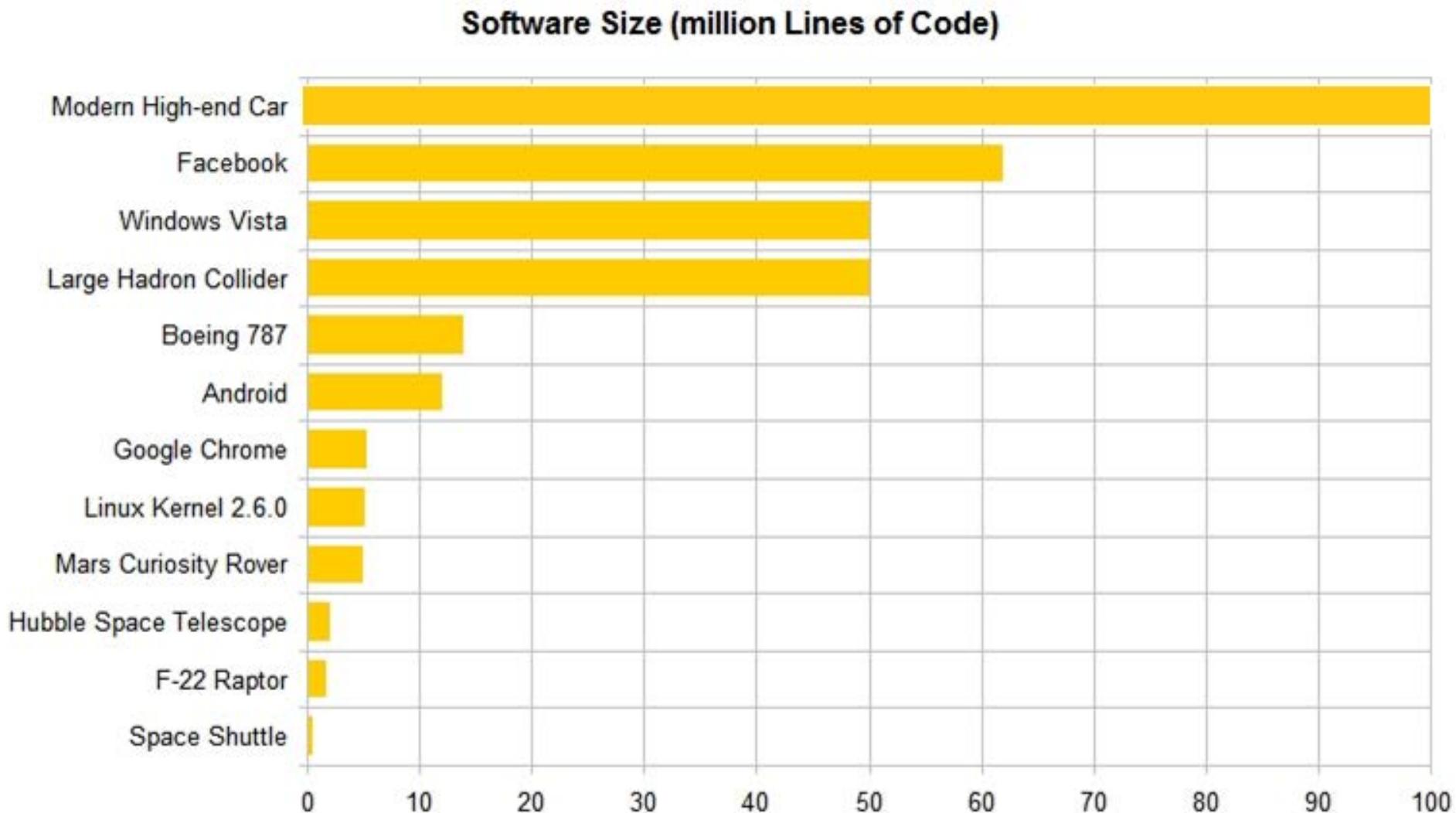
- “... When you look at a big commercial software company like Microsoft, there's actually as much testing that goes in as development. We have as many testers as we have developers. Testers basically test all the time, and developers basically are involved in the testing process about half the time...”
- “... We've probably changed the industry we're in. We're not in the software industry; we're in the testing industry, and writing the software is the thing that keeps us busy doing all that testing.”
- “...The test cases are unbelievably expensive; in fact, there's more lines of code in the test harness than there is in the program itself. Often that's a ratio of about **three to one**.”

# SW Verification & Testing Market Trends

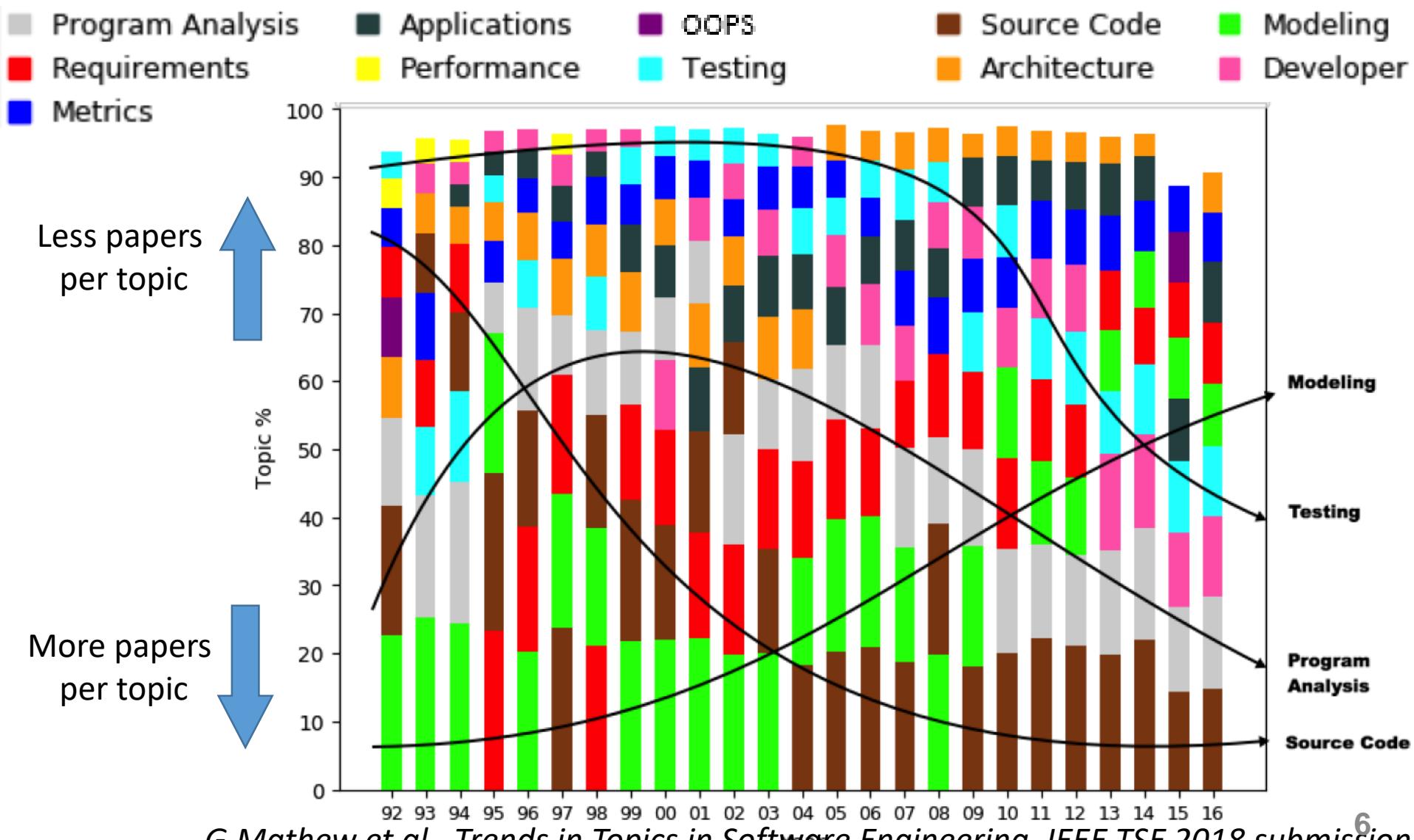
- SW verification and testing market: 19.3 Million USD @ 2015, annual growth: **15%** (expected) [IDC]
- 31% of total expenses of IT companies is due to QA and SW testing, increasing to **40%** (expected) [World Quality Report 2016-2017]



# Size and Complexity of Modern SW



# SE Research Topic Trends among 11 Major Topics (1992-2016)



# Limitations of the Conventional Quality Assurance Techniques

- Most QA techniques in industry practice target **easy-to-detect bugs at low cost** (i.e., light-weight approaches)
  - Secure coding rule checkers:
    - MISRA C, CERT C Coding standard, CERT Oracle secure coding standard
  - Static analyzer:
    - Coverity, Sparrow, Code sonar, Findbugs
  - Various random + heuristic test case generation techniques
    - Suresoft codescroll
- Such techniques often fail to detect **hard-to-detect corner case bugs** because
  - These techniques focus to analyze the **syntax** (i.e., pattern/structure) of a target program
  - However, the difficulty/complexity is caused by the **semantics** (i.e., meaning) of a target program.

# SOFTWARE CAUSES OF MEMORY CORRUPTION

Type of Software Defect	Causes Memory Corruption?	Defect in 2005 Camry L4?
Buffer Overflow	Yes	Yes
Invalid Pointer Dereference/Arithmetic	Yes	Yes
Race Condition (a.k.a., “Task Interference”)	Yes	Yes
Nested Scheduler Unlock	Yes	Yes
Unsafe Casting	Yes	Yes
Stack Overflow	Yes	Yes

Static analysis falls short of detecting ⇒ Systematic and dynamic analysis such complex bugs accurately is MUST for high quality SW

- High false negatives
- High false positives

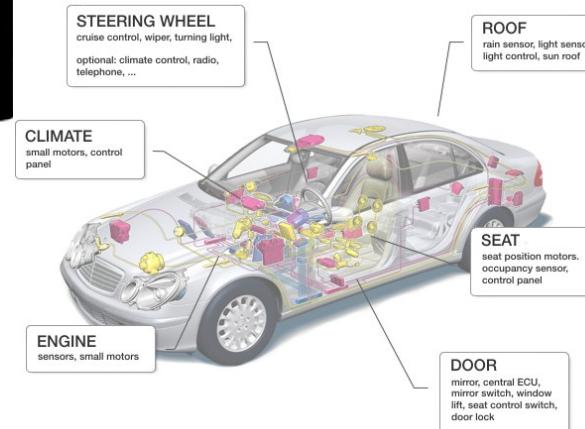
# Significance of Automated SW Analysis

- Software has become more ubiquitous and more complex at the same time
- Human resources are becoming less reliable and more expensive for testing highly complex software systems
- Computing resources are becoming **ubiquitous and free**
  - Tencent @ China provides 10TB storage **free**
  - Amazon AWS price: you can use thousands of CPUs at 0.05 \$/hr for 3.2Ghz Quad-core CPU
- To-do:
  - To develop automated and scientific software analysis tools to utilize computing resource effectively and efficiently

# Strong IT Industry in South Korea



**KIA MOTORS**



**LG**

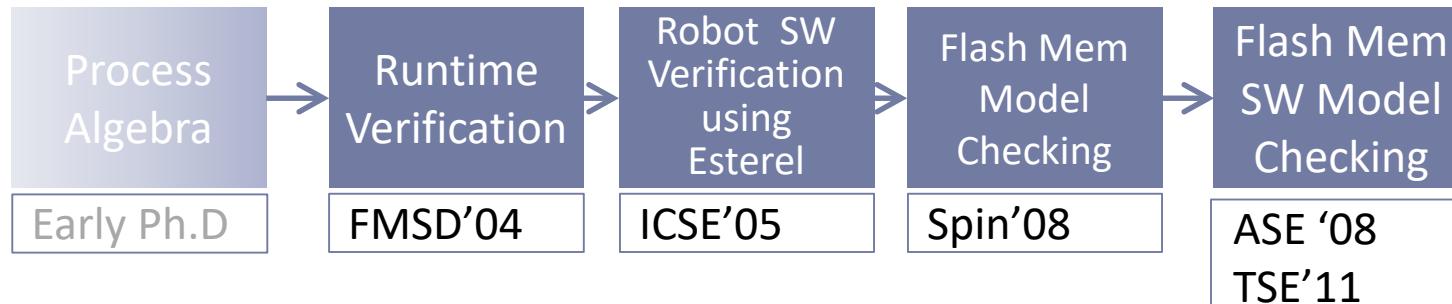
**MOBIS**



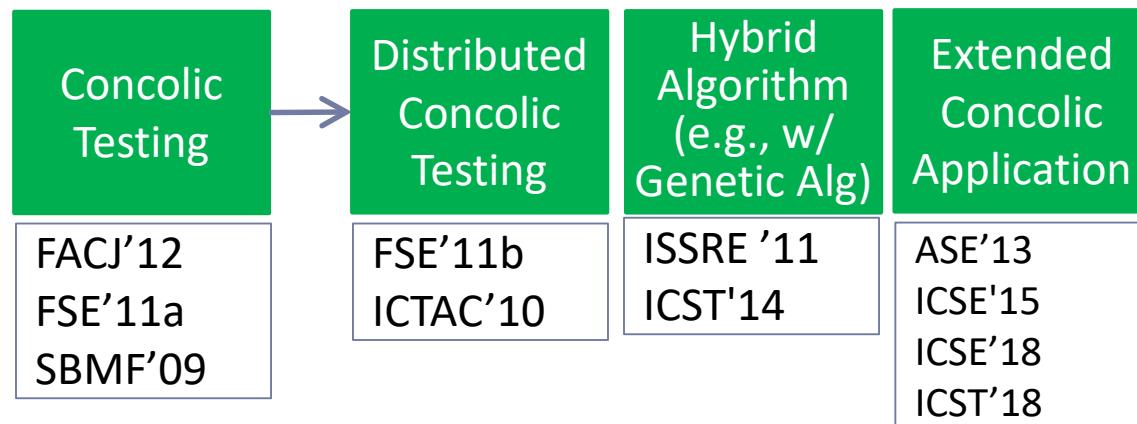
**HYUNDAI**

# Personal Research Roadmap

## ■ Past: RV (dynamic) && MC (static)



## ■ Current: Concolic Testing (Dynamic Symbolic Exec.)



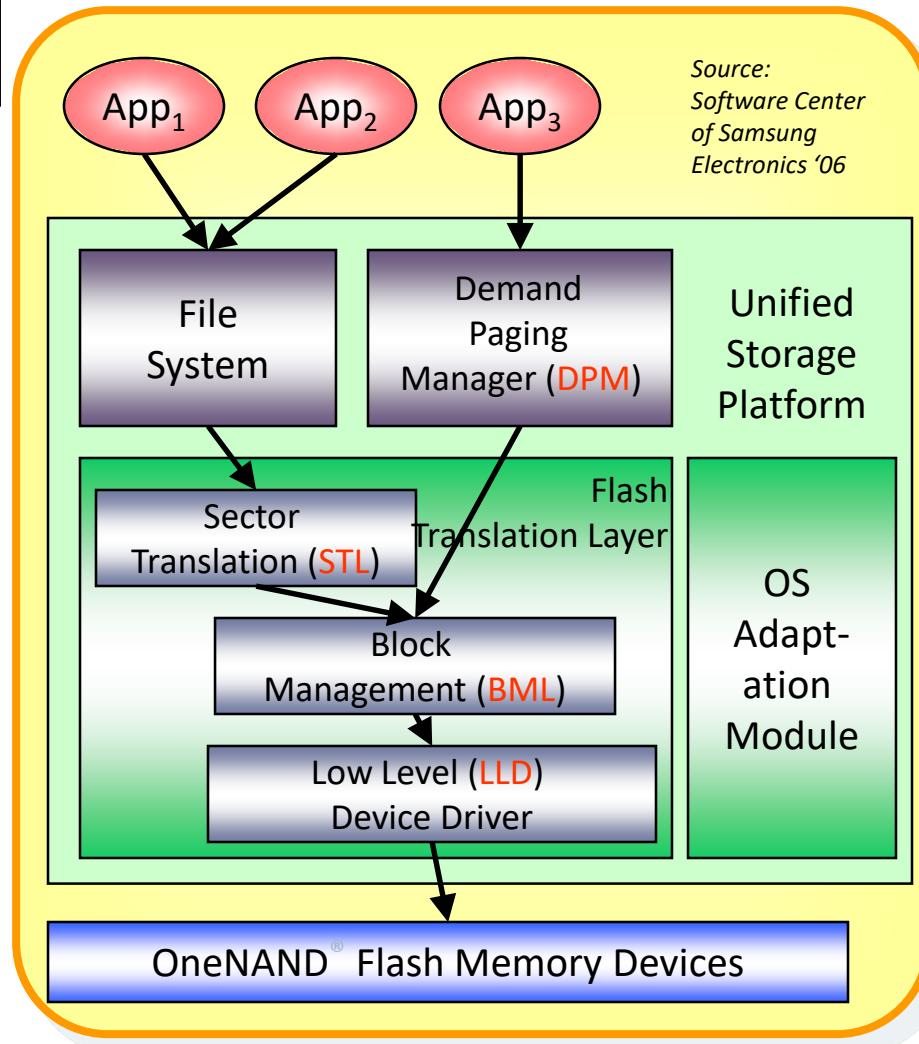
## ■ Future: Concolic Testing with Intelligence



# Part II: Industrial Experience w/ Model Checking

Target system: Samsung Unified Storage Platform (USP) for OneNAND® flash memory (around 30K lines of C code)

- ▶ Characteristics of OneNAND® flash mem
  - ▶ Each memory cell can be written limited number of times only
    - ▶ Logical-to-physical sector mapping
    - ▶ Bad block management, wear-leveling, etc
  - ▶ Concurrent I/O operations
    - ▶ Synchronization among processes is crucial
  - ▶ XIP by emulating NOR interface through demand-paging scheme
    - ▶ binary execution has a highest priority
  - ▶ Performance enhancement
    - ▶ Multi-sector read/write
    - ▶ Asynchronous operations
    - ▶ Deferred operation result check



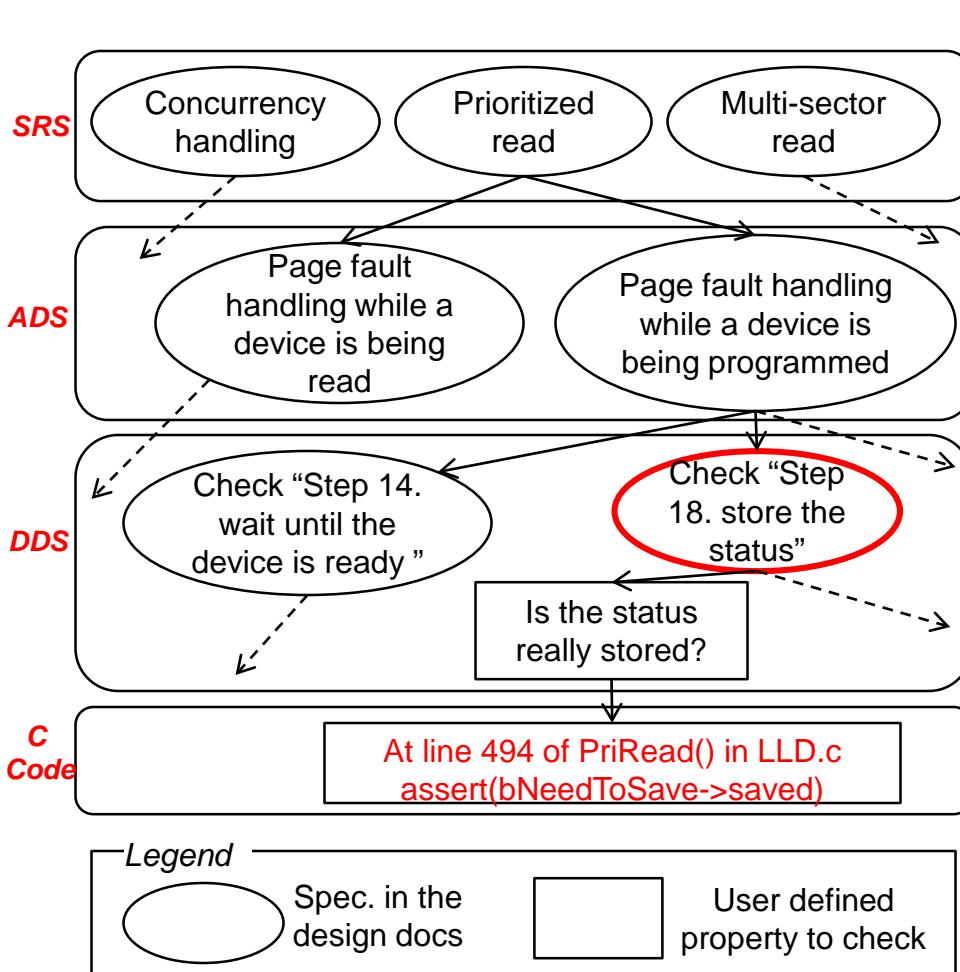
# Project Overview

- The goal of the project
  - To check whether USP conforms to the given high-level requirements
    - we needed to **identify** the code-level properties to check from the given high-level requirements
- A **top-down approach** to identify the code level properties from high-level requirements
  - USP has a set of elaborated design documents
    - Software requirement specification (SRS)
    - Architecture design specification (ADS)
    - Detailed design specification (DDS)
      - DPM, STL, BML, and LLD

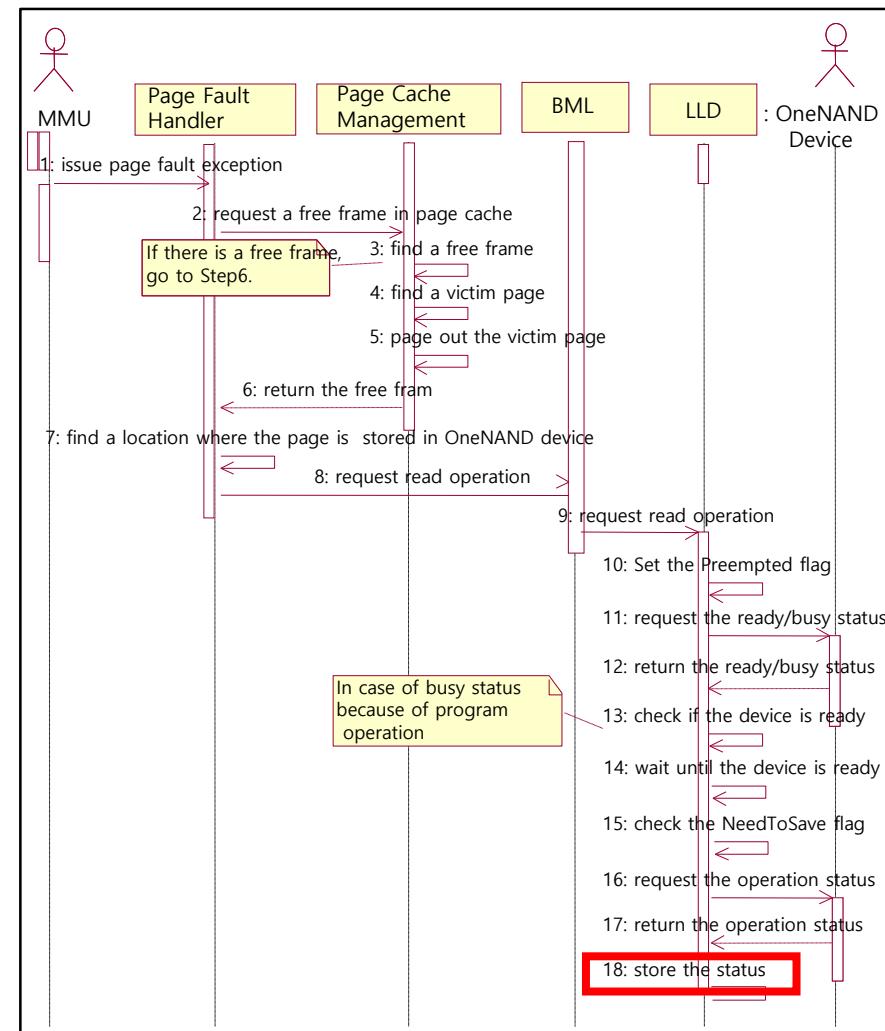
# Three High-level Requirements in SRS

- SRS specifies 13 functional requirements, 3 of which have “very high” priorities
  - Support prioritized read operation
    - To minimize the fault latency, USP should serve a read request from DPM prior to generic requests from a file system.
    - This prioritized read request can preempt a generic I/O operation and the preempted operation can be resumed later.
  - Concurrency handling
    - BML and LLD should avoid a race condition or deadlock through synchronization mechanisms such as semaphores and locks.
  - Manage sectors
    - STL provides logical-to-physical mapping, i.e. multiple logical sectors written over the distributed physical sectors should be read back correctly.

# Top-down Approach to Identify Code-level Property



- Total 43 code-level properties are identified



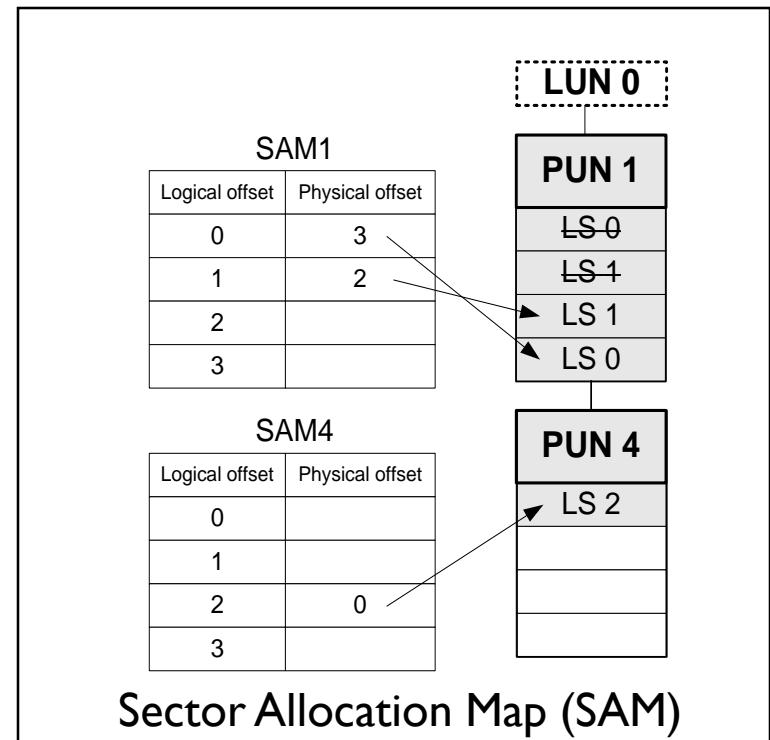
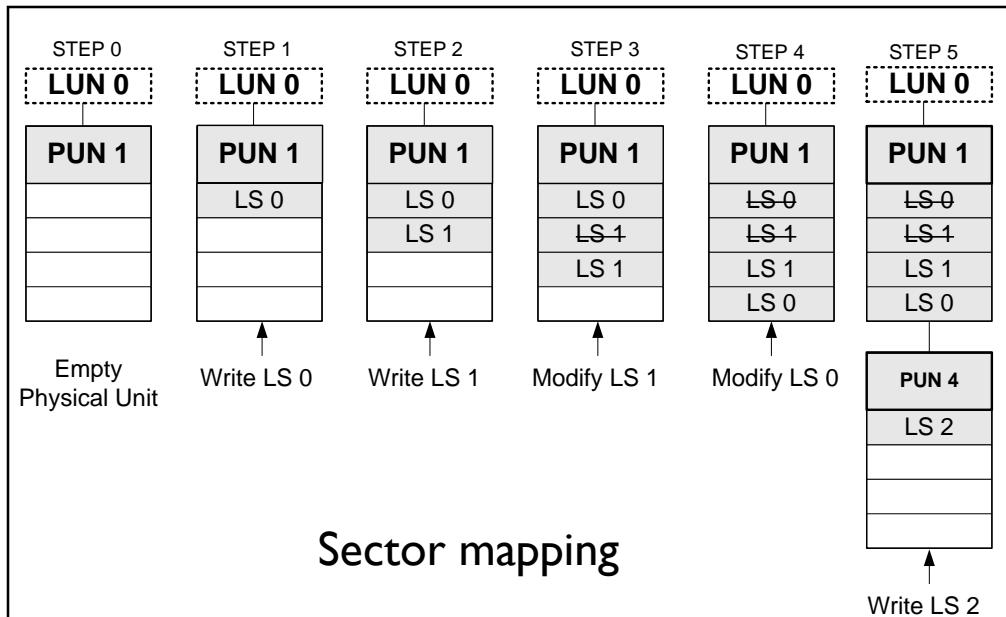
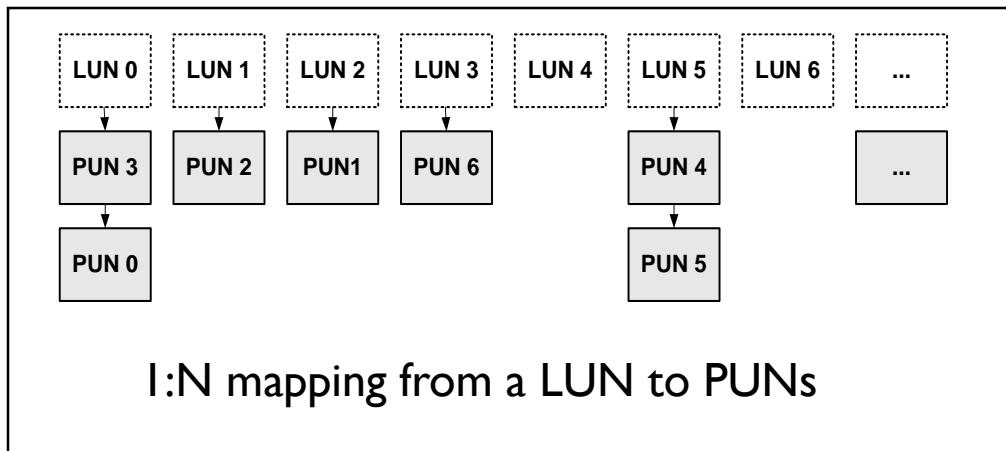
A sequence diagram of page fault handling while a device is being programmed in LLD DDS

# Results of Applying CBMC and BLAST [TSE'11]

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- ▶ Demand paging manager (234 LOC)
  - ▶ Detected a bug of not saving the status of suspended erase operation
- ▶ Concurrency handling
  - ▶ Confirmed that the BML semaphore was used correctly in all 14 BML functions (150 LOC on average)
  - ▶ Detected a bug of ignoring BML semaphore exceptions in a call sequence from STL (2500 LOC on average)
- ▶ Multi-sector read operation (MSR) (157 LOC)
  - ▶ Provided high assurance on the correctness of MSR
    - ▶ no violation was detected even after exhaustive analysis (at least with a small number of physical units(~10))
  - ▶ In addition, we evaluated and compared pros and cons of CBMC and BLAST empirically

# Logical to Physical Sector Mapping



- In flash memory, logical data are distributed over physical sectors.

# Multi-sector Read Operation (MSR)

	SAM0~SAM4	PU0~PU4	SAM0~SAM4	PU0~PU4	SAM0~SAM4	PU0~PU4
Sector 0	1 0	E	3 3	B	0	E
Sector 1	1 1	AB F	0 2	D	1	F
Sector 2	2	C	3	F	AC	E
Sector 3	3	D	1		3	D

a) A distribution of "ABCDEF"    b) Another distribution of "ABCDEF"    c) **Invalid** distribution of "ABCDEF"

- ▶ MSR reads adjacent multiple physical sectors once in order to improve read speed
  - ▶ MSR is 157 lines long, but highly complex due to its 4 level loops
  - ▶ 4 parameters to specify logical data to read (from, to, how long, read flag )
- ▶ The requirement property is to check
  - ▶  $\text{after\_MSR} \rightarrow (\forall i. \text{logical\_sectors}[i] == \text{buf}[i])$
- ▶ We built a **verification environment model** for MSR

# Environment Modeling

1. One PU is mapped to at most one LU
2. Valid correspondence between SAMs and PUs:

If the  $i$  th LS is written in the  $k$  th sector of the  $j$  th PU, then the  $i$  th offset of the  $j$  th SAM is valid and indicates the  $k$ 'th PS ,

Ex>      3<sup>rd</sup> LS ('C') is in the 3<sup>rd</sup> sector of the 2<sup>nd</sup> PU, then SAM1[2] ==2

$$i=2 \quad k=2 \quad j=1$$

3. For one LS, there exists only one PS that contains the value of the LS:

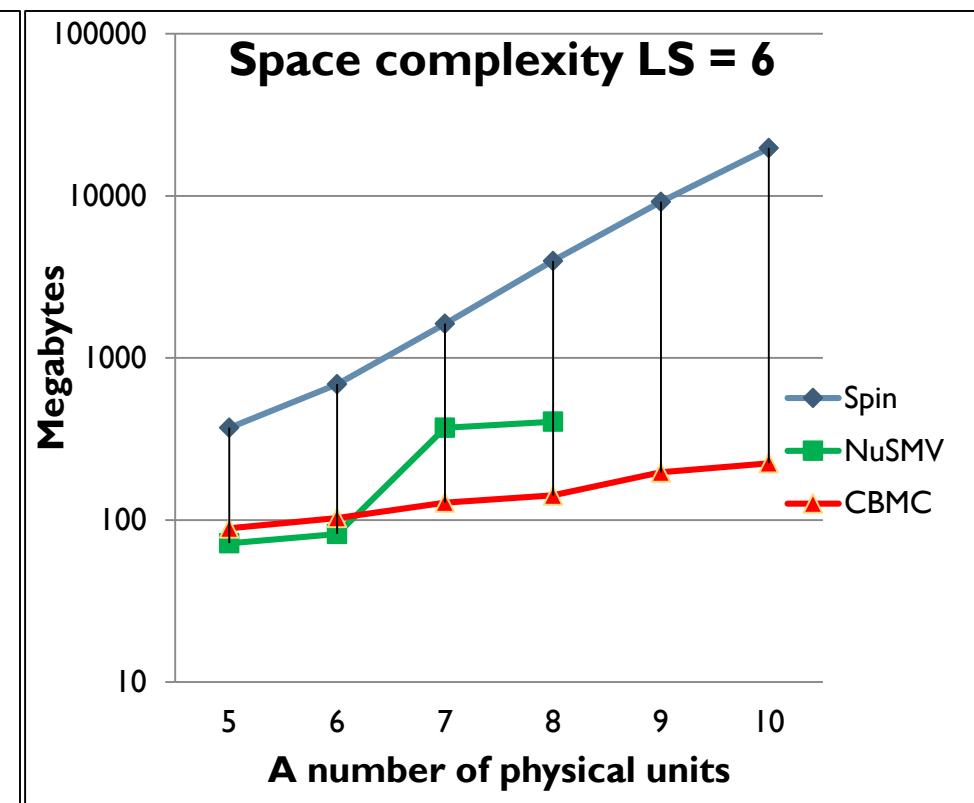
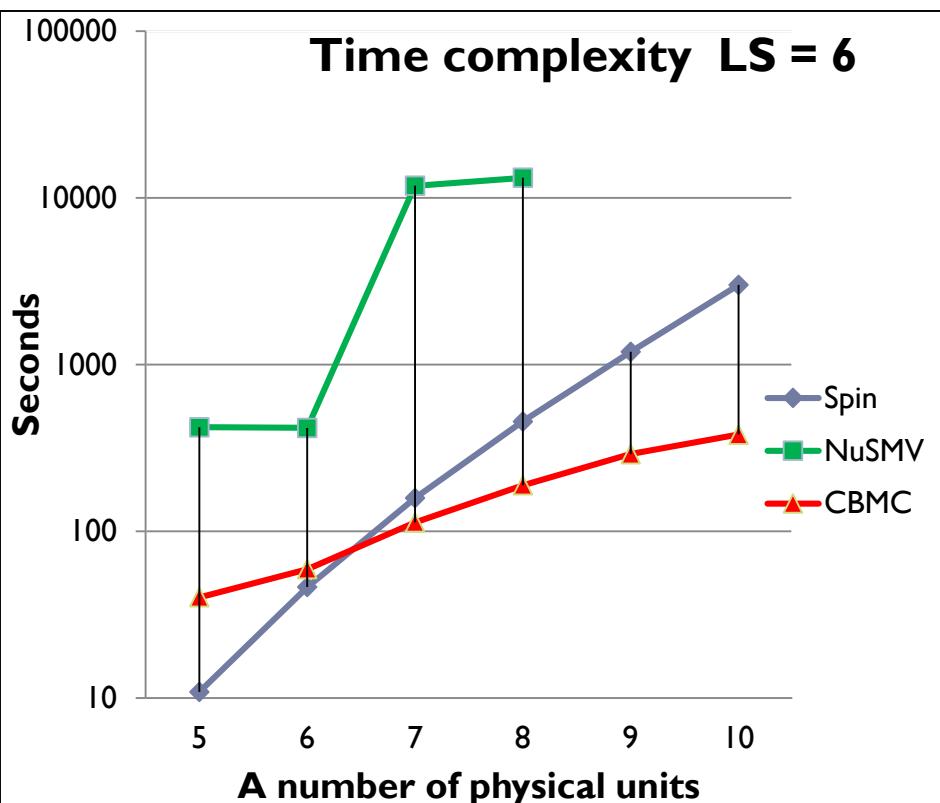
The PS number of the  $i$  th LS must be written in only one of the  $(i \bmod 4)$  th offsets of the SAM tables for the PUs mapped to the corresponding LU.

$$\forall i, j, k (LS[i] = PU[j].sect[k] \rightarrow (SAM[j].valid[i \bmod m] = true \& SAM[j].offset[i \bmod m] = k \& \forall p. (SAM[p].valid[i \bmod m] = false) \text{ where } p \neq j \text{ and } PU[p] \text{ is mapped to } \lfloor \frac{i}{m} \rfloor_{th} LU))$$

	SAM0~SAM4				PU0~PU4	
	Sector 0	Sector 1	Sector 2	Sector 3		
1		0				E
	1		1		AB	F
2					C	
		3			D	

# Model Checking Results of MSR [Spin'08]

- ▶ Verification of MSR by using NuSMV, Spin, and CBMC
- ▶ No violation was detected within  $|LS| \leq 8$ ,  $|PU| \leq 10$ 
  - ▶  $10^{10}$  configurations were exhaustively analyzed for  $|LS|=8$ ,  $|PU|=10$



# Feedbacks from Samsung Electronics

Main challenge :

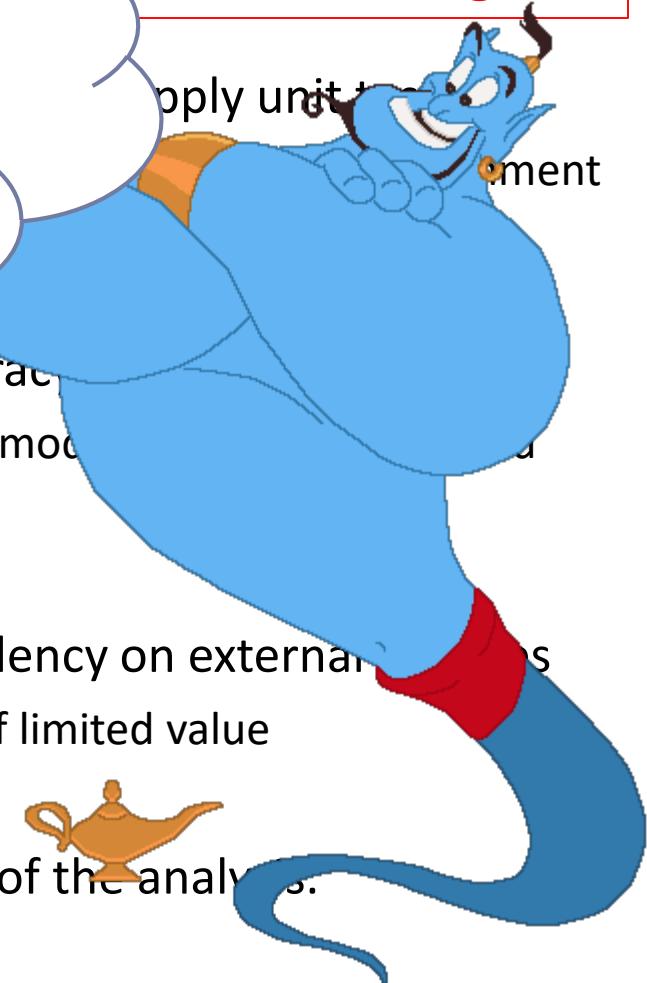
- IT industry

## Concolic testing

can resolve most  
of the problems 🎶

Unit testing

1. Current mode
  - ▶ Tight mode
2. Needs large scalability even at the cost of accuracy
  - ▶ Rigorous automated tools for small unit (i.e., SW module) have limited practical value
3. Many embedded SW components have dependency on external resources
  - ▶ Pure analysis methods on source code only are of limited value
4. It is desirable to generate test cases as a result of the analysis.
  - ▶ Current SW V&V practice operates on test cases

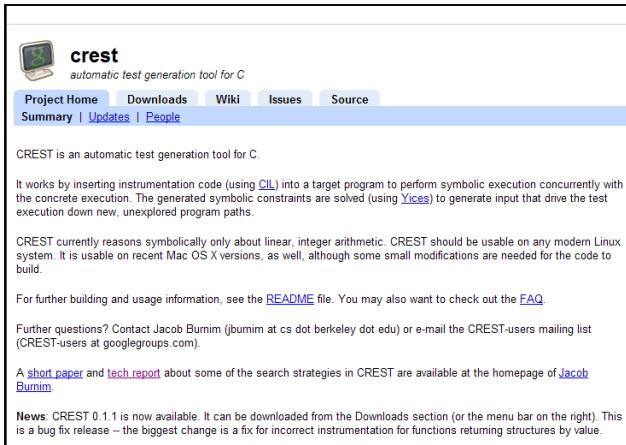


# Background on Concolic Testing

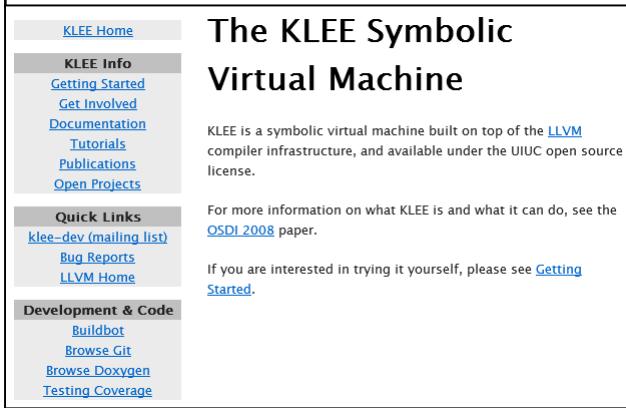
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- ▶ **Concrete runtime execution guides symbolic path analysis**
  - ▶ a.k.a. dynamic symbolic execution (DSE), white-box fuzzing
- ▶ **Automated test case (TC) generation technique**
  - ▶ Applicable to a large target program (no memory bottleneck)
  - ▶ Applicable to testing stages seamlessly
  - ▶ External binary library can be handled (partially)
- ▶ **Explicit path model checker**
  - ▶ All possible execution paths are explored based on the generated TCs
  - ▶ Anytime algorithm
    - ▶ User can get partial analysis result (i.e., TCs) anytime
  - ▶ Analysis of each path is independent from each other
    - ▶ Parallelization for linear speed up
    - ▶ Ex. Scalable CONcolic testing for Reliable Embedded Software (SCORE) on thousands of Amazon EC2 cloud computing nodes [FSE'11b]

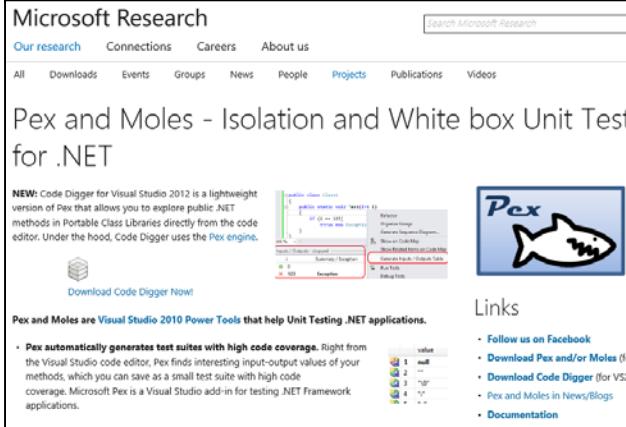
# Concolic Testing Tools



The screenshot shows the GitHub project page for 'crest'. It features a logo of a book with a gear, the name 'crest' in bold, and a subtitle 'automatic test generation tool for C'. Below this is a navigation bar with links for 'Project Home', 'Downloads', 'Wiki', 'Issues', and 'Source'. Under 'Project Home', there are links for 'Summary', 'Updates', and 'People'. The main content area contains text about CREST's purpose (generating symbolic constraints from concrete execution), its current limitations (only linear integer arithmetic), and its compatibility with various Linux and Mac OS X versions. It also includes links to the README file, FAQ, and mailing list.



The screenshot shows the GitHub project page for 'KLEE'. It has a sidebar with links for 'KLEE Home', 'KLEE Info' (including 'Getting Started', 'Get Involved', 'Documentation', 'Tutorials', 'Publications', and 'Open Projects'), 'Quick Links' (including 'klee-dev (mailing list)', 'Bug Reports', 'LLVM Home'), and 'Development & Code' (including 'Buildbot', 'Browse Git', 'Browse Doxygen', and 'Testing Coverage'). The main content area is titled 'The KLEE Symbolic Virtual Machine' and explains that KLEE is a symbolic virtual machine built on LLVM. It provides links to the OSDI 2008 paper and the 'Getting Started' guide.



The screenshot shows the Microsoft Research page for 'Pex and Moles - Isolation and White box Unit Test for .NET'. It includes a search bar, a navigation bar with links for 'Our research', 'Connections', 'Careers', 'About us', and a menu bar with 'All', 'Downloads', 'Events', 'Groups', 'News', 'People', 'Projects', 'Publications', and 'Videos'. Below this is a section titled 'Pex and Moles - Isolation and White box Unit Test for .NET' with a brief description and a screenshot of the Visual Studio interface showing code coverage analysis. A 'Download Code Digger Now!' button is also present.

- **CROWN (open source)**
  - Target: C
  - Instrumentation based extraction
  - BV supported
  - <https://github.com/swtv-kaist/CROWN>
- **KLEE (open source)**
  - Target: LLVM
  - VM based symbolic formula extraction
  - BV supported
  - Symbolic POSIX library supported
  - <http://ccadar.github.io/klee/>
- **PEX (IntelliTest incorporated in Visual Studio 2015)**
  - Target: C#
  - VM based symbolic formula extraction
  - BV supported
  - Integrated with Visual Studio
  - <http://research.microsoft.com/en-us/projects/pex/>
- **CATG (open source)**
  - Target: Java
  - Trace/log based symbolic formula extraction
  - LIA supported

# Part III. Industrial Experience w/ Concolic Testing

## ▶ System level testing

1. Samsung Linux Platform (SLP) file manager [FSE'11]
  - ▶ Covered 20% of the branches and detected an infinite loop bug
2. 10 Busybox utilities
  - ▶ Covered 80% of the branches with 4 different search strategy and 10,000 TCs in 20 min each (a buffer overflow bug in grep was detected)
3. Libexif [ICSE'12]
  - ▶ Covered 43% of the branches with 4 different search strategy and 10,000 TCs in 8 hours each
  - ▶ 2 null pointer dereferences and 5 divide-by-0 bugs were detected
  - ▶ Reported 2 security bugs to Common Vulnerability Exposure (CVE)
4. Failure to control LG home appliances [ICSE'2015 SEIP]
5. Hyundai automotive software (2015- 2017) : inconsistency between spec. and impl. found

## ▶ Unit-level testing

1. Busybox ls (1100 LOC) [ICST'12]: 98% of branches covered and 4 bugs detected
2. Samsung security library (2300 LOC) [ICST'12]
  - ▶ 73% of branches covered and a memory violation bug detected
3. CONcrete and symBOLic (CONBOL) framework [ASE'13]
  - ▶ **Detected 24 crash bugs in 4 MLOC embedded program**
  - ▶ **Detected 6 crash bugs in 0.2 MLOC in another embedded program**
4. Automated unit testing framework for Hyundai Mobis automotive software (2017 - now):
  - ▶ reducing manual testing time more than 50% (= 0.5 million USD per year @ Mobis India) [ICSE'19 submitted]

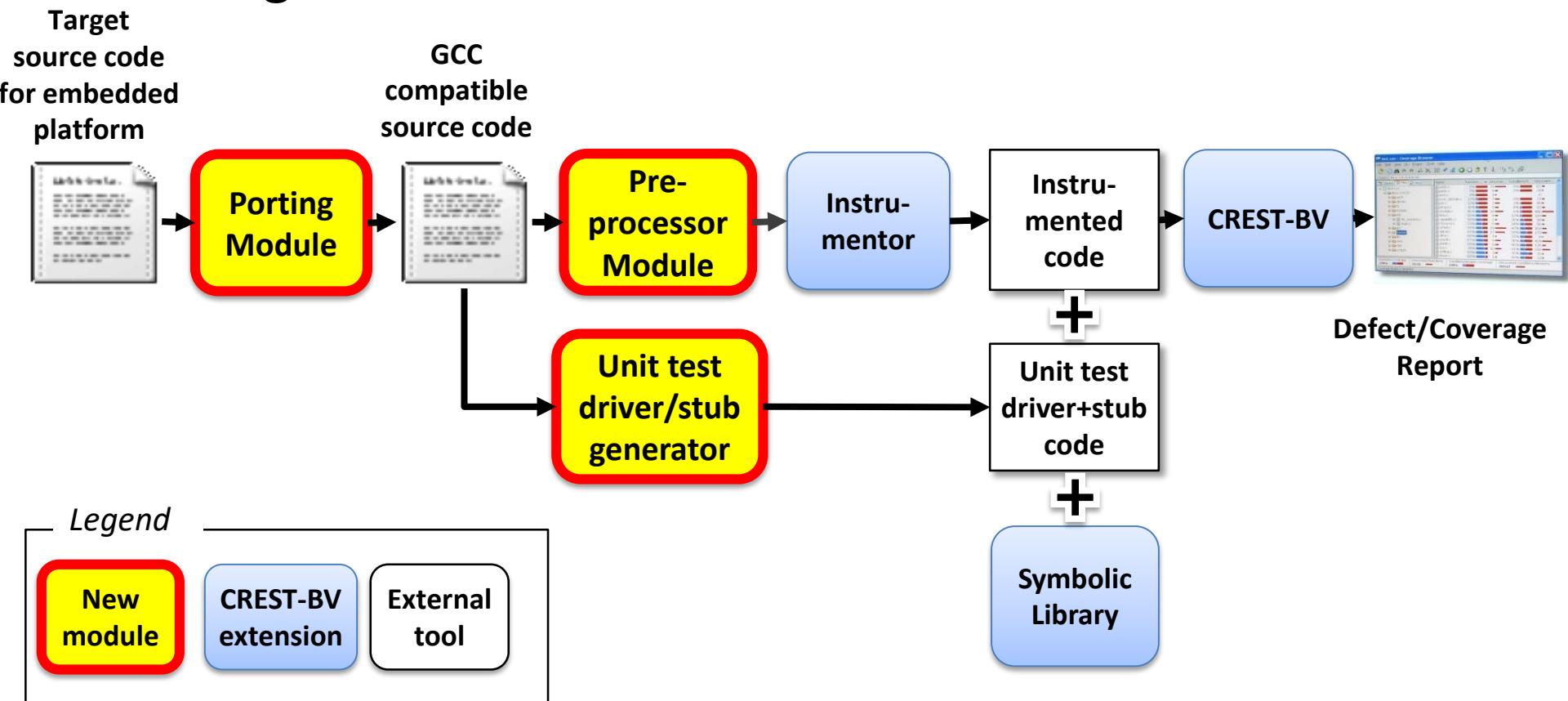
# Summary of the Case Study

- Embedded SW is becoming larger and more complex
  - Ex. Android: 12 MLOC, Tizen > 6 MLOC
- Smartphone development period is very short
  - No time to manually test smartphones sufficiently
- Solution: **Automated unit test generation** for industrial embedded SW using **CONBOL** (CONcrete and symBOLic testing)
  - CONBOL automatically generates unit-test driver/stubs
  - CONBOL automatically generates test cases using concolic testing
  - CONBOL targets crash bugs (i.e. null pointer dereference, etc.)
- CONBOL detected **24 crash bugs** in 4 MLOC Android SW in 16 hours



# Overview of CONBOL

- We have developed the CONcrete and symBOLic (CONBOL) framework: an automated concolic unit testing tool based-on CREST-BV for embedded SW



# Unit Test Driver/Stub Generator(1/2)

- The unit test driver/stub generator **automatically generates unit test driver/stub** functions for unit testing of a target function
  - A unit test driver symbolically sets all visible global variables and parameters of the target function

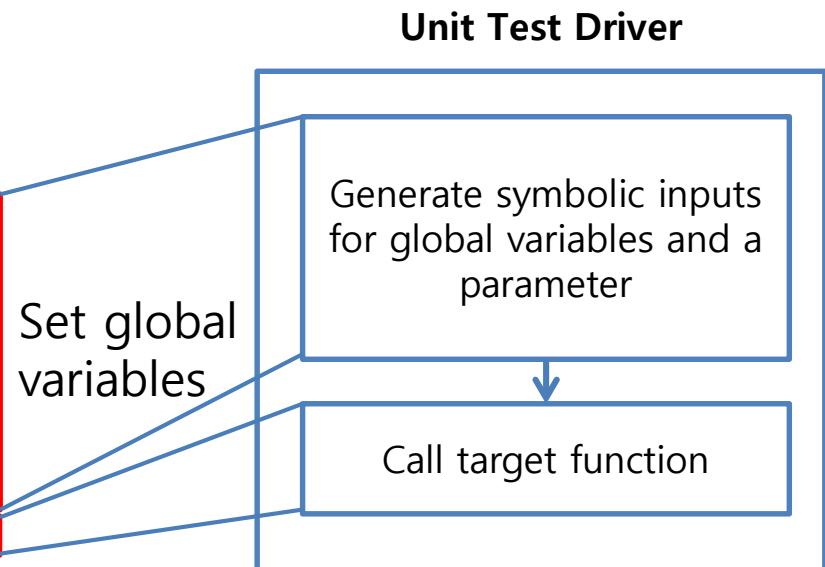
Type	Description	Code Example
Primitive	set a corresponding symbolic value	<code>int a; SYM_int(a);</code>
Array	set a fixed number of elements	<code>int a[3]; SYM_int(a[0]); ... SYM_int(a[2]);</code>
Structure	set NULL to all pointer fields and set symbolic value to all primitive fields	<code>struct _st{int n,struct _st*p}a; SYM_int(a.n); a.p=NULL;</code>
Pointer	allocate memory for a pointee and set a symbolic value of corresponding type of the pointee	<code>int *a; a = malloc(sizeof(int)); SYM_int(*a);</code>

- The test driver/stub generator replaces sub-functions invoked by the target function with symbolic stub functions

# Unit Test Driver/Stub Generator(2/2)

- Example of an automatically generated unit-test driver

```
01:typedef struct Node_{
02:    char c;
03:    struct Node_ *next;
04:} Node;
05:Node *head;
06:// Target unit-under-test
07:void add_last(char v){
08:    // add a new node containing v
09:    // to the end of the linked list
10:    ...
11:// Test driver for the target unit
12:void test_add_last(){
13:    char v1;
14:    head = malloc(sizeof(Node));
15:    SYM_char(head->c);
16:    head->next = NULL;
17:    SYM_char(v1);    } Set parameter
18:    add_last(v1); }
```



# Statistics of Project S

- Project S, our target program, is an industrial embedded software for smartphones developed by Samsung Electronics
  - Project S targets ARM platforms

Metric	Data
Total lines of code	About 4,000,000
# of branches	397,854
# of functions	Total
	Having more than one branch
# of files	Sources
	Headers

# Test Experiment Setting

- CONBOL uses a DFS strategy used by CREST-BV in Kim et al. [ICSE12 SEIP]
- Termination criteria and timeout setting
  - Concolic unit testing of a target function terminates when
    - CONBOL detect a violation of an assertion, or
    - All possible execution paths are explored, or
    - Concolic unit testing spends 30 seconds (Timeout1)
  - In addition, a single test execution of a target unit should not spend more than 15 seconds (Timeout2)
- HW setting
  - Intel i5 3570K @ 3.4 GHz, 4GB RAM running Debian Linux 6.0.4 32bit

# Results (1/2)

- Results of branch coverage and time cost
  - CONBOL tested **86.7% (=25,425)** of target functions on a host PC
    - 13.3% of functions were not inherently portable to a host PC due to inline ARM assembly, direct memory access, etc
  - CONBOL covered **59.6%** of branches in **15.8 hours**

Statistics	Number
Total # of test cases generated	About 800,000
Branch coverage (%)	59.6
Execution time (hour)	15.8
# of functions reaching timtout1 (30s)	742
# of functions reaching timtout2 (15s)	134
Execution time w/o timeout (hour)	9.0

# Results (2/2)

- CONBOL raised 277 alarms
- 2 Samsung engineers (w/o prior knowledge on the target program) took 1 week to remove 227 false alarms out of 277 alarms
  - We reported 50 alarms and **24 crash bugs** were confirmed by the developers of Project S
- Pre-conditions and scoring rules filtered out **14.1% and 81.2%** of likely false alarms, respectively
- Note that Coverity prevent could **not** detect any of these crash bugs

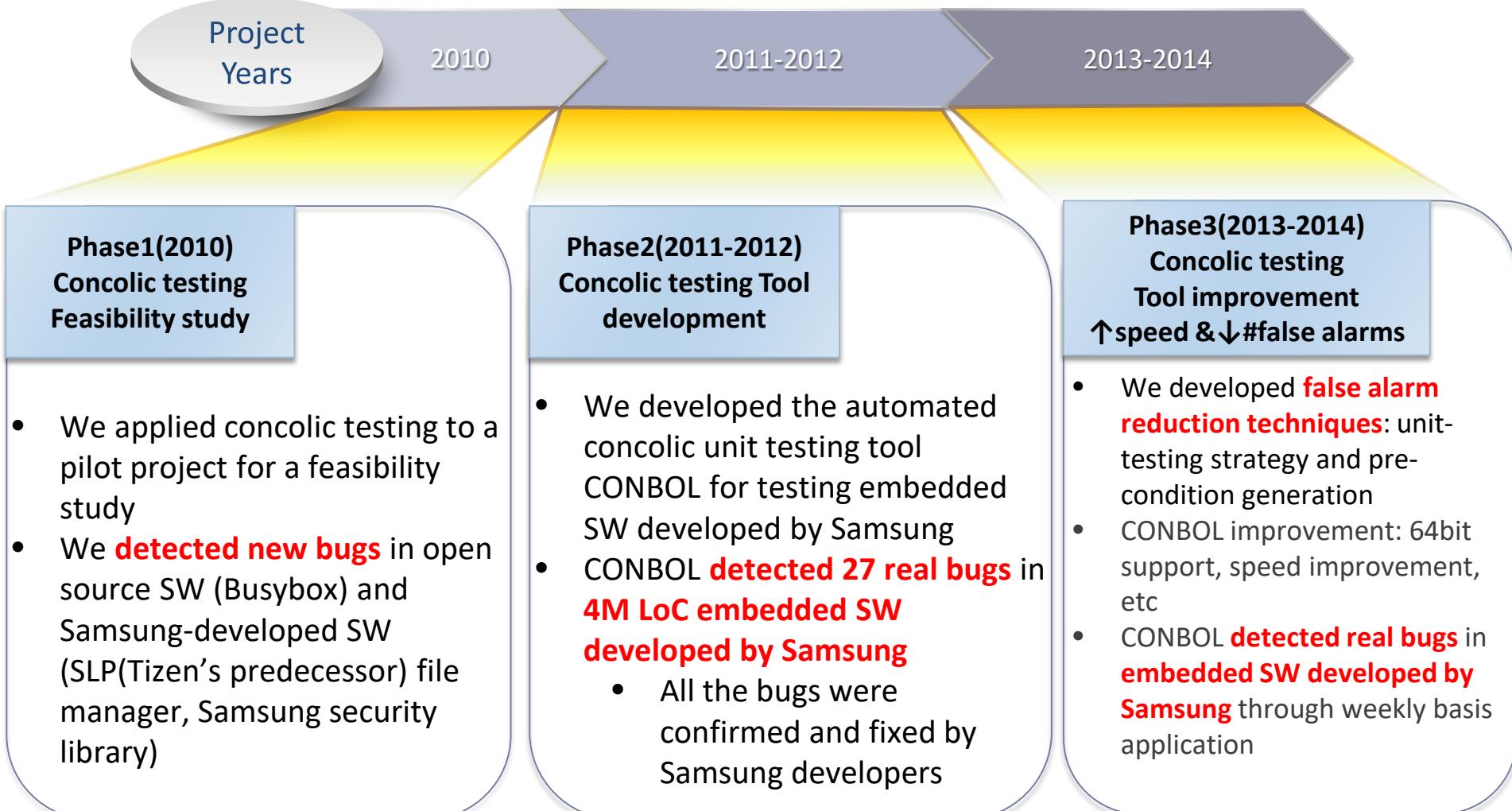
# of reported alarms	Out-of-bound		NULL-pointer-dereference		Divide-by-zero		Total	
	# of alarms	Ratio (%)	# of alarms	Ratio (%)	# of alarms	Ratio (%)	# of alarms	Ratio (%)
W/O any heuristics	3235	100.0	2588	100.0	61	100.0	5884	100.0
W/ inserted pre-conditions	2486	76.8	2511	97.0	58	95.1	5055	85.9
W/ inserted pre-conditions + scoring rules	220	6.8	42	1.6	15	24.6	277	4.7
<b>Confirmed and fixed bugs</b>	<b>13</b>	<b>0.4</b>	<b>5</b>	<b>0.2</b>	<b>6</b>	<b>9.8</b>	<b>24</b>	<b>0.4</b>

# Concolic Testing w/ Samsung for 5 Years

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- ▶ Goal: Developing **automated test generation technique** based on concolic testing to **effectively detect bugs** in **embedded C programs** developed by Samsung
- ▶ Project period: 2010 ~ 2014
- ▶ Outcome:
  - ▶ Tool development: We have developed the concolic unit testing tool CONBOL to **automatically detect bugs** in **embedded C programs**
    - ▶ CONBOL has detected more than **100 real crash bugs** in 4M LoC embedded software developed by Samsung and 0.2M LoC open-source C program
    - ▶ Publications: We have published **4 papers** to prestigious SE conferences: **ICSE 2012, FSE 2011, ASE 2013, and ICST 2012**

# Industrial Achievement from the Project

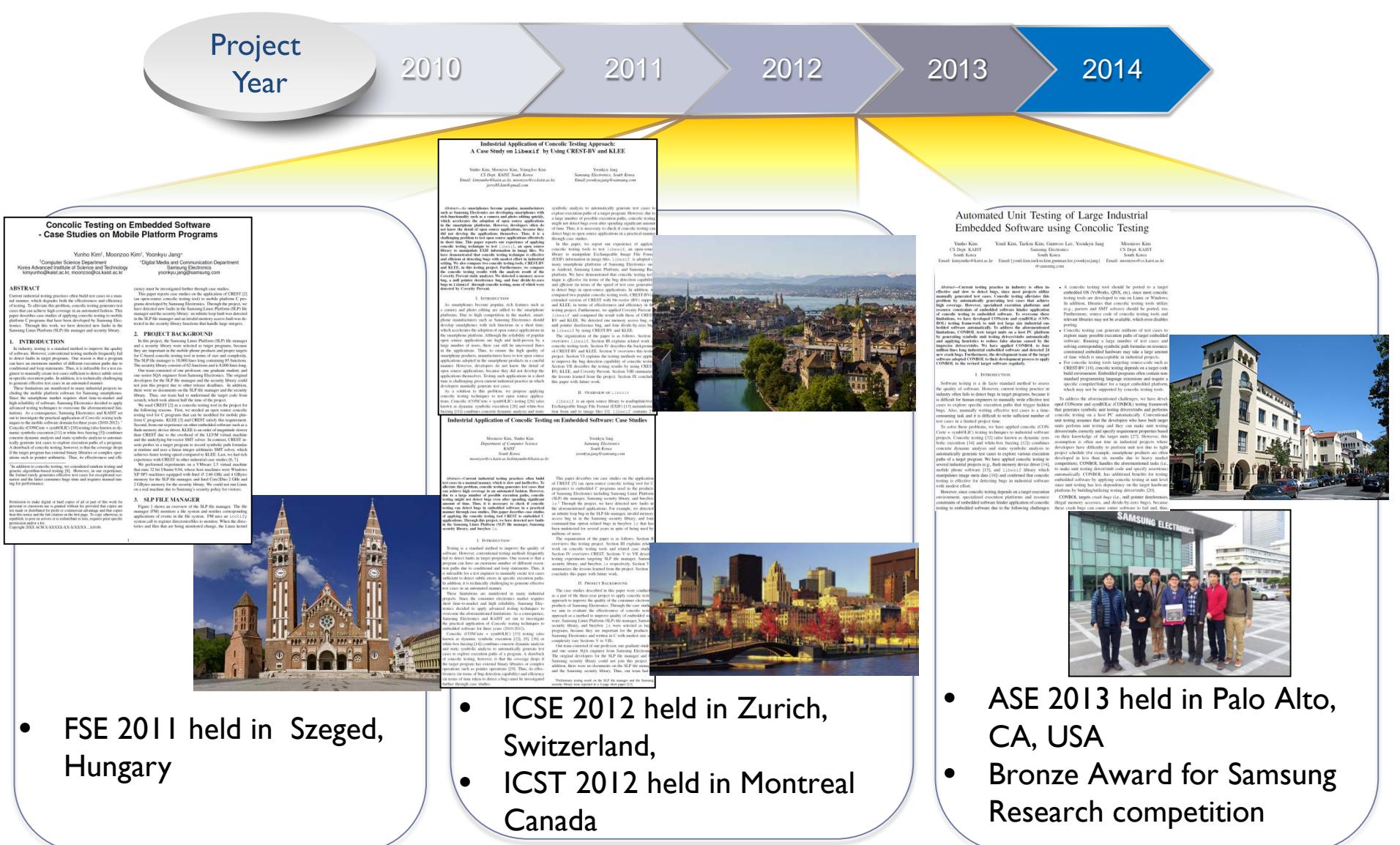


# Success of CONBOL at Samsung Electronics



- ▶ Bronze Award at Samsung Best Paper Award
- ▶ Oct's Best Practice Award
- ▶ Team leader Dr. Yoonkyu Jang received Samsung Award of Honor

# Academic Achievement from the Project



- FSE 2011 held in Szeged, Hungary

- ICSE 2012 held in Zurich, Switzerland,
  - ICST 2012 held in Montreal Canada

- ASE 2013 held in Palo Alto, CA, USA
  - Bronze Award for Samsung Research competition

# 현대모비스, AI 기반 소프트웨어 검증시스템 도입..."효율 2배로"

2018-07-22 10:00

댓글 f TALK ...

가- 가+

'마이스트' 적용...대화형 검색 로봇 '마이봇'도 도입

(서울=연합뉴스) 윤보람 기자 = 현대모비스[012330]가 인공지능(AI)을 활용해 자율주행, 커넥티비티(연결성) 등 미래 자동차 소프트웨어(SW) 개발에 속도를 낸다.

현대모비스는 AI를 기반으로 하는 소프트웨어 검증시스템 '마이스트'(MAIST: Mobis Artificial Intelligence Software Testing)를 최근 도입했다고 22일 밝혔다.

Hyundai Mobis and a research team lead by Prof. Moonzoo Kim at KAIST jointly developed MAIST for automated testing

MAIST automates unit coverage testing performed by human engineers by applying concolic unit testing

실제 현대모비스가 통합형 차체제어시스템(IBU)과 써라

MAIST can reduce 53% and 70% of manual testing effort for IBU(Integrated Body Unit) and SVM(Surround View Monitoring)

현대모비스는 하반기부터 소프트웨어가 탑재되는 제동, 조향 등 모든 전장부품으로 마이스트를 확대 적용할 계획이다. 글로벌 소프트웨어 연구기지인 인도연구소에도 적용한다.

## ■ 현대모비스 인공지능 도입 사례

AI 시스템	목적	도입 효과
MAIST	소프트웨어 검증 자동화	IBU 53%
마이봇 (Mobis AI Robot)	소프트웨어 개발문서 검색	SVM 70%

Reduction of manual testing effort

딥러닝 기반, 개발문서 20만 건 관리

<http://m.yna.co.kr/kr/contents/?cid=AKR2018072015880003&mobile>

# Microsoft Project Springfield

- Azure-based cloud service to find security bugs in x86 windows binary
- Based on concolic testing techniques of SAGE



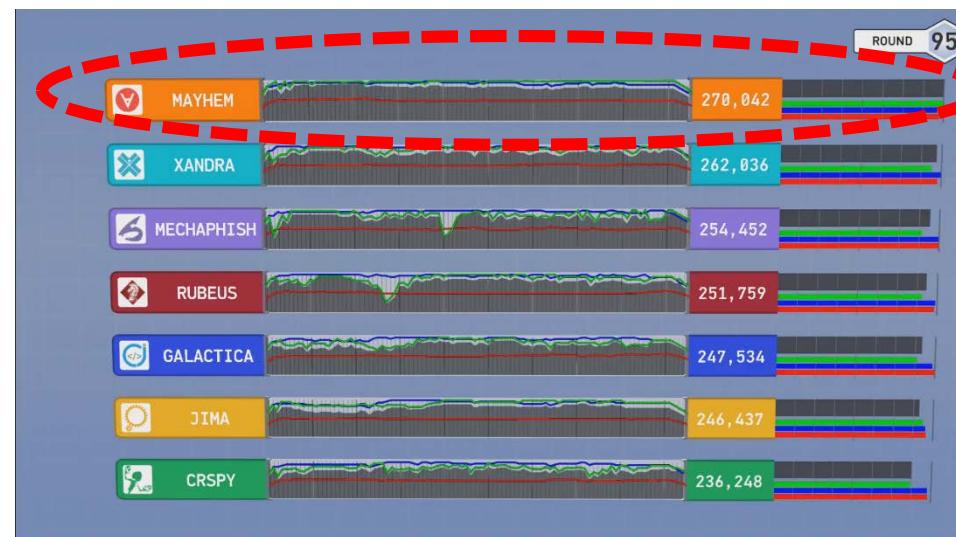
The landing page for Project Springfield features a blue header with the text "Project Springfield" and "Fuzz your code before hackers do". A "Sign up" button is located in the top-left corner. To the right is a large graphic of a shield with a lock, surrounded by arrows and a gear, symbolizing protection and security. Below the header, the text "What is Project Springfield?" is displayed, followed by a description: "Project Springfield is Microsoft's unique fuzz testing service for finding security critical bugs in software. Project Springfield helps customers quickly adopt practices and technology battle-tested over the last 15 years at Microsoft." The page also includes four icons: a dollar sign with wavy lines, a binary code grid, a cluster of squares, and two user profiles with a magnifying glass.

 <p>"Million Dollar" Bugs Project Springfield uses "Whitebox Fuzzing" technology which discovered 1/3rd of the "million dollar" security bugs during Windows 7 development.</p>	 <p>Battle tested tech The same state-of-the-art tools and practices used inside Microsoft to fuzz Windows and Office applications.</p>	 <p>Fast, Consistent Roll-out Project Springfield provides the platform to ensure systematic security risk assessment and testing consistency.</p>	 <p>Available now Enterprise customers are currently using Project Springfield to find and fix critical security issues. <a href="#">See examples &gt;</a></p>
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# 2016 Aug DARPA Cyber Grand Challenge

-the world's 1<sup>st</sup> all-machine hacking tournament

- Each team's Cyber Reasoning System **automatically** identifies security flaws and applies patches to its own system in a hack-and-defend style contest targeting a new Linux-based OS DECREE
- Mayhem won the best score, which is CMU's concolic testing based tool

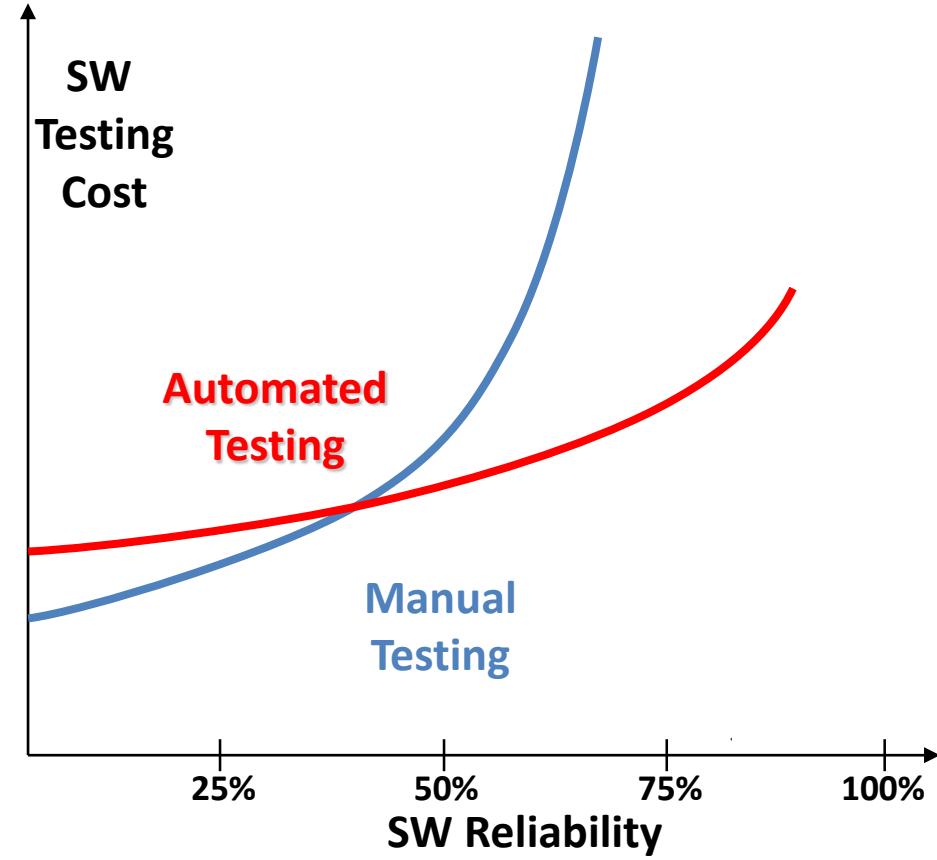


# Summary: Lessons Learned for Successful Industrial Application of Automated Analysis Technique

- ▶ Expect a large amount of manual work to understand and modify a target program and analysis tools
  - ▶ Field engineers may be too busy to explain a target program for you
    - ▶ Industrial software may not have good documents
- ▶ Be flexible for selecting target techniques to apply
  - ▶ Use appropriate techniques for the project, not the one you like
- ▶ Remote access right to target code is important
  - ▶ Due to IP issue, most companies are reluctant to give remote code access right.
- ▶ Expertise of field engineers in both target domain and the techniques is crucial

# Conclusion

- Formal verification techniques really work in industry !
  - Software model checking and concolic testing detected hidden bugs in industrial embedded software
- Concolic testing is an industry friendly model checking technique.
  - Concolic testing is effective and efficient for testing industrial embedded software
- Successful application of automated testing techniques still requires expertise of human engineers in the domain



## Traditional testing

- Manual TC gen
- Testing main scenarios
- System-level testing
- Small # of TCs



## Concolic testing

- Automated TC gen
- Testing exceptional scenarios
- Unit-level testing
- Large # of TCs